Course Code - CS223

Course Name - Digital Design

Section – 001

Lab Number – 04

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Date – 30/10/2023

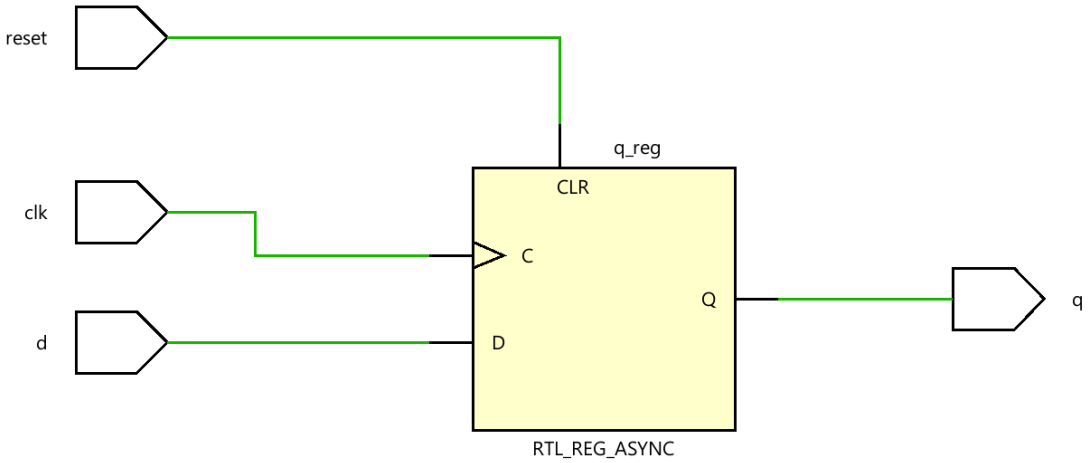
1. Resettable D Flip-Flop

```
1  `timescale 1ps / 1ps
2
3
4
5  module D_S_FF(input wire clk,
6   input wire reset,
7   input wire  d,
8   output reg q);
9
10  always_ff @(posedge clk, posedge reset)
11  if (reset) q <= 1'b0;
12  else q <= d;
13 endmodule
14
```

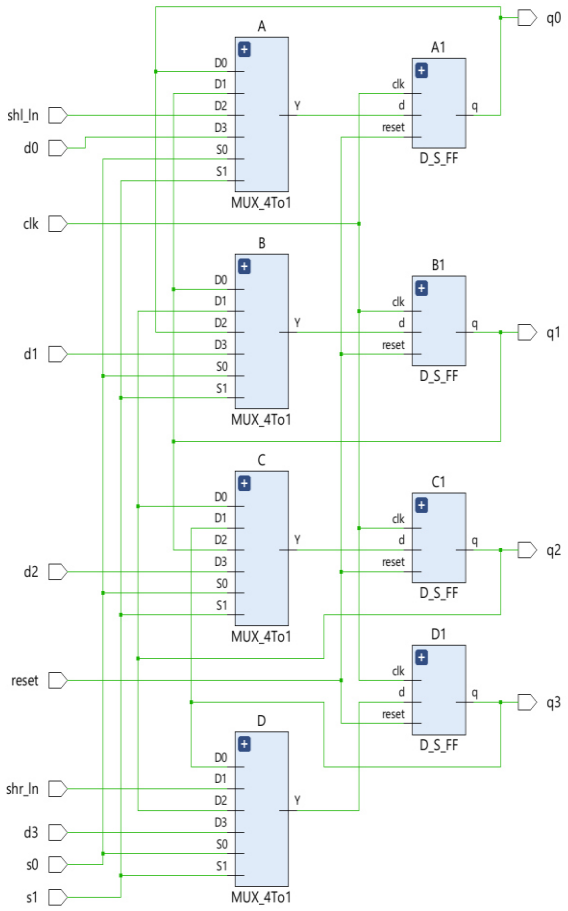
`timescale 1ps / 1ps

module D_S_FF(input wire clk,
 input wire reset,
 input wire d,
 output reg q);

 always_ff @(posedge clk, posedge reset)
 if (reset) q <= 1'b0;
 else q <= d;
endmodule



2. Circuit Schematic of Multi-Function Register



3. Structural System Verilog Module of Multi-Function Register

```
`timescale 1ps / 1ps
module MF_Register(input wire
d0,d1,d2,d3,s0,s1,shr_In,shl_In,reset,reg clk, output reg q0,q1,q2,q3);
reg w0,w1,w2,w3;
MUX_4To1 A(s1,s0,d0,shl_In,q1,q0,w0);
MUX_4To1 B(s1,s0,d1,q0,q2,q1,w1);
MUX_4To1 C(s1,s0,d2,q1,q3,q2,w2);
MUX_4To1 D(s1,s0,d3,q2,shr_In,q3,w3);
D_S_FF A1(clk,reset,w0,q0);
D_S_FF B1(clk,reset,w1,q1);
D_S_FF C1(clk,reset,w2,q2);
D_S_FF D1(clk,reset,w3,q3);

endmodule
```

4. Structural System Verilog Test-Bench for Multi-Function Register

```
`timescale 1ps / 1ps
module MF_Register_TB();
reg d0,d1,d2,d3,s0,s1,shr_In,shl_In,reset,clk;
wire q0,q1,q2,q3;
MF_Register test(d0,d1,d2,d3,s0,s1,shr_In,shl_In,reset,clk,q0,q1,q2,q3);
initial begin
    clk = 0;
    forever #10 clk = ~clk;
```

```
  end
 initial begin
 assign d0 = 1'b1; assign d1 = 1'b1; assign d2 = 1'b1; assign d3 = 1'b1;
assign shr_ln = 1'b1; assign shl_ln = 1'b0; #5;

assign  reset =1'b0; assign s1 = 1'b1; assign s0 = 1'b1; #10;
assign  reset =1'b1; #5;
assign  reset =1'b0; assign s1 = 1'b1; assign s0 = 1'b1; #10;
assign  reset =1'b0; assign s1 = 1'b0; assign s0 = 1'b0; #10;
assign  reset =1'b0; assign s1 = 1'b1; assign s0 = 1'b0; #10;
assign  reset =1'b0; assign s1 = 1'b0; assign s0 = 1'b1; #10;

$finish;

end

endmodule
```