Course Code - CS223

Course Name - Digital Design

Section – 001

Lab Number – 03

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1. Behavioural 2-to-4 decoder

```
1  `timescale 1ns / 1ps
2
3  module Decoder_2To4(input wire A1,A0, output wire Y3,Y2,Y1,Y0);
4  assign Y3 = A1&A0;
5  assign Y2 = A1&(~A0);
6  assign Y1 = (~A1)&A0;
7  assign Y0 = (~A1)&(~A0);
8  endmodule
9
```

`timescale 1ns / 1ps

module Decoder_2To4(input wire A1,A0, output wire Y3,Y2,Y1,Y0);

assign Y3 = A1&A0;

assign Y2 = A1&(~A0);

assign Y1 = (~A1)&A0;

assign Y0 = (~A1)&(~A0);

endmodule

1.1 Test Bench

```
1  `timescale 1ps / 1ps
2
3  module Decoder_2To4_TB();
4  reg A1,A0;
5  wire Y3,Y2,Y1,Y0;
6  Decoder_2To4 test(A1,A0,Y3,Y2,Y1,Y0);
7  initial begin
8  assign A1=0; assign A0 = 0; #5;
9  assign A1=0; assign A0 = 1; #5;
10 assign A1=1; assign A0 = 0; #5;
11 assign A1=1; assign A0 = 1; #5;
12
13 $finish;
14 end
15
16 endmodule
17
```

```
`timescale 1ps / 1ps

module Decoder_2To4_TB();
reg A1,A0;
wire Y3,Y2,Y1,Y0;
Decoder_2To4 test(A1,A0,Y3,Y2,Y1,Y0);
initial begin
assign A1=0; assign A0 = 0; #5;
assign A1=0; assign A0 = 1; #5;
assign A1=1; assign A0 = 0; #5;
assign A1=1; assign A0 = 1; #5;
$finish;
end
endmodule
```

2. Behavioural 2-to-1 multiplexer

```
1  `timescale 1ns / 1ps
2
3  module MUX_2To1(input wire S,D1,D0, output wire Y);
4  assign Y = (~S&D0) | ( S & D1);
5  endmodule
6
```

```
`timescale 1ns / 1ps

module MUX_2To1(input wire S,D1,D0, output wire Y);
assign Y = (~S&D0) | ( S & D1);
endmodule
```

3. Behavioural 4-to-1 multiplexer

```
1  `timescale 1ps / 1ps
2
3
4
5  module MUX_4To1(inout wire S1,S0,D3,D2,D1,D0,output wire Y);
6  wire w1,w2;
7  MUX_2To1 A(S0,D3,D2,w2);
8  MUX_2To1 B(S0,D1,D0,w1);
9  MUX_2To1 C(S1,w2,w1,Y);
10
11
12 endmodule
13
```

`timescale 1ps / 1ps

module MUX_4To1(inout wire S1,S0,D3,D2,D1,D0,output wire Y);

wire w1,w2;

MUX_2To1 A(S0,D3,D2,w2);

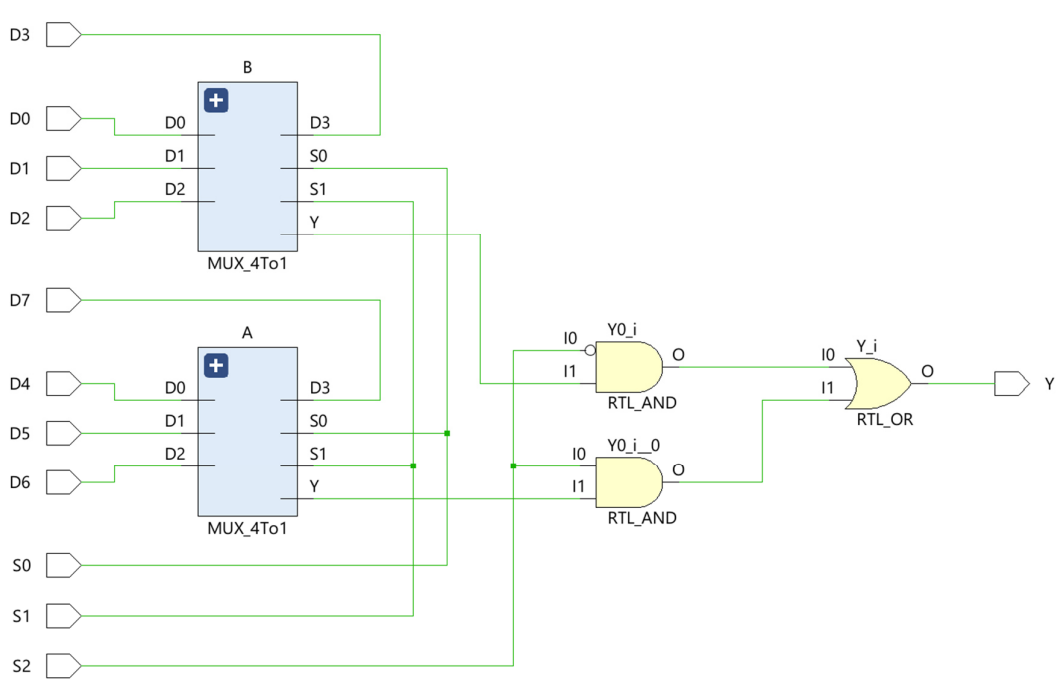
MUX_2To1 B(S0,D1,D0,w1);

MUX_2To1 C(S1,w2,w1,Y);

endmodule

4. Structural 8-to-1 MUX

4.1 Schematics



4.2 System Verilog module

```
1  `timescale 1ps / 1ps
2
3
4
5  module MUX_8To1(input wire S2,S1,S0,D7,D6,D5,D4,D3,D2,D1,D0,output wire Y);
6  wire w1,w2,w3,w4;
7  MUX_4To1 A(S1,S0,D7,D6,D5,D4,w2);
8  MUX_4To1 B(S1,S0,D3,D2,D1,D0,w1);
9  assign Y = (~S2 &w1) | ( S2 & w2);
10 endmodule
11
```

`timescale 1ps / 1ps

module MUX_8To1(input wire S2,S1,S0,D7,D6,D5,D4,D3,D2,D1,D0,output wire Y);

wire w1,w2,w3,w4;

MUX_4To1 A(S1,S0,D7,D6,D5,D4,w2);

MUX_4To1 B(S1,S0,D3,D2,D1,D0,w1);

assign Y = (~S2 &w1) | (S2 & w2);

endmodule

4.3 Test Bench 8 To 1 MUX

```
`timescale 1ps / 1ps


module MUX_8To1_TB();
reg S2,S1,S0,D7,D6,D5,D4,D3,D2,D1,D0;
wire Y;

MUX_8To1 test(S2,S1,S0,D7,D6,D5,D4,D3,D2,D1,D0,Y);
initial begin
assign S2 =0 ; assign S1 = 0; assign S0 = 0;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 1; #5;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
assign S2 =0 ; assign S1 = 0; assign S0 = 1;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 1;assign D0 = 0; #5;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
assign S2 =0 ; assign S1 = 1; assign S0 = 0;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 1;assign D1 = 0;assign D0 = 0; #5;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
assign S2 =0 ; assign S1 = 1; assign S0 = 1;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 1;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
assign S2 =1 ; assign S1 = 0; assign S0 = 0;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 1;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
assign S2 =1 ; assign S1 = 0; assign S0 = 1;
assign D7 = 0; assign D6 = 0;assign D5 = 1;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
assign S2 =1 ; assign S1 = 1; assign S0 = 0;
assign D7 = 0; assign D6 = 1;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
assign S2 =1 ; assign S1 = 1; assign S0 = 1;
assign D7 = 1; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;

$finish;
end
endmodule
```

`timescale 1ps / 1ps

module MUX_8To1_TB();

reg S2,S1,S0,D7,D6,D5,D4,D3,D2,D1,D0;

wire Y;

MUX_8To1 test(S2,S1,S0,D7,D6,D5,D4,D3,D2,D1,D0,Y);

initial begin

```
assign S2 =0 ; assign S1 = 0; assign S0 = 0;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 1; #5;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;

assign S2 =0 ; assign S1 = 0; assign S0 = 1;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 1;assign D0 = 0; #5;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;

assign S2 =0 ; assign S1 = 1; assign S0 = 0;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 1;assign D1 = 0;assign D0 = 0; #5;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;

assign S2 =0 ; assign S1 = 1; assign S0 = 1;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 1;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;

assign S2 =1 ; assign S1 = 0; assign S0 = 0;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 1;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;

assign S2 =1 ; assign S1 = 0; assign S0 = 1;

assign D7 = 0; assign D6 = 0;assign D5 = 1;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;

assign S2 =1 ; assign S1 = 1; assign S0 = 0;

assign D7 = 0; assign D6 = 1;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;
```

```
assign S2 =1 ; assign S1 = 1; assign S0 = 1;

assign D7 = 1; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;

assign D7 = 0; assign D6 = 0;assign D5 = 0;assign D4 = 0;assign D3 = 0;assign D2 = 0;assign D1 = 0;assign D0 = 0; #5;


$finish;

end

endmodule
```

5. Function