Selective Gray-Coded Bit-Plane-Based Two-Bit Transform and Its Efficient Hardware Architecture for Low-Complexity Motion Estimation

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***Abstract*—In this paper, a novel low bit-depth representation-based motion estimation approach with its hardware architecture is presented. The low bit-depth representation of pixels in the proposed method is constructed by choosing them from the gray-coded bit planes in an efficient way. Additionally, a new matching creation is also presented to improve the motion estimation accuracy. Thanks to the proposed binarization approach, the computation load is considerably reduced compared to filtering-based low bit-depth representation motion estimation methods. A novel hardware architecture for the proposed method is also presented in this paper. Experimental results revealed that the proposed motion estimation method and its hardware architecture provides a good balance between motion estimation accuracy and hardware resources especially for consumer electronics applications.**

***Index Terms*—Low-complexity binarization, gray coding, motion estimation, one-bit transform.**

I. Introduction

RECENTLY, the high definition (HD) and ultra HD (UHD) videos are widely used in numerous fields for example entertainment, telecommunication etc. However, with increased video resolution, there has been great demand to video coding technology. So, the digital video technology seriously needs video compression for transmitting and storing the HD and UHD videos because of the limited bandwidth and memory of devices which has video recording capability.

Nowadays, video compression methods are widely used in various multimedia application and consumer electronic devices such as digital televisions, portable video units, digital camcorders, mobile phones. The compression performance of the video coding standards increases thanks to improvements in video coding systems. In the literature, there are MPEG 1, MPEG-4, H.261 and H.263 video encoding standards. Today, H.264/AVC [1] which is still widely used whereas HEVC [2] (High Efficient Video Coding) standard is introduced in 2013. These video coding standards have a relatively high computational cost. Therefore, especially for high-definition video applications, it is not possible to perform encoding in real-time using software solutions. A significant part of this high computational load (50-70%) is necessary for the coding of inter-frame redundancy in motion estimation step. Hence, it is necessary to reduce the computational complexity which may be achieved by fast and effective ME algorithms.

Because of the removing the temporal redundancy between video frames, ME is the most important part of video coding standards. In the literature, many ME algorithms have been proposed. Block based motion estimation (BMA) is the most popular algorithm where the input frame is divided into non-overlapping fixed size blocks, the best matched candidate block within a search window in the reference frame is founded and motion vectors are obtained based on the sum of absolute differences (SAD) criterion. If all possible candidate points in search area are checked this approach is called as full-search (FS) based ME and it requires high power consumption and complexity [3]. Because of the high complexity of FS based ME, many fast ME methods have been proposed in the literature. One approach employed in fast ME methods is to reduce the number of search points by making use of some patterns such as, Diamond Search (DS) [4], Hexagon Search (HS) [5], Four Step Search (FSS) [6], Three step search (TSS) [7], New Three Step Search (NTSS) [8]. Another group of fast ME methods utilize low bit-depth representation of input frames to simplify matching computation. In this approach, each pixel is represented using a few bits instead of 8 to 10 full bit depth. In this way, Boolean Exclusive-OR (EX-OR) operation which can be implemented efficiently in hardware is used for matching criterion computation to reduce computational complexity of SAD. The one-bit transform (1BT) [9] is proposed to represent video frame in 1-bit depth of 8-bit. In this approach, video frames are filtered by a multi-band pass filter and binary frames are obtained by comparing filtered and original frames. The motion vector is computed using NNMP (Number of Non-Matching Points)

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criterion which requires only EX-OR operation. The 1BT kernel has 25 non-zero elements which is not power of 2. Because of the normalization coefficient is non-integer in 1BT approach, multiplication free 1BT transform (MF-1BT) [10] using a new diamond shaped multi bandpass filter is proposed. This approach as named as two-bit transform (2BT) based ME which uses local mean and standard deviation values improves to obtain bit-planes. Thanks to additional bit plane introduced ME accuracy of this approach is better than 1BT and MF-1BT based methods. Constrained one-bit transform (C-1BT) method [12] is proposed where a constraint mask is used to mark the reliable pixels for matching stage. While this approach increases ME performance of 1BT and 2BT based ME approaches, it decreases computational complexity compared to 2BT based ME approach. Enhanced two-bit transform based ME as shown by Choi and Jeong [13] is proposed by extending the typical 2BT matching criterion. This approach improves the ME accuracy with the same computational complexity compared to 2BT based ME. Enhanced constrained one-bit transform is presented which improves ME performance of C-1BT based ME method by Lee *et al.* [14]. It uses enhanced NNMP criterion to provide broader dynamic range and improves the accuracy of the ME approaches using standard NNMP. A weighted constraint mask as shown by Güllü [15] is proposed in place of constraint mask of C-1BT based ME approach. This mask is obtained according to the difference between a pixel and its 1BT threshold value. This method uses two-bit depth constraint mask and three-bit plane in total for ME and hence increases complexity. In addition to filtering based low-bit depth ME approaches, Gray coding-based ME approaches are proposed. Çelebi *et al.* [16] proposed truncated gray-coded bit-plane matching (T-GCBPM) based ME to reduce binarization complexity. T-GCBPM approach utilizes 3 most significant bit-planes from Gray-coded pixels instead of 8-bit depth pixel values. Several hardware architectures are presented for the aforementioned methods in the literature. Çelebi *et al.* [17] presented a reconfigurable bit plane matching based variable block size ME method and a runtime reconfigurable hardware architecture. In this work, variable block size form of the fixed block size ME method presented in [16] is proposed and it is named as weightless TGCBPM (W-TGCBPM). An adaptive search range determination-based ME method is proposed in order to speed-up C-1BT based ME by Urhan [18] and its novel hardware architecture is presented for this method by Çelebi and Urhan [19]. A high-performance hardware architecture [20] with early termination mechanism is presented for C-1BT based ME. A fast ME method which is a combination of diamond search algorithm and weighted C-1BT (WC-1BT) [15] and its hardware architecture is presented in [21]. Recently, selective-gray coding-based ME approach and related hardware architecture [23] is proposed to obtain a single bit-plane by choosing certain bits of Gray coded pixels. This approach reduces binarization cost and increases ME performance considerably. In this paper, a new two-bit depth selective-gray coding based ME approach and its efficient hardware architectures is proposed. The proposed approach has lower computation complexity and better accuracy compared to other ME approaches presented in the literature which use more than one-bit planes for matching. Recently a novel 1-dimensional filtering-based ME method (1DF-2BT) with its novel hardware architecture is proposed by Çelebi *et al.* [24]. The proposed ME method improves ME accuracy of the 2-dimensional filtering-based methods. In addition, it has the lowest hardware complexity among other low bit depth approaches.

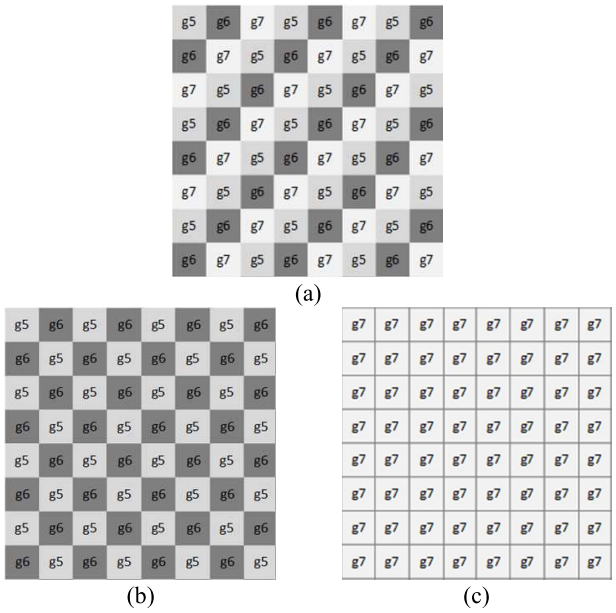
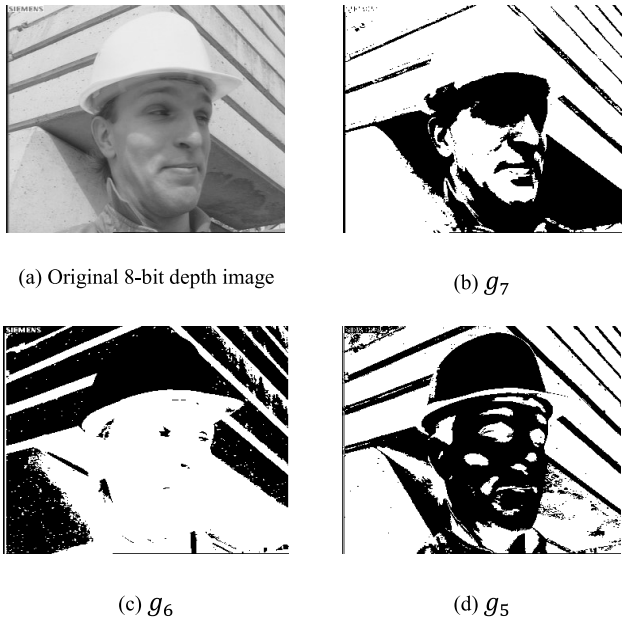


Fig. 1. Bit-plane selection patterns for an 8×8 image block, a) For the method presented in [23], b) For the first bit plane of proposed method, c) For the second bit-plane of proposed method.

II. Proposed Method

As seen from recent work as presented by Yavuz *et al.* [23], Gray coding-based ME methods are more convenient compared to other low complexity ME methods presented in [9]–[15] in terms of simplicity in binarization process. Although Gray coding-based ME methods facilitate the binarization process, ME accuracy is not adequate relative to presented methods in [9]–[15] for the same number of bit-planes used in matching process. Hence, a novel Gray coding based two-bit transform (2BT) ME approach which is named as selective Gray coding based 2BT (SGCB 2BT) is proposed in this work.

As mentioned earlier [23], a single bit plane is obtained by selectively choosing certain bits of Gray coded pixels. In the proposed binarization approach, instead of a single bit plane, two-bit planes are constructed by applying selection scheme which is modified form of scheme presented in [23]. While Figure 1a illustrates the bit-plane selection scheme of the method in [23] for an 8×8 image block, Figure 1b and Figure 1c show the bit-plane selection schemes of proposed method in this paper. As seen from Figure 1a, a single bit plane is constructed by selecting from the 3 most significant bit-planes (g5, g6, g7) which contain Gray-coded pixel values according to a certain selection scheme. In the selectively choosing g5 and g6 bits whereas the second bit plane is generated by using only g7 bits as illustrated in Figure 1b and 1c.



(a) Original 8-bit depth image (b) g_7 (c) g_6 (d) g_5

Fig. 2. Gray-coded three bit-planes of Foreman frame #5.

Fig. 2 shows three most significant gray-coded bit planes of an image frame from the Foreman sequence. The proposed approach only uses these three planes because, these bit-planes contain most of the textural information available in the original frame. As seen from this figure, the most significant bit-plane (g_7) provides rough information about the image content. By selecting from the g_6 and g_5, fine details are extracted from the image. Other bit-planes are not used in the proposed approach because they do not provide essential information about the motion characteristics according to the experimental analysis. After binarization process, 2BT representations of images are obtained and 2-bit planes are utilized in matching process. The matching criterion of proposed approach is different from standard *NNMP*. The proposed matching criterion is called $NNMP_{2BT}$ and is computed as follows:

$$\begin{aligned} nnmp_1(m,n) &= \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} B_{c_1}(i,j) \oplus B_{sw_1}(i+m, j+n) \\ nnmp_2(m,n) &= \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} B_{c_2}(i,j) \oplus B_{sw_2}(i+m, j+n) \\ nnmp_3(m,n) &= nnmp_1(m,n) \odot nnmp_2(m,n) \\ NNMP_{2BT}(m,n) &= nnmp_1(m,n) + nnmp_2(m,n) \\ &\quad + nnmp_3(m,n) \end{aligned} \tag{1}$$

where $-s \le m, n \le s$ whereas $\oplus$, $\odot$, N, (m,n), and s denote XOR operation, AND operation, block size, candidate motion vector and search range, respectively. B_c and B_{sw} determine binary representations of current block and search window. The aim of using $NNMP_{2BT}$ is to improve dynamic range of conventional NNMP. Note that some part of the proposed criterion is computed similar to the standard *NNMP* ($nnmp_1$ and $nnmp_2$). In addition to these parts, $nnmp_3$ part is calculated to take the effect of common different points on current block and search window into consideration for each bit plane. Thus, by combining these three values, it is ensured that the new matching criterion has higher dynamic range compared to that of *NNMP*.

III. Hardware Architecture

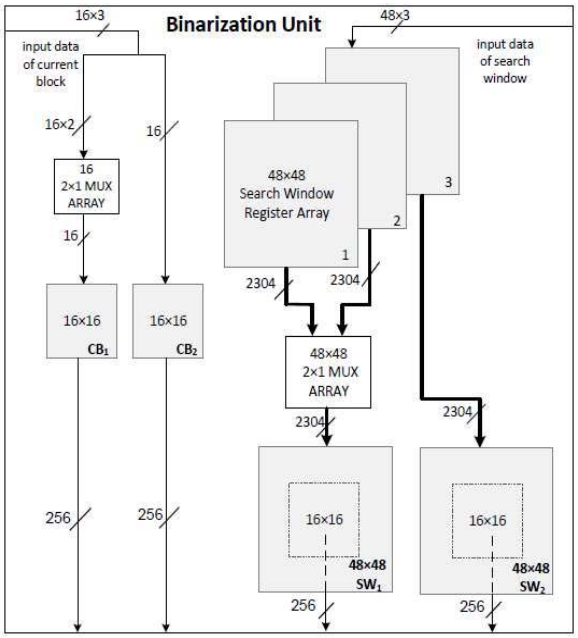
Recently, because of limited storage resources and battery power in new portable consumer electronic devices, size and low power consumption have become desired requirement. Instead of assessing 8-bits/pixel for motion estimation, using lower bits to represent image frames reduces computational load and provides efficient hardware implementation. As mentioned in the previous section, Gray coding-based ME methods are very suitable for efficient hardware implementation thanks to their significant advantage in binarization cost.

T-GCBPM based ME approach [16] is achieved by truncating some of the least significant Gray-coded bit planes and its binarization process is carried out by utilizing simple EX-OR operations. According to experimental results, best ME accuracy is obtained when only 3 most significant bit (MSB) planes are utilized. Binarization process is performed by applying a selection scheme to construct single bit-plane from 3 bit-planes and its hardware architecture is presented by Yavuz *et al.* [23].

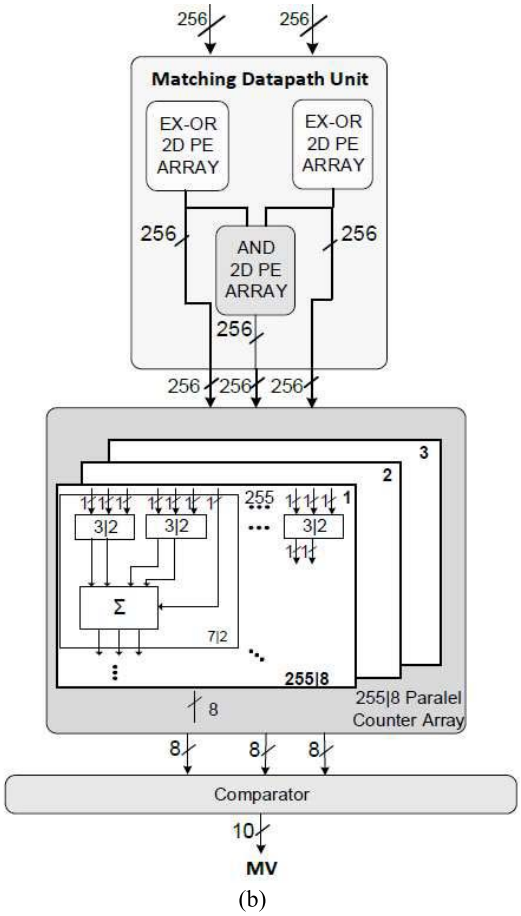
In this work, in order to improve ME performance of method presented in [23], a novel ME method which utilizes 2 bit-planes in the matching part is developed. Proposed hardware architecture of this method is illustrated in Figure 3. Figure 3a shows the binarization unit of hardware architecture diagram for proposed method which is modified version of the method presented in [23]. Data_in_cb and Data_in_sw signals are the most significant 3-bits of the current block and the search window respectively. Figure 3b illustrates matching unit of proposed method.

As seen from this figure, the number of bit planes utilized for matching unit are 2 for proposed method whereas 1 bit-plane is utilized in [23]. For the hardware architecture in Figure 3a, search window and current block are composed of 3 and 2 bit-planes, respectively. In this architecture, search window and current block bit planes are stored by making use of shift register arrays which are consisted of flip flops with three and four direction shifting capabilities as presented in [19]. As shown in Figure 3a, so as to reduce from the first 2 bit-planes of 48×48 search window to single bit-plane, 48×48 2×1 multiplexer array is used. Owing to multiplexer array, the first search window which is used in matching process, is obtained by applying a selection scheme. Figure 4a illustrates a 2×1 multiplexer used in the array.

According to the selection scheme in the method, a 2×1 multiplexer selects the appropriate bit from Gray coded 2 bits in its input. The second search window is directly composed of the third bit-plane of 3-bits search window register arrays. Input data of current blocks is separated into two. One of them is driven to 16 2×1 multiplexers to construct the first current block which consists of the first 2 Gray-coded bit-planes and the other is directly driven to the second current block which consists of the third Gray-coded bit-planes



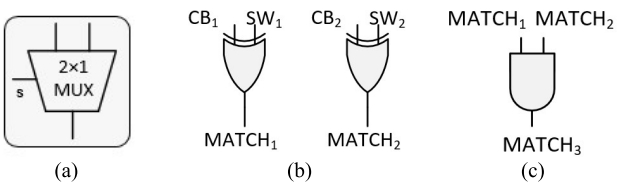
(a)



(b)

Fig. 3. Proposed hardware architectures, (a) Binarization unit, (b) Matching unit.

of 3-bits current block register arrays. Consequently, two bit-planes are obtained to exploit them in the matching process for both search window and current block.



(a) (b) (c)

Fig. 4. Datapath components, (a) A 2×1 multiplexer, (b) EX-OR processing element, (c) AND processing element.

After binarization process, block matching is performed based on $NNMP_{2BT}$ criterion defined in (1). Firstly, 256 bits of two reference blocks which are 16×16 blocks located on the center of 48×48 search windows and 256 bits of two current blocks are driven to matching datapath unit. In this unit, there are 3 processing element (PE) arrays and these sub-units are illustrated in Figure 3b. The EX-OR processing element which performs comparison between 1bit/pixel of current block and reference block is shown in Figure 4b. Figure 4c shows the AND processing element. This PE performs Boolean AND operation among the bits in the outputs of EX-OR sub-units which are composed of 16×16 sized 2D PE arrays in Figure 3b. This sub-unit is also composed of 16×16 sized 2D PE arrays. Matching data-path unit has three 256-bits output ports which are the output of each sub-unit.

Secondly, three parallel counter arrays compute $NNMP_{2BT}$ values for three 256-bits in its inputs. Parallel counter array is the same with presented in [23] and it is utilized for 3 times in this architecture. Once the computation of 3 *NNMPs* is completed, comparator block adds them and determines the motion vector of candidate blocks according to calculated the minimum total $NNMP_{2BT}$ value.

IV. Experimental Results

In this paper, performance of the proposed ME approach and proposed hardware architecture are evaluated separately as follows.

A. Motion Estimation Performance

In order to determine the performance of the proposed ME method and compare with other low-bit-depth ME methods, Peak Signal to Noise Ratio (PSNR) between the original and estimated image frames is computed. This computation is carried out via an open loop scheme where each frame is estimated from the previous frame. Table I shows PSNR results of different low-bit depth ME methods together with the proposed method in dB for six different sequences which have different motion characteristics. The block size and search window are set to 16 for the result given in this table. As seen from Table I, proposed method provides superior performance than 2-bit representation based ME approaches such as 2BT [11], C-1BT [12] early terminated C-1BT [20], Adaptive SR based C-1BT [18], 1DF-2BT [24] and T-GCBPM [16] when 2-bit planes are used. In addition, proposed method has same performance with T-GCBPM [16] when 3-bit planes are utilized while outperforming another WC-1BT based method in [21] where 3-bit

TABLE I
MOTION ESTIMATION PERFORMANCE OF LOW-COMPLEXITY ME METHODS (IN DB)

ME Method	Video Sequences (Frame Size, Sequence Length)						
	Football (352×240) (125 frames)	Foreman (352×288) (300 frames)	Flowergarden (352×240) (115 frames)	Coastguard (352×288) (300 frames)	Tennis (352×240) (150 frames)	Mobile (352×240) (300 frames)	Average of six video sequences
SAD (8-bit depth)	22.88	32.09	23.79	30.48	29.45	23.94	27.11
1BT [9]	21.83	30.32	23.31	29.83	28.11	23.61	26.17
MF-1BT [10]	21.81	30.38	23.26	29.88	28.18	23.63	26.19
2BT [11]	22.06	30.70	23.43	29.94	28.46	23.66	26.38
C-1BT [12]	22.10	30.86	23.38	29.98	28.71	23.69	26.45
Early Terminated C-1BT [20]	21.85	30.37	23.20	29.99	28.60	23.60	26.33
Adaptive SR based C-1BT [18]	22.06	30.71	23.44	30.05	28.60	23.67	26.42
T-GCBPM [16] NTB=6	22.38	30.64	23.61	29.14	28.69	23.78	26.33
T-GCBPM [16] NTB=5	22.59	31.32	23.67	30.16	28.78	23.81	**26.72**
Modified XOR (8-bit depth) [22]	22.64	31.91	23.65	30.40	29.25	23.80	26.94
Selective Gray-coding (SGC-1BT) [23]	22.24	31.03	23.38	29.85	28.69	23.47	26.44
1DF-2BT [24]	22.35	30.86	23.55	29.97	28.30	23.75	26.46
SGC-2BT **(Proposed Method)**	22.56	31.35	23.62	30.14	28.92	23.75	**26.72**

TABLE II
HARDWARE UTILIZATION AND DATA THROUGHPUT PERFORMANCE OF THE LOW COMPLEXITY ME METHODS FOR FIXED BLOCK SIZE (16×16) ME

	[20]	[22]	[23]	[24]	SGCB-2BT (Proposed)
Binarization Included	No	Yes	Yes	Yes	Yes
Bit depth utilized in binarization	NA	8	3	8	3
Bit depth utilized in matching	2	8	1	2	2
Dedicated on chip memory	9632 bits	8192 bits	0	0	0
Area	5035 LUTs 4100 DFFs	6157 LUTs NA (0 LUTs 0 DFFs for memory)	8747 LUTs 7877 DFFs (8086 LUTs 7677 DFFs for memory)	8607 LUTs 7598 DFFs (8062 LUTs 5856 DFFs for memory)	12283 LUTs 8743 DFFs (10737 LUTs 7427 DFFs for memory)
Dynamic Power (On Chip)	N/A 202mW@100MHz	190mW@50MHz N/A	111mW@50MHz 137mW@100MHz	26,3mW@50MHz 52,22mW@100MHz	171mW@50MHz 222mW@100MHz
Technology scaling factor normalized predicted power @28nm	N/A@50MHz 94,39mW@100MHz	132,87mW@50MHz N/A@100MHz	111mW@50MHz 137mW@100MHz	26,3mW @50MHz 52,22mW @100MHz	171mW@50MHz 222mW@100MHz
Maximum frequency	265 MHz	293 MHz	327 MHz	209.24 MHz	309 MHz
Performance @720p	NA	19,85 fps	83,41 fps	29.24 fps	78,81 fps
Performance @1080p	NA	8,82 fps	37,07 fps	13.01 fps	35,03 fps
Performance @4K	> 30 fps	2,20 fps	9,26 fps	3.25 fps	8,75 fps
Technology	FPGA 65 nm	FPGA 40 nm	FPGA 28 nm	FPGA 28 nm	FPGA 28 nm
Search range	[-16 16]	[-16 16]	[-16 16]	[-16 16]	[-16 16]
Search method	Full search /early termination	Full search	Full search	Full search	Full search
Scanning pattern	NA	Raster scan	Spiral scan	Spiral scan	Spiral scan
Supported MB partitions	16×16 (4 MBs in parallel)	4×4, 4×8, 8×4, 8×8, 8×16, 16×8, 16×16	16×16	16×16	16×16
# of reference frames	1	1	1	1	1

planes are used. The proposed algorithm achieves PSNR gain of 0.3 dB on average compared to the recently proposed Selective-Gray Coding [23] based ME. The presented method in [22] uses modified XOR function for matching criteria gives better performance than the proposed algorithm. However, it should be noted that this approach has more computational complexity because it utilizes 8-bit depth per pixel for computations similar to the SAD approach. The architectural impact of this approach is discussed in the following section.

B. Hardware Implementation Results

In this work, the proposed hardware architecture is implemented on a 28 nm FPGA device as in [23]. Implementation results reveal that the proposed architecture for SGCB-2BT occupies 12283 LUTs and 8743 DFFs which the 2.83% and 1.01% of the total available resources of the target FPGA device, respectively. ME performance of the proposed architecture is comprehensively compared to other low-complexity block matching architectures in the literature in Table II.

TABLE III
POWER ANALYSIS RESULTS

3 different motion characteristics	Dynamic Power Consumption (mW) 20 ns/10 ns
1	170/219
	182/242
	160/202
2	179/238
	160/200
	181/242
3	165/211
	164/208
	182/243
Average	171/222

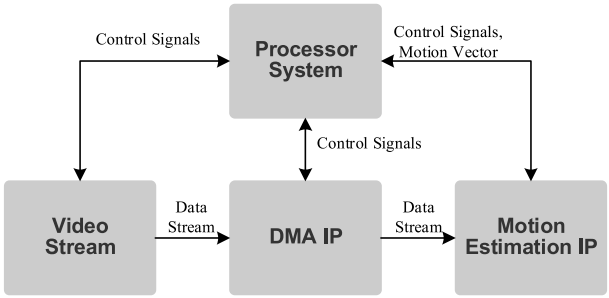


Fig. 5. CPU integration scheme proposed in [23].

Gray selective approach is also used in [23] where 1 bit is utilized for matching process however, the proposed method utilizes 2 bits. Thus, a new binarization datapath is designed in this work. Because of additional hardware resources utilized, the proposed architecture consumes more area compared to the architecture in [23]. Even the number of bit-planes utilized in the matching stage is doubled, as seen from the Table II, the number of LUTs has increased 40% whereas number of DFFs is increased 11% which is much lower compared to increase ratio of bit-planes. The power consumption of the proposed method is increased roughly 50% compared to the method in [23].

It is important to note that when the amount of utilized resources for memory is subtracted from total resources, the remaining amount of LUTs and DFFs are approximately 1500 and 2200, respectively. Hence, proposed architecture is comparable with [20] in terms of utilized resources in matching part. It is revealed from the Table II that the proposed architecture can process more frames in a second compared to the architectures presented in [22] and [24] and achieve higher maximum operating frequency compared to [20], [22], and [24]. The ME performance of the method presented in this work is also better compared to these works except [22]. However, it is important to note that the method in [22] utilizes 8-bits per pixel. Thus, this architecture is not easy to be considered as a low-complexity approach compared to the proposed architecture. It is also clear form Table II that even the architecture given in [22] seems like occupying similar hardware resources, it is almost 4 times slower in terms of frame rate as a result of which lower power consumption also seems similar to the proposed low-complexity approach in this work. Thus, it should be expected that if the architecture in [22] is adapted to provide similar frame rate, it will consume almost 4 times more hardware resource and power which makes it similar to the conventional SAD based hardware ME architectures.

Power analysis of the proposed architecture is performed by using a power estimation and analysis tool in which switching activity that is obtained after post-timing simulation is used. It is important to note that the power consumption results given in Table II are only provided for the switching activity in the core of chip by neglecting the impact of external memory interface. Thus, the considerable amount of power consumption caused by the I/O blocks of the chip is not taken into account. Furthermore, in order to perform a fair comparison in terms of power consumption among different technology nodes, the scaling factor should be taken into account.

If core voltages are assumed constant between each technology node, the power consumption of a design would have a rate of 1, 1.43, 2.14 for 28 nm, 40 nm and 65 nm, respectively [25]. Hence, the hardware architectures presented in [20] and [22] should be evaluated with this perspective the details of which is discussed in [25].

According to the power consumption results presented in Table II even though the proposed architecture seems to consume the highest power, it must be noted that the architecture in [20] does not implement binarization process which may cause a significant contribution to total power consumption, the impact of which is well discussed in [24]. When compared to the architecture in [23], roughly doubled power consumption should be considered normal as the number of bit-planes utilized in the matching process is doubled. Additionally, CPU integration perspective should be taken into account while assessing the power consumption performance. Thus, the lower power consumption of the architecture in [24] should be investigated carefully. For instance, the proposed architecture may be driven 24 pixels for a single CPU transaction which is performed in a 64-bits wide data-bus whereas the architecture proposed in [24] can only be driven 8 pixels in this case which results in 3 times more CPU transaction to load the data to the ME block. Thus, roughly 2.5 times more CPU power would be consumed to fully utilize the architecture proposed in [24]. Furthermore, the increase in the external memory bandwidth is not taken into account as well for that architecture.

The main reason for the higher power consumption in Gray Selective scheme-based ME hardware architectures is the extra switching activity caused by the binarization scheme which may be considered as a draw-back of this ME method compared to the other advantages discussed in this paper. Dynamic power consumption result which is obtained for the clock periods of 20ns and 10ns for proposed hardware architecture is presented in Table III. The power analysis is performed for 9 different MBs with 3 different motion characteristics.

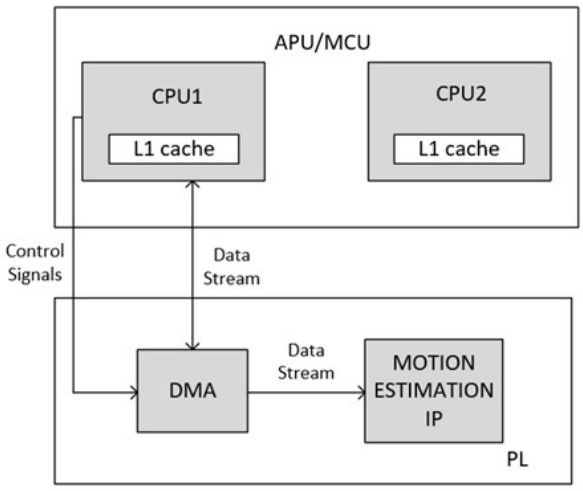


Fig. 6. CPU integration scheme proposed in [24].

V. Consumer Electronics Device Integration

It is shown in [23] and [24] that the low complexity ME hardware architectures can be integrated into the state of the embedded processing platforms. In [23], a DMA based scheme is proposed for the CPU integration of the proposed architectures as illustrated in Fig. 5.

Another integration scenario is proposed in [24] where the integration with the cache of the CPU is proposed which may be more capable compared to the scenario proposed in [23] as illustrated in Fig. 6. Both integration schemes are successfully implemented for the architecture proposed in this work.

VI. Conclusion

In this work, a novel ME algorithm and its hardware architecture based on the selective Gray coding method is presented. The proposed approach constructs and employs two-bit planes in a novel scheme which also improves the ME accuracy of methods within the same category, it provides similar ME performance compared to the methods in which three bit-planes are utilized. Furthermore, a novel hardware architecture for the proposed method is also presented in this work. A new binarization and matching data-path is designed to implement the proposed ME approach. It is shown that both the ME approach and its hardware architecture provides considerable performance gain in terms of ME accuracy, speed, power consumption and hardware area.

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