Recent Innovations in CMOS Image Sensors

Ray Fontaine
Technology Analysis Group
Chipworks Inc.
3685 Richmond Road
Ottawa, Ontario, Canada K2H 5B7
rfontaine@chipworks.com

***Abstract* - The trend in semiconductor manufacturing over the last decade has been an accelerated rate for both materials integration and wafer fabrication process development. While the cutting edge of semiconductor technology is driven by digital logic and memory applications, several other technology sectors benefit from innovation by the leaders. Of these technology sectors, image sensor manufacturers have realized many benefits from the selective use of developments within advanced technology node manufacturing.**

The motivations for the imaging industry to pursue Moore's Law type of scaling are comparable to that of the broader semiconductor industry. Additionally, image sensor companies seek a reduction of camera module form factor, an increase in pixel resolution, and an increase in pixel array performance.

Today, semi-professional grade digital single-lens reflex (DSLR) pixels have scaled down to the size of what were state-of-the-art "small pixel" consumer grade camera phone sensors just a few years ago. The pixel size of recent camera phones has shrunk to 1.12 µm. The resolution for recent camera phones has reached 16.4 Mp. Beyond silicon foundry processes, imaging companies must also concern themselves with the optical systems and packaging solutions required to integrate their silicon devices with the consumer electronics supply chain.

Chipworks, as a supplier of competitive intelligence to the semiconductor and electronics industries, monitors the evolution of image sensor technologies as they come into production. Chipworks has obtained charge-coupled devices (CCD) and CMOS image sensor (CIS) chips from leading manufacturers and performed structural, compositional, and design analyses to benchmark the technology of the market leaders.

Keywords: CMOS Image Sensors; Advanced Processes; Advanced Materials

I. INTRODUCTION

A. Background of CMOS Image Sensor Pixels

Consumer grade CMOS image sensors (CIS) for mobile applications, including camera phones, laptops, tablets, etc., have gone from novelty to ubiquitous status in about a decade. As the successor to passive pixel charge-coupled devices (CCD), current system-on-chip (SoC) CIS devices comprise an array of active pixels and supporting circuitry which enables both still and motion photography [1].

Current CIS devices are a result of quickly evolving pixel architectures, which resulted in the now common four-transistor (4T) pinned photodiode structure [2]. 4T pixels include a photon collection region (pinned photodiode), charge transfer transistor, reset transistor, source follower transistor (in-pixel amplifier), and column bus transistor. Essentially, photon generated charge is collected and converted to the voltage domain within each pixel, and ultimately read out to an on-chip analog-to-digital (ADC) to be transformed to the digital domain for image processing.

The fundamental motivations for shrinking pixel size, discussed elsewhere [2, 3], include decreasing the overall chip size and camera module form factor for a given resolution, or increasing the resolution for a given camera module size. In either case, there is both push from industry and pull from consumers for CIS technologists to shrink pixel size and improve pixel performance. Therein lies the fundamental challenge of the image sensor community: how to do more with less available light at each collection node.

II. THE EVOLUTION OF PIXEL STRUCTURES

The conventional planar CMOS fabrication process lends itself quite well to the task of digital imaging. A silicon substrate, optically transparent dielectric stack, and the ability to produce fine pitch interconnect lines are all complementary to CIS device requirements. Fig. 1 shows an 8.0 µm pixel pitch front illuminated (FI) CIS produced by Hynix in 2002 (analyzed in 2004). The structure comprises, from top to bottom, a microlens, planarizing lens buffer layer, color filter, dielectric film stack, pixel interconnect, tungsten silicided transistor gates, and LOCOS isolation. The device was fabricated in a 0.5 µm CMOS process and used spin-on-glass (SOG) to partially planarize the dielectric stack. The color filters, deposited by an iterative spin-on process, and lens buffer film have provided a nearly planar surface for the microlenses. Microlenses significantly increase the light-gathering capabilities of small pixels, effectively increasing the

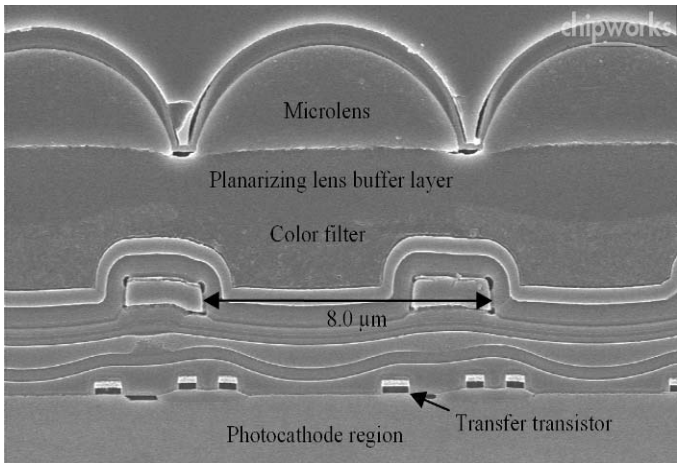


Figure 1. Hynix 8.0 µm Pixel, 0.5 µm Process Technology Generation

978-1-61284-409-1/11/$26.00 ©2011 IEEE

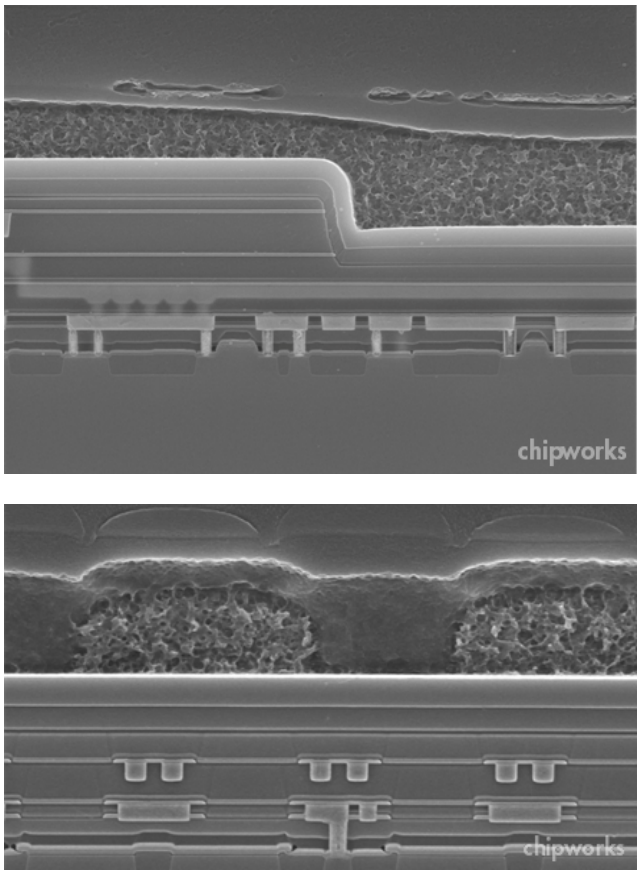


Figure 2. STMicroelectronics 2.2 µm Pixel, 0.13 µm Process Technology (Peripheral and Pixel Regions)

pixel fill factor. While fabricated in a mature process by today's standards, modern FI CIS devices represent refinements of this type of structure.

The 3.0 µm to 3.5 µm pixel generation CIS devices circa 2005 generally featured 0.18 µm process technology with aluminum metallization, chemical mechanical planarization (CMP) of the dielectrics, and shallow trench isolation (STI). Most manufacturers optimized general logic processes for CIS production, and the four to five levels of interconnect enabled sophisticated SoC features to be integrated with the pixel process flow.

A disadvantage of the pixel structures of this era was the shadowing caused by the thick back-end-of-line (BEOL) stack for pixels at the outer edges of increasingly larger pixel arrays. The effects of these comparatively tall structures were somewhat mitigated for outer pixels, where progressively shifting the microlenses toward the array center partially compensated for the chief ray angle (CRA) variance between the outer and central pixels.

A. Shared Pixels

Early implementations of the 4T architecture featured all four transistors occupying valuable real estate which could otherwise be used to collect incident photons. When pixels scaled to the 2.2 µm generation circa 2006, designers evolved to a pixel sharing scheme whereby neighboring pixels, each with a dedicated transfer gate, shared common readout transistors (source follower, reset, row select). Both two-shared and four-shared pixel architectures are currently in production, netting an effective 2.5 transistors (2.5T) or 1.75 transistors (1.75T), respectively, per pixel. These designs, and other pixel sharing configurations, continue to be significant enablers for pixel scaling.

B. BEOL Stack Reduction and Optical Symmetry

Coinciding with the 2.2 µm pixel generation was the broad adoption of 0.13 µm process technology for production CIS devices. In turn, CIS companies utilized divergent approaches to fabrication. For example, STMicroelectonics, an independent device manufacturer (IDM), utilized a copper BEOL scheme with relatively narrow interconnect lines and a four-shared pixel layout that allowed the implementation of the pixel wiring within only two levels of metallization. Fig. 2 shows a cross section view of STMicroelectronics' pixel and logic BEOL structures, illustrating the partial thickness reduction of the pixel BEOL. The reduced metal interconnect in the pixel BEOL greatly reduced the metal shadowing effects.

A new challenge coincident with the use of damascene copper processes was the presence of silicon nitride trench etch stops and copper diffusion barriers in the pixel BEOL. If left in the optical path, the presence of these films could potentially introduce optical interference effects. STMicroelectronics chose to include a mask and etch step to open windows in the nitride films over the photocathodes.

Another approach was taken by Micron (now Aptina), also using a 0.13 µm process, who converted its depreciated DRAM fabs to CIS production. While some IDMs and foundries switched to (then) more expensive copper processes, the narrow aluminum metallization afforded by a DRAM process allowed Micron to produce competitive devices at the 1.75 µm pixel generation. In addition to the advantageous BEOL design rules, the low-leakage transistor requirements for DRAM wordlines were a natural fit for the low noise performance of CIS pixels.

Fig. 3 shows an overview of a Micron 1.75 µm pixel generation CIS, which featured a pixel array dielectric etch back resulting in a pixel BEOL (including filters and lenses), which was essentially the same thickness as the BEOL stack in the logic regions.

Another approach to reduce the pixel BEOL thickness was employed by Samsung, who used a tungsten "metal 0" local pixel interconnect to reduce metal obstruction. Both approaches served to aggressively move the microlenses closer to the silicon surface, thereby improving the angular response of the sensors.

Out of necessity, image sensor technologists focused intently on the pixel BEOL for the 1.75 µm pixel generation. After implementing shared pixel architectures and reducing the thickness of the pixel BEOL stack, there was an awareness by technologists that performance gains could be obtained by optimizing the pixel metallization for optical symmetry.

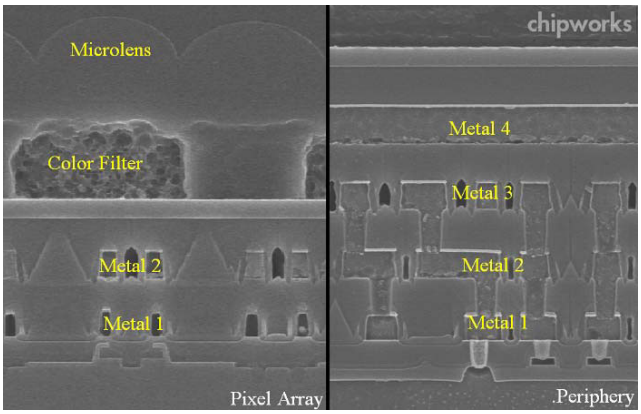


Figure 3. Micron (Aptina) 1.75 µm Pixel, 0.13 µm DRAM Process Technology

Prior to this, the pixel wiring was primarily routed for electrical interconnect requirements, with less emphasis on lateral symmetry through the optical path. The 1.75 µm pixel generation saw the prevalence of balanced interconnect patterning, particularly the use of dummy metal structures to reduce optical cross talk. A high degree of symmetry is considered critical for the optical performance of small pixel FI CIS devices.

Fig. 4 shows two examples of the symmetrical top metal layout of 1.75 µm generation pixels from Samsung and OmniVision. Samsung, an IDM, used a 90 nm process for this generation, while OmniVision's foundry partner TSMC utilized a 0.11 µm aluminum process. Interestingly, the 1.75 µm pixel generation was found to be implemented using 180 nm through 90 nm design rules.

C. Light Pipes

Material integration for CIS production began to accelerate at the 1.4 µm pixel generation with the introduction of so-called "light pipes," or optical waveguides, in the pixels. The addition of light pipes serves to couple the upper region of the pixel BEOL to the photocathode region with minimal photon loss or cross talk.

The processes in production generally comprise: a deep trench etched into the dielectric stack, a silicon nitride trench liner, and a spin-on light pipe fill having an index of refraction

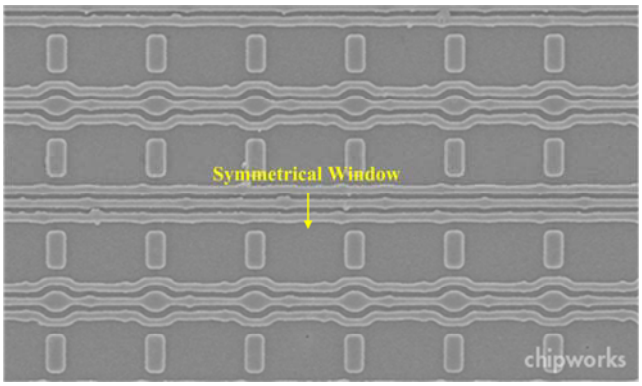


Figure 4a. Samsung 1.75 µm Pixels with Symmetric Interconnect Layout

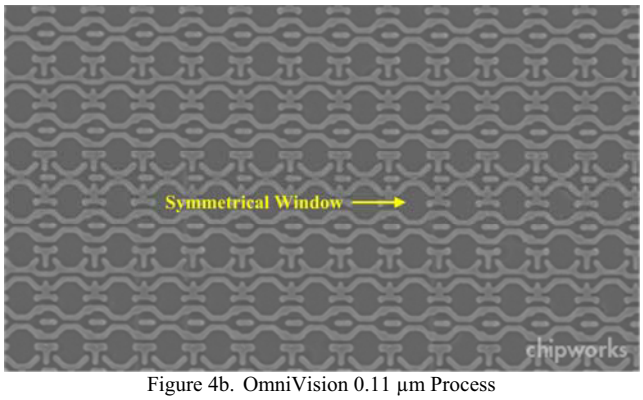


Figure 4b. OmniVision 0.11 µm Process

higher than the surrounding dielectrics [4]. With this type of structure, the microlenses are optimized to shift the focal point to the upper region of the light pipe, enabling the collection of more off-axis light into the light pipe.

The results are improved quantum efficiency, angular response, and optical cross talk performance. Fig. 5 shows an example each of Aptina and Sony light pipes in production for their 1.4 µm pixel CIS devices. Aptina's light pipe fill is an organic film. The shape of the light pipe is reported to effectively collimate the incoming light, thereby, reducing electrical cross talk in the substrate [5]. This device was fabricated using hybrid 130 nm FEOL/90 nm aluminum BEOL design rules.

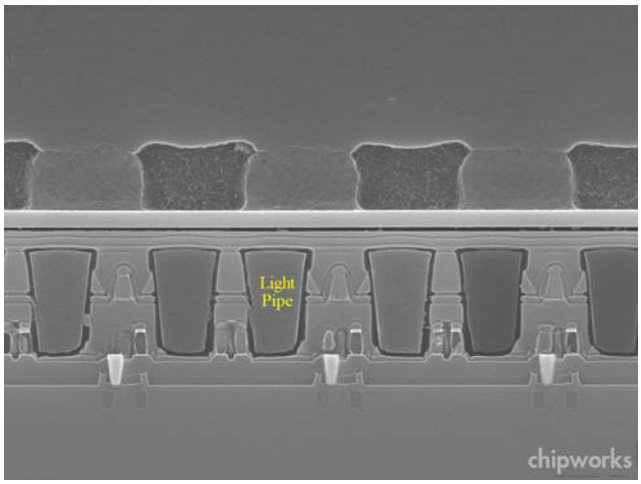
Aptina chose to employ pixel dielectric stack thinning and two levels of metal interconnect, while Sony's light pipe implementation included the full dielectric stack and four levels of metal interconnect. Sony's light pipe fill was found to be titanium-based, likely titanium dioxide (TiO_2). Sony's light pipe process was implemented in a 90 nm copper process.

III. BACK ILLUMINATED CIS DEVICES

Despite the cleverness of sharing pixels, the use of advanced node wafer fabs, and innovation in the pixel BEOL, there exists within a FI CIS device an intrinsic competition between the light sensitive area and the pixel control and readout circuitry.

Amongst the several analyzed commercial FI 1.75 µm pixel and smaller generations, the fill factor is typically less than 50% (excluding the effects of microlenses). In 2009, Sony and OmniVision each began mass production of first generation small pixel back illuminated, or back side illuminated (BI, BSI) CIS devices.

Originally used in specialty CCD applications, BI technology had previously been cost prohibitive for introduction into the consumer electronics supply chain. BI devices potentially enable fill factors approaching 100%.



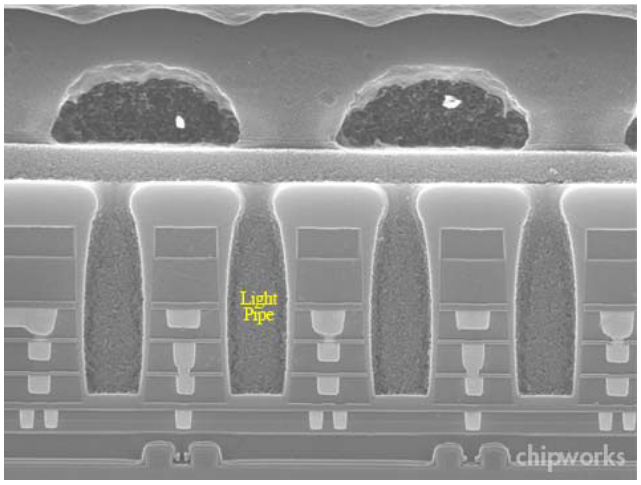
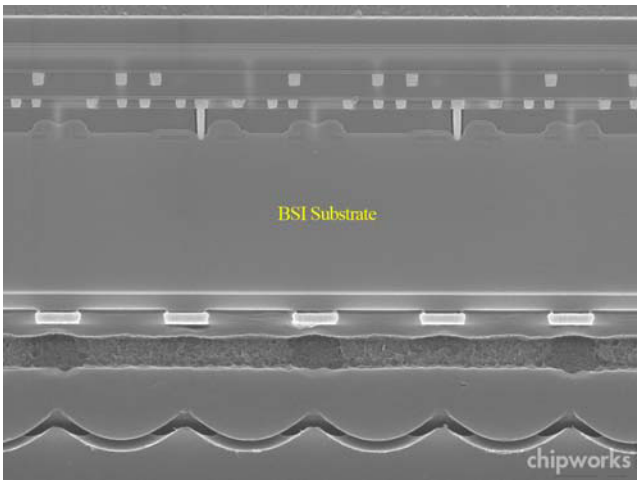


Figure 5. Aptina and Sony 1.4 µm Pixels with Light Pipes



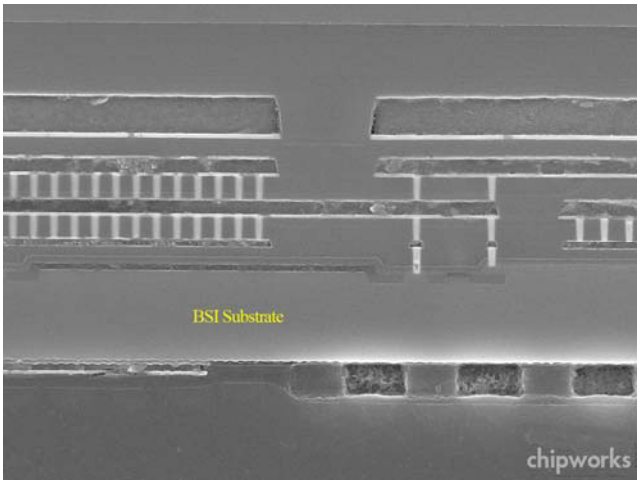


Figure 6. Sony and OmniVision First Generation Back Illuminated Devices

Fig. 6 shows examples of the Sony and OmniVision first generation BI devices. Sony's device was fabricated using a silicon-on-insulator (SOI) process, in which a conventional CMOS process flow was run on SOI wafers with 3 µm thick active silicon.

After completion of the FEOL and BEOL structures, the planarized dielectric stack served as a bonding surface for the joining of the SOI wafer to a silicon chip carrier wafer using an adhesive bonding technique. Next, the sacrificial SOI handle wafer and buried (BOX) layers were removed. The unobstructed back of the substrate functions as the light receiving surface.

For many FI devices, the reflectivity of planar silicon had been addressed through the use of silicon nitride films deposited over the photocathode regions to serve as anti-reflection (AR) layers. For its first BI device, Sony chose to use a hafnium oxide (HfO_2) AR layer blanket deposited over the back of the die. It also included tungsten metallization on the back which optically shielded the peripheral regions, and was patterned to form an aperture grid improving color separation in the pixel array.

While Sony's device had a 1.77 µm pixel size and relatively large form factor module for camcorder applications, OmniVision's first BI device featured a 1.4 µm pixel size, and was deployed in a small form factor camera module. OmniVision and TSMC developed a bulk BI process for their 1.4 µm pixel size sensor, fabricated using 0.11 µm generation process technology [6, 7].

The device used oxide bonding to join the planarized finished wafer to a silicon carrier wafer. The bulk P-type substrate with P-epitaxial layer was mechanically back ground and wet etched, with the epi serving as an etch stop. The resulting substrate thickness was 2.1 µm and displayed some back surface roughness, an artifact of the wafer thinning process. A back surface implant and laser anneal process were used to reduce the crystal defects induced by the wafer thinning process. Due to the small form factor application, OmniVision also adapted its wafer level chip scale (WL-CSP) packaging, first used for its FI devices, to the new BI device structure.

IV. PRESENT AND NEAR FUTURE TRENDS

Many novel CMOS process technologies have been adopted in recent front and back illuminated CIS devices.

STMicroelectronics has incorporated deep trench isolation (DTI) as pixel isolation in FI devices, while Sony has used DTI to isolate the bond pads in BI devices. The emergence of BI devices in mass production has driven the evolution of advanced packaging for CIS devices. Through silicon vias (TSV) were first used by Toshiba and STMicroelectonics in FI devices, and have been used by Samsung in BI devices. Sony has incorporated embedded passive components and semiconductor die in the printed wiring board (PWB) substrates.

Today, CIS devices using 65 nm design rules and 300 mm wafer production are in production. The trend of advanced technology generation pixel manufacturing will continue, likely to below sub-diffraction limit pixels [1]. Beyond silicon, InVisage Technologies, Inc. introduced its quantum dot based image sensors in 2010. Progress in these and other areas ensure that the acceleration of pixel innovation will continue for the near future.

V. REFERENCES

[1] E.R. Fossum, "CMOS Active Pixel Image Sensors: Past, Present, and Future," January, 2008

[2] A. Theuwissen, "CMOS Image Sensors: State-of-The-Art and Future Perspectives," Solid-State Electronics, Vol. 52, 2008, pp. 1401-1406

[3] M. Okincha, "OmniBSI™ Technology Backgrounder," OmniVision Technologies, June, 2009

[4] J. Gambino, et al., "CMOS image sensor with high refractive index lightpipe," 2009 International Image Sensors Workshop (IISW), June 2009

[5] G. Agranov, et al., "Pixel continues to shrink . . . Pixel Development for Novel CMOS Image Sensors," 2009 International Image Sensors Workshop (IISW), June 2009

[6] H. Rhodes, "The Mass Production of BSI CMOS Image Sensors," 2009 International Image Sensors Workshop (IISW), June 2009

[7] S. G. Wuu, "BSI Technology with Bulk Si Wafer," 2009 International Image Sensors Workshop (IISW), June 2009