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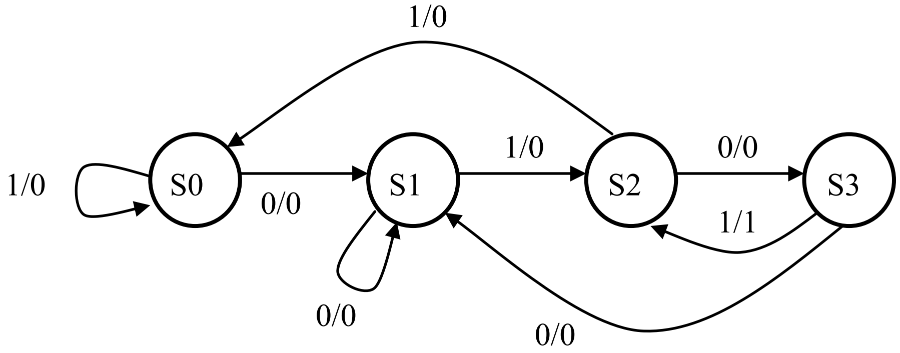
Lab 3: VHDL Design of Sequential Circuits

Part 1

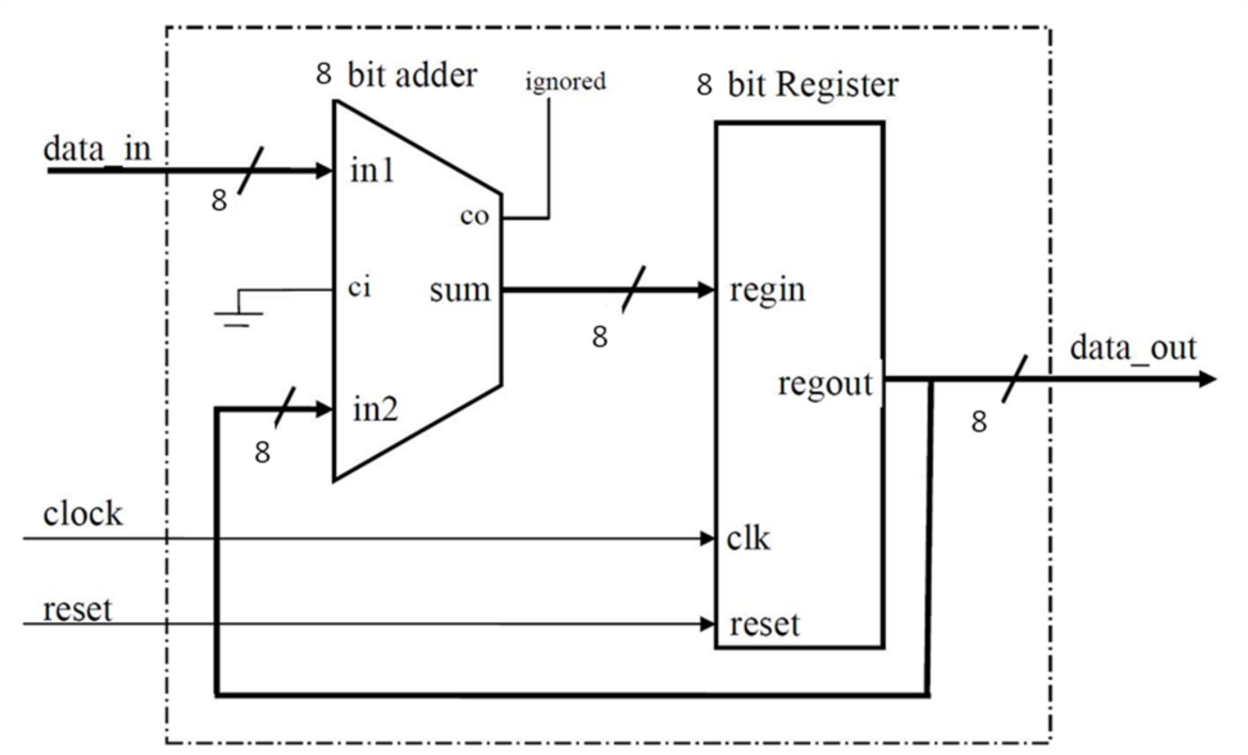
The state diagram of a 0101 sequence detector is shown in the following. Assume that the detector starts in state S0 and that S2 is the accepting state. The labels on the arrow indicate the input/output associated with the indicated transitions.



Develop a VHDL model for the sequence detector described above. Simulate the model using Quartus software. Present a timing diagram of your simulation showing that it works.

Part 2

Using the 8-bit adder from lab 2, design a structural model of a 8-bit accumulator as shown in the figure. The steps for the design are shown below.



Step 1: 8-Bit Adder

1. Design a 8-bit ripple carry adder circuit using the full adders created in Lab 2.
2. Create a new project “adder8bit” in the same folder.
3. Inputs are
   - in1, in2: *in std_logic_vector(7 downto 0);*
   - ci: *in std_logic;*
   - sum: *out std_logic_vector(7 downto 0);*
   - co: *out std_logic;*

Step 2: 8-Bit Register

1. Design a synchronous 8-bit register circuit using VHDL. The register must send the input signal
to the output at the rising edge of the clock. The reset signal must be synchronous.

2. Create a new project “register8bit” in the same folder
3. Inputs are

- regin: *in std_logic_vector(7 downto 0);*
- clk, reset: *in std_logic;*
- regout: *out std_logic_vector(7 downto 0);*

Step 3: 8-Bit Accumulator

1. Design a synchronous 8-bit accumulator circuit. The reset signal must be synchronous.
2. Create a new project “accumulator” in the same folder
3. Inputs are

- data_in: *in std_logic_vector(7 downto 0);*
- clock, reset: *in std_logic;*
- data_out: *out std_logic_vector(7 downto 0);*

4. Four temporary signals are needed

- temp1 – for output of the 8-bit adder which in turn becomes input of the 8-bit register.
- temp2 – for the output of the 8-bit register which in turn becomes second input to the 8-bit adder.
- Cin: carry in signal which must be initialized to ground
- Cout: carry out signal from the 8-bit adder which is ignored.