

- A. This schedule is serializable and can occur in a scheme using 2PL protocol
  - B. This schedule is serializable but cannot occur in a scheme using 2PL protocol
  - C. This schedule is not serializable but can occur in a scheme using 2PL protocol
  - D. This schedule is not serializable and cannot occur in a scheme using 2PL protocol

Which of the following scenarios may lead to an irrecoverable error in a database system?

- A. A transaction writes a data item after it is read by an uncommitted transaction
  - B. A transaction reads a data item after it is read by an uncommitted transaction
  - C. A transaction reads a data item after it is written by a committed transaction
  - D. A transaction reads a data item after it is written by an uncommitted transaction

gate2003-cse databases transaction-and-concurrency easy isro2009

## Answer

3.17.3 Transaction And Concurrency: GATE CSE 2003 | Question: 87 top ↴

► <https://gateoverflow.in/970>



Consider three data items  $D1$ ,  $D2$ , and  $D3$ , and the following execution schedule of transactions  $T1$ ,  $T2$ , and  $T3$ . In the diagram,  $R(D)$  and  $W(D)$  denote the actions reading and writing the data item  $D$  respectively.

T1	T2	T3
R(D1); W(D1);	R(D3); R(D2); W(D2);	R(D2); R(D3);
R(D2); W(D2);	R(D1);	W(D2); W(D3);
		W(D1);

Which of the following statements is correct?

- A. The schedule is serializable as  $T_2; T_3; T_1$   
 B. The schedule is serializable as  $T_2; T_1; T_3$   
 C. The schedule is serializable as  $T_3; T_2; T_1$   
 D. The schedule is not serializable

gate2003-cse databases transaction-and-concurrency normal

Answer 

#### 3.17.4 Transaction And Concurrency: GATE CSE 2006 | Question: 20, ISRO2015-17 [top](#)

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Consider the following log sequence of two transactions on a bank account, with initial balance 12000, that transfer 2000 to a mortgage payment and then apply a 5% interest.

1. T1 start
2. T1 B old = 12000 new = 10000
3. T1 M old = 0 new = 2000
4. T1 commit
5. T2 start
6. T2 B old = 10000 new = 10500
7. T2 commit

Suppose the database system crashes just before log record 7 is written. When the system is restarted, which one statement is true of the recovery procedure?

- A. We must redo log record 6 to set B to 10500  
 B. We must undo log record 6 to set B to 10000 and then redo log records 2 and 3  
 C. We need not redo log records 2 and 3 because transaction T1 has committed  
 D. We can apply redo and undo operations in arbitrary order because they are idempotent

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gate2006-cse databases transaction-and-concurrency normal isro2015

Answer 

#### 3.17.5 Transaction And Concurrency: GATE CSE 2007 | Question: 64 [top](#)

https://gateoverflow.in/1262



Consider the following schedules involving two transactions. Which one of the following statements is TRUE?

- $S_1 : r_1(X); r_1(Y); r_2(X); r_2(Y); w_2(Y); w_1(X)$
- $S_2 : r_1(X); r_2(X); r_2(Y); w_2(Y); r_1(Y); w_1(X)$

- A. Both  $S_1$  and  $S_2$  are conflict serializable.  
 B.  $S_1$  is conflict serializable and  $S_2$  is not conflict serializable.  
 C.  $S_1$  is not conflict serializable and  $S_2$  is conflict serializable.  
 D. Both  $S_1$  and  $S_2$  are not conflict serializable.

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gate2007-cse databases transaction-and-concurrency normal

Answer 

#### 3.17.6 Transaction And Concurrency: GATE CSE 2009 | Question: 43 [top](#)

https://gateoverflow.in/1329



Consider two transactions  $T_1$  and  $T_2$ , and four schedules  $S_1, S_2, S_3, S_4$ , of  $T_1$  and  $T_2$  as given below:

$T_1 : R_1[x]W_1[x]W_1[y]$

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$T_2 : R_2[x]R_2[y]W_2[y]$

$S_1 : R_1[x]R_2[x]R_2[y]W_1[x]W_1[y]W_2[y]$

$S_2 : R_1[x]R_2[x]R_2[y]W_1[x]W_2[y]W_1[y]$

$S_3 : R_1[x]W_1[x]R_2[x]W_1[y]R_2[y]W_2[y]$

$S_4 : R_2[x]R_2[y]R_1[x]W_1[x]W_1[y]W_2[y]$

Which of the above schedules are conflict-serializable?

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- A.  $S_1$  and  $S_2$
- B.  $S_2$  and  $S_3$
- C.  $S_3$  only
- D.  $S_4$  only

gate2009-cse databases transaction-and-concurrency normal

Answer ↗

### 3.17.7 Transaction And Concurrency: GATE CSE 2010 | Question: 20

↗ <https://gateoverflow.in/2196>



Which of the following concurrency control protocols ensure both conflict serializability and freedom from deadlock?

- I. 2-phase locking
- II. Time-stamp ordering
  - A. I only
  - B. II only
  - C. Both I and II
  - D. Neither I nor II

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gate2010-cse databases transaction-and-concurrency normal

Answer ↗

### 3.17.8 Transaction And Concurrency: GATE CSE 2010 | Question: 42

↗ <https://gateoverflow.in/2343>



Consider the following schedule for transactions  $T1$ ,  $T2$  and  $T3$ :

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T1	T2	T3
Read(X)		
	Read(Y)	
		Read(Y)
	Write(Y)	
Write(X)		
	goclasses.in	Write(X)
	Read(X)	
	Write(X)	

Which one of the schedules below is the correct serialization of the above?

- A.  $T1 \rightarrow T3 \rightarrow T2$
- B.  $T2 \rightarrow T1 \rightarrow T3$
- C.  $T2 \rightarrow T3 \rightarrow T1$
- D.  $T3 \rightarrow T1 \rightarrow T2$

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gate2010-cse databases transaction-and-concurrency normal

Answer ↗

### 3.17.9 Transaction And Concurrency: GATE CSE 2012 | Question: 27

↗ <https://gateoverflow.in/1612>



Consider the following transactions with data items  $P$  and  $Q$  initialized to zero:

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$T_1$	read (P); read (Q); if P = 0 then Q := Q + 1; write (Q)
$T_2$	read (Q); read (P); if Q = 0 then P := P + 1; write (P)

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Any non-serial interleaving of **T1** and **T2** for concurrent execution leads to

- A. a serializable schedule
- B. a schedule that is not conflict serializable
- C. a conflict serializable schedule
- D. a schedule for which a precedence graph cannot be drawn

gate2012-cse   tests.gatecse.in   databases   transaction-and-concurrency   normal

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Answer 

### 3.17.10 Transaction And Concurrency: GATE CSE 2014 Set 1 | Question: 29 top ↗

<https://gateoverflow.in/1796>

Consider the following four schedules due to three transactions (indicated by the subscript) using *read* and *write* on a data item x, denoted by  $r(x)$  and  $w(x)$  respectively. Which one of them is conflict serializable?

- A.  $r_1(x); r_2(x); w_1(x); r_3(x); w_2(x);$
- B.  $r_2(x); r_1(x); w_2(x); r_3(x); w_1(x);$
- C.  $r_3(x); r_2(x); r_1(x); w_2(x); w_1(x);$
- D.  $r_2(x); w_2(x); r_3(x); r_1(x); w_1(x);$

gate2014-cse-set1   databases   transaction-and-concurrency   normal

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Answer 

### 3.17.11 Transaction And Concurrency: GATE CSE 2014 Set 2 | Question: 29 top ↗

<https://gateoverflow.in/1988>

Consider the following schedule S of transactions  $T_1, T_2, T_3, T_4$ :

<b>T1</b>	<b>T2</b>	<b>T3</b>	<b>T4</b>
Writes(X) Commit	Reads(X)  Writes(Y) Reads(Z) Commit	Writes(X) Commit  Reads(X) Reads(Y) Commit	

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Which one of the following statements is CORRECT?

- A. S is conflict-serializable but not recoverable
- B. S is not conflict-serializable but is recoverable
- C. S is both conflict-serializable and recoverable
- D. S is neither conflict-serializable nor is it recoverable

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gate2014-cse-set2 databases transaction-and-concurrency normal

Answer ↗

3.17.12 Transaction And Concurrency: GATE CSE 2014 Set 3 | Question: 29 [top ↵](#)



Consider the transactions  $T_1, T_2$ , and  $T_3$  and the schedules  $S_1$  and  $S_2$  given below.

- $T_1 : r1(X); r1(Z); w1(X); w1(Z)$
- $T_2 : r2(Y); r2(Z); w2(Z)$
- $T_3 : r3(Y); r3(X); w3(Y)$
- $S_1 : r1(X); r3(Y); r3(X); r2(Y); r2(Z); w3(Y); w2(Z); r1(Z); w1(X); w1(Z)$
- $S_2 : r1(X); r3(Y); r2(Y); r3(X); r1(Z); r2(Z); w3(Y); w1(X); w2(Z); w1(Z)$

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Which one of the following statements about the schedules is TRUE?

- A. Only  $S_1$  is conflict-serializable.
- B. Only  $S_2$  is conflict-serializable.
- C. Both  $S_1$  and  $S_2$  are conflict-serializable.
- D. Neither  $S_1$  nor  $S_2$  is conflict-serializable.

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gate2014-cse-set3 databases transaction-and-concurrency normal

Answer ↗

3.17.13 Transaction And Concurrency: GATE CSE 2015 Set 2 | Question: 1 [top ↵](#)



Consider the following transaction involving two bank accounts  $x$  and  $y$ .

```
read(x); x:=x-50; write(x); read(y); y:=y+50; write(y)
```

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The constraint that the sum of the accounts  $x$  and  $y$  should remain constant is that of

- A. Atomicity
- B. Consistency
- C. Isolation
- D. Durability

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gate2015-cse-set2 databases transaction-and-concurrency easy

Answer ↗

3.17.14 Transaction And Concurrency: GATE CSE 2015 Set 2 | Question: 46 [top ↵](#)



Consider a simple checkpointing protocol and the following set of operations in the log.

```
(start, T4); (write, T4, y, 2, 3); (start, T1); (commit, T4); (write, T1, z, 5, 7);  
(checkpoint);  
(start, T2); (write, T2, x, 1, 9); (commit, T2); (start, T3); (write, T3, z, 7, 2);
```

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If a crash happens now and the system tries to recover using both undo and redo operations, what are the contents of the undo list and the redo list?

- A. Undo: T3, T1; Redo: T2
- B. Undo: T3, T1; Redo: T2, T4
- C. Undo: none; Redo: T2, T4, T3, T1
- D. Undo: T3, T1, T4; Redo: T2

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gate2015-cse-set2 databases transaction-and-concurrency normal

Answer 

3.17.15 Transaction And Concurrency: GATE CSE 2015 Set 3 | Question: 29 [top](#)

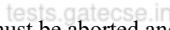
<https://gateoverflow.in/8482>



Consider the partial Schedule  $S$  involving two transactions  $T_1$  and  $T_2$ . Only the *read* and the *write* operations have been shown. The *read* operation on data item  $P$  is denoted by *read*( $P$ ) and *write* operation on data item  $P$  is denoted by *write*( $P$ ).  

Time Instance	Schedule S	
	T1	T2
1	read(A)	
2	write(A)	
3		read(C)
tests.gatecse.in	4	write(C)
	5	read(B)
	6	write(B)
	7	read(A)
	8	commit
	9	read(B)

Suppose that the transaction  $T_1$  fails immediately after time instance 9. Which of the following statements is correct?

-   
- A.  $T_2$  must be aborted and then both  $T_1$  and  $T_2$  must be re-started to ensure transaction atomicity
  - B. Schedule  $S$  is non-recoverable and cannot ensure transaction atomicity
  - C. Only  $T_2$  must be aborted and then re-started to ensure transaction atomicity
  - D. Schedule  $S$  is recoverable and can ensure transaction atomicity and nothing else needs to be done

[gate2015-cse-set3](#) databases transaction-and-concurrency normal

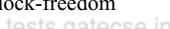
Answer 

3.17.16 Transaction And Concurrency: GATE CSE 2016 Set 1 | Question: 22 [top](#)

<https://gateoverflow.in/39644>



Which one of the following is NOT a part of the ACID properties of database transactions?

-   
- A. Atomicity
  - B. Consistency
  - C. Isolation
  - D. Deadlock-freedom

[gate2016-cse-set1](#) databases transaction-and-concurrency easy

Answer 

3.17.17 Transaction And Concurrency: GATE CSE 2016 Set 1 | Question: 51 [top](#)

<https://gateoverflow.in/39703>



Consider the following two phase locking protocol. Suppose a transaction  $T$  accesses (for read or write operations), a certain set of objects  $\{O_1, \dots, O_k\}$ . This is done in the following manner:

-   
- Step 1.  $T$  acquires exclusive locks to  $O_1, \dots, O_k$  in increasing order of their addresses.
  - Step 2. The required operations are performed .
  - Step 3. All locks are released

This protocol will

-   
- A. guarantee serializability and deadlock-freedom
  - B. guarantee neither serializability nor deadlock-freedom
  - C. guarantee serializability but not deadlock-freedom
  - D. guarantee deadlock-freedom but not serializability.

[gate2016-cse-set1](#) databases transaction-and-concurrency normal

Answer 



Suppose a database schedule  $S$  involves transactions  $T_1, \dots, T_n$ . Construct the precedence graph of  $S$  with vertices representing the transactions and edges representing the conflicts. If  $S$  is serializable, which one of the following orderings of the vertices of the precedence graph is guaranteed to yield a serial schedule?

- A. Topological order
- B. Depth-first order
- C. Breadth- first order
- D. Ascending order of the transaction indices

[gate2016-cse-set2](#) [databases](#) [transaction-and-concurrency](#) [normal](#)

Answer



Consider the following database schedule with two transactions  $T_1$  and  $T_2$ .

$$S = r_2(X); r_1(X); r_2(Y); w_1(X); r_1(Y); w_2(X); a_1; a_2$$

Where  $r_i(Z)$  denotes a read operation by transaction  $T_i$  on a variable  $Z$ ,  $w_i(Z)$  denotes a write operation by  $T_i$  on a variable  $Z$  and  $a_i$  denotes an abort by transaction  $T_i$ .

Which one of the following statements about the above schedule is TRUE?

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- A.  $S$  is non-recoverable.
- B.  $S$  is recoverable, but has a cascading abort.
- C.  $S$  does not have a cascading abort.
- D.  $S$  is strict.

[gate2016-cse-set2](#) [databases](#) [transaction-and-concurrency](#) [normal](#)

Answer



Consider the following two statements about database transaction schedules:

- I. Strict two-phase locking protocol generates conflict serializable schedules that are also recoverable.
- II. Timestamp-ordering concurrency control protocol with Thomas' Write Rule can generate view serializable schedules that are not conflict serializable

Which of the above statements is/are TRUE?

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- A. I only
- B. II only
- C. Both I and II
- D. Neither I nor II

[gate2019-cse](#) [databases](#) [transaction-and-concurrency](#)

Answer



Consider a schedule of transactions  $T_1$  and  $T_2$ :

$T_1$	$RA$			$RC$		$WD$		$WB$	Commit
$T_2$		$RB$	$WB$		$RD$		$WC$		Commit

Here, RX stands for “Read(X)” and WX stands for “Write(X)”. Which one of the following schedules is conflict equivalent to the above schedule?

- |       |      |      |      |      |      |      |      |  |        |
|-------|------|------|------|------|------|------|------|--|--------|
| $T_1$ |      |      |      | $RA$ | $RC$ | $WD$ | $WB$ |  | Commit |
| $T_2$ | $RB$ | $WB$ | $RD$ |      |      |      | $WC$ |  | Commit |
- |       |      |      |      |      |      |      |      |        |        |
|-------|------|------|------|------|------|------|------|--------|--------|
| $T_1$ | $RA$ | $RC$ | $WD$ | $WB$ |      |      |      | Commit |        |
| $T_2$ |      |      |      | $RB$ | $WB$ | $RD$ | $WC$ |        | Commit |
- A. 

$T_1$				$RA$	$RC$	$WD$	$WB$		Commit
$T_2$	$RB$	$WB$	$RD$				$WC$		Commit

B. 

$T_1$	$RA$	$RC$	$WD$	$WB$				Commit	
$T_2$				$RB$	$WB$	$RD$	$WC$		Commit

C.	<table border="1"> <tr><td><math>T_1</math></td><td><math>RA</math></td><td><math>RC</math></td><td><math>WD</math></td><td></td><td></td><td></td><td><math>WB</math></td><td></td><td>Commit</td><td></td></tr> </table>	$T_1$	$RA$	$RC$	$WD$				$WB$		Commit	
$T_1$	$RA$	$RC$	$WD$				$WB$		Commit			
	<table border="1"> <tr><td><math>T_2</math></td><td></td><td></td><td></td><td><math>RB</math></td><td><math>WB</math></td><td><math>RD</math></td><td></td><td><math>WC</math></td><td></td><td>Commit</td></tr> </table>	$T_2$				$RB$	$WB$	$RD$		$WC$		Commit
$T_2$				$RB$	$WB$	$RD$		$WC$		Commit		
D.	<table border="1"> <tr><td><math>T_1</math></td><td></td><td></td><td></td><td></td><td><math>RA</math></td><td><math>RC</math></td><td><math>WD</math></td><td><math>WB</math></td><td>Commit</td><td></td></tr> </table>	$T_1$					$RA$	$RC$	$WD$	$WB$	Commit	
$T_1$					$RA$	$RC$	$WD$	$WB$	Commit			
	<table border="1"> <tr><td><math>T_2</math></td><td><math>RB</math></td><td><math>WB</math></td><td><math>RD</math></td><td><math>WC</math></td><td></td><td></td><td></td><td></td><td></td><td>Commit</td></tr> </table>	$T_2$	$RB$	$WB$	$RD$	$WC$						Commit
$T_2$	$RB$	$WB$	$RD$	$WC$						Commit		

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gate2020-cse databases transaction-and-concurrency

Answer ↗

### 3.17.22 Transaction And Concurrency: GATE CSE 2021 Set 1 | Question: 13

↪ <https://gateoverflow.in/357439>



Suppose a database system crashes again while recovering from a previous crash. Assume checkpointing is not done by the database either during the transactions or during recovery.

Which of the following statements is/are correct?

- A. The same undo and redo list will be used while recovering again
- B. The system cannot recover any further
- C. All the transactions that are already undone and redone will not be recovered again
- D. The database will become inconsistent

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gate2021-cse-set1 multiple-selects databases transaction-and-concurrency

Answer ↗

### 3.17.23 Transaction And Concurrency: GATE IT 2004 | Question: 21

↪ <https://gateoverflow.in/3662>



Which level of locking provides the highest degree of concurrency in a relational database ?

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- A. Page
- B. Table
- C. Row
- D. Page, table and row level locking allow the same degree of concurrency

gate2004-it databases normal transaction-and-concurrency

Answer ↗

### 3.17.24 Transaction And Concurrency: GATE IT 2004 | Question: 77

↪ <https://gateoverflow.in/3721>



Consider the following schedule  $S$  of transactions  $T_1$  and  $T_2$  :

$T_1$	$T_2$
Read(A) $A = A - 10$	
	Read(A) $Temp = 0.2 * A$ Write(A) Read(B)
Write(A) Read(B) $B = B + 10$ Write(B)	$B = B + Temp$ Write(B)

Which of the following is TRUE about the schedule  $S$  ?

- A.  $S$  is serializable only as  $T_1, T_2$
- B.  $S$  is serializable only as  $T_2, T_1$
- C.  $S$  is serializable both as  $T_1, T_2$  and  $T_2, T_1$

- D.  $S$  is not serializable either as  $T1, T2$  or as  $T2, T1$

gate2004-it databases transaction-and-concurrency normal

Answer 

**3.17.25 Transaction And Concurrency: GATE IT 2005 | Question: 24** top ↗

<https://gateoverflow.in/3769>



Amongst the ACID properties of a transaction, the 'Durability' property requires that the changes made to the database by a successful transaction persist

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- A. Except in case of an Operating System crash
- B. Except in case of a Disk crash
- C. Except in case of a power failure
- D. Always, even if there is a failure of any kind

gate2005-it databases transaction-and-concurrency easy

Answer 

**3.17.26 Transaction And Concurrency: GATE IT 2005 | Question: 67** top ↗

<https://gateoverflow.in/3830>



A company maintains records of sales made by its salespersons and pays them commission based on each individual's total sales made in a year. This data is maintained in a table with following schema:

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$\text{salesinfo} = (\text{salespersonid}, \text{totalsales}, \text{commission})$

In a certain year, due to better business results, the company decides to further reward its salespersons by enhancing the commission paid to them as per the following formula:

If  $\text{commission} \leq 50000$ , enhance it by 2%

If  $50000 < \text{commission} \leq 100000$ , enhance it by 4%

If  $\text{commission} > 100000$ , enhance it by 6%

The IT staff has written three different SQL scripts to calculate enhancement for each slab, each of these scripts is to run as a separate transaction as follows:

T1

```
Update salesinfo
Set commission = commission * 1.02
Where commission <= 50000;
```

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T2

```
Update salesinfo
Set commission = commission * 1.04
Where commission > 50000 and commission is <= 100000;
```

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T3

```
Update salesinfo
Set commission = commission * 1.06
Where commission > 100000;
```

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Which of the following options of running these transactions will update the commission of all salespersons correctly

- A. Execute T1 followed by T2 followed by T3
- B. Execute T2, followed by T3; T1 running concurrently throughout
- C. Execute T3 followed by T2; T1 running concurrently throughout
- D. Execute T3 followed by T2 followed by T1

gate2005-it databases transaction-and-concurrency normal

Answer 

**3.17.27 Transaction And Concurrency: GATE IT 2007 | Question: 66** top ↗

<https://gateoverflow.in/3511>



Consider the following two transactions:  $T1$  and  $T2$ .

$T1 :$	read (A);	$T2 :$	read (B);
	read (B);		read (A);
	If $A = 0$ then $B \leftarrow B + 1$ ;		If $B \neq 0$ then $A \leftarrow A - 1$ ;
	write (B);		write (A);

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Which of the following schemes, using shared and exclusive locks, satisfy the requirements for strict two phase locking for the above transactions?

	$S_1 :$	lock S(A); read (A); lock S(B); read (B); If $A = 0$ then $B \leftarrow B + 1;$ write (B); commit; unlock (A); unlock (B);	$S_2 :$	lock S(B); read (B); lock S(A); read (A); If $B \neq 0$ then $A \leftarrow A - 1;$ write (A); commit; unlock (B); unlock (A);	tests.gatecse.in	goclasses.in	tests.gatecse.in
	$S_1 :$	lock X(A); read (A); lock X(B); read (B); If $A = 0$ then $B \leftarrow B + 1;$ write (B); unlock (A); commit; unlock (B);	$S_2 :$	lock X(B); read (B); lock X(A); read (A); If $B \neq 0$ then $A \leftarrow A - 1;$ write (A); unlock (A); commit; unlock (A);	tests.gatecse.in	goclasses.in	tests.gatecse.in
	$S_1 :$	lock S(A); read (A); lock X(B); read (B); If $A = 0$ then $B \leftarrow B + 1;$ write (B); unlock (A); commit; unlock (B);	$S_2 :$	lock S(B); read (B); lock X(A); read (A); If $B \neq 0$ then $A \leftarrow A - 1;$ write (A); unlock (B); commit; unlock (A);	tests.gatecse.in	goclasses.in	tests.gatecse.in
	$S_1 :$	lock S(A); read (A); lock X(B); read (B); If $A = 0$ then $B \leftarrow B + 1;$ write (B); unlock (A); commit; unlock (B);	$S_2 :$	lock S(B); read (B); lock X(A); read (A); If $B \neq 0$ then $A \leftarrow A - 1;$ write (A); unlock (B); commit; unlock (A);	tests.gatecse.in	goclasses.in	tests.gatecse.in
D.	$S_1 :$	lock S(A); read (A); lock X(B); read (B); If $A = 0$ then $B \leftarrow B + 1;$ write (B); unlock (A); unlock (B); commit;	$S_2 :$	lock S(B); read (B); lock X(A); read (A); If $B \neq 0$ then $A \leftarrow A - 1;$ write (A); unlock (A); unlock (A); commit;	tests.gatecse.in	goclasses.in	tests.gatecse.in

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gate2007-it databases transaction-and-concurrency normal

Answer ↗

3.17.28 Transaction And Concurrency: GATE IT 2008 | Question: 63 top ↗

↗ <https://gateoverflow.in/3374>



Consider the following three schedules of transactions T1, T2 and T3. [Notation: In the following NYO represents the action Y (R for read, W for write) performed by transaction N on object O.]

(S1)	2RA	2WA	3RC	2WB	3WA	3WC	1RA	1RB	1WA	1WB
(S2)	3RC	2RA	2WA	2WB	3WA	1RA	1RB	1WA	1WB	3WC
(S3)	2RA	3RC	3WA	2WA	2WB	3WC	1RA	1RB	1WA	1WB

Which of the following statements is TRUE?

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- A. S1, S2 and S3 are all conflict equivalent to each other
- B. No two of S1, S2 and S3 are conflict equivalent to each other
- C. S2 is conflict equivalent to S3, but not to S1
- D. S1 is conflict equivalent to S2, but not to S3

gate2008-it databases transaction-and-concurrency normal

Answer 

#### Answers: Transaction And Concurrency

##### 3.17.1 Transaction And Concurrency: GATE CSE 1999 | Question: 2.6

<https://gateoverflow.in/1484>



If we draw the precedence graph we get a loop, and hence the schedule is not conflict serializable.

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There is no blind write too so, there is no chance that view serializability can occur.

Now 2pl ensures CS.

Since possibility of CS is ruled out at the onset, so schedule cannot occur in 2PL.

Ans d)

 42 votes

-- Sourav Roy (2.9k points)

##### 3.17.2 Transaction And Concurrency: GATE CSE 2003 | Question: 29, ISRO2009-73

<https://gateoverflow.in/919>



- ✓ A. Here if transaction writing data commits, then transaction which read the data might get phantom tuple/ Unrepeatable error. Though there is no irrecoverable error possible even in this option.
- B. This is non issue. Both transaction reading data.
- C. This is non issue.
- D. This is dirty read. In case if transaction reading uncommitted data commits, irrecoverable error occurs of uncommitted transaction fails. So (D) is answer

 42 votes

-- Akash Kanase (36k points)

##### 3.17.3 Transaction And Concurrency: GATE CSE 2003 | Question: 87

<https://gateoverflow.in/970>



- ✓ There is a cycle in precedence graph so schedule is not conflict serialisable.

Check View Serializability:

Checking View Serializability is NPC problem so proving by contradiction..

1. Initial Read  
T2 read D2 value from initial database and T1 modify D2 so T2 should execute before T1.  
i.e., T2 → T1
2. Final write.  
final write of D1 in given schedule done by T2 and T1 modify D1 i.e. W(D1)..  
that means T2 should execute after T1.  
i.e., T1 → T2

So, schedule not even View Serializable.

Not Serializable.

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Correct Answer: D

39 votes

-- Digvijay (44.9k points)

3.17.4 Transaction And Concurrency: GATE CSE 2006 | Question: 20, ISRO2015-17 [top](#)

<https://gateoverflow.in/981>



- ✓ Answer should be **B**. Here we are not using checkpoints so, redo log records 2 and 3 and undo log record 6. Consider the following steps taken from the book 'Navathe':

PROCEDURE RIU\_M

1. Use two lists of transactions maintained by the system: the committed transactions since the last checkpoint and the active transactions
2. Undo all the *write\_item* operations of the *active* (uncommitted) transaction, using the UNDO procedure. The operations should be undone in the reverse order in which they were written into the log.
3. Redo all the *write\_item* operations of the *committed* transactions from the log, in the order in which they were written into the log.

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105 votes

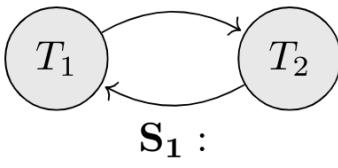
-- Pooja Palod (24.1k points)

3.17.5 Transaction And Concurrency: GATE CSE 2007 | Question: 64 [top](#)

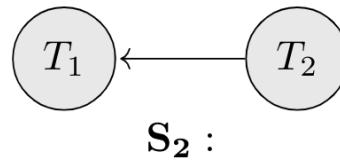
<https://gateoverflow.in/1262>



- For  $S_1$  : it is **not conflict serializable**
- For  $S_2$  : it is **conflict serializable**



**S<sub>1</sub>** :



**S<sub>2</sub>** :

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Answer is option **C**.

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28 votes

-- Amar Vashishth (25.2k points)

3.17.6 Transaction And Concurrency: GATE CSE 2009 | Question: 43 [top](#)

<https://gateoverflow.in/1329>



- ✓ The answer is B.

- S1 has a cycle from  $T1 \rightarrow T2$  and  $T2 \rightarrow T1$ .
- S2-- It is uni-directional and has only  $T2 \rightarrow T1$ .
- S3-- It is uni-directional and has only  $T1 \rightarrow T2$ .
- S4-- same as S1.

A schedule is conflict serializable if there is no cycle in the directed graph made by the schedules.

In the schedules we check for RW, WR, WW conflicts between the schedules and only these conflicts contribute in the edges of the graph.

26 votes

-- Gate Keeda (15.9k points)

3.17.7 Transaction And Concurrency: GATE CSE 2010 | Question: 20 [top](#)

<https://gateoverflow.in/2196>



- ✓ In basic two phase locking there is a chance for deadlock

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Conservative 2pl is deadlock free

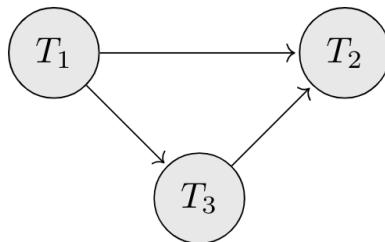
I go with B.

49 votes

-- Sankaranarayanan P.N (8.5k points)



- ✓ Answer is option A.  
create precedence graph and apply [Topological sort](#) on it to obtain  
 $T_1 \rightarrow T_3 \rightarrow T_2$



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## References



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[42 votes](#)

-- Amar Vashishth (25.2k points)



- ✓ Answer is (B). Explanation:  $T_1 : r(P), r(Q), w(Q)$   $T_2 : r(Q), r(P), w(P)$  now, consider any non serial schedule for example,  $S : r_1(P), r_2(Q), r_1(Q), r_2(P), w_1(Q), w_2(P)$  now, draw a precedence graph for this schedule. here there is a conflict from  $T_1 -> T_2$  and there is a conflict from  $T_2 -> T_1$  therefore, the graph will contain a cycle. so we can say that the schedule is not conflict serializable.

[68 votes](#)

-- jayendra (6.7k points)



- ✓ (D) make precedence graph for all the options, for option (D) only graph will be acyclic, hence (D) is CSS.

[22 votes](#)

-- Manu Thakur (34k points)



- ✓ Answer: S is both conflict serializable and recoverable.

Recoverable? Look if there are any dirty reads? Since there are no dirty read, it simply implies schedule is recoverable( if there were dirty read, then we would have taken into consideration the order in which transactions commit)

Conflict serializable? Draw the precedence graph( make edges if there is a conflict instruction among  $T_i$  and  $T_j$ . But for the given schedule, no cycle exists in precedence graph, thus it's conflict serializable.

Hope this helps.

[50 votes](#)

-- Ramandeep Singh (131 points)

Even though [@Ramandeep Singh](#) has answered this question, I'd like to add some additional points because in the comments and discussion on this question, many students are having incorrect arguments which they think are correct.

The Mistake that most students are doing (in the comments to this question) is that they are Not making correct Precedence Graph because they are not making conflict edges in the Precedence graph "from a committed transaction to a newly started transaction"....which is completely wrong because if you do so then How will you make Precedence Graph for Serial Schedule??

Following all the definitions and concepts are directly (without modification) picked mostly from **Navathe** and some from the following link : <http://www.ict.griffith.edu.au/~rwt/uec/1.1.ccc.html>

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Refer Navathe if you still have some doubt.

### Transactions :

A **transaction** is effectively a sequence of read and write operations on atomic database items. A transaction may be incomplete because the (database) system crashes, or because it is *aborted* by either the system or the user (or application). Complete transactions are *committed*. **Transactions must terminate by either aborting or committing.**

### Complete Schedule :

A schedule  $S$  of  $n$  transactions  $T_1, T_2, \dots, T_n$  is said to be a complete schedule if the following conditions hold:

1. The operations in  $S$  are exactly those operations in  $T_1, T_2, \dots, T_n$ , **including a commit or abort operation as the last operation for each transaction in the schedule.**
2. For any pair of operations from the same transaction  $T_i$ , their relative order of appearance in  $S$  is the same as their order of appearance in  $T_i$ . (i.e Operation order in/of every transaction must preserve.)
3. For any two conflicting operations, one of the two must occur before the other in the schedule.

Condition 1 simply states that all operations in the transactions must appear in the complete schedule. Since every transaction has either committed or aborted, **a complete schedule will not contain any active transactions at the end of the schedule.**

In general, it is difficult to encounter complete schedules in a transaction processing system because new transactions are continually being submitted to the system. Hence, it is useful to define the concept of the committed projection  $C(S)$  of a schedule  $S$ .

### Committed Projection of a schedule :

Committed Projection  $C(S)$  of a schedule  $S$  includes only the operations in  $S$  that belong to **committed transactions**—that is, transactions  $T_i$  whose commit operation  $C_i$  is in  $S$ .

Given a schedule  $S$ , the committed projection  $C(S)$  is the subset of  $S$  consisting of operations ( $r1(X), w2(Y)$ , etc) that are part of transactions that have committed (that is,  $r1(X)$  would be part of  $C(S)$  only if transaction 1's commit,  $c1$ , were also part of  $S$ ). This is sometimes useful in analyzing schedules when transactions are continuously being added.

A committed projection  $C(S)$  of a schedule  $S$  includes the operations in  $S$  only from the committed transactions. Let's take an example :

Transactions:

- $T_1 : r1(X); w1(X); r1(Y); w1(Y); c1;$
- $T_2 : r2(Y); w2(Y); a2;$
- $T_3 : r3(X); w3(X);$
- $S_1 : r1(X); r2(Y); w1(X); w2(Y); r1(Y); a2; w1(Y); c1; r3(X); w3(X);$

Then  $C(S_1) = ??$

Well,  $C(S_1)$  will be the same as  $T_1$  because  $T_3$  has No Commit/Abort operation as the last operation of the transaction and  $T_2$  is Not committed. So, by the definition of Committed Transaction,  $C(S_1) = T_1$ .

Now, as according to Navathe,

We can theoretically define a schedule  $S$  to be serializable if its committed projection  $C(S)$  is equivalent to some serial schedule, since only committed transactions are guaranteed by the DBMS.

And It applies to both Conflict and View Serializability.

A schedule is *serialisable* if the effect of its committed projection (the restriction to its committed transactions) on any consistent database is identical to that of some serial schedule of its committed transactions.

### (Conflict) Serialisability theorem :

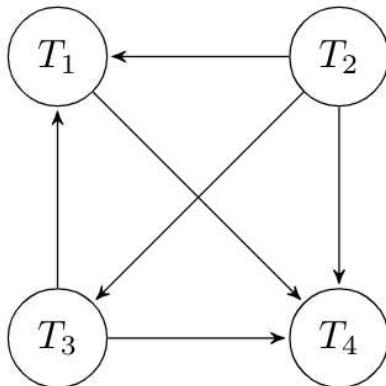
Given a schedule  $S$ , define the serialisation graph(Precedence Graph)  $SG(S)$  to have the committed transactions of  $S$  as its nodes, and a directed edge from  $T_1$  to  $T_2$  if  $T_1$  and  $T_2$  contain conflicting operations  $O_1$  and  $O_2$  such that  $O_1$  precedes  $O_2$  in  $S$ . Then  $S$  is serialisable if and only if  $SG(S)$  is acyclic.

<http://www.ict.griffith.edu.au/~rwt/uoe/1.1.ccc.html>

Now, coming to the given question :

The given schedule is Complete Schedule as all the transactions in the schedule are committed(or aborted). Moreover, the given schedule is Committed Projection of itself as well because all the Transactions are committed. Now, as the above definition of Conflict serializability suggests, we make Precedence graph for this schedule and in the precedence graph, the Nodes will be the Transactions participating in the committed projection of the schedule(which is same as the given schedule ) ..

The precedence graph will be as following :



From the precedence graph we can see that Only One serial schedule is conflict equivalent to the given schedule which is  $T_2, T_3, T_1, T_4, \dots$ . No other schedule is conflict equivalent to the given schedule.

Only One serial schedule is conflict equivalent to the given schedule which is  $T_2, T_3, T_1, T_4, \dots$ . This makes sense because  $T_2$  is reading the initial value of data item  $X$  (directly from the database) But if we run either of  $T_3$  or  $T_1$  before  $T_2$  then they will write the data item  $X$  and  $T_2$  will have to read the modified value of  $X$ . Hence, Only one Serial Schedule can be equivalent to the given schedule and that is  $T_2, T_3, T_1, T_4$ .

The Mistake that most students are doing (in the comments to this question) is that they are Not making correct Precedence Graph because they are not making conflict edges from a committed transaction to a new started transaction....which is completely wrong because if you do so then How will you make Precedence Graph for Serial Schedule??

**Serial Schedule (Definition as it is given in Navathe)** : Formally, a schedule S is serial if, for every transaction T participating in the schedule, all the operations of T are executed consecutively in the schedule; otherwise, the schedule is called nonserial. Therefore, in a serial schedule, only one transaction at a time is active—**the commit (or abort) of the active transaction initiates execution of the next transaction**. No interleaving occurs in a serial schedule.

$$S = R_1(X) W_1(X) C_1 R_2(X) W_2(X) C_2 R_3(X) W_3(X) C_3$$

If you make precedence graph for this schedule, then you must get a acyclic precedence graph But those students who are not putting conflict edges in the precedence graph "from a committed transaction to a newly started transaction" then you won't get any edges in this graph and the graph will be empty graph, which you know is not correct.

Consider this schedule :

<b>T1</b>	<b>T2</b>	<b>T3</b>
	Write(X)	
Writes(Z)		
Writes(X)		
<b>Commit</b>		
	Writes(Y)	
	Reads(Y)	
		Writes(Z)
		Writes(M)
		<b>Commit</b>
	Reads(M)	
	<b>Commit</b>	

Try to find whether this schedule is Conflict Serializable Or Not??

If you do it correctly, It is Not conflict serializable because there is Cycle in the precedence graph of this schedule. But If you don't put conflict edges in the precedence graph "from a committed transaction ( $T_1$ ) to a newly started transaction ( $T_3$ )" then you won't get edge  $T_1 \rightarrow T_3$  in the precedence graph and hence, you will incorrectly get the answer as Conflict serializable.

#### References



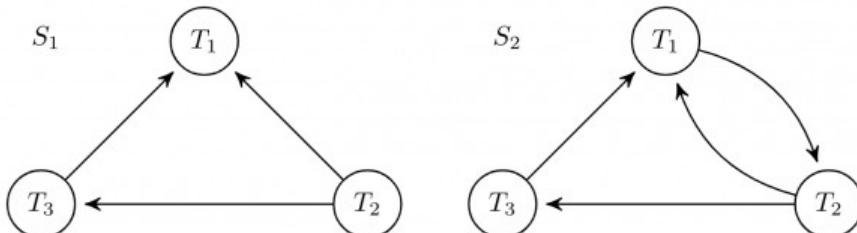
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45 votes

-- Deepak Poonia (23.4k points)

3.17.12 Transaction And Concurrency: GATE CSE 2014 Set 3 | Question: 29 top<https://gateoverflow.in/2063>\$S\_1\$ has no cycle hence, **Conflict-Serializable**\$S\_2\$ has cycle hence **NOT Conflict-Serializable**

Answer is option A.

37 votes

-- Amar Vashishth (25.2k points)

3.17.13 Transaction And Concurrency: GATE CSE 2015 Set 2 | Question: 1 top<https://gateoverflow.in/8047>

B. Consistency

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In the given transaction Atomicity guarantees that the said constraint is satisfied. But this constraint is not part of Atomicity property. It is just that Atomicity implies Consistency here.

23 votes

-- Arjun Suresh (332k points)

3.17.14 Transaction And Concurrency: GATE CSE 2015 Set 2 | Question: 46 top<https://gateoverflow.in/8246>

T1	T2	T3	T4
			start
			w(y, 2, 3)
start		gateoverflow.in	
			commit
w(z, 5, 7)			
checkpoint	checkpoint	checkpoint	checkpoint
	start		
	w(x, 1, 9)		
	commit		
		start	
		w(z, 7, 2)	
crash	crash	crash	crash

Now from the table we can find that \$T\_1\$ and \$T\_3\$ has uncommitted write operation, so they must be undone. Even though \$T\_2\$ has committed after writing, but it is after checkpoint. So, it needs to be redone.

Answer is A.

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71 votes

-- worst\_engineer (2.8k points)



- ✓ The correct option is B.

Why A is not correct because it says abort transaction T2 and then redo all the operations .

But is there a guarantee that it will succeed this time ??(no maybe again T1 will fail).

Now as to why b is correct because as the other answer points out it is by definition an irrecoverable schedule now even if we start to undo the actions on by one(after t1 fails) in order to ensure transaction atomicity. Still we cannot undo a committed transaction. Hence, this schedule is unrecoverable by definition and also not atomic since it leaves the data base in an inconsistent state.

66 votes

-- Tamojit Chatterjee (1.9k points)



- ✓ A - Atomicity
- C - Consistency
- I - Isolation
- D - Durability.

Answer (D)

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33 votes

-- Abhilash Panicker (7.6k points)



- ✓ Two Phase Locking protocol is conflict serializable. So this is a modified version of the basic 2PL protocol, So serializability should be guaranteed.. and we can get a serializable scheduling by ordering based on Lock points(same as in basic 2PL )..

Now in Step 1, exclusive locks are acquired to  $O_1, O_2, O_3 \dots$  in increasing order of addresses..since it is mentioned as exclusive lock, only one transaction can lock the object..

Due to acquiring of locks based on ordering of addresses.. and locks aren't released until the transaction completes its operation.. we can prevent the circular wait condition, and hence making it deadlock free.

So, the answer should be (A) guarantees serializability and deadlock freedom

78 votes

-- Abhilash Panicker (7.6k points)



- ✓ Topological Order.

24 votes

-- Sharathkumar Anbu (595 points)



- ✓ Answer is C

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T1	T2
R(x)	R(x)
R(x)	R(y)
W(x)	
R(y)	W(x)
a1	a2

(A): This is not possible, because we have no dirty read ! No dirty read  $\implies$  Recoverable

(B): This is not possible, because of no Dirty read ! No dirty read  $\implies$  No cascading aborts !

(D): This is not true, because we can see clearly in image that after W1(X) before T1 commit or aborts T2 does W2(x) !

C is only option remaining !

1 like 62 votes

-- Akash Kanase (36k points)

### 3.17.20 Transaction And Concurrency: GATE CSE 2019 | Question: 11 top

<https://gateoverflow.in/30283>



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1. Strict 2PL allows only schedules whose precedence graph is acyclic i.e. schedule is Conflict Serial. In 2PL, transactions do not release exclusive locks until the transaction has committed or aborted i.e. schedule is recoverable.
2. Time stamp ordering schedule with Thomas write rule generate View serial schedule with BLIND WRITE. Because of BLIND WRITE it won't be Conflict Serial.

So, Option C - both are true

1 like 41 votes

-- Digvijay (44.9k points)

### 3.17.21 Transaction And Concurrency: GATE CSE 2020 | Question: 37 top

<https://gateoverflow.in/333194>



- ✓ If you draw the dependency graph, you'll notice that there is a cycle. Hence **Option (D)** and **Option (B)** are straightaway False.

Now in **Option (C)**, there is a swapping operation of conflicting operations  $W_1(D)$  and  $R_2(D)$ . Hence it's **False** as well.

Hence, **Option(A)** is the answer

1 like 8 votes

-- Debasish Das (1.5k points)

### 3.17.22 Transaction And Concurrency: GATE CSE 2021 Set 1 | Question: 13 top

<https://gateoverflow.in/357439>



- ✓ Answer: A

**Ideation/Source of the content:** Navathe 6th Edition, 22.1: Recovery Concepts

**Explanation:**

**Support for option A and against option C:** Since check-pointing is not used we have to depend on the system logs. Let's suppose we have three transactions A, B and C. Also assume that transaction A and C commits before failure and B was started but the system crashed before it can commit. So, in the first recovery process database will redo A and C as per the system logs. Now consider that while redoing A successfully commits, the system crashed for the second time before the B can commit. So, while recovering for the second time the same system logs will be used. However, it is should be noted that the system logs will also have entry to redo transaction A since it was committed after the first failure. However, the undo/redo operations are idempotent (they are the same no matter how many time they are executed).

**Against option B:** If the system crashes again same logic as above can be used for recovery.

**Against option D:** Inconsistency refers to situations (generally) when the value of a shared variable varies in two or more transactions, but that doesn't seem to happen here as no uncommitted transaction's data is being read/written during the entire recovery process.

**Conclusion:** So, the only option of selecting the same list for undo/redo seems to be correct.

1 like 1 votes

-- Abhishek Dutta (145 points)

### 3.17.23 Transaction And Concurrency: GATE IT 2004 | Question: 21 top

<https://gateoverflow.in/3662>



- ✓ Row level locking provides more concurrency, because different transactions can access different rows in a table / page at same time,

Correct Answer: C

1 like 41 votes

-- Sankaranarayanan P.N (8.5k points)



- ✓ There is a cycle in the precedence graph - so the given schedule is not Conflict Serializable.

If a schedule is view serializable but not conflict serializable it MUST have one or more blind writes. Here, there is no blind writes. So, the given schedule is not even view serializable.

Option D is the Answer.

51 votes

-- Sandeep\_Uniyal (6.5k points)



- ✓ Answer d. Irrespective of any failure the successful result of transaction should persist.

Suppose we book ticket 2 months in advance in irctc and transaction success.

Then when we are going to board the train on that time they tells because of system/disk/power crash they dont have your seat information and you are not allowed in the seat.

it is a serious problem. hence result should persist irrespective of all crashes.

89 votes

-- Sankaranarayanan P.N (8.5k points)



- ✓ Correct Answer : D

$T_3$  followed by  $T_2$  followed by  $T_1$  will be correct execution sequence:

other cases some people will get two times increment

eg. if we have  $T_1$  followed by  $T_2$

if initial commision is 49500

then he is belonging to < 50000

hence,  $49500 * 1.02 = 50490$

now, he is eligible in second category

then,  $50490 * 1.04 = 52509.6$

so, he wil get increment two times. but he is eligible for only one slab of commision.

91 votes

-- Sankaranarayanan P.N (8.5k points)



- ✓ Answer is (C).

Many of you would point a DEADLOCK and I won't deny But see Question just asks for requirement to follow Strict 2PL. Requirement are

1. Exclusive locks should be released after the commit.
2. No Locking can be done after the first Unlock and vice versa.

In 2PL deadlock may occur BUT it may be that it doesn't occur at all.

Consider that in option (C) if both execute in serial order without concurrency. Then that is perfectly valid and YES it follows Strict 2PL.

50 votes

-- Sandeep\_Uniyal (6.5k points)



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Two schedules are conflict equivalent if we can derive one schedule by swapping the non-conflicting operations of the other schedule.

**S1**

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T1	T2	T3
	R(A)	
	W(A)	
		R(C)
		W(B)
		W(A)
		W(C)
R(A)		
R(B)		
W(A)		
W(B)		

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Here, we can swap R(C) and W(B) since they are non-conflicting pair (since they are operating on different data items)

After swapping the schedule will become  $T2 \rightarrow T3 \rightarrow T1$

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T1	T2	T3
	R(A)	
	W(A)	
	W(B)	
		R(C)
		W(A)
		W(C)
R(A)		
R(B)		
W(A)		
W(B)		

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**S2**

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T1	T2	T3
		R(C)
		R(A)
		W(A)
		W(B)
R(A)		W(A)
R(B)		
W(A)		
W(B)		
		W(C)

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Here, we can swap and write R(C) after performing T2 operations:- R(A), W(A) and W(B) since each of them form non-conflicting pair with R(C) (since they are operating on different data items)

Also, we can swap W(C) and can execute it before all the T1 operations as each of the t1 operations are forming non-conflicting pair with W(C) (since they are operating on different data items)

After swapping the schedule will become  $T2 \rightarrow T3 \rightarrow T1$

$T1$	$T2$	$T3$
	$R(A)$	
	$W(A)$	
	$W(B)$	
		$R(C)$
		$W(A)$
		$W(C)$
$R(A)$		
$R(B)$		
$W(A)$		
$W(B)$		

**S3**

$T1$	$T2$	$T3$
	$R(A)$	
		$R(C)$
		$W(A)$
	$W(A)$	
	$W(B)$	
		$W(C)$
$R(A)$		
$R(B)$		
$W(A)$		
$W(B)$		

Here, we can't swap the operations and make it as  $T2 \rightarrow T3 \rightarrow T1$  because of the conflicting pairs  $W(A)$ and  $W(A)$

$\therefore$  Option D. ***S1 is conflict equivalent to S2, but not to S3*** is the correct answer.

17 votes

-- Satbir Singh (21k points)

## Answer Keys

3.1.1	N/A	3.1.2	N/A	3.1.3	N/A	3.1.4	N/A	3.1.5	B
3.1.6	N/A	3.1.7	B	3.1.8	N/A	3.1.9	N/A	3.1.10	N/A
3.1.11	C	3.1.12	B	3.1.13	C	3.1.14	D	3.1.15	A
3.1.16	C	3.1.17	C	3.1.18	B	3.1.19	5	3.1.20	50
3.1.21	A	3.1.22	52	3.1.23	B	3.1.24	C	3.1.25	A
3.1.26	C	3.1.27	A	3.1.28	A	3.2.1	N/A	3.2.2	A
3.2.3	8	3.2.4	19	3.2.5	B	3.3.1	54	3.3.2	B
3.3.3	B	3.4.1	False	3.5.1	True	3.5.2	N/A	3.5.3	N/A
3.5.4	N/A	3.5.5	N/A	3.5.6	N/A	3.5.7	B;D	3.5.8	False
3.5.9	N/A	3.5.10	A	3.5.11	D	3.5.12	N/A	3.5.13	B
3.5.14	D	3.5.15	B	3.5.16	C	3.5.17	A	3.5.18	N/A
3.5.19	C	3.5.20	C	3.5.21	D	3.5.22	B	3.5.23	C

3.5.24	D	3.5.25	C	3.5.26	D	3.5.27	C	3.5.28	A
3.5.29	C	3.5.30	B	3.5.31	A	3.5.32	B	3.5.33	A
3.5.34	C	3.5.35	B	3.5.36	B	3.5.37	A	3.5.38	B
3.5.39	C	3.5.40	A	3.5.41	A	3.5.42	A;C;D	3.5.43	B
3.5.44	A	3.5.45	B	3.5.46	B	3.5.47	A	3.5.48	D
3.5.49	A	3.6.1	B	3.6.2	B	3.6.3	A	3.6.4	C
3.6.5	4	3.6.6	C	3.6.7	A	3.6.8	A	3.6.9	B
3.6.10	C	3.7.1	N/A	3.7.2	N/A	3.7.3	3	3.7.4	C
3.7.5	A	3.7.6	C	3.7.7	C	3.7.8	C	3.7.9	C
3.7.10	4	3.7.11	698 : 698	3.8.1	A	3.8.2	A	3.8.3	A
3.8.4	C	3.8.5	B	3.8.6	A	3.8.7	A	3.9.1	C
3.10.1	C	3.10.2	A	3.10.3	C	3.11.1	B	3.11.2	C
3.11.3	0.00	3.11.4	D	3.12.1	N/A	3.12.2	N/A	3.12.3	N/A
3.12.4	N/A	3.12.5	N/A	3.12.6	N/A	3.12.7	D	3.12.8	N/A
3.12.9	B	3.12.10	C	3.12.11	D	3.12.12	C	3.12.13	N/A
3.12.14	A	3.12.15	D	3.12.16	B	3.12.17	D	3.12.18	A
3.12.19	A	3.12.20	D	3.12.21	D	3.12.22	4	3.12.23	C
3.12.24	1	3.12.25	C	3.12.26	B	3.13.1	N/A	3.13.2	N/A
3.13.3	D	3.13.4	C	3.13.5	C	3.13.6	C	3.13.7	B
3.13.8	C	3.13.9	C	3.13.10	A	3.13.11	A	3.13.12	D
3.13.13	D	3.13.14	C	3.14.1	D	3.15.1	N/A	3.15.2	N/A
3.15.3	N/A	3.15.4	N/A	3.15.5	N/A	3.15.6	N/A	3.15.7	N/A
3.15.8	D	3.15.9	N/A	3.15.10	N/A	3.15.11	A	3.15.12	C
3.15.13	N/A	3.15.14	C	3.15.15	N/A	3.15.16	N/A	3.15.17	N/A
3.15.18	C	3.15.19	D	3.15.20	D	3.15.21	C	3.15.22	B
3.15.23	C	3.15.24	A	3.15.25	X	3.15.26	C	3.15.27	A
3.15.28	C	3.15.29	C	3.15.30	B	3.15.31	D	3.15.32	B
3.15.33	C	3.15.34	D	3.15.35	2	3.15.36	A	3.15.37	2
3.15.38	2.6	3.15.39	7	3.15.40	D	3.15.41	5	3.15.42	A
3.15.43	819 : 820 ; 205 : 205	3.15.44	B	3.15.45	D	3.15.46	C	3.15.47	C
3.15.48	D	3.15.49	A	3.15.50	B	3.15.51	D	3.16.1	A
3.17.1	D	3.17.2	D	3.17.3	D	3.17.4	B	3.17.5	C
3.17.6	B	3.17.7	B	3.17.8	A	3.17.9	B	3.17.10	D
3.17.11	C	3.17.12	A	3.17.13	B	3.17.14	A	3.17.15	B
3.17.16	D	3.17.17	A	3.17.18	A	3.17.19	C	3.17.20	C
3.17.21	A	3.17.22	A	3.17.23	C	3.17.24	X	3.17.25	D

3.17.26

D

3.17.27

C

3.17.28

D



Boolean algebra. Combinational and sequential circuits. Minimization. Number representations and computer arithmetic (fixed and floating point)

#### Mark Distribution in Previous GATE

Year	2021-1	2021-2	2020	2019	2018	2017-1	2017-2	2016-1	2016-2	Minimum	Average	Maximum
1 Mark Count	2	3	2	4	2	3	2	3	3	2	2.6	4
2 Marks Count	2	2	1	2	2	0	4	2	0	0	1.6	4
Total Marks	6	7	4	8	6	3	10	7	3	3	6	10

## 4.1

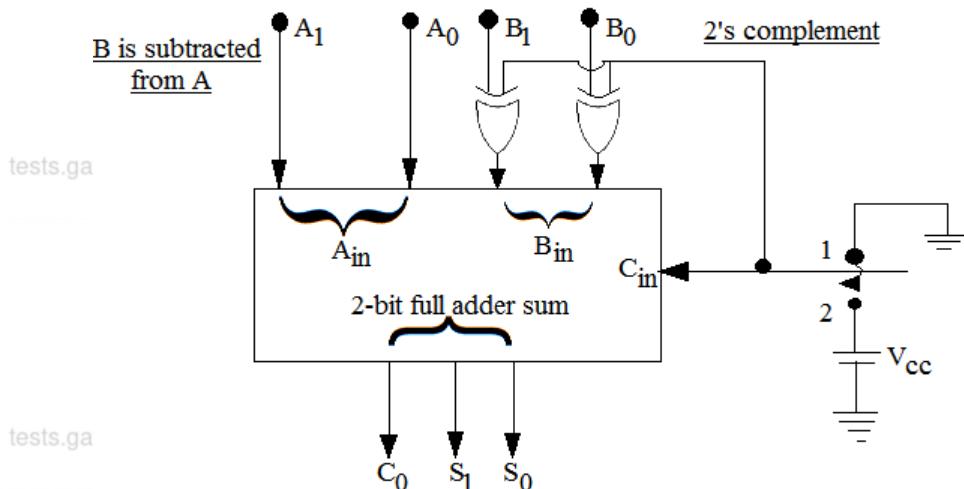
Adder (10) [top](#)4.1.1 Adder: GATE CSE 1988 | Question: 4ii [top](#)
<https://gateoverflow.in/94360>


Using binary full adders and other logic gates (if necessary), design an adder for adding 4-bit number (including sign) in 2's complement notation.

[gate1988](#) [digital-logic](#) [descriptive](#) [adder](#)
[aoclasses.in](#)
[tests.gatecse.in](#)
[Answer](#)
4.1.2 Adder: GATE CSE 1990 | Question: 1-i [top](#)
<https://gateoverflow.in/83829>

[tests.gatecse.in](#)
[goclasses.in](#)
[tests.gatecse.in](#)

In the two bit full-adder/subtractor unit shown in below figure, when the switch is in position 2 \_\_\_\_\_ using \_\_\_\_\_ arithmetic.


[gate1990](#) [digital-logic](#) [adder](#) [fill-in-the-blanks](#)
[Answer](#)
4.1.3 Adder: GATE CSE 1993 | Question: 9 [top](#)
<https://gateoverflow.in/2306>


Assume that only half adders are available in your laboratory. Show that any binary function can be implemented using half adders only.

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[goclasses.in](#)
[tests.gatecse.in](#)
[gate1993](#) [digital-logic](#) [combinational-circuits](#) [adder](#) [descriptive](#)
[Answer](#)
4.1.4 Adder: GATE CSE 1997 | Question: 2.5 [top](#)
<https://gateoverflow.in/2231>


An N-bit carry lookahead adder, where  $N$  is a multiple of 4, employs ICs 74181 (4 bit ALU) and 74182 (4 bit carry lookahead generator).

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[goclasses.in](#)
[tests.gatecse.in](#)

The minimum addition time using the best architecture for this adder is

- A. proportional to  $N$
- B. proportional to  $\log N$
- C. a constant
- D. None of the above

gate1997 digital-logic normal adder

Answer ↗

4.1.5 Adder: GATE CSE 1999 | Question: 2.16 top ↺

tests.gatecse.in <https://gateoverflow.in/1494>



The number of full and half-adders required to add 16-bit numbers is

- A. 8 half-adders, 8 full-adders
- B. 1 half-adder, 15 full-adders
- C. 16 half-adders, 0 full-adders
- D. 4 half-adders, 12 full-adders

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gate1999 digital-logic normal adder

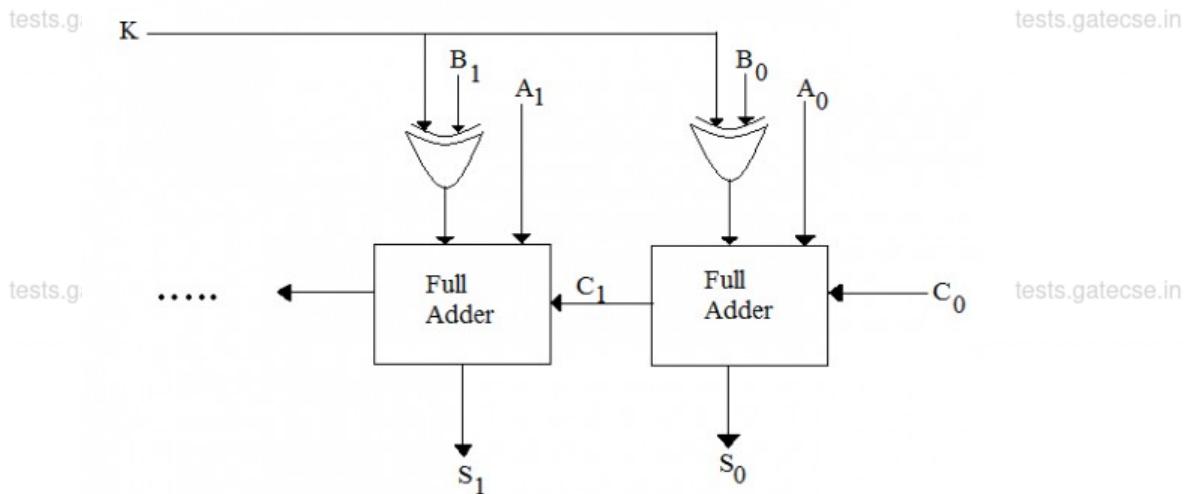
Answer ↗

4.1.6 Adder: GATE CSE 2003 | Question: 46 top ↺

tests.gatecse.in <https://gateoverflow.in/937>



Consider the ALU shown below.



If the operands are in 2's complement representation, which of the following operations can be performed by suitably setting the control lines  $K$  and  $C_0$  only (+ and - denote addition and subtraction respectively)?

- A.  $A + B$ , and  $A - B$ , but not  $A + 1$
- B.  $A + B$ , and  $A + 1$ , but not  $A - B$
- C.  $A + B$ , but not  $A - B$  or  $A + 1$
- D.  $A + B$ , and  $A - B$ , and  $A + 1$

gate2003-cse digital-logic normal adder

Answer ↗

4.1.7 Adder: GATE CSE 2004 | Question: 62 top ↺

tests.gatecse.in <https://gateoverflow.in/1057>



A 4-bit carry look ahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate is one time

unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.

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- A. 4 time units
- B. 6 time units
- C. 10 time units
- D. 12 time units

gate2004-cse digital-logic normal adder

Answer ↗

#### 4.1.8 Adder: GATE CSE 2015 Set 2 | Question: 48 top ↗

↗ <https://gateoverflow.in/8250>



A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit-ripple-carry binary adder is implemented by using four full adders. The total propagation time of this 4-bit binary adder in microseconds is \_\_\_\_\_.

gate2015-cse-set2 digital-logic adder normal numerical-answers

Answer ↗

#### 4.1.9 Adder: GATE CSE 2016 Set 1 | Question: 33 top ↗

↗ <https://gateoverflow.in/39688>



Consider a carry look ahead adder for adding two n-bit integers, built using gates of fan-in at most two. The time to perform addition using this adder is

- A.  $\Theta(1)$
- B.  $\Theta(\log(n))$
- C.  $\Theta(\sqrt{n})$
- D.  $\Theta(n)$

gate2016-cse-set1 digital-logic adder normal

Answer ↗

#### 4.1.10 Adder: GATE CSE 2016 Set 2 | Question: 07 top ↗

↗ <https://gateoverflow.in/39575>



Consider an eight-bit ripple-carry adder for computing the sum of  $A$  and  $B$ , where  $A$  and  $B$  are integers represented in 2's complement form. If the decimal value of  $A$  is one, the decimal value of  $B$  that leads to the longest latency for the sum to stabilize is \_\_\_\_\_

tests.gatecse.in gate2016-cse-set2 digital-logic adder normal numerical-answers

goclasses.in

tests.gatecse.in

Answer ↗

#### Answers: Adder

#### 4.1.1 Adder: GATE CSE 1988 | Question: 4ii top ↗

↗ <https://gateoverflow.in/94360>



✓ Overflow condition in  
2's complement number system:-

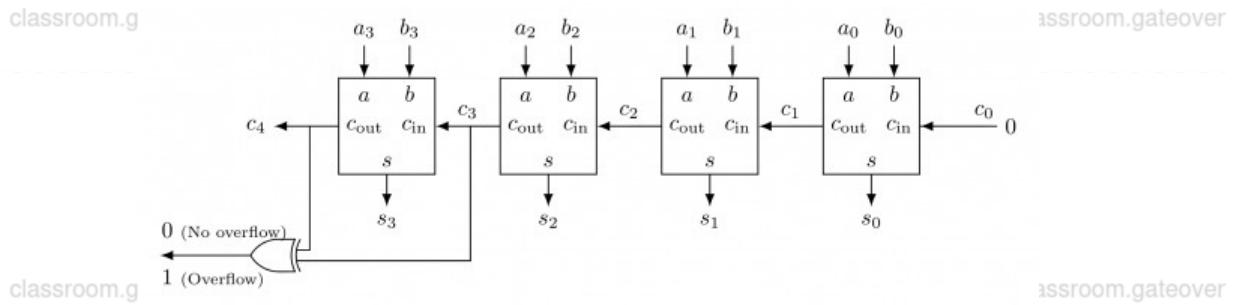
1.  $c_3 = 1, c_4 = 1 \implies$  No overflow
2.  $c_3 = 0, c_4 = 0 \implies$  No overflow
3.  $c_3 = 1, c_4 = 0 \implies$  Overflow ( $a_3 = b_3 = 0$ )
4.  $c_3 = 0, c_4 = 1 \implies$  Overflow ( $a_3 = b_3 = 1$ )

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We can conclude that the overflow condition for 2's complement number system is:

$$c_3 \oplus c_4 = 1 (\text{OR}) \bar{a}_3 \cdot \bar{b}_3 \cdot s_3 + a_3 \cdot b_3 \cdot \bar{s}_3 = 1$$



Here, we used  $4 - bit$  binary full adder and Ex-OR gate.

The Ex-OR gate is used to check the overflow condition.

10 votes

-- Lakshman Patel (65.7k points)

#### 4.1.2 Adder: GATE CSE 1990 | Question: 1-i top

<https://gateoverflow.in/83829>



- ✓ When the switch is at position 2, it is connected to  $V_{cc}$  thus, the value of control input  $M = 1$  which is fed to XOR gates as well. So

- $B_1 \oplus 1 = \overline{B_1}$  and
- $B_0 \oplus 1 = \overline{B_0}$

And the basic hardware is of adder only.

Now  $C_{in}$  is connected to  $V_{cc}$  as well. Hence,  $C_{in} = 1$ .

Net operation can be denoted as :  $S_0 = A_0 + \overline{B_0} + 1$  and similarly for  $S_1$  as well.

This is nothing but an expression of subtraction using  $2's$  complement. (Had it been  $A_0 + \overline{B_0}$ , it would have been addition of  $1's$  complement merely, but for subtraction we need to have  $2's$  complement of other operand which is  $B$  here)

**Hence, the correct answer should be : subtraction, 2's complement**

34 votes

-- HABIB MOHAMMAD KHAN (67.5k points)

#### 4.1.3 Adder: GATE CSE 1993 | Question: 9 top

<https://gateoverflow.in/2309>



- ✓ Half Adder gives two outputs:

- $S = A \oplus B$
- $C = A \cdot B$

We can perform any operation using Half adder if we can implement basic gates using half adder.

- AND operation  $C = A \cdot B$
- Not operation  $= S$  (with  $A$  and 1)  $= A \oplus 1 = A' \cdot 1 + A \cdot 1' = A'$
- OR operation  $= ((A \oplus 1) \cdot (B \oplus 1)) \oplus 1 = (A' \cdot B')' = A + B$

26 votes

-- Praveen Saini (41.9k points)

#### 4.1.4 Adder: GATE CSE 1997 | Question: 2.5 top

<https://gateoverflow.in/2231>



- ✓ For  $N = 64$  bits.

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Suppose you want to build a  $64$  bit adder then you need  $16$   $4$ -bit ALU and  $16$   $4$ -bit carry generator, at this point there will be  $16$  carries that will ripple through these  $16$  ALU modules, to speed up the adder we need to get rid of these  $16$  rippling carries, now we can again use  $4$   $4$ -bit carry generator to generate these  $16$  carries, now we have only  $4$  carries to ripple through, again we can use the same trick to minimize the rippling of these  $4$  carries, we can use an additional  $4$ -bit carry generator which will generate these carry and we are done :) there will be no more propagation of carry among the ALU modules.

So, we have used  $3$  level of  $4$ -bit carry generator, and the time taken to add  $64$  bits will be proportional to  $3$  which is  $\log_4 64$ .

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So, in general to add  $N$  – bits it takes  $\log_4 N$  time.

Correct Answer: [B](#)

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44 votes

-- Vikrant Singh (11.2k points)



#### 4.1.5 Adder: GATE CSE 1999 | Question: 2.16 [top](#)

<https://gateoverflow.in/1494>

- ✓ Answer is B.

For LSB addition we do not need a full adder.

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For addition of subsequent bits we need full adders since carry from previous addition has to be fed into the addition operation.

55 votes

-- Ankit Rokde (6.9k points)



#### 4.1.6 Adder: GATE CSE 2003 | Question: 46 [top](#)

<https://gateoverflow.in/937>

- ✓ Correct Option: A

There are two control line one is  $K$  and another is  $C_0$ .

- When  $K = 1$ ,  $C_0 = 1$  we can perform  $A - B$
- When  $K = 0$ ,  $C_0 = 0$  we can perform  $A + B$

But without manipulating  $B(B_0, B_1, \dots)$  we cannot perform  $A+1$ . But here we have only two control lines which is  $K, C_0$ .

Therefore the answer is A.

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Note:

**For A+B :**  $C_0 = 0$ ,  $K = 0$ , and  $0 \oplus x = x$

$$\begin{array}{r} & A_3 & A_2 & A_1 & A_0 \\ + & B_3 & B_2 & B_1 & B_0 \\ \hline & S_3 & S_2 & S_1 & S_0 \end{array}$$
$$\begin{array}{r} & C_3 & C_2 & C_1 & C_0=0 \\ & A_3 & A_2 & A_1 & A_0 \\ + & B_3 & B_2 & B_1 & B_0 \\ \hline & S_3 & S_2 & S_1 & S_0 \end{array}$$
$$\begin{array}{r} & C_4 & C_3 & C_2 & C_1 \\ \text{Sum Output:} & S_3 & S_2 & S_1 & S_0 \\ \text{Carry Output:} & C_4 & C_3 & C_2 & C_1 \end{array}$$

**For A-B :**  $C_0 = 1$ ,  $K = 1$ , and  $1 \oplus x = \bar{x}$

given that numbers are in 2's complement representations, So  $A - B = A + 2^k$ 's complement of  $B$

How to get 2's complement of  $B$  ?

2's complement of  $B = 1$ 's complement of  $B + 1$

So, by keeping  $K=1$ , we get 1's complement of  $B$  and By keeping  $C_0 = 1$ , we are adding 1 to 1's complement of  $B$ .

41 votes

-- Riya Roy(Arayana) (5.3k points)



#### 4.1.7 Adder: GATE CSE 2004 | Question: 62 [top](#)

<https://gateoverflow.in/1057>

- ✓ It would take 6 time units.

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We know that:

$$G_i = A_i B_i,$$

$$P_i = A_i \oplus B_i \text{ and}$$

$$S_i = P_i \oplus C_i$$

Also

$$C_1 = G_0 + P_0 C_0$$

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$$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0$$

$$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0$$

$$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$$

XOR can be implemented in 2 levels; level-1 ANDs and Level-2 OR. Hence it would take 2 time units to calculate  $P_i$  and  $S_i$

The 4-bit addition will be calculated in 3 stages

1. **(2 time units)** In 2 time units we can compute  $G_i$  and  $P_i$  in parallel. 2 time units for  $P_i$  since its an XOR operation and 1 time unit for  $G_i$  since its an AND operation.

2. **(2 time units)** Once  $G_i$  and  $P_i$  are available, we can calculate the carries,  $C_i$ , in 2 time units.

Level-1 we compute all the conjunctions (AND). Example  $P_3G_2$ ,  $P_3P_2G_1$ ,  $P_3P_2P_1G_0$  and  $P_3P_2P_1P_0C_0$  which are required for  $C_4$ .

Level-2 we get the carries by computing the disjunction (OR).

3. **(2 time units)** Finally we compute the Sum in 2 time units, as its an XOR operation.

Hence, the total is  $2 + 2 + 2 = \text{6 time units}$ .

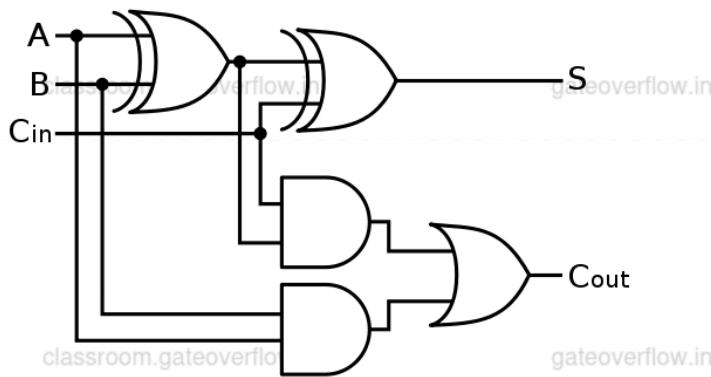
133 votes

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-- ryan sequeira (3k points)

#### 4.1.8 Adder: GATE CSE 2015 Set 2 | Question: 48 top

<https://gateoverflow.in/8250>



$S_1$  should wait for  $C_1$  to be ready. Delay for generating  $C$  is  $1 \text{ EXOR} + 1 \text{ AND} + 1 \text{ OR} = 2.4 + 1.2 + 1.2 = 4.8 \mu\text{s}$

Delay for sum is  $\text{XOR} + \text{XOR} = 2.4 + 2.4 = 4.8 \mu\text{s}$

But for the second adder, there the first EXOR can be done even before waiting for the previous output. So, we can get the sum in Another  $2.4 \mu\text{s}$  and carry in another  $2.4 \mu\text{s}$ . In this way, 4-bit sum can be obtained after

$$4.8 \mu\text{s} + 3 * 2.4 \mu\text{s} = 12 \mu\text{s}.$$

But the question says we use ripple-carry adder. So, each adder must wait for the full output from the previous adder. This would make the total delay =  $4 * 4.8 = 19.2 \mu\text{s}$  and this is the key given by GATE, so obviously they meant this.

116 votes

-- Arjun Suresh (332k points)

#### 4.1.9 Adder: GATE CSE 2016 Set 1 | Question: 33 top

<https://gateoverflow.in/39688>



- ✓ Look ahead carry generator gives output in constant time if fan in = number of inputs.

Example, it will take  $O(1)$  to calculate  $c_4 = g_3 + p_3g_2 + p_3p_2g_1 + p_3p_2p_1g_0 + p_3p_2p_1p_0c_0$ , if OR gate with 5 inputs is present.

If we have 8 inputs, and OR gate with 2 inputs, to build an OR gate with 8 inputs, we will need 4 gates in level-1, 2 in level-2 and 1 in level-3. Hence, 3 gate delays, for each level.

Similarly an n-input gate constructed with 2-input gates, total delay will be  $O(\log n)$ .

Hence, **answer is option B.**

103 votes

-- ryan sequeira (3k points)



- ✓ Answer is -1.

In case of -1 we get bit sequence 11111111 adding this we get a carry upto carry flag, so largest time to ripple!

57 votes

-- viv696 (1.7k points)

## 4.2

Array Multiplier (2) [top](#)

The maximum gate delay for any output to appear in an array multiplier for multiplying two  $n$  bit numbers is

- A.  $O(n^2)$  [ests.gatecse.in](#)
- B.  $O(n)$  [goclasses.in](#)
- C.  $O(\log n)$  [tests.gatecse.in](#)
- D.  $O(1)$  [tests.gatecse.in](#)

[gate1999](#) [digital-logic](#) [normal](#) [array-multiplier](#)

Answer



Consider an array multiplier for multiplying two  $n$  bit numbers. If each gate in the circuit has a unit delay, the total delay of the multiplier is

- A.  $\Theta(1)$  [tests.gatecse.in](#)
- B.  $\Theta(\log n)$  [goclasses.in](#)
- C.  $\Theta(n)$  [tests.gatecse.in](#)
- D.  $\Theta(n^2)$  [tests.gatecse.in](#)

[gate2003-cse](#) [digital-logic](#) [normal](#) [array-multiplier](#)

Answer

## Answers: Array Multiplier



- ✓ In an  $N \times M$  array multiplier we have  $N \times M$  AND gates and  $(M - 1), N - \text{bit}$  adders are used.

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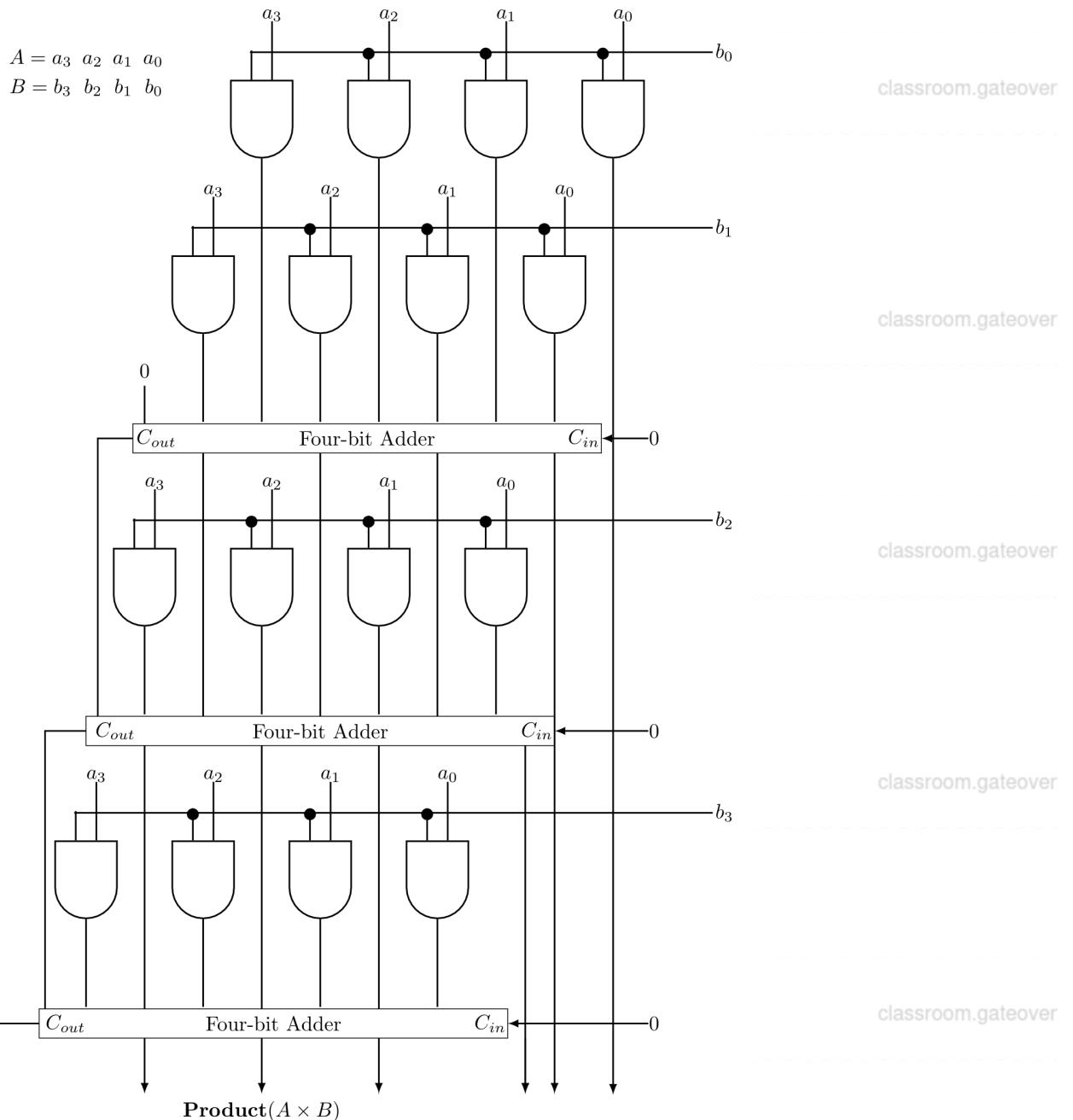
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Total delay in  $N \times M$  ( $N \geq M$ ) array multiplier due to AND gate in partial products at all level is just 1 unit AND gate delay as the operation is done parallel wise at each step. Now delays at level 1 to  $(M - 1) = (M - 1) \times$  delay due to 1 unit of  $N - bit$  adder. Therefore the maximum gate delay is  $O(M)$  but here  $M = N \therefore O(N)$ .

[gateoverflow.in](http://www.gateoverflow.in)  
[http://www.dauniv.ac.in/downloads/CArch\\_PPTs/CompArchCh03L06ArrayMult.pdf](http://www.dauniv.ac.in/downloads/CArch_PPTs/CompArchCh03L06ArrayMult.pdf) or [archive](#)

Refer this article page 16.

Correct Answer: **B**

References



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23 votes

-- Riya Roy(Arayana) (5.3k points)



<input checked="" type="checkbox"/> classroom.gateoverflow.in $  \begin{array}{r}  & & A_3 & A_2 & A_1 & A_0 \\  \times & B_3 & B_2 & B_1 & B_0 \\  \hline  C & B_0 \times A_3 & B_0 \times A_2 & B_0 \times A_1 & B_0 \times A_0  \end{array}  $ $  \begin{array}{r}  + \\  B_1 \times A_3 & B_1 \times A_2 & B_1 \times A_1 & B_1 \times A_0 \\  \hline  C & \text{Sum} & \text{Sum} & \text{Sum} & \text{Sum}  \end{array}  $ $  \begin{array}{r}  + \\  B_2 \times A_3 & B_2 \times A_2 & B_2 \times A_1 & B_2 \times A_0 \\  \hline  C & \text{Sum} & \text{Sum} & \text{Sum} & \text{Sum}  \end{array}  $ $  \begin{array}{r}  + \\  B_3 \times A_3 & B_3 \times A_2 & B_3 \times A_1 & B_3 \times A_0 \\  \hline  C & \text{Sum} & \text{Sum} & \text{Sum} & \text{Sum}  \end{array}  $	$  \begin{array}{r}  & & A_3 & A_2 & A_1 & A_0 \\  \times & B_3 & B_2 & B_1 & B_0 \\  \hline  C & B_0 \times A_3 & B_0 \times A_2 & B_0 \times A_1 & B_0 \times A_0  \end{array}  $ $  \begin{array}{r}  + \\  B_1 \times A_3 & B_1 \times A_2 & B_1 \times A_1 & B_1 \times A_0 \\  \hline  C & \text{Sum} & \text{Sum} & \text{Sum} & \text{Sum}  \end{array}  $ $  \begin{array}{r}  + \\  B_2 \times A_3 & B_2 \times A_2 & B_2 \times A_1 & B_2 \times A_0 \\  \hline  C & \text{Sum} & \text{Sum} & \text{Sum} & \text{Sum}  \end{array}  $ $  \begin{array}{r}  + \\  B_3 \times A_3 & B_3 \times A_2 & B_3 \times A_1 & B_3 \times A_0 \\  \hline  C & \text{Sum} & \text{Sum} & \text{Sum} & \text{Sum}  \end{array}  $	<b>Inputs</b> <b>Internal Signals</b> <b>Outputs</b>
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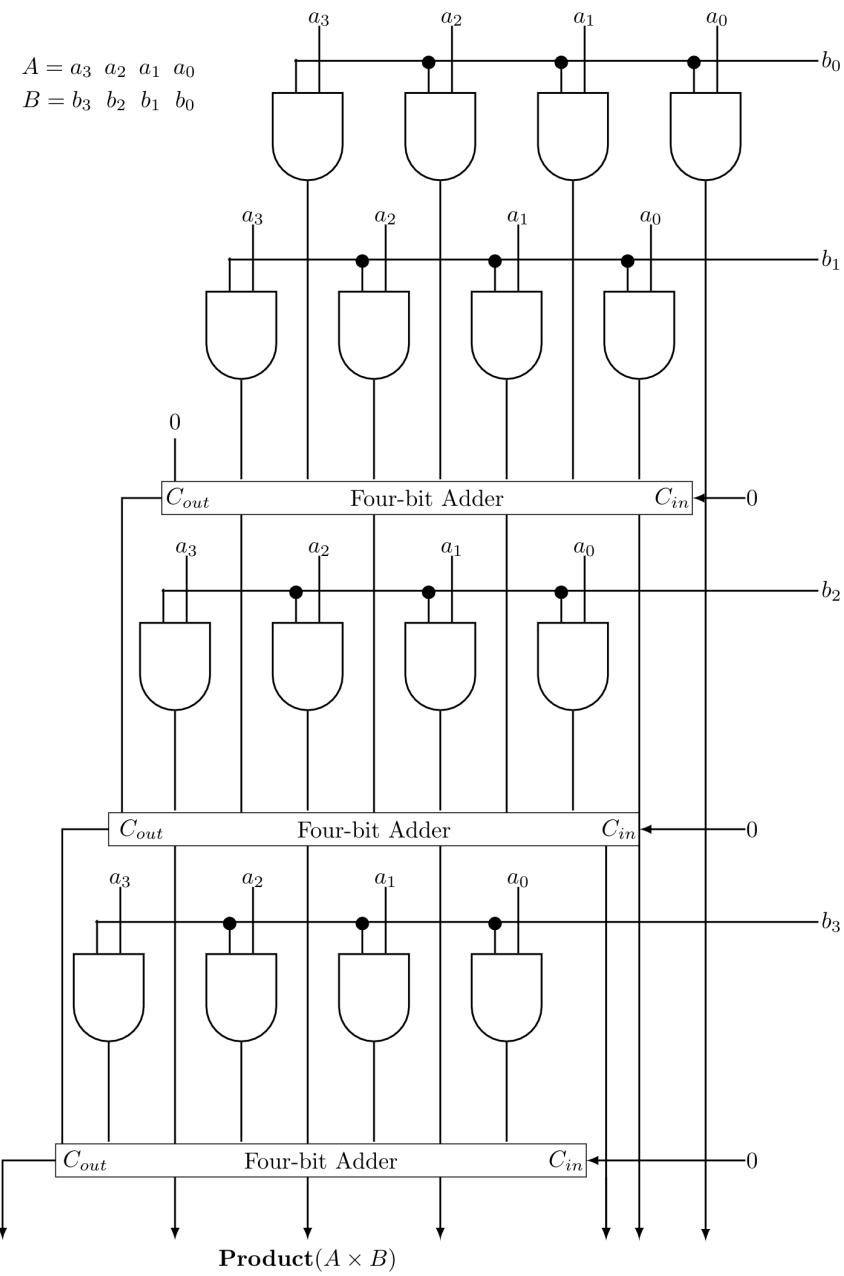
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Now to MULTIPLY these two Numbers:

1. 4 AND GATEs REQUIRED  $B_0$  MULTIPLY WITH  $A_3 \ A_2 \ A_1 \ A_0$ .
2. 4 AND GATEs REQUIRED  $B_1$  MULTIPLY WITH  $A_3 \ A_2 \ A_1 \ A_0$ .
3. 4 BIT ADDER
4. 4 AND GATEs REQUIRED  $B_2$  MULTIPLY WITH  $A_3 \ A_2 \ A_1 \ A_0$ .
5. 4 BIT ADDER
6. 4 AND GATEs REQUIRED  $B_3$  MULTIPLY WITH  $A_3 \ A_2 \ A_1 \ A_0$ .
7. 4 BIT ADDER

For 4 bits, Total Delay=  $3 + 4 = 7$

For  $n$  bits, Total Delay=  $n - 1 + n = 2n - 1$

So, Total Delay =  $\Theta(n)$ .

Correct Answer: C

👍 52 votes

-- Vidhi Sethi (8.3k points)



Consider numbers represented in 4-bit Gray code. Let  $h_3 h_2 h_1 h_0$  be the Gray code representation of a number  $n$  and let  $g_3 g_2 g_1 g_0$  be the Gray code of  $(n + 1)(\text{modulo}16)$  value of the number. Which one of the following functions is correct?

- A.  $g_0(h_3 h_2 h_1 h_0) = \sum(1, 2, 3, 6, 10, 13, 14, 15)$
- B.  $g_1(h_3 h_2 h_1 h_0) = \sum(4, 9, 10, 11, 12, 13, 14, 15)$
- C.  $g_2(h_3 h_2 h_1 h_0) = \sum(2, 4, 5, 6, 7, 12, 13, 15)$
- D.  $g_3(h_3 h_2 h_1 h_0) = \sum(0, 1, 6, 7, 10, 11, 12, 13)$

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Answer



Consider the binary code that consists of only four valid codewords as given below:

00000, 01011, 10101, 11110

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Let the minimum Hamming distance of the code  $p$  and the maximum number of erroneous bits that can be corrected by the code be  $q$ . Then the values of  $p$  and  $q$  are

- A.  $p = 3$  and  $q = 1$
- B.  $p = 3$  and  $q = 2$
- C.  $p = 4$  and  $q = 1$
- D.  $p = 4$  and  $q = 2$

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[gate2017-cse-set2](#) [digital-logic](#) [binary-codes](#)

Answer

## Answers: Binary Codes



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Decimal n	Binary n	H(x) = Gray(n)	G(x) = Gray[(n + 1) mod 16]
0	0000	0000(00)	0001
1	0001	0001(01)	0011
2	0010	0011(03)	0010
3	0011	0010(02)	0110
4	0100	0110(06)	0111
5	0101	0111(07)	0101
6	0110	0101(05)	0100
7	0111	0100(04)	1100
8	1000	1100(12)	1101
9	1001	1101(13)	1111
10	1010	1111(15)	1110
11	1011	1110(14)	1010
12	1100	1010(10)	1011
13	1101	1011(11)	1001
14	1110	1001(09)	1000
15	1111	1000(08)	0000

We need to map min terms of  $g_3 g_2 g_1 g_0$  with respect to  $h_3 h_2 h_1 h_0$ .

Hence as highlighted  $g_2$  matches with option C.

**Edit :**

We have to map  $h(x)$  with  $g(x)$ . Mod 16 is used in  $g(x)$  only because since we have 4 bits, the maximum possible no that can be represented is 15, so after 15 we shouldn't get 16 and go back to 0. that's why.

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Now, mapping is simple. We just have to map such that  $h(x) \rightarrow g(x + 1)$

This means if  $h$  represents gray code of 0 then  $g$  will represent the gray code of 1

If  $h$  represents the gray code of 1 then  $g$  will represent 2 and so on.

For the last number  $h(15) \bmod 16$  actually comes into the picture which will make it represent as  $g(0)$

So, drawing the table as mentioned above.

Now, write  $g$  as a function of  $f$ . Simply how we do minimization. See the minterms.

Be careful only in one thing here.

An example for 2 gray code representations is 0011 meaning 3 in decimal. So, if we select this row as a minterm(just an example) then we have selected 3 and not 2, means row numbers are not representing minterms. Rest everything is fine!

1 66 votes

-- ryan sequeira (3k points)

#### 4.3.2 Binary Codes: GATE CSE 2017 Set 2 | Question: 34 [top](#)



- ✓ 00000(**code1**), 01011(**code2**), 10101(**code3**), 11110 (**code4**)

Haming distance = min of all hamming distances.

Which is 3 b/w (**code1**) and (**code2**) so,

$p = 3$

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Now to correct d bit error we need hamming distance =  $2d + 1$

So,  $2d + 1 = 3$  will gives  $d = 1$ .

**A is answer.**

1 41 votes

-- Prashant Singh (47.2k points)

#### 4.4

#### Boolean Algebra (31) [top](#)



#### 4.4.1 Boolean Algebra: GATE CSE 1987 | Question: 1-II [top](#)

<https://gateoverflow.in/80032>

The total number of Boolean functions which can be realised with four variables is:

- A. 4
- B. 17
- C. 256
- D. 65,536

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boolean-algebra

functions

combinatory

Answer

#### 4.4.2 Boolean Algebra: GATE CSE 1987 | Question: 12-a [top](#)

<https://gateoverflow.in/82556>



The Boolean expression  $A \oplus B \oplus A$  is equivalent to

- A.  $AB + \bar{A} \bar{B}$
- B.  $\bar{A} B + A \bar{B}$
- C.  $B$
- D.  $\bar{A}$

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easy

Answer

#### 4.4.3 Boolean Algebra: GATE CSE 1988 | Question: 2-iii [top](#)

<https://gateoverflow.in/91679>



Let  $*$  be defined as a Boolean operation given as  $x * y = \bar{x} \bar{y} + xy$  and let  $C = A * B$ . If  $C = 1$  then prove that  $A = B$ .

gate1988

digital-logic

descriptive

boolean-algebra

Answer

#### 4.4.4 Boolean Algebra: GATE CSE 1989 | Question: 4-x [top](#)

<https://gateoverflow.in/88166>



A switching function is said to be neutral if the number of input combinations for which its value is 1 is equal to the number of

input combinations for which its value is 0. Compute the number of neutral switching functions of  $n$  variables (for a given  $n$ ).

gate1989 descriptive digital-logic boolean-algebra

Answer 

#### 4.4.5 Boolean Algebra: GATE CSE 1989 | Question: 5-a top ↺

► <https://gateoverflow.in/88230>



Find values of Boolean variables  $A, B, C$  which satisfy the following equations:

- $A + B = 1$
- $AC = BC$
- $A + C = 1$
- $AB = 0$

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Answer 

#### 4.4.6 Boolean Algebra: GATE CSE 1992 | Question: 02-i top ↺

► <https://gateoverflow.in/555>



The operation which is commutative but not associative is:

- A. AND
- B. OR
- C. EX-OR
- D. NAND

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gate1992 easy digital-logic boolean-algebra multiple-selects

Answer 

#### 4.4.7 Boolean Algebra: GATE CSE 1994 | Question: 4 top ↺

► <https://gateoverflow.in/2500>



- A. Let  $*$  be a Boolean operation defined as  $A * B = AB + \bar{A} \bar{B}$ . If  $C = A * B$  then evaluate and fill in the blanks:

i.  $A * A = \underline{\hspace{2cm}}$   
ii.  $C * A = \underline{\hspace{2cm}}$

- B. Solve the following boolean equations for the values of  $A, B$  and  $C$ :

$$\begin{aligned} AB + \bar{A}C &= 1 \\ AC + B &= 0 \end{aligned}$$

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gate1994 digital-logic normal boolean-algebra descriptive

Answer 

#### 4.4.8 Boolean Algebra: GATE CSE 1995 | Question: 2.5 top ↺

► <https://gateoverflow.in/2617>



What values of  $A, B, C$  and  $D$  satisfy the following simultaneous Boolean equations?

$$\bar{A} + AB = 0, AB = AC, AB + \bar{A}\bar{C} + CD = \bar{C}D$$

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- A.  $A = 1, B = 0, C = 0, D = 1$
- B.  $A = 1, B = 1, C = 0, D = 0$
- C.  $A = 1, B = 0, C = 1, D = 1$
- D.  $A = 1, B = 0, C = 0, D = 0$

gate1995 digital-logic boolean-algebra easy

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Answer 

**4.4.9 Boolean Algebra: GATE CSE 1997 | Question: 2-1**<https://gateoverflow.in/2227>

Let  $*$  be defined as  $x * y = \bar{x} + y$ . Let  $z = x * y$ . Value of  $z * x$  is

- A.  $\bar{x} + y$
- B.  $x$
- C. 0
- D. 1

[gate1997](#) [digital-logic](#) [normal](#) [boolean-algebra](#)

[goclasses.in](#)[tests.gatecse.in](#)[Answer](#)**4.4.10 Boolean Algebra: GATE CSE 1998 | Question: 1.13**<https://gateoverflow.in/1650>

What happens when a bit-string is XORed with itself  $n$ -times as shown:

$$[B \oplus (B \oplus (B \oplus (B \dots n \text{ times})))]$$

- A. complements when  $n$  is even
- B. complements when  $n$  is odd
- C. divides by  $2^n$  always
- D. remains unchanged when  $n$  is even

[gate1998](#) [digital-logic](#) [normal](#) [boolean-algebra](#)

[goclasses.in](#)[tests.gatecse.in](#)[Answer](#)**4.4.11 Boolean Algebra: GATE CSE 1998 | Question: 2.8**<https://gateoverflow.in/1680>

Which of the following operations is commutative but not associative?

- A. AND
- B. OR
- C. NAND
- D. EXOR

[gate1998](#) [digital-logic](#) [easy](#) [boolean-algebra](#)

[goclasses.in](#)[tests.gatecse.in](#)[Answer](#)**4.4.12 Boolean Algebra: GATE CSE 1999 | Question: 1.7**<https://gateoverflow.in/1460>

Which of the following expressions is not equivalent to  $\bar{x}$ ?

- A.  $x \text{ NAND } x$
- B.  $x \text{ NOR } x$
- C.  $x \text{ NAND } 1$
- D.  $x \text{ NOR } 1$

[gate1999](#) [digital-logic](#) [easy](#) [boolean-algebra](#)

[goclasses.in](#)[tests.gatecse.in](#)[Answer](#)**4.4.13 Boolean Algebra: GATE CSE 2000 | Question: 2.10**<https://gateoverflow.in/657>

The simultaneous equations on the Boolean variables  $x, y, z$  and  $w$ ,

- $x + y + z = 1$
- $xy = 0$
- $xz + w = 1$
- $xy + \bar{z}\bar{w} = 0$

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have the following solution for  $x, y, z$  and  $w$ , respectively:

- A. 0 1 0 0

- B. 1 1 0 1  
 C. 1 0 1 1  
 D. 1 0 0 0

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gate2000-cse digital-logic boolean-algebra easy

Answer 

**4.4.14 Boolean Algebra: GATE CSE 2002 | Question: 2-3** top ↗

<https://gateoverflow.in/833>



Let  $f(A, B) = A' + B$ . Simplified expression for function  $f(f(x + y, y), z)$  is

- A.  $x' + z$   
 B.  $xyz$   
 C.  $xy' + z$   
 D. None of the above

gate2002-cse digital-logic boolean-algebra normal

Answer 

**4.4.15 Boolean Algebra: GATE CSE 2004 | Question: 17** top ↗

<https://gateoverflow.in/1014>



A Boolean function  $x'y' + xy + x'y$  is equivalent to

- A.  $x' + y'$   
 B.  $x + y$   
 C.  $x + y'$   
 D.  $x' + y$

gate2004-cse digital-logic easy boolean-algebra

Answer 

**4.4.16 Boolean Algebra: GATE CSE 2007 | Question: 32** top ↗

<https://gateoverflow.in/1230>



Let  $f(w, x, y, z) = \sum(0, 4, 5, 7, 8, 9, 13, 15)$ . Which of the following expressions are NOT equivalent to  $f$ ?

- P:  $x'y'z' + w'xy' + wy'z + xz$   
 Q:  $w'y'z' + wx'y' + xz$   
 R:  $w'y'z' + wx'y' + xyz + xy'z$   
 S:  $x'y'z' + wx'y' + w'y$

- A. P only  
 B. Q and S  
 C. R and S  
 D. S only

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Answer 

**4.4.17 Boolean Algebra: GATE CSE 2007 | Question: 33** top ↗

<https://gateoverflow.in/1231>



Define the connective  $*$  for the Boolean variables  $X$  and  $Y$  as:

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$$X * Y = \overline{XY} + X'Y'.$$

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Let  $Z = X * Y$ . Consider the following expressions  $P, Q$  and  $R$ .

$$P : X = Y * Z, Q : Y = X * Z, R : X * Y * Z = 1$$

Which of the following is TRUE?

- A. Only  $P$  and  $Q$  are valid.

- B. Only  $Q$  and  $R$  are valid.  
 C. Only  $P$  and  $R$  are valid.  
 D. All  $P, Q, R$  are valid.

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Answer 

**4.4.18 Boolean Algebra: GATE CSE 2008 | Question: 26** top ↗

<https://gateoverflow.in/424>



If  $P, Q, R$  are Boolean variables, then

$(P + \bar{Q})(P \cdot \bar{Q} + P \cdot R)(\bar{P} \cdot \bar{R} + \bar{Q})$  simplifies to

- A.  $P \cdot \bar{Q}$   
 B.  $P \cdot \bar{R}$   
 C.  $P \cdot \bar{Q} + R$   
 D.  $P \cdot \bar{R} + Q$

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Answer 

**4.4.19 Boolean Algebra: GATE CSE 2012 | Question: 6** top ↗

<https://gateoverflow.in/38>



The truth table

X	Y	(X, Y)
0	0	0
0	1	0
1	0	1
1	1	1

represents the Boolean function

- A.  $X$   
 B.  $X + Y$   
 C.  $X \oplus Y$   
 D.  $Y$

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gate2012-cse digital-logic easy boolean-algebra

Answer 

**4.4.20 Boolean Algebra: GATE CSE 2013 | Question: 21** top ↗

<https://gateoverflow.in/1532>



Which one of the following expressions does NOT represent exclusive NOR of  $x$  and  $y$ ?

- A.  $xy + x'y'$   
 B.  $x \oplus y'$   
 C.  $x' \oplus y$   
 D.  $x' \oplus y'$

gate2013-cse digital-logic easy boolean-algebra

Answer 

**4.4.21 Boolean Algebra: GATE CSE 2014 Set 3 | Question: 55** top ↗

<https://gateoverflow.in/2090>



Let  $\oplus$  denote the exclusive OR (XOR) operation. Let '1' and '0' denote the binary constants. Consider the following Boolean expression for  $F$  over two variables  $P$  and  $Q$ :

$$F(P, Q) = ((1 \oplus P) \oplus (P \oplus Q)) \oplus ((P \oplus Q) \oplus (Q \oplus 0))$$

The equivalent expression for  $F$  is

- A.  $P + Q$

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- B.  $\overline{P+Q}$   
 C.  $P \oplus Q$   
 D.  $\overline{P \oplus Q}$

gate2014-cse-set3 digital-logic normal boolean-algebra

Answer 

4.4.22 Boolean Algebra: GATE CSE 2015 Set 1 | Question: 39 [top](#)

<https://gateoverflow.in/8294>



Consider the operations

$$f(X, Y, Z) = X'YZ + XY' + Y'Z' \text{ and } g(X, Y, Z) = X'YZ + X'YZ' + XY$$

Which one of the following is correct?

- A. Both  $\{f\}$  and  $\{g\}$  are functionally complete  
 B. Only  $\{f\}$  is functionally complete  
 C. Only  $\{g\}$  is functionally complete  
 D. Neither  $\{f\}$  nor  $\{g\}$  is functionally complete

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Answer 

4.4.23 Boolean Algebra: GATE CSE 2015 Set 2 | Question: 37 [top](#)

<https://gateoverflow.in/8162>



The number of min-terms after minimizing the following Boolean expression is \_\_\_\_\_.

$$[D'+AB'+A'C+AC'D+A'C'D]'$$

gate2015-cse-set2 digital-logic boolean-algebra normal numerical-answers

Answer 

4.4.24 Boolean Algebra: GATE CSE 2016 Set 1 | Question: 06 [top](#)

<https://gateoverflow.in/39629>



Consider the Boolean operator # with the following properties :

$x\#0=x$ ,  $x\#1=\bar{x}$ ,  $x\#x=0$  and  $x\#\bar{x}=1$ . Then  $x\#y$  is equivalent to

- A.  $x\bar{y} + \bar{x}y$   
 B.  $x\bar{y} + \bar{x}\bar{y}$   
 C.  $\bar{x}y + xy$   
 D.  $xy + \bar{x}\bar{y}$

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gate2016-cse-set1 digital-logic boolean-algebra easy

Answer 

4.4.25 Boolean Algebra: GATE CSE 2016 Set 2 | Question: 08 [top](#)

<https://gateoverflow.in/39540>



Let,  $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$  where  $x_1, x_2, x_3, x_4$  are Boolean variables, and  $\oplus$  is the XOR operator.

Which one of the following must always be TRUE?

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- A.  $x_1x_2x_3x_4 = 0$   
 B.  $x_1x_3 + x_2 = 0$   
 C.  $\bar{x}_1 \oplus \bar{x}_3 = \bar{x}_2 \oplus \bar{x}_4$   
 D.  $x_1 + x_2 + x_3 + x_4 = 0$

gate2016-cse-set2 digital-logic boolean-algebra normal

Answer 



If  $w, x, y, z$  are Boolean variables, then which one of the following is INCORRECT?

- A.  $wx + w(x + y) + x(x + y) = x + wy$
- B.  $w\bar{x}(y + \bar{z}) + \bar{w}x = \bar{w} + x + \bar{y}z$
- C.  $(w\bar{x}(y + x\bar{z}) + \bar{w}\bar{x})y = x\bar{y}$
- D.  $(w + y)(wx\bar{y} + w\bar{y}z) = wx\bar{y} + w\bar{y}z$

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[gate2017-cse-set2](#) [digital-logic](#) [boolean-algebra](#) [normal](#)

Answer



Let  $\oplus$  and  $\odot$  denote the Exclusive OR and Exclusive NOR operations, respectively. Which one of the following is NOT CORRECT?

- A.  $\overline{P \oplus Q} = P \odot Q$
- B.  $\overline{P} \oplus Q = P \odot Q$
- C.  $\overline{P} \oplus \overline{Q} = P \oplus Q$
- D.  $P \oplus \overline{P} \oplus Q = (P \odot \overline{P} \odot \overline{Q})$

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Answer



Which one of the following is NOT a valid identity?

- A.  $(x \oplus y) \oplus z = x \oplus (y \oplus z)$
- B.  $(x + y) \oplus z = x \oplus (y + z)$
- C.  $x \oplus y = x + y$ , if  $xy = 0$
- D.  $x \oplus y = (xy + x'y')'$

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Answer



Consider the following Boolean expression.

$$F = (X + Y + Z)(\bar{X} + Y)(\bar{Y} + Z)$$

Which of the following Boolean expressions is/are equivalent to  $\bar{F}$  (complement of  $F$ )?

- A.  $(\bar{X} + \bar{Y} + \bar{Z})(X + \bar{Y})(Y + \bar{Z})$
- B.  $X\bar{Y} + \bar{Z}$
- C.  $(X + \bar{Z})(\bar{Y} + \bar{Z})$
- D.  $X\bar{Y} + Y\bar{Z} + X\bar{Y}\bar{Z}$

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[gate2021-cse-set1](#) [multiple-selects](#) [digital-logic](#) [boolean-algebra](#)

Answer



The function  $A\bar{B}C + \bar{A}BC + ABC\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C}$  is equivalent to

- A.  $A\bar{C} + AB + \bar{A}C$
- B.  $A\bar{B} + A\bar{C} + \bar{A}C$

- C.  $\bar{A}B + A\bar{C} + A\bar{B}$   
D.  $\bar{A}B + AC + A\bar{B}$

gate2004-it digital-logic boolean-algebra easy

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Answer 

#### 4.4.31 Boolean Algebra: GATE IT 2005 | Question: 7

<https://gateoverflow.in/3752>



Which of the following expressions is equivalent to  $(A \oplus B) \oplus C$

- A.  $(A + B + C)(\bar{A} + \bar{B} + \bar{C})$   
B.  $(A + B + C)(\bar{A} + \bar{B} + C)$   
C.  $ABC + \bar{A}(B \oplus C) + \bar{B}(A \oplus C)$   
D. None of these

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gate2005-it digital-logic normal boolean-algebra

Answer 

#### Answers: Boolean Algebra

#### 4.4.1 Boolean Algebra: GATE CSE 1987 | Question: 1-II

<https://gateoverflow.in/80032>



- ✓ A Boolean function of 4 variables is a function from a set of  $2^4 = 16$  elements (all combinations of 4 variables) to a set of  $2(\{0, 1\})$  elements. So, number of such functions will be  $2^{16} = 65,536$

Correct Answer: D

References



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 26 votes

-- Prashant Singh (47.2k points)

#### 4.4.2 Boolean Algebra: GATE CSE 1987 | Question: 12-a

<https://gateoverflow.in/82556>



- ✓ Option (C) 

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$$A \oplus A = 0 \text{ and } 0 \oplus A = A$$

$$A \oplus B \oplus A = (A \oplus A) \oplus B = 0 \oplus B = B$$

 25 votes

-- Prajwal Bhat (7.6k points)

#### 4.4.3 Boolean Algebra: GATE CSE 1988 | Question: 2-iii

<https://gateoverflow.in/91679>



- ✓  $C = A * B$

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$$\Rightarrow C = \bar{A} \bar{B} + AB$$

$$\Rightarrow C = \bar{A} \text{ XOR } B$$

$$\Rightarrow C = A \text{ XNOR } B$$

Truth table is: [n.gateoverflow.in](https://n.gateoverflow.in)

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A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

When  $C = 1$ , observing the truth table we can say  $A = B$ .

16 votes

-- Arnab Bhadra (3.7k points)

#### 4.4.4 Boolean Algebra: GATE CSE 1989 | Question: 4-x top

<https://gateoverflow.in/88166>



For an 'n' variable function, total number of possible minterms(input combinations) will be  $2^n$ . Half of them will be one i.e,  $2^{n-1}$ .

Thus total number of neutral functions possible = Choosing any  $2^{n-1}$  combinations to be 1 out of  $2^n$  combination. i.e  $\binom{2^n}{2^{n-1}}$ .

17 votes

-- Jeeten (95 points)

#### 4.4.5 Boolean Algebra: GATE CSE 1989 | Question: 5-a top

<https://gateoverflow.in/88230>



- ✓ From  $A + B = 1$  and  $AB = 0$  we get either of  $A, B$  is 1 and another is 0

Now,  $AC = BC$ , here  $C$  has to be 0 (because  $A, B$  has different values)

$$C = 0$$

$$\text{Now, } A + C = 1$$

$$\text{So, } A = 1 \text{ and } AB = 0 \text{ so, } B = 0$$

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So, we get:

$$A = 1, B = 0, C = 0$$

These are the values.

21 votes

-- Aboveallplayer (12.5k points)

#### 4.4.6 Boolean Algebra: GATE CSE 1992 | Question: 02-i top

<https://gateoverflow.in/555>



- ✓ The answer is D.

Remark:

1. Every logic gate follows Commutative law.
2. AND, OR, Ex-OR, EX-NOR follows Associative law also. NAND, NOR doesn't follow Associative law.

31 votes

-- Ankit Rokde (6.9k points)

#### 4.4.7 Boolean Algebra: GATE CSE 1994 | Question: 4 top

<https://gateoverflow.in/2500>



✓

A.

- i.  $A * A = AA + A'A' = A + A' = 1$
- ii.  $C * A = (A * B) * A = (AB + A'B') * A = (AB + A'B')A + (AB + A'B')'A'$

$$(AB + A'B')A + (A'B + AB')A' = AB + 0 + A'B + 0 = B.$$

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$$\text{B. } AB + A'C = 1, AC + B = 0$$

$$\implies AC + B = 0, \text{ means both } B = 0 \text{ and } AC = 0$$

$$\implies AB + A'C = 1$$

$$\implies A'C = 1 \quad [ \because B = 0, AB = 0 ]$$

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So,  $C = 1$  and  $A = 0$

$A = 0, B = 0$  and  $C = 1$

1 27 votes

-- Praveen Saini (41.9k points)

#### 4.4.8 Boolean Algebra: GATE CSE 1995 | Question: 2.5 top



✓  $A' + AB = 0 \implies A' + B = 0$

$$\therefore A' = 0 \text{ and } B = 0$$

$$A = 1$$

$$AB = AC \implies B = C \implies C = 0$$

$$AB + AC' + CD = C'D$$

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$$\implies 0 + 1 + 0 = D$$

$$\implies D = 1$$

Correct Answer: A

1 16 votes

-- Sutanay Bhattacharjee (3.1k points)

#### 4.4.9 Boolean Algebra: GATE CSE 1997 | Question: 2-1 top



✓ Answer is option B.

$$z * x = (x * y) * x$$

$$= (\bar{x} + y) * x$$

$$= \bar{x} + \bar{y} + x$$

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$$x \cdot \bar{y} + x = x$$

1 29 votes

-- Arjun Suresh (332k points)

#### 4.4.10 Boolean Algebra: GATE CSE 1998 | Question: 1.13 top



✓ It should be (D).

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Let number of  $\oplus$  be two (even case):

$$B \oplus B \oplus B = B \oplus 0 = B \text{ (remains unchanged)}$$

Let number of  $\oplus$  be three (odd case):

$$B \oplus B \oplus B \oplus B = B \oplus B \oplus 0 = B \oplus B = 0 \text{ (gives 0)}$$

1 37 votes

-- Rajarshi Sarkar (27.9k points)

#### 4.4.11 Boolean Algebra: GATE CSE 1998 | Question: 2.8 top



✓ We all know AND ,OR are both associative and commutative.we dont know about EXOR and NAND

We can consume some time and prove it by truth table..and come up with the results that EXOR is also associative and commutative so the only left out is NAND its commutative but not associative

Correct Answer: C

17 votes

-- Bhagirathi Nayak (11.7k points)

**4.4.12 Boolean Algebra: GATE CSE 1999 | Question: 1.7**<https://gateoverflow.in/1460>

- A.  $\bar{x}\bar{x} = \bar{x}$
- B.  $\bar{x} + \bar{x} = \bar{x}$
- C.  $x \cdot 1 = \bar{x} + 0 = \bar{x}$
- D.  $x + 1 = \bar{x} \cdot 0 = 0$

Here,  $x$  NOR 1 will not be equal to  $\bar{x}$ .Hence, option (D)  $x$  NOR 1.

11 votes

-- Leen Sharma (28.7k points)

**4.4.13 Boolean Algebra: GATE CSE 2000 | Question: 2.10**<https://gateoverflow.in/657>

- ✓ Take each option one by one and try to put the values of  $x, y, z$  and  $w$  in question:  
1.

- $0 + 1 + 0 = 1$
- $0 \cdot 1 = 0$
- $0 \cdot 0 + 0 = 0$  (went wrong) So, this is not the right option

2.

- $1 + 1 + 0 = 1$
- $1 \cdot 1 = 1$  (went wrong) not right

3.

- $1 + 0 + 1 = 1$
- $1 \cdot 0 = 0$  (went wrong)
- $1 \cdot 1 + 1 = 1$
- $1 \cdot 0 + 1 \cdot 0 = 0$  This is the right option

Correct Answer: C

31 votes

-- shekhar chauhan (32.8k points)

**4.4.14 Boolean Algebra: GATE CSE 2002 | Question: 2-3**<https://gateoverflow.in/833>

$$\begin{aligned}
 & f(f(x+y, y), z) = f((x+y)' + y, z) \\
 &= ((x+y)' + y)' + z \\
 &= (x+y) \cdot y' + z (\because (a+b)' = a' \cdot b') \\
 &= xy' + z
 \end{aligned}$$

Correct Answer: C

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30 votes

-- Arjun Suresh (332k points)

**4.4.15 Boolean Algebra: GATE CSE 2004 | Question: 17**<https://gateoverflow.in/1014>

- ✓ Answer is option D.

$$\begin{aligned}
 x'y' + x'y &= x'(y + y') = x' \\
 x' + xy &= x' + y
 \end{aligned}$$

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26 votes

-- Arjun Suresh (332k points)

4.4.16 Boolean Algebra: GATE CSE 2007 | Question: 32 [top](#)

<https://gateoverflow.in/1230>



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	00	01	11	10
00	1	1		1
01		1	1	1
11		1	1	
10				

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K-map

So, minimized expression will be

$xz + w'y'z' + wx'y'$  which is Q. From the K-map, we can also get P and R. So, only S is NOT equivalent to f.

[http://www.eecs.berkeley.edu/~newton/Classes/CS150sp98/lectures/week4\\_2/sld011.htm](http://www.eecs.berkeley.edu/~newton/Classes/CS150sp98/lectures/week4_2/sld011.htm)

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Alternatively,

Go with Minterm representation of each option, (Note that order of W, X, Y, Z should be preserved.)

Here, x means do not care (x takes value either 0 or 1)

$$\begin{aligned}P &: X'Y'Z' + W'XY' + WY'Z + XZ \\&= xX'Y'Z' + W'XY'x + WxY'Z + xXxZ \\&= x000 + 010x + 1x01 + x1x1 \\&= 0000 + 1000 + 0100 + 0101 + 1001 + 1101 + 0101 + 0111 + 1101 + 1111 \\&= 0 + 8 + 4 + 5 + 9 + 13 + 5 + 7 + 13 + 15 \\&= \sum m(0, 4, 5, 7, 8, 9, 13, 15)\end{aligned}$$

$$\begin{aligned}Q &: W'Y'Z' + WX'Y' + XZ \\&= W'xY'Z' + WX'Y'x + xXxZ \\&= x000 + 100x + x1x1 \\&= 0000 + 0100 + 1000 + 1001 + 0101 + 0111 + 1101 + 1111 \\&= 0 + 4 + 8 + 9 + 5 + 7 + 13 + 15 \\&= \sum m(0, 4, 5, 7, 8, 9, 13, 15)\end{aligned}$$

$$\begin{aligned}R &: W'Y'Z' + WX'Y' + XYZ + XY'Z \\&= W'xY'Z' + WX'Y'x + xXYZ + xXY'Z \\&= x000 + 100x + x111 + x101 \\&= 0000 + 0100 + 1000 + 1001 + 0111 + 1111 + 0101 + 1101 \\&= 0 + 4 + 8 + 9 + 7 + 15 + 5 + 13 \\&= \sum m(0, 4, 5, 7, 8, 9, 13, 15)\end{aligned}$$

$$\begin{aligned}S &: X'Y'Z' + WX'Y' + W'Y \\&= xX'Y'Z' + WX'Y'x + W'xYx \\&= x000 + 100x + 0x1x \\&= 0000 + 1000 + 1000 + 1001 + 0010 + 0011 + 0110 + 0111 \\&= 0 + 8 + 8 + 9 + 2 + 3 + 6 + 7 \\&= \sum m(0, 2, 3, 6, 7, 8, 9)\end{aligned}$$

Correct Answer: D

References

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42 votes

-- Arjun Suresh (332k points)

4.4.17 Boolean Algebra: GATE CSE 2007 | Question: 33 top<https://gateoverflow.in/1231>

P:

$$\begin{aligned}
 Y * Z &= Y * (X * Y) \\
 &= Y * (XY + X'Y') \\
 &= Y(XY + X'Y') + Y'(XY + X'Y')' \\
 &= XY + Y'((X' + Y')(X + Y)) \\
 &= XY + Y'(X'Y + XY') \\
 &= XY + XY' \\
 &= X(Y + Y') \\
 &= X
 \end{aligned}$$

So, P is valid.

Q: classroom.gateoverflow.in

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$$\begin{aligned}
 X * Z &= X * (X * Y) \\
 &= X * (XY + X'Y') \\
 &= X(XY + X'Y') + X'(XY + X'Y')' \\
 &= XY + X'((X' + Y')(X + Y)) \\
 &= XY + X'(X'Y + XY') \\
 &= XY + X'Y \\
 &= Y(X + X') \\
 &= Y
 \end{aligned}$$

So, Q is also valid.

R:

$$\begin{aligned}
 X * Y * Z &= (X * Y) * (X * Y) \\
 &= (XY + X'Y') * (XY + X'Y') \\
 &= (XY + X'Y')(XY + X'Y') + (XY + X'Y')'(XY + X'Y')' \\
 &= (XY + X'Y') + (XY + X'Y')' (\because AA = A) \\
 &= 1 (\because A + A' = 1)
 \end{aligned}$$

So, R is also valid.

Hence, D choice.

42 votes

-- Arjun Suresh (332k points)

4.4.18 Boolean Algebra: GATE CSE 2008 | Question: 26 top<https://gateoverflow.in/424>Ans is (A)  $P\bar{Q}$ 

$$\begin{aligned}
 &(P + \bar{Q})(P\bar{Q} + PR)(\bar{P}\bar{R} + \bar{Q}) \\
 &= (PP\bar{Q} + PPR + P\bar{Q} + P\bar{Q}R)(\bar{P}\bar{R} + \bar{Q}) \\
 &= (P\bar{Q} + PR + P\bar{Q} + P\bar{Q}R)(\bar{P}\bar{R} + \bar{Q}) \\
 &= P\bar{Q} + P\bar{Q}R \\
 &= P\bar{Q}
 \end{aligned}$$

41 votes

-- Keith Kr (4.5k points)

4.4.19 Boolean Algebra: GATE CSE 2012 | Question: 6 [top](#)

<https://gateoverflow.in/38>



- ✓ Whenever  $X$  is true ( $X, Y$ ) is true and whenever  $X$  is false ( $X, Y$ ) is false, so the answer is (A)  $X$ .

39 votes

-- Omesh Pandita (1.9k points)

4.4.20 Boolean Algebra: GATE CSE 2013 | Question: 21 [top](#)

<https://gateoverflow.in/1532>



- ✓  $A$  : means both are either true OR both are false. then it will be true = ExNOR

$B \& C$  : whenever any one of the literal is complemented then ExOR can be turned to ExNOR and complement sign on the literal can be removed. So these two also represents ExNOR operation of  $x$  and  $y$ .

Answer is option D. It is the ExOR operation b/w the two.

29 votes

-- Amar Vashishth (25.2k points)

4.4.21 Boolean Algebra: GATE CSE 2014 Set 3 | Question: 55 [top](#)

<https://gateoverflow.in/2090>



- ✓ XOR is associative and commutative. Also,  $A \oplus A = 0$  and  $A \oplus 1 = \overline{A}$  and  $A \oplus 0 = A$ . So
$$\begin{aligned} & ((1 \oplus P) \oplus (P \oplus Q)) \oplus ((P \oplus Q) \oplus (Q \oplus 0)) \\ & \implies (1 \oplus P) \oplus ((P \oplus Q) \oplus (P \oplus Q)) \oplus (Q \oplus 0) \\ & \implies (1 \oplus 0) \oplus (P \oplus Q) \\ & \implies 1 \oplus (P \oplus Q) \\ & \implies \overline{(P \oplus Q)} \end{aligned}$$

Correct Answer: D

40 votes

-- Arjun Suresh (332k points)

4.4.22 Boolean Algebra: GATE CSE 2015 Set 1 | Question: 39 [top](#)

<https://gateoverflow.in/8294>



- ✓  $g$  is preserving 0 as when all inputs are zero, output is always 0 and so  $g$  cannot be functionally complete.

$f$  is not preserving 0.

$f$  is not preserving 1. (when all inputs are 1, output is 0).

$f$  is not linear as in  $XY'$  only one (odd) input ( $X = 1, Y = Z = 0$ ) needs to be 1 and in  $X'YZ$  two inputs (even) ( $X = 0, Y = Z = 1$ ) need to be 1.

$f$  is not monotone as changing  $Y$  from 0 to 1, can take  $f$  from 1 to 0.

$f$  is not self dual as  $f(X, Y, Z) \neq \neg f(\neg X, \neg Y, \neg Z)$

So,  $f$  satisfies all 5 conditions required for functional completeness.

Hence, B is the answer.

<http://cs.ucsb.edu/~victor/ta/cs40/posts-criterion.pdf>

References



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93 votes

-- Arjun Suresh (332k points)

4.4.23 Boolean Algebra: GATE CSE 2015 Set 2 | Question: 37 [top](#)

<https://gateoverflow.in/8162>



- ✓  $F = [D' + AB' + A'C + AC'D + A'C'D']'$

$$F' = D' + AB' + A'C + AC'D + A'C'D$$

Now we have  $F'$ , so fill 0's (maxterms) in K-map for each term

As for  $D'$

		CD	00	01	11	10
		AB	00	01	11	10
AB	00	0				0
	01	0				0
	11	0				0
	10	0				0

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Similarly for  $AB'$ ,  $A'C$ ,  $AC'D$  and  $A'C'D$ . We will get

		CD	00	01	11	10
		AB	00	01	11	10
AB	00	0	0	0	0	0
	01	0	0	0	0	0
	11	0	0			0
	10	0	0	0	0	0

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We get one place for minterm and that is **ABCD**

拇指 62 votes

-- Praveen Saini (41.9k points)



4.4.24 Boolean Algebra: GATE CSE 2016 Set 1 | Question: 06 [top](#)

<https://gateoverflow.in/39629>

- ✓ These are properties of XOR function.. so answer is A)  $x\bar{y} + \bar{x}y$

拇指 35 votes

-- Abhilash Panicker (7.6k points)

4.4.25 Boolean Algebra: GATE CSE 2016 Set 2 | Question: 08 [top](#)

<https://gateoverflow.in/39540>



- ✓ Let  $x_1 = 1$   $x_2 = 1$   $x_3 = 1$  and  $x_4 = 1$

such that  $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 1 \oplus 1 \oplus 1 \oplus 1 = 0$

- classroom.gateoverflow.in  
A.  $x_1x_2x_3x_4 = 1.1.1.1 = 1$  , False  
B.  $x_1x_3 + x_2 = 1.1 + 1 = 1$  , False  
C. is always True.  
D.  $x_1 + x_2 + x_3 + x_4 = 1 + 1 + 1 + 1 = 1$  , False

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Correct Answer: C

拇指 61 votes

-- Praveen Saini (41.9k points)



4.4.26 Boolean Algebra: GATE CSE 2017 Set 2 | Question: 27 [top](#)

<https://gateoverflow.in/118494>

- ✓ Let us try to simplify (minimize) the expression given in each option

**Option - A:**  $wx + w(x + y) + x(x + y) = x + wy$

$wx + wx + wy + x$

$wx + wy + x$   
 $x(1+w) + wy$   
 $x + wy$

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**Option - B:**  $\bar{w}\bar{x}(y+\bar{z}) + \bar{w}x = \bar{w} + x + \bar{y}z$

$\bar{w}\bar{x} + \bar{(y+\bar{z})} + \bar{w}x$   
 $\bar{w} + x + \bar{y}z + \bar{w}x$   
 $\bar{w} + \bar{w}x + x + \bar{y}z$   
 $\bar{w} + x + \bar{y}z$

**Option - D:**  $(w+y)(wxy + wyz) = wxy + wyz$

$wxy + wyz + wxy + wyz$   
 $wxy + wyz$

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Option A, B, D are matching fine.

Hence, **Option - C** is the answer

拇指图标 29 votes

-- Arunav Khare (3.9k points)

#### 4.4.27 Boolean Algebra: GATE CSE 2018 | Question: 4 top

<https://gateoverflow.in/204078>



- ✓ Consider Option(D). LHS can be simplified as,

$$(P \oplus \bar{P}) \oplus Q = 1 \oplus Q = \bar{Q}$$

Similarly, for RHS

$$(P \odot \bar{P}) \odot \bar{Q} = 0 \odot \bar{Q} = Q$$

LHS  $\neq$  RHS therefore, **Option (D)** is the correct answer.

Other options can be simplified as follows.

1.  $\overline{P \oplus Q} = \overline{\overline{PQ} + \overline{PQ}} = \overline{(\overline{PQ})} \overline{(\overline{PQ})} = (\bar{P} + Q) (P + \bar{Q}) = PQ + \bar{P} \bar{Q} = P \odot Q$
2.  $\bar{P} \oplus Q = (\bar{P}) \bar{Q} + (\bar{P}) Q = PQ + \bar{P} \bar{Q} = P \odot Q$
3.  $\bar{P} \oplus \bar{Q} = (\bar{P}) (\bar{Q}) + (\bar{P}) (\bar{Q}) = \bar{P}Q + P\bar{Q} = P \oplus Q$

拇指图标 18 votes

-- Prateek Dwivedi (3.5k points)

#### 4.4.28 Boolean Algebra: GATE CSE 2019 | Question: 6 top

<https://gateoverflow.in/302842>



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1. XOR is associative so  $(x \oplus y) \oplus z = x \oplus (y \oplus z)$
2. For 2 input, XOR and XNOR are complement to each other i.e.  $x \oplus y = (xy + x'y')'$
3.  $x \oplus y = x + y$  if  $xy = 0$

Only false statement is option B.

拇指图标 26 votes

-- Digvijay (44.9k points)

#### 4.4.29 Boolean Algebra: GATE CSE 2021 Set 1 | Question: 42 top

<https://gateoverflow.in/357409>



- ✓  $F = (X + Y + Z)(\bar{X} + Y)(\bar{Y} + Z)$

Taking complement of above expression;

$$\bar{F} = \overline{(X + Y + Z)(\bar{X} + Y)(\bar{Y} + Z)}$$

Applying De-Morgan's law;

$$\bar{F} = \overline{(X + Y + Z)} + \overline{(X + Y)} + \overline{(\bar{Y} + Z)}$$

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$$\bar{F} = (\bar{X} \cdot \bar{Y} \cdot \bar{Z}) + \bar{X} \cdot \bar{Y} + \bar{Y} \cdot \bar{Z}$$

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$$[\because \bar{\bar{X}} = X, \text{ Using double negation law}]$$

$$\therefore \bar{F} = (\bar{X} \cdot \bar{Y} \cdot \bar{Z}) + (X \cdot \bar{Y}) + (Y \cdot \bar{Z}) \rightarrow \text{Option (D)}$$

Taking  $\bar{Y}$  as common we get;

$$\bar{F} = \bar{Y} [(\bar{X} \cdot \bar{Z}) + X] + Y \cdot \bar{Z}$$

[ $\because A + BC = (A + B)(A + C)$  Applying distributive law here]

$$\bar{F} = \bar{Y} [(X + \bar{X})(X + \bar{Z})] + Y \cdot \bar{Z}$$

$$\bar{F} = \bar{Y} [X + \bar{Z}] + Y \cdot \bar{Z}$$

$$\bar{F} = X \cdot \bar{Y} + \bar{Y} \cdot \bar{Z} + Y \cdot \bar{Z}$$

Taking  $\bar{Z}$  as common

$$\bar{F} = X \cdot \bar{Y} + \bar{Z}(Y + \bar{Y})$$

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$$\therefore (Y + \bar{Y} = 1) \text{ using complement law}$$

$$\therefore \bar{F} = X \cdot \bar{Y} + \bar{Z} \rightarrow \text{Option (B)}$$

Applying distributive law here we get;

$$\bar{F} = (X + \bar{Z})(\bar{Y} + \bar{Z}) \rightarrow \text{Option (C)}$$

So, correct options are *B, C, D*.

Option A is false and can be proved as follows:

Take  $X = 0, Y = 1, Z = 0$

Now,  $F = 0$ , since  $(\bar{Y} + Z)$  term will be zero. So,  $\bar{F}$  must be 1.

But option A gives 0 as the term  $X + \bar{Y}$  evaluates to 0. So, option A is not equal to  $\bar{F}$ .

### Properties of Boolean Algebra

#### References



1 votes

-- Hira (14.1k points)

#### 4.4.30 Boolean Algebra: GATE IT 2004 | Question: 44 top 5

► <https://gateoverflow.in/3687>



AB	00	01	11	10
C				
0			1	1
1	1	1		1

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So, the equivalent expression will be  $\bar{A}C + A\bar{C} + A\bar{B}$

(B) option

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36 votes

-- Arjun Suresh (332k points)

#### 4.4.31 Boolean Algebra: GATE IT 2005 | Question: 7 [top](#)

<https://gateoverflow.in/3752>



- ✓ Correct answer is C

$$(A \oplus B) \oplus C$$

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$$\text{At } C = 0, (A \oplus B) \oplus C = (A \oplus B) \quad \text{---(I)} \quad [\text{as } 0 \oplus x = 0.x' + 0'.x = x]$$

$$\text{At } C = 0, ABC + A'(B \oplus C) + B'(A \oplus C)$$

$$= 0 + A'(B \oplus 0) + B'(A \oplus 0) = A'B + AB' = A \oplus B \quad \text{---(II)}$$

$$\text{At } C = 1, (A \oplus B) \oplus C = (A \odot B) \quad \text{--- (III)} \quad [\text{as } 1 \oplus x = 1.x' + 1'.x = x' ]$$

$$\text{At } C = 1, ABC + A'(B \oplus C) + B'(A \oplus C)$$

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$$= AB + A'(B \oplus 1) + B'(A \oplus 1) = AB + A'B' = (A \odot B) \quad \text{--(IV)}$$

from eq (I), (II), (III) and (IV) it is clear

$$(A \oplus B) \oplus C = ABC + A'(B \oplus C) + B'(A \oplus C)$$

39 votes

-- Praveen Saini (41.9k points)

#### 4.5

#### Booth's Algorithm (6) [top](#)

#### 4.5.1 Booths Algorithm: GATE CSE 1990 | Question: 8b [top](#)

<https://gateoverflow.in/85671>



State the Booth's algorithm for multiplication of two numbers. Draw a block diagram for the implementation of the Booth's algorithm for determining the product of two 8-bit signed numbers.

gate1990 descriptive digital-logic booths-algorithm

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Answer

#### 4.5.2 Booths Algorithm: GATE CSE 1996 | Question: 1.23 [top](#)

<https://gateoverflow.in/2727>



Booth's algorithm for integer multiplication gives worst performance when the multiplier pattern is

- A. 101010...1010
- B. 100000...0001
- C. 111111...1111
- D. 011111...1110

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gate1996 digital-logic booths-algorithm normal

Answer

#### 4.5.3 Booths Algorithm: GATE CSE 1999 | Question: 1.20 [top](#)

<https://gateoverflow.in/1473>



Booth's coding in 8 bits for the decimal number -57 is:

- A. 0 - 100 + 1000
- B. 0 - 100 + 100 - 1
- C. 0 - 1 + 100 - 10 + 1
- D. 00 - 10 + 100 - 1

gate1999 digital-logic number-representation booths-algorithm normal

goclasses.in

tests.gatecse.in

Answer



Using Booth's Algorithm for multiplication, the multiplier  $-57$  will be recoded as

- A. 0 -1 00 1 00 -1
- B. 1 1 00 0 1 1 1
- C. 0 -1 0 0 1 0 0 0
- D. 0 1 0 0 -1 0 0 1

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[gate2005-it](#) [digital-logic](#) [booths-algorithm](#) [normal](#)

Answer



When multiplicand  $Y$  is multiplied by multiplier  $X = x_{n-1}x_{n-2}\dots x_0$  using bit-pair recoding in Booth's algorithm, partial products are generated according to the following table.

Row	$x_{i+1}$	$x_i$	$x_{i-1}$	Partial Product
1	0	0	0	0
2	0	0	1	$Y$
3	0	1	0	$Y$
4	0	1	1	$2Y$
5	1	0	0	?
6	1	0	1	$-Y$
7	1	1	0	$-Y$
8	1	1	1	?

The partial products for rows 5 and 8 are

- A.  $2Y$  and  $Y$
- B.  $-2Y$  and  $2Y$
- C.  $-2Y$  and 0
- D. 0 and  $Y$

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[gate2006-it](#) [digital-logic](#) [booths-algorithm](#) [difficult](#)

Answer



The two numbers given below are multiplied using the Booth's algorithm.

Multiplicand :            0101 1010 1110 1110  
Multiplier:            0111 0111 1011 1101

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How many additions/Subtractions are required for the multiplication of the above two numbers?

- A. 6
- B. 8
- C. 10
- D. 12

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[gate2008-it](#) [digital-logic](#) [booths-algorithm](#) [normal](#)

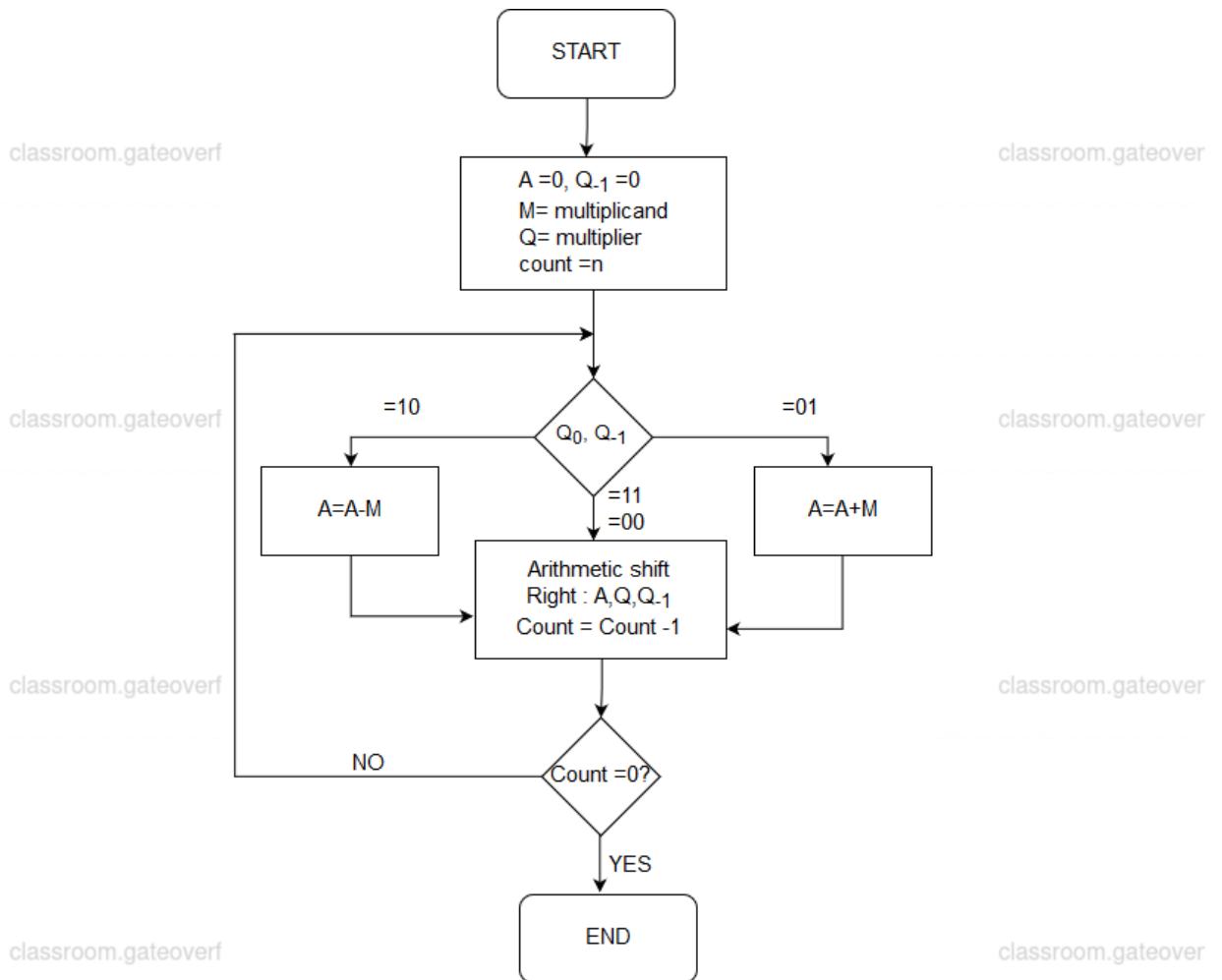
Answer

### Answers: Booths Algorithm



- ✓ [Booth's multiplication algorithm](#) is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation.

The block diagram for the implementation of the Booth's algorithm for determining the product of two 8-bit signed numbers is as shown below.



The Multiplier and Multiplicand are placed in the  $Q$  and  $M$  registers, respectively. There is also a 1-bit register placed logically to the right of the least significant bit( $Q_0$ ) of the  $Q$  register and designated  $Q_{-1}$ .

The results of the multiplication will appear in the  $A$  and  $Q$  registers.  $A$  and  $Q_{-1}$  are initialized to 0. The control logic scans the bits of the multiplier one at a time. Now, as each bit is examined, the bit to its right is also examined. If the two bits are the same (11 or 00), then all of the bits of the  $A$ ,  $Q$ , and  $Q_{-1}$  registers are shifted to the right 1 bit. If the two bits differ, then the multiplicand is added to or subtracted from the  $A$  register, depending on whether the two bits are 01 or 10. Following, the addition or subtraction, the right shift occurs.

In either case, the right shift is such that the leftmost bit of  $A$ , namely  $A_{n-1}$ , not only is shifted into  $A_{n-2}$ , but also remains in  $A_{n-1}$ . This is required to preserve the sign of the number in  $A$  and  $Q$ . It is known as an arithmetic shift, because it preserves the sign bit.

#### References



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6 votes

-- Satbir Singh (21k points)

#### 4.5.2 Booths Algorithm: GATE CSE 1996 | Question: 1.23 top ↗

↗ <https://gateoverflow.in/2727>



✓ Answer: A

The worst case of an implementation using Booth's algorithm is when pairs of 01s or 10s occur very frequently in the multiplier.

30 votes

-- Rajarshi Sarkar (27.9k points)



- ✓ Convert 57 to Binary & Get 2's complement. It is "11000111" & Attach one extra 0 to right of it  
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110001110

To calculate booth code subtract right digit from left digit in every consecutive 2 digits.

So, 11 → 0, 10 → +1. Finally, 10 → +1

So, answer is (B).

There is another way to solve this question.

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$0 - 100 + 100 - 1 \rightarrow$  If you check binary weighted sum of this code you will get  $-57$ . This is trick to quick check. Booth code is always equivalent to its original value if checked as weighted code. If you check it before doing above procedure & if only one of option maps, you don't need to do above procedure, just mark the answer.

Here,  $(-1) \times 64 + (+1) \times 8 + (-1) \times 1 = -57$ .

1 like 37 votes

-- Akash Kanase (36k points)



- ✓ 2's complement of  $-57$  is (11000111)

**Booth multiplier :**

$$\begin{array}{r} 1 \quad 1 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1 \quad 1 \\ 1 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1 \quad 1 \quad 0 \\ \hline 0 \quad -1 \quad 0 \quad 0 \quad 1 \quad 0 \quad 0 \quad -1 \end{array} \quad (\text{put } 0 \text{ in 1st and shift multiplier left by 1 bit})$$

Use this encoded scheme: 00 → 0, 01 → +1, 10 → -1, 11 → 0

Correct Answer: A.

1 like 21 votes

-- Prashant Singh (47.2k points)



- ✓ We can have 1 bit or 2 bit Booth codes. This question is about 2 bit Booth codes. In Booth's algorithm, we get partial products by multiplying specific codes with the multiplicand. These partial products are used to get the actual product. We initially calculate 2 bit booth code of the multiplier in this question. Then each bit of the code is multiplied with the multiplicand to get the partial product as shown in the last column of the given table.  
 Here, the multiplicand is  $Y$ . So, notice that each row of partial product column is multiplied with  $Y$ .

Now, the question is how to get these codes i.e., how to represent a multiplier with a 2 bit booth code. For that we need to look at the pair of 3 bits as shown in the table below. To get code  $C_i$ , look for 3 bits as shown.

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$x_{i+1}$	$x_i$	$x_{i+1}$	Boothcode( $C_i$ )
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	2
1	0	0	-2
1	0	1	-1
1	1	0	-1
1	1	1	0

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Now, multiply  $i^{\text{th}}$  code to get partial product.

Therefore, Option C is correct.

1 like 6 votes

-- Monanshi Jain (7k points)



Answer is **B**.

Append **0** the end of multiplier : 0111 0111 1011 1101 **0**

Now, Paired bits from right end as 00-(**0**), 01-(+1), 10-(**1**) and 11-(**0**)

note:- pairs are overlapped.

Count +1=4 (additions required)

Count -1=4 (subtractions required)

So, total 8 pair hence addition/subtraction required = 8.

27 votes

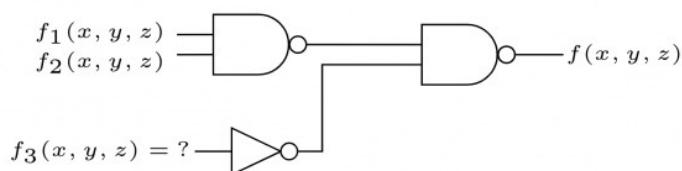
-- Rajarshi Sarkar (27,9k points)

## 4.6

## Canonical Normal Form (7) top



Consider the following logic circuit whose inputs are functions  $f_1, f_2, f_3$  and output is  $f$



Given that

- $f_1(x, y, z) = \Sigma(0, 1, 3, 5)$
- $f_2(x, y, z) = \Sigma(6, 7)$ , and
- $f(x, y, z) = \Sigma(1, 4, 5)$ .

$f_3$  is

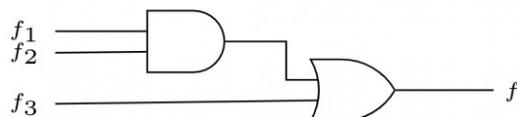
- A.  $\Sigma(1, 4, 5)$
- B.  $\Sigma(6, 7)$
- C.  $\Sigma(0, 1, 3, 5)$
- D. None of the above

[gate2002-cse](#) [digital-logic](#) [normal](#) [canonical-normal-form](#) [circuit-output](#)

**Answer**



Given  $f_1, f_3$  and  $f$  in canonical sum of products form (in decimal) for the circuit



$$f_1 = \Sigma m(4, 5, 6, 7, 8)$$

$$f_3 = \Sigma m(1, 6, 15)$$

$$f = \Sigma m(1, 6, 8, 15)$$

then  $f_2$  is

- A.  $\Sigma m(4, 6)$
- B.  $\Sigma m(4, 8)$
- C.  $\Sigma m(6, 8)$

D.  $\Sigma m(4, 6, 8)$

gate2008-cse digital-logic canonical-normal-form easy

Answer 

4.6.3 Canonical Normal Form: GATE CSE 2010 | Question: 6 [top](#)

<https://gateoverflow.in/2177>



The minterm expansion of  $f(P, Q, R) = PQ + Q\bar{R} + P\bar{R}$  is

- A.  $m_2 + m_4 + m_6 + m_7$
- B.  $m_0 + m_1 + m_3 + m_5$
- C.  $m_0 + m_1 + m_6 + m_7$
- D.  $m_2 + m_3 + m_4 + m_5$

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gate2010-cse digital-logic canonical-normal-form normal

Answer 

4.6.4 Canonical Normal Form: GATE CSE 2015 Set 3 | Question: 43 [top](#)

<https://gateoverflow.in/8503>



The total number of prime implicants of the function  $f(w, x, y, z) = \sum(0, 2, 4, 5, 6, 10)$  is \_\_\_\_\_

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Answer 

4.6.5 Canonical Normal Form: GATE CSE 2015 Set 3 | Question: 44 [top](#)

<https://gateoverflow.in/8504>



Given the function  $F = P' + QR$ , where  $F$  is a function in three Boolean variables  $P, Q$  and  $R$  and  $P' = !P$ , consider the following statements.

- (S1) $F = \sum(4, 5, 6)$
  - (S2) $F = \sum(0, 1, 2, 3, 7)$
  - (S3) $F = \Pi(4, 5, 6)$
  - (S4) $F = \Pi(0, 1, 2, 3, 7)$
- Which of the following is true?
- A. (S1)-False, (S2)-True, (S3)-True, (S4)-False
  - B. (S1)-True, (S2)-False, (S3)-False, (S4)-True
  - C. (S1)-False, (S2)-False, (S3)-True, (S4)-True
  - D. (S1)-True, (S2)-True, (S3)-False, (S4)-False

gate2015-cse-set3 digital-logic canonical-normal-form normal

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Answer 

4.6.6 Canonical Normal Form: GATE CSE 2019 | Question: 50 [top](#)

<https://gateoverflow.in/302798>



What is the minimum number of 2-input NOR gates required to implement a 4-variable function expressed in sum-of-minterms form as  $f = \sum(0, 2, 5, 7, 8, 10, 13, 15)$ ? Assume that all the inputs and their complements are available. Answer:

gate2019-cse numerical-answers digital-logic canonical-normal-form

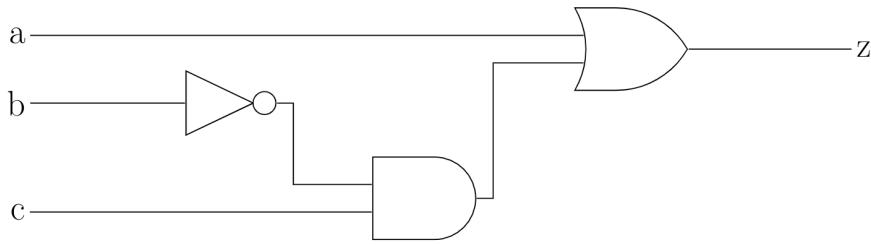
Answer 

4.6.7 Canonical Normal Form: GATE CSE 2020 | Question: 28 [top](#)

<https://gateoverflow.in/333203>



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Which one of the following minterm lists represents the circuit given above?

- A.  $z = \sum(0, 1, 3, 7)$
- B.  $z = \sum(1, 4, 5, 6, 7)$
- C.  $z = \sum(2, 4, 5, 6, 7)$
- D.  $z = \sum(2, 3, 5)$

gate2020-cse

digital-logic

canonical-normal-form

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Answer

#### Answers: Canonical Normal Form

4.6.1 Canonical Normal Form: GATE CSE 2002 | Question: 2-1

<https://gateoverflow.in/831>



- ✓  $f = ((f_1 f_2)' f_3')' = f_1 f_2 + f_3$

In minimum sum of products form, AND of two expressions will contain the common terms. Since  $f_1$  and  $f_2$  don't have any common term,  $f_1 f_2$  is 0 and hence  $f = f_3 = \Sigma(1, 4, 5)$ .

Correct Answer: A

81 votes

-- Arjun Suresh (332k points)

4.6.2 Canonical Normal Form: GATE CSE 2008 | Question: 8

<https://gateoverflow.in/406>



- ✓ Answer is C.

With AND gates we will choose intersection of min-terms.

With OR gates we will take union of min-terms.

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45 votes

-- Ankit Rokde (6.9k points)

4.6.3 Canonical Normal Form: GATE CSE 2010 | Question: 6

<https://gateoverflow.in/2177>



$$\begin{aligned}
 & \checkmark PQ + QR' + PR' = PQR + PQR' + PQR' + P'QR' + PQR' + PQ'R' \\
 & = PQR + PQR' + P'QR' + PQ'R' (111 + 110 + 010 + 100) \\
 & = m_7 + m_6 + m_2 + m_4
 \end{aligned}$$

Option A.

Alternatively,  
Using K-map

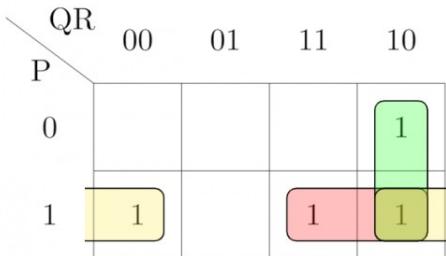
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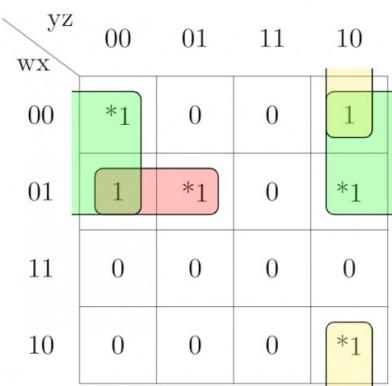
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34 votes

-- Arjun Suresh (332k points)

#### 4.6.4 Canonical Normal Form: GATE CSE 2015 Set 3 | Question: 43 top ↗

↗ <https://gateoverflow.in/8503>



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As you can see that there is one 4-set and two 2-set that are covering the star marked 1's (i.e. the ones that are not covered by any other combinations).

So, the answer is 3.

53 votes

-- Tamojit Chatterjee (1.9k points)

#### 4.6.5 Canonical Normal Form: GATE CSE 2015 Set 3 | Question: 44 top ↗

↗ <https://gateoverflow.in/8504>



- ✓  $F = P' + QR$ , draw the Kmap for this

We can find the minterm  $\sum(0, 1, 2, 3, 7)$  and maxterm  $\Pi(4, 5, 6)$

So, option A is correct: (S1)-False, (S2)-True, (S3)-True, (S4)-False

33 votes

-- Anoop Sonkar (4.1k points)

$$F = P' + QR$$

for SOP we have :

$$F = P \cdot 1 + 1 \cdot QR' = P'(Q + Q')(R + R') + (P + P')QR$$

$$P'QR + P'QR' + P'Q'R + P'Q'R' + PQR + P'QR$$

$$P'QR + P'QR' + P'Q'R + P'Q'R' + PQR$$

$F = \sum(0, 1, 2, 3, 7)$  (considering barred terms as 0 and unbarred as 1 and converting them to binary and then to decimal).

now for POS we have :

$$F = P' + QR = (P' + Q)(P' + R) = (P' + Q + 0)(P' + R + 0)$$

$$(P' + Q + R \cdot R')(P' + R + Q \cdot Q')$$

$$(P' + Q + R)(P' + Q + R)(P' + Q + R')(P' + Q' + R)$$

$$(P' + Q + R)(P' + Q + R')(P' + Q' + R)$$

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$F = \prod(4, 5, 6)$  (considering barred terms as 1 and unbarred as 0 and converting them to binary and then to decimal).

<http://mcs.uwsuper.edu/sb/461/PDF/sop.html>

#### References



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15 votes

-- Tamojit Chatterjee (1.9k points)

#### 4.6.6 Canonical Normal Form: GATE CSE 2019 | Question: 50 top

<https://gateoverflow.in/302798>



	CD	00	01	11	10
AB	1	0	0	1	
00	1	0	1	0	1
01	0	1	1	0	
11	0	1	1	0	
10	1	0	0	1	

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$$f = (B' + D) \cdot (B + D')$$

It is mentioned that both Complementary as well as Uncomplementary forms are available.

$$B' \text{ NOR } D = (B' + D)'$$

$$B \text{ NOR } D' = (B + D')'$$

$$(B' \text{ NOR } D) \text{ NOR } (B \text{ NOR } D')$$

$$= ((B' + D)' + (B + D')')$$

$$= ((B' + D)'' \cdot (B + D'')')$$

$$= ((B' + D) \cdot (B + D'))$$

$$= f$$

Thus, 3 NOR Gates are required.

32 votes

-- Balaji Jegan (3.5k points)

#### 4.6.7 Canonical Normal Form: GATE CSE 2020 | Question: 28 top

<https://gateoverflow.in/333203>



From given circuit  $z = a + b'c$

K-Map for the above expression is:

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	$bc$	00	01	11	10
$a$	0	0	1	0	0
	1	1	1	1	1

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Minterms are  $\sum(1, 4, 5, 6, 7)$ **Hence, option (B) is correct**

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7 votes

-- Ashwani Kumar (13k points)

4.7

Carry Generator (2) [top](#)4.7.1 Carry Generator: GATE CSE 2006 | Question: 36 [top](#)<https://gateoverflow.in/1294>

Given two three bit numbers  $a_2a_1a_0$  and  $b_2b_1b_0$  and  $c$  the carry in, the function that represents the *carry generate* function when these two numbers are added is:

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- A.  $a_2b_2 + a_2a_1b_1 + a_2a_1a_0b_0 + a_2a_0b_1b_0 + a_1b_2b_1 + a_1a_0b_2b_0 + a_0b_2b_1b_0$
- B.  $a_2b_2 + a_2b_1b_0 + a_2a_1b_1b_0 + a_1a_0b_2b_1 + a_1a_0b_2 + a_1a_0b_2b_0 + a_2a_0b_1b_0$
- C.  $a_2 + b_2 + (a_2 \oplus b_2)(a_1 + b_1 + (a_1 \oplus b_1) + (a_0 + b_0))$
- D.  $a_2b_2 + \bar{a}_2a_1b_1 + \bar{a}_2\bar{a}_1a_0b_0 + \bar{a}_2\bar{a}_0b_1b_0 + a_1\bar{b}_2b_1 + \bar{a}_1a_0\bar{b}_2b_0 + a_0\bar{b}_2\bar{b}_1b_0$

gate2006-cse digital-logic normal carry-generator

Answer

4.7.2 Carry Generator: GATE CSE 2007 | Question: 35 [top](#)<https://gateoverflow.in/1233>

In a look-ahead carry generator, the carry generate function  $G_i$  and the carry propagate function  $P_i$  for inputs  $A_i$  and  $B_i$  are given by:

$$P_i = A_i \oplus B_i \text{ and } G_i = A_i B_i$$

The expressions for the sum bit  $S_i$  and the carry bit  $C_{i+1}$  of the look ahead carry adder are given by:

$$S_i = P_i \oplus C_i \text{ and } C_{i+1} = G_i + P_i C_i, \text{ where } C_0 \text{ is the input carry.}$$

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all  $P_i$  and  $G_i$  are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with  $S_3, S_2, S_1, S_0$  and  $C_4$  as its outputs are respectively:

- A. 6, 3
- B. 10, 4
- C. 6, 4
- D. 10, 5

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gate2007-cse digital-logic normal carry-generator adder

Answer

## Answers: Carry Generator

4.7.1 Carry Generator: GATE CSE 2006 | Question: 36 [top](#)<https://gateoverflow.in/1294>

✓  $c_1 = a_0 b_0$

$$c_2 = a_1 b_1 + a_1 c_1 + b_1 c_1$$

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$$c_3 = a_2 b_2 + a_2 c_2 + b_2 c_2$$

$$= a_2 b_2 + a_2 a_1 b_1 + a_2 a_1 c_1 + a_2 b_1 c_1 + b_2 a_1 b_1 + b_2 a_1 c_1 + b_2 b_1 c_1$$

$$= a_2 b_2 + a_2 a_1 b_1 + a_2 a_1 a_0 b_0 + a_2 b_1 a_0 b_0 + b_2 a_1 b_1 + b_2 a_1 a_0 b_0 + b_2 b_1 a_0 b_0$$

Option is A.

Considering the carry in function  $c$ ,  $c_1 = a_0 b_0 + a_0 c + b_0 c$ , but  $c$  is missing in all options and hence ignored.

65 votes

-- Arjun Suresh (332k points)

#### 4.7.2 Carry Generator: GATE CSE 2007 | Question: 35 top

<https://gateoverflow.in/1233>



✓  $C1 = G0 + C0.P0$

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$$C2 = G1 + G0.P1 + C0.P0.P1$$

$$C3 = G2 + G1.P2 + G0.P1.P2 + C0.P0.P1.P2$$

$C4 = G3 + G2.P3 + G1.P2.P3 + G0.P1.P2.P3 + C0.P0.P1.P2.P3$  // read this as carry is generated in 3<sup>rd</sup> stage OR carry is generated in 2<sup>nd</sup> stage AND propagated to 3<sup>rd</sup> stage OR carry is generated in 1<sup>st</sup> stage AND carry is propagated through 2<sup>nd</sup> AND 3<sup>rd</sup> stage OR carry is generated in 0th stage AND propagated through 1<sup>st</sup> 2<sup>nd</sup> AND 3<sup>rd</sup> stage OR initial carry is propagated through 0<sup>th</sup>, 1<sup>st</sup>, 2<sup>nd</sup> AND 3<sup>rd</sup> stage.

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4 OR gates are required for  $C1, C2, C3, C4$

- 1 AND gate for  $C1$
- 2 AND gate for  $C2$
- 3 AND gate for  $C3$
- 4 AND gate for  $C4$
- AND = 10
- OR = 4

Correct Answer: B.

60 votes

-- Vikrant Singh (11.2k points)

#### 4.8

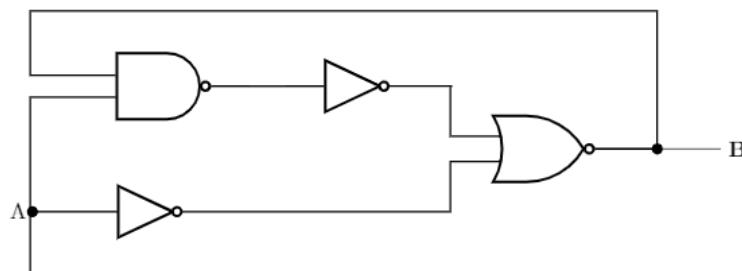
#### Circuit Output (38) top

##### 4.8.1 Circuit Output: GATE CSE 1989 | Question: 4-ix top

<https://gateoverflow.in/88164>



Explain the behaviour of the following logic circuit with level input  $A$  and output  $B$ .



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[gate1989](#) [descriptive](#) [digital-logic](#) [circuit-output](#)

Answer

##### 4.8.2 Circuit Output: GATE CSE 1990 | Question: 3-i top

<https://gateoverflow.in/84051>



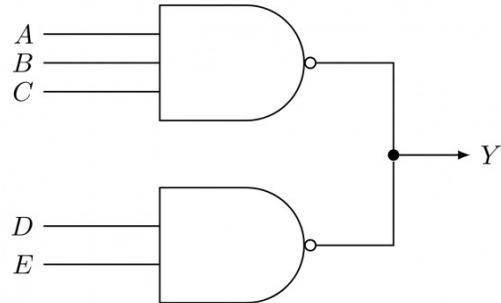
Choose the correct alternatives (More than one may be correct).

Two NAND gates having open collector outputs are tied together as shown in below figure.

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The logic function  $Y$ , implemented by the circuit is,

- A.  $Y = ABC + DE$
- B.  $Y = \overline{ABC} + \overline{DE}$
- C.  $Y = ABC \cdot DE$
- D.  $Y = \overline{ABC} \cdot \overline{DE}$

gate1990 normal digital-logic circuit-output

Answer

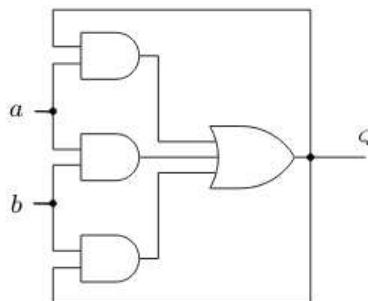
#### 4.8.3 Circuit Output: GATE CSE 1991 | Question: 5-a top ↗

<https://gateoverflow.in/531>



Analyse the circuit in Fig below and complete the following table

a	b	$Q_n$
0	0	
0	1	
1	0	
1	1	



gate1991 digital-logic normal circuit-output sequential-circuit descriptive

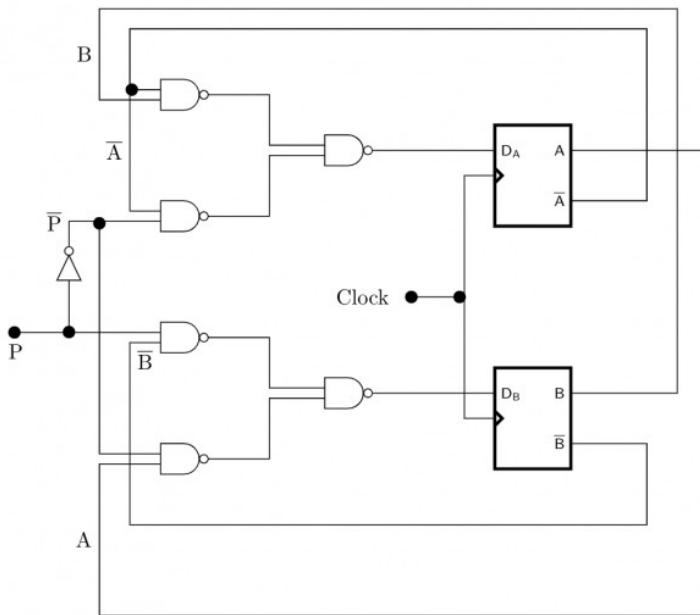
Answer

#### 4.8.4 Circuit Output: GATE CSE 1993 | Question: 19 top ↗

<https://gateoverflow.in/2316>



A control algorithm is implemented by the NAND – gate circuitry given in figure below, where  $A$  and  $B$  are state variable implemented by  $D$  flip-flops, and  $P$  is control input. Develop the state transition table for this controller.



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gate1993 digital-logic sequential-circuit flip-flop circuit-output normal descriptive

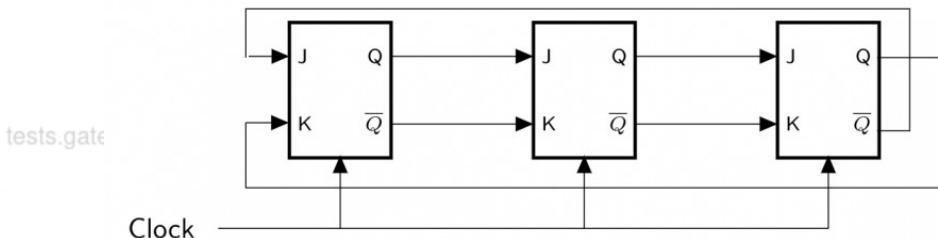
Answer ↗

#### 4.8.5 Circuit Output: GATE CSE 1993 | Question: 6-3 top ↗

↗ <https://gateoverflow.in/17237>



For the initial state of 000, the function performed by the arrangement of the J-K flip-flops in figure is:



- A. Shift Register
- B. Mod- 3 Counter
- C. Mod- 6 Counter
- D. Mod- 2 Counter
- E. None of the above

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tests.gatecse.in

gate1993 digital-logic sequential-circuit flip-flop digital-counter circuit-output multiple-selects

Answer ↗

#### 4.8.6 Circuit Output: GATE CSE 1993 | Question: 6.1 top ↗

↗ <https://gateoverflow.in/2288>

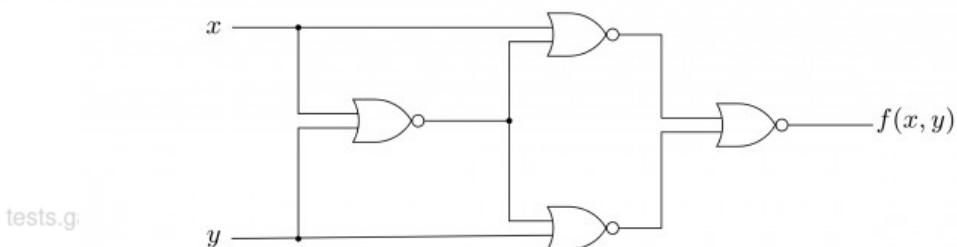


Identify the logic function performed by the circuit shown in figure.

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- A. exclusive OR  
 B. exclusive NOR  
 C. NAND  
 D. NOR  
 E. None of the above

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gate1993 digital-logic combinational-circuits circuit-output normal

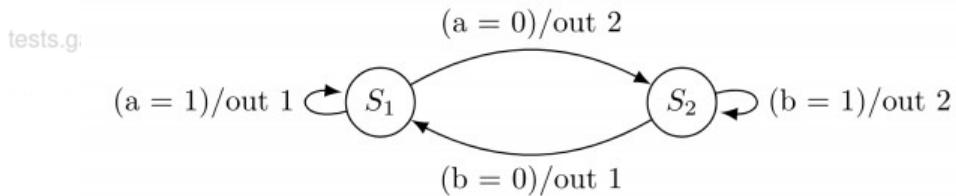
Answer 

**4.8.7 Circuit Output: GATE CSE 1993 | Question: 6.2** top ↺

<https://gateoverflow.in/17235>



If the state machine described in figure should have a stable state, the restriction on the inputs is given by



- A.  $a \cdot b = 1$   
 B.  $a + b = 1$   
 C.  $\bar{a} + \bar{b} = 0$   
 D.  $\overline{a \cdot b} = 1$   
 E.  $\overline{a + b} = 1$

gate1993 digital-logic normal circuit-output sequential-circuit

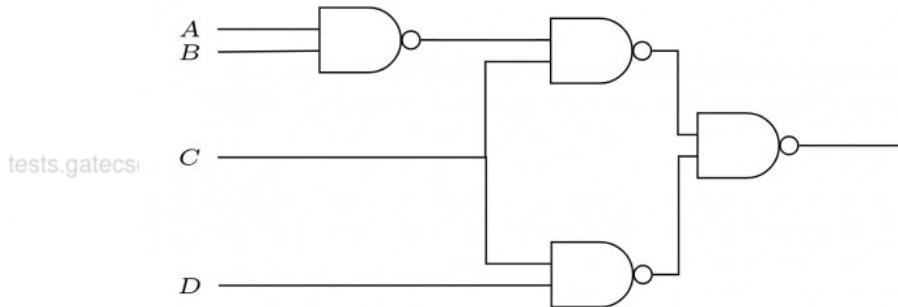
Answer 

**4.8.8 Circuit Output: GATE CSE 1994 | Question: 1.8** top ↺

<https://gateoverflow.in/2445>



The logic expression for the output of the circuit shown in figure below is:



- A.  $\overline{AC} + \overline{BC} + CD$   
 B.  $\overline{AC} + \overline{BC} + CD$   
 C.  $ABC + \overline{C} \overline{D}$   
 D.  $\overline{A} \overline{B} + \overline{B} \overline{C} + CD$

gate1994 digital-logic circuit-output normal

Answer 

**4.8.9 Circuit Output: GATE CSE 1994 | Question: 11** top ↺

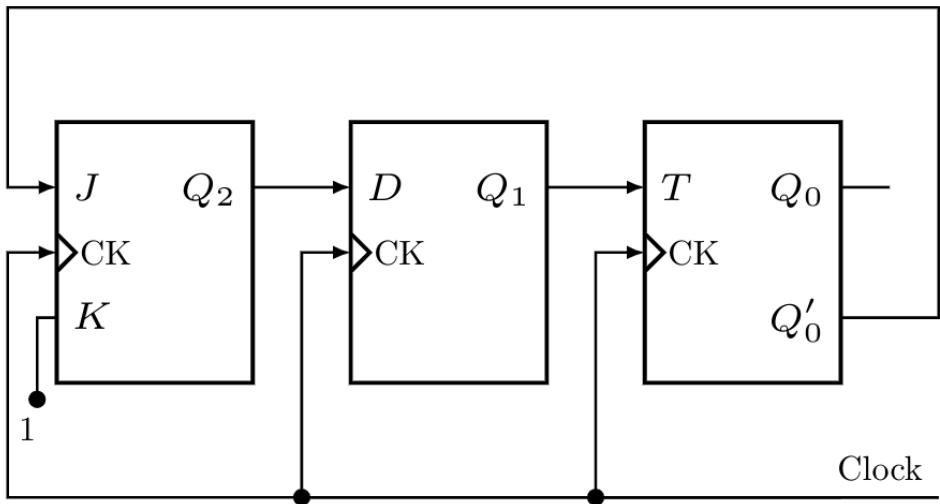
<https://gateoverflow.in/2507>



Find the contents of the flip-flop  $Q_2, Q_1$  and  $Q_0$  in the circuit of figure, after giving four clock pulses to the clock terminal. Assume  $Q_2 Q_1 Q_0 = 000$  initially.

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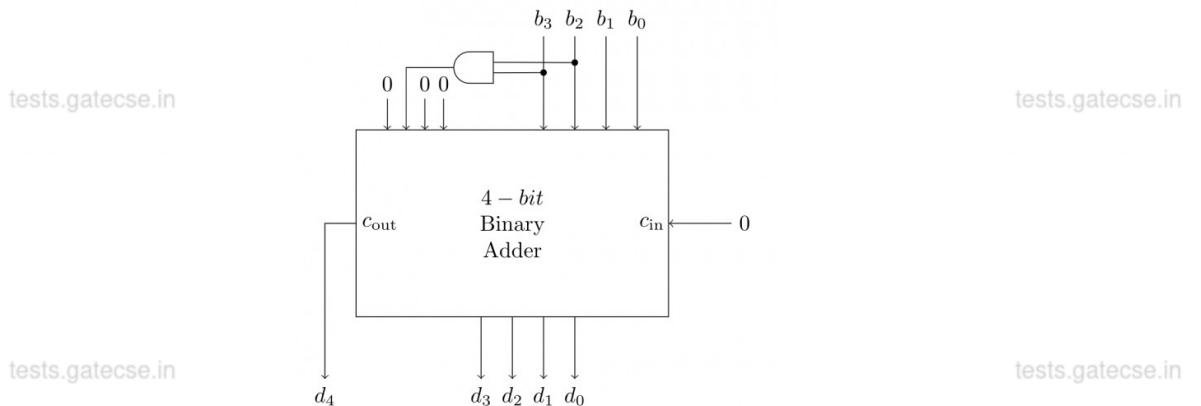
gate1994 digital-logic sequential-circuit digital-counter circuit-output normal descriptive

Answer ↗

#### 4.8.10 Circuit Output: GATE CSE 1996 | Question: 2.21 top ↗



Consider the circuit in below figure which has a four bit binary number  $b_3 b_2 b_1 b_0$  as input and a five bit binary number,  $d_4 d_3 d_2 d_1 d_0$  as output.



- A. Binary to Hex conversion
- B. Binary to BCD conversion
- C. Binary to Gray code conversion
- D. Binary to radix - 12 conversion

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gate1996 digital-logic circuit-output normal

Answer ↗

#### 4.8.11 Circuit Output: GATE CSE 1996 | Question: 24-a top ↗

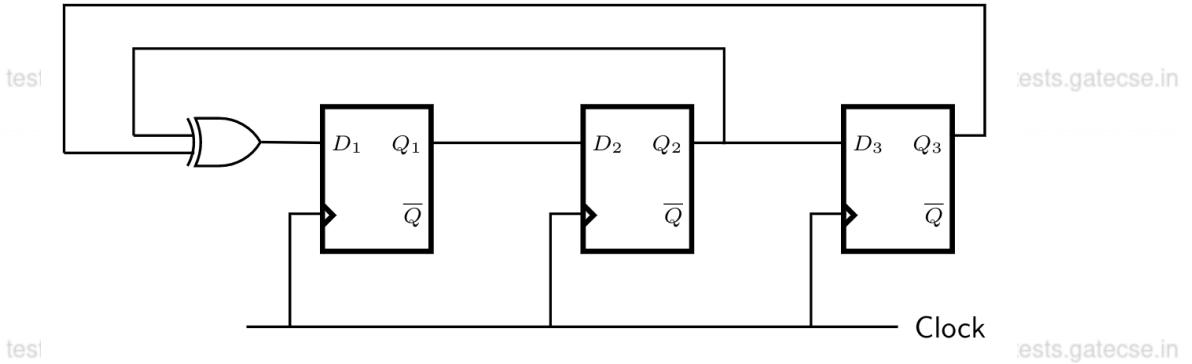


Consider the synchronous sequential circuit in the below figure

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Draw a state diagram, which is implemented by the circuit. Use the following names for the states corresponding to the values of flip-flops as given below.

Q1	Q2	Q3	State
0	0	0	S <sub>0</sub>
0	0	1	S <sub>1</sub>
—	—	—	—
—	—	—	—
—	—	—	—
1	1	1	S <sub>7</sub>

gate1996 digital-logic circuit-output normal descriptive

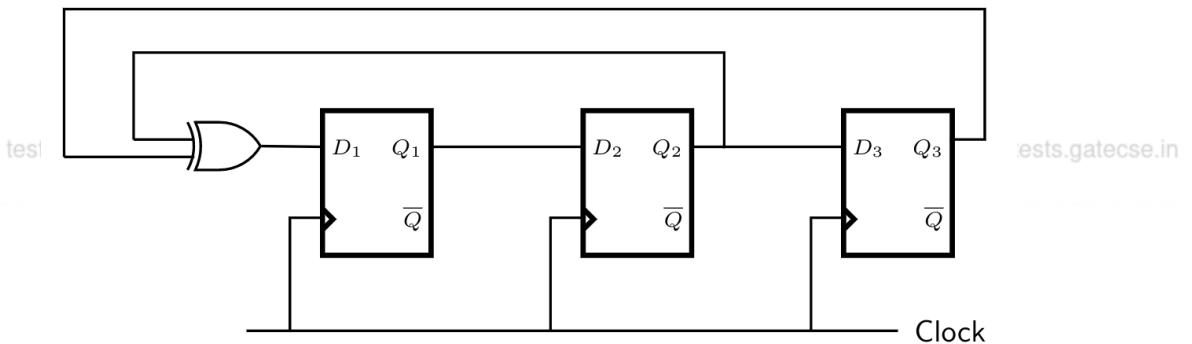
Answer ↗

#### 4.8.12 Circuit Output: GATE CSE 1996 | Question: 24-b top ↗

↗ <https://gateoverflow.in/203691>



Consider the synchronous sequential circuit in the below figure



Given that the initial state of the circuit is S<sub>4</sub>, identify the set of states, which are not reachable.

gate1996 normal digital-logic circuit-output descriptive

Answer ↗

#### 4.8.13 Circuit Output: GATE CSE 1997 | Question: 5.5 top ↗

↗ <https://gateoverflow.in/2256>

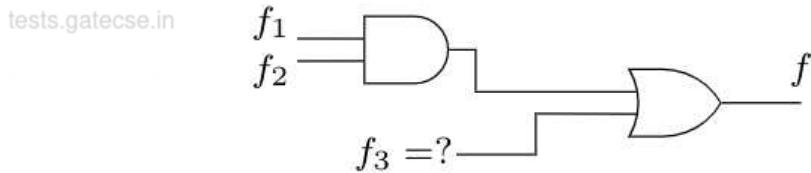


Consider a logic circuit shown in figure below. The functions  $f_1$ ,  $f_2$  and  $f$  (in canonical sum of products form in decimal notation) are:

$$f_1(w, x, y, z) = \sum 8, 9, 10$$

$$f_2(w, x, y, z) = \sum 7, 8, 12, 13, 14, 15$$

$$f(w, x, y, z) = \sum 8, 9$$



The function  $f_3$  is

- A.  $\sum 9, 10$
- B.  $\sum 9$
- C.  $\sum 1, 8, 9$
- D.  $\sum 8, 10, 15$

[gate1997](#) [digital-logic](#) [circuit-output](#) [normal](#)

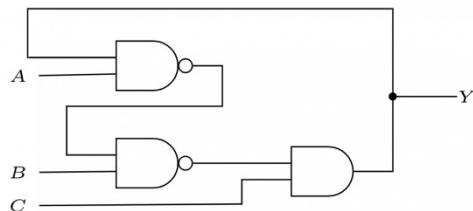
[Answer](#)

#### 4.8.14 Circuit Output: GATE CSE 1999 | Question: 2.8 top ↗

<https://gateoverflow.in/1486>



Consider the circuit shown below. In a certain steady state, the line  $Y$  is at '1'. What are the possible values of  $A, B$  and  $C$  in this state?



- A.  $A = 0, B = 0, C = 1$
- B.  $A = 0, B = 1, C = 1$
- C.  $A = 1, B = 0, C = 1$
- D.  $A = 1, B = 1, C = 1$

[gate1999](#) [digital-logic](#) [circuit-output](#) [normal](#)

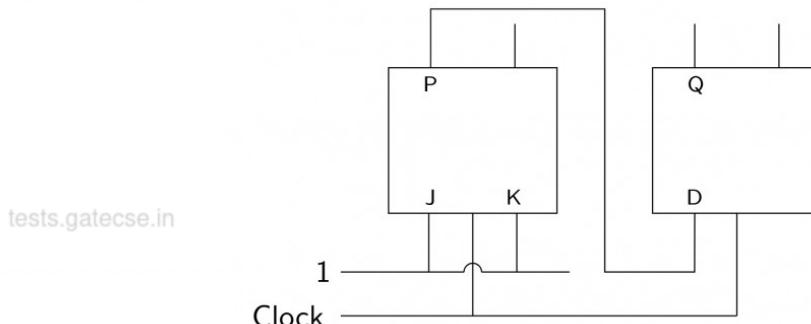
[Answer](#)

#### 4.8.15 Circuit Output: GATE CSE 2000 | Question: 2.12 top ↗

<https://gateoverflow.in/659>



The following arrangement of master-slave flip flops



has the initial state of  $P, Q$  as 0, 1 (respectively). After three clock cycles the output state  $P, Q$  is (respectively),

- A. 1, 0
- B. 1, 1

- C. 0, 0  
D. 0, 1

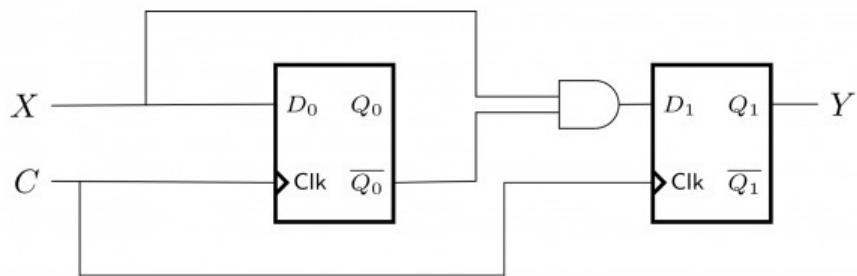
Answer ↗

4.8.16 Circuit Output: GATE CSE 2001 | Question: 2.8 top ↗

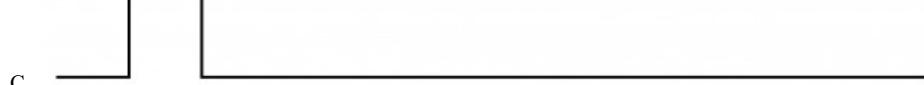
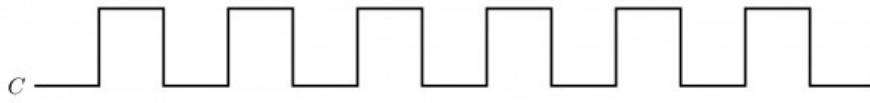
↗ <https://gateoverflow.in/726>



Consider the following circuit with initial state  $Q_0 = Q_1 = 0$ . The D Flip-flops are positive edged triggered and have set up times 20 nanosecond and hold times 0.



Consider the following timing diagrams of X and C. The clock period of  $C \geq 40$  nanosecond. Which one is the correct plot of Y?



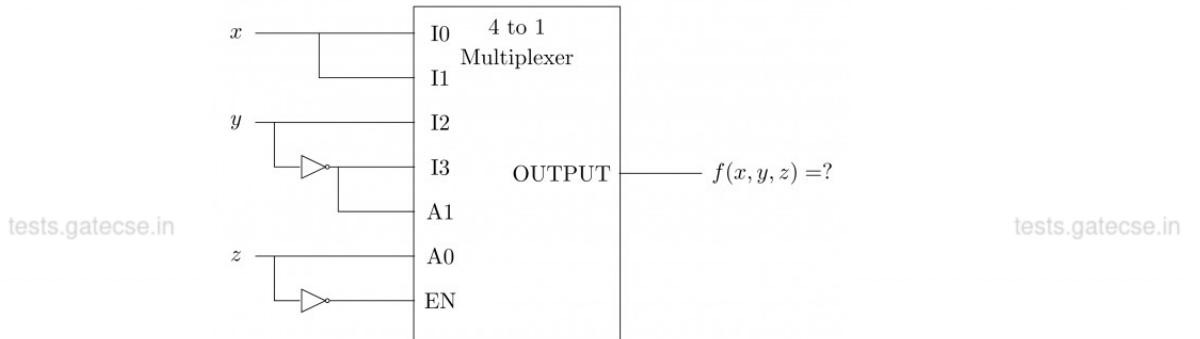
Answer ↗

4.8.17 Circuit Output: GATE CSE 2002 | Question: 2.2 top ↗

↗ <https://gateoverflow.in/832>



Consider the following multiplexer where  $I0, I1, I2, I3$  are four data input lines selected by two address line combinations  $A1A0 = 00, 01, 10, 11$  respectively and  $f$  is the output of the multiplexor. EN is the Enable input.



The function  $f(x, y, z)$  implemented by the above circuit is

- A.  $xyz'$
- B.  $xy + z$
- C.  $x + y$
- D. None of the above

[gate2002-cse](#) [digital-logic](#) [circuit-output](#) [normal](#)

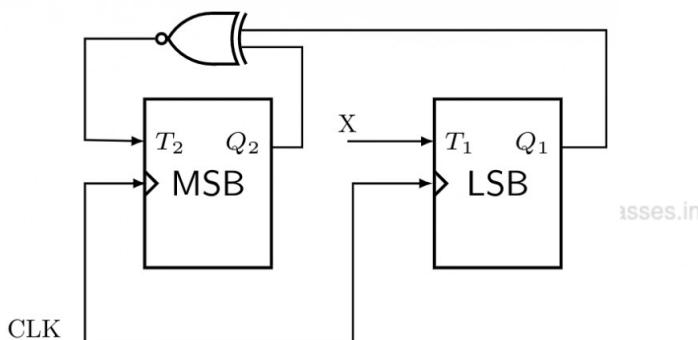
[Answer](#)

#### 4.8.18 Circuit Output: GATE CSE 2004 | Question: 61 top ↗

<https://gateoverflow.in/1056>



Consider the partial implementation of a 2-bit counter using  $T$ -flip-flops following the sequence  $0 - 2 - 3 - 1$ , as shown below.



To complete the circuit, the input  $X$  should be

- A.  $Q_2^c$
- B.  $Q_2 + Q_1$
- C.  $(Q_1 + Q_2)^c$
- D.  $Q_1 \oplus Q_2$

[gate2004-cse](#) [digital-logic](#) [circuit-output](#) [normal](#)

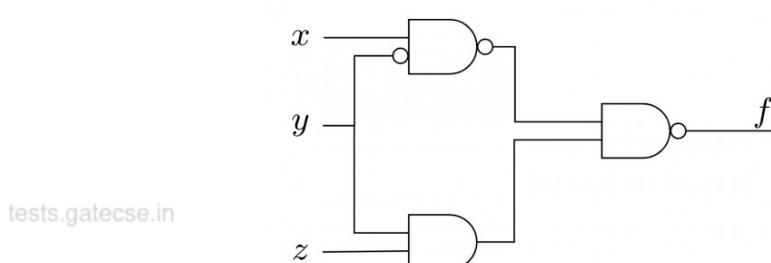
[Answer](#)

#### 4.8.19 Circuit Output: GATE CSE 2005 | Question: 15 top ↗

<https://gateoverflow.in/1351>



Consider the following circuit.



Which one of the following is TRUE?

- A.  $f$  is independent of  $x$
- B.  $f$  is independent of  $y$
- C.  $f$  is independent of  $z$
- D. None of  $x, y, z$  is redundant

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gate2005-cse digital-logic circuit-output normal

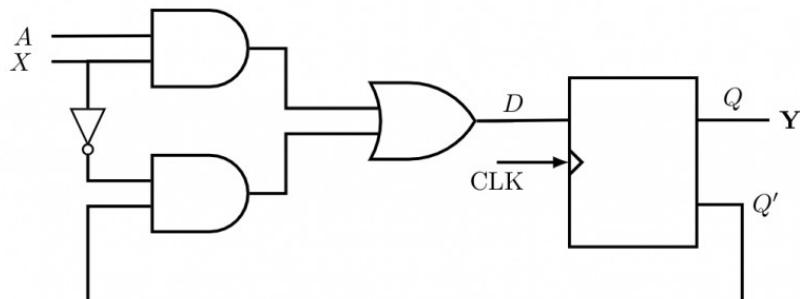
Answer ↗

4.8.20 Circuit Output: GATE CSE 2005 | Question: 62 top 5

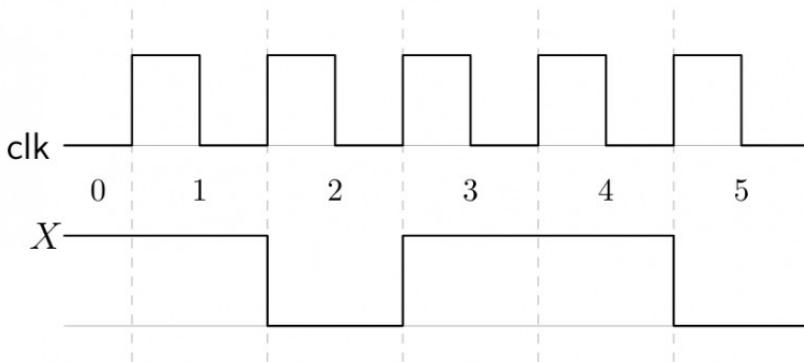
↗ <https://gateoverflow.in/264>



Consider the following circuit involving a positive edge triggered D FF.



Consider the following timing diagram. Let  $A_i$  represents the logic level on the line  $a$  in the  $i$ -th clock period.



Let  $A'$  represent the compliment of  $A$ . The correct output sequence on  $Y$  over the clock periods 1 through 5 is:

- A.  $A_0 A_1 A'_1 A_3 A_4$
- B.  $A_0 A_1 A'_2 A_3 A_4$
- C.  $A_1 A_2 A'_2 A_3 A_4$
- D.  $A_1 A'_2 A_3 A_4 A'_5$

gate2005-cse digital-logic circuit-output normal

Answer ↗

4.8.21 Circuit Output: GATE CSE 2005 | Question: 64 top 5

↗ <https://gateoverflow.in/1387>

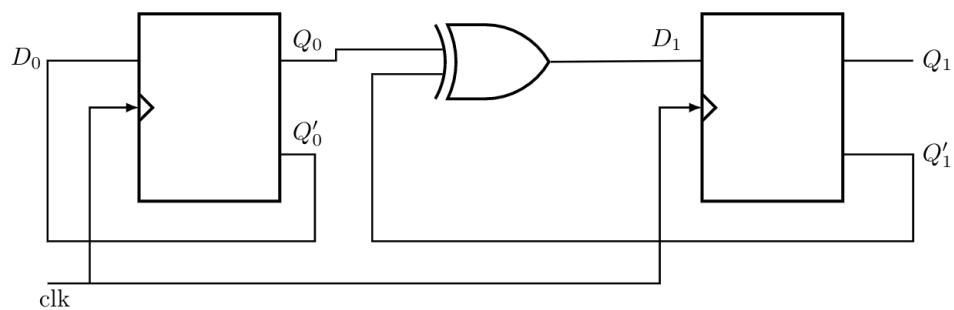


Consider the following circuit:

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The flip-flops are positive edge triggered  $D$  FFs. Each state is designated as a two-bit string  $Q_0Q_1$ . Let the initial state be 00. The state transition sequence is

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$$00 \rightarrow 11 \rightarrow 01$$

A.

$$00 \rightarrow 11$$

B.

$$00 \rightarrow 10 \rightarrow 01 \rightarrow 11$$

C.

$$00 \rightarrow 11 \rightarrow 01 \rightarrow 10$$

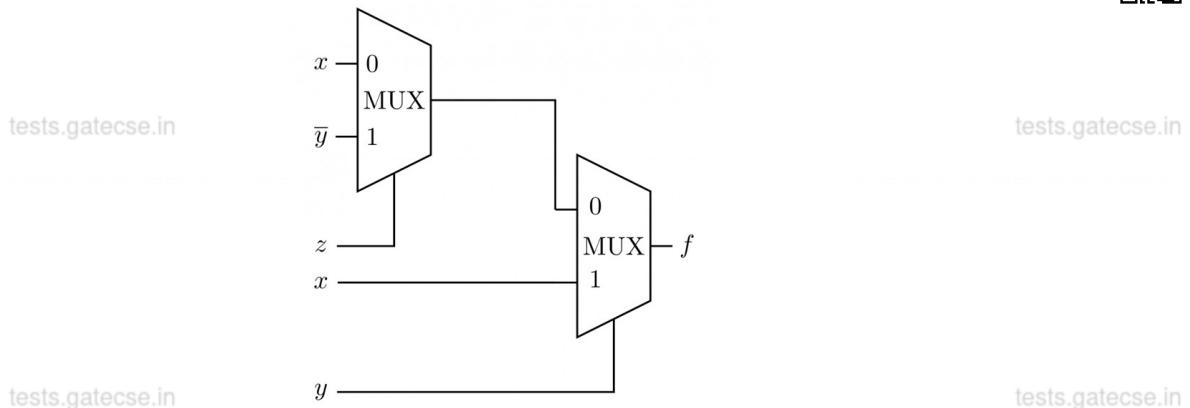
D.

gate2005-cse digital-logic circuit-output  
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Answer

#### 4.8.22 Circuit Output: GATE CSE 2006 | Question: 35 top 5

<https://gateoverflow.in/1292>



Consider the circuit above. Which one of the following options correctly represents  $f(x, y, z)$

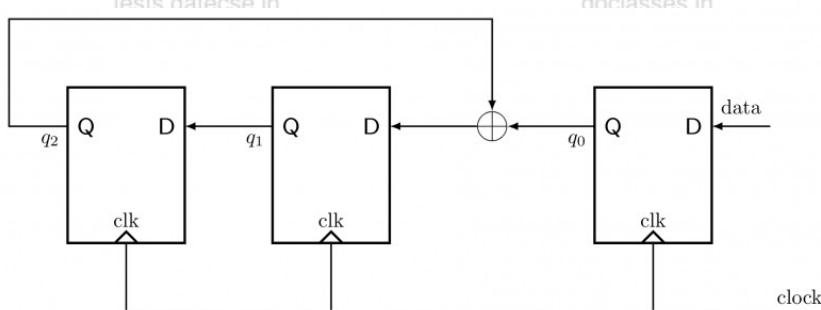
- A.  $x\bar{z} + xy + \bar{y}z$
- B.  $x\bar{z} + xy + \bar{yz}$
- C.  $xz + xy + \bar{yz}$
- D.  $xz + x\bar{y} + \bar{yz}$

gate2006-cse digital-logic circuit-output normal  
goclasses.in tests.gatecse.in

Answer



Consider the circuit in the diagram. The  $\oplus$  operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared).

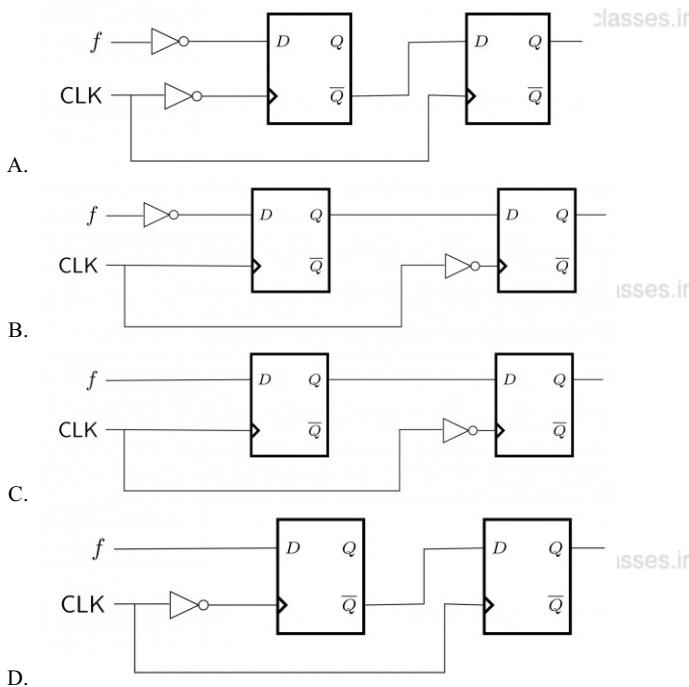


The following data: 100110000 is supplied to the “data” terminal in nine clock cycles. After that the values of  $q_2 q_1 q_0$  are:

- A. 000
- B. 001
- C. 010
- D. 101



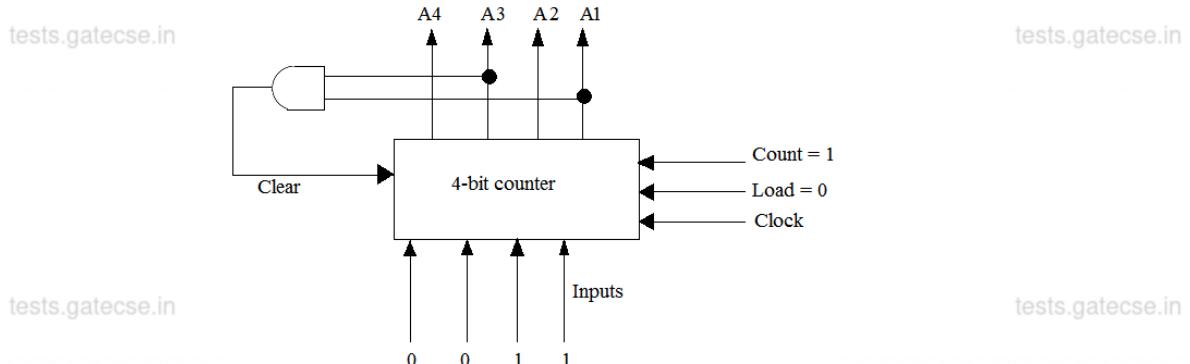
You are given a free running clock with a duty cycle of 50% and a digital waveform  $f$  which changes only at the negative edge of the clock. Which one of the following circuits (using clocked D flip-flops) will delay the phase of  $f$  by  $180^\circ$ ?



The control signal functions of a 4-bit binary counter are given below (where X is “don’t care”):

Clear	Clock	Load	Count	Function
1	X	0	0	Clear to 0
0	X	0	0	No Change
0	↑	1	X	Load Input
0	↑	0	1	Count Next

The counter is connected as follows:



Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence:

- A. 0, 3, 4
- B. 0, 3, 4, 5
- C. 0, 1, 2, 3, 4
- D. 0, 1, 2, 3, 4, 5

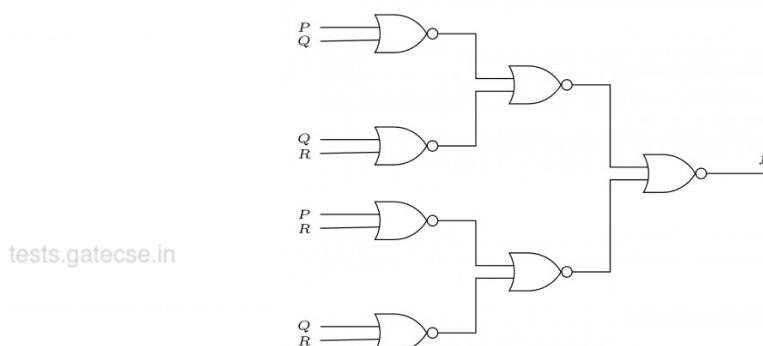
Answer

#### 4.8.26 Circuit Output: GATE CSE 2010 | Question: 31

<https://gateoverflow.in/2205>



What is the boolean expression for the output  $f$  of the combinational logic circuit of NOR gates given below?



- A.  $\overline{Q + R}$
- B.  $P + \overline{Q}$
- C.  $\overline{P + R}$
- D.  $\overline{P + Q + R}$

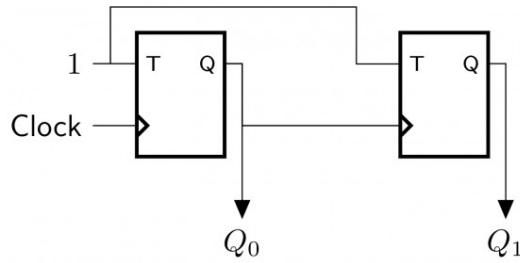
Answer

#### 4.8.27 Circuit Output: GATE CSE 2010 | Question: 32

<https://gateoverflow.in/2206>



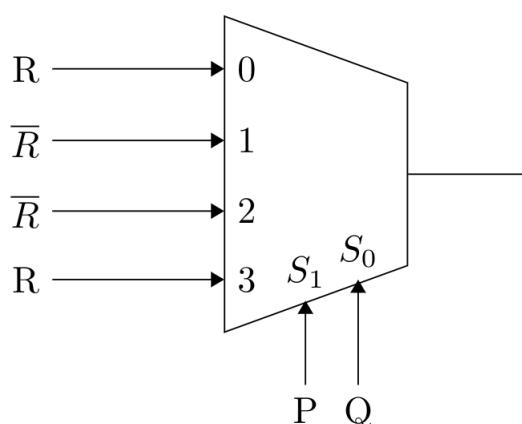
In the sequential circuit shown below, if the initial value of the output  $Q_1Q_0$  is 00. What are the next four values of  $Q_1Q_0$ ?



- A. 11, 10, 01, 00  
 B. 10, 11, 01, 00  
 C. 10, 00, 01, 11  
 D. 11, 10, 00, 01

4.8.28 Circuit Output: GATE CSE 2010 | Question: 9 top ↗

The Boolean expression of the output  $f$  of the multiplexer shown below is



- A.  $P \oplus Q \oplus R$   
 B.  $P \oplus Q \oplus R$   
 C.  $P + Q + R$   
 D.  $\overline{P + Q + R}$

4.8.29 Circuit Output: GATE CSE 2011 | Question: 50 top ↗

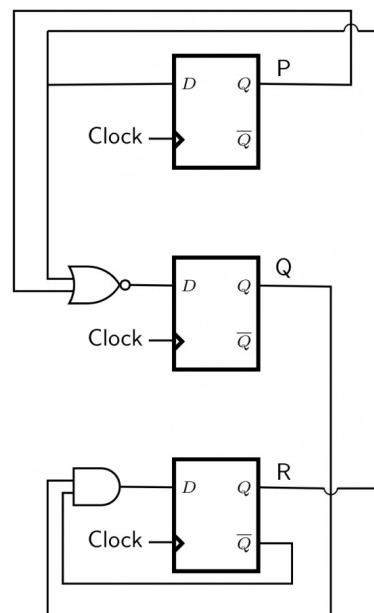
Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.

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If at some instance prior to the occurrence of the clock edge,  $P, Q$  and  $R$  have a value 0, 1 and 0 respectively, what shall be the value of  $PQR$  after the clock edge?

- A. 000
- B. 001
- C. 010
- D. 011

gate2011-cse digital-logic circuit-output flip-flop normal

Answer ↗

#### 4.8.30 Circuit Output: GATE CSE 2011 | Question: 51 top ↗

↗ <https://gateoverflow.in/43318>



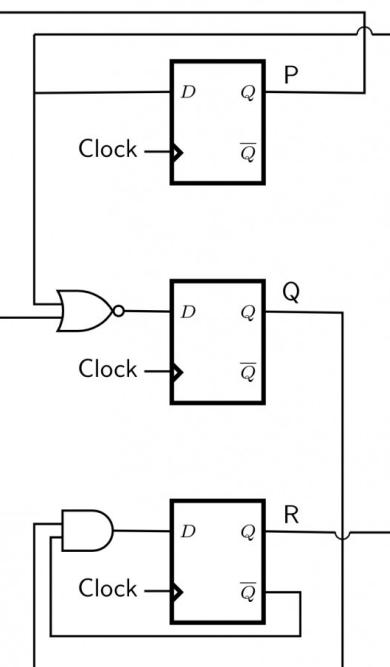
Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.

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If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by  $PQR$  generated by the counter?

- A. 3

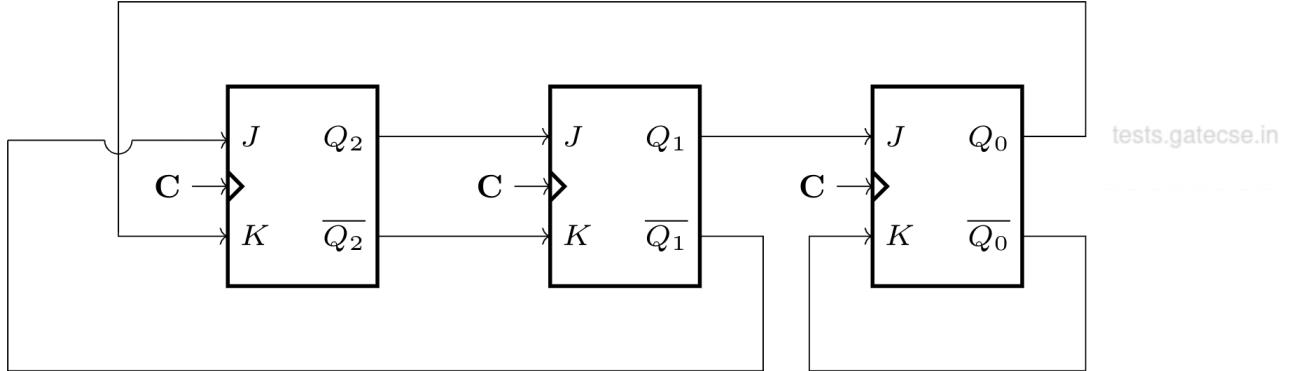
- B. 4  
C. 5  
D. 6

gate2011-cse digital-logic circuit-output normal

Answer 

4.8.31 Circuit Output: GATE CSE 2014 Set 3 | Question: 45 top ↗

<https://gateoverflow.in/2079>



The above synchronous sequential circuit built using JK flip-flops is initialized with  $Q_2Q_1Q_0 = 000$ . The state sequence for this circuit for the next 3 clock cycles is

- A. 001, 010, 011  
B. 111, 110, 101  
C. 100, 110, 111  
D. 100, 011, 001

gate2014-cse-set3 digital-logic circuit-output normal

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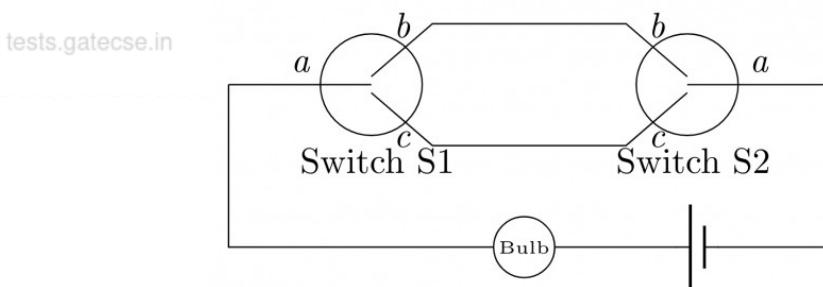
Answer 

4.8.32 Circuit Output: GATE IT 2005 | Question: 10 top ↗

<https://gateoverflow.in/3755>



A two-way switch has three terminals  $a$ ,  $b$  and  $c$ . In ON position (logic value 1),  $a$  is connected to  $b$ , and in OFF position,  $a$  is connected to  $c$ . Two of these two-way switches  $S1$  and  $S2$  are connected to a bulb as shown below.



Which of the following expressions, if true, will always result in the lighting of the bulb ?

- A.  $S1 \cdot \overline{S2}$   
B.  $\overline{S1} + S2$   
C.  $\overline{S1} \oplus S2$   
D.  $S1 \oplus S2$

gate2005-it digital-logic circuit-output normal

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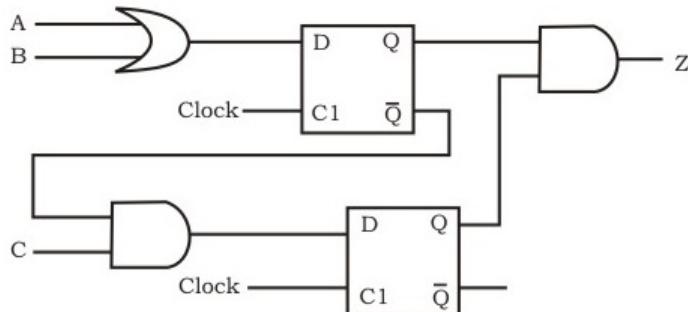
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Answer 



Which of the following input sequences will always generate a 1 at the output  $z$  at the end of the third cycle?

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	A	B	C
A.	0	0	0
	1	0	1
	1	1	1

	A	B	C
B.	1	0	1
	1	1	0
	1	1	1

	A	B	C
C.	0	1	1
	1	0	1
	1	1	1

	A	B	C
D.	0	0	1
	1	1	0
	1	1	1

Answer



The majority function is a Boolean function  $f(x, y, z)$  that takes the value 1 whenever a majority of the variables  $x, y, z$  are 1. In the circuit diagram for the majority function shown below, the logic gates for the boxes labeled  $P$  and  $Q$  are, respectively,

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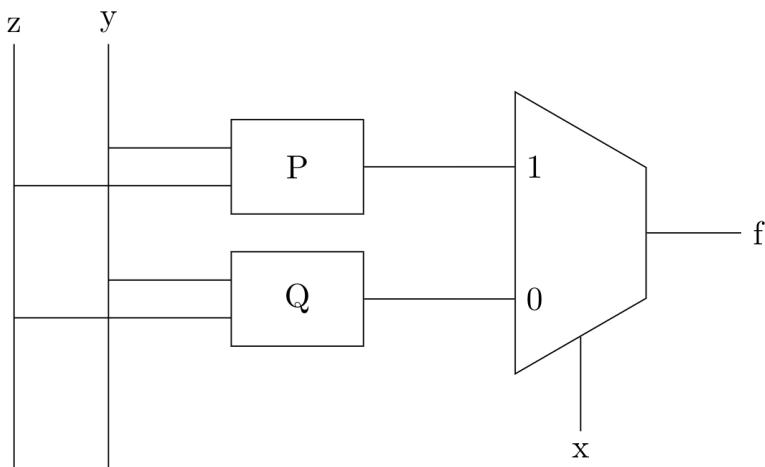
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- A. XOR, AND
- B. XOR, XOR
- C. OR, OR
- D. OR, AND

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gate2006-it digital-logic circuit-output normal

Answer ↗

#### 4.8.35 Circuit Output: GATE IT 2007 | Question: 38 top ↗

↗ <https://gateoverflow.in/3471>



The following expression was to be realized using 2-input AND and OR gates. However, during the fabrication all 2-input AND gates were mistakenly substituted by 2-input NAND gates.

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$(a \cdot b) \cdot c + (a' \cdot c) \cdot d + (b \cdot c) \cdot d + a \cdot d$   
What is the function finally realized ?

- A. 1
- B.  $a' + b' + c' + d'$
- C.  $a' + b + c' + d'$
- D.  $a' + b' + c + d'$

gate2007-it digital-logic circuit-output normal

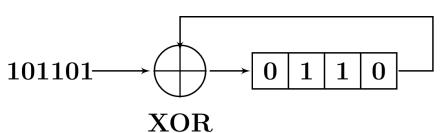
Answer ↗

#### 4.8.36 Circuit Output: GATE IT 2007 | Question: 40 top ↗

↗ <https://gateoverflow.in/3473>



What is the final value stored in the linear feedback shift register if the input is 101101?



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- A. 0110
- B. 1011
- C. 1101
- D. 1111

gate2007-it digital-logic circuit-output normal

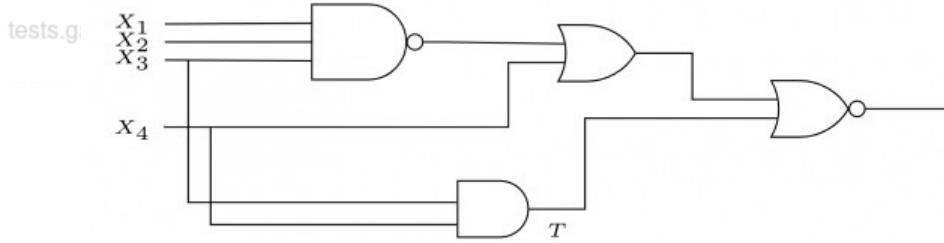
Answer ↗

#### 4.8.37 Circuit Output: GATE IT 2007 | Question: 45 top ↗

↗ <https://gateoverflow.in/3480>



The line  $T$  in the following figure is permanently connected to the ground.



Which of the following inputs ( $X_1X_2X_3X_4$ ) will detect the fault? [ses.in](#)

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- A. 0000
- B. 0111
- C. 1111
- D. None of these

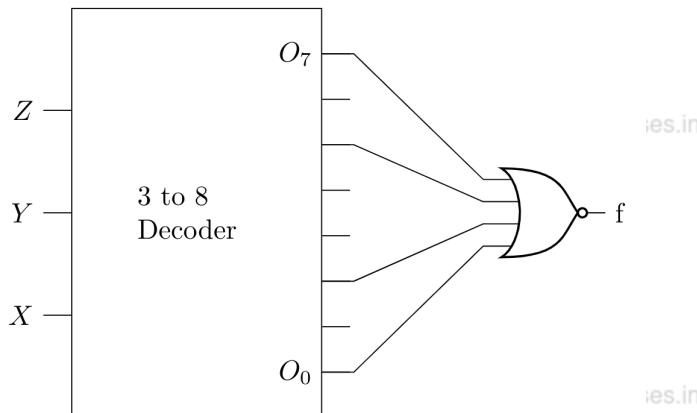
[gate2007-it](#) [digital-logic](#) [circuit-output](#) [normal](#)

[Answer](#)

#### 4.8.38 Circuit Output: GATE IT 2008 | Question: 9 [top](#) [https://gateoverflow.in/3269](#)



What Boolean function does the circuit below realize?



- A.  $xz + \bar{x}\bar{z}$
- B.  $x\bar{z} + \bar{x}z$
- C.  $\bar{x}y + yz$
- D.  $xy + \bar{y}\bar{z}$

[gate2008-it](#) [digital-logic](#) [circuit-output](#) [normal](#)

[Answer](#)

#### Answers: Circuit Output

##### 4.8.1 Circuit Output: GATE CSE 1989 | Question: 4-ix [top](#) [https://gateoverflow.in/88164](#)



- ✓ This is a **sequential circuit** (whose output depends not only on the present value of its input signals but on the sequence of past inputs) not a **combinational** one (whose output depends only on the present inputs), therefore solving using just input variable does not yield correct output.

First we need to simplify the circuit.

The two NOT gates at the input end of the NOR gate can be combined with the gate to get:  $(A' + B')' = AB$

Now, since we have two variables we will have 4 combinations 00 01 10 11.

On analyzing each we will see that for every combination where

- $A = 0$  we have the stable output of 0
- $A = 1$  we will have a RACE condition

**4.8.2 Circuit Output: GATE CSE 1990 | Question: 3-i** [top](#)

<https://gateoverflow.in/84051>

- From [wikipedia \(third paragraph\)](#),

By tying the output of several open collectors together, the common line becomes a "wired AND" (positive-true logic) or "wired OR" (negative-true logic) gate. A "wired AND" behaves like the boolean AND of the two (or more) gates in that it will be logic 1 whenever (all) are in the high impedance state, and 0 otherwise. A "wired OR" behaves like the Boolean OR for negative-true logic, where the output is LOW if any of its inputs are low.

So, after tying the open-collector NAND Gates, the common line becomes a **wired AND**.

$$\text{So, } Y = (\overline{ABC}) \cdot (\overline{DE})$$

$$\text{By D'Morgan's law, } Y = \overline{\overline{ABC} + \overline{DE}}$$

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Hence,

**Correct Answer: Option (B)**

References



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**4.8.3 Circuit Output: GATE CSE 1991 | Question: 5-a** [top](#)

<https://gateoverflow.in/531>

- The output of the circuit given as :  $Q = aQ_{n-1} + ab + bQ_{n-1}$

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Hence,  $Q_n = Q_{n-1}(a+b) + ab$

$$00 \implies Q_{n-1}(0+0) + 0.0 = Q_{n-1}(0) + 0 = 0 + 0 = 0$$

$$01 \implies Q_{n-1}(0+1) + 0.1 = Q_{n-1}(1) + 0 = Q_{n-1} + 0 = Q_{n-1}$$

$$10 \implies Q_{n-1}(1+0) + 1.0 = Q_{n-1}(1) + 0 = Q_{n-1} + 0 = Q_{n-1}$$

$$11 \implies Q_{n-1}(1+1) + 1.1 = Q_{n-1}(1) + 1 = Q_{n-1} + 1 = 1$$

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a	b	Q <sub>n</sub>
0	0	0
0	1	Q <sub>n-1</sub>
1	0	Q <sub>n-1</sub>
1	1	1

**4.8.4 Circuit Output: GATE CSE 1993 | Question: 19** [top](#)

<https://gateoverflow.in/2316>

- $A(t+1) = D_a = A'B + A'P'$

$$B(t+1) = D_b = PB' + P'A$$

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Present State		Input	Next State	
A	B	P	A(t+1)	B(t+1)
0	0	0	1	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	0	0

Note: Recheck the table by putting the values of  $A$ ,  $B$  and  $P$  in equations of  $A(t + 1)$  and  $B(t + 1)$ .

1 like 24 votes

-- Praveen Saini (41.9k points)

#### 4.8.5 Circuit Output: GATE CSE 1993 | Question: 6-3 top

<https://gateoverflow.in/17237>



- ✓ Circuit behaves as shift register and mod 6 counter

Clock Cycle	Output
1	100
2	110
3	111
4	011
5	001
6	000

This is Johnson counter which is an application of Shift Register. And Johnson counter is mod  $2N$  counter.

1 like 50 votes

-- Pooja Palod (24.1k points)

#### 4.8.6 Circuit Output: GATE CSE 1993 | Question: 6.1 top

<https://gateoverflow.in/2288>



- ✓  $(x + x'y').(y + x'y') = (x + y')(x' + y) = xy + x'y' = \text{Exclusive-NOR}$

1 like 16 votes

-- Praveen Saini (41.9k points)

#### 4.8.7 Circuit Output: GATE CSE 1993 | Question: 6.2 top

<https://gateoverflow.in/17235>



- ✓ If  $a = 0$  state changes from  $S_1$  to  $S_2$  and if  $b = 0$  state changes from  $S_2$  to  $S_1$ .

So,  $a = 0, b = 0$  is surely not a stable state as then the states will be oscillating. So, the condition for stability is that both  $a$  and  $b$  should not be 0 together which is given by  $a + b = 1$  or  $\bar{a}\bar{b} = 0$ .

Options A and C are equivalent and both ensures stable states albeit by enforcing stricter than required conditions.

Correct Answer: Option B.

1 like 13 votes

-- Arjun Suresh (332k points)

#### 4.8.8 Circuit Output: GATE CSE 1994 | Question: 1.8 top

<https://gateoverflow.in/2445>



- ✓  $((AB)'C)'(CD)' = ((AB)'C) + CD = (A' + B')C + CD = A'C + B'C + CD$

1 like 39 votes

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#### 4.8.9 Circuit Output: GATE CSE 1994 | Question: 11 top

<https://gateoverflow.in/2507>



- ✓ Initial  $Q_2 = 0, Q_1 = 0, Q_0 = 0$

Clock 1 :

- $Q_2 = 1$  [ $J = (\text{old } Q_0)' = 1, K = 1$ , New  $Q_2 = \text{Complement of old } Q_2 = 1$ ]
- $Q_1 = 0$  [ $D = \text{old } Q_2 = 0$ , new  $Q_1 = D = 0$ ]
- $Q_0 = 0$  [ $T = \text{old } Q_1 = 0$ , New  $Q_0 = \text{old } Q_0 = 0$ ]

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Clock 2 :

- $Q_2 = 0$  [ $J = (\text{old } Q_0)' = 1, K = 1$ , New  $Q_2 = \text{Complement of old } Q_2 = 0$ ]
- $Q_1 = 1$  [ $D = \text{old } Q_2 = 1$ , new  $Q_1 = D = 1$ ]
- $Q_0 = 0$  [ $T = \text{old } Q_1 = 0$ , New  $Q_0 = \text{old } Q_0 = 0$ ]

Clock 3 :

- $Q_2 = 1$  [ $J = (\text{old } Q_0)' = 1, K = 1$ , New  $Q_2 = \text{Complement of old } Q_2 = 1$ ]
- $Q_1 = 0$  [ $D = \text{old } Q_2 = 0$ , New  $Q_1 = D = 0$ ]
- $Q_0 = 1$  [ $T = \text{old } Q_1 = 1$ , New  $Q_0 = \text{complement of old } Q_0 = 1$ ]

Clock 4 :

- $Q_2 = 0$  [ $J = (\text{old } Q_0)' = 0, K = 1$ , new  $Q_2 = \text{Reset} = 0$ ]
- $Q_1 = 1$  [ $D = \text{old } Q_2 = 1$ , new  $Q_1 = D = 1$ ]
- $Q_0 = 1$  [ $T = \text{old } Q_1 = 0$ , new  $Q_0 = \text{old } Q_0 = 1$ ]

After 4 clock pulses  $Q_2Q_1Q_0$  is 011

Note : for JK flipflops,  $Q_{(t+1)} = JQ' + K'Q$ , for D flipflops,  $Q_{(t+1)} = D$ , and for T flipflops  $Q_{(t+1)} = T \oplus Q$  Where  $Q_{(t+1)}$  represent new value of  $Q$ .

31 votes

-- Praveen Saini (41.9k points)



4.8.10 Circuit Output: GATE CSE 1996 | Question: 2.21 [top](#)

<https://gateoverflow.in/2750>

- ✓ Whenever,  $b_2 = b_3 = 1$ , then only 0100 i.e., 4 is added to the given binary number. Let's write all possibilities for  $b$ .

$b_3$	$b_2$	$b_1$	$b_0$
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

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Note that the last 4 combinations (1100, 1101, 1110, 1111) leads to  $b_3$  and  $b_2$  as 1. So, in these combinations only 0100 will be added.

1100 is 12  
1101 is 13  
1110 is 14  
1111 is 15  
in binary unsigned number system.

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$1100 + 0100 = 10000$ .  
 $1101 + 0100 = 10001$  and so on.  
This is conversion to radix 12.

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21 votes

-- Monanshi Jain (7k points)

#### 4.8.11 Circuit Output: GATE CSE 1996 | Question: 24-a top

<https://gateoverflow.in/2776>



✓ State Diagram :

$$S_7 \rightarrow S_3 \rightarrow S_1 \rightarrow S_4 \rightarrow S_2 \rightarrow S_5 \rightarrow S_6 \rightarrow S_7$$

b. Given the initial state  $S_4$ ,  $S_0$  state will not be reachable. If the system enters  $S_0$  state then  $Q_0 = Q_1 = Q_2 = 0$  and after that it will stay in  $S_0$  state indefinitely and can't go to any other state.

18 votes

-- shreya ghosh (2.8k points)

#### 4.8.12 Circuit Output: GATE CSE 1996 | Question: 24-b top

<https://gateoverflow.in/203691>



- $Q_{3N} = D_3 \Rightarrow Q_{3N} = Q_2$
- $Q_{2N} = D_2 \Rightarrow Q_{2N} = Q_1$
- $Q_{1N} = D_1 \Rightarrow Q_{1N} = Q_3 \oplus Q_2$

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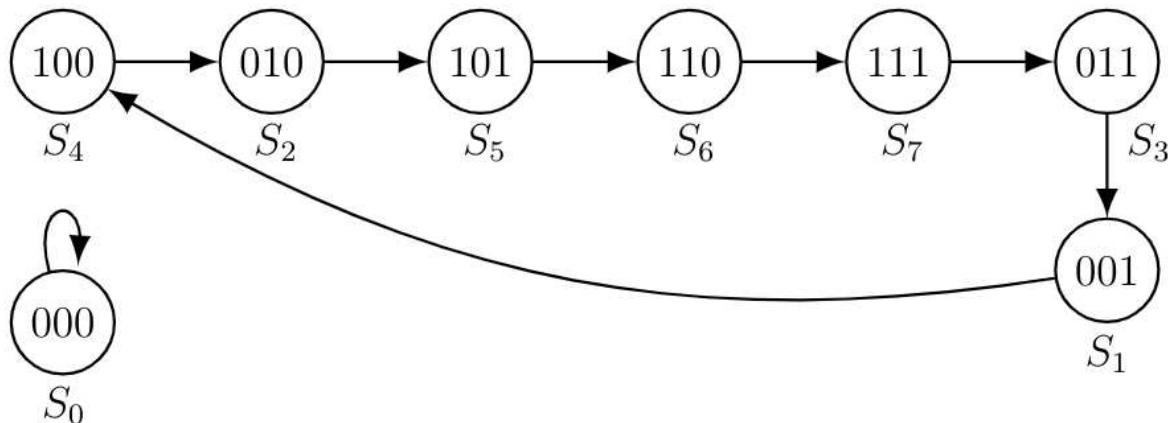
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$Q_1$	$Q_2$	$Q_3$	$Q_{1N}$	$Q_{2N}$	$Q_{3N}$
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	1	1

Given that the initial state  $= S_4 = 100$ .



Unreachable state is  $S_0$

So, set of states which are not reachable =  $\{S_0\}$

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-- Pinaki Dash (1.5k points)

9 votes

#### 4.8.13 Circuit Output: GATE CSE 1997 | Question: 5.5 top

► <https://gateoverflow.in/2256>



✓  $f = (f_1 \wedge f_2) \vee f_3$

Since  $f_1$  and  $f_2$  are in canonical sum of products form,  $f_1 \wedge f_2$  will only contain their common terms- that is  $f_1 \wedge f_2 = \Sigma 8$

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Now,  $\Sigma 8 \vee f_3 = \Sigma 8, 9$

So,  $f_3 = \Sigma 9$

Correct Answer: B

31 votes

-- Arjun Suresh (332k points)

#### 4.8.14 Circuit Output: GATE CSE 1999 | Question: 2.8 top

► <https://gateoverflow.in/1486>



✓  $Y = \overline{(\overline{AY}) \cdot B} \cdot C$

$1 = \overline{A} \cdot B + \overline{C}$

So,  $C = 0$  or  $\overline{A} \cdot B = 1$

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So, option B is TRUE.

19 votes

-- Arjun Suresh (332k points)

#### 4.8.15 Circuit Output: GATE CSE 2000 | Question: 2.12 top

► <https://gateoverflow.in/659>



✓ Here, clocks are applied to both flip flops simultaneously. Outputs for 3 cycles will proceed as follows:

- When 11 is applied to JK flip flop it toggles the value of P. So, output at P will be 1.
- Input to D flip flop will be 0 (initial value of P). So, output at Q will be 0.

JK flip flop it toggles the value of P. So, output at P will be 0.

- Input to D flip flop will be 1 (current value of P). So, output at Q will be 1.

- JK flip flop it toggles the value of P. So, output at P will be 1.

- Input to D flip flop will be 0 (initial value of P) so output at Q will be 0.

So, answer is A.

56 votes

-- Pooja Palod (24.1k points)

#### 4.8.16 Circuit Output: GATE CSE 2001 | Question: 2.8 top

► <https://gateoverflow.in/726>



✓ Answer is (a).

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Given clock is + edge triggered.

See the first positive edge. X is 0, and hence, the output is 0.  $Q_0$  is 0 and  $Q'_0$  is 1.

Second + edge, X is 1 and  $Q'_0$  is also 1. So, output is 1. (When second positive edge of the clock arrives,  $Q'_0$  would surely be 1 because the setup time of flip-flop is given as 20 ns and the clock period is  $\geq 40$  ns)

Third + edge, X is 1 and  $Q'_0$  is 0, So, output is 0. ( $Q'_0$  becomes 0 before the third positive edge, but output Y would not change)

as the flip-flop is positive edge triggered)

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Now, output never changes back to 1 as  $Q'_0$  is always 0 and when  $Q'_0$  finally becomes 1,  $X$  is 0.

Set up time and hold times are given just to ensure that edge triggering works properly.

50 votes

-- Arjun Suresh (332k points)

#### 4.8.17 Circuit Output: GATE CSE 2002 | Question: 2.2 top

<https://gateoverflow.in/832>



- ✓ As  $x$  is connected to  $I0$  &  $I1$ ,  $y$  connected to  $I2$ ,  $y'$  connected to  $I3$  &  $A1$ ,  $z$  connected to  $A0$  and  $z'$  connected to ENABLE ( $EN$ ),

$$f = (\overline{A1} \cdot \overline{A0} \cdot I0 + \overline{A1} \cdot A0 \cdot I1 + A1 \cdot \overline{A0} \cdot I2 + A1 \cdot A0 \cdot I3) \cdot EN$$

$$\begin{aligned} \Rightarrow f &= (xyz' + xyz + y'z'y + zy')z' \\ &= (xyz' + xyz + zy')z' = xyz' \end{aligned}$$

Correct Answer: A

58 votes

-- Digvijay (44.9k points)

#### 4.8.18 Circuit Output: GATE CSE 2004 | Question: 61 top

<https://gateoverflow.in/1056>



- ✓ Sequence is 0 – 2 – 3 – 1 – 0

From the given sequence, we have state table as

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$Q_2$	$Q_1$	$Q_2^+$	$Q_1^+$
0	0	1	0
0	1	0	0
1	0	1	1
1	1	0	1

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Now we have present state and next state, use excitation table of  $T$  flip-flop

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$Q_2$	$Q_1$	$Q_2^+$	$Q_1^+$	$T_2$	$T_1$
0	0	1	0	1	0
0	1	0	0	0	1
1	0	1	1	0	1
1	1	0	1	1	0

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From state table,  $T_2 = Q_2 \odot Q_1$ , and  $T_1 = Q_2 \oplus Q_1$

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$$X = T_1 = Q_2 \oplus Q_1$$

Correct Answer: D

85 votes

-- Praveen Saini (41.9k points)

#### 4.8.19 Circuit Output: GATE CSE 2005 | Question: 15 top

<https://gateoverflow.in/1351>



- ✓ The expression will be

$$f = [(x \cdot y')' \cdot (y \cdot z)]' = [(x' + y) \cdot (y \cdot z)]' = [x' \cdot y \cdot z + y \cdot z]' = [(x' + 1) \cdot (y \cdot z)]' = [1 \cdot (y \cdot z)]' = [y \cdot z]' = y' + z'$$

The final expression only contains  $y$  and  $z$ ,

Therefore, answer will be (a) f is Independent of  $x$

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28 votes

-- jec.himanshu (189 points)

4.8.20 Circuit Output: GATE CSE 2005 | Question: 62 [top](#)

<https://gateoverflow.in/264>



- $D = AX + X'Q'$
- $Y = D$

$A_i$  represent the logic level on the line  $A$  at the  $i^{th}$  clock period. If we see the timing diagram carefully, we can see that during over the rising edge, the output  $Y$  is determined by the  $X$  value just before that rising edge. i.e., during the rising edge say for clk2,  $X$  value that determines the output is 1 and not 0 (because it takes some propagation delay for the 0 to reach the flip flop). Similarly, the  $A$  output that determines the output for clk  $i$ , is  $A_{i-1}$ .

- For clk1,  $X$  is 1, so,  $D = A = A_0$
- For clk2,  $X$  is 1, so  $D = A = A_1$
- For clk3,  $X$  is 0, so  $D = Q'_2 = A'_1$
- For clk4,  $X$  is 1, so  $D = A = A_3$
- For clk5,  $X$  is 1, so  $D = A = A_4$

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So, answer is A choice.

69 votes

-- Arjun Suresh (332k points)

4.8.21 Circuit Output: GATE CSE 2005 | Question: 64 [top](#)

<https://gateoverflow.in/1387>



Clearly,  $Q_0$  alternates in every clk cycle as  $Q'_0$  is fed as input and it is **D** flipflop.

$Q_1$  becomes 1 if its prev value and current  $Q_0$  differs (EXOR).

So, the sequence of transitions will be :  $00 \rightarrow 11 \rightarrow 01 \rightarrow 10 \rightarrow 00$ , (**D**) choice.

34 votes

-- Arjun Suresh (332k points)

4.8.22 Circuit Output: GATE CSE 2006 | Question: 35 [top](#)

<https://gateoverflow.in/1292>



Result of MUX (first one), is, say  $f_1 = x\bar{z} + \bar{y}z$   
Result of MUX(second one),  $f = f_1\bar{y} + xy$

$$\begin{aligned} &= (x\bar{z} + \bar{y}z)\bar{y} + xy \\ &= xy\bar{z} + \bar{y}z + xy \\ &= x(\bar{y}\bar{z} + y) + \bar{y}z \\ &= x(\bar{y} + y)(\bar{z} + y) + \bar{y}z \\ &= xz' + xy + y'z. \end{aligned}$$

Option A. classroom.gateoverflow.in

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Note:

1.  $f = I_0\bar{S} + I_1S$ , for 2 : 1 MUX, where  $I_0$  and  $I_1$  are inputs,  $S$  is the select line
2. Distributive property,  $A + BC = (A + B)(A + C)$
3.  $A + \bar{A} = 1$

52 votes

-- Praveen Saini (41.9k points)

4.8.23 Circuit Output: GATE CSE 2006 | Question: 37 [top](#)

<https://gateoverflow.in/1295>



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Data	$Q_0$	$Q_1$	$Q_2$
1	1	$Q_0_{start} \text{ XOR } Q_2_{start} = 0 \text{ XOR } 0 = 0$	$Q_1_{start} = 0$
0	0	$1 \text{ XOR } 0 = 1$	0
0	0	$0 \text{ XOR } 0 = 0$	1
1	1	$0 \text{ XOR } 1 = 1$	0
1	1	$1 \text{ XOR } 0 = 1$	1
0	0	$1 \text{ XOR } 1 = 0$	1
0	0	$0 \text{ XOR } 1 = 1$	0
0	0	$0 \text{ XOR } 0 = 0$	1
0	0	$0 \text{ XOR } 1 = 1$	0

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So, option C.

40 votes

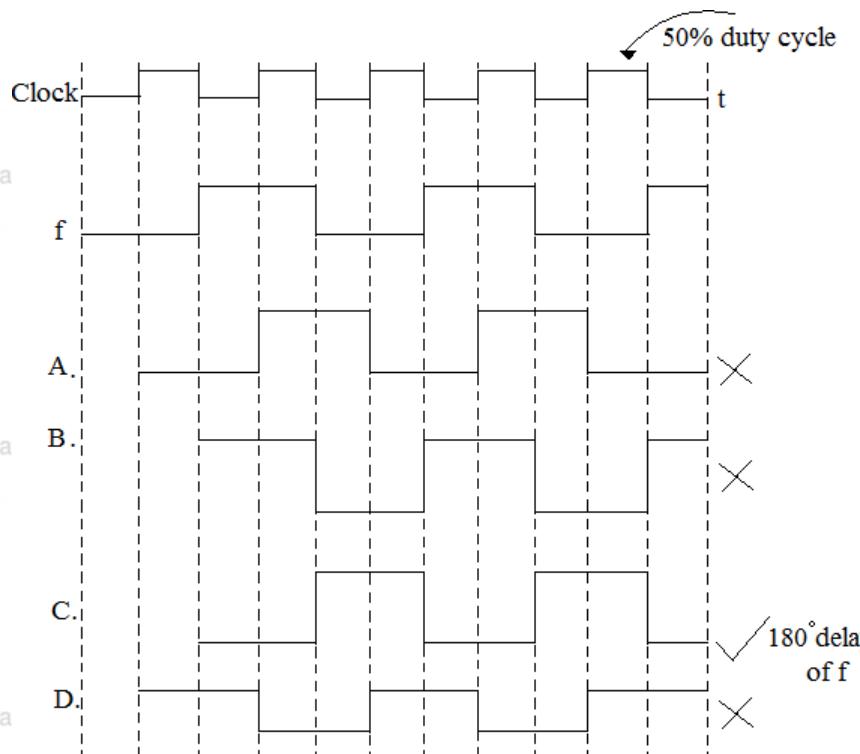
-- Arjun Suresh (332k points)

#### 4.8.24 Circuit Output: GATE CSE 2006 | Question: 8 top

<https://gateoverflow.in/887>



Ans- C.



42 votes

-- Aaditya Pundir (361 points)

B and D are inverting f and hence cannot be the answer.

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In A, the output is activated by CLK on the final D flip flop. So, the output will have the same phase as f.

In C, the output is activated by CLK', and since CLK is having 50% duty cycle, this should mean the output will now have a

phase difference of 180 degrees.

11 votes

-- Arjun Suresh (332k points)

4.8.25 Circuit Output: GATE CSE 2007 | Question: 36 [top](#)



- ✓ Whenever  $A_4A_3A_2A_1 = 0101$ , clear line will be enabled as  $A_3$  and  $A_1$  are set.

Given table says that whenever clear control signal is set, it clears to 0000, before the current clock cycle completes.

So, 5 is cleared to 0 in the same clock cycle and counter sequence is 0, 1, 2, 3, 4

Hence, option C .

40 votes

-- pramod (2.8k points)

(C) is the correct answer!

Remark :

1. If  $clear = 1$ , counter will be reset to 0000 without any delay, and counter doesn't count 5 .
2. If  $load = 1$ , counter will be loaded with the input 0011, but note that counter counts 5 in this case unlike clear input.
3. Counter counts from 0 to 4.
4. Clear and Load are **direct inputs**, it means they can be applied to the counter without using any pulse.

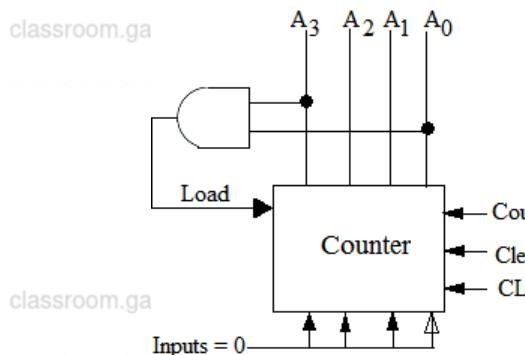


Fig a : Using the load input

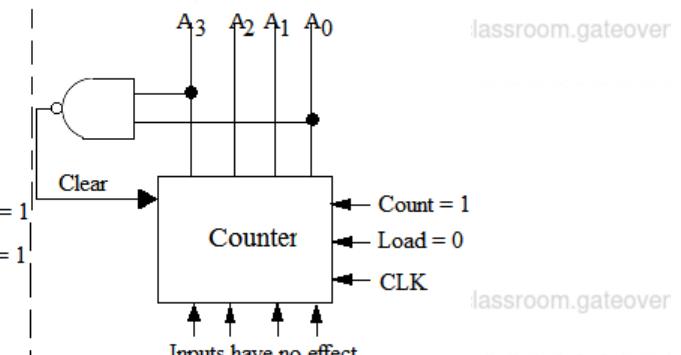


Fig b: Using the clear input

Two ways to achieve a BCD counter with parallel load

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When the output reaches the count of 1001, both  $A_0$  and  $A_3$  become 1, making the output of the AND gate equal to 1. This condition activates the Load input; therefore, on the next clock edge the register does not count, but is loaded from its four inputs . Since all four inputs are connected to logic 0, an all-0's value is loaded into the register following the count of 1001. Thus, the circuit goes through the count from 0000 through 1001 and back to 0000, as is required in a BCD counter.

In Fig (b), the NAND gate detects the count of 1010, but as soon as this count occurs, the register is cleared. The count 1010 has no chance of staying on for any appreciable time, because the register goes immediately to 0

1. If  $clear = 1$ , then clear the counter.
2. If  $clear = 0$ ,  $load = 0$ ,  $count = 1$ , counter counts.
3.  $load = 1$ , loads the input to the counter.

If  $load = 1$ , then counter will be loaded with  $i/p = 0011$

to the given counter,  $count = 1$   $load = 0$   $clock = \uparrow$

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Counter counts:  $0 \rightarrow 1 \rightarrow 3 \rightarrow 4$

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On  $i/p$ ,  $clear = 1$ , & counter reset to 0

**Note:** If o/p of *AND* gate is led to *load*, then counter will be loaded with 0011.

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29 votes

-- Manu Thakur (34k points)

4.8.26 Circuit Output: GATE CSE 2010 | Question: 31 top 5

https://gateoverflow.in/2205



✓ Level 1:

$$\overline{(P+Q)(Q+R)}(\overline{P+R})(\overline{Q+R})$$

Level 2:

$$\begin{aligned} \overline{(P+Q)+(\overline{Q+R})} &= (P+Q)(Q+R) = PQ + PR \\ \overline{(P+R)(Q+R)} &= (P+R)(Q+R) = PQ + R + QR + PR \end{aligned}$$

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Level 3:

$$PR + QR + PQ + Q + R = Q + R \therefore \text{Answer: Option A}$$

24 votes

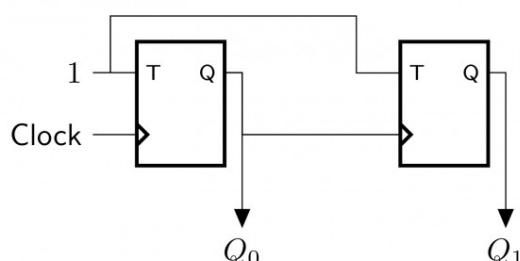
-- Sona Praneeth Akula (3.4k points)

4.8.27 Circuit Output: GATE CSE 2010 | Question: 32 top 5

https://gateoverflow.in/2206



✓ Option A.



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2<sup>nd</sup> flip-flop will be active only when 1<sup>st</sup> flip flop produces output 1. For clocks 2 and 4 old output is retained by Flip-Flop 2.

	T	Q <sub>0</sub>	T	Q <sub>1</sub>		Q <sub>1</sub>	Q <sub>0</sub>
		0		0		1	1
0		1	1	1		1	0
		1	0	1		0	1
1		Q <sub>n</sub>	1	1		0	0
		1	1	1		0	0
		1	0	1		0	0

For rows 2 and 4, Clk for T<sub>1</sub> is 0 and hence old o/p is retained

47 votes

-- Akhil Nadh PC (16.5k points)

4.8.28 Circuit Output: GATE CSE 2010 | Question: 9 top 5

https://gateoverflow.in/2182



$$\begin{aligned} f &= S'_0 S'_1 R + S'_0 S_1 R' + S_0 S'_1 R' + S_0 S_1 R \\ &= Q' P' R + Q' P R' + Q P' R' + Q P R \\ &= Q'(P \oplus R) + Q(P \oplus R)' \\ &= Q \oplus P \oplus R = P \oplus Q \oplus R \end{aligned}$$

Doing truth value substitution,

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P	Q	R	f	$P \oplus Q \oplus R$
0	0	0	0	0
0	0	g1eo1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

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Correct Answer: B

32 votes

-- Arjun Suresh (332k points)

**4.8.29 Circuit Output: GATE CSE 2011 | Question: 50**<https://gateoverflow.in/2157>

✓ Answer - D

As in D-flip-flop , next output is  $Q^+ = D$ 

- $P_{i+1} = R_i$
- $Q_{i+1} = (P_i + R_i)'$
- $R_{i+1} = R'_i Q_i$

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CLOCK	Inputs			Outputs		
	$D_1 = R$	$D_2 = \overline{(P + R)}$	$D_3 = Q \bar{R}$	P	Q	R
1	0	1	0	0	1	0
2	0	1	1	0	1	1
3	1	0	0	1	0	0
4	0	0	0	0	0	0
5	0	1	0	0	1	0

So, total number of distinct outputs = 4.

28 votes

-- Ankit Rokde (6.9k points)

**4.8.30 Circuit Output: GATE CSE 2011 | Question: 51**<https://gateoverflow.in/43318>✓ Characteristic equation of D FF is ,  $Q(t+1) = D$ So,  $P^+ = R$ ,  $Q^+ = \overline{P + R}$ , and  $R^+ = Q \cdot R'$ 

Sequence of states will be as:

Clock Pulse	PQR
Initially	000
1	010
2	011
3	100
4	000

4 is the number of distinct states.

Correct Answer: B

1 27 votes

-- Praveen Saini (41.9k points)

4.8.31 Circuit Output: GATE CSE 2014 Set 3 | Question: 45 [top](#)

<https://gateoverflow.in/2079>



Initial State			Input						Next State		
Q2	Q1	Q0	J2	K2	J1	K1	J0	K0	Q2'	Q1'	Q0'
0	0	0	1	0	0	1	0	1	1	0	0
1	0	0	1	0	1	0	0	1	1	1	0
1	1	0	0	0	1	0	1	1	1	1	1

Option C

1 39 votes

-- Gate\_15\_isHere (459 points)

4.8.32 Circuit Output: GATE IT 2005 | Question: 10 [top](#)

<https://gateoverflow.in/3755>



- ✓ If we look carefully, bulb will be ON when both switches  $S1$  and  $S2$  are in the same state, either off or on.

$S1$	$S2$	Bulb
0	0	On
0	1	Off
1	0	Off
1	1	On

This is Ex-NOR operation, hence (C) is the correct option.

1 53 votes

-- Manu Thakur (34k points)

4.8.33 Circuit Output: GATE IT 2005 | Question: 43 [top](#)

<https://gateoverflow.in/3804>



	A	B	C	Q <sub>1</sub>	Q <sub>2</sub>	Z	Comment
After 1 <sup>st</sup> Cycle	X	X	X	X	X	X	
After 2 <sup>nd</sup> Cycle	0	0	X	0	X	X	$Q_1$ is 0 making A and B 0
After 3 <sup>rd</sup> Cycle	X	X	1	1	1	1	Z is 1 making $Q_1$ and $Q_2$ 1, Either A or B is 1. $Q_1'$ of previous cycle is 1.

The filling is done in reverse order. Here, none of the options match. So, something wrong somewhere.

1 41 votes

-- Arjun Suresh (332k points)

4.8.34 Circuit Output: GATE IT 2006 | Question: 36 [top](#)

<https://gateoverflow.in/3575>



- ✓ Given expression:

$$xP + \bar{x}Q = f$$

$$\text{Or, } x(y op_1 z) + \bar{x}(y op_2 z) = f \rightarrow (1)$$

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X	Y	Z	Output(f)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

x\yz	00	01	11	10
0	...	...	1	...
1	...	1	1	1

$$f \implies xz + xy + yz$$

$$\implies xz + xy + (x + \bar{x})yz$$

$$\implies xz + xy + xyz + \bar{xy}z$$

$$\implies x(z + y + yz) + \bar{x}yz$$

$$\implies x[z + y(1 + z)] + \bar{x}(y \bullet z)$$

$$\implies x(z + y) + \bar{x}(y \bullet z) \rightarrow (2)$$

Comparing (1) and (2) we get,

$$OP_1 = +(OR)$$

$$OP_2 = \bullet(AND)$$

Correct Answer: D

1 like 63 votes

-- Subhankar Das (357 points)

#### 4.8.35 Circuit Output: GATE IT 2007 | Question: 38 top 5

<https://gateoverflow.in/3471>



- ✓ The final answer will come as:

$$a' + c' + d' + a'c + ab + bc$$

$$= a'(c + 1) + c' + d' + ab + bc$$

$$= a' + c' + d' + ab + bc$$

$$= (a' + a)(a' + b) + (c' + c)(c' + b) + d'$$

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$$= a' + b + c' + b + d'$$

$$= a' + b + c' + d'$$

Option is C.

1 like 29 votes

-- Manali (2.1k points)

#### 4.8.36 Circuit Output: GATE IT 2007 | Question: 40 top 5

<https://gateoverflow.in/3473>



- ✓ Answer: (A)

The four bit register contains: 1011, 1101, 0110, 1011, 1101, **0110** after each shift.

1 like 29 votes

-- Rajarshi Sarkar (27.9k points)



- ✓ To detect the fault, we should get an unexpected output. The final gate here is a NOR gate which produces output 0 if either of its input is 1 and else 1. i.e., the output will be 0 for inputs (0, 1), (1, 0) and (1, 1) and output will be 1 for (0, 0).

By grounding  $T$  is at 0. So, we can ignore the inputs (1, 0) and (0, 0) to the final NOR gate as they won't be detecting faults. Now, expected (1, 1) input will become (1, 0) due to grounding of  $T$  but produces same output 0 as for (1, 1). Hence this also cannot detect the defect. So, to detect the defect, the input to the final gate must be (0, 1) which is expected to produce a 0 but will produce a 1 due to grounding of  $T$ .

Now, for (0, 1) input for the final gate, we must have,

$$X_3 = X_4 = 1$$

But if  $X_4 = 1$ , the OR gate makes 1 output and we won't get (0, 1) input for the final gate. This means, no input sequence can detect the fault of the circuit.

Alternatively, we can write equation for the circuit as

$$((x_1 \cdot x_2 \cdot x_3)' + x_4)' = ((x_1 \cdot x_2 \cdot x_3)' + x_4)' \cdot (x_3 \cdot x_4)' = x_1 \cdot x_2 \cdot x_3 \cdot x_4' \cdot (x_3' + x_4') = x_1 \cdot x_2 \cdot x_3 \cdot x_4'$$

For the faulty circuit output will be

$$((x_1 \cdot x_2 \cdot x_3)' + x_4)' = x_1 \cdot x_2 \cdot x_3 \cdot x_4'$$

So, there is no effect of  $T$  being grounded here. Answer is D option.

69 votes

-- Arjun Suresh (332k points)



- ✓ Answer: B

$$F = \overline{(\bar{x}\bar{z} + xz)} = x\bar{z} + \bar{x}z$$

35 votes

-- Rajarshi Sarkar (27.9k points)



Which of the following is TRUE about formulae in Conjunctive Normal Form?

- For any formula, there is a truth assignment for which at least half the clauses evaluate to true.
- For any formula, there is a truth assignment for which all the clauses evaluate to true.
- There is a formula such that for each truth assignment, at most one-fourth of the clauses evaluate to true.
- None of the above.

[gate2007-cse](#) [digital-logic](#) [normal](#) [conjunctive-normal-form](#)

Answer

#### Answers: Conjunctive Normal Form



- ✓ Answer is **option A.**

**To Prove:** For any formula, there is a truth assignment for which at least half the clauses evaluate to true

**Proof:**

Consider an arbitrary truth assignment. For each of its clause  $i$ , introduce a random variable.

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$$X_i = \begin{cases} 1 & \text{if clause } i \text{ is satisfied;} \\ 0 & \text{otherwise.} \end{cases}$$

[classroom.gateoverflow.in](#)

Then,  $X = \sum_i X_i$  is the number of satisfied clauses.

Given any clause  $c$ , it is unsatisfied only if all of its  $k$  constituent literals evaluate to false; as they are joined by OR operator coz the formula is in CNF.

Now, because each literal within a clause has a  $\frac{1}{2}$  chance of evaluating to true independently of any of the truth value of any of the other literals, the probability that they are all false is  $(\frac{1}{2})^k$ .

Thus, the probability that  $c$  is satisfied(true) is  $1 - \frac{1}{2^k}$

$$\text{So, } E(X_i) = 1 \times \left(1 - \frac{1}{2^k}\right) = 1 - \frac{1}{2^k}$$

This means that  $E(X_i) \geq \frac{1}{2}$

(try putting arbitrary valid values of  $k$  to see that)

Summation on both sides to get  $E(X)$ ,

Therefore, we have  $E(X) = \sum_i E(X_i) \geq \frac{m}{2}$ ; where  $m$  is the number of clauses.  
 $E(X)$  represents expected number of satisfied(to true) clauses.

So, there must exist an assignment that satisfies(to true) at least half of the clauses.

Upvotes: 52

-- Amar Vashishth (25.2k points)

#### 4.10

#### Decoder (2)

top

##### 4.10.1 Decoder: GATE CSE 2007 | Question: 8, ISRO2011-31

<https://gateoverflow.in/1206>



How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?

- A. 7
- B. 8
- C. 9
- D. 10

gate2007-cse digital-logic normal isro2011 decoder

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Answer

##### 4.10.2 Decoder: GATE CSE 2020 | Question: 20

<https://gateoverflow.in/333211>



If there are  $m$  input lines and  $n$  output lines for a decoder that is used to uniquely address a byte addressable 1 KB RAM, then the minimum value of  $m + n$  is \_\_\_\_\_.

gate2020-cse numerical-answers digital-logic decoder

Answer

#### Answers: Decoder

##### 4.10.1 Decoder: GATE CSE 2007 | Question: 8, ISRO2011-31

<https://gateoverflow.in/1206>



✓ Answer is C:

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To get 6 : 64 we need 64 o/p

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We have 3 : 8 decode with 8 o/p. So, we need  $64/8 = 8$  decoders.

Now, to select any of this 8 decoder we need one more decoder.

Total =  $8 + 1 = 9$  decoders

Upvotes: 45

-- jayendra (6.7k points)

##### 4.10.2 Decoder: GATE CSE 2020 | Question: 20

<https://gateoverflow.in/333211>



- Given that we need to address every byte of a 1 KB RAM. Therefore 1K addresses are needed.

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By using decoder, output lines should be  $n = \log_2 1024 = 10$ . This means we should have number of input lines,  $m = \log_2 1024 = 10$ .

Thus,  $m + n = 10 + 1024 = 1034$ .

12 votes

-- Shaik Masthan (50.4k points)

4.11

Digital Circuits (7) top

4.11.1 Digital Circuits: GATE CSE 1992 | Question: 02-II top



All digital circuits can be realized using only

- A. Ex-OR gates
- B. Multiplexers
- C. Half adders
- D. OR gates

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gate1992 normal digital-logic digital-circuits multiple-selects

Answer ↗

4.11.2 Digital Circuits: GATE CSE 1996 | Question: 5 top



A logic network has two data inputs  $A$  and  $B$ , and two control inputs  $C_0$  and  $C_1$ . It implements the function  $F$  according to the following table.

$C_1$	$C_0$	$F$
0	0	$A + B$
0	1	$A + B$
1	0	$A \oplus B$

Implement the circuit using one 4 to 1 Multiplexer, one 2–input Exclusive OR gate, one 2–input AND gate, one 2–input OR gate and one Inverter.

gate1996 digital-logic normal descriptive

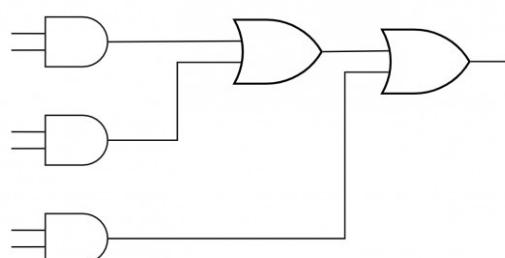
Answer ↗

4.11.3 Digital Circuits: GATE CSE 2002 | Question: 7 top



- A. Express the function  $f(x, y, z) = xy' + yz'$  with only one complement operation and one or more AND/OR operations. Draw the logic circuit implementing the expression obtained, using a single NOT gate and one or more AND/OR gates.
- B. Transform the following logic circuit (without expressing its switching function) into an equivalent logic circuit that employs only 6 NAND gates each with 2-inputs.

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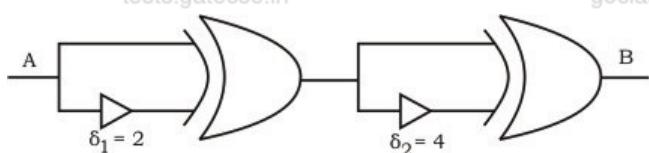
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gate2002-cse digital-logic normal descriptive digital-circuits

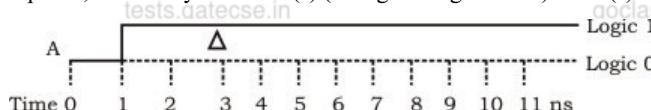
Answer ↗



Consider the following circuit composed of XOR gates and non-inverting buffers.



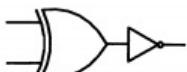
The non-inverting buffers have delays  $\delta_1 = 2\text{ns}$  and  $\delta_2 = 4\text{ns}$  as shown in the figure. Both XOR gates and all wires have zero delays. Assume that all gate inputs, outputs, and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A, how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns?

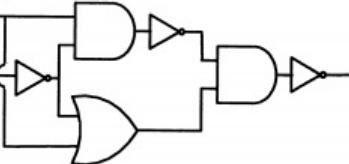


- A. 1
- B. 2
- C. 3
- D. 4



Which one of the following circuits is NOT equivalent to a 2-input XNOR (exclusive NOR) gate?



- A. 
- B. 
- C. 
- D. 



In the following truth table,  $V = 1$  if and only if the input is valid.

### Inputs

### Outputs

$D_0$	$D_1$	$D_2$	$D_3$
0	0	0	0
1	0	0	0
x	1	0	0
x	x	1	0
x	x	x	1

$X_0$	$X_1$	$V$
x	x	0
0	0	1
0	1	1
1	0	1
1	1	1

What function does the truth table represent?

- A. Priority encoder
- B. Decoder
- C. Multiplexer
- D. Demultiplexer

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Answer ↗

#### 4.11.7 Digital Circuits: GATE CSE 2014 Set 3 | Question: 8 top ↗

https://gateoverflow.in/2042



Consider the following combinational function block involving four Boolean variables  $x, y, a, b$  where  $x, a, b$  are inputs and  $y$  is the output.

```
f(x, a, b, y)
{
    if(x is 1) y = a;
    else y = b;
}
```

Which one of the following digital logic blocks is the most suitable for implementing this function?

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- A. Full adder
- B. Priority encoder
- C. Multiplexor
- D. Flip-flop

gate2014-cse-set3 | digital-logic | easy | digital-circuits

Answer ↗

#### Answers: Digital Circuits

#### 4.11.1 Digital Circuits: GATE CSE 1992 | Question: 02-ii top ↗

https://gateoverflow.in/556



✓ Answer: B, C gateoverflow.in

gateoverflow.in

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NOR gate, NAND gate, Multiplexers and Half adders can also be used to realise all digital circuits.

19 votes

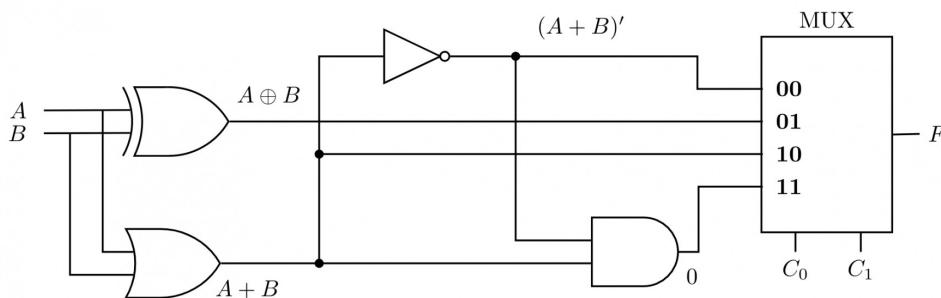
-- Rajarshi Sarkar (27.9k points)

#### 4.11.2 Digital Circuits: GATE CSE 1996 | Question: 5 top ↗

https://gateoverflow.in/2757



✓



This is the implementation asked in question

- $C_0 = 0, C_1 = 0$  line 00 will be selected and  $F$  will give  $(A \oplus B)'$
- $C_0 = 0, C_1 = 1$  line 01 will be selected and  $F$  will give  $(A \oplus B)$
- $C_0 = 1, C_1 = 0$  line 10 will be selected and  $F$  will give  $(A + B)$
- $C_0 = 1, C_1 = 1$  line 11 will be selected and  $F$  will give  $(A + B)' \cdot (A \oplus B) = 0$

26 votes

-- Praveen Saini (41.9k points)



✓  $f(x, y, z) = xy' + yz' = xy'z' + xy'z + x'y'z' + xyz'$

$$f(x, y, z) = \sum_m(2, 4, 5, 6)$$

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x\yz	00	01	11	10
0	0	0	0	1
1	1	1	0	1

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K-map  
gateoverflow.in

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By pairing of 1's, we get two pairs (2, 6), (4, 5) resulting in same expression  $F = xy' + yz'$

But by pairing of 0's, we get two pairs (0, 1), (2, 7), we get  $F' = yz + x'y'$

Take complement,  $F = \overline{(yz)} \cdot (x + y)$

so we can implement the function with 1 NOT, 1 OR and 2 AND gates.

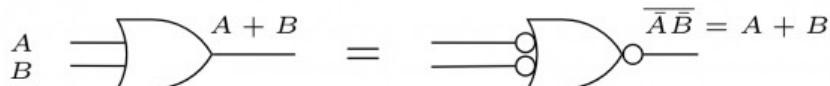
For the second part, we need to implement given circuit using NANDs only.

so best way is to replace OR with Invert NAND,  $A + B = (\bar{A}\bar{B})$

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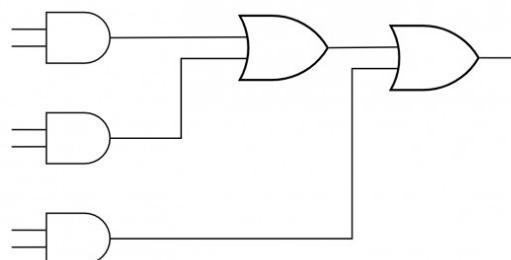
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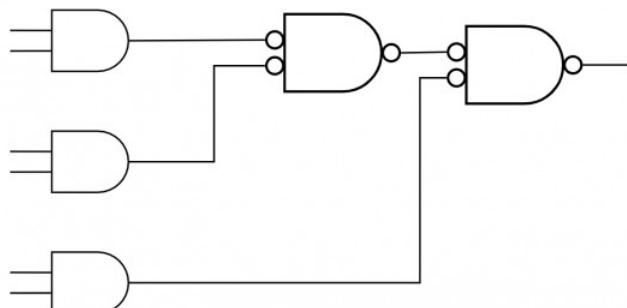
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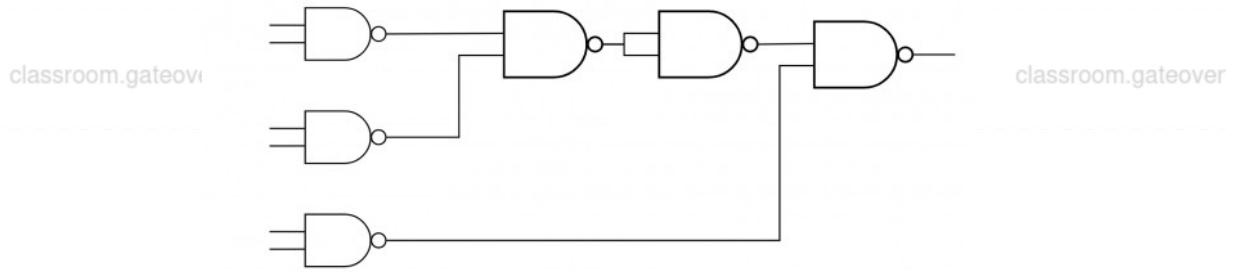
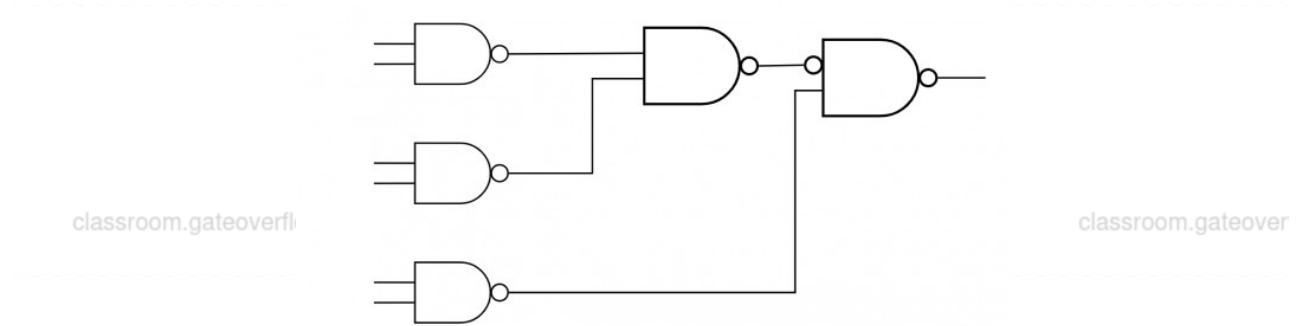
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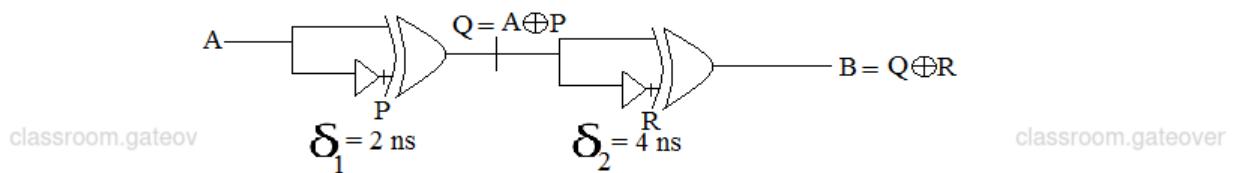


44 votes

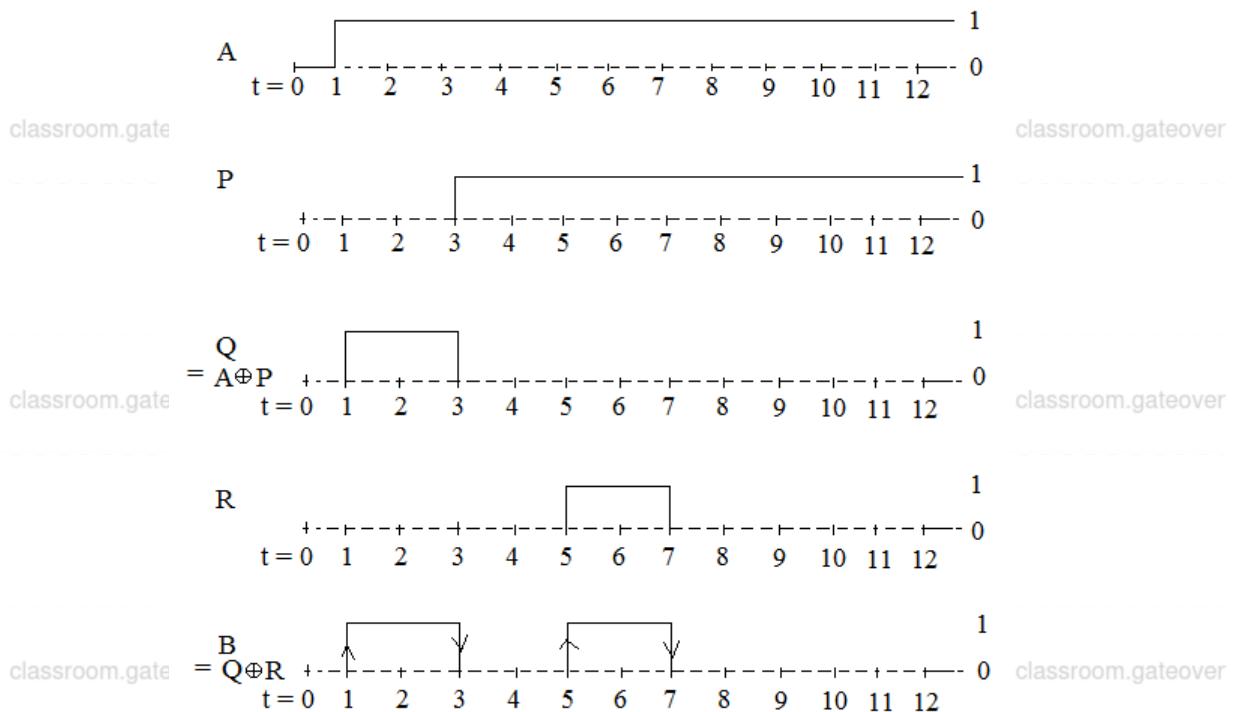
-- Praveen Saini (41.9k points)

#### 4.11.4 Digital Circuits: GATE CSE 2003 | Question: 47 top

<https://gateoverflow.in/29098>



Let us plot the logic states at the various points of interests in this circuit.



### Explanation :



Note that, is not an inverter but a buffer used for introducing delay.

∴ Output at 'P' and 'R' will be obtained at 2 ns and 4 ns respectively after the change in their inputs.

Hence, waveforms of 'P' and 'R' are shifted by 2 ns and 4 ns as compared to their inputs.

Also, note that 'Q' and 'B' are plotted using their corresponding input waveforms.

Finally, we can see that there are 4 changes in logic levels in the waveforms of 'B'.

Answer is : Option D

👍 108 votes

-- tvkkk (1.1k points)

#### 4.11.5 Digital Circuits: GATE CSE 2011 | Question: 13 top

► <https://gateoverflow.in/2115>



- A.  $(AB' + A'B)' = A \odot B$
- B.  $(A'(B')' + (A')'B')' = (A \oplus B)' = A \odot B$
- C.  $A'B' + (A')'B = A \odot B$
- D.  $((AB')'.(A + B'))' = (AB') + (A + B')' = AB' + A'B = A \oplus B$

So, Answer is (D)

👍 26 votes

-- srestha (85.2k points)

#### 4.11.6 Digital Circuits: GATE CSE 2013 | Question: 5 top

► <https://gateoverflow.in/1414>



Answer is A.

For  $2^n$  inputs we are having  $n$  outputs. Here  $n=2$ .

[http://en.wikipedia.org/wiki/Priority\\_encoder](http://en.wikipedia.org/wiki/Priority_encoder)

#### References



👍 27 votes

-- Sona Praneeth Akula (3.4k points)

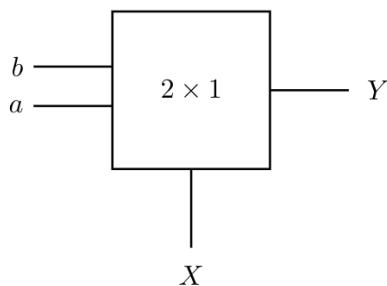
#### 4.11.7 Digital Circuits: GATE CSE 2014 Set 3 | Question: 8 top

► <https://gateoverflow.in/2042>



If  $X = 1$        $Y = a;$   
else  $(X = 0)$        $Y = b;$

Input :  $(a, b, X)$       Output :  $Y$



$$Y = \bar{X}b + Xa.$$

38 votes

-- Prateek kumar (6.7k points)

4.12

Digital Counter (10) top

## 4.12.1 Digital Counter: GATE CSE 1987 | Question: 10c top

<https://gateoverflow.in/82452>

Give a minimal DFA that performs as a  $\mod -3$ , 1's counter, i.e. outputs a 1 each time the number of 1's in the input sequence is a multiple of 3.

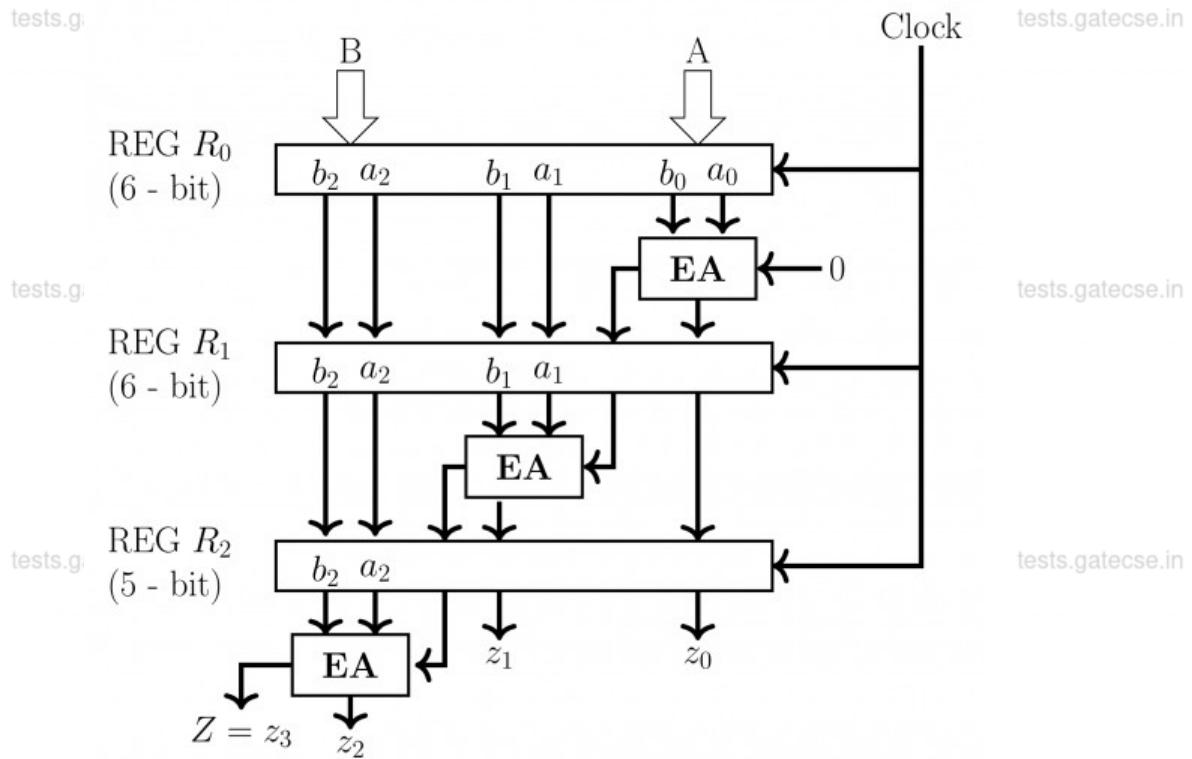
gate1987 digital-logic digital-counter descriptive

Answer

## 4.12.2 Digital Counter: GATE CSE 2002 | Question: 8 top

<https://gateoverflow.in/861>

Consider the following circuit.  $A = a_2a_1a_0$  and  $B = b_2b_1b_0$  are three bit binary numbers input to the circuit. The output is  $Z = z_3z_2z_1z_0$ .  $R_0$ ,  $R_1$  and  $R_2$  are registers with loading clock shown. The registers are loaded with their input data with the falling edge of a clock pulse (signal CLOCK shown) and appears as shown. The bits of input number A, B and the full adders are as shown in the circuit. Assume Clock period is greater than the settling time of all circuits.



- a. For 8 clock pulses on the CLOCK terminal and the inputs  $A, B$  as shown, obtain the output  $Z$  (sequence of 4-bit values of  $Z$ ). Assume initial contents of  $R_0, R_1$  and  $R_2$  as all zeros.

A	110	011	111	101	000	000	000	000
B	101	101	011	110	000	000	000	000
Clock No	1	2	3	4	5	6	7	8

- b. What does the circuit implement?

gate2002-cse digital-logic normal descriptive digital-counter

Answer



The minimum number of D flip-flops needed to design a mod-258 counter is

- A. 9
- B. 8
- C. 512
- D. 258

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[gate2011-cse](#) [digital-logic](#) [normal](#) [digital-counter](#)

Answer



Let  $k = 2^n$ . A circuit is built by giving the output of an  $n$ -bit binary counter as input to an  $n$ -to- $2^n$  bit decoder. This circuit is equivalent to a

- A.  $k$ -bit binary up counter.
- B.  $k$ -bit binary down counter.
- C.  $k$ -bit ring counter.
- D.  $k$ -bit Johnson counter.

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[gate2014-cse-set2](#) [digital-logic](#) [normal](#) [digital-counter](#)

Answer



Consider a 4-bit Johnson counter with an initial value of 0000. The counting sequence of this counter is

- A. 0, 1, 3, 7, 15, 14, 12, 8, 0
- B. 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
- C. 0, 2, 4, 6, 8, 10, 12, 14, 0
- D. 0, 8, 12, 14, 15, 7, 3, 1, 0

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[gate2015-cse-set1](#) [digital-logic](#) [digital-counter](#) [easy](#)

Answer



The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0, 0, 1, 1, 2, 2, 3, 3, 0, 0, ...) is \_\_\_\_\_.

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[gate2015-cse-set2](#) [digital-logic](#) [digital-counter](#) [normal](#) [numerical-answers](#)

Answer



We want to design a synchronous counter that counts the sequence 0 – 1 – 0 – 2 – 0 – 3 and then repeats. The minimum number of J-K flip-flops required to implement this counter is \_\_\_\_\_.

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[gate2016-cse-set1](#) [digital-logic](#) [digital-counter](#) [flip-flop](#) [normal](#) [numerical-answers](#)

Answer



The next state table of a 2-bit saturating up-counter is given below.

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$Q_1$	$Q_0$	$Q_1^+$	$Q_0^+$
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

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The counter is built as a synchronous sequential circuit using  $T$  flip-flops. The expressions for  $T_1$  and  $T_0$  are

- A.  $T_1 = Q_1 Q_0, T_0 = \bar{Q}_1 \bar{Q}_0$
- B.  $T_1 = \bar{Q}_1 Q_0, T_0 = \bar{Q}_1 + \bar{Q}_0$
- C.  $T_1 = Q_1 + Q_0, T_0 = \bar{Q}_1 \bar{Q}_0$
- D.  $T_1 = \bar{Q}_1 Q_0, T_0 = Q_1 + Q_0$

gate2017-cse-set2 digital-logic digital-counter

Answer ↗

## 4.12.9 Digital Counter: GATE IT 2005 | Question: 11 top ↗

https://gateoverflow.in/3756



How many pulses are needed to change the contents of a 8-bit up counter from 10101100 to 00100111 (rightmost bit is the LSB)?

- A. 134
- B. 133
- C. 124
- D. 123

gate2005-it digital-logic digital-counter normal

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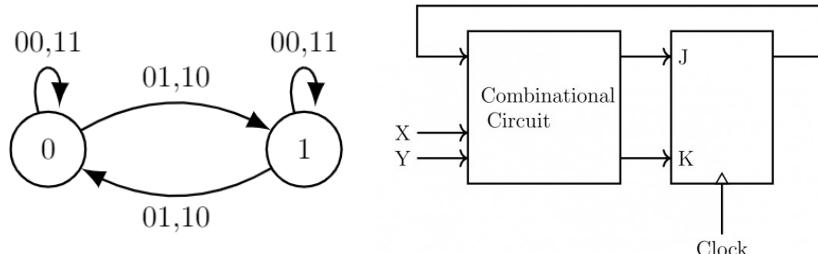
Answer ↗

## 4.12.10 Digital Counter: GATE IT 2008 | Question: 37 top ↗

https://gateoverflow.in/3347



Consider the following state diagram and its realization by a JK flip flop



The combinational circuit generates J and K in terms of x, y and Q.

The Boolean expressions for J and K are :

- A.  $\overline{x \oplus y}$  and  $\overline{x \oplus y}$
- B.  $x \oplus y$  and  $x \oplus y$
- C.  $x \oplus y$  and  $x \oplus y$
- D.  $x \oplus y$  and  $x \oplus y$

gate2008-it digital-logic boolean-algebra normal digital-counter

Answer ↗

## Answers: Digital Counter

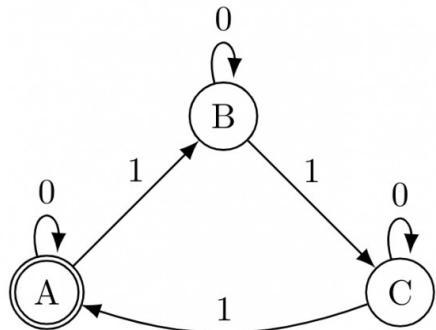
## 4.12.1 Digital Counter: GATE CSE 1987 | Question: 10c top ↗

https://gateoverflow.in/82452



- ✓ Since it is given that the minimal DFA outputs 1  $\implies$  we have to make a minimal DFA and then convert it into mealy/moore machine by associating output with each input or state.

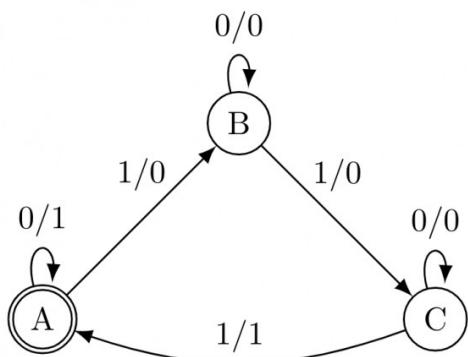
the minimal DFA will be as shown below :-



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I am associating output with each input i.e. creating a mealy machine. It will print 1 each time the number of 1's in the input sequence is a multiple of 3.



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7 votes

-- Satbir Singh (21k points)

#### 4.12.2 Digital Counter: GATE CSE 2002 | Question: 8 top 5

<https://gateoverflow.in/861>



✓ (A)

	output Z
Clock-1	0000
Clock-2	0000
Clock-3	1011
Clock-4	1000
Clock-5	1010
Clock-6	1011
Clock-7	0000
Clock-8	0000

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(B) The circuit is a 3 – bit ripple binary adder.

9 votes

-- Himanshu Agarwal (12.4k points)

#### 4.12.3 Digital Counter: GATE CSE 2011 | Question: 15 top 5

<https://gateoverflow.in/2117>



✓ Mod 258 counter has 258 states. We need to find no. of bits to represent 257 at max.  $2^n \geq 258 \implies n \geq 9$ .

Answer is A.

28 votes

-- Sona Praneeth Akula (3.4k points)



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- ✓ Binary counter of  $n$  bits can count up to  $2^n$  numbers. When this output from counter is fed as input (n bit) to decoder one out of  $2^n$  output lines will be activated. So, this arrangement of counter and decoder is behaving as  $2^n$  or  $k - bit$  ring counter.

Correct Answer: C

36 votes

-- Pooja Palod (24.1k points)



- ✓ Johnson Counter is a **switch-tail ring counter** in which a **circular shift register** with the complemented output of the last flip-flop connected to the input of the first flip-flop.

(D) is the correct answer!

25 votes

-- Manu Thakur (34k points)



- ✓ First, let's design a counter for 0, 1, 2, 3. It is a MOD - 4 counter. Hence, number of Flip Flops required will be two. Count sequence will be:

00 → 01 → 10 → 11

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Count sequence mentioned in question is:

00 → 00 → 01 → 01 → 10 → 10 → 11 → 11

Now, two flip flops won't suffice. Since we are confronted with repeated sequence, we may add another bit to the above sequence:

000 → 100 → 001 → 101 → 010 → 110 → 011 → 111

Now each and every count is unique, occurring only once. Meanwhile, our machine has been extended to a MOD - 8 counter. Hence, three Flip Flops suffice.

Just neglect the MSB flip flop output and take the o/p of other two only. So, we have :

0, 0, 1, 1, 2, 2, 3, 3, ...

So, correct answer: 3.

151 votes

-- Mithlesh Upadhyay (4.3k points)



- ✓ We need four JK flipflops.

0 → 1 → 0 → 2 → 0 → 3

0000 → 0001 → 0100 → 0010 → 1000 → 0011

There are 6 states and 3 of them correspond to same states.

To differentiate between 0, 1, 2, 3 we need 2 bits.

To differentiate between 3 0's we need another 2 bits.

So, total 4 - bits → 4FFs

**Edit:**

whether using extra combinational logic for output is allowed in a counter?

Page No. 10/11 <http://textofvideo.nptel.iitm.ac.in/117105080/lec23.pdf> or [archive](#)

Now, if you see the counters, now a counter we can define in this way the counter is a degenerate finite state machine, where the **state** is the **only** output. So, there is **no other primary output** from this machine, so the counter is defined like that.

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ALSO

Page No. 3 <http://textofvideo.nptel.iitm.ac.in/117106086/lec24.pdf> or [archive](#)

Counter you know what counter it is, that's what we want we count the output of counter what is the current count that is the output of a count so no external output. **The counter is a case of a state machine in which there are no external inputs, no external outputs.**

Page No. 10 <http://textofvideo.nptel.iitm.ac.in/117106086/lec24.pdf> or [archive](#)

always do that let us say 1 0 0 you want count twice you can put 1 0 0 to 1 0 0 but then when you draw the Karnaugh Map you don't know which 1 0 0 you are talking about so instead of doing that you can have an external input defined when x is equal to 0 it remains there so you can put x is equal to 0 and for all of those x is equal to 1. So from  $S_0$  to  $S_1$  it will remain, both 0 and 1 it will take here, from here it will take here only if x is equal to 1 and if x is equal to 0 it will remain here so external input can be used more elegantly for that design.

At 35:30 [www.youtube.com/watch?v=MiuMYEn3dp](http://www.youtube.com/watch?v=MiuMYEn3dp)

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Here In Counter, we cannot use external variable, that purpose will be served by FF's only  
We have four distinct states 0, 1, 2, 3 so, 2FF for them for 3 0's to distinguish we need 2 more FF's  
<http://www.youtube.com/watch?v=MiuMYEn3dp>

4FF required.

References



118 votes

-- Abhilash Panicker (7.6k points)

#### 4.12.8 Digital Counter: GATE CSE 2017 Set 2 | Question: 42 [top](#)

<https://gateoverflow.in/118557>



✓ Answer is **B**

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$Q_1$	$Q_0$	$Q_1^+$	$Q_0^+$	$T_1$	$T_2$
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	0	0

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By using above excitation table,

$$T_1 = Q_1'Q_0,$$

$$T_2 = (Q_1Q_0)' = Q_1' + Q_0'$$

23 votes

-- jatin saini (4.2k points)

#### 4.12.9 Digital Counter: GATE IT 2005 | Question: 11 [top](#)

<https://gateoverflow.in/3756>



✓ **D.123 Pulses.**

As in a  $2^8$  Counter, the range would be from 0 – 255. Hence to go from 10101100(172) to 00100111(39), the counter has to go initially from 172 to 255 and then from 0 to 39.

Hence to go from 172 to 255,  $255 - 172 = 83$  Clock pulses would be required. Then from 255 to 0, again 1 clock pulse would be required. Then, from 0 to 39, 39 clock pulses would be required. Hence in total  $83 + 1 + 39 = 123$  Clock pulses would be

required.

73 votes

-- Afaque Ahmad (727 points)

#### 4.12.10 Digital Counter: GATE IT 2008 | Question: 37 top

<https://gateoverflow.in/3347>



- From state diagram:

Q	X	Y	Q <sub>n+1</sub>	J	K
0	0	0	0	0	X
0	0	1	1	1	X
0	1	0	1	1	X
0	1	1	0	0	X
1	0	0	1	X	0
1	0	1	0	X	1
1	1	0	0	X	1
1	1	1	1	X	0

Excitation table of JK

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Q	Q <sub>n+1</sub>	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

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XY	Q			
	00	01	11	10
Q	1			1
0	X	X	X	X
1				

$$J = X'Y + XY' = X \oplus Y$$

Option D.

XY	Q			
	00	01	11	10
Q	X	X	X	X
0		1		
1				

$$K = X'Y + XY' = X \oplus Y$$

71 votes

-- Riya Roy(Arayana) (5.3k points)

#### 4.13

#### Dual Function (1) top

##### 4.13.1 Dual Function: GATE CSE 2014 Set 2 | Question: 6 top

<https://gateoverflow.in/1958>



The dual of a Boolean function  $F(x_1, x_2, \dots, x_n, +, \cdot, ', )$ , written as  $F^D$  is the same expression as that of  $F$  with  $+$  and  $\cdot$  swapped.  $F$  is said to be self-dual if  $F = F^D$ . The number of self-dual functions with  $n$  Boolean variables is

- A.  $2^n$
- B.  $2^{n-1}$
- C.  $2^{2^n}$
- D.  $2^{2^{n-1}}$

gate2014-cse-set2 digital-logic normal dual-function

Answer

Answers: Dual Function



- ✓ A function is self dual if it is equal to its dual (A dual function is obtained by interchanging . and +).

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For self-dual functions,

1. Number of min terms equals number of max terms
2. Function should not contain two complementary minterms - whose sum equals  $2^n - 1$ , where  $n$  is the number of variables.

	A	B	C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

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So, here  $(0, 7)(1, 6)(2, 5)(3, 4)$  are complementary terms so in self-dual we can select any one of them but not both.

Totally  $2 \times 2 \times 2 \times 2 = 2^4$  possibility because say from  $(0, 7)$  we can pick anyone in minterm but not both.

For example, let  $f = \sum(0, 6, 2, 3)$

**NOTE: here I have taken only one of the complementary term for min term from the sets.**

So, remaining numbers will go to MAXTERMS

For above example,  $2^4 = 16$  self dual functions are possible

So, if we have  $N$  variables, total Minterms possible is  $2^n$

Then half of them we selected so  $2^{n-1}$ .

Now we have 2 choices for every pair for being selected.

So total such choices =  $\underbrace{2 \times 2 \times 2 \times 2 \dots 2}_{2^{n-1} \text{ times}}$

$\therefore 2^{2^{n-1}}$  (option D)

1 like 64 votes

-- Kalpish Singhal (1.6k points)

## 4.14

Fixed Point Representation (2) [top](#)4.14.1 Fixed Point Representation: GATE CSE 2017 Set 1 | Question: 7 [top](#)

The  $n$ -bit fixed-point representation of an unsigned real number  $X$  uses  $f$  bits for the fraction part. Let  $i = n - f$ . The range of decimal values for  $X$  in this representation is

- A.  $2^{-f}$  to  $2^i$
- B.  $2^{-f}$  to  $(2^i - 2^{-f})$
- C. 0 to  $2^i$
- D. 0 to  $(2^i - 2^{-f})$

gate2017-cse-set1 digital-logic number-representation fixed-point-representation

Answer

4.14.2 Fixed Point Representation: GATE CSE 2018 | Question: 33 [top](#)

Consider the unsigned 8-bit fixed point binary number representation, below,

$b_7 \ b_6 \ b_5 \ b_4 \ b_3 \cdot b_2 \ b_1 \ b_0$

where the position of the primary point is between  $b_3$  and  $b_2$ . Assume  $b_7$  is the most significant bit. Some of the decimal numbers

listed below **cannot** be represented **exactly** in the above representation:  
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- i. 31.500
- ii. 0.875
- iii. 12.100
- iv. 3.001

Which one of the following statements is true?

- A. None of *i*, *ii*, *iii*, *iv* can be exactly represented
- B. Only *ii* cannot be exactly represented
- C. Only *iii* and *iv* cannot be exactly represented
- D. Only *i* and *ii* cannot be exactly represented

gate2018-cse digital-logic number-representation fixed-point-representation normal

Answer ↗

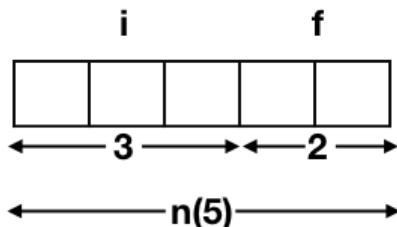
#### Answers: Fixed Point Representation

4.14.1 Fixed Point Representation: GATE CSE 2017 Set 1 | Question: 7 [top ↵](#)

↗ <https://gateoverflow.in/118287>

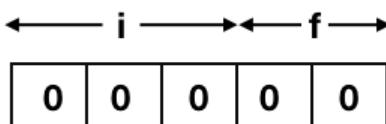


Unsigned real number  $x$ .



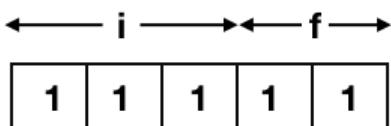
Let  $n = 5$ ,  $f = 2$ ,  $i = 5 - 2 = 3$ .

1. Minimum value of  $x$ :



Value on decimal = 0.

2. Maximum value of  $x$ :



Value on decimal =  $2^3 - 2^{-2} = 8 - 0.25 = 7.75$  (Or  $2^2 + 2^1 + 2^0 + 2^{-1} + 2^{-2} = 7.75$ )

So (D) is the answer.

👍 92 votes

-- 2018 (5.5k points)

4.14.2 Fixed Point Representation: GATE CSE 2018 | Question: 33 [top ↵](#)

↗ <https://gateoverflow.in/204107>



- ✓ 31.500 can be represented as 11111.100 in the above mentioned fixed form representation

0.875 can be represented as 00000.111.

We can't represent 3 and 4.

Hence, C is the correct answer.

19 votes

-- Prashant Kumar (1k points)

4.15

Flip Flop (6) [top](#)

4.15.1 Flip Flop: GATE CSE 2001 | Question: 11 [top](#)

<https://gateoverflow.in/752>



A sequential circuit takes an input stream of  $0's$  and  $1's$  and produces an output stream of  $0's$  and  $1's$ . Initially it replicates the input on its output until two consecutive  $0's$  are encountered on the input. From then onward, it produces an output stream, which is the bit-wise complement of input stream until it encounters two consecutive  $1's$ , whereupon the process repeats. An example input and output stream is shown below.

The input stream:	101100		01001011		011
The desired output:	101100		10110100		011

J-K master-slave flip-flops are to be used to design the circuit.

- Give the state transition diagram
- Give the minimized sum-of-product expression for J and K inputs of one of its state flip-flops

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[gate2001-cse](#) [digital-logic](#) [normal](#) [descriptive](#) [flip-flop](#)

Answer

4.15.2 Flip Flop: GATE CSE 2004 | Question: 18, ISRO2007-31 [top](#)

<https://gateoverflow.in/1015>



In an  $SR$  latch made by cross-coupling two NAND gates, if both  $S$  and  $R$  inputs are set to 0, then it will result in

- A.  $Q = 0, Q' = 1$
- B.  $Q = 1, Q' = 0$
- C.  $Q = 1, Q' = 1$
- D. Indeterminate states

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[gate2004-cse](#) [digital-logic](#) [easy](#) [isro2007](#) [flip-flop](#)

Answer

4.15.3 Flip Flop: GATE CSE 2015 Set 1 | Question: 37 [top](#)

<https://gateoverflow.in/8287>



A positive edge-triggered  $D$  flip-flop is connected to a positive edge-triggered  $JK$  flip-flop as follows. The  $Q$  output of the  $D$  flip-flop is connected to both the  $J$  and  $K$  inputs of the  $JK$  flip-flop, while the  $Q$  output of the  $JK$  flip-flop is connected to the input of the  $D$  flip-flop. Initially, the output of the  $D$  flip-flop is set to logic one and the output of the  $JK$  flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the  $Q$  output of the  $JK$  flip-flop when the flip-flops are connected to a free-running common clock? Assume that  $J = K = 1$  is the toggle mode and  $J = K = 0$  is the state holding mode of the  $JK$  flip-flops. Both the flip-flops have non-zero propagation delays.

- A. 0110110...
- B. 0100100...
- C. 011101110...
- D. 011001100...

<tests.gatecse.in>

[gate2015-cse-set1](#) [digital-logic](#) [flip-flop](#) [normal](#)

Answer

4.15.4 Flip Flop: GATE CSE 2017 Set 1 | Question: 33 [top](#)

<https://gateoverflow.in/118315>

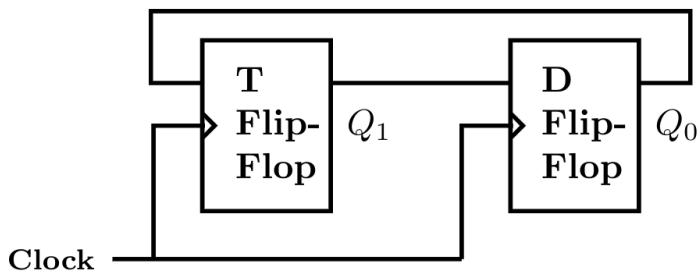


Consider a combination of  $T$  and  $D$  flip-flops connected as shown below. The output of the  $D$  flip-flop is connected to the input of the  $T$  flip-flop and the output of the  $T$  flip-flop is connected to the input of the  $D$  flip-flop.

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<goclasses.in>

<tests.gatecse.in>



tests.gatecse.in

Initially, both  $Q_0$  and  $Q_1$  are set to 1 (before the 1<sup>st</sup> clock cycle). The outputs

- A.  $Q_1Q_0$  after the 3<sup>rd</sup> cycle are 11 and after the 4<sup>th</sup> cycle are 00 respectively.
- B.  $Q_1Q_0$  after the 3<sup>rd</sup> cycle are 11 and after the 4<sup>th</sup> cycle are 01 respectively.
- C.  $Q_1Q_0$  after the 3<sup>rd</sup> cycle are 00 and after the 4<sup>th</sup> cycle are 11 respectively.
- D.  $Q_1Q_0$  after the 3<sup>rd</sup> cycle are 01 and after the 4<sup>th</sup> cycle are 01 respectively.

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gate2017-cse-set1 digital-logic flip-flop normal

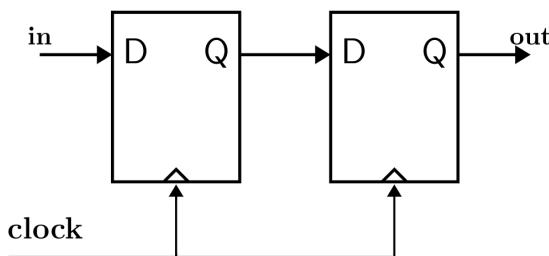
Answer ↗

4.15.5 Flip Flop: GATE CSE 2018 | Question: 22 top ↗

↗ <https://gateoverflow.in/204096>



Consider the sequential circuit shown in the figure, where both flip-flops used are positive edge-triggered D flip-flops.



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The number of states in the state transition diagram of this circuit that have a transition back to the same state on some value of "in" is \_\_\_\_\_

gate2018-cse digital-logic flip-flop numerical-answers normal

Answer ↗

4.15.6 Flip Flop: GATE IT 2007 | Question: 7 top ↗

↗ <https://gateoverflow.in/3440>



Which of the following input sequences for a cross-coupled  $R - S$  flip-flop realized with two  $NAND$  gates may lead to an oscillation?

- A. 11, 00
- B. 01, 10
- C. 10, 01
- D. 00, 11

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gate2007-it digital-logic normal flip-flop

Answer ↗

Answers: Flip Flop

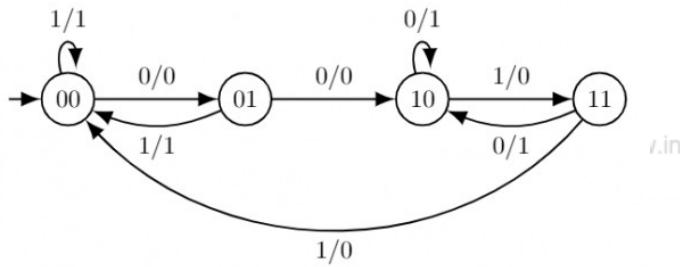
4.15.1 Flip Flop: GATE CSE 2001 | Question: 11 top ↗

↗ <https://gateoverflow.in/752>



- ✓ We can design a Mealy Machine as per the requirement given in the question.

From which we will get state table, and we can design sequential circuit using any Flip-flop from the state table (with the help of excitation table).



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As we get 4 states (renaming state component to binary states), we need two FFs to implement it.

Let  $A$  and  $B$  be present states,  $x$  be the input and  $y$  be the output.

Present State	Input	Next State	Output	FF inputs	FF inputs		
$AB$	$X$	$A'B'$	$Y$	$J_A$	$K_A$	$J_B$	$K_B$
00	0	01	0	0	$X$	1	$X$
00	1	00	1	0	$X$	0	$X$
01	0	10	0	1	$X$	$X$	1
01	1	00	1	0	$X$	$X$	1
10	0	10	1	$X$	0	0	$X$
10	1	11	0	$X$	0	1	$X$
11	0	10	1	$X$	0	$X$	1
11	1	00	0	$X$	1	$X$	1

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$Q_t$	$Q_{t+1}$	$J$	$K$
0	0	0	$X$
0	1	1	$X$
1	0	$X$	1
1	1	$X$	0

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$A$	$BX$	00	01	11	10
0					1
1	X	X	X	X	

$$J_A = BX'$$

$A$	$BX$	00	01	11	10
0		X	X	X	X
1				1	

$$K_A = BX$$

$A$	$BX$	00	01	11	10
0	1			X	
1		1	X		X

$$J_B = A'X' + AX$$

$$J_B = A \odot X$$

$A$	$BX$	00	01	11	10
0	X	X		1	1
1	X	X	1	1	1

$$K_B = 1$$

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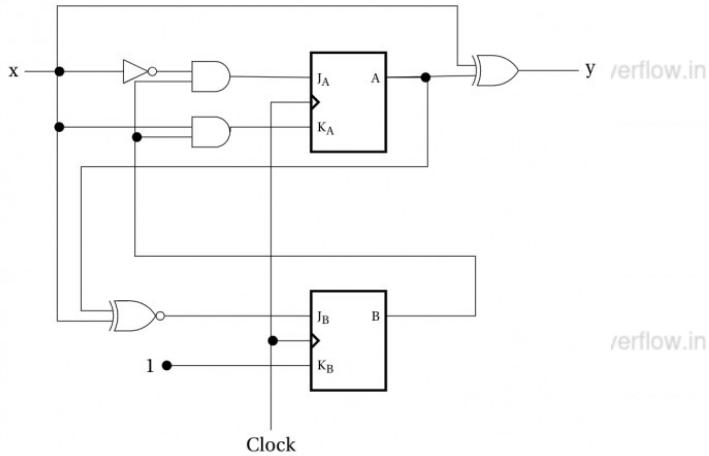
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$A$	$BX$	00	01	11	10
0			1	1	
1		1			1

$Y = A'X + AX'$   
 $Y = A \oplus X$

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29 votes

-- Praveen Saini (41.9k points)

## 4.15.2 Flip Flop: GATE CSE 2004 | Question: 18, ISRO2007-31

<https://gateoverflow.in/1015>

- ✓ Answer should be C. The reasoning is as follows:

When both  $R$  and  $S$  are set as 0, we will get both  $Q$  and  $Q'$  as 1 (these must be ideally mutually complementary). This output will be permanent and is not dependent on any sequence of events but just the input values (so no race condition). But after this state if we enter both  $R$  and  $S$  as 1, the output will be indeterminate depending on which NAND gate processes first (either  $Q$  or  $Q'$  will become 0 but we can't determine which (race condition) and it will lead to an indeterminate state.

PS:  $R = 0, S = 0$  in an SR latch made by cross coupling 2 NAND gates will lead to a forbidden state. Forbidden state means, this state is invalid and must not be entered. This is different from an indeterminate state which means a state where we are not sure of the output. Again this is different from a toggling state where the output changes continuously.

57 votes

-- Preetek Arora (285 points)

## 4.15.3 Flip Flop: GATE CSE 2015 Set 1 | Question: 37

<https://gateoverflow.in/8287>

$Q_{prev}$	D	$Q(JK)$	Explanation
-	1	0	Now, the D output is 1, meaning J and K = 1; for next cycle
0	0	1	$J = K = 1$ (D output from prev state), so output toggles from 0 to 1
1	1	1	$J = K = 0$ , so output remains 1
1	1	0	$J = K = 0$ , so output remains 1
0	0	1	$J = K = 1$ , so output toggles from 0 to 1
1	1	1	$J = K = 0$ , so output remains 1

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D flipflop output will be same as its input and JK flipflop output toggles when 1 is given to both J and K inputs.  
i.e.,  $Q = D_{prev}(Q_{prev}')$  +  $(D_{prev})Q_{prev}$

Correct Answer: A

35 votes

-- Arjun Suresh (332k points)



- ✓ Since it is synchronous so, after every clock cycle **T will toggle if input is 1** and will be in **Hold State if input is 0**. D flip-flop's output always follows input

- After 1 clock cycles :  $Q_1=0$  (Toggle)  $Q_0=1$
- After 2 clock cycles :  $Q_1=1$  (Toggle)  $Q_0=0$
- After 3 clock cycles:  $Q_1=1$  (Hold)  $Q_0=1$
- After 4 clock cycles:  $Q_1=0$  (Toggle)  $Q_0=1$

Hence option **(B)** is correct

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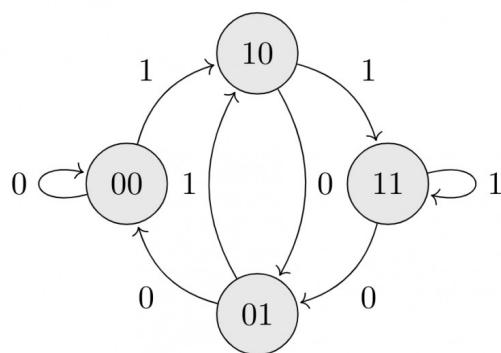
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-- sriv\_shubham (2.8k points)



- ✓ Answer Is 2.



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Here **00 on input 0** and **11 on input 1** have transition back to itself. So, answer is **2**.



-- Suraj Sajeev (311 points)



- ✓ For a cross-coupled  $R - S$  flip flop with two NAND gates 11 is no change and 00 is forbidden. 00 is forbidden (not allowed but not indeterminate) because in this state both  $Q$  and  $Q'$  equals 1. Moreover, in this state if inputs are changed to 11, next state is indeterminate (meaning we cannot determine the output)-  $Q$  can be 0 and  $Q'$  can be 1 or  $Q = 1$  and  $Q' = 0$ . There is also a chance that outputs can oscillate here when the following happens:

1. Inputs are set to 11
2. When both inputs of NAND gates are 1 output is 0
3. Suppose NAND gate 1 becomes 0 first.
4. This 0 goes as input to NAND gate 2.
5. By this time NAND gate 2 produces its own output as 0.
6. Now, this 0 goes as input to NAND gate 1 which makes its output 1.
7. The 0 input to NAND gate 2 (from step 4) now makes its output 1.
8. Whole cycle can repeat and output toggles between 1 and 0.

This is just a possibility and that is why question says "may oscillate."

The input sequence 00,11 (Option D) may oscillate.

[https://en.wikipedia.org/wiki/Flip-flop\\_\(electronics\)#SR\\_NAND\\_latch](https://en.wikipedia.org/wiki/Flip-flop_(electronics)#SR_NAND_latch)

References



29 votes

-- Arjun Suresh (332k points)

4.16

Floating Point Representation (9) [top](#)

4.16.1 Floating Point Representation: GATE CSE 1987 | Question: 1-vii [top](#)

<https://gateoverflow.in/80201>



The exponent of a floating-point number is represented in excess-N code so that:

- A. The dynamic range is large.
- B. The precision is high.
- C. The smallest number is represented by all zeros.
- D. Overflow is avoided.

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[gate1987](#) [digital-logic](#) [number-representation](#) [floating-point-representation](#)

Answer

4.16.2 Floating Point Representation: GATE CSE 1989 | Question: 1-vi [top](#)

<https://gateoverflow.in/87053>



Consider an excess -50 representation for floating point numbers with 4 BCD digit mantissa and 2 BCD digit exponent in normalised form. The minimum and maximum positive numbers that can be represented are \_\_\_\_\_ and \_\_\_\_\_ respectively.

[descriptive](#) [gate1989](#) [digital-logic](#) [number-representation](#) [floating-point-representation](#)

Answer

4.16.3 Floating Point Representation: GATE CSE 1990 | Question: 1-iv-a [top](#)

<https://gateoverflow.in/83830>



A 32-bit floating-point number is represented by a 7-bit signed exponent, and a 24-bit fractional mantissa. The base of the scale factor is 16,

The range of the exponent is \_\_\_\_\_

[gate1990](#) [digital-logic](#) [number-representation](#) [floating-point-representation](#) [fill-in-the-blanks](#)

Answer

4.16.4 Floating Point Representation: GATE CSE 1990 | Question: 1-iv-b [top](#)

<https://gateoverflow.in/203832>



A 32-bit floating-point number is represented by a 7-bit signed exponent, and a 24-bit fractional mantissa. The base of the scale factor is 16,

The range of the exponent is \_\_\_\_\_, if the scale factor is represented in excess-64 format.

[gate1990](#) [digital-logic](#) [number-representation](#) [floating-point-representation](#) [fill-in-the-blanks](#)

Answer

4.16.5 Floating Point Representation: GATE CSE 1997 | Question: 72 [top](#)

<https://gateoverflow.in/19702>



Following floating point number format is given

$f$  is a fraction represented by a 6-bit mantissa (includes sign bit) in sign magnitude form,  $e$  is a 4-bit exponent (includes sign bit) in sign magnitude form and  $n = (f, e) = f \cdot 2^e$  is a floating point number. Let  $A = 54.75$  in decimal and  $B = 9.75$  in decimal

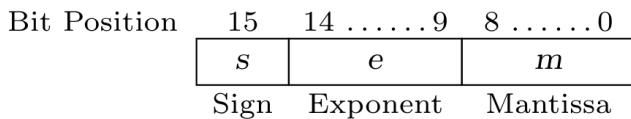
- a. Represent  $A$  and  $B$  as floating point numbers in the above format.
- b. Show the steps involved in floating point addition of  $A$  and  $B$ .
- c. What is the percentage error (up to one position beyond decimal point) in the addition operation in (b)?

[gate1997](#) [digital-logic](#) [floating-point-representation](#) [normal](#) [descriptive](#)

Answer



The following is a scheme for floating point number representation using 16 bits.



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Let  $s$ ,  $e$ , and  $m$  be the numbers represented in binary in the sign, exponent, and mantissa fields respectively. Then the floating point number represented is:

$$\begin{cases} (-1)^s (1 + m \times 2^{-9}) 2^{e-31}, & \text{if the exponent } \neq 111111 \\ 0, & \text{otherwise} \end{cases}$$

What is the maximum difference between two successive real numbers representable in this system?

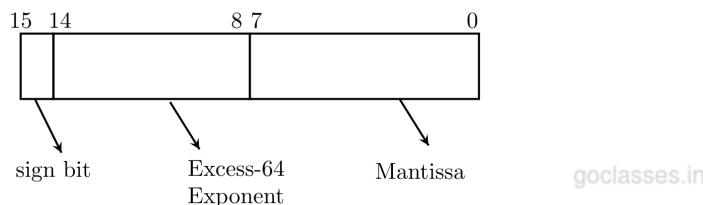
- A.  $2^{-40}$
- B.  $2^{-9}$
- C.  $2^{22}$
- D.  $2^{31}$

gate2003-cse digital-logic number-representation floating-point-representation normal

Answer



Consider the following floating-point format.



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Mantissa is a pure fraction in sign-magnitude form.

The decimal number  $0.239 \times 2^{13}$  has the following hexadecimal representation (without normalization and rounding off):

- A. 0D 24
- B. 0D 4D
- C. 4D 0D
- D. 4D 3D

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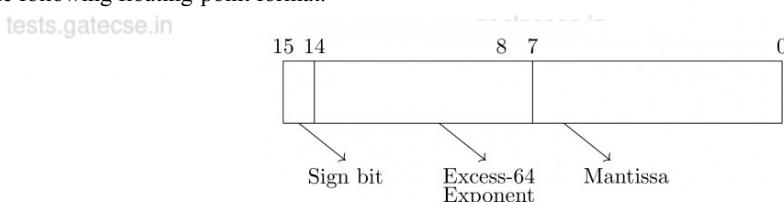
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gate2005-cse digital-logic number-representation floating-point-representation normal

Answer



Consider the following floating-point format.



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Mantissa is a pure fraction in sign-magnitude form.

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The normalized representation for the above format is specified as follows. The mantissa has an implicit 1 preceding the binary (radix) point. Assume that only 0's are padded in while shifting a field.

The normalized representation of the above number ( $0.239 \times 2^{13}$ ) is:

- A. 0A 20
- B. 11 34
- C. 49 D0
- D. 4A E8

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gate2005-cse digital-logic number-representation floating-point-representation normal

Answer 

#### 4.16.9 Floating Point Representation: GATE CSE 2020 | Question: 29 [top](#)

<https://gateoverflow.in/333202>



Consider three registers  $R1$ ,  $R2$ , and  $R3$  that store numbers in IEEE-754 single precision floating point format. Assume that  $R1$  and  $R2$  contain the values (in hexadecimal notation) 0x42200000 and 0xC1200000, respectively.

If  $R3 = \frac{R1}{R2}$ , what is the value stored in  $R3$ ?

- A. 0x40800000
- B. 0xC0800000
- C. 0x83400000
- D. 0xC8500000

gate2020-cse floating-point-representation digital-logic

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Answer 

#### Answers: Floating Point Representation

#### 4.16.1 Floating Point Representation: GATE CSE 1987 | Question: 1-vii [top](#)

<https://gateoverflow.in/80201>



✓ Answer : C) The smallest number is represented by all zeros.

In computer system, a floating-point number is represented as S E M, i.e. using Sign bit, Exponent bits and Mantissa bits.

The exponent can be a positive as well as a negative number. So to represent negative number we can use 1's complement or 2's complement. Better choice would be 2's complement.

If we use 2's complement system to represent exponent, then problem will arise while comparing 2 floating point numbers. For example, if exponent of the 2 numbers are negative then for comparing we will have to convert them into positive number.

So, to avoid this extra work, excess-N code is used so that all exponent can be represented in positive numbers, starting with 0.

 28 votes

-- Kantikumar (3.4k points)

#### 4.16.2 Floating Point Representation: GATE CSE 1989 | Question: 1-vi [top](#)

<https://gateoverflow.in/87053>



✓ In binary we have normalized number of the form  $(-1)^S \times 1.M \times 2^{E-Bias}$  where,

- $S$  : sign bit
- $M$  : Mantissa
- $E$  : Exponent

Similarly for for Binary Coded Decimal (BCD) numbers the normalized number representation will be  
 $: (-1)^S \times 1.M \times 10^{E-Bias}$

Here bias is given to be excess - 50 meaning that we need to subtract 50 from the base exponent field to get the actual exponent.

So, maximum mantissa value with 4 BCD digits = 9999

Maximum base exponent value with 2 BCD digits = 99

So, maximum actual exponent value possible with 2 BCD digits = 99 - Bias

$$= 99 - 50$$

$$= 49$$

So, the magnitude of the largest positive number =  $9.9999 \times 10^{49}$

Similarly,

To get a minimum positive number, we have to set mantissa = 0 and exponent field = 0

So, doing that we get exponent =  $0 - 50 = -50$

So, magnitude of minimum positive number =  $1.0000 \times 10^{-50}$

Therefore, maximum positive number =  $9.9999 \times 10^{49}$

Minimum positive number =  $1.0000 \times 10^{-50}$

8 votes

-- HABIB MOHAMMAD KHAN (67.5k points)

- 4.16.3 Floating Point Representation: GATE CSE 1990 | Question: 1-iv-a [top](#) <https://gateoverflow.in/83830> 
- PS: It is an old question and IEEE format was not there then. Currently we use IEEE format if anything is unspecified.

As given exponent bits are 7 bits.

So, minimum it could be all 7 bit are 0's and maximum it could all 1's.

Assuming 2's complement representation minimum value =  $-2^6 = -64$  and maximum value =  $2^6 - 1 = 63$ .

18 votes

-- minal (13.1k points)

4.16.4 Floating Point Representation: GATE CSE 1990 | Question: 1-iv-b [top](#) <https://gateoverflow.in/20382> 

- ✓ Minimum number = 0 , maximum number = 127,

Given excess 64 so, bias number is 64,

Range will be  $0 - 64 = -64$  to  $(127 - 64 = 63)63$ .

Here, in question given that base is 16, so the actual value represented will be  $(-1)^s(0.M) \times 16^{E-\text{bias}}$ .

10 votes

-- minal (13.1k points)

4.16.5 Floating Point Representation: GATE CSE 1997 | Question: 72 [top](#) <https://gateoverflow.in/19702> 

PART A

$$A = 54.75 = 110110.11_2$$

Coming to the floating point representation we need to know whether to use "implied 1" in normalized representation or not. This is a 1997 question and IEEE-754 was not there and hence we cannot assume implied one.

$$\text{So, } A = 110110.11 = 0.11011011 \times 2^6$$

Thus mantissa = 11011011 and exponent = 110. We use sign magnitude representation for both mantissa and exponent, mantissa bits are 6 including sign and exponent bits are 4 including sign. So, we get

mantissa = 011011 and exponent = 0110 which means  $A = (011011, 0110)$

$$B = 9.75 = 1001.11_2$$

$$= 0.100111 \times 2^4$$

So, mantissa bits = 010011 (truncated to 6 bits) and exponent bits = 0100.

$$\Rightarrow B = (010011, 0100)$$

PART B

To add two floating point numbers we must first make their exponents same and then add the mantissas. To make the exponents same we must make the smaller one equal to the larger (we cannot do the other way around as we can only shift the mantissa bits to right but not the left).

Here,  $A = (011011, 0110)$  and  $B = (010011, 0100)$ .

Since, exponent of  $A$  is larger we change  $B$  to  $B = (000100, 0110)$ .

Now, adding the mantissa parts of  $A$  and  $B$  (MSB is sign bit and not added as in  $2^7$ 's complement representation) we get  $11011 + 00100 = 11111$ . Thus we get  $A + B = (011111, 0110)$ .

PART C

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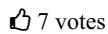
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Precise Result of  $A + B = 54.75 + 9.75 = 64.5$

Result got in Part (b) =  $0.10010 \times 2^7 = 1001000_2 = 72_{10}$ .

So, error =  $72 - 64.5 = 7.5$

$$\text{Percentage Error} = \frac{\text{Error}}{\text{Original Value}} \times 100 = \frac{7.5}{64.5} \times 100 = 11.63\%$$



7 votes

-- Arjun Suresh (332k points)

#### 4.16.6 Floating Point Representation: GATE CSE 2003 | Question: 43

[top](https://gateoverflow.in/934)



- ✓ The maximum difference between two successive real numbers will occur at extremes. This is because numbers are represented up to mantissa bits and as the exponent grows larger, the difference gets multiplied by a larger value. (The minimum difference happens for the least positive exponent value).

Biasing will be done by adding 31 as given in the question. So, actual value of exponent will be represented value  $-31$ . Also, we can not have exponent field as all 1's as given in question (usually taken for representing infinity, NAN etc). So, largest value that can be stored is  $111110 = 62$ .

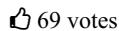
Largest number will be  $1.11111111 \times 2^{62-31} = (2 - 2^{-9}) \times 2^{31}$

Second largest number will be  $1.11111110 \times 2^{62-31} = (2 - 2^{-8}) 2^{31}$

So, difference between these two numbers

$$= (2 - 2^{-9}) \times 2^{31} - (2 - 2^{-8}) \times 2^{31} = 2^{31} [(2 - 2^{-9}) - (2 - 2^{-8})] = 2^{31} [2^{-8} - 2^{-9}] = 2^{31} \times 2^{-9} = 2^{22}$$

Correct Answer: C.



69 votes

-- Ashish Gupta (759 points)

#### 4.16.7 Floating Point Representation: GATE CSE 2005 | Question: 85-a

[top](https://gateoverflow.in/1407)



- ✓ Answer is **option D** in both questions.

$$0.239 = (0.00111101)_2$$

(a) Stored exponent = actual + biasing

$$13 + 64 = 77$$

$$(77)_{10} = (1001101)_2$$

Answer is:  $\underbrace{0}_{\text{sign}} \underbrace{1001101}_{\text{exponent}} \underbrace{00111101}_{\text{mantissa}} = 0x 4D 3D$

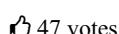
(b) For normalized representation

$$0.00111101 * 2^{13} = 1.11101 * 2^{10}$$

$$\text{Stored exponent} = 10 + 64 = 74$$

$$(74)_{10} = (1001010)_2$$

Answer:  $\underbrace{0}_{\text{sign}} \underbrace{1001010}_{\text{exponent}} \underbrace{11101000}_{\text{mantissa}} = 0x 4A E8$



47 votes

-- Pooja Palod (24.1k points)

#### 4.16.8 Floating Point Representation: GATE CSE 2005 | Question: 85-b

[top](https://gateoverflow.in/82139)



- ✓ For finding normalised representation we need to find unnormalised one first. So, we have:

$0.239 \times 2^{13}$  as the number. So, we find the binary equivalent of 0.239 till 8 digits as capacity of mantissa field is 8 bits. We follow the following procedure:

- $0.239 \times 2 = 0.478$
- $0.478 \times 2 = 0.956$
- $0.956 \times 2 = 1.912$
- $0.912 \times 2 = 1.824$
- $0.824 \times 2 = 1.648$
- $0.648 \times 2 = 1.296$
- $0.296 \times 2 = 0.512$
- $0.512 \times 2 = 1.024$

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We stop here as we have performed 8 iterations and hence, 8 digits of mantissa of unnormalised number is obtained. Now we have:

Mantissa of given number = 00111101

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So, the number can be written as:  $0.00111101 \times 2^{13}$

Now we need to align the mantissa towards left to get normalised number. And in the question it is mentioned that during alignment process 0's will be padded in the right side as a result of mantissa alignment to left.

So, to get normalised number, we align to left 3 times, to get new mantissa = 11101000

Exponent will also decrease by 3 hence, new exponent = 10

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So, normalised number =  $1.1101000 \times 2^{10}$

Actual exponent = 10

Given excess 64 is used which means bias value = 64

So, exponent field value =  $10 + 64 = 74$

And of course sign bit = 0 being a positive number.

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Thus the final representation of number

$$\begin{aligned} &= 01001010\ 11101000 \\ &= 0100\ 1010\ 1110\ 1000 \\ &= (4AE8)_{16} \end{aligned}$$

Hence, (D) should be the correct answer.

32 votes

-- HABIB MOHAMMAD KHAN (67.5k points)

#### 4.16.9 Floating Point Representation: GATE CSE 2020 | Question: 29 top

<https://gateoverflow.in/333202>



$$R_3 = \frac{R_1}{R_2} = \frac{42200000}{C1200000} = \frac{0100\ 0010\ 010}{1100\ 0001\ 010} = \frac{+132\ 010}{-130\ 010} = -(2 + 127)000 = 110000001000 = C08$$

For IEEE single precision format,  
 S(Sign Bit) = 1 bit  
 E(Exponent) = 8 bits  
 M(Mantissa) = 23 bits

- (1) Sign bit will be -ve because division of +ve and -ve will result in a -ve number  
 (2) Exponent will be  $(132 - 130 = 2)$  and biased exponent will be  $2 + 127 = 129$   
 (3) Normalized Mantissa will be  $\frac{1.010}{1.010} = 1.000$

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 For more elaboration, please refer: [General Floating-Point Division](#)

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References



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👉 23 votes

-- Vijay Verma (195 points)

$$R1 = 0x42200000 = 0100\ 0010\ 0010\ 0000\ 0000\ 0000\ 0000$$

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As per IEEE -754 single precision format,

S=0 ==> +ve number

$$\text{Exponent} = (10000100)_2 = 128+4 = 132$$

$$\text{true exponent} = 132-127 = 5$$

$$\text{Mantissa} = (010\ 00000000)_2$$

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$$\text{value} = (-1)^0 \cdot (1.0100000000\dots) * 2^5 = (101000.000000\dots)_2 = 40$$

$$R2 = 0xC1200000 = 1100\ 0001\ 0010\ 0000\ 0000\ 0000\ 0000$$

As per IEEE -754 single precision format,

S=1 ==> -ve number

$$\text{Exponent} = (10000010)_2 = 128+2 = 130$$

$$\text{true exponent} = 130-127 = 3$$

$$\text{Mantissa} = (010\ 00000000)_2$$

$$\text{value} = (-1)^1 \cdot (1.0100000000\dots) * 2^3 = (1010.000000\dots)_2 = -10$$

$$R3 = \frac{40}{-10} = -4$$

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represent -4 in IEEE-754 single precision format

S=1

$$\text{Value} = (100.0000) * 2^0 = (1.0000000\dots) * 2^2$$

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$$\text{true exponent} = 2 ==> \text{exponent} = 2+127=129 = (10000001)_2$$

$$\text{Mantissa} = 000000..0$$

$$-4 \text{ in IEEE format : } 1100\ 0000\ 1000\ 0000\ 0000\ 0000\ 0000$$

$$\text{in Hexa decimal format : } 0xC0800000$$

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option B is correct

👉 33 votes

-- Shaik Masthan (50.4k points)



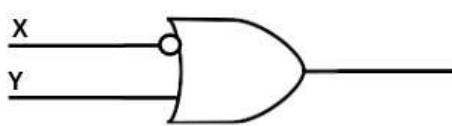
Show that  $\{\text{NOR}\}$  is a functionally complete set of Boolean operations.

gate1989 descriptive digital-logic functional-completeness

Answer



The implication gate, shown below has two inputs ( $x$  and  $y$ ); the output is 1 except when  $x = 1$  and  $y = 0$ , realize  $f = \bar{x}y + x\bar{y}$  using only four implication gates.



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Show that the implication gate is functionally complete.

gate1998 digital-logic functional-completeness descriptive

Answer



Which of the following sets of component(s) is/are sufficient to implement any arbitrary Boolean function?

- A. XOR gates, NOT gates
- B. 2 to 1 multiplexers
- C. AND gates, XOR gates
- D. Three-input gates that output  $(A \cdot B) + C$  for the inputs  $A, B$  and  $C$ .

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gate1999 digital-logic normal functional-completeness multiple-selects

Answer



A set of Boolean connectives is functionally complete if all Boolean functions can be synthesized using those. Which of the following sets of connectives is NOT functionally complete?

- A. EX-NOR
- B. implication, negation
- C. OR, negation
- D. NAND

gate2008-it digital-logic easy functional-completeness

Answer

### Answers: Functional Completeness



- ✓ The functionally complete set is by which you can perform all operations. So, if any logical set is able to implement the operation  $\{\text{And}, \text{NOT}\}$  or  $\{\text{OR}, \text{NOT}\}$ ; it is known as functionally complete.

Now come to NOR gate.

$$\text{classroom.gateoverflow.in} \\ \bullet A(\text{NOR})B = (A + B)'$$

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- $A(\text{NOR})A = (A + A)' = (A)'$ , so we can perform the NOT operation .
- $(A + B)' \text{ NOR } (A + B)' = ((A + B)' + (A + B)')' = ((A + B)')' = (A + B)$  , so OR operation is also performed successfully .

So, NOR is functionally complete.

16 votes

-- Amit Pal (3k points)

#### 4.17.2 Functional Completeness: GATE CSE 1998 | Question: 5



- ✓ Implication gate is  $A \rightarrow B$  which becomes  $A' + B$

So, let  $f(A, B) = A' + B$

$$f(A, 0) = A' \text{ (we get complement)}$$

$$f(f(A, 0), B) = f(A', B) = A + B \text{ (we get OR gate)}$$

Thus it is functionally complete.

$$\text{Let } F(X, Y) = X' + Y$$

$$F(Y, X) = Y' + X$$

$$F(F(Y' + X), 0) = X'Y$$

$F(F(X, Y), X'Y) = XY' + XY'$  Therefore, the above function is implemented with 4 implication gates.

16 votes

-- Riya Roy(Arayana) (5.3k points)

#### 4.17.3 Functional Completeness: GATE CSE 1999 | Question: 2.9



- ✓ 1. XOR and NOT gates can only make XOR and XNOR which are not functionally complete-  $a \oplus \bar{a} = 1, a \oplus a = 0$ .

2. 2-1 multiplexer is functionally complete provided we have external 1 and 0 available. For NOT gate, use  $x$  as select line and use 0 and 1 as inputs. For AND gate, use  $y$  and 0 as inputs and  $x$  as select. With {AND, NOT} any other gate can be made.

3. XOR can be used to make a NOT gate ( $a \oplus 1 = \bar{a}$ ) and {AND, NOT} is functionally complete. Again this requires external 1.

4. We have  $AB + C$ . Using  $C = 0$ , we get an AND gate. Using  $B = 1$  we get an OR gate. But we cannot derive a NOT gate here.

So, options B and C are true provided external 1 and 0 are available.

49 votes

-- Arjun Suresh (332k points)

#### 4.17.4 Functional Completeness: GATE IT 2008 | Question: 1



- ✓ EX-NOR is not functionally complete.

NOR and NAND are functionally complete logic gates, OR , AND, NOT any logic gate can be implemented using them.

And (Implication, Negation) is also functionally complete

First complement  $q$  to get  $q'$  then

$$p \rightarrow q = p' + q'$$

Now complement the result to get AND gate

$$(p' + q')' \Rightarrow pq$$

43 votes

-- Manu Thakur (34k points)

## 4.18

### Ieee Representation (7)

#### 4.18.1 Ieee Representation: GATE CSE 2008 | Question: 4



In the IEEE floating point representation the hexadecimal value 0x00000000 corresponds to

- A. The normalized value  $2^{-127}$   
 B. The normalized value  $2^{-126}$   
 C. The normalized value  $+0$   
 D. The special value  $+0$

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 gate2008-cse digital-logic floating-point-representation ieee-representation easy

Answer 

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4.18.2 Ieee Representation: GATE CSE 2012 | Question: 7 [top](#) 

<https://gateoverflow.in/39>

The decimal value 0.5 in IEEE single precision floating point representation has

- A. fraction bits of 000...000 and exponent value of 0  
 B. fraction bits of 000...000 and exponent value of  $-1$   
 C. fraction bits of 100...000 and exponent value of 0  
 D. no exact representation

gate2012-cse digital-logic normal number-representation ieee-representation

Answer 

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4.18.3 Ieee Representation: GATE CSE 2014 Set 2 | Question: 45 [top](#) 

<https://gateoverflow.in/2011>

The value of a float type variable is represented using the single-precision 32-bit floating point format of IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for the mantissa. A float type variable  $X$  is assigned the decimal value of  $-14.25$ . The representation of  $X$  in hexadecimal notation is

- A. C1640000H  
 B. 416C0000H  
 C. 41640000H  
 D. C16C0000H

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 gate2014-cse-set2 digital-logic number-representation normal ieee-representation

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Answer 

4.18.4 Ieee Representation: GATE CSE 2017 Set 2 | Question: 12 [top](#) 

<https://gateoverflow.in/118434>

Given the following binary number in 32-bit (single precision) IEEE-754 format :

00111110011011010000000000000000

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The decimal value closest to this floating-point number is :

- A.  $1.45 * 10^1$   
 B.  $1.45 * 10^{-1}$   
 C.  $2.27 * 10^{-1}$   
 D.  $2.27 * 10^1$

gate2017-cse-set2 digital-logic number-representation floating-point-representation ieee-representation

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Answer 

4.18.5 Ieee Representation: GATE CSE 2021 Set 1 | Question: 24 [top](#) 

<https://gateoverflow.in/357427>

Consider the following representation of a number in IEEE 754 single-precision floating point format with a bias of 127.

$S : 1 \quad E : 10000001 \quad F : 11110000000000000000000000000000$

Here  $S$ ,  $E$  and  $F$  denote the sign, exponent, and fraction components of the floating point representation.

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The decimal value corresponding to the above representation (rounded to 2 decimal places) is \_\_\_\_\_.

gate2021-cse-set1 digital-logic number-representation ieee-representation numerical-answers

Answer 

#### 4.18.6 Ieee Representation: GATE CSE 2021 Set 2 | Question: 4 top

<https://gateoverflow.in/357536>

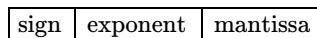


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The format of the single-precision floating point representation of a real number as per the IEEE 754 standard is as follows:



Which one of the following choices is correct with respect to the *smallest* normalized positive number represented using the standard?

- A. exponent = 00000000 and mantissa = 00000000000000000000000000000000
- B. exponent = 00000000 and mantissa = 00000000000000000000000000000001
- C. exponent = 00000001 and mantissa = 00000000000000000000000000000000
- D. exponent = 00000001 and mantissa = 00000000000000000000000000000001

gate2021-cse-set2 digital-logic number-representation ieee-representation

Answer 

#### 4.18.7 Ieee Representation: GATE IT 2008 | Question: 7 top

<https://gateoverflow.in/3267>



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The following bit pattern represents a floating point number in IEEE 754 single precision format

1 10000011 10100000000000000000000000000000

The value of the number in decimal form is

- A. -10
- B. -13
- C. -26
- D. None of the above

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gate2008-it digital-logic number-representation floating-point-representation ieee-representation normal

Answer 

### Answers: Ieee Representation

#### 4.18.1 Ieee Representation: GATE CSE 2008 | Question: 4 top

<https://gateoverflow.in/402>



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S	BE	M	Value
0 / 1	All 0's	All 0's	0
0	All 1's	All 0's	$+\infty$
1	All 1's	All 0's	$-\infty$
0 / 1	All 1's	Non-zero	NaN

The answer is option D.

Reference: <http://steve.hollasch.net/cgindex/coding/ieefloat.html>

References



48 votes

-- Amar Vashishth (25.2k points)

#### 4.18.2 Ieee Representation: GATE CSE 2012 | Question: 7 top

<https://gateoverflow.in/39>



- ✓ (B) is the answer. IEEE 754 representation uses normalized representation when the exponent bits are all non zeroes and hence an implicit '1' is used before the decimal point. So, if mantissa is:

0000..0

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Ut would be treated as:

1.000..0

and hence, the exponent need to be  $-1$  for us to get 0.1 which is the binary representation of 0.5.

More into IEEE floating point representation:

<http://steve.hollasch.net/cgindex/coding/ieeefloat.html>

References



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36 votes

-- gatecse (63.3k points)



4.18.3 Ieee Representation: GATE CSE 2014 Set 2 | Question: 45 top

<https://gateoverflow.in/2011>

- ✓ IEEE-754 representation for float (single-precision) type is as follows

0 Sign	1-8 Exponent	9-31 Mantissa
-----------	-----------------	------------------

Thus, the exponent field is of 8 bits and mantissa is of 23 bits (precision is actually of 24 bits due to an implied 1 mandated in normalized representation; IEEE 754 also allows denormalized numbers which are close to 0 but this is not applicable to the given question).

The exponent field also requires sign to represent fractions. IEEE 754 does this by giving a bias -- 127 for single-precision which means we simply subtract 127 from the represented value to get the actual value. Thus, 0 becomes  $-127$  and 255 (maximum value representable using 8 bits) becomes 128.

Now, coming to the given question we need to represent  $-14.25$  which equals  $-1110.01$  in binary.

Converting to normalized form (only one 1 to the left of .) we get

$$-1110.01 = -1.11001 \times 2^3$$

Since we omit the implied 1 in IEEE-754 representation we get

- Mantissa bits = 11001
- Exponent bits =  $11 + 011111 = 10000010$  (Adding bias 127)
- Sign bit = 1 (since number is negative)

This will be 1 10000010 11001000000000000000000000000000

Grouping in 4 bits to convert to Hexadecimal we get

$$\begin{array}{cccccccc} 1 & 1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{array}$$

= C164000H

Option A.

More Reference: <http://steve.hollasch.net/cgindex/coding/ieeefloat.html>

References



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11 votes

-- Arjun Suresh (332k points)



- ✓ In 32 bit (single precision) IEEE-754 format, binary number is represented as  $S(1 \text{ bit}) E(8 \text{ bit}) M(23 \text{ bits})$  with implicit normalization and exponent is represented with Excess-127 code.

Here, Sign *bit* = 0  $\Rightarrow$  Number is positive.

Exponent bits = 01111100 = 124  $\Rightarrow E = 124 - 127 = -3$  (Excess-127)

Mantissa bits = 1101101000000000000000000  $\Rightarrow$  Number = 1.1101101 (Implicit normalization).

$$\therefore \text{Number} = 1.1101101 * 2^{-3} = 0.0011101101 = 0.227 \approx 2.27 \times 10^{-1}$$

$\therefore$  Answer should be **C**.

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1 like 38 votes

-- Kantikumar (3.4k points)



- ✓ -7.75 is correct answer.

Here, Sign bit = 1  $\rightarrow$  Number is negative.

Exponent bits = 10000001 = 129<sub>10</sub>  $\rightarrow E = 129 - 127 = 2$  as IEEE-754 single precision format uses 127 as the exponent bias.

Mantissa bits = 11110000000000000000000000000000

$$\text{Number} = -1.111100\dots00 \times 2^2 = -111.11$$

$$\therefore \text{Number} = (-7.75)_{10}.$$

Reference: <https://steve.hollasch.net/cgindex/coding/ieefloat.html>

References



1 like 4 votes

-- Himanshu (929 points)



- ✓ In IEEE 754 representation all 1s in exponent field is reserved for special numbers

- + (when sign bit is positive) and - (when sign bit is negative) infinities when all mantissa bits are zeroes.
- SNAN (Signaling Not A Number): when leading mantissa bit is 0 and at least one other mantissa bit is non-zero
- NAN (Quiet NAN): when leading mantissa bit is 1

More read on QNAN vs SNAN: <https://stackoverflow.com/questions/18118408/what-is-the-difference-between-quiet-nan-and-signaling-nan>

Also, all 0s for exponent field is reserved for denormalized numbers (small numbers between 0 and  $\pm 1$  which cannot be represented using normalized numbers). That is, a normalized IEEE 754 represented number (both single and double precision) must have at least one bit set in the exponent field and for the smallest exponent this will be the right most bit. Now, to make it the smallest **positive** normalized number in single-precision format, we can have all mantissa bits 0 which will give the numerical value as  $1.\underbrace{000\dots0}_{23 \text{ zeroes}} \times 2^{1-127} = 2^{-126}$ . (Here, 1 before "." is implied in IEEE 754 representation for every

normalized numbers and 127 is the exponent bias used to have negative exponents without an explicit sign bit)

Reference: <https://steve.hollasch.net/cgindex/coding/ieefloat.html>

References



1 like 2 votes

-- gatecse (63.3k points)

#### 4.18.7 Ieee Representation: GATE IT 2008 | Question: 7 top ↗

↗ <https://gateoverflow.in/3267>



- ✓ Sign bit is 1  $\implies$  number is negative

Exponent bits- 10000011

Exponent is added with 127 bias in IEEE single precision format. So, actual exponent =  $10000011 - 127 = 131 - 127 = 4$

Mantissa bits- 10100000000000000000000000000000

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In IEEE format, an implied 1 is before mantissa, and hence the actual number is:

$$-1.101 \times 2^4$$

$$= -(1101)_2 = -26$$

<http://steve.hollasch.net/cgindex/coding/ieefloat.html>

Correct Answer: C

References



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1 like 44 votes

-- Arjun Suresh (332k points)

#### 4.19

#### K Map (19) top ↗

##### 4.19.1 K Map: GATE CSE 1987 | Question: 16-a top ↗

↗ <https://gateoverflow.in/82698>



A Boolean function  $f$  is to be realized only by NOR gates. Its K-map is given below:

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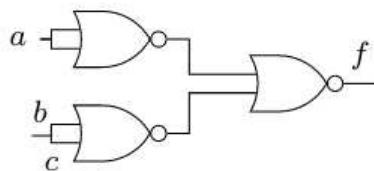
		ab	00	01	11	10
		c	0	0	1	1
0	0	0	0	1	1	
	1	0	1	1	1	

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The realization is

A.

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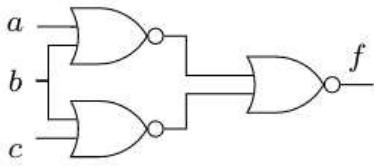
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B.

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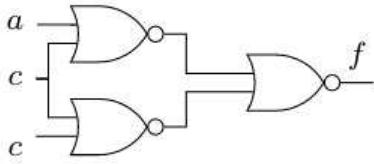


C.

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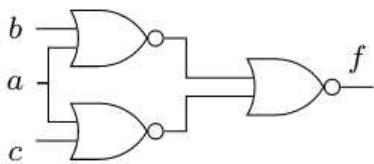


D.

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gate1987 digital-logic k-map

Answer ↗

4.19.2 K Map: GATE CSE 1988 | Question: 3a-b top ↺<https://gateoverflow.in/94358>

		BC			
		00	01	11	10
A	0	1		1	1
	1		1	1	

		B	
		0	1
A	0	$\bar{C}$	1
	1	C	C

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The Karnaugh map of a function of  $(A, B, C)$  is shown on the left hand side of the above figure.The reduced form of the same map is shown on the right hand side, in which the variable  $C$  is entered in the map itself. Discuss,

- The methodology by which the reduced map has been derived and
- the rules (or steps) by which the boolean function can be derived from the entries in the reduced map.

gate1988 descriptive digital-logic k-map

Answer ↗

4.19.3 K Map: GATE CSE 1992 | Question: 01-i top ↺<https://gateoverflow.in/545>

The Boolean function in sum of products form where K-map is given below (figure) is \_\_\_\_\_

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	<i>C</i>	0	1
	<i>B</i>		
0		1	0
1		$\bar{A}$	$A$

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gate1992 digital-logic k-map normal fill-in-the-blanks

Answer **4.19.4 K Map: GATE CSE 1995 | Question: 15-a** top ↺<https://gateoverflow.in/2651>

Implement a circuit having the following output expression using an inverter and a nand gate

$$Z = \bar{A} + \bar{B} + C$$

gate1995 digital-logic k-map normal descriptive

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Answer **4.19.5 K Map: GATE CSE 1995 | Question: 15-b** top ↺<https://gateoverflow.in/203837>

What is the equivalent minimal Boolean expression (in sum of products form) for the Karnaugh map given below?

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	<i>AB</i>	00	01	11	10
	<i>CD</i>				
00		1			1
01			1	1	
11			1	1	
10		1			1

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gate1995 digital-logic boolean-algebra k-map normal descriptive

Answer **4.19.6 K Map: GATE CSE 1996 | Question: 2.24** top ↺<https://gateoverflow.in/2753>

What is the equivalent Boolean expression in product-of-sums form for the Karnaugh map given in Fig

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	<i>AB</i>	00	01	11	10
	<i>CD</i>				
00			1	1	
01		1			1
11		1			1
10			1	1	

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- A.  $B\bar{D} + \bar{B}D$

B.  $(B + \bar{C} + D)(\bar{B} + C + \bar{D})$

C.  $(B + D)(\bar{B} + \bar{D})$

D.  $(B + \bar{D})(\bar{B} + D)$

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gate1996 digital-logic k-map easy

Answer 

4.19.7 K Map: GATE CSE 1998 | Question: 2.7 [top](#) 



The function represented by the Karnaugh map given below is

		BC	00	01	10	11
		A	1	0	0	1
0	0	1	0	0	1	
	1	1	0	0	1	

A.  $A \cdot B$

B.  $AB + BC + CA$

C.  $\overline{B} \oplus C$

D.  $A \cdot BC$

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gate1998 digital-logic k-map normal

Answer 

4.19.8 K Map: GATE CSE 1999 | Question: 1.8 [top](#) 



Which of the following functions implements the Karnaugh map shown below?

		CD	00	01	11	10
		AB	0	0	1	0
00	00	0	0	X	X	
	01	0	1	1	0	
11	00	0	1	1	0	
	01	0	1	1	0	

A.  $\bar{A}B + CD$

B.  $D(C + A)$

C.  $AD + \bar{A}B$

D.  $(C + D)(\bar{C} + D) + (A + B)$

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gate1999 digital-logic k-map easy

Answer 

4.19.9 K Map: GATE CSE 2000 | Question: 2.11 [top](#) 



Which functions does NOT implement the Karnaugh map given below?

$wz \backslash xy$	00	01	11	10
00	0	X	0	0
01	0	X	1	1
11	1	1	1	1
10	0	X	0	0

- A.  $(w + x)y$   
 B.  $xy + yw$   
 C.  $(w + x)(\bar{w} + y)(\bar{x} + y)$   
 D. None of the above

[gate2000-cse](#) [digital-logic](#) [k-map](#) [normal](#)
Answer 4.19.10 K Map: GATE CSE 2001 | Question: 1.11 [top](#)<https://gateoverflow.in/704>

Given the following karnaugh map, which one of the following represents the minimal Sum-Of-Products of the map?

$wx \backslash yz$	00	01	11	10
00	0	X	0	X
01	X	1	X	1
11	0	X	1	0
10	0	1	X	0

- A.  $XY + Y'Z$   
 B.  $WX'Y' + XY + XZ$   
 C.  $W'X + Y'Z + XY$   
 D.  $XZ + Y$

[gate2001-cse](#) [k-map](#) [digital-logic](#) [normal](#)
Answer 4.19.11 K Map: GATE CSE 2002 | Question: 1.12 [top](#)<https://gateoverflow.in/816>

Minimum sum of product expression for  $f(w, x, y, z)$  shown in Karnaugh-map below

	<i>wx</i>	00	01	11	10
<i>yz</i>		0	1	1	0
00		X	0	0	1
01		X	0	0	1
11		0	1	1	X
10					

- A.  $xz + y'z$   
 B.  $xz' + zx'$   
 C.  $x'y + zx'$   
 D. None of the above

Answer 4.19.12 K Map: GATE CSE 2003 | Question: 45 top ↴

The literal count of a Boolean expression is the sum of the number of times each literal appears in the expression. For example, the literal count of  $(xy + xz')$  is 4. What are the minimum possible literal counts of the product-of-sum and sum-of-product representations respectively of the function given by the following Karnaugh map? Here, X denotes "don't care"

	<i>zw</i>	00	01	11	10
<i>xy</i>		X	1	0	1
00		0	1	X	0
01		1	X	X	0
11		X	0	0	X
10					

- A. (11, 9)  
 B. (9, 13)  
 C. (9, 10)  
 D. (11, 11)

Answer 4.19.13 K Map: GATE CSE 2008 | Question: 5 top ↴

In the Karnaugh map shown below, X denotes a don't care term. What is the minimal form of the function represented by the Karnaugh map?

	ab	00	01	11	10
cd	00	1	1		1
	01	X			
	11	X			
	10	1	1		X

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- A.  $\bar{b} \cdot \bar{d} + \bar{a} \cdot \bar{d}$   
 B.  $\bar{a} \cdot \bar{b} + \bar{b} \cdot \bar{d} + \bar{a} \cdot b \cdot \bar{d}$   
 C.  $\bar{b} \cdot \bar{d} + \bar{a} \cdot b \cdot \bar{d}$   
 D.  $\bar{a} \cdot \bar{b} + \bar{b} \cdot \bar{d} + \bar{a} \cdot \bar{d}$

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gate2008-cse digital-logic k-map easy

Answer **4.19.14 K Map: GATE CSE 2012 | Question: 30** top ↴<https://gateoverflow.in/1615>

What is the minimal form of the Karnaugh map shown below? Assume that X denotes a don't care term

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	ab	00	01	11	10
cd	00	1	X	X	1
	01	X			1
	11				
	10	1			X

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- A.  $\bar{b}\bar{d}$   
 B.  $\bar{b}\bar{d} + \bar{b}\bar{c}$   
 C.  $\bar{b}\bar{d} + a\bar{b}\bar{c}\bar{d}$   
 D.  $\bar{b}\bar{d} + \bar{b}\bar{c} + \bar{c}\bar{d}$

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gate2012-cse digital-logic k-map easy

Answer **4.19.15 K Map: GATE CSE 2017 Set 1 | Question: 21** top ↴<https://gateoverflow.in/118301>

Consider the Karnaugh map given below, where X represents "don't care" and blank represents 0.

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ba	00	01	11	10
dc		X	X	
00				
01	1			X
11	1			1
10		X	X	

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Assume for all inputs  $(a, b, c, d)$ , the respective complements  $(\bar{a}, \bar{b}, \bar{c}, \bar{d})$  are also available. The above logic is implemented using 2-input NOR gates only. The minimum number of gates required is \_\_\_\_\_.

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gate2017-cse-set1 digital-logic k-map numerical-answers normal

Answer 

#### 4.19.16 K Map: GATE CSE 2019 | Question: 30 top

<https://gateoverflow.in/302818>

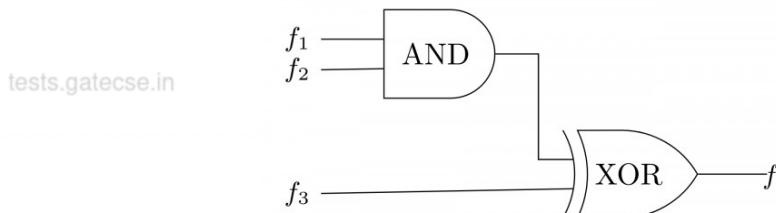


Consider three 4-variable functions  $f_1, f_2$ , and  $f_3$ , which are expressed in sum-of-minterms as  
 $f_1 = \Sigma(0, 2, 5, 8, 14)$ ,

$$f_2 = \Sigma(2, 3, 6, 8, 14, 15),$$

$$f_3 = \Sigma(2, 7, 11, 14)$$

For the following circuit with one AND gate and one XOR gate the output function  $f$  can be expressed as:



- A.  $\Sigma(7, 8, 11)$
- B.  $\Sigma(2, 7, 8, 11, 14)$
- C.  $\Sigma(2, 14)$
- D.  $\Sigma(0, 2, 3, 5, 6, 7, 8, 11, 14, 15)$

gate2019-cse digital-logic k-map digital-circuits

Answer 

#### 4.19.17 K Map: GATE IT 2006 | Question: 35 top

<https://gateoverflow.in/3574>



The boolean function for a combinational circuit with four inputs is represented by the following Karnaugh map.

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RS	PQ	00	01	11	10
00		1	0	0	1
01		0	0	1	1
11		1	1	1	0
10		1	0	0	1

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Which of the product terms given below is an essential prime implicant of the function?

- A. QRS tests.gatecse.in
- B. PQS goclasses.in
- C. PQ'S' tests.gatecse.in
- D. Q'S' goclasses.in

gate2006-it digital-logic k-map normal

Answer 

4.19.18 K Map: GATE IT 2007 | Question: 78 top ↗

↗ <https://gateoverflow.in/3530>



Consider the following expression

$$ad + \bar{a}\bar{c} + b\bar{c}d$$

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Which of the following Karnaugh Maps correctly represents the expression?

A.

		cd	00	01	11	10	
		ab	00	X	X		
		01	X	X			
		11	X	X		X	
		10	X			X	

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tests.gatecse.in

B.

		cd	00	01	11	10	
		ab	00	X	X		
		01	X				
		11	X	X		X	
		10	X	X		X	

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tests.gatecse.in

C.

		cd	00	01	11	10	
		ab	00	X	X		
		01	X	X		X	
		11	X	X		X	
		10	X			X	

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D.

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		cd	00	01	11	10	
		ab	00	X	X		
		01	X	X		X	
		11	X	X		X	
		10	X		X	X	

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gate2007-it digital-logic k-map normal

Answer ↗

**4.19.19 K Map: GATE IT 2007 | Question: 79** top ↗↗ <https://gateoverflow.in/3531>

Consider the following expression

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$$ad + \bar{a}\bar{c} + b\bar{c}d$$

Which of the following expressions does not correspond to the Karnaugh Map obtained for the given expression?

- A.  $\bar{c}\bar{d} + ad + ab\bar{c} + \bar{a}\bar{c}d$
- B.  $\bar{a}\bar{c} + \bar{c}\bar{d} + ad + ab\bar{c}d$
- C.  $\bar{a}\bar{c} + ad + ab\bar{c} + \bar{c}d$
- D.  $\bar{b}\bar{c}\bar{d} + ac\bar{d} + \bar{a}\bar{c} + ab\bar{c}$

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gate2007-it digital-logic k-map normal

Answer ↗

**Answers: K Map****4.19.1 K Map: GATE CSE 1987 | Question: 16-a** top ↗↗ <https://gateoverflow.in/82698>

- ✓ classroom.gateoverflow.in  
Two Max Terms are:

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(a + b)(a + c) so, "a" is common here only possibility is option D.

K-map will give min terms = a[41's circle] + bc[21's box]

Option D circuit will give = (a + b)(a + c) = a + bc

D will be answer.

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20 votes

-- papesh (18k points)

**4.19.2 K Map: GATE CSE 1988 | Question: 3a-b** top ↗↗ <https://gateoverflow.in/94358>



	BC			
	00	01	11	10
A	0	1		1
	1		1	

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We can get the truth table as

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Now, to reduce the K-map to a Variable Entrant Map we can write the function  $F$  in terms of  $C$ . i.e., wherever  $F$  is becoming 1 dependent on  $C$  (i.e. when  $C$  complements  $F$  must become 0), we replace 1 with  $C$  or  $\bar{C}$  based on whichever is giving output 1. So, we can rewrite the truth table as

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A	B	F
0	0	$\bar{C}$
0	1	1
1	0	$C$
1	1	$C$

In the above truth table  $F = 1$  for second row, because when  $A = 0, B = 1, F = 1$  for both  $C$  and  $\bar{C}$  making  $F$  independent of  $C$ . Now, if we draw the K-map for the above truth table we get the reduced Variant Entrant map given.

10 votes

-- Arjun Suresh (332k points)

#### 4.19.3 K Map: GATE CSE 1992 | Question: 01-i top

► <https://gateoverflow.in/545>



- ✓ Answer -  $ABC + B'C' + A'C'$

Expand this K map of 2 variables (4 cells) to K map of three variable (8 cells)

Entries which are non zero are:  $A'B'C'$ ,  $AB'C'$ ,  $A'BC'$  and  $ABC$

Minimize SOP expression using that K map.

22 votes

-- Ankit Rokde (6.9k points)

#### 4.19.4 K Map: GATE CSE 1995 | Question: 15-a top

► <https://gateoverflow.in/2651>

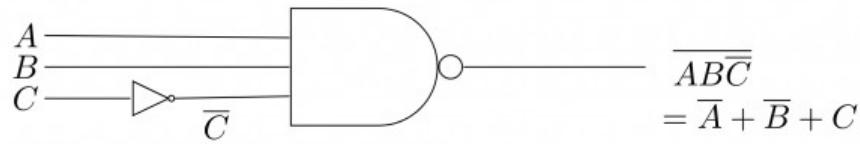


- ✓ The circuit can be implemented as follows:

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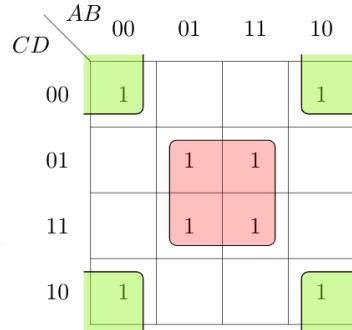
16 votes

-- Leen Sharma (28.7k points)



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SUM OF PRODUCT is equal to XNOR GATE

$$SOP = BD + \bar{B}\bar{D} = \overline{B \oplus D} = B \odot D$$

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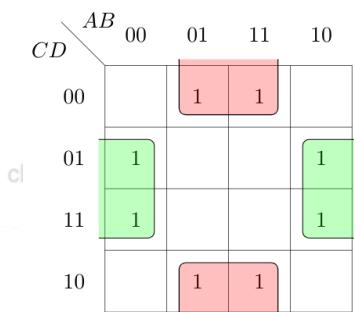
10 votes

-- Lakshman Patel (65.7k points)



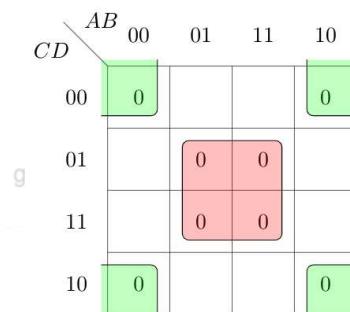
Following two K-Maps are equivalent and represent the same boolean function.

While the first K-Map gives us the boolean expression in Sum-of-Product form, and the second K-Map gives us the same boolean function in Product-of-Sum form:



(i)

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(ii)

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**(C) is correct option!**

PS: If SOP is asked answer will be (A).

11 votes

-- Manu Thakur (34k points)



- ✓ The given K-map is not standard as after "01" we have "10" and two variables are changing for consecutive column. This means it is not safe to merge adjacent 1s. By converting the K-map to standard form we get

		BC	00	01	11	10	
		A	0	1	0	1	0
		0	1	0	1	0	
		1	1	0	1	0	

which gives

$$BC + \bar{B}\bar{C} = B \text{ XNOR } C = B \odot C$$

This can be represented as negation of XOR =  $\overline{B \oplus C}$

Option C is correct.

👍 24 votes

-- shekhar chauhan (32.8k points)



		CD	00	01	11	10	
		AB	00	0	0	1	0
		00	X	X	1	X	
		01	0	1	1	0	
		11	0	1	1	0	
		10	0	1	1	0	

$$CD + AD$$

$$= D(C + A)$$

Correct Answer: B

👍 11 votes

-- Rameez Raza (1.8k points)



- ✓ Answer is D.

See we can simplify each equation given in the option and get that all of them gives  $xy + w\bar{y}$ . But let think in another way.

1<sup>st</sup> option is written in POS form, as we can check we get the same if we consider the following implicants.

		wz	00	01	11	10	
		xy	00	0	X	0	0
		00	0	X	1	1	
		01	0	X	1	1	
		11	1	1	1	1	
		10	0	X	0	0	

which is  $(w + x)y$

for the second one

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$wz \backslash xy$	00	01	11	10
00	0	X	0	0
01	0	X	1	1
11	1	1	1	1
10	0	X	0	0

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Which gives  $wy + xy$

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$wz \backslash xy$	00	01	11	10
00	0	X	0	0
01	0	X	1	1
11	1	1	1	1
10	0	X	0	0

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now for 3rd one, we can verify like this

which is  $(w + x)(\bar{w} + y)(\bar{x} + y)$

So as we can verify each equation in a given K-Map, so the answer is option D

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14 votes

-- akshat sinha (609 points)

#### 4.19.10 K Map: GATE CSE 2001 | Question: 1.11 top ↹

↗ <https://gateoverflow.in/704>



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$wx \backslash yz$	00	01	11	10
00	0	X	0	X
01	X	1	X	1
11	0	X	1	0
10	0	1	X	0

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22 votes

-- Priya Sukumaran (141 points)

#### 4.19.11 K Map: GATE CSE 2002 | Question: 1.12 top ↹

↗ <https://gateoverflow.in/816>



$wx \backslash yz$	00	01	11	10
00	0	1	1	0
01	X	0	0	1
11	X	0	0	1
10	0	1	1	X

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Two quads are getting formed  $x\bar{z}$  and  $z\bar{x}$ 

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**Ans is Option B**

15 votes

-- GATE\_2016 (469 points)

4.19.12 K Map: GATE CSE 2003 | Question: 45 top<https://gateoverflow.in/936>

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We will be getting two different grouping..

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Grouping 1 : (9, 8)

$xy \backslash zw$	00	01	11	10
cl	X	1	0	1
00	0	1	X	0
01	1	X	X	0
10	X	0	0	X

cl

$$\begin{aligned} \text{SOP} &: 2 + 3 \\ &+ 3 = 8 \end{aligned}$$

$xy \backslash zw$	00	01	11	10
ga	X	1	0	1
00	0	1	X	0
01	1	X	X	0
10	X	0	0	X

ga

$$\begin{aligned} \text{POS} &: 2 + 2 + 2 \\ &+ 3 = 9 \end{aligned}$$

GROUPING 2 : (9, 10)

$xy \backslash zw$	00	01	11	10
cl	X	1	0	1
00	0	1	X	0
01	1	X	X	0
11	X	0	0	X
10	X	0	0	X

$xy \backslash zw$	00	01	11	10
gateo	X	1	0	1
00	0	1	X	0
01	1	X	X	0
11	X	0	0	X
10	X	0	0	X

gateo

$$\begin{aligned} \text{POS} &: 2 + 2 + 2 \\ &+ 3 = 9 \end{aligned}$$

$$\begin{aligned} \text{SOP} : & 2 + 2 + 3 \\ & + 3 = 10 \end{aligned}$$

classroom.gateoverflow.in Both the grouping are correct representation of the function  $f(wxyz)$

PS: Some wrong beliefs about don't cares

1. "once you have assumed a don't care as '1' u can't use the same don't care for grouping zeros and vice versa"
2. "if don't care has been used in POS than can't be used in SOP"

Both these statements are wrong. Don't care simply means just don't care -- say we use don't care  $d3$  for grouping 1 in SOP we can use  $d3$  for grouping 0 in POS. (The literals in SOP and POS may not be the same)

K-Map grouping is not unique. And the question says about minimal literals. So, the **best answer would be (9,8)** Since there is no option in GATE we can go with (9, 10) (the question setter might have missed Grouping 1)

77 votes

-- Akhil Nadh PC (16.5k points)

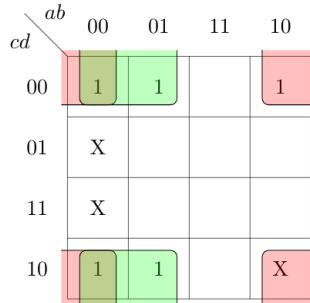
#### 4.19.13 K Map: GATE CSE 2008 | Question: 5 top

<https://gateoverflow.in/403>



- ✓ 2 quads are getting formed:

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Value for first one is  $a'd'$  and value for 2<sup>nd</sup> one is  $b'd'$ .

**Answer is Option A.**

26 votes

-- GATE\_2016 (469 points)

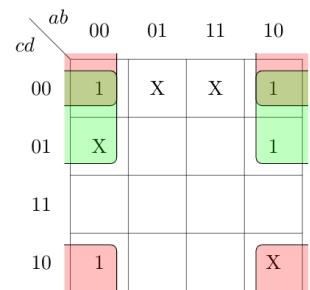
#### 4.19.14 K Map: GATE CSE 2012 | Question: 30 top

<https://gateoverflow.in/1615>



- ✓

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2 quads are getting formed.

Value for First one is  $b'd'$  and value for 2<sup>nd</sup> one is  $b'c'$ . So, **answer is option B.**

31 votes

-- GATE\_2016 (469 points)

#### 4.19.15 K Map: GATE CSE 2017 Set 1 | Question: 21 top

<https://gateoverflow.in/118301>



- ✓ From K-map simplification we get the min-term as  $CA'$ . So We can simplyfy it for NOR gate expression

I.e.  $C' \text{ NOR } A = (C' + A)' = CA'$

Now complemented inputs are also given to us so, for 2 input NOR gate **we need only 1 NOR gate.**

1 is correct answer .

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-- Aboveallplayer (12.5k points)

1 like

#### 4.19.16 K Map: GATE CSE 2019 | Question: 30 [top](#)

<https://gateoverflow.in/302818>



- ✓ Perform  $f_1 \cdot f_2$  first, then with the result perform  $XOR$  with  $f_3$ .

$f_1 \cdot f_2$  means just take common minterms in  $f_1$  and  $f_2$  (WHY? due to AND gate present, the minterm should be present in both functions.)

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$$f_1 \cdot f_2 = \Sigma(0, 2, 5, 8, 14) \cdot \Sigma(2, 3, 6, 8, 14, 15) = \Sigma(2, 8, 14)$$

$$\Sigma(2, 8, 14) \oplus \Sigma(2, 7, 11, 14) = \Sigma(7, 8, 11)$$

1 like

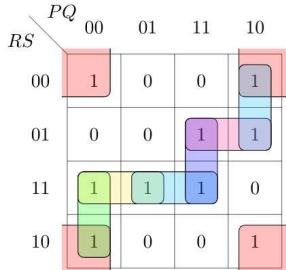
-- Shaik Masthan (50.4k points)

#### 4.19.17 K Map: GATE IT 2006 | Question: 35 [top](#)

<https://gateoverflow.in/3574>



- ✓



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Only the top leftmost and bottom rightmost 1s have no alternate groupings. So, they form the essential prime implicants.

Answer is D.  $Q'S'$

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1 like

-- Ankit Kumar (265 points)

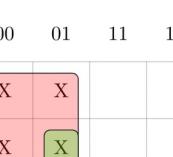
#### 4.19.18 K Map: GATE IT 2007 | Question: 78 [top](#)

<https://gateoverflow.in/3530>



- ✓

$$\begin{aligned} ad + \bar{a}\bar{c} + b\bar{c}d &= ab\bar{c}\bar{d} + \bar{a}bcd + ab\bar{c}\bar{d} + abc\bar{d} \\ &+ \bar{a}b\bar{c}d + \bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}\bar{b}\bar{c}d + \bar{a}\bar{b}cd \\ &+ \bar{a}\bar{b}\bar{c}d + ab\bar{c}d \end{aligned}$$



When we minimize a K-map, we can assume either 0 or 1 for don't cares. But here they have asked for the expression

represented by the K-map. So we can consider  $X$  as 1 and not as a don't care. Also the given expression is equivalent to the above K-map but not the minimal one. Minimal expression will be  $\bar{a}\bar{c} + b\bar{c} + a\bar{d}$ .

Hence, Option A.

10 votes

-- Arjun Suresh (332k points)

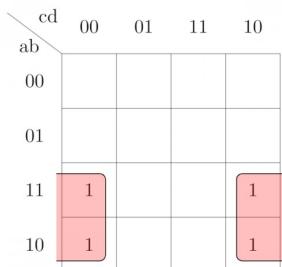
#### 4.19.19 K Map: GATE IT 2007 | Question: 79 top

<https://gateoverflow.in/3531>



- ✓  $ad'$  [fill minterm in K-map in front for  $a$  and  $d'$ ] [gateoverflow.in](https://gateoverflow.in)

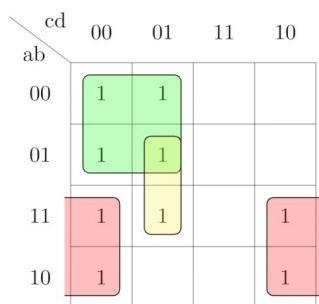
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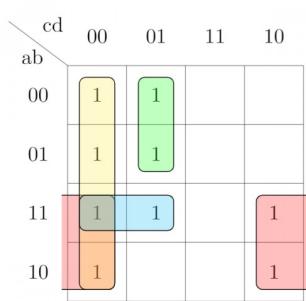
Similarly, fill all minterms for  $ad' + a'c' + bc'd$ , resulting K-map will be:



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**Option (a)**  $c'd' + ad' + abc' + a'c'd$



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is equivalent to given expression

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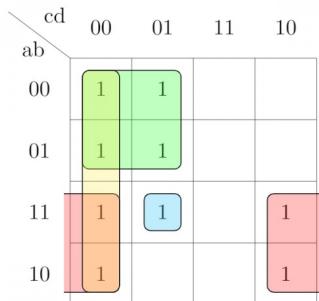
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Option (b)  $a'c' + c'd' + ad' + abc'd$

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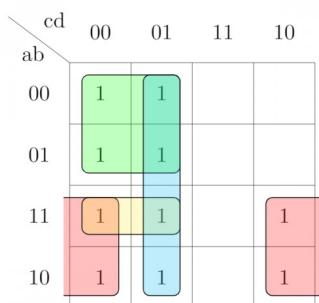
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is equivalent to given expression.

**Option (c)**  $a'c' + ad' + abc' + c'd'$

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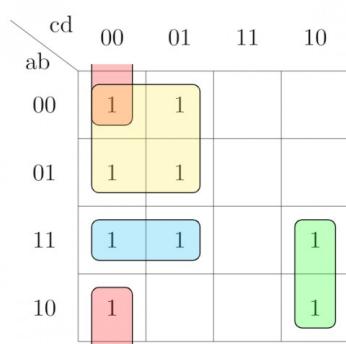
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is not equivalent to given expression.

**Option (d)**  $b'c'd' + acd' + a'c' + abc'$

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is equivalent to given expression.

So, answer is C.

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👉 29 votes

-- Praveen Saini (41.9k points)

4.20

LittleEndianBigEndian (1) [top](#)

#### 4.20.1 LittleEndianBigEndian: GATE CSE 2021 Set 2 | Question: 44 [top](#)

<https://gateoverflow.in/357496>



If the numerical value of a 2-byte unsigned integer on a little endian computer is 255 more than that on a big endian computer, which of the following choices represent(s) the unsigned integer on a little endian computer?

- A. 0x6665

### Answers: Little Endian Big Endian

#### 4.20.1 Little Endian Big Endian: GATE CSE 2021 Set 2 | Question: 44 [top](#)

<https://gateoverflow.in/357496>



- ✓ This question is poorly framed and has interpretation ambiguity. Refer to the discussion on this question in the below link :

<https://cs.stackexchange.com/questions/135713/representation-of-unsigned-integer-on-a-little-endian-big-endian-computer>

All kinds of “interpretations” are available in that discussion.

#### The following is my interpretation of the question :

It is asking “which of the following choices represent(s) the unsigned integer **on a little-endian computer?**”

Take Option “**0x6665**” :

It is saying that **0x6665** is the representation of an integer on a little-endian computer, so, it means that the original number must have been **0x6566**.

So, for the original number **0x6566** :

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- On little endian(LE) : **0x6665**
- On Big endian(BE) : **0x6566**

Clearly,  $LE = 255 + BE$

Similarly, for **0x0100**.

Take **0x0100** :

It is saying that **0x0100** is the representation of an integer on a little-endian computer, so, it means that the original number must have been **0x0001**.

So, for the number **0x0001** :

- On little endian(LE) : **0x0100**
- On Big endian(BE) : **0x0001**

Clearly,  $LE = 255 + BE$

Similarly for **0x4243** and **0x0001**, They do not satisfy “ $LE = 255 + BE$ ”, So, answer is option A,D.

Refer to Slide 26 in the below article :

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Nice Reference: <https://www.cs.utexas.edu/~byoung/cs429/slides2-bits-bytes.pdf>

#### Representing Integers:

```
int A = 15213;
int B = -15213;
long int C = 15213;
```

$$15213_{10} = 0011101101101101_2 = 3B6D_{16}$$

	Linux (little endian)	Alpha (little endian)	Sun (big endian)
A	6D 3B 00 00	6D 3B 00 00	00 00 3B 6D
B	93 C4 FF FF	93 C4 FF FF	FF FF C4 93
C	6D 3B 00 00 00 00 00 00	6D 3B 00 00 00 00 00 00	00 00 00 00 00 00 3B 6D

#### Byte Ordering Examples:

1. BigEndian: Most significant byte has lowest (first) address.
2. LittleEndian: Least significant byte has lowest address.

Example:

- Int variable **x** has 4-byte representation **0x01234567**.

- Address given by `&x` is `0x100`.

Big Endian:

<b>Address:</b>			0x100	0x101	0x102	0x103		
<b>Value:</b>	00	01	23	45	67	89	00	00

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Little Endian:

<b>Address:</b>			0x100	0x101	0x102	0x103		
<b>Value:</b>			67	45	23	01	00	00

Note that different people are having different interpretations of this question. I have asked this question on cs.StackExchange, and you can read the discussion in the below link :

<https://cs.stackexchange.com/questions/135713/representation-of-unsigned-integer-on-a-little-endian-big-endian-computer>

References



12 votes

-- Deepak Poonia (23.4k points)

4.21

Memory Interfacing (3) top

#### 4.21.1 Memory Interfacing: GATE CSE 1995 | Question: 2.2 top

<https://gateoverflow.in/2614>



The capacity of a memory unit is defined by the number of words multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of  $4K \times 16$ ?

- A. 10 address, 16 data lines
- B. 11 address, 8 data lines
- C. 12 address, 16 data lines
- D. 12 address, 12 data lines

gate1995 digital-logic memory-interfacing normal

Answer ↗

#### 4.21.2 Memory Interfacing: GATE CSE 2010 | Question: 7 top

<https://gateoverflow.in/2178>



The main memory unit with a capacity of 4 megabytes is built using  $1M \times 1$ -bit DRAM chips. Each DRAM chip has  $1K$  rows of cells with  $1K$  cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is

- A. 100 nanoseconds
- B.  $100 \times 2^{10}$  nanoseconds
- C.  $100 \times 2^{20}$  nanoseconds
- D.  $3200 \times 2^{20}$  nanoseconds

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gate2010-cse digital-logic memory-interfacing normal

Answer ↗

#### 4.21.3 Memory Interfacing: GATE IT 2005 | Question: 9 top

<https://gateoverflow.in/3754>



A dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec. What percentage of the memory cycle time is used for refreshing?

- A. 10
- B. 6.4
- C. 1
- D. 0.64

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## Answers: Memory Interfacing

4.21.1 Memory Interfacing: GATE CSE 1995 | Question: 2.2 [top](#)<https://gateoverflow.in/2614>

- ✓ ROM memory size =  $2^m \times n$

$m$  = no. of address lines  $n$  = no. of data lines

Given,  $4K \times 16$

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$$= 2^2 \times 2^{10} \times 16$$

$$= 2^{12} \times 16$$

Address lines = 12

Data lines = 16

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Correct Answer: C

 36 votes

-- Sanket\_ (3.1k points)

4.21.2 Memory Interfacing: GATE CSE 2010 | Question: 7 [top](#)<https://gateoverflow.in/2178>

- ✓ There are  $4*8 = 32$  DRAM chips to get 4MB from  $1M \times 1$ -bit chips. Now, all chips can be refreshed in parallel so do all cells in a row. So, the total time for refresh will be number of rows times the refresh time

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$$= 1K \times 100$$

$$= 100 \times 2^{10} \text{ nanoseconds}$$

Reference: <http://www.downloads.reactivemicro.com/Public/Electronics/DRAM/DRAM%20Refresh.pdf>

Correct Answer: B

References



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 60 votes

-- Arjun Suresh (332k points)

4.21.3 Memory Interfacing: GATE IT 2005 | Question: 9 [top](#)<https://gateoverflow.in/3754>

- ✓ Ans : (C) 1

In 1 ms refresh 100 times

$$\text{In } 64 \text{ ns - refresh } \frac{100}{10^{-3}} \times 64 \times 10^{-9} \text{ times}$$

$$= 10^5 \times 10^{-9} \times 64 = 64 \times 10^{-4} \text{ times}$$

In 1 memory cycle, refresh  $64 \times 10^{-4}$  times

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1 refresh takes 100 ns

$$64 \times 10^{-4} \text{ refreshes take } 100 \times 10^{-9} \times 64 \times 10^{-4}$$

$$= 64 \times 10^{-11} \text{ s}$$

$$\therefore \% \text{ refreshing time} = \frac{\text{refreshing time in cycle}}{\text{total time}} \times 100$$

$$= \frac{64 \times 10^{-11}}{64 \times 10^{-9}} \times 100$$

$$= \frac{1}{10^2} \times 100 = 1\%$$

65 votes

-- Afaque Ahmad (727 points)

4.22

Min No Gates (4) [top](#)

4.22.1 Min No Gates: GATE CSE 2000 | Question: 9 [top](#)

<https://gateoverflow.in/680>



Design a logic circuit to convert a single digit BCD number to the number modulo six as follows (Do not detect illegal input):

- A. Write the truth table for all bits. Label the input bits  $I_1, I_2, \dots$  with  $I_1$  as the least significant bit. Label the output bits  $R_1, R_2, \dots$  with  $R_1$  as the least significant bit. Use 1 to signify truth.
- B. Draw one circuit for each output bit using, *altogether*, two two-input AND gates, one two-input OR gate and two NOT gates.

[gate2000-cse](#) [digital-logic](#) [min-no-gates](#) [descriptive](#)

Answer

4.22.2 Min No Gates: GATE CSE 2004 | Question: 58 [top](#)

<https://gateoverflow.in/1053>



A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 by 0001, ..., 9 by 1001. A combinational circuit is to be designed which takes these 4 bits as input and outputs 1 if the digit  $\geq 5$ , and 0 otherwise. If only AND, OR and NOT gates may be used, what is the minimum number of gates required?

- A. 2
- B. 3
- C. 4
- D. 5

[gate2004-cse](#) [digital-logic](#) [normal](#) [min-no-gates](#)

Answer

4.22.3 Min No Gates: GATE CSE 2009 | Question: 6 [top](#)

<https://gateoverflow.in/1298>



What is the minimum number of gates required to implement the Boolean function  $(AB+C)$  if we have to use only 2-input NOR gates?

- A. 2
- B. 3
- C. 4
- D. 5

[gate2009-cse](#) [digital-logic](#) [min-no-gates](#) [normal](#)

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Answer

4.22.4 Min No Gates: GATE IT 2004 | Question: 8 [top](#)

<https://gateoverflow.in/3649>



What is the minimum number of NAND gates required to implement a 2-input EXCLUSIVE-OR function without using any other logic gate?

- A. 2
- B. 4
- C. 5
- D. 6

[gate2004-it](#) [digital-logic](#) [min-no-gates](#) [normal](#)

Answer

Answers: Min No Gates



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<b>I<sub>4</sub></b>	<b>I<sub>3</sub></b>	<b>I<sub>2</sub></b>	<b>I<sub>1</sub></b>		<b>R<sub>3</sub></b>	<b>R<sub>2</sub></b>	<b>R<sub>1</sub></b>
0	0	0	0	<b>0</b>	0	0	0
0	0	0	1	<b>1</b>	0	0	1
0	0	1	0	<b>2</b>	0	1	0
0	0	1	1	<b>3</b>	0	1	1
0	1	0	0	<b>4</b>	1	0	0
0	1	0	1	<b>5</b>	1	0	1
0	1	1	0	<b>6</b>	0	0	0
0	1	1	1	<b>7</b>	0	0	1
1	0	0	0	<b>8</b>	0	1	0
1	0	0	1	<b>9</b>	0	1	1

- $R_1 = I_1$
- $R_2 = I_2 \bar{I}_3 + I_4$
- $R_3 = I_3 \bar{I}_2$

This requires 2 NOT gates, 2 two-input AND gates and 1 two-input OR gate.

14 votes

-- Savir husen khan (305 points)

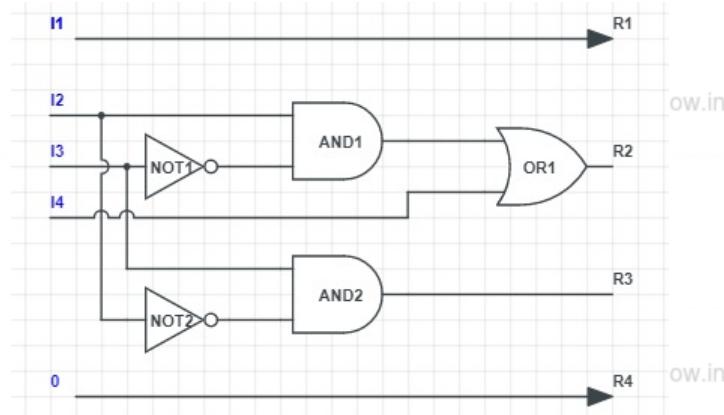
After using Don't care (10,11,12,13,14,15) and after K-Map simplification you will get

$$R_1 = I_1$$

$$R_2 = I_2 \cdot I_3' + I_4$$

$$R_3 = I_3 \cdot I_2'$$

$$R_4 = 0$$



Here, 2 input AND Gate used=2

2 input OR Gate used=1

NOT Gate used=2

11 votes

-- Krishn Kumar Gupta (1.1k points)



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✓ Answer should be (B). As according to question, truth table will be like:

A	B	C	D	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	don't care
1	0	1	1	don't care
1	1	0	0	don't care
1	1	0	1	don't care
1	1	1	0	don't care
1	1	1	1	don't care

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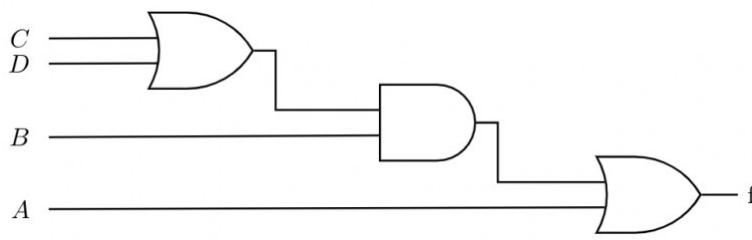
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Using this truth table we get 3 sub cube which are combined with following minterms  $A(8, 9, 10, 11, 12, 13, 14, 15)$ ,  $BD(5, 13, 7, 15)$  and  $BC(6, 7, 14, 15)$

$$\text{So, } f = A + BD + BC = A + B(C + D)$$

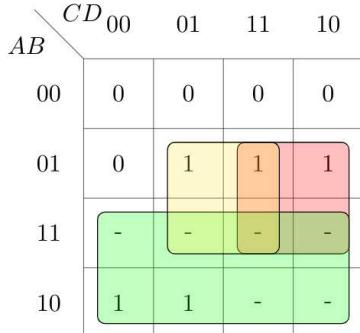
So, minimum gate required 2 OR gate and 1 AND gate = 3 minimum gates.



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42 votes

-- minal (13.1k points)

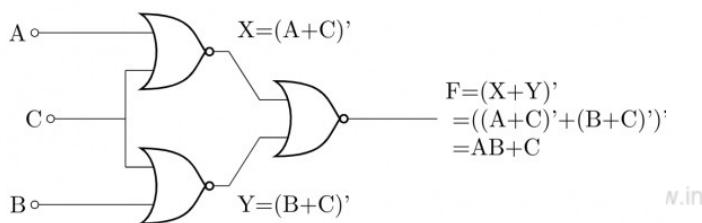
#### 4.22.3 Min No Gates: GATE CSE 2009 | Question: 6 top 5

https://gateoverflow.in/1298



Given boolean function is

$$\begin{aligned}
 f &= AB + C \\
 &= (A + C) \cdot (B + C) \\
 &= ((A + C)' + (B + C)')'
 \end{aligned}$$



N.in

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Therefore, 3 NOR gates required .

Correct Answer: *B*

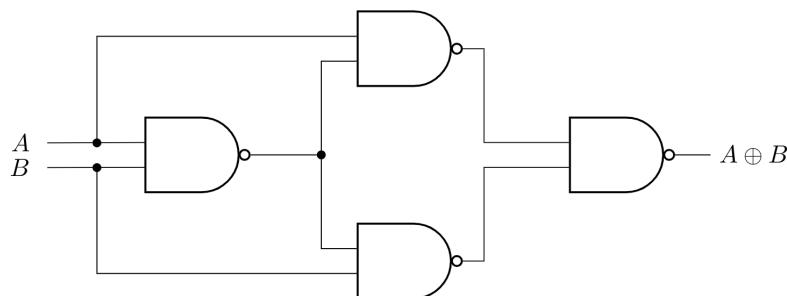
77 votes

-- Mithlesh Upadhyay (4.3k points)

#### 4.22.4 Min No Gates: GATE IT 2004 | Question: 8 top ↗



✓ Correct Option B 4.



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A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

20 votes

-- Manu Madhavan (827 points)

#### 4.23

#### Min Product Of Sums (2) top ↗



#### 4.23.1 Min Product Of Sums: GATE CSE 1990 | Question: 5-a top ↗

<https://gateoverflow.in/85396>

Find the minimum product of sums of the following expression

$$f = ABC + \bar{A} \bar{B} \bar{C}$$

gate1990 digital-logic boolean-algebra min-product-of-sums canonical-normal-form descriptive

Answer

#### 4.23.2 Min Product Of Sums: GATE CSE 2017 Set 2 | Question: 28 top ↗

<https://gateoverflow.in/118370>



Given  $f(w, x, y, z) = \Sigma_m(0, 1, 2, 3, 7, 8, 10) + \Sigma_d(5, 6, 11, 15)$ ; where  $d$  represents the 'don't-care' condition in Karnaugh maps. Which of the following is a minimum product-of-sums (POS) form of  $f(w, x, y, z)$ ?

- A.  $f = (\bar{w} + \bar{z})(\bar{x} + z)$
- B.  $f = (\bar{w} + z)(x + z)$
- C.  $f = (w + z)(\bar{x} + z)$
- D.  $f = (w + \bar{z})(\bar{x} + z)$

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gate2017-cse-set2 digital-logic min-product-of-sums

Answer

Answers: Min Product Of Sums



- ✓ Minimal POS

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		BC	00	01	11	10
		A	0	0	0	0
A	0	0	0	0		0
		1	0			0

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$$f = (\bar{A} + B)(A + \bar{B}) + (\bar{C})(\bar{B} + C)$$

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👉 26 votes

-- Lokesh Dafale (8.2k points)



- ✓ A.  $(\bar{x} + z)(\bar{z} + \bar{w})$

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		WX	00	01	11	10
		YZ	00	0	0	1
		00	1	d	0	0
		01	1	d	0	0
		11	1	1	d	d
		10	1	d	0	1

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👉 34 votes

-- Joker (1.6k points)



Three switching functions  $f_1$ ,  $f_2$  and  $f_3$  are expressed below as sum of minterms.

- $f_1(w, x, y, z) = \sum 0, 1, 2, 3, 5, 12$
- $f_2(w, x, y, z) = \sum 0, 1, 2, 10, 13, 14, 15$
- $f_3(w, x, y, z) = \sum 2, 4, 5, 8$

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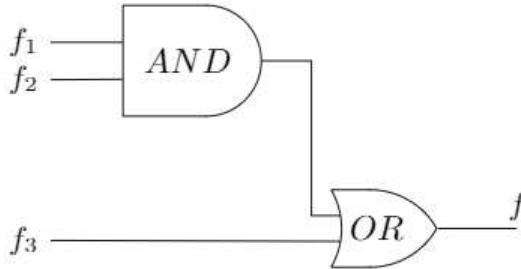
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Express the function  $f$  realised by the circuit shown in the below figure as the sum of minterms (in decimal notation).

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gate1988 descriptive digital-logic easy circuit-output min-sum-of-products-form

Answer ↗

#### 4.24.2 Min Sum Of Products Form: GATE CSE 1991 | Question: 5-b

↗ <https://gateoverflow.in/26437>



Find the minimum sum of products form of the logic function  $f(A, B, C, D) = \Sigma_m(0, 2, 8, 10, 15) + \Sigma_d(3, 11, 12, 14)$  where  $m$  and  $d$  represent minterm and don't care term respectively.

gate1991 digital-logic boolean-algebra min-sum-of-products-form descriptive

Answer ↗

#### 4.24.3 Min Sum Of Products Form: GATE CSE 1997 | Question: 71

↗ <https://gateoverflow.in/19701>



Let  $f = (\bar{w} + y)(\bar{x} + y)(w + \bar{x} + z)(\bar{w} + z)(\bar{x} + z)$

- A. Express  $f$  as the minimal sum of products. Write only the answer.
- B. If the output line is stuck at 0, for how many input combinations will the value of  $f$  be correct?

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gate1997 digital-logic min-sum-of-products-form numerical-answers

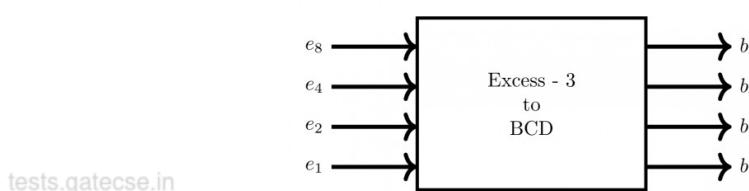
Answer ↗

#### 4.24.4 Min Sum Of Products Form: GATE CSE 2001 | Question: 10

↗ <https://gateoverflow.in/751>



- a. Is the 3-variable function  $f = \Sigma(0, 1, 2, 4)$  its self-dual? Justify your answer.
- b. Give a minimal product-of-sum form of the  $b$  output of the following excess-3 to BCD converter.



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gate2001-cse digital-logic normal descriptive min-sum-of-products-form

Answer ↗

#### 4.24.5 Min Sum Of Products Form: GATE CSE 2005 | Question: 18

↗ <https://gateoverflow.in/1354>



The switching expression corresponding to  $f(A, B, C, D) = \Sigma(1, 4, 5, 9, 11, 12)$  is:

- A.  $BC'D' + A'C'D + AB'D$
- B.  $ABC' + ACD + B'C'D$
- C.  $ACD' + A'BC' + AC'D'$
- D.  $A'BD + ACD' + BCD'$

Answer ↗

4.24.6 Min Sum Of Products Form: GATE CSE 2007 | Question: 9 top ↗↗ <https://gateoverflow.in/1207>

Consider the following Boolean function of four variables:

$$f(w, x, y, z) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14)$$

The function is

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- A. independent of one variables.
- B. independent of two variables.
- C. independent of three variables.
- D. dependent on all variables

Answer ↗

4.24.7 Min Sum Of Products Form: GATE CSE 2011 | Question: 14 top ↗↗ <https://gateoverflow.in/1216>

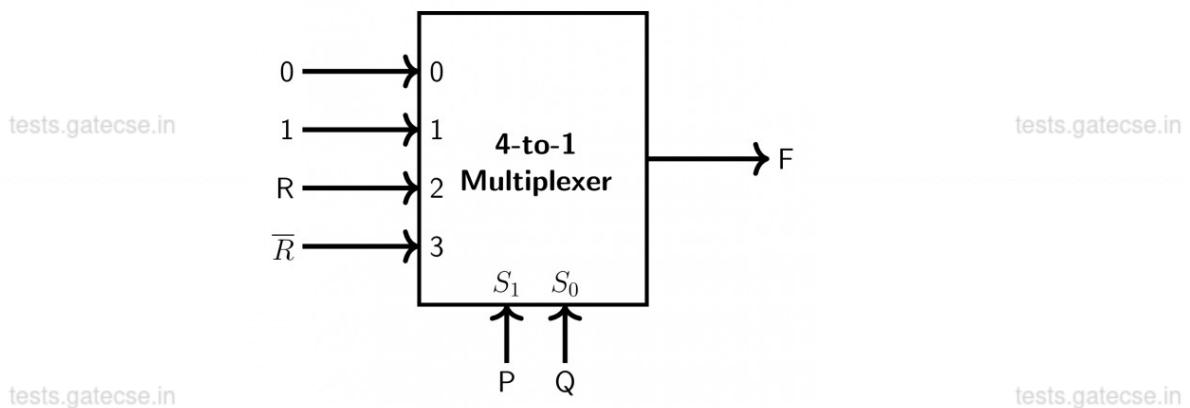
The simplified SOP (Sum of Product) from the Boolean expression

$$(P + \bar{Q} + \bar{R}) \cdot (P + \bar{Q} + R) \cdot (P + Q + \bar{R})$$

is

- A.  $(\bar{P} \cdot Q + \bar{R})$
- B.  $(P + \bar{Q} \cdot \bar{R})$
- C.  $(\bar{P} \cdot Q + R)$
- D.  $(P \cdot Q + R)$

Answer ↗

4.24.8 Min Sum Of Products Form: GATE CSE 2014 Set 1 | Question: 45 top ↗↗ <https://gateoverflow.in/1923>Consider the 4-to-1 multiplexer with two select lines  $S_1$  and  $S_0$  given below

The minimal sum-of-products form of the Boolean expression for the output F of the multiplexer is

- A.  $\bar{P}Q + Q\bar{R} + P\bar{Q}R$
- B.  $\bar{P}Q + \bar{P}Q\bar{R} + PQ\bar{R} + P\bar{Q}R$
- C.  $\bar{P}QR + \bar{P}Q\bar{R} + Q\bar{R} + P\bar{Q}R$

D.  $PQ\bar{R}$

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gate2014-cse-set1 digital-logic normal multiplexer min-sum-of-products-form

Answer ↗

4.24.9 Min Sum Of Products Form: GATE CSE 2014 Set 1 | Question: 7 [top ↵](#)



Consider the following Boolean expression for F:

$$F(P, Q, R, S) = PQ + \bar{P}QR + \bar{P}Q\bar{R}S$$

The minimal sum-of-products form of F is

- A.  $PQ + QR + QS$
- B.  $P + Q + R + S$
- C.  $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$
- D.  $\bar{P}R + \bar{R}\bar{P}S + P$

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gate2014-cse-set1 digital-logic normal min-sum-of-products-form

Answer ↗

4.24.10 Min Sum Of Products Form: GATE CSE 2014 Set 3 | Question: 7 [top ↵](#)



Consider the following minterm expression for F:

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$$F(P, Q, R, S) = \sum 0, 2, 5, 7, 8, 10, 13, 15$$

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The minterms 2, 7, 8 and 13 are 'do not care' terms. The minimal sum-of-products form for F is

- A.  $Q\bar{S} + \bar{Q}S$
- B.  $\bar{Q}\bar{S} + QS$
- C.  $Q\bar{R}\bar{S} + \bar{Q}R\bar{S} + Q\bar{R}S + QRS$
- D.  $\bar{P}Q\bar{S} + \bar{P}QS + PQS + P\bar{Q}\bar{S}$

gate2014-cse-set3 digital-logic min-sum-of-products-form normal

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Answer ↗

4.24.11 Min Sum Of Products Form: GATE CSE 2018 | Question: 49 [top ↵](#)



Consider the minterm list form of a Boolean function F given below.

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$$F(P, Q, R, S) = \Sigma m(0, 2, 5, 7, 9, 11) + d(3, 8, 10, 12, 14)$$

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Here, m denotes a minterm and d denotes a don't care term. The number of essential prime implicants of the function F is \_\_\_\_\_

gate2018-cse digital-logic min-sum-of-products-form numerical-answers

Answer ↗

4.24.12 Min Sum Of Products Form: GATE CSE 2021 Set 2 | Question: 52 [top ↵](#)



Consider a Boolean function  $f(w, x, y, z)$  such that

$$\begin{aligned}f(w, 0, 0, z) &= 1 \\f(1, x, 1, z) &= x + z \\f(w, 1, y, z) &= wz + y\end{aligned}$$

The number of literals in the minimal sum-of-products expression of f is \_\_\_\_\_

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Answer

**4.24.13 Min Sum Of Products Form: GATE IT 2008 | Question: 8** top ↗<https://gateoverflow.in/3268>

Consider the following Boolean function of four variables

$$f(A, B, C, D) = \Sigma(2, 3, 6, 7, 8, 9, 10, 11, 12, 13)$$

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The function is

- A. independent of one variable
- B. independent of two variables
- C. independent of three variable
- D. dependent on all the variables

Answer

**Answers: Min Sum Of Products Form****4.24.1 Min Sum Of Products Form: GATE CSE 1988 | Question: 2-v** top ↗<https://gateoverflow.in/91685>✓ Final output =  $\sum 0, 1, 2, 4, 5, 8$ 

- $f_1(w, x, y, z) = \sum 0, 1, 2, 3, 5, 12$
- $f_2(w, x, y, z) = \sum 0, 1, 2, 10, 13, 14, 15$
- $f_3(w, x, y, z) = \sum 2, 4, 5, 8$

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 $f_1$  AND  $f_2$  will give the common minterms -  $f_{12} = \sum 0, 1, 2$ .Now  $f_{12}$  OR  $f_3 = \sum 0, 1, 2, 4, 5, 8$ .

16 votes

-- kunal chalota (13.6k points)

**4.24.2 Min Sum Of Products Form: GATE CSE 1991 | Question: 5-b** top ↗<https://gateoverflow.in/26437>

✓

		CD	00	01	11	10
		AB	1		X	1
00	01	00				
		01				
11	10	11	X		1	X
		10	1		X	1

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The minimum SOP form of the logic function is given as :  $f(A, B, C, D) = B'D' + AC$ .

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18 votes

-- Kalpana Bhargav (2.5k points)

**4.24.3 Min Sum Of Products Form: GATE CSE 1997 | Question: 71** top ↗<https://gateoverflow.in/19701>

✓

	WX	00	01	11	10
YZ					
00	1	0	0	0	
01	1	0	0	0	
11	1	1	1	1	
10	1	0	0	0	

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Answer of question A:  $w'x' + yz$

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Answer of question B:

Stuck at 0, means output is fixed at 0 (No matter what the input is). We got 0 for 9 input combinations (Check K-Map). So, answer is **9**.

28 votes

-- Akash Kanase (36k points)

#### 4.24.4 Min Sum Of Products Form: GATE CSE 2001 | Question: 10 top

► <https://gateoverflow.in/751>



- ✓ There are two conditions for a function being self dual.

1. it should be a neutral function. (no. of minterms = no. of max terms)
2. no two mutually exclusive terms should be there like (0 – 7 are mutually exclusive 1 – 6, 2 – 5, 3 – 4) from these pairs only one should be there.

Clearly, there are 4 minterms, so number of minterms = no. of maxterms.

And second condition is also satisfied. So, it is a self dual function .

(b) Excess-3 to BCD

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Truth Table

Inputs				Outputs			
W	X	Y	Z	A	B	C	D
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	1	0	1
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

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MAPS:

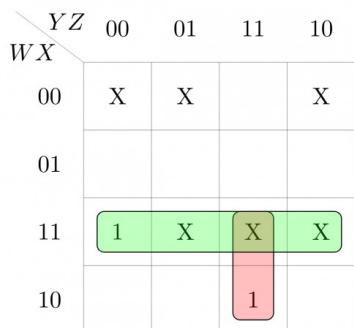
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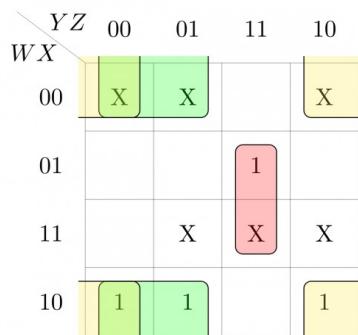
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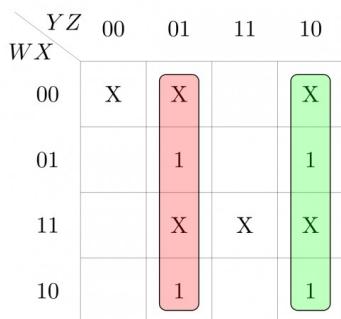
Map for  $A$   
 $A = WX + WYZ$



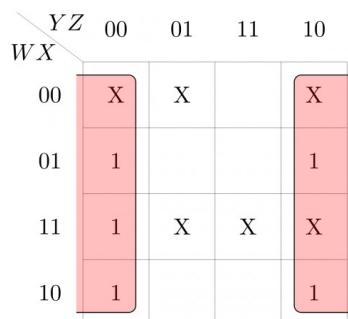
Map for  $B$   
 $B = X'Y' + XYZ + X'Z'$

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Map for  $C$   
 $C = Y'Z + ZY' = Y \oplus Z$



Map for  $D$   
 $D = Z'$

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👍 26 votes

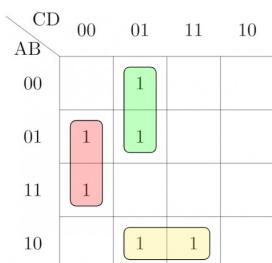
-- Ravi Singh (11.8k points)



4.24.5 Min Sum Of Products Form: GATE CSE 2005 | Question: 18 top 8

↗ <https://gateoverflow.in/1354>

✓ Answer is: [A]



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👍 15 votes

-- Desert\_Warrior (6k points)



4.24.6 Min Sum Of Products Form: GATE CSE 2007 | Question: 9 top 8

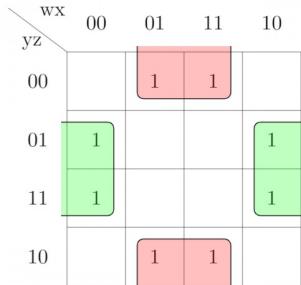
↗ <https://gateoverflow.in/1207>

✓ The K-map would be

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So, the minimized expression would be

$$x'z + xz' = x \oplus z.$$

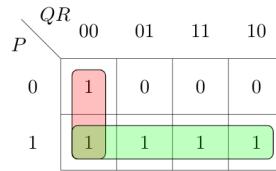
Option B.

21 votes

-- Arjun Suresh (332k points)

#### 4.24.7 Min Sum Of Products Form: GATE CSE 2011 | Question: 14 top ↗

► <https://gateoverflow.in/2116>



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K-map

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Answer is B

26 votes

-- Sona Praneeth Akula (3.4k points)

#### 4.24.8 Min Sum Of Products Form: GATE CSE 2014 Set 1 | Question: 45 top ↗

► <https://gateoverflow.in/1923>



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$S_0$  and  $S_1$  are used to select the input given to be given as output.

$S_0$	$S_1$	Output
0	0	0
0	1	1
1	0	R
1	1	R'

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 $S'_0S_1 + S_0S'_1R + S_0S_1R'$

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$$= P'Q + PQ'R + PQR'$$

$$= P'Q + PQR' + PQ'R$$

$$= Q(P' + PR') + PQ'R$$

$$= Q(P' + R') + PQ'R \quad (\because A + A'B = A + B) \\ = P'Q + QR' + PQ'R$$

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Option (A)

31 votes

-- Arjun Suresh (332k points)



		RS	00	01	11	10
		PQ	00	01	11	10
00	00	0	0	0	0	0
01	01	0	1	1	1	1
11	11	1	1	1	1	1
10	10	0	0	0	0	0

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$$\text{Minimal SOP} = PQ + QR + QS$$

Hence, **option A** is correct.

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👍 32 votes

-- Amar Vashishth (25.2k points)



- While putting the terms to K-map the 3<sup>rd</sup> and 4<sup>th</sup> columns are swapped so, do 3<sup>rd</sup> and 4th rows. So, term 2 is going to (0, 3) column instead of (0, 2), 8 is going to (3, 0) instead of (2, 0) etc.

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Solving this k-map gives **B**) as the answer.

Reference: <http://www.cs.uiuc.edu/class/sp08/cs231/lectures/04-Kmap.pdf>

#### References



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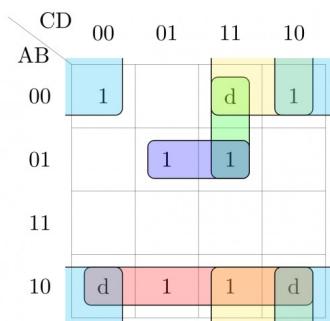
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👍 22 votes

-- Srinath Jayachandran (2.9k points)



✓



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**Implicant:** Any product term  $p$  in SOP form such that  $p \implies f$  is an implicant of  $f$ . So, we have 9 implicants for  $F$  here one corresponding to each 1 or  $d$  in the K-map.

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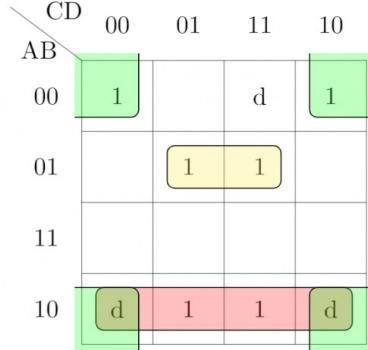
**Prime Implicant:** A minimal implicant is called a prime implicant (no extra literals than required). So, we have 5 prime implicants for  $F - \{\bar{A}BD, \bar{B}\bar{D}, A\bar{B}, \bar{A}CD, \bar{B}C\}$ . (for each 1 or  $d$  in  $K-map$  try to combine with near by 1s and do not care conditions)

**Essential Prime Implicant:** A prime implicant which cannot be replaced by any other for getting the output. i.e., essential prime implicants cover the output that no other combination of other prime implicants can. In K-map, this means an essential prime implicant must cover a 1 (**we do not consider don't care as essential**) which is not covered by any other prime implicant. Here, we have 3 essential prime implicants corresponding to 3 selections shown in the below  $K-map$ .

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So, 3 Essential Prime Implicants.

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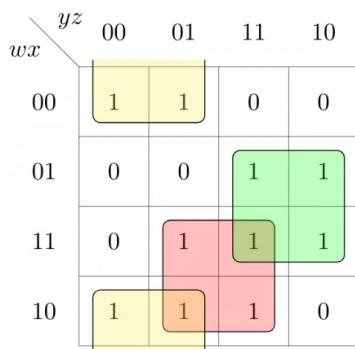
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41 votes

-- Digvijay (44.9k points)





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We can see 3 squares, so number of literals =  $3 \times 2 = 6$ . gateoverflow.in

8 votes

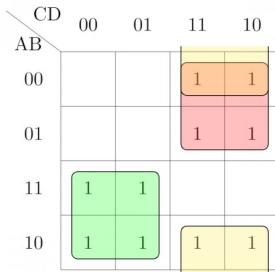
-- zxy123 (2.8k points)

#### 4.24.13 Min Sum Of Products Form: GATE IT 2008 | Question: 8 top

<https://gateoverflow.in/3268>



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$$\begin{aligned}
 (2, 3, 6, 7) & : \bar{A}C \\
 (2, 3, 10, 11) & : \bar{B}C \\
 (8, 9, 12, 13) & : A\bar{C} \\
 \hline
 y &= \bar{A}C + \bar{B}C + A\bar{C}
 \end{aligned}$$

Option A.

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21 votes

-- Aditi Tiwari (879 points)

#### 4.25

#### Multiplexer (13) top

#### 4.25.1 Multiplexer: GATE CSE 1987 | Question: 1-IV top

<https://gateoverflow.in/80193>



The output  $F$  of the below multiplexer circuit can be represented by

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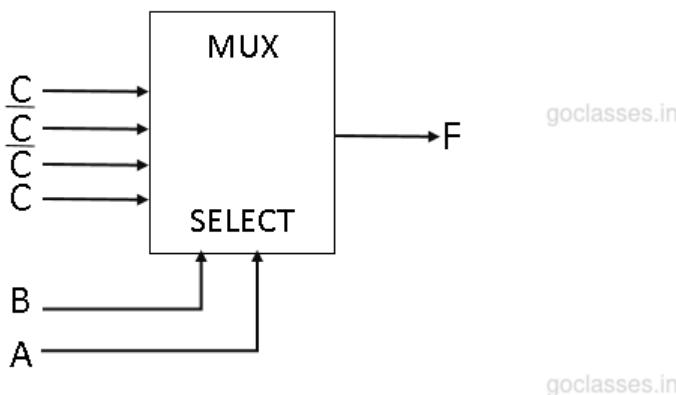
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- A.  $AB + B\bar{C} + \bar{C}A + \bar{B}\bar{C}$   
 B.  $A \oplus B \oplus C$   
 C.  $A \oplus B$   
 D.  $\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$

gate1987 digital-logic combinational-circuits multiplexer circuit-output

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Answer ↗

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4.25.2 Multiplexer: GATE CSE 1990 | Question: 5-b top ↗

↗ <https://gateoverflow.in/85398>



Show with the help of a block diagram how the Boolean function :

$$f = AB + BC + CA$$

can be realised using only a 4 : 1 multiplexer.

gate1990 descriptive digital-logic combinational-circuits multiplexer

Answer ↗

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4.25.3 Multiplexer: GATE CSE 1996 | Question: 2.22 top ↗

↗ <https://gateoverflow.in/2751>



Consider the circuit in figure.  $f$  implements

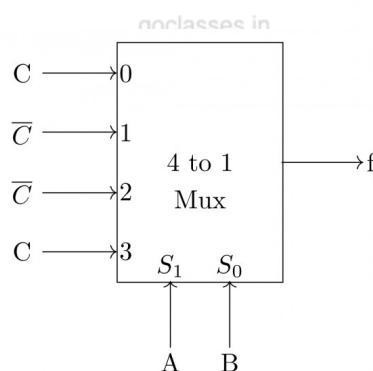
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- A.  $\overline{ABC} + \overline{ABC} + ABC$   
 B.  $A + B + C$   
 C.  $A \oplus B \oplus C$   
 D.  $AB + BC + CA$

gate1996 digital-logic circuit-output easy multiplexer

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## Answer ↗

### 4.25.4 Multiplexer: GATE CSE 1998 | Question: 1.14 top ↗

↗ <https://gateoverflow.in/1651>



A multiplexer with a  $4-bit$  data select input is a

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- A. 4 : 1 multiplexer
- B. 2 : 1 multiplexer
- C. 16 : 1 multiplexer
- D. 8 : 1 multiplexer

gate1998 digital-logic multiplexer easy

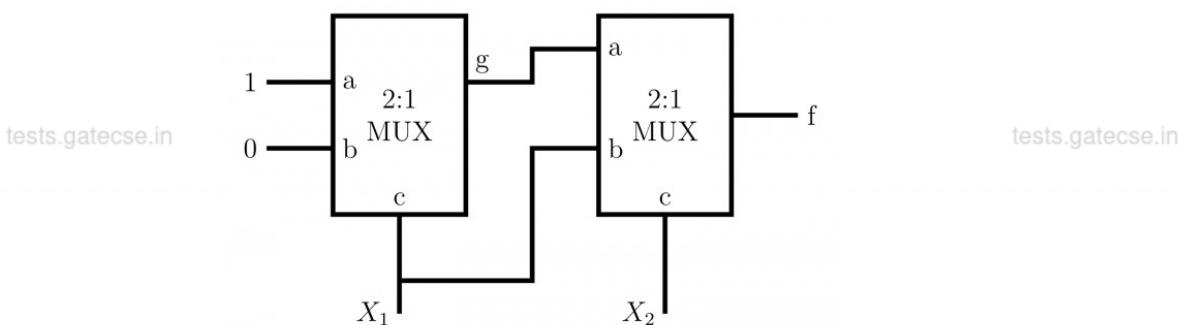
## Answer ↗

### 4.25.5 Multiplexer: GATE CSE 2001 | Question: 2.11 top ↗

↗ <https://gateoverflow.in/729>



Consider the circuit shown below. The output of a 2 : 1 MUX is given by the function  $(ac' + bc)$ .



Which of the following is true?

- A.  $f = X_1' + X_2$
- B.  $f = X_1'X_2 + X_1X_2'$
- C.  $f = X_1X_2 + X_1'X_2'$
- D.  $f = X_1 + X_2'$

gate2001-cse digital-logic normal multiplexer

## Answer ↗

### 4.25.6 Multiplexer: GATE CSE 2004 | Question: 60 top ↗

↗ <https://gateoverflow.in/1055>



Consider a multiplexer with  $X$  and  $Y$  as data inputs and  $Z$  as the control input.  $Z = 0$  selects input  $X$ , and  $Z = 1$  selects input  $Y$ . What are the connections required to realize the 2-variable Boolean function  $f = T + R$ , without using any additional hardware?

- A. R to X, 1 to Y, T to Z
- B. T to X, R to Y, T to Z
- C. T to X, R to Y, 0 to Z
- D. R to X, 0 to Y, T to Z

gate2004-cse digital-logic normal multiplexer

## Answer ↗

### 4.25.7 Multiplexer: GATE CSE 2007 | Question: 34 top ↗

↗ <https://gateoverflow.in/1232>



Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of  $n$  variables. What is the minimum size of the multiplexer needed?

- A.  $2^n$  line to 1 line
- B.  $2^{n+1}$  line to 1 line

C.  $2^{n-1}$  line to 1line

D.  $2^{n-2}$  line to 1line

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gate2007-cse digital-logic normal multiplexer

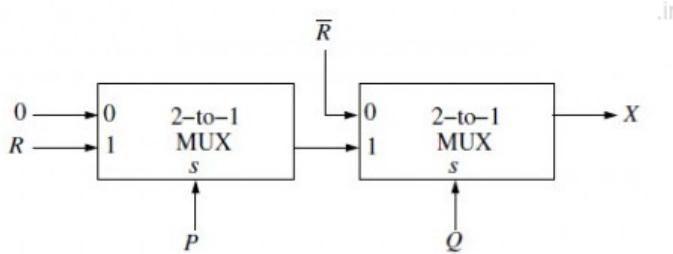
Answer ↗

4.25.8 Multiplexer: GATE CSE 2016 Set 1 | Question: 30 [top ↵](#)

↗ <https://gateoverflow.in/39722>



Consider the two cascade 2 to 1 multiplexers as shown in the figure .



The minimal sum of products form of the output  $X$  is

- A.  $\overline{P} \overline{Q} + PQR$
- B.  $\overline{P} Q + QR$
- C.  $PQ + \overline{P} \overline{Q} R$
- D.  $\overline{Q} \overline{R} + PQR$

gate2016-cse-set1 digital-logic multiplexer normal

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Answer ↗

4.25.9 Multiplexer: GATE CSE 2020 | Question: 19 [top ↵](#)

↗ <https://gateoverflow.in/333212>



A multiplexer is placed between a group of 32 registers and an accumulator to regulate data movement such that at any given point in time the content of only one register will move to the accumulator. The number of select lines needed for the multiplexer is

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Answer ↗

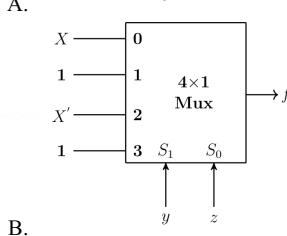
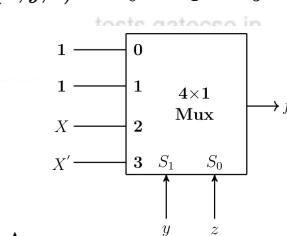
4.25.10 Multiplexer: GATE CSE 2021 Set 2 | Question: 5 [top ↵](#)

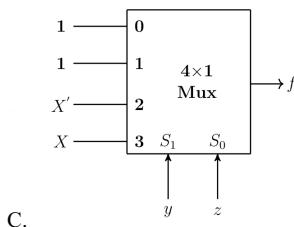
↗ <https://gateoverflow.in/357535>



Which one of the following circuits implements the Boolean function given below?

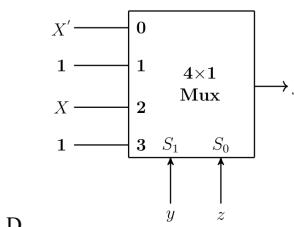
$f(x, y, z) = m_0 + m_1 + m_3 + m_4 + m_5 + m_6$  , where  $m_i$  is the  $i^{\text{th}}$  minterm.





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gate2021-cse-set2 digital-logic combinational-circuits multiplexer

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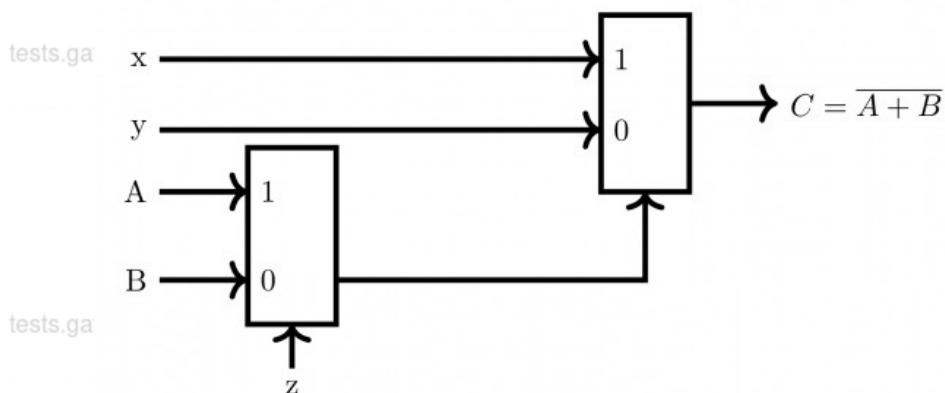
Answer ↗

#### 4.25.11 Multiplexer: GATE IT 2005 | Question: 48 top ↗

↗ <https://gateoverflow.in/3809>



The circuit shown below implements a 2-input NOR gate using two 2 – 4 MUX (control signal 1 selects the upper input). What are the values of signals  $x$ ,  $y$  and  $z$ ?



- A. 1, 0,  $B$
- B. 1, 0,  $A$
- C. 0, 1,  $B$
- D. 0, 1,  $A$

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gate2005-it digital-logic normal multiplexer

Answer ↗

#### 4.25.12 Multiplexer: GATE IT 2007 | Question: 8 top ↗

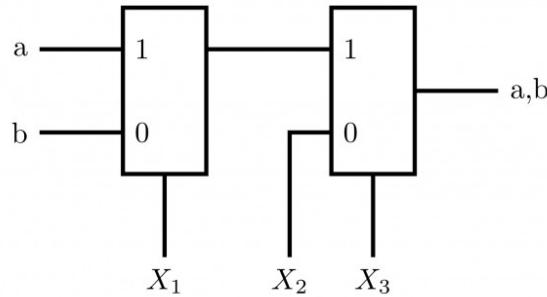
↗ <https://gateoverflow.in/3441>



The following circuit implements a two-input AND gate using two 2 – 1 multiplexers.

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What are the values of  $X_1, X_2, X_3$ ?

- A.  $X_1 = b, X_2 = 0, X_3 = a$
- B.  $X_1 = b, X_2 = 1, X_3 = b$
- C.  $X_1 = a, X_2 = b, X_3 = 1$
- D.  $X_1 = a, X_2 = 0, X_3 = b$

**Answer**

#### 4.25.13 Multiplexer: GATE1992-04-b [top](#)

<https://gateoverflow.in/17407>



A priority encoder accepts three input signals ( $A, B$  and  $C$ ) and produces a two-bit output ( $X_1, X_0$ ) corresponding to the highest priority active input signal. Assume  $A$  has the highest priority followed by  $B$  and  $C$  has the lowest priority. If none of the inputs are active the output should be 00, design the priority encoder using 4 : 1 multiplexers as the main components.

**Answer**

#### Answers: Multiplexer

#### 4.25.1 Multiplexer: GATE CSE 1987 | Question: 1-IV [top](#)

<https://gateoverflow.in/80193>



✓ Answer is B)

$$\begin{aligned}
 & A'B'C + AB'C' + A'BC' + ABC \\
 &= (A+B')(A'+B)C + A'BC' + AB'C' \\
 &= A \oplus B \oplus C
 \end{aligned}$$

18 votes

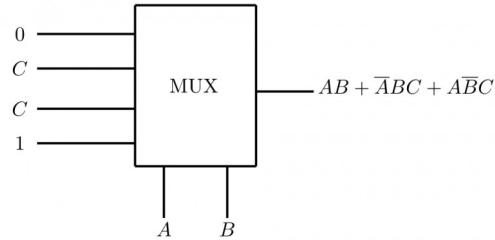
-- srestha (85.2k points)

#### 4.25.2 Multiplexer: GATE CSE 1990 | Question: 5-b [top](#)

<https://gateoverflow.in/85398>



✓  $AB + BC + CA = AB + A'BC + AB'C$



18 votes

-- kirti singh (2.6k points)



- $0 - C$  will be selected for  $A = 0, B = 0$ .
- $1 - \bar{C}$  will be selected for  $A = 0, B = 1$ .
- $2 - \bar{C}$  will be selected for  $A = 1, B = 0$ .
- $3 - C$  will be selected for  $A = 1, B = 1$ .

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$$\text{So, } f = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$

$$= \bar{A}(B \oplus C) + A(B \odot C)$$

$$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$$

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$$= A \oplus B \oplus C$$

Correct Answer: *C*

25 votes

-- Arjun Suresh (332k points)



- for  $n$  bit data select input

$$2^n : 1$$

for 4 it is 16 : 1

Correct Answer: *C*

27 votes

-- Bhagirathi Nayak (11.7k points)



$$g = X'_1$$

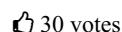
So,  $f = ac' + bc$

$$= X'_1X'_2 + X_1X_2$$

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30 votes

-- Arjun Suresh (332k points)



- Answer is **option A.**

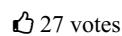
$$Z'X + ZY$$

$$\begin{aligned} \text{Put } Z = T, X = R, Y = 1 \text{ in } Z'X + ZY \\ = T'R + 1 * T \end{aligned}$$

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$$\begin{aligned} &= (T + T')(T + R) \\ &= T + R \end{aligned}$$



27 votes

-- Digvijay (44.9k points)



- $2^{n-1}$  to 1

We will map  $(n - 1)$  variables to select lines and 1 variable to input line

44 votes

-- Anurag Semwal (6.7k points)

**4.25.8 Multiplexer: GATE CSE 2016 Set 1 | Question: 30** top

<https://gateoverflow.in/39722>



- ✓ For 2 : 1 MUX, output  $Y = S'I_o + SI_1$   
So, output of MUX1,  $f_1 = P'0 + PR = PR$

Output of MUX2,  $f_2 = Q'R' + Qf_1 = Q'R' + PQR$

which is option **D**

43 votes

-- Monanshi Jain (7k points)

**4.25.9 Multiplexer: GATE CSE 2020 | Question: 19** top

<https://gateoverflow.in/333212>



- ✓ If there are ' $m$ ' select lines for a multiplexor, then it may have up to  $2^m$  input lines.

Given that there are 32 input lines. So, there must be  $\lceil \log_2 n \rceil = \lceil \log_2 32 \rceil = 5$  select lines.

12 votes

-- Shaik Masthan (50.4k points)

**4.25.10 Multiplexer: GATE CSE 2021 Set 2 | Question: 5** top

<https://gateoverflow.in/357535>



- ✓
  - $f(x, y, z) = m_0 + m_1 + m_3 + m_4 + m_5 + m_6$
  - $S_1 = y, S_0 = z$

Draw a small table as following and mark the min-terms in  $f$ .

	$I_0$	$I_1$	$I_2$	$I_3$
$\bar{x}$	0	1	2	3
$x$	4	5	6	7

$$I_0 = (\bar{x} + x) = 1 \quad (\text{both rows are marked})$$

$$I_1 = (\bar{x} + x) = 1 \quad (\text{both rows are marked})$$

$$I_2 = x \quad (\text{only row corresponding to } x \text{ is marked})$$

$$I_3 = \bar{x} \quad (\text{only row corresponding to } \bar{x} \text{ is marked})$$

**A is correct.**

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-- Nikhil Dhama (2.5k points)

2 votes

**4.25.11 Multiplexer: GATE IT 2005 | Question: 48** top

<https://gateoverflow.in/3809>



- ✓  $f = Az + B\bar{z}$  (As  $A$  will be selected when  $z$  is high).

So, next function will become  $g = xf + y\bar{f}$

$$= x(Az + B\bar{z}) + y(\overline{Az + B\bar{z}})$$

Putting  $x = 0, y = 1, z = A$ , we get  $g = \overline{AA + B\bar{A}} = \overline{A + B} \quad (\because A + B\bar{A} = A + B)$  and answer will become **D**

38 votes

-- John Carter (1.4k points)

**4.25.12 Multiplexer: GATE IT 2007 | Question: 8** top

<https://gateoverflow.in/3441>



- ✓ Answer: A

$$F = (bX'_1 + aX_1)X_3 + X_2X'_3$$

Put  $X_1 = b, X_2 = 0, X_3 = a$  to get  $F = ab$ .

1 26 votes

-- Rajarshi Sarkar (27.9k points)

#### 4.25.13 Multiplexer: GATE1992-04-b top

<https://gateoverflow.in/17407>



- ✓ MSB – Most Significant Bit  
LSB – Least Significant Bit

#### TRUTH TABLE

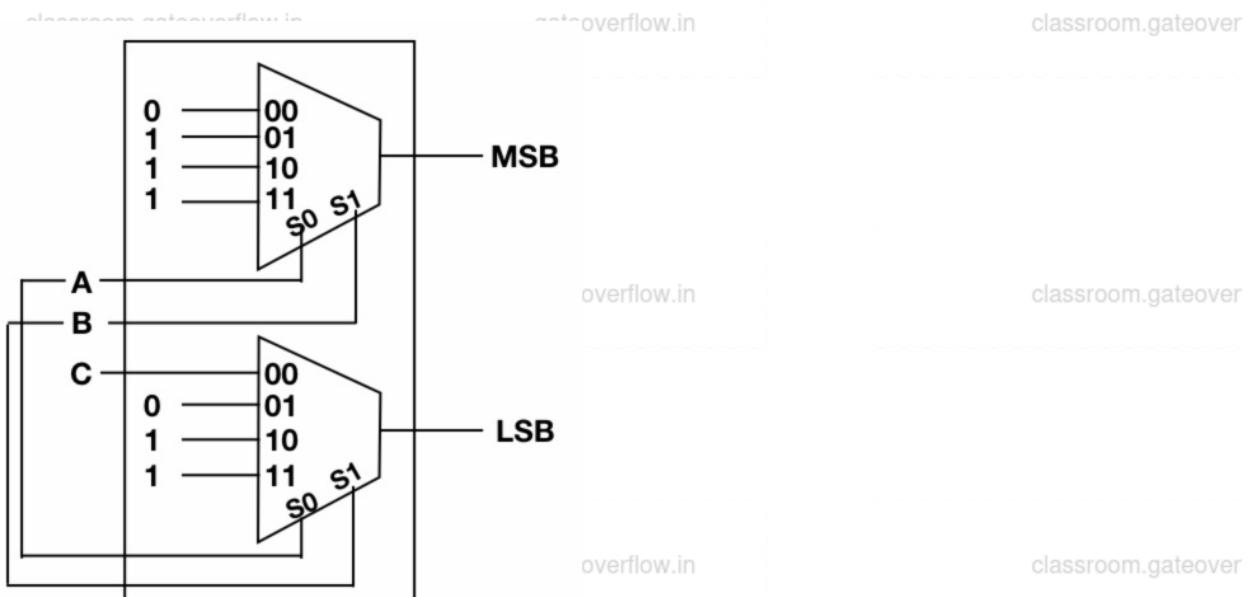
Inputs :  $A, B, C$

Outputs : MSB, LSB

$A$	$B$	$C$	MSB	LSB
0	0	0	0	0
0	0	1	0	1
0	1	$X$	1	0
1	$X$	$X$	1	1

$$\text{MSB} = A + B$$

$$\text{LSB} = A + \bar{B}C$$



It can be implemented using two  $4 \times 1$  Multiplexers.

1 34 votes

-- Anurag Pandey (10.5k points)

#### 4.26

#### Number Representation (51) top

##### 4.26.1 Number Representation: GATE CSE 1988 | Question: 2-vi top

<https://gateoverflow.in/91687>



Define the value of  $r$  in the following:  $\sqrt{(41)_r} = (7)_{10}$

gate1988 digital-logic normal number-representation descriptive

Answer ↗

##### 4.26.2 Number Representation: GATE CSE 1990 | Question: 1-viii top

<https://gateoverflow.in/87055>



The condition for overflow in the addition of two  $2's$  complement numbers in terms of the carry generated by the two most significant bits is \_\_\_\_\_.

gate1990 digital-logic number-representation fill-in-the-blanks

Answer 

4.26.3 Number Representation: GATE CSE 1991 | Question: 01-iii [top](#)

<https://gateoverflow.in/500>



Consider the number given by the decimal expression:

$$16^3 * 9 + 16^2 * 7 + 16 * 5 + 3$$

The number of 1's in the unsigned binary representation of the number is \_\_\_\_\_

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gate1991 digital-logic number-representation normal numerical-answers

Answer 

4.26.4 Number Representation: GATE CSE 1991 | Question: 01-v [top](#)

<https://gateoverflow.in/503>



When two 4-bit numbers  $A = a_3a_2a_1a_0$  and  $B = b_3b_2b_1b_0$  are multiplied, the bit  $c_1$  of the product  $C$  is given by \_\_\_\_\_

gate1991 digital-logic normal number-representation fill-in-the-blanks

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Answer 

4.26.5 Number Representation: GATE CSE 1992 | Question: 4-a [top](#)

<https://gateoverflow.in/583>



Consider addition in two's complement arithmetic. A carry from the most significant bit does not always correspond to an overflow. Explain what is the condition for overflow in two's complement arithmetic.

gate1992 digital-logic normal number-representation descriptive

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Answer 

4.26.6 Number Representation: GATE CSE 1993 | Question: 6.5 [top](#)

<https://gateoverflow.in/2286>



Convert the following numbers in the given bases into their equivalents in the desired bases:

- A.  $(110.101)_2 = (x)_{10}$   
B.  $(1118)_{10} = (y)_H$

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gate1993 digital-logic number-representation normal descriptive

Answer 

4.26.7 Number Representation: GATE CSE 1994 | Question: 2.7 [top](#)

<https://gateoverflow.in/2474>



Consider  $n$ -bit (including sign bit) 2's complement representation of integer numbers. The range of integer values,  $N$ , that can be represented is \_\_\_\_\_  $\leq N \leq$  \_\_\_\_\_.

gate1994 digital-logic number-representation easy fill-in-the-blanks

Answer 

4.26.8 Number Representation: GATE CSE 1995 | Question: 18 [top](#)

<https://gateoverflow.in/2655>



The following is an incomplete Pascal function to convert a given decimal integer (in the range  $-8$  to  $+7$ ) into a binary integer in 2's complement representation. Determine the expressions  $A$ ,  $B$ ,  $C$  that complete program.

```
function TWOSCOMPS(N:integer):integer;
var
  REM, EXPONENT:integer;
  BINARY :integer;
begin
  if (N>=-8) and (N<=+7) then
  begin
    if N<0 then
      N:=-A;
    BINARY:=0;
    EXPONENT:=1;
    while N<>0 do
```

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```

begin ~
    REM:=N mod 2;
    BINARY:=BINARY + B*EXPONENT;
    EXPONENT:=EXPONENT*10;
    N:=C
end
TWOSCOMP:=BINARY
end;

```

gate1995 digital-logic number-representation normal descriptive

Answer 

#### 4.26.9 Number Representation: GATE CSE 1995 | Question: 2.12, ISRO2015-9 [top](#)

<https://gateoverflow.in/2624>



The number of 1's in the binary representation of  $(3 * 4096 + 15 * 256 + 5 * 16 + 3)$  are:

- A. 8
- B. 9
- C. 10
- D. 12

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gate1995 digital-logic number-representation normal isro2015

Answer 

#### 4.26.10 Number Representation: GATE CSE 1996 | Question: 1.25 [top](#)

<https://gateoverflow.in/2729>



Consider the following floating-point number representation.

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31	24	23	0
Exponent	Mantissa		

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The exponent is in 2's complement representation and the mantissa is in the sign-magnitude representation. The range of the magnitude of the normalized numbers in this representation is

- A. 0 to 1
- B. 0.5 to 1
- C.  $2^{-23}$  to  $0.5$
- D. 0.5 to  $(1 - 2^{-23})$

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gate1996 digital-logic number-representation normal

Answer 

#### 4.26.11 Number Representation: GATE CSE 1997 | Question: 5.4 [top](#)

<https://gateoverflow.in/2255>



Given  $\sqrt{(224)_r} = (13)_r$ .

The value of the radix  $r$  is:

- A. 10
- B. 8
- C. 5
- D. 6

gate1997 digital-logic number-representation normal

Answer 

#### 4.26.12 Number Representation: GATE CSE 1998 | Question: 1.17 [top](#)

<https://gateoverflow.in/1654>



The octal representation of an integer is  $(342)_8$ . If this were to be treated as an eight-bit integer in an 8085 based computer, its decimal equivalent is

- A. 226
- B. -98
- C. 76

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D. -30

gate1998 digital-logic number-representation normal 8085

Answer ↗

4.26.13 Number Representation: GATE CSE 1998 | Question: 2.20 top ⓘ

↗ <https://gateoverflow.in/1693>



Suppose the domain set of an attribute consists of signed four digit numbers. What is the percentage of reduction in storage space of this attribute if it is stored as an integer rather than in character form?

- A. 80%
- B. 20%
- C. 60%
- D. 40%

gate1998 digital-logic number-representation normal

Answer ↗

4.26.14 Number Representation: GATE CSE 1999 | Question: 2.17 top ⓘ

↗ <https://gateoverflow.in/1495>



Zero has two representations in

- A. Sign-magnitude
- B. 2's complement
- C. 1's complement
- D. None of the above

gate1999 digital-logic number-representation easy multiple-selects

Answer ↗

4.26.15 Number Representation: GATE CSE 2000 | Question: 1.6 top ⓘ

↗ <https://gateoverflow.in/629>



The number 43 in 2's complement representation is

- A. 01010101
- B. 11010101
- C. 00101011
- D. 10101011

gate2000-cse digital-logic number-representation easy

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Answer ↗

4.26.16 Number Representation: GATE CSE 2000 | Question: 2.14 top ⓘ

↗ <https://gateoverflow.in/661>



Consider the values of  $A = 2.0 \times 10^{30}$ ,  $B = -2.0 \times 10^{30}$ ,  $C = 1.0$ , and the sequence

X := A + B	Y := A + C
X := X + C	Y := Y + B

executed on a computer where floating point numbers are represented with 32 bits. The values for  $X$  and  $Y$  will be

- A.  $X = 1.0, Y = 1.0$
- B.  $X = 1.0, Y = 0.0$
- C.  $X = 0.0, Y = 1.0$
- D.  $X = 0.0, Y = 0.0$

gate2000-cse digital-logic number-representation normal

Answer ↗

4.26.17 Number Representation: GATE CSE 2001 | Question: 2.10 top ⓘ

↗ <https://gateoverflow.in/728>



The 2's complement representation of  $(-539)_{10}$  in hexadecimal is

- A. ABE
- B. DBC
- C. DE5
- D. 9E7

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gate2001-cse digital-logic number-representation easy

Answer 

**4.26.18 Number Representation: GATE CSE 2002 | Question: 1.14** top ↗

<https://gateoverflow.in/818>



The decimal value 0.25

- A. is equivalent to the binary value 0.1
- B. is equivalent to the binary value 0.01
- C. is equivalent to the binary value 0.00111
- D. cannot be represented precisely in binary

gate2002-cse digital-logic number-representation easy

Answer 

**4.26.19 Number Representation: GATE CSE 2002 | Question: 1.15** top ↗

<https://gateoverflow.in/819>



The 2's complement representation of the decimal value  $-15$  is

- A. 1111
- B. 11111
- C. 111111
- D. 10001

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gate2002-cse digital-logic number-representation easy

Answer 

**4.26.20 Number Representation: GATE CSE 2002 | Question: 1.16** top ↗

<https://gateoverflow.in/821>



Sign extension is a step in

- A. floating point multiplication
- B. signed 16 bit integer addition
- C. arithmetic left shift
- D. converting a signed integer from one size to another

gate2002-cse digital-logic easy number-representation

Answer 

**4.26.21 Number Representation: GATE CSE 2002 | Question: 1.21** top ↗

<https://gateoverflow.in/826>



In 2's complement addition, overflow

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- A. is flagged whenever there is carry from sign bit addition
- B. cannot occur when a positive value is added to a negative value
- C. is flagged when the carries from sign bit and previous bit match
- D. None of the above

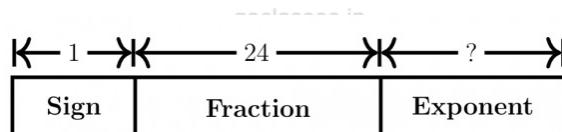
gate2002-cse digital-logic number-representation normal

Answer 



Consider the following 32-bit floating-point representation scheme as shown in the format below. A value is specified by 3 fields, a one bit sign field (with 0 for positive and 1 for negative values), a 24 bit fraction field (with the binary point is at the left end of the fraction bits), and a 7 bit exponent field (in excess-64 signed integer representation, with 16 is the base of exponentiation). The sign bit is the most significant bit.

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- It is required to represent the decimal value  $-7.5$  as a normalized floating point number in the given format. Derive the values of the various fields. Express your final answer in the hexadecimal.
- What is the largest value that can be represented using this format? Express your answer as the nearest power of 10.

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Answer



Assuming all numbers are in  $2^s$  complement representation, which of the following numbers is divisible by 11111011?

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- A. 11100111
- B. 11100100
- C. 11010111
- D. 11011011

[gate2003-cse](#) [digital-logic](#) [number-representation](#) [normal](#)

Answer



If  $73_x$  (in base- $x$  number system) is equal to  $54_y$  (in base  $y$ -number system), the possible values of  $x$  and  $y$  are

- A. 8, 16
- B. 10, 12
- C. 9, 13
- D. 8, 11

[gate2004-cse](#) [digital-logic](#) [number-representation](#) [easy](#)

Answer



What is the result of evaluating the following two expressions using three-digit floating point arithmetic with rounding?

(113. + -111.)

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113. + (-111. + 7.51)

- A. 9.51 and 10.0 respectively
- B. 10.0 and 9.51 respectively
- C. 9.51 and 9.51 respectively
- D. 10.0 and 10.0 respectively

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[gate2004-cse](#) [digital-logic](#) [number-representation](#) [normal](#)

Answer

**4.26.26 Number Representation: GATE CSE 2004 | Question: 66**<https://gateoverflow.in/1060>

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Let  $A = 11111010$  and  $B = 00001010$  be two 8-bit 2's complement numbers. Their product in 2's complement is

- A. 11000100
- B. 10011100
- C. 10100101
- D. 11010101

gate2004-cse digital-logic number-representation easy

Answer

**4.26.27 Number Representation: GATE CSE 2005 | Question: 16, ISRO2009-18, ISRO2015-2**<https://gateoverflow.in/1352>

The range of integers that can be represented by an  $n$  bit 2's complement number system is:

- A.  $-2^{n-1}$  to  $(2^{n-1} - 1)$
- B.  $-(2^{n-1} - 1)$  to  $(2^{n-1} - 1)$
- C.  $-2^{n-1}$  to  $2^{n-1}$
- D.  $-(2^{n-1} + 1)$  to  $(2^{n-1} - 1)$

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gate2005-cse digital-logic number-representation easy isro2009 isro2015

Answer

**4.26.28 Number Representation: GATE CSE 2005 | Question: 17**<https://gateoverflow.in/1353>

The hexadecimal representation of  $(657)_8$  is:

- A. 1AF
- B. D78
- C. D71
- D. 32F

gate2005-cse digital-logic number-representation easy

Answer

**4.26.29 Number Representation: GATE CSE 2006 | Question: 39**<https://gateoverflow.in/1815>

We consider the addition of two 2's complement numbers  $b_{n-1}b_{n-2}\dots b_0$  and  $a_{n-1}a_{n-2}\dots a_0$ . A binary adder for adding unsigned binary numbers is used to add the two numbers. The sum is denoted by  $c_{n-1}c_{n-2}\dots c_0$  and the carry-out by  $c_{out}$ . Which one of the following options correctly identifies the overflow condition?

- A.  $c_{out} \left( \overline{a_{n-1}} \oplus \overline{b_{n-1}} \right)$
- B.  $a_{n-1}b_{n-1}\overline{c_{n-1}} + \overline{a_{n-1}}\overline{b_{n-1}}c_{n-1}$
- C.  $c_{out} \oplus c_{n-1}$
- D.  $a_{n-1} \oplus b_{n-1} \oplus c_{n-1}$

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gate2006-cse digital-logic number-representation normal

Answer

**4.26.30 Number Representation: GATE CSE 2008 | Question: 6**<https://gateoverflow.in/404>

Let  $r$  denote number system radix. The only value(s) of  $r$  that satisfy the equation  $\sqrt{121_r} = 11_r$ , is/are

- A. decimal 10
- B. decimal 11
- C. decimal 10 and 11
- D. any value > 2

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Answer

**4.26.31 Number Representation: GATE CSE 2009 | Question: 5, ISRO2017-57** top ↗<https://gateoverflow.in/1297>

$(1217)_8$  is equivalent to

- A.  $(1217)_{16}$
- B.  $(028F)_{16}$
- C.  $(2297)_{10}$
- D.  $(0B17)_{16}$

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Answer

**4.26.32 Number Representation: GATE CSE 2010 | Question: 8** top ↗<https://gateoverflow.in/2179>

$P$  is a 16-bit signed integer. The 2's complement representation of  $P$  is  $(F87B)_{16}$ . The 2's complement representation of  $8 \times P$  is

- A.  $(C3D8)_{16}$
- B.  $(187B)_{16}$
- C.  $(F878)_{16}$
- D.  $(987B)_{16}$

Answer

**4.26.33 Number Representation: GATE CSE 2013 | Question: 4** top ↗<https://gateoverflow.in/1413>

The smallest integer that can be represented by an  $8 - bit$  number in  $2^l s$  complement form is

- A.  $-256$
- B.  $-128$
- C.  $-127$
- D.  $0$

Answer

**4.26.34 Number Representation: GATE CSE 2014 Set 1 | Question: 8** top ↗<https://gateoverflow.in/1766>

The base (or radix) of the number system such that the following equation holds is \_\_\_\_\_.

$$\frac{312}{20} = 13.1$$

Answer

**4.26.35 Number Representation: GATE CSE 2014 Set 2 | Question: 8** top ↗<https://gateoverflow.in/1961>

Consider the equation  $(123)_5 = (x8)_y$  with  $x$  and  $y$  as unknown. The number of possible solutions is \_\_\_\_\_.

Answer

**4.26.36 Number Representation: GATE CSE 2015 Set 3 | Question: 35** top ↗<https://gateoverflow.in/8494>

Consider the equation  $(43)_x = (y3)_8$  where  $x$  and  $y$  are unknown. The number of possible solutions is \_\_\_\_\_

gate2015-cse-set3 digital-logic number-representation normal numerical-answers

Answer 

4.26.37 Number Representation: GATE CSE 2016 Set 1 | Question: 07 [top](#) 

<https://gateoverflow.in/39649>

The  $16-bit$   $2's$  complement representation of an integer is 1111 1111 1111 0101; its decimal representation is \_\_\_\_\_

gate2016-cse-set1 digital-logic number-representation normal numerical-answers

Answer 

4.26.38 Number Representation: GATE CSE 2016 Set 2 | Question: 09 [top](#) 

<https://gateoverflow.in/3956>

Let  $X$  be the number of distinct 16-bit integers in  $2's$  complement representation. Let  $Y$  be the number of distinct 16-bit integers in sign magnitude representation Then  $X - Y$  is \_\_\_\_\_.

gate2016-cse-set2 digital-logic number-representation normal numerical-answers

Answer 

4.26.39 Number Representation: GATE CSE 2017 Set 1 | Question: 9 [top](#) 

<https://gateoverflow.in/118289>

When two 8-bit numbers  $A_7 \dots A_0$  and  $B_7 \dots B_0$  in  $2's$  complement representation (with  $A_0$  and  $B_0$  as the least significant bits) are added using a **ripple-carry adder**, the sum bits obtained are  $S_7 \dots S_0$  and the carry bits are  $C_7 \dots C_0$ . An overflow is said to have occurred if \_\_\_\_\_

- A. the carry bit  $C_7$  is 1
- B. all the carry bits  $(C_7, \dots, C_0)$  are 1
- C.  $(A_7 \cdot B_7 \cdot S_7 + A_7 \cdot B_7 \cdot S_7)$  is 1
- D.  $(A_0 \cdot B_0 \cdot S_0 + A_0 \cdot B_0 \cdot S_0)$  is 1

gate2017-cse-set1 digital-logic number-representation

Answer 

4.26.40 Number Representation: GATE CSE 2017 Set 2 | Question: 1 [top](#) 

<https://gateoverflow.in/118337>

The representation of the value of a  $16-bit$  unsigned integer  $X$  in hexadecimal number system is  $BCA9$ . The representation of the value of  $X$  in octal number system is \_\_\_\_\_

- A. 571244
- B. 736251
- C. 571247
- D. 136251

gate2017-cse-set2 digital-logic number-representation

Answer 

4.26.41 Number Representation: GATE CSE 2019 | Question: 22 [top](#) 

<https://gateoverflow.in/302826>

Two numbers are chosen independently and uniformly at random from the set  $\{1, 2, \dots, 13\}$ .

The probability (rounded off to 3 decimal places) that their  $4-bit$  (unsigned) binary representations have the same most significant bit is \_\_\_\_\_.

gate2019-cse numerical-answers digital-logic number-representation probability goclasses.in

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Answer 

**4.26.42 Number Representation: GATE CSE 2019 | Question: 4** top ↗↗ <https://gateoverflow.in/302844>

In 16-bit 2's complement representation, the decimal number  $-28$  is:

- A. 1111 1111 0001 1100
- B. 0000 0000 1110 0100
- C. 1111 1111 1110 0100
- D. 1000 0000 1110 0100

goclasses.intests.gatecse.ingate2019-cse digital-logic number-representation**Answer ↗****4.26.43 Number Representation: GATE CSE 2019 | Question: 8** top ↗↗ <https://gateoverflow.in/302840>

Consider  $Z = X - Y$  where  $X, Y$  and  $Z$  are all in sign-magnitude form.  $X$  and  $Y$  are each represented in  $n$  bits. To avoid overflow, the representation of  $Z$  would require a minimum of:

- A.  $n$  bits
- B.  $n - 1$  bits
- C.  $n + 1$  bits
- D.  $n + 2$  bits

goclasses.intests.gatecse.ingate2019-cse digital-logic number-representation**Answer ↗****4.26.44 Number Representation: GATE CSE 2021 Set 1 | Question: 6** top ↗↗ <https://gateoverflow.in/357526>

Let the representation of a number in base 3 be 210. What is the hexadecimal representation of the number?

- A. 15
- B. 21
- C. D2
- D. 528

tests.gatecse.ingoclasses.intests.gatecse.ingate2021-cse-set1 digital-logic number-representation normal**Answer ↗****4.26.45 Number Representation: GATE CSE 2021 Set 2 | Question: 18** top ↗↗ <https://gateoverflow.in/357522>

If  $x$  and  $y$  are two decimal digits and  $(0.1101)_2 = (0.8xy5)_{10}$ , the decimal value of  $x + y$  is \_\_\_\_\_

tests.gatecse.ingate2021-cse-set2 numerical-answers digital-logic number-representation**Answer ↗****4.26.46 Number Representation: GATE IT 2004 | Question: 42** top ↗↗ <https://gateoverflow.in/3685>

Using a 4-bit 2's complement arithmetic, which of the following additions will result in an overflow?

- i. 1100 + 1100
- ii. 0011 + 0111
- iii. 1111 + 0111

- A. i only
- B. ii only
- C. iii only
- D. i and iii only

goclasses.intests.gatecse.ingate2004-it digital-logic number-representation normal**Answer ↗**



The number  $(123456)_8$  is equivalent to

- A.  $(A72E)_{16}$  and  $(22130232)_4$
- B.  $(A72E)_{16}$  and  $(22131122)_4$
- C.  $(A73E)_{16}$  and  $(22130232)_4$
- D.  $(A62E)_{16}$  and  $(22120232)_4$

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Answer



$(34.4)_8 \times (23.4)_8$  evaluates to

- A.  $(1053.6)_8$
- B.  $(1053.2)_8$
- C.  $(1024.2)_8$
- D. None of these

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[gate2005-it](#) [digital-logic](#) [number-representation](#) [normal](#)

Answer



The addition of 4-bit, two's complement, binary numbers 1101 and 0100 results in

- A. 0001 and an overflow
- B. 1001 and no overflow
- C. 0001 and no overflow
- D. 1001 and an overflow

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[gate2006-it](#) [digital-logic](#) [number-representation](#) [normal](#) [isro2009](#)

Answer



$$(C012.25)_H - (10111001110.101)_B =$$

- A.  $(135103.412)_o$
- B.  $(564411.412)_o$
- C.  $(564411.205)_o$
- D.  $(135103.205)_o$

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Answer



A processor that has the carry, overflow and sign flag bits as part of its program status word (PSW) performs addition of the following two 2's complement numbers 01001101 and 11101001. After the execution of this addition operation, the status of the carry, overflow and sign flags, respectively will be:

- A. 1, 1, 0
- B. 1, 0, 0
- C. 0, 1, 0
- D. 1, 0, 1

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## Answer

### Answers: Number Representation

#### 4.26.1 Number Representation: GATE CSE 1988 | Question: 2-vi [top](#)

<https://gateoverflow.in/31687>



- ✓  $\sqrt{41_r} = 7_{10}$

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Squaring both sides we get

$$41_r = 49_{10}$$

$$\Rightarrow 4r + 1 = 10 \times 4 + 9$$

$$\Rightarrow 4r = 48$$

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$$\Rightarrow r = 12.$$

23 votes

-- kunal chalota (13.6k points)

#### 4.26.2 Number Representation: GATE CSE 1990 | Question: 1-viii [top](#)

<https://gateoverflow.in/8705>



- ✓ The condition for overflow in the addition of two 2's complement numbers in terms of the carry generated by the two most significant bits is when carry on MSB but not From MSB, or Carry from MSB but not on MSB. i.e.,

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$$C_{out} \oplus C_{n-1} = 1.$$

i.e. For overflow to happen during addition of two numbers in 2's complement form



**They must have same sign and result is of opposite sign** Overflow occurs if 1.  $(+A) + (+B) = -C$  2.  $(-A) + (-B) = +C$

PS: Overflow is useful for signed numbers and useless for unsigned numbers

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21 votes

-- Prashant Singh (47.2k points)

#### 4.26.3 Number Representation: GATE CSE 1991 | Question: 01-iii [top](#)

<https://gateoverflow.in/500>



- ✓ The hex representation of given no. is  $(9753)_{16}$

Its binary representation is  $(1001011101010011)_2$

The no. of 1's is 9.

38 votes

-- Keith Kr (4.5k points)

#### 4.26.4 Number Representation: GATE CSE 1991 | Question: 01-v [top](#)

<https://gateoverflow.in/503>



	$a_3$	$a_2$	$a_1$	$a_0$
$b_3$	$a_3 b_0$	$a_2 b_0$	$a_1 b_0$	$a_0 b_0$
$a_3 b_1$	$a_2 b_1$	$a_1 b_1$	$a_0 b_1$	—
$a_3 b_2$	$a_2 b_2$	$a_1 b_2$	$a_0 b_2$	—
$a_3 b_3$	$a_2 b_3$	$a_1 b_3$	$a_0 b_3$	—
$c_7$	$c_6$	$c_5$	$c_4$	$c_3$
	$c_2$	$c_1$	$c_0$	

$$c_1 = b_1 a_0 \oplus a_1 b_0$$

55 votes

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-- Pooja Palod (24.1k points)

**4.26.5 Number Representation: GATE CSE 1992 | Question: 4-a**<https://gateoverflow.in/583>

- ✓ XOR of  $C_{in}$  with  $C_{out}$  of the MSB position.

**17 votes**

-- Amar Vashishth (25.2k points)

**4.26.6 Number Representation: GATE CSE 1993 | Question: 6.5**<https://gateoverflow.in/2286>

- ✓
  - $1 * 2^2 + 1 * 2^1 + 0 * 2^0 + 1 * 2^{-1} + 0 * 2^{-2} + 1 * 2^{-3} = 6.625$
  - $1118 \bmod 16 = 14$ , quotient = 69

$$\begin{aligned} 69 \bmod 16 &= 5, \text{ quotient } = 4 \\ 4 \bmod 16 &= 4. \end{aligned}$$

Writing the mods in the reverse order (in hex) gives  $(45E)_H$ .

Both can be done using a calculator also.

**21 votes**

-- Arjun Suresh (332k points)

**4.26.7 Number Representation: GATE CSE 1994 | Question: 2.7**<https://gateoverflow.in/2474>

- ✓  $-2^{n-1} \leq N \leq 2^{n-1} - 1$

Example : Let us have 3 bit binary numbers (unsigned )

$000 (0_{10})$  to  $111(7_{10})$  total of  $8(2^3)$  numbers.

But when we have one sign bit then we have half the number of negatives  $-4$  to  $-1$ ,  $0$  and  $1$  to  $3$ .

bit pattern:	100	101	110	111	000	001	010	011
--------------	-----	-----	-----	-----	-----	-----	-----	-----

1's comp:	-3	-2	-1	0	0	1	2	3
-----------	----	----	----	---	---	---	---	---

2's comp.:	-4	-3	-2	-1	0	1	2	3
------------	----	----	----	----	---	---	---	---

**26 votes**

-- Praveen Saini (41.9k points)

**4.26.8 Number Representation: GATE CSE 1995 | Question: 18**<https://gateoverflow.in/2655>

- ✓  $A = 16 + N$ , ( for  $N = -1$ ,  $A = 15$  which is the largest value, for  $N = -8$ ,  $A = 8$ )

$B = \text{REM}$

$C = N/2$

**7 votes**

-- Shaun Patel (6.1k points)

**4.26.9 Number Representation: GATE CSE 1995 | Question: 2.12, ISRO2015-9**<https://gateoverflow.in/2624>

- ✓ I suggest the following approach, here we can clearly see that numbers are getting multiplied by powers of 16. So this is nothing but Hexadecimal number in disguise.

$$(3 \times 4096 + 15 \times 256 + 5 \times 16 + 3) = (3F53)_{16} = (001111101010011)_2 \quad \text{which has total } 2+4+2+2=10 \text{ 1's}$$

Correct Answer: C.

**77 votes**

-- Akash Kanase (36k points)

**4.26.10 Number Representation: GATE CSE 1996 | Question: 1.25**<https://gateoverflow.in/2729>

- ✓ Here, we are asked "magnitude" - so we just need to consider the mantissa bits.

Also, we are told "normalized representation"- so most significant bit of mantissa is always 1 (this is different from IEEE 754 over normalized representation where this 1 is omitted in representation, but here it seems to be added on the right of decimal point as

seen from options).

So, the maximum value of mantissa will be 23 1's where a decimal point is assumed before first 1. So, this value will be  $1 - 2^{-23}$ .

Due to the 1 in normalized representation, the smallest positive number will be 1 followed by 23 0's which will be  $2^{-1} = 0.5$ .

So ans d.

#### References



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46 votes

-- Pooja Palod (24.1k points)



#### 4.26.11 Number Representation: GATE CSE 1997 | Question: 5.4 top

✓  $\sqrt{(224)_r} = (13)_r$

Converting  $r$  base to decimal

$$\sqrt{2 \times r^2 + 2 \times r + 4} = 1 \times r + 3$$

Take square on both sides

$$2r^2 + 2r + 4 = r^2 + 6r + 9$$

$$\Rightarrow r^2 - 4r - 5 = 0$$

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$$\Rightarrow r^2 - 5r + r - 5 = 0$$

$$\Rightarrow (r - 5)(r + 1) = 0$$

$r$  being a base, it can not be  $-1$ .

So, C.  $r = 5$  is correct answer

26 votes

-- Praveen Saini (41.9k points)



#### 4.26.12 Number Representation: GATE CSE 1998 | Question: 1.17 top

✓  $(3\ 4\ 2)_8 = (011\ 100\ 010)_2 = (11100010)_2$

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If we treat this as an 8 bit integer, the first bit becomes sign bit and since it is "1", number is negative. 8085 uses 2's complement representation for integers and hence the decimal equivalent will be  $-(00011110)_2 = -30$ .

Correct Answer: D

39 votes

-- Arjun Suresh (332k points)



#### 4.26.13 Number Representation: GATE CSE 1998 | Question: 2.20 top

✓ I assume byte addressable memory- nothing smaller than a byte can be used.

We have four digits. So, to represent signed 4 digit numbers we need 5 bytes- 4 for four digits and 1 for the sign (like -7354). So, required memory = 5 bytes

Now, if we use integer, the largest number needed to represent is 9999 and this requires 2 bytes of memory for signed representation (one byte can represent only 256 unique integers).

So, memory savings while using integer is  $\frac{(5-2)}{5} = \frac{3}{5} = 60\%$

Correct Answer: C

50 votes

-- Arjun Suresh (332k points)

4.26.14 Number Representation: GATE CSE 1999 | Question: 2.17 [top](#)

<https://gateoverflow.in/1495>



- ✓ A and C.

Sign Magnitude

- $+0 = 0000$
- $-0 = 1000$

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1's complement

- $+0 = 0000$
- $-0 = 1111$

26 votes

-- neelansh (151 points)

4.26.15 Number Representation: GATE CSE 2000 | Question: 1.6 [top](#)

<https://gateoverflow.in/629>



- ✓  $2^s$  complement representation is not same as  $2^r$ 's complement of a number. In  $2^s$  complement representation positive integers are represented in its normal binary form while negative numbers are represented in its  $2^r$ 's complement form. So, (c) is correct here.

[http://www.ele.uri.edu/courses/ele447/proj\\_pages/divid/twos.html](http://www.ele.uri.edu/courses/ele447/proj_pages/divid/twos.html) or [archive](#)

References



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58 votes

-- Arjun Suresh (332k points)

4.26.16 Number Representation: GATE CSE 2000 | Question: 2.14 [top](#)

<https://gateoverflow.in/661>



- ✓ Given 32 bits representation. So, the maximum precision can be 32 bits (In 32-bit IEEE representation, maximum precision is 24 bits but we take the best case here). This means approximately 10 digits.

$$A = 2.0 \times 10^{30}, C = 1.0$$

So,  $A + C$  should make the 31st digit to 1, which is surely outside the precision level of  $A$  (it is 31st digit and not 31st bit). So, this addition will just return the value of  $A$  which will be assigned to  $Y$ .

So,  $Y + B$  will return 0.0 while  $X + C$  will return 1.0.

choice.

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Sample program if anyone wants to try:

```
#include<stdio.h>
int main()
{
    float a = 2.0e30;
    float b = -2.0e30;
    float c = 1.0;
    float y = a+c;
    printf("a = %0.25f y = %0.25f\n",a, y);
    y = y + b;
    float x = a + b;
    printf("x = %0.25f\n",x);
    x = x + c;
    printf("x = %0.25f\n",x);
}
```

32 votes

-- Arjun Suresh (332k points)

4.26.17 Number Representation: GATE CSE 2001 | Question: 2.10 [top](#)

<https://gateoverflow.in/728>



- ✓  $539 = 512 + 16 + 8 + 2 + 1 = 2^9 + 2^4 + 2^3 + 2^1 + 2^0$   
 $= (1000011011)_2$

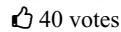
Now all answers have 12 bits, so we add two 0's at beginning =  $(001000011011)_2$

To convert to 2's complement invert all bits till the rightmost 1, which will be  $(110111100101)_2$

$$= (110111100101)_2$$

$$= (DE5)_{16}$$

Correct Answer: C



40 votes

-- Arjun Suresh (332k points)



4.26.18 Number Representation: GATE CSE 2002 | Question: 1.14 top

→ <https://gateoverflow.in/818>

✓ **First Multiplication Iteration**

Multiply 0.25 by 2

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$0.25 * 2 = 0.50$  (Product) Fractional part = 0.50 Carry = 0 (**MSB**)

**Second Multiplication Iteration**

Multiply 0.50 by 2

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$0.50 * 2 = 1.00$  (Product) Fractional part = 1.00 Carry = 1 (**LSB**)

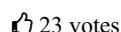
The fractional part in the 2nd iteration becomes zero and hence we stop the multiplication iteration.

Carry from the 1st multiplication iteration becomes **MSB** and carry from 2nd iteration becomes **LSB**.

So the result is 0.01

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Correct Answer: B.



23 votes

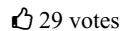
-- shekhar chauhan (32.8k points)



4.26.19 Number Representation: GATE CSE 2002 | Question: 1.15 top

→ <https://gateoverflow.in/819>

- ✓ D) is the correct ans.In 2's complement representation, positive numbers are represented in simple binary form and negative numbers are represented in its 2's complement form. So, for -15, we have to complement its binary value - 01111 and add a 1 to it, which gives 10001. Option D.



29 votes

-- Ujjwal Saini (283 points)

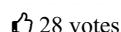


4.26.20 Number Representation: GATE CSE 2002 | Question: 1.16 top

→ <https://gateoverflow.in/821>



- ✓ (D) is the answer. Sign extension (filling the upper bits using the sign bit) is needed while increasing the number of bits for representing a number. For positive numbers, 0 is extended and for negative numbers 1 is extended.



28 votes

-- gatecse (63.3k points)



4.26.21 Number Representation: GATE CSE 2002 | Question: 1.21 top

→ <https://gateoverflow.in/826>

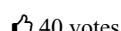
- ✓ (B) is the answer. When a positive value and negative value are added overflow never happens.

<http://sandbox.mc.edu/~bennet/cs110/tc/orules.html>

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References



40 votes

-- Arjun Suresh (332k points)



- ✓ Here, mantissa is represented in normalized representation and exponent in excess-64 (subtract 64 to get actual value).

a. We have to represent  $-(7.5)_{10} = -(111.1)_2$ .

Now we are using base 16 for exponent. So, mantissa will be .01111 and this makes exponent as 1(4 bit positions and no hiding first 1 as in IEEE 754 as this is not mentioned in question) which in excess-64 will be  $64 + 1 = 65$ . Number being negative sign bit is 1. So, we get

$$(1 \underbrace{01111000 \dots 0}_{19 \text{ zeroes}} 1000001)_2 = (\text{BC}000041)_{16}$$

b. Largest value will be with largest possible mantissa, largest possible exponent and positive sign bit. So, this will be all 1's except sign bit which will be

$$\underbrace{0.111 \dots 1}_{24 \text{ ones}} \times 16^{127-64} = (1 - 2^{-24}) \times 16^{63} = (1 - 2^{-24}) \times 16^{63}$$

(Again we did not add implicit 1 as in IEEE 754)

$$2^x = 10^y \implies y = \log 2^x = x \log 2$$

$$\text{So, } (1 - 2^{-24}) \times 16^{63} = (1 - 10^{-24 \log 2}) \times 10^{63 \log 16} \approx (1 - 10^{-7}) \times 10^{76} = 10^{76}$$

Not directly relevant here, but a useful read: <https://jeapostrophe.github.io/courses/2015/fall/305/notes/dist/reading/help-floating-point.pdf>

#### References



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34 votes

-- Arjun Suresh (332k points)



- ✓ MSB of 2's compliment number has a weight of  $-2^{(n-1)}$

( Trick: (from reversing sign extension) just skip all leading 1's from MSB expect but 1, and then calculate the value as normal signed binary rep. )

so by calculating, we get the given number is  $-5$  in decimal. and options are

- A.  $-25$
- B.  $-28$
- C.  $-41$
- D.  $-37$

Therefore it is clear that  $-25$  is divisible by  $-5$ . so we can say that (A) is correct ☺

28 votes

-- Nitin Sharma (2.2k points)



- ✓ Answer is D.

$$x \times 7 + 3 = 5 \times y + 4 \implies 7x = 5y + 1$$

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Only option satisfying this is D.

25 votes

-- Aditi Dan (4k points)



- ✓  $(113. + -111.) = 1.13 \times 10^2 + -1.11 \times 10^2 = 0.02 \times 10^2 = 2.0 \times 10^0$

$$2.0 \times 10^0 + 7.51 \times 10^0 = 9.51 \times 10^0$$

$$(-111. + 7.51) = -1.11 \times 10^2 + 7.51 \times 10^0 = -1.11 \times 10^2 + 0.08 \times 10^2 = -1.03 \times 10^2$$

$$113. + -1.03 \times 10^2 = 1.13 \times 10^2 + -1.03 \times 10^2 = 0.1 \times 10^2 = 10.0$$

Reference: <https://www.doc.ic.ac.uk/~eedwards/compsys/float/>

Correct Answer: A

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#### References



73 votes

-- Arjun Suresh (332k points)

#### 4.26.26 Number Representation: GATE CSE 2004 | Question: 66 [top](#)

<https://gateoverflow.in/1060>



- ✓  $A = 1111 \quad 1010 = -6$
- $B = 0000 \quad 1010 = 10$
- $A \times B = -60 = 1100 \quad 0100$

Correct Answer: A

30 votes

-- Digvijay (44.9k points)

#### 4.26.27 Number Representation: GATE CSE 2005 | Question: 16, ISRO2009-18, ISRO2015-2 [top](#)

<https://gateoverflow.in/1352>



- ✓ Total number of distinct numbers that can be represented using  $n$  bits =  $2^n$ .

In case of unsigned numbers these corresponds to numbers from 0 to  $2^n - 1$ .

In case of signed numbers in 1's complement or sign magnitude representation, these corresponds to numbers from  $-(2^{n-1} - 1)$  to  $2^{n-1} - 1$  with 2 separate representations for 0.

In case of signed numbers in 2's complement representation, these corresponds to numbers from  $-2^{n-1}$  to  $2^{n-1} - 1$  with a single representation for 0.

4 votes

-- Arjun Suresh (332k points)

#### 4.26.28 Number Representation: GATE CSE 2005 | Question: 17 [top](#)

<https://gateoverflow.in/1353>



$$(657)_8 = (\underbrace{110}_6 \underbrace{101}_5 \underbrace{111}_7)_2 = (\underbrace{1}_1 \underbrace{1010}_A \underbrace{1111}_F)_2 = (1AF)_{16}$$

Correct Answer: A.

17 votes

-- Arjun Suresh (332k points)

#### 4.26.29 Number Representation: GATE CSE 2006 | Question: 39 [top](#)

<https://gateoverflow.in/1815>



- ✓ Number representation in 2's complement representation:

- Positive numbers as they are
- Negative numbers in 2's complement form.

So, the overflow conditions are

1. When we add two positive numbers (sign bit 0) and we get a sign bit 1
2. When we add two negative numbers (sign bit 1) and we get sign bit 0
3. Overflow is relevant only for signed numbers and carry is used for unsigned numbers
4. When the carryout bit and the carryin to the most significant bit differs

PS: When we add one positive and one negative number we won't get a carry. Also points 1 and 2 are leading to point 4.

Now the question is a bit tricky. It is actually asking the condition of overflow of signed numbers when we use an adder which is meant to work for unsigned numbers.

So, if we see the options, B is the correct one here as the first part takes care of case 2 (negative numbers) and the second part takes care of case 1 (positive numbers) - point 4. We can see counterexamples for other options:

A - Let  $n = 4$  and we do  $0111 + 0111 = 1110$ . This overflows as in 2's complement representation we can store only up to 7. But the overflow condition in A returns false as  $c_{out} = 0$ .

C - This works for the above example. But fails for  $1001 + 0001 = 1010$  where there is no actual overflow ( $-7 + 1 = -6$ ), but the given condition gives an overflow as  $c_{out} = 0$  and  $c_{n-1} = 1$ .

D - This works for both the above examples, but fails for  $1111 + 1111 = 1110$  ( $-1 + -1 = -2$ ) where there is no actual overflow but the given condition says so.

Reference: [http://www.mhhe.com/engcs/electrical/hamacher/5e/graphics/ch02\\_025-102.pdf](http://www.mhhe.com/engcs/electrical/hamacher/5e/graphics/ch02_025-102.pdf)

Thanks, @Dilpreet for the link and correction.

#### References



1 like 61 votes

-- Digvijay (44.9k points)

### 4.26.30 Number Representation: GATE CSE 2008 | Question: 6

<https://gateoverflow.in/404>



✓  $\sqrt{(121)_r} = 11_r$

$$\sqrt{(1 \times r^0) + (2 \times r^1) + (1 \times r^2)} = (1 \times r^0) + (1 \times r^1)$$

$$\sqrt{(1+r)^2} = 1+r$$

$$1+r = 1+r$$

So any integer  $r$  satisfies this but  $r$  must be greater than 2 as we have 2 in 121 and radix must be greater than any of the digits. **(D) is the most appropriate answer**

1 like 43 votes

-- Keith Kr (4.5k points)

### 4.26.31 Number Representation: GATE CSE 2009 | Question: 5, ISRO2017-57

<https://gateoverflow.in/1297>



✓ Answer: (b)

Here are two different ways of solving this problem.

#### Short Method

Given number is in base 8 thus each digit can be represented in three binary bits to get overall binary equivalent.

$$(1217)_8 = (001\ 010\ 001\ 111)_2$$

I have written the equivalent in group of three bits for easy understanding of the conversion. We can rearrange them in group of four to get equivalent hexadecimal number (in similar manner).

$$(001010001111)_2 = (0010\ 1000\ 1111)_2 = (28F)_{16}$$

#### Long Method

In a nut shell the long method follow the following conversion

$$OCT \rightarrow DEC \rightarrow HEX$$

This procedure is good in a sense that the given option also have a decimal equivalent, and thereby might save some time (no in this case, unfortunately).

Here is the the decimal equivalent

$$(1217)_8 = (1 * 8^3 + 2 * 8^2 + 1 * 8^1 + 7 * 8^0)_{10} = (655)_{10}$$

And we see that decimal equivalent is not in option therefore we proceed for hexadecimal conversion using [division method](#).

$$(655)_{10} = (28F)_{16}$$

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Which we can find in given options.

HTH

References



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1 24 votes

-- Prateek Dwivedi (3.5k points)



#### 4.26.32 Number Representation: GATE CSE 2010 | Question: 8 top

► <https://gateoverflow.in/2179>

- ✓ Multiplication can be directly carried in 2's complement form.  $F87B = 1111\ 1000\ 0111\ 1011$  can be left shifted 3 times to give  $8P = 1100\ 0011\ 1101\ 1000 = C3D8$ .

Or, we can do as follows:

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MSB in ( $F87B$ ) is 1. So, P is a negative number. So,  $P = -1 * 2^7$  complement of ( $F87B$ ) =  $-1 * (0785) = -1 * (0000\ 0111\ 1000\ 0101)$

$8 * P = -1 * (0011\ 1100\ 0010\ 1000)$  (P in binary left shifted 3 times)

In 2's complement representation , this equals,  $1100\ 0011\ 1101\ 1000 = C3D8$

Correct Answer: A

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1 68 votes

-- Arjun Suresh (332k points)



#### 4.26.33 Number Representation: GATE CSE 2013 | Question: 4 top

► <https://gateoverflow.in/1413>

- ✓ Range of 2's compliment no  $\Rightarrow (-2^{n-1})$  to  $(2^{n-1} - 1)$

Here  $n = \text{No of bits} = 8$ .

So minimum no  $= -2^7 = (B) -128$

1 33 votes

-- Akash Kanase (36k points)



#### 4.26.34 Number Representation: GATE CSE 2014 Set 1 | Question: 8 top

► <https://gateoverflow.in/1766>

- ✓ Let 'x' be the base or radix of the number system .

The equation is : 
$$\frac{3.x^2 + 1.x^1 + 2.x^0}{2.x^1 + 0.x^0} = 1.x^1 + 3.x^0 + 1.x^1$$

$$\Rightarrow \frac{3.x^2 + x + 2}{2.x} = x + 3 + 1/x$$

$$\Rightarrow \frac{3.x^2 + x + 2}{2.x} = \frac{x^2 + 3x + 1}{x}$$

$$\Rightarrow 3.x^2 + x + 2 = 2.x^2 + 6x + 2$$

$$\Rightarrow x^2 + 5x = 0$$

$$\Rightarrow x(x - 5) = 0$$

$$\Rightarrow x = 0 \text{ or } x = 5$$

As base or radix of a number system cannot be zero, here  $x = 5$ .

1 41 votes

-- vinodmits (363 points)



- ✓ Converting both sides to decimal,

$$25 + 10 + 3 = x * y + 8$$

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So,  $xy = 30$

Possible pairs are  $(1, 30), (2, 15), (3, 10)$  as the minimum base should be greater than 8.

42 votes

-- Tejas Jaiswal (559 points)



$$(43)_x = (y3)_8$$

Since a number in base  $-k$  can only have digits from 0 to  $(k - 1)$ , we can conclude that:  $x \geq 5$  and  $y \leq 7$

Now, the original equation, when converted to decimal base gives:

$$4x^1 + 3x^0 = y(8^1) + 3(8^0)$$

$$4x + 3 = 8y + 3$$

$$x = 2y$$

So, we have the following constraints:

$$x \geq 5 \\ y \leq 7 \\ x = 2y, y \text{ are integers}$$

The set of values of  $(x, y)$  that satisfy these constraints are:

$$\underline{(x, y)}$$

$$(6, 3)$$

$$(8, 4)$$

$$(10, 5)$$

$$(12, 6)$$

$$(14, 7)$$

**I am counting 5 pairs of values.**

52 votes

-- Praveen Saini (41.9k points)



- ✓ 1111 1111 1111 0101

$2's$  complement of

$$1111 1111 1111 0101 =$$

$$0000 0000 0000 1011 =$$

$$+11$$

$2's$  complement of

$$-11 =$$

$$+11, \text{ in }$$

$2's$  complement representation

$2's$  complement of

$$+11 =$$

$$-11, \text{ in }$$

$2's$  complement representation

So

$-11$  it should be

34 votes

-- Praveen Saini (41.9k points)

#### 4.26.38 Number Representation: GATE CSE 2016 Set 2 | Question: 09 [top](#)

<https://gateoverflow.in/39546>



##### ✓ 2's Complement Representation

The range of  $n - bit$  2's Complement Numbers is  $-(2^{n-1})$  to  $+(2^{n-1} - 1)$

For example, if  $n = 2$ , then  $-2, -1, 0, 1$  belong to the range (which are distinct)

In general  $2^n$  distinct integers are possible with  $n - bit$  2's Complement Number  $\rightarrow X$

##### Sign Magnitude Representation

The range of  $n - bit$  Sign Magnitude numbers is  $-(2^{n-1} - 1)$  to  $+(2^{n-1} - 1)$

For example, if  $n = 2$ , then  $-1, -0, +0, +1$  belong to the range in which  $-0 = +0$  and both represent zero.

In general  $2^n - 1$  distinct integers are possible with  $n - bit$  Sign magnitude representation  $\rightarrow Y$

$$X - Y = 2^n - (2^n - 1) = 1$$

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37 votes

-- Uzumaki Naruto (1.6k points)

#### 4.26.39 Number Representation: GATE CSE 2017 Set 1 | Question: 9 [top](#)

<https://gateoverflow.in/118289>



##### ✓ Answer is (C)

Overflow is said to occur in the following cases

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C7	C6	Overflow
0	0	NO
0	1	YES
1	0	YES
1	1	NO

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The 3<sup>rd</sup> condition occurs in the following case A7B7S7', now the question arises how?

C7	C6
A7	1
B7	1
S7	0

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NOW,  $A7 = 1$  AND  $B7 = 1$   $S7 = 0$  is only possible when  $C6 = 0$  otherwise  $S7$  would become 1.

$C7$  has to be 1 ( $1 + 1 + 0$  generates carry)

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ON similar basis we can prove that  $C7 = 0$  and  $C6 = 1$  is produced by  $A7' B7' S7$ . Hence, either of the two conditions cause overflow. Hence(C).

Why not A? when  $C7 = 1$  and  $C6 = 1$  this doesn't indicate overflow (4<sup>th</sup> row in the table)

Why not B? if all carry bits are 1 then,  $C7 = 1$  and  $C6 = 1$  (This also generates 4<sup>th</sup> row)

Why not D? These combinations are  $C0$  and  $C1$ , the lower carries do not indicate overflow

36 votes

-- (points)

#### 4.26.40 Number Representation: GATE CSE 2017 Set 2 | Question: 1 [top](#)

<https://gateoverflow.in/118337>



##### ✓ Given: (BCA9)<sub>16</sub>

1011 1100 1010 1001

For octal number system: grouping of three- three bits from right to left

1 011 110 010 101 001

1 3 6 2 5 1

Answer: option D) (1 3 6 2 5 1)<sub>8</sub>

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22 votes

-- Smriti012 (2.8k points)



4.26.41 Number Representation: GATE CSE 2019 | Question: 22 [top](#)

<https://gateoverflow.in/302826>

✓ These are two groups: flow.in

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1. MSB with 1
2. MSB with 0

$$n_{MSB0} = 7, n_{MSB1} = 6, n_{total} = 13$$

Choose randomly and INDEPENDENTLY two elements out of 13 elements such that MSB is same.

$$P = \frac{n_{MSB1} * n_{MSB1} + n_{MSB0} * n_{MSB0}}{n_{Total}}$$

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$$P = \frac{7*7+6*6}{13*13} = \frac{85}{169} = 0.5029$$

39 votes

-- Digvijay (44.9k points)



4.26.42 Number Representation: GATE CSE 2019 | Question: 4 [top](#)

<https://gateoverflow.in/302844>

✓  $(+28)_{10} = (0000\ 0000\ 00011100)_2$   
-28 is nothing but 2s complement of +28.

So, 2s complement of  $(0000\ 0000\ 0001\ 1100)_2$  is  $(1111\ 1111\ 1110\ 0100)_2$

$$(-28)_{10} = (1111\ 1111\ 1110\ 0100)_2. \text{ Answer is (C).}$$

28 votes

-- Digvijay (44.9k points)



4.26.43 Number Representation: GATE CSE 2019 | Question: 8 [top](#)

<https://gateoverflow.in/302840>

✓ Let  $X$  and  $Y$  represents 31 and -31 respectively in binary sign magnitude form.  $X$  and  $Y$  will take 6 bits as range of sign magnitude form is  $-(2^{(n-1)} - 1)$  to  $2^{(n-1)} - 1$ ; where  $n$  is the number of bits.

Now in question  $Z = X - Y$ ,

$$Z = 31 - (-31) = 62$$

To represent 62 in sign magnitude form we need 7 ( $6 + 1$ ) bits.

Hence,  $n + 1$  bits needed.

Answer is C.

36 votes

-- DIVYANSHU SAXENA (421 points)



4.26.44 Number Representation: GATE CSE 2021 Set 1 | Question: 6 [top](#)

<https://gateoverflow.in/357446>

✓ Firstly convert base 3 into a decimal number system(Base 10):

$$(210)_3 = (x)_{10} \implies 0 * 3^0 + 1 * 3^1 + 2 * 3^2 = (21)_{10}$$

Now convert  $(21)_{10}$  into a hexadecimal system. dividing by 16 that is:

$$(21)_{10} = (z)_{16}$$

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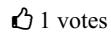
16	21	
		in
1	5	

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$$\therefore z = (15)_{16}$$

Option A is correct.



1 votes

-- Hira (14.1k points)

#### 4.26.45 Number Representation: GATE CSE 2021 Set 2 | Question: 18 top

<https://gateoverflow.in/357522>

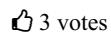


**Answer: 3**

This conversion is just

$$\frac{1}{2} + \frac{1}{4} + \frac{1}{16} = \frac{8+4+1}{16} = \frac{13}{16} = 0.8125$$

On comparison we get  $x = 1$  and  $y = 2$ . Hence,  $x + y = 3$ .



3 votes

-- witness\_07 (145 points)

Answer = 3

- A.  $(0.1)_2 = (0.5)_{10}$
- B.  $(0.01)_2 = (0.25)_{10}$
- C.  $(0.001)_2 = (0.125)_{10}$
- D.  $(0.0001)_2 = (0.0625)_{10}$

$$A + B + D \Rightarrow (0.1101)_2 = 0.8125$$

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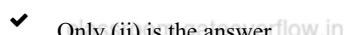


7 votes

-- JATIN MITTAL (2.1k points)

#### 4.26.46 Number Representation: GATE IT 2004 | Question: 42 top

<https://gateoverflow.in/3685>



Only (ii) is the answer.

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In 2's complement arithmetic, overflow happens only when

1. Sign bit of two input numbers is 0, and the result has sign bit 1
2. Sign bit of two input numbers is 1, and the result has sign bit 0.

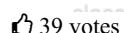
Overflow is important only for signed arithmetic while carry is important only for unsigned arithmetic.

A carry happens when there is a carry to (or borrow from) the most significant bit. Here, (i) and (iii) cause a carry but only (ii) causes overflow.

[http://teaching.idallen.com/dat2343/10f/notes/040\\_overflow.txt](http://teaching.idallen.com/dat2343/10f/notes/040_overflow.txt)

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References



39 votes

-- Arjun Suresh (332k points)



✓  $(123456)_8 = (001\ 010\ 011\ 100\ 101\ 110)_2 = (00 \underbrace{1010}_A \underbrace{0111}_7 \underbrace{0010}_2 \underbrace{1110}_E)_2 = (A72E)_{16}$   
 $= (00\ 10\ 10\ 01\ 11\ 00\ 10\ 11\ 10)_2 = (22130232)_4$

So, option (A).

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28 votes

-- Arjun Suresh (332k points)



✓ Simply convert  $(34.4)_8$  and  $(23.4)_8$  to decimal.

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$$(34.4)_8 = 28.5 \text{ in decimal and } (23.4)_8 = 19.5 \text{ in decimal.}$$

$$28.5 \times 19.5 = 555.75$$

Now convert 555.75 back to octal which is  $(1053.6)_8$

$\overleftarrow{(34.4)}_8$  to decimal

$$\begin{aligned} &= 3 \times 8^1 + 4 \times 8^0 + 4 \times 8^{-1} \\ &= 24 + 4 + 0.5 \\ &= (28.5)_{10} \end{aligned}$$

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$\overleftarrow{(23.4)}_8$  to decimal

$$\begin{aligned} &= 2 \times 8^1 + 3 \times 8^0 + 4 \times 8^{-1} \\ &= 16 + 3 + 0.5 \\ &= (19.5)_{10} \end{aligned}$$

$$(28.5)_{10} \times (19.5)_{10} = (555.75)_{10}$$

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Now,

$$(555.75)_{10} = (?)_8$$

To convert the integer part

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8	555	
8	69	3
8	8	5
8	1	0
8	0	1 ↑

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We get 1053.

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To convert the decimal, keep multiplying by 8 till decimal part becomes 0.

$$0.75 \times 8 \rightarrow \quad \underbrace{6}_{\text{keep the integral part}} \quad . \quad \underbrace{00}_{\text{0 decimal part}}$$

$$\therefore (555.75)_{10} = (1053.6)_8$$

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Correct Answer: A

24 votes

-- Afaque Ahmad (727 points)



✓ Answer: C.

The addition results in 0001 and no overflow with 1 as carry bit.

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In 2's complement addition Overflow happens only when:

- Sign bit of two input numbers is 0, and the result has sign bit 1.
- Sign bit of two input numbers is 1, and the result has sign bit 0.

1 like votes

-- Rajarshi Sarkar (27.9k points)



✓  $(C012.25)_H - (10111001110.101)_B$

$$\begin{array}{r} = 1100\ 0000\ 0001\ 0010.\ 0010\ 0101 \\ - 0000\ 0101\ 1100\ 1110.\ 1010\ 0000 \end{array}$$

$$= 1011\ 1010\ 0100\ 0011.\ 1000\ 0101$$

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$$= 1\ 011\ 101\ 001\ 000\ 011.\ 100\ 001\ 010$$

$$= (135103.412)_o$$

Binary subtraction is like decimal subtraction:  $0 - 0 = 0, 1 - 1 = 0, 1 - 0 = 1, 0 - 1 = 1$  with 1 borrow.

Correct Answer: A

1 like votes

-- Arjun Suresh (332k points)



✓ Answer: B

$01001101$

$+ 11101001$

-----

$100110110$

Carry = 1

Overflow = 0 (In 2's complement addition Overflow happens only when: Sign bit of two input numbers is 0, and the result has sign bit 1 OR Sign bit of two input numbers is 1, and the result has sign bit 0.)

Sign bit = 0.

1 like votes

-- Rajarshi Sarkar (27.9k points)



State whether the following statements are TRUE or FALSE with reason:

RAM is a combinational circuit and PLA is a sequential circuit.

gate1990 true-false digital-logic ram pla

Answer

Answers: Pla



Both the statements are false.

- RAM is not a combinational circuit. For **RAM**, the input is the memory location selector and the operation (read or write) and another byte (which can be input for write operation, or output for read operation), and the output is either a success indicator (for write operation) or the byte at the selected location (for read operation). It does depend on past inputs, or rather, on the past write operations at the selected byte. This is a **Sequential logic circuit**.
- PLA is a combinational circuit as ROM & PAL. PLA is a programmable logic device with a programmable AND array and a programmable OR array. A PLA with  $n$  inputs has fewer than  $2n$  AND gates (otherwise there would be no advantage over a ROM implementation of the same size). A PLA only needs to have enough AND gates to decode as many unique terms as there are in the functions it will implement.

11 votes

-- vamsi2376 (2.8k points)

## 4.28

## Prime Implicants (2) top



Let  $f(x, y, z) = \bar{x} + \bar{y}x + xz$  be a switching function. Which one of the following is valid?

- A.  $\bar{y}x$  is a prime implicant of  $f$
- B.  $xz$  is a minterm of  $f$
- C.  $xz$  is an implicant of  $f$
- D.  $y$  is a prime implicant of  $f$

gate1997 digital-logic normal prime-implicants

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Answer



Which are the essential prime implicants of the following Boolean function?

$$f(a, b, c) = a'c + ac' + b'c$$

- A.  $a'c$  and  $ac'$
- B.  $a'c$  and  $b'c$
- C.  $a'c$  only.
- D.  $ac'$  and  $bc'$

gate2004-cse digital-logic normal prime-implicants

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tests.gatecse.in

Answer

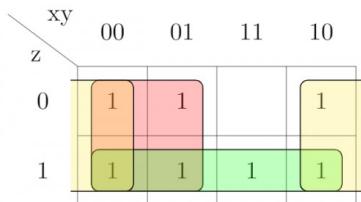
## Answers: Prime Implicants



- ✓ In sum of terms, any term is an implicant because it implies the function. So,  $xz$  is an implicant and hence C is the answer. Still, let's see the other options.

If no minimization is possible for an implicant (by removing any variable) it becomes a prime implicant.

If a prime implicant is present in any possible expression for a function, it is called an essential prime implicant. (For example in K-map we might be able to choose among several prime implicants but for essential prime implicants there won't be a choice).



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So,  $f = x' + y'x + xz$   
 $= y' + x' + z$  (could be also derived using algebraic rules as in <http://www.ee.surrey.ac.uk/Projects/Labview/boolalgebra/>)

So, the prime implicants are  $x'$ ,  $y'$  and  $z$ . Being single variable ones and with no common variables, all must be essential also.

Now, a choice is false, as  $y'$  is a prime implicant and hence,  $y'x$  is just an implicant but not prime.

**b choice -  $xz$**  is not a minterm. A minterm must include all variables. So,  $xyz$  is a minterm so, is  $xy'z$ , but not  $xz$ .

**d choice -  $y'$**  is a prime implicant not  $y$ .

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References



33 votes

-- Arjun Suresh (332k points)

#### 4.28.2 Prime Implicants: GATE CSE 2004 | Question: 59 top

<https://gateoverflow.in/1054>



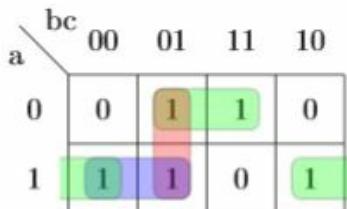
- ✓  $f(a, b, c) = a'c + ac' + b'c$

We can write these product of sum terms into canonical product of sum form.

$$f(a, b, c) = \underbrace{a'b'c}_{001} + \underbrace{a'bc}_{011} + \underbrace{ab'c'}_{100} + \underbrace{abc'}_{110} + \underbrace{ab'c}_{101} + \underbrace{a'b'c}_{001}$$

$$f(a, b, c) = \sum(1, 3, 4, 5, 6)$$

Now, we can draw the k-map for these minterms.



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- Prime implicant of  $f$  is an implicant that is minimal - that is, the removal of any literal from product term results in a non-implicant for  $f$ .
- Essential prime implicant is a prime implicant that covers an output of the function that no combination of other prime implicants is able to cover.

Prime implicants are:  $a'c, b'c, ab', ac'$

Essential prime implicants are:  $a'c, ac'$  (green color).

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References:

- [http://dispert.international-university.eu/Digital\\_Design\\_Website\\_English/digital\\_2/dig002\\_5.html](http://dispert.international-university.eu/Digital_Design_Website_English/digital_2/dig002_5.html)
- <http://web.cecs.pdx.edu/~mcnames/ECE171/Lectures/Lecture10.html>

References

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14 votes

-- Lakshman Patel (65.7k points)

4.29

Rom (4) [top](#)

4.29.1 Rom: GATE CSE 1993 | Question: 6.6 [top](#)

<https://gateoverflow.in/2285>



A ROM is used to store the Truth table for binary multiple units that will multiply two 4-bit numbers. The size of the ROM (number of words  $\times$  number of bits) that is required to accommodate the Truth table is M words  $\times$  N bits . Write the values of M and N.

gate1993 digital-logic normal rom descriptive

goclasses.in

tests.gatecse.in

Answer

4.29.2 Rom: GATE CSE 1996 | Question: 1.21 [top](#)

<https://gateoverflow.in/2725>



A ROM is used to store the table for multiplication of two 8-bit unsigned integers. The size of ROM required is

- A.  $256 \times 16$
- B.  $64K \times 8$
- C.  $4K \times 16$
- D.  $64K \times 16$

gate1996 digital-logic normal rom

goclasses.in

tests.gatecse.in

Answer

4.29.3 Rom: GATE CSE 2012 | Question: 19 [top](#)

<https://gateoverflow.in/51>



The amount of ROM needed to implement a 4 – bit multiplier is

- A. 64 bits
- B. 128 bits
- C. 1 Kbits
- D. 2 Kbits

gate2012-cse digital-logic normal rom

goclasses.in

tests.gatecse.in

Answer

4.29.4 Rom: GATE IT 2004 | Question: 10 [top](#)

<https://gateoverflow.in/3651>



What is the minimum size of ROM required to store the complete truth table of an 8 – bit  $\times$  8 – bit multiplier?

- A.  $32K \times 16$  bits
- B.  $64K \times 16$  bits
- C.  $16K \times 32$  bits
- D.  $64K \times 32$  bits

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gate2004-it digital-logic normal rom

Answer

Answers: Rom

4.29.1 Rom: GATE CSE 1993 | Question: 6.6 [top](#)

<https://gateoverflow.in/2285>



- ✓ A is 4 bit binary no A4A3A2A1

$B$  is 4 bit binary no  $B_4B_3B_2B_1$

$M$  is result of multiplication  $M_8M_7M_6M_5M_4M_3M_2M_1$  [check biggest no  $1111 \times 1111 = 11100001$  ]

A4	A3	A2	A1	B4	B3	B2	B1	M8	M7	M6	M5	M4	M3	M2	M1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	0	1	1	0	1	0	0	1	0
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1

4 bits of  $A$  and 4 bits of  $B$  mean input will consist of 8 bits and need address 00000000 to 11111111 =  $2^8$  address

The output will be of 8 bits

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So memory will be of  $2^8 \times 8$

$$M = 256, N = 8$$



22 votes

-- Praveen Saini (41.9k points)



#### 4.29.2 Rom: GATE CSE 1996 | Question: 1.21 [top](#)

► <https://gateoverflow.in/2725>

- ✓ When we multiply two 8 bit numbers result can go up to 16 bits. So, we need 16 bits for each of the multiplication result. Number of results possible =  $2^8 \times 2^8 = 2^{16} = 64 K$  as we need to store all possible results of multiplying two 8 bit numbers. So,  $64 K \times 16$  is the answer.

Correct Answer: D



74 votes

-- Arjun Suresh (332k points)

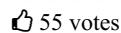


#### 4.29.3 Rom: GATE CSE 2012 | Question: 19 [top](#)

► <https://gateoverflow.in/51>

- ✓ A ROM cannot be written. So, to implement a 4-bit multiplier we must store all the possible combinations of  $2^4 \times 2^4$  inputs and their corresponding 8 output bits giving a total of  $2^4 \times 2^4 \times 8$  bits = 2048 bits. So, (D) is the answer.

PS: We are not storing the input bits explicitly -- those are considered in order while accessing the output 8 bits. In this way, by storing all the possible outputs in order we can avoid storing the input combinations.



-- Arjun Suresh (332k points)



#### 4.29.4 Rom: GATE IT 2004 | Question: 10 [top](#)

► <https://gateoverflow.in/3651>

- ✓ Answer - B.

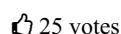
Multiplying 2 8 bit digits will give result in maximum 16 bits

Total number of multiplications possible =  $2^8 \times 2^8$

Hence, space required =  $64K \times 16$  bits

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-- Ankit Rokde (6.9k points)



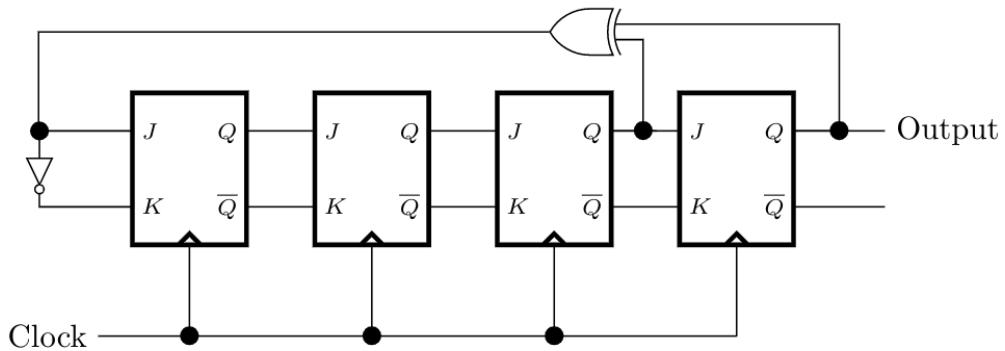
### 4.30

#### Sequential Circuit (6) [top](#)



#### 4.30.1 Sequential Circuit: GATE CSE 1987 | Question: 1-III [top](#)

► <https://gateoverflow.in/80034>



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The above circuit produces the output sequence:

- A. 1111 1111 0000 0000
- B. 1111 0000 1111 0000
- C. 1111 0001 0011 0101
- D. 1010 1010 1010 1010

gate1987 digital-logic sequential-circuit flip-flop digital-counter

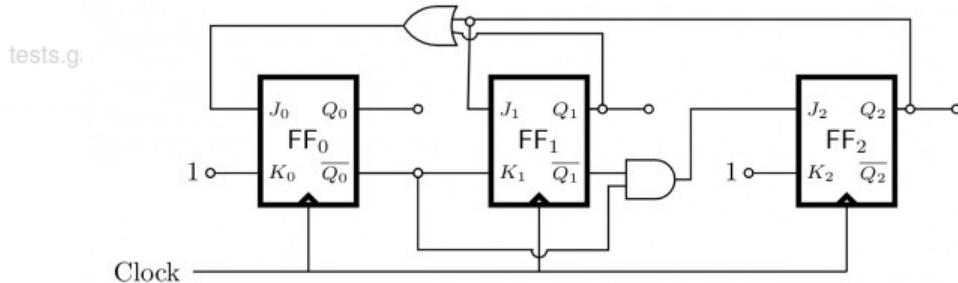
Answer ↗

#### 4.30.2 Sequential Circuit: GATE CSE 1990 | Question: 5-c

<https://gateoverflow.in/85400>



For the synchronous counter shown in Fig.3, write the truth table of  $Q_0, Q_1$ , and  $Q_2$  after each pulse, starting from  $Q_0 = Q_1 = Q_2 = 0$  and determine the counting sequence and also the modulus of the counter.



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gate1990 descriptive digital-logic sequential-circuit flip-flop digital-counter

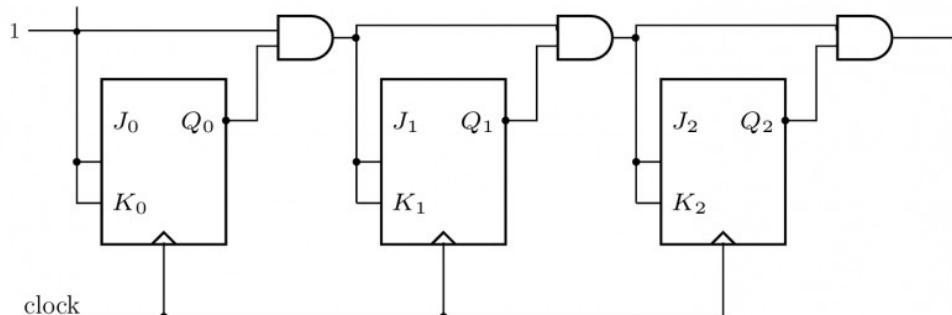
Answer ↗

#### 4.30.3 Sequential Circuit: GATE CSE 1991 | Question: 5-c

<https://gateoverflow.in/26442>



Find the maximum clock frequency at which the counter in the figure below can be operated. Assume that the propagation delay through each flip flop and each AND gate is 10 ns. Also, assume that the setup time for the JK inputs of the flip flops is negligible.



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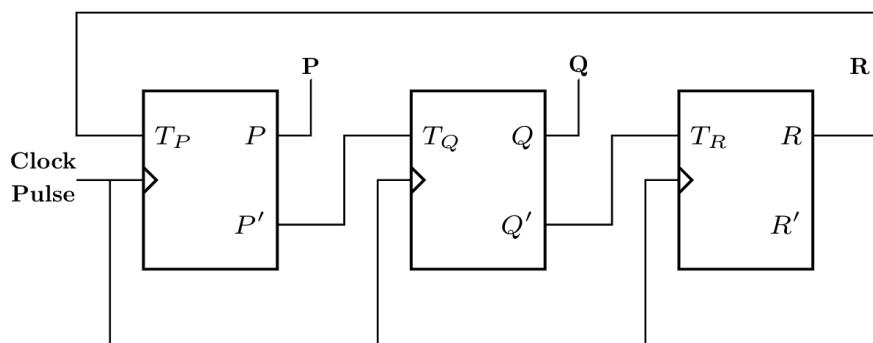
Answer ↗

## 4.30.4 Sequential Circuit: GATE CSE 1994 | Question: 2-1 top ↗

↗ <https://gateoverflow.in/2468>The number of flip-flops required to construct a binary modulo  $N$  counter is \_\_\_\_\_

Answer ↗

## 4.30.5 Sequential Circuit: GATE CSE 2021 Set 1 | Question: 28 top ↗

↗ <https://gateoverflow.in/357423>Consider a 3-bit counter, designed using  $T$  flip-flops, as shown below:

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Assuming the initial state of the counter given by PQR as 000, what are the next three states?

- A. 011, 101, 000  
 B. 001, 010, 111  
 C. 011, 101, 111  
 D. 001, 010, 000

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Answer ↗

## 4.30.6 Sequential Circuit: GATE1992-04-c top ↗

↗ <https://gateoverflow.in/17408>

Design a 3-bit counter using D-flip flops such that not more than one flip-flop changes state between any two consecutive states.

Answer ↗

## Answers: Sequential Circuit

## 4.30.1 Sequential Circuit: GATE CSE 1987 | Question: 1-III top ↗

↗ <https://gateoverflow.in/80034>

- ✓ Let us suppose the initial output of all the JK flip flops is 1

So we can draw the below table to get the output  $Q_3$ 

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Index	$Q_3$	$Q_2$	$Q_1$	$Q_0$	$J_3$	$K_3$	$J_2$	$K_2$	$J_1$	$K_1$	$J_0$	$K_0$
					$Q'_2$	$Q'_1$	$Q_1$	$Q'_0$	$Q_0$	$Q'_0$	$Q_3 \oplus Q_2$	$J'_0$
0	1	1	1	1	1	0	1	0	1	0	0	1
1	1	1	1	0	1	0	1	0	0	1	0	1
2	1	1	0	0	1	0	0	1	0	1	0	1
3	1	0	0	0	0	1	0	1	0	1	1	0
4	0	0	0	1	0	1	0	1	1	0	0	1
5	0	0	1	0	0	1	1	0	0	1	0	1
6	0	1	0	0	1	0	0	1	0	1	1	0
7	1	0	0	0	1	0	1	0	1	1	0	0
8	0	0	1	1	0	1	1	0	1	0	0	1
9	0	1	1	0	1	0	1	0	0	1	1	0
10	1	1	0	1	1	0	0	1	1	0	0	1
11	1	0	1	0	0	1	1	0	0	1	1	0
12	0	1	0	1	1	0	0	1	1	0	1	0
13	1	0	1	1	0	1	1	0	1	0	1	0
14	0	1	1	1	1	0	1	0	1	0	1	0
15	1	1	1	1								

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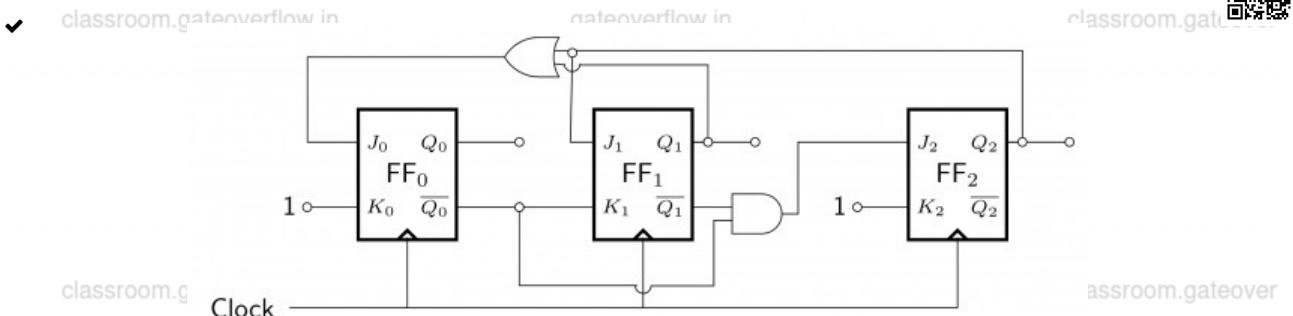
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From the above table  $Q_3$  that is output is 1111 0001 0011 0101

So the answer should be C.

3 votes

-- Digvijaysingh Gautam (6.3k points)

**4.30.2 Sequential Circuit: GATE CSE 1990 | Question: 5-c**<https://gateoverflow.in/85400>

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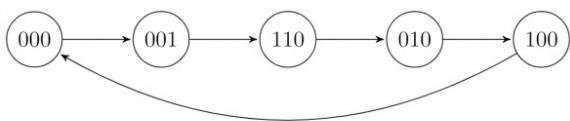
$Q_0$	$Q_1$	$Q_2$	$Q_{0N}$	$Q_{1N}$	$Q_{2N}$
0	0	0	0	0	1
0	0	1	1	1	0
0	1	0	1	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	1	0

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$$Q_{0N} = Q_0 \implies J_0 = Q_1 + Q_2, K_0 = 1$$

$$Q_{1N} = Q_1 \implies J_1 = Q_2, K_1 = \bar{Q}_0$$

$$Q_{2N} = Q_2 \implies J_2 = Q_1, K_2 = 1$$



$$0 - 1 - 6 - 2 - 4 - 0$$

So, MOD 5 counter.

25 votes

-- Akash Dinkar (27.9k points)

#### 4.30.3 Sequential Circuit: GATE CSE 1991 | Question: 5-c top

<https://gateoverflow.in/26442>



- ✓ In a JK flip flop the output toggles when both J and K inputs are 1. So, we must ensure that with each clock the output from the previous stage reaches the current stage.

Setup time is defined as the minimum amount of time before the clock's active edge that the data must be stable for it to be latched correctly

It is given that setup time is negligible - means as soon as data is stable, the next clock can be given.

- Time to get output from  $FF$  once input (and clock) is given =  $10\text{ns}$ . (Propagation Delay)
- Time for inputs to reach  $FF_1 = 0$ . (Zero AND gate)
- Time for inputs to reach  $FF_2 = 10$ . (One AND gate)
- Time for inputs to reach  $FF_3 = 20$ . (Two AND gates)

So, minimum time period needed for clock is  $10 + \max(0, 10, 20) = 10 + 20 = 30\text{ns}$  which would mean a maximum clock frequency of  $1/30\text{GHz} = 33.33\text{MHz}$

88 votes

-- Arjun Suresh (332k points)

#### 4.30.4 Sequential Circuit: GATE CSE 1994 | Question: 2-1 top

<https://gateoverflow.in/2468>



- ✓ Let say we have to design a mod-8 counter i.e 000 to 111. So we need 3 bits to represent i.e 3 FF.

For mod  $N : 2^x = N$

$$\implies x = \lceil (\log_2 N) \rceil$$

27 votes

-- Praveen Saini (41.9k points)

#### 4.30.5 Sequential Circuit: GATE CSE 2021 Set 1 | Question: 28 top

<https://gateoverflow.in/357423>



- ✓ From the given 3 state counter made from  $T$  flipflops, the next input sequence are as follows:

- $T_P = R$
- $T_Q = \overline{P}$
- $T_R = \overline{Q}$

Initial State			Current input			Next State		
P	Q	R	$T_P$	$T_Q$	$T_R$	$P^+$	$Q^+$	$R^+$
0	0	0	0	1	1	0	1	1
0	1	1	1	1	0	1	0	1
1	0	1	1	0	1	0	0	0

In  $T$  flip flop for low input(0), the next state is  $Q_n$  (current state) and for high input(1), it toggles/complements the present state ( $\overline{Q_n}$ )

011, 101, 000

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Option A is correct.

4 votes

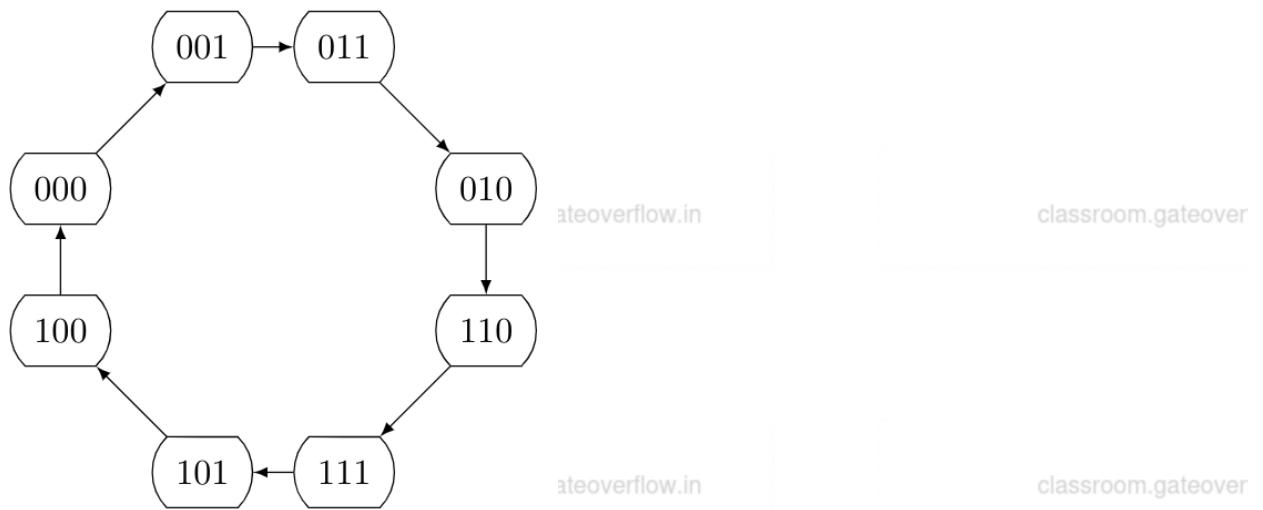
-- Hira (14.1k points)

#### 4.30.6 Sequential Circuit: GATE1992-04-c top

<https://gateoverflow.in/17408>



- ✓ State diagram will be as (remember concept of GRAY code)



State table and 3-bit synchronous counter with D FFs, will be as

Present State	Next State	FF Inputs
$ABC$	$\bar{A}\bar{B}\bar{C}$	$D_A D_B D_C$
001	011	011
000	001	001
010	110	110
011	010	010
100	000	000
101	100	100
110	111	111

		BC	00	01	11	10
		A	0	0	0	1
		0	0	0	0	1
		1	0	1	1	1

$$D_A = AC + BC$$

		BC	00	01	11	10
		A	0	0	1	1
		0	0	1	1	1
		1	0	0	0	1

$$D_B = \bar{A}C + B\bar{C}$$

		BC	00	01	11	10
		A	0	1	0	0
		0	1	1	0	0
		1	0	0	1	1

$$D_C = \bar{A}\bar{B} + AB = A \odot B$$

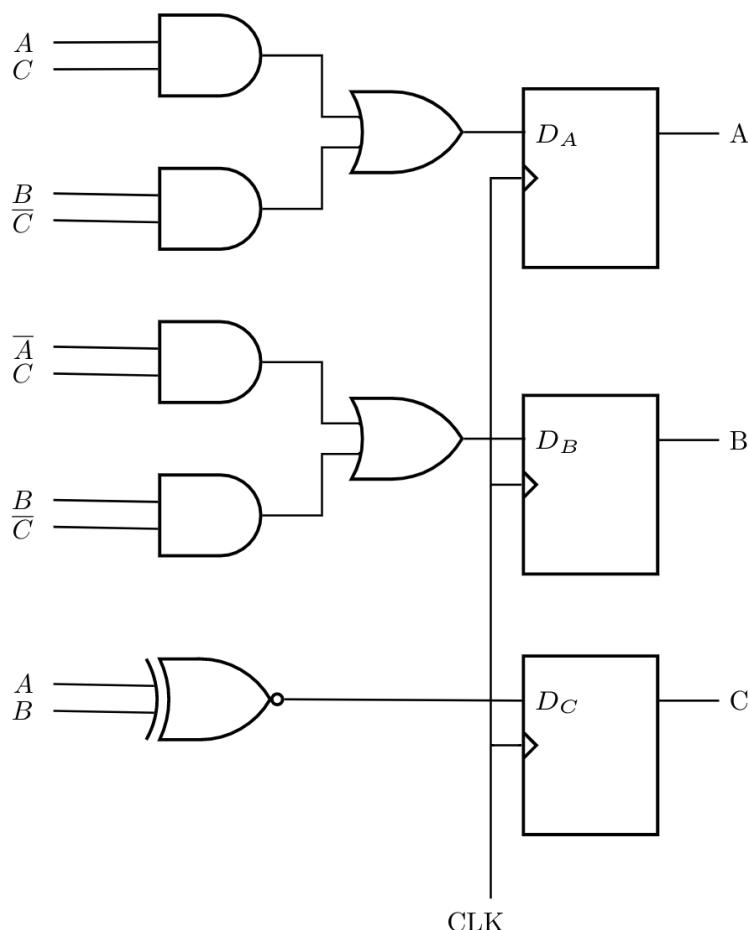
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29 votes

-- Praveen Saini (41.9k points)

4.31

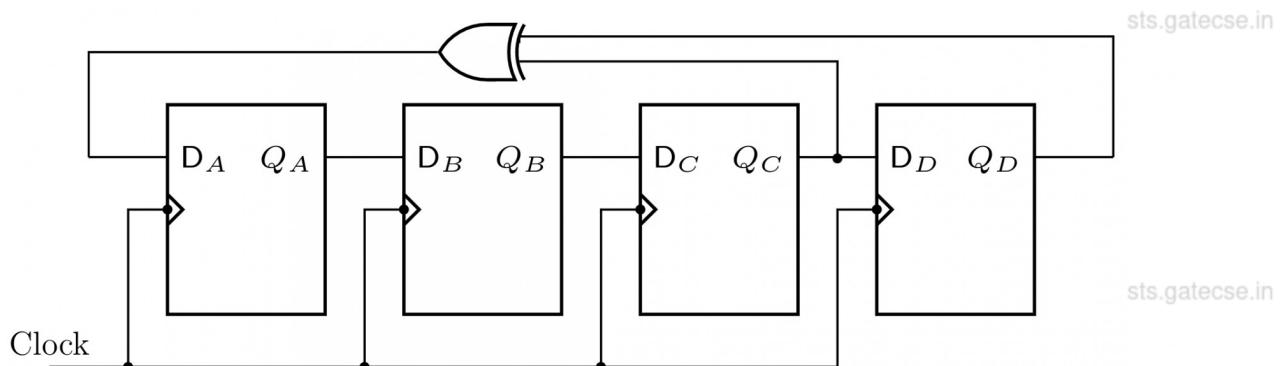
Shift Registers (2) top

#### 4.31.1 Shift Registers: GATE CSE 1987 | Question: 13-a top

<https://gateoverflow.in/82607>



The below figure shows four D-type flip-flops connected as a shift register using a XOR gate. The initial state and three subsequent states for three clock pulses are also given.



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State	$Q_A$	$Q_B$	$Q_C$	$Q_D$
Initial	1	1	1	1
After the first clock	0	1	1	1
After the second clock	0	0	1	1
After the third clock	0	0	0	1

The state  $Q_AQ_BQ_CQ_D$  after the fourth clock pulse is

- A. 0000

- B. 1111  
C. 1001  
D. 1000

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gate1987

digital-logic

circuit-output

sequential-circuit

digital-counter

shift-registers

Answer 

#### 4.31.2 Shift Registers: GATE CSE 1991 | Question: 06,a

<https://gateoverflow.in/532>



Using D flip-flop gates, design a parallel-in/serial-out shift register that shifts data from left to right with the following input lines:

- Clock CLK
- Three parallel data inputs  $A, B, C$
- Serial input  $S$
- Control input load/SHIFT.

gate1991

digital-logic

difficult

sequential-circuit

flip-flop

shift-registers

descriptive

Answer 

#### Answers: Shift Registers

#### 4.31.1 Shift Registers: GATE CSE 1987 | Question: 13-a

<https://gateoverflow.in/82607>



✓ Option (D) 1000

$Q_{An} = Q_C \oplus Q_D, Q_{Bn} = Q_A, Q_{Cn} = Q_B$  and  $Q_{Dn} = Q_C$

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QA	QB	QC	QD
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
<b>1</b>	<b>0</b>	<b>0</b>	<b>0</b>

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 13 votes

-- Prajwal Bhat (7.6k points)

#### 4.31.2 Shift Registers: GATE CSE 1991 | Question: 06,a

<https://gateoverflow.in/532>



Refer the Logic diagram for the parallel-in/serial-out SHIFT REGISTER, using D flip-flop gates that shifts data from left to right in this video : <https://youtu.be/7LmBcGiiYwk>

 0 votes

-- Pradip13 (17 points)

4.32

Static Hazard (1) 

#### 4.32.1 Static Hazard: GATE CSE 2006 | Question: 38

<https://gateoverflow.in/1814>



Consider a Boolean function  $f(w, x, y, z)$ . Suppose that exactly one of its inputs is allowed to change at a time. If the function happens to be true for two input vectors  $i_1 = \langle w_1, x_1, y_1, z_1 \rangle$  and  $i_2 = \langle w_2, x_2, y_2, z_2 \rangle$ , we would like the function to remain true as the input changes from  $i_1$  to  $i_2$  ( $i_1$  and  $i_2$  differ in exactly one bit position) without becoming false momentarily. Let  $f(w, x, y, z) = \sum(5, 7, 11, 12, 13, 15)$ . Which of the following cube covers of  $f$  will ensure that the required property is satisfied?

- tests.gatecse.in
- A.  $\bar{w}xz, \bar{w}\bar{y}, \bar{x}\bar{y}z, xyz, wyz$   
 B.  $wxy, \bar{w}xz, wyz$   
 C.  $wxyz, xz, wxyz$   
 D.  $wxy, wyz, wxz, \bar{w}xz, \bar{x}\bar{y}z, xyz$
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Answer 

## Answers: Static Hazard

4.32.1 Static Hazard: GATE CSE 2006 | Question: 38 [top](#)<https://gateoverflow.in/1814>

- ✓ The question is indirectly asking for static-1 hazard in the circuit - that is output becoming 0 momentarily when it is supposed to be 1.

Static 1 Hazard: Output going to 0 when it should remain 1

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- Happens in a 2 level SOP implementation.
- Suppose only one AND gate (minterm) is 1 in an SOP implementation.
- A variable in that minterm changes causing the output of that AND gate to become 0 and another AND gate to be 1.
- Depending on the propagation delay of the gates, the output can momentarily become 0 before finalizing on 1. For example, consider  $f = a'b' + ac$  and initially  $a = 0, b = 0, c = 1$ , so that output is 1. Now, if  $a$  changes to 1, again output should be 1 due to  $ac$  term. But if  $a'b'$  turns to 0 before  $ac$  turns to 1, output can be momentarily 0 causing a static-1 hazard.
- Can be detected in a K-map if there are any adjacent 1's not covered by an implicant. i.e., to avoid static hazard, all adjacent 1's in a K-map must be covered by some implicant. In the below K-map, the implicant shown in green ensures no static-1 hazard.

		bc	00	01	11	10
		a	0	1	0	0
		0	1	1	0	0
		1	0	1	1	0

Here  $f(w, x, y, z) = \sum(5, 7, 11, 12, 13, 15)$ 

So, K-map will be

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		yz	00	01	11	10
		wx	00	0	0	0
		01	0	1	1	0
		11	1	1	1	0
		10	0	0	1	0

So, its minimized sum of product expression will be  $xz + wxy' + wyz$ . Since all the minterms are overlapping, there is no chance of static hazard here.

Now, let's consider the options one by one:

A.  $\bar{w}xz, wxy, \bar{x}yz, xyz, wyz$ 

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		yz			
		00	01	11	10
		wx			
wx	00	0	0	0	0
	01	0	1	1	0
	11	1	1	1	0
	10	0	0	1	0

Chance of static hazard.

Here, when  $y$  changes from 0 to 1, the gate for  $wyz$  should give 1 (from earlier 0, assuming  $w = z = 1$ ) and that of  $xy'z$  should give 0 (from earlier 1). But there is a possibility of circuit giving 0 (static 1 hazard) momentarily due to gate delays ( $xy'z$  coming first and  $wyz$  coming later). In order to avoid this, we must add a gate with  $wxz$  also which ensure that all adjacent blocks in K-map are overlapped or a single variable change cannot momentarily change the circuit output.

B.  $wxy, \bar{w}xz, wyz$

This is not correct as  $wxy$  is not a minterm for the given function

C.  $wxy\bar{z}, xz, w\bar{x}yz$

		yz			
		00	01	11	10
		wx			
wx	00	0	0	0	0
	01	0	1	1	0
	11	1	1	1	0
	10	0	0	1	0

Here, also static-1 hazard is possible as the middle 4 pairs are separated by 1 bit difference to both  $wxy'z'$  as well as  $wx'yz$ . Could have been avoided by using  $wxy'$  instead of  $wxy'z'$  and  $wyz$  instead of  $wx'yz$  which will ensure that all neighboring blocks are overlapped.

D.  $wx\bar{y}, wyz, wxz, \bar{w}xz, \bar{x}yz, xyz$

		yz			
		00	01	11	10
		wx			
wx	00	0	0	0	0
	01	0	1	1	0
	11	1	1	1	0
	10	0	0	1	0

These minterms cover all the minterms of  $f$  and also, all the neighboring 1's are overlapped by minterms. So, no chance of hazard here, and hence is the required answer.

Correct Answer: D.

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56 votes      -- minal (13.1k points)

4.33

Synchronous Asynchronous Circuits (4) [top](#)

4.33.1 Synchronous Asynchronous Circuits: GATE CSE 1991 | Question: 03-ii [top](#)

<https://gateoverflow.in/516>



Advantage of synchronous sequential circuits over asynchronous ones is:  
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- A. faster operation

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- B. ease of avoiding problems due to hazards
- C. lower hardware requirement
- D. better noise immunity
- E. none of the above

[gate1991](#) [digital-logic](#) [normal](#) [sequential-circuit](#) [synchronous-asynchronous-circuits](#) [multiple-selects](#)

Answer 

#### 4.33.2 Synchronous Asynchronous Circuits: GATE CSE 1998 | Question: 16 [top](#)

<https://gateoverflow.in/1730>



Design a synchronous counter to go through the following states:

1, 4, 2, 3, 1, 4, 2, 3, 1, 4 ...

[gate1998](#) [digital-logic](#) [normal](#) [descriptive](#) [synchronous-asynchronous-circuits](#)

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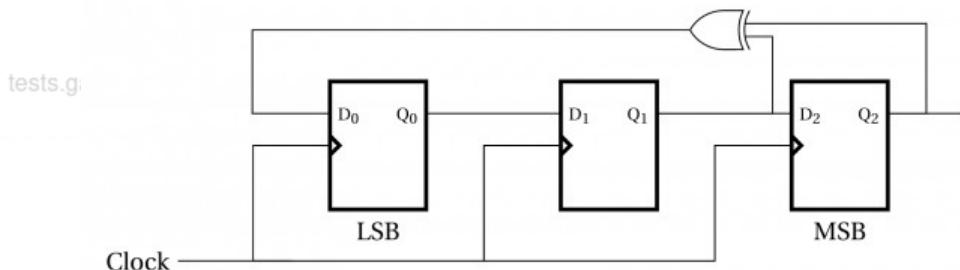
Answer 

#### 4.33.3 Synchronous Asynchronous Circuits: GATE CSE 2001 | Question: 2.12 [top](#)

<https://gateoverflow.in/730>



Consider the circuit given below with initial state  $Q_0 = 1, Q_1 = Q_2 = 0$ . The state of the circuit is given by the value  $4Q_2 + 2Q_1 + Q_0$



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Which one of the following is correct state sequence of the circuit?

- A. 1, 3, 4, 6, 7, 5, 2
- B. 1, 2, 5, 3, 7, 6, 4
- C. 1, 2, 7, 3, 5, 6, 4
- D. 1, 6, 5, 7, 2, 3, 4

[gate2001-cse](#) [digital-logic](#) [normal](#) [synchronous-asynchronous-circuits](#)

Answer 

#### 4.33.4 Synchronous Asynchronous Circuits: GATE CSE 2003 | Question: 44 [top](#)

<https://gateoverflow.in/935>



A 1-input, 2-output synchronous sequential circuit behaves as follows:

Let  $z_k, n_k$  denote the number of 0's and 1's respectively in initial  $k$  bits of the input  $(z_k + n_k = k)$ . The circuit outputs 00 until one of the following conditions holds.

- $z_k - n_k = 2$ . In this case, the output at the  $k$ -th and all subsequent clock ticks is 10.
- $n_k - z_k = 2$ . In this case, the output at the  $k$ -th and all subsequent clock ticks is 01.

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What is the minimum number of states required in the state transition graph of the above circuit?

- A. 5
- B. 6
- C. 7
- D. 8

[gate2003-cse](#) [digital-logic](#) [synchronous-asynchronous-circuits](#) [normal](#)

Answer 

## 4.33.1 Synchronous Asynchronous Circuits: GATE CSE 1991 | Question: 03-ii top

<https://gateoverflow.in/516>

- ✓ Synchronization means less chance of hazards but can only increase the delay. So, synchronous circuits cannot have faster operation than asynchronous one but it is easier to avoid hazards in synchronous circuits. So, (A) is false and (B) is true.

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(C) is false if we don't consider how to avoid the hazards in asynchronous circuits.

(D) Is not necessarily true - often asynchronous circuits have better noise immunity. Reasons are given here: <http://www.cs.columbia.edu/~nowick/async-applications-PIEEE-99-berkel-josephs-nowick-published.pdf>

[https://en.wikipedia.org/wiki/Asynchronous\\_circuit](https://en.wikipedia.org/wiki/Asynchronous_circuit)

## References



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25 votes

-- Arjun Suresh (332k points)

## 4.33.2 Synchronous Asynchronous Circuits: GATE CSE 1998 | Question: 16 top

<https://gateoverflow.in/1730>

- ✓ Sequence given is as

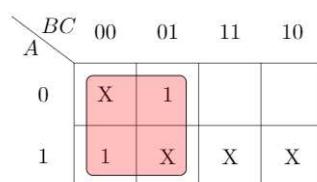
1, 4, 2, 3, 1 ...

From the given sequence of states we can design the state table and Suppose we are using T-FF for sequential circuit of counter.

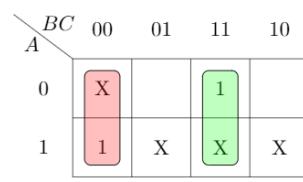
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Present State			Next State			FF Inputs		
A	B	C	$A^+$	$B^+$	$C^+$	$T_A$	$T_B$	$T_C$
0	0	0	x	x	x	x	x	x
0	0	1	1	0	0	1	0	1
0	1	0	0	1	1	0	0	1
0	1	1	0	0	1	0	1	0
1	0	0	0	1	0	1	1	0
1	0	1	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x

From the above table, we will find the equation of  $T_A$ ,  $T_B$  and  $T_C$

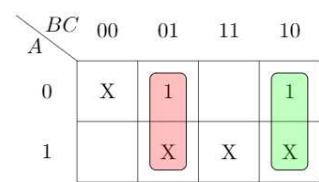


$$T_A = B'$$



$$T_B = B'C' + BC$$

$$T_B = B \oplus C$$



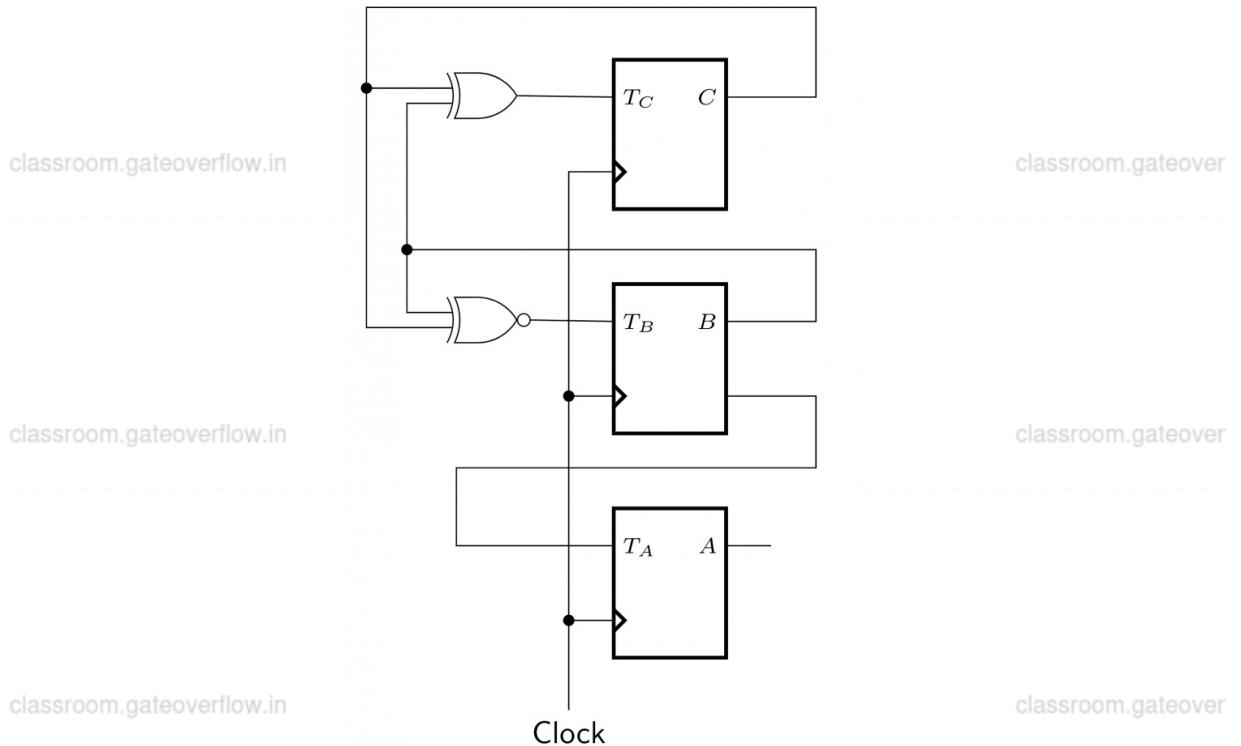
$$T_C = B'C + BC'$$

$$T_C = B \oplus C$$

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22 votes

-- Praveen Saini (41.9k points)

#### 4.33.3 Synchronous Asynchronous Circuits: GATE CSE 2001 | Question: 2.12 [top](#)

<https://gateoverflow.in/730>



$Q_0 = Q_{1\text{prev}} \oplus Q_{2\text{prev}}$	$Q_1 = Q_{0\text{prev}}$	$Q_2 = Q_{1\text{prev}}$
1	0	0
0	1	0
1	0	1
1	1	0
1	1	1
0	1	1
0	0	1
1	0	0

State =  $4Q_2 + 2Q_1 + Q_0$   
So, state sequence = 1, 2, 5, 3, 7, 6, 4

Correct Answer: B

41 votes

-- Arjun Suresh (332k points)

#### 4.33.4 Synchronous Asynchronous Circuits: GATE CSE 2003 | Question: 44 [top](#)

<https://gateoverflow.in/935>



- Though the question is from digital logic, the answer is purely from automata. As per the question, we just need to count the difference of the number of 0's and 1's in the first k bit of a number. And we just need to count till this count reaches 2 or -2 (negative when the number of 0's is less than the number of 1's). So, the possibilities are -2, -1, 0, 1 and 2 which represents the five states of the state transition diagram.

For state -2, the output of the circuit will be 01, for state 2, the output will be 10 (both these states not having any outgoing transitions) and for other 3 states, the output will be 00 as per the given description of the circuit.

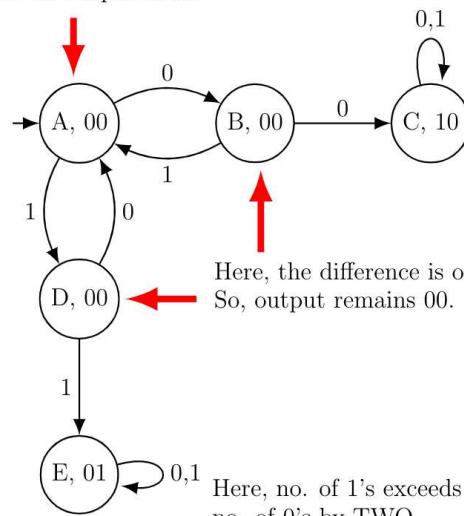
Correct Answer: A

59 votes

-- gatecse (63.3k points)

Initially difference between 0's and 1's is ZERO. So output is 00.

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Here, no. of 0's exceeds no. of 1's by TWO.  
Once this happens we will always output 10.

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Here, the difference is one.  
So, output remains 00.

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Here, no. of 1's exceeds no. of 0's by TWO.  
Once this happens we will always output 01.

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The Automaton will look like this. ☺

97 votes

-- Rajendra Kumar Dangwal (1.2k points)

## Answer Keys

4.1.1	N/A	4.1.2	N/A	4.1.3	N/A	4.1.4	B	4.1.5	B
4.1.6	A	4.1.7	B	4.1.8	19.2	4.1.9	B	4.1.10	-1
4.2.1	B	4.2.2	C	4.3.1	C	4.3.2	A	4.4.1	D
4.4.2	C	4.4.3	N/A	4.4.4	N/A	4.4.5	N/A	4.4.6	D
4.4.7	N/A	4.4.8	A	4.4.9	B	4.4.10	D	4.4.11	C
4.4.12	D	4.4.13	C	4.4.14	C	4.4.15	D	4.4.16	D
4.4.17	D	4.4.18	A	4.4.19	A	4.4.20	D	4.4.21	D
4.4.22	B	4.4.23	1	4.4.24	A	4.4.25	C	4.4.26	C
4.4.27	D	4.4.28	B	4.4.29	B;C;D	4.4.30	B	4.4.31	C
4.5.1	N/A	4.5.2	A	4.5.3	B	4.5.4	A	4.5.5	C
4.5.6	B	4.6.1	A	4.6.2	C	4.6.3	A	4.6.4	3
4.6.5	A	4.6.6	3	4.6.7	B	4.7.1	A	4.7.2	B
4.8.1	N/A	4.8.2	C	4.8.3	N/A	4.8.4	N/A	4.8.5	A;C
4.8.6	B	4.8.7	B	4.8.8	B	4.8.9	011	4.8.10	D
4.8.11	N/A	4.8.12	N/A	4.8.13	B	4.8.14	B	4.8.15	A
4.8.16	A	4.8.17	A	4.8.18	D	4.8.19	A	4.8.20	A
4.8.21	D	4.8.22	A	4.8.23	C	4.8.24	C	4.8.25	C
4.8.26	A	4.8.27	A	4.8.28	B	4.8.29	D	4.8.30	B

4.8.31	C	4.8.32	C	4.8.33	X	4.8.34	D	4.8.35	C
4.8.36	A	4.8.37	D	4.8.38	B	4.9.1	A	4.10.1	C
4.10.2	1034	4.11.1	B;C	4.11.2	N/A	4.11.3	N/A	4.11.4	D
4.11.5	D	4.11.6	A	4.11.7	C	4.12.1	N/A	4.12.2	N/A
4.12.3	A	4.12.4	C	4.12.5	D	4.12.6	3	4.12.7	4
4.12.8	B	4.12.9	D	4.12.10	D	4.13.1	D	4.14.1	D
4.14.2	C	4.15.1	N/A	4.15.2	C	4.15.3	A	4.15.4	B
4.15.5	2	4.15.6	D	4.16.1	C	4.16.2	N/A	4.16.3	N/A
4.16.4	N/A	4.16.5	N/A	4.16.6	C	4.16.7	D	4.16.8	D
4.16.9	B	4.17.1	N/A	4.17.2	N/A	4.17.3	B;C	4.17.4	A
4.18.1	D	4.18.2	B	4.18.3	A	4.18.4	C	4.18.5	-7.75 : -7.75
4.18.6	C	4.18.7	C	4.19.1	D	4.19.2	N/A	4.19.3	N/A
4.19.4	N/A	4.19.5	N/A	4.19.6	C	4.19.7	C	4.19.8	B
4.19.9	D	4.19.10	A	4.19.11	B	4.19.12	C	4.19.13	A
4.19.14	B	4.19.15	1	4.19.16	A	4.19.17	D	4.19.18	A
4.19.19	C	4.20.1	A;D	4.21.1	C	4.21.2	B	4.21.3	C
4.22.1	N/A	4.22.2	B	4.22.3	B	4.22.4	B	4.23.1	N/A
4.23.2	A	4.24.1	N/A	4.24.2	N/A	4.24.3	9	4.24.4	N/A
4.24.5	A	4.24.6	B	4.24.7	B	4.24.8	A	4.24.9	A
4.24.10	B	4.24.11	3	4.24.12	6 : 6	4.24.13	A	4.25.1	B
4.25.2	N/A	4.25.3	C	4.25.4	C	4.25.5	C	4.25.6	A
4.25.7	C	4.25.8	D	4.25.9	5	4.25.10	A	4.25.11	D
4.25.12	A	4.25.13	N/A	4.26.1	12	4.26.2	N/A	4.26.3	9
4.26.4	N/A	4.26.5	N/A	4.26.6	N/A	4.26.7	N/A	4.26.8	N/A
4.26.9	C	4.26.10	D	4.26.11	C	4.26.12	D	4.26.13	C
4.26.14	A;C	4.26.15	C	4.26.16	B	4.26.17	C	4.26.18	B
4.26.19	D	4.26.20	D	4.26.21	B	4.26.22	N/A	4.26.23	A
4.26.24	D	4.26.25	A	4.26.26	A	4.26.27	A	4.26.28	A
4.26.29	B	4.26.30	D	4.26.31	B	4.26.32	A	4.26.33	B
4.26.34	5	4.26.35	3	4.26.36	5	4.26.37	-11	4.26.38	1
4.26.39	C	4.26.40	D	4.26.41	0.502 : 0.504	4.26.42	C	4.26.43	C
4.26.44	A	4.26.45	3 : 3	4.26.46	B	4.26.47	A	4.26.48	A
4.26.49	C	4.26.50	A	4.26.51	B	4.27.1	False	4.28.1	C
4.28.2	A	4.29.1	N/A	4.29.2	D	4.29.3	D	4.29.4	B
4.30.1	C	4.30.2	N/A	4.30.3	33.33	4.30.4	N/A	4.30.5	A
4.30.6	N/A	4.31.1	D	4.31.2	N/A	4.32.1	D	4.33.1	B

4.33.2	N/A	4.33.3	B	4.33.4	A
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