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EDITION 3 GATE 2022



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led by

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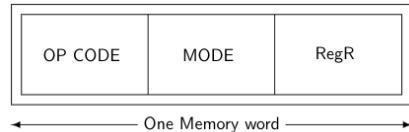
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Mode and RegR together specify the operand. RegR specifies a CPU register and Mode specifies an addressing mode. In particular, Mode = 2 specifies that 'the register RegR contains the address of the operand, after fetching the operand, the contents of RegR are incremented by 1'.

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An instruction at memory location 2000 specifies Mode = 2 and the RegR refers to program counter (PC).

- A. What is the address of the operand?
- B. Assuming that is a non-jump instruction, what are the contents of PC after the execution of this instruction?

gate1993 co-and-architecture addressing-modes normal descriptive

Answer

1.1.5 Addressing Modes: GATE CSE 1996 | Question: 1.16, ISRO2016-42 [top](#)

<https://gateoverflow.in/2720>



Relative mode of addressing is most relevant to writing:

- A. Co – routines
- B. Position – independent code
- C. Shareable code
- D. Interrupt Handlers

gate1996 co-and-architecture addressing-modes easy isro2016

Answer

1.1.6 Addressing Modes: GATE CSE 1998 | Question: 1.19 [top](#)

<https://gateoverflow.in/1656>



Which of the following addressing modes permits relocation without any change whatsoever in the code?

- A. Indirect addressing
- B. Indexed addressing
- C. Base register addressing
- D. PC relative addressing

gate1998 co-and-architecture addressing-modes easy

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Answer

1.1.7 Addressing Modes: GATE CSE 1999 | Question: 2.23 [top](#)

<https://gateoverflow.in/1500>



A certain processor supports only the immediate and the direct addressing modes. Which of the following programming language features cannot be implemented on this processor?

- A. Pointers
- B. Arrays
- C. Records
- D. Recursive procedures with local variable

gate1999 co-and-architecture addressing-modes normal multiple-selects

Answer

1.1.8 Addressing Modes: GATE CSE 2000 | Question: 1.10 [top](#)

<https://gateoverflow.in/633>



The most appropriate matching for the following pairs

- | | |
|------------------------------|--------------|
| X: Indirect addressing | 1: Loops |
| Y: Immediate addressing | 2: Pointers |
| Z: Auto decrement addressing | 3: Constants |

is

- A. $X - 3, Y - 2, Z - 1$
 B. $X - 1, Y - 3, Z - 2$
 C. $X - 2, Y - 3, Z - 1$
 D. $X - 3, Y - 1, Z - 2$

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gate2000-cse co-and-architecture normal addressing-modes

Answer ↗

1.1.9 Addressing Modes: GATE CSE 2001 | Question: 2.9 top ↗

↗ <https://gateoverflow.in/727>



Which is the most appropriate match for the items in the first column with the items in the second column:

X.	Indirect Addressing	I.	Array implementation
Y.	Indexed Addressing	II.	Writing relocatable code
Z.	Base Register Addressing	III.	Passing array as parameter

- A. (X, III), (Y, I), (Z, II)
 B. (X, II), (Y, III), (Z, I)
 C. (X, III), (Y, II), (Z, I)
 D. (X, I), (Y, III), (Z, II)

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gate2001-cse co-and-architecture addressing-modes normal

Answer ↗

1.1.10 Addressing Modes: GATE CSE 2002 | Question: 1.24 top ↗

↗ <https://gateoverflow.in/829>



In the absolute addressing mode:

- A. the operand is inside the instruction
- B. the address of the operand is inside the instruction
- C. the register containing the address of the operand is specified inside the instruction
- D. the location of the operand is implicit

gate2002-cse co-and-architecture addressing-modes easy

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Answer ↗

1.1.11 Addressing Modes: GATE CSE 2004 | Question: 20 top ↗

↗ <https://gateoverflow.in/1017>



Which of the following addressing modes are suitable for program relocation at run time?

- I. Absolute addressing
 - II. Based addressing
 - III. Relative addressing
 - IV. Indirect addressing
- A. I and IV
 B. I and II
 C. II and III
 D. I, II and IV

gate2004-cse co-and-architecture addressing-modes easy

goclasses.in

tests.gatecse.in

Answer ↗



Consider a three word machine instruction

$\text{ADD} A[R_0], @B$

The first operand (destination) “ $A[R_0]$ ” uses indexed addressing mode with R_0 as the index register. The second operand (source) “ $@B$ ” uses indirect addressing mode. A and B are memory addresses residing at the second and third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is:

- A. 3
- B. 4
- C. 5
- D. 6

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[gate2005-cse](#) [co-and-architecture](#) [addressing-modes](#) [normal](#)

Answer



Match each of the high level language statements given on the left hand side with the most natural addressing mode from those listed on the right hand side.

- | | |
|-------------------|-------------------------|
| (1) $A[I] = B[J]$ | (a) Indirect addressing |
| (2) while (*A++); | (b) Indexed addressing |
| (3) int temp = *x | (c) Auto increment |

- A. (1, c), (2, b), (3, a)
- B. (1, c), (2, c), (3, b)
- C. (1, b), (2, c), (3, a)
- D. (1, a), (2, b), (3, c)

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[gate2005-cse](#) [co-and-architecture](#) [addressing-modes](#) [easy](#)

Answer



Which of the following is/are true of the auto-increment addressing mode?

- I. It is useful in creating self-relocating code
 - II. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation
 - III. The amount of increment depends on the size of the data item accessed
-
- A. I only
 - B. II only
 - C. III only
 - D. II and III only

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[gate2008-cse](#) [addressing-modes](#) [co-and-architecture](#) [normal](#) [isro2009](#)

Answer



Consider a hypothetical processor with an instruction of type LW R1, 20(R2), which during execution reads a 32 – bit word from memory and stores it in a 32 – bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for the operand in memory?

- A. Immediate addressing
- B. Register addressing
- C. Register Indirect Scaled Addressing

D. Base Indexed Addressing

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gate2011-cse | co-and-architecture | addressing-modes | easy

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tests.gatecse.in

Answer 

1.1.16 Addressing Modes: GATE CSE 2017 Set 1 | Question: 11 [top](#)

<https://gateoverflow.in/118291>

Consider the C struct defined below:

```
struct data {  
    int marks [100];  
    char grade;  
    int cnumber;  
};  
struct data student;
```

The base address of student is available in register R1. The field student.grade can be accessed efficiently using:

- A. Post-increment addressing mode, $(R1) +$
- B. Pre-decrement addressing mode, $-(R1)$
- C. Register direct addressing mode, $R1$
- D. Index addressing mode, $X(R1)$, where X is an offset represented in 2's complement 16-bit representation

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gate2017-cse-set1 | co-and-architecture | addressing-modes

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tests.gatecse.in

Answer 

1.1.17 Addressing Modes: GATE IT 2006 | Question: 39, ISRO2009-42 [top](#)

<https://gateoverflow.in/3578>

Which of the following statements about relative addressing mode is FALSE?

- A. It enables reduced instruction size
- B. It allows indexing of array element with same instruction
- C. It enables easy relocation of data
- D. It enables faster address calculation than absolute addressing

gate2006-it | co-and-architecture | addressing-modes | normal | isro2009

Answer 

1.1.18 Addressing Modes: GATE IT 2006 | Question: 40 [top](#)

<https://gateoverflow.in/3581>

The memory locations 1000, 1001 and 1020 have data values 18, 1 and 16 respectively before the following program is executed.

MOVI	$R_s, 1$; Move immediate
LOAD	$R_d, 1000(R_s)$; Load from memory
ADDI	$R_d, 1000$; Add immediate
STOREI	$0(R_d), 20$; Store immediate

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tests.gatecse.in
Which of the statements below is TRUE after the program is executed ?

- A. Memory location 1000 has value 20
- B. Memory location 1020 has value 20
- C. Memory location 1021 has value 20
- D. Memory location 1001 has value 20

gate2006-it | co-and-architecture | addressing-modes | normal

Answer 

Answers: Addressing Modes

1.1.1 Addressing Modes: GATE CSE 1987 | Question: 1-V [top](#)

<https://gateoverflow.in/80194>

- ✓ (C) Relative Mode since we can just change the content of base register if we wish to relocate.

REFERENCE: <https://gateoverflow.in/155280/self-doubt-computer-organization?show=155312>

References



26 votes

classroom.gateover

-- srestha (85.2k points)

1.1.2 Addressing Modes: GATE CSE 1988 | Question: 9iii [top](#)

<https://gateoverflow.in/94388>



MOV instructions here are problematic for Position Independent behaviour if they use Indexed addressing mode and the base address is loaded using some Absolute value.

I'm assuming R_0 is having some relative address. So, the first two MOV instructions are fine for Position Independent behaviour.

But $\text{MOV } 2(R_0), R_1$

is not fine for position independent behaviour as the source operand address here is $2 + R_0 = 2 + X$ which remains the same even when program is loaded to a new address. So, it should catch invalid content when program is loaded to a new address.

Similarly the last MOV will also cause problem.

5 votes

-- Arjun Suresh (332k points)

1.1.3 Addressing Modes: GATE CSE 1989 | Question: 2-ii [top](#)

<https://gateoverflow.in/87078>



(A) Base addressing	(s) Position independent (By changing the value in base register, location of address can be changed)
(B) Indexed addressing	(r) Array
(C) Stack addressing	(p) Reentrancy (Whenever code happens to be used again, address need not be the same)
(D) Implied addressing	(q) Accumulator (If an address is not specified, it is assumed/implied to be the Accumulator)

32 votes

-- Prashant Singh (47.2k points)

1.1.4 Addressing Modes: GATE CSE 1993 | Question: 10 [top](#)

<https://gateoverflow.in/2307>



- A. Address of the operand = content of PC = 2001 as PC holds the address of the next instruction to be executed and instruction size is 1 – word as given in the diagram.
- B. After execution of the current instruction PC will be automatically incremented by 1 when the next instruction is fetched. Also one extra increment will be done by operand fetch. So, PC = 2003 supposing next instruction is fetched. If we assume next instruction fetch is not done (this should be the default here), it should be 2002.

31 votes

-- Arjun Suresh (332k points)

1.1.5 Addressing Modes: GATE CSE 1996 | Question: 1.16, ISRO2016-42 [top](#)

<https://gateoverflow.in/2720>



- ✓ Answer is (B).

Relative mode addressing is most relevant to writing a position-independent code.

Reference: http://en.wikipedia.org/wiki/Addressing_mode#PC-relative

References

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1 26 votes

-- Rajarshi Sarkar (27.9k points)

1.1.6 Addressing Modes: GATE CSE 1998 | Question: 1.19 top ↴

<https://gateoverflow.in/1656>



- ✓ (D) PC relative addressing is the best option. For Base register addressing, we have to change the address in the base register while in PC relative there is absolutely no change in code needed.

1 36 votes

-- Arjun Suresh (332k points)

1.1.7 Addressing Modes: GATE CSE 1999 | Question: 2.23 top ↴

<https://gateoverflow.in/1500>



- ✓ Pointer access requires indirect addressing which can be simulated with indexed addressing or register indirect addressing but not with direct and immediate addressing. An array and record access needs a pointer access. So, options (A), (B) and (C) cannot be implemented on such a processor.

Now, to handle recursive procedures we need to use stack. A local variable inside the stack will be accessed as $*(SP + \text{offset})$ which is nothing but a pointer access and requires indirect addressing. Usually this is done by moving the **SP** value to Base register and then using Base Relative addressing to avoid unnecessary memory accesses for indirect addressing- but not possible with just direct and immediate addressing.

So, options (A), (B), (C) and (D) are correct.

1 70 votes

-- Arjun Suresh (332k points)

1.1.8 Addressing Modes: GATE CSE 2000 | Question: 1.10 top ↴

<https://gateoverflow.in/633>



- ✓ (C) is the most appropriate one.

General instruction format: **[opcode|Mode|Address Field]**

Pointer dereference → Indirect addressing, $E.A = M$ [Value stored in address field]

Operating with a constant → Immediate addressing, $E.A = \text{Value}$ of the instruction.

Loop iteration counter check → Auto decrement addressing $R1 = R1 - 1$; $E.A = R1$

E.A = Effective address, where the required operand will be found.

1 28 votes

-- Bhagirathi Nayak (11.7k points)

1.1.9 Addressing Modes: GATE CSE 2001 | Question: 2.9 top ↴

<https://gateoverflow.in/727>



- ✓ (A) is the answer.

Array implementation can use Indexed addressing.

While passing array as parameter we can make use of a pointer (as in (C)) and hence can use Indirect addressing.

Base Register addressing can be used to write relocatable code by changing the content of Base Register.

1 49 votes

-- Arjun Suresh (332k points)

1.1.10 Addressing Modes: GATE CSE 2002 | Question: 1.24 top ↴

<https://gateoverflow.in/829>



- ✓ (B) is the answer. Absolute addressing mode means address of operand is given in the instruction.

option (A), operand is inside the instruction → immediate addressing

option (C), register containing the address is specified in operand → register Indirect addressing

option (D), the location of operand is implicit → implicit addressing

60 votes

-- gatecse (63.3k points)

1.1.11 Addressing Modes: GATE CSE 2004 | Question: 20 [top](#)

<https://gateoverflow.in/1017>



- ✓ Answer: (C)

A displacement type addressing should be preferred. So, (I) is not the answer.

Indirect Addressing leads to extra memory reference which is not preferable at run time. So, (IV) is not the answer.

33 votes

-- Rajarshi Sarkar (27.9k points)

1.1.12 Addressing Modes: GATE CSE 2005 | Question: 65 [top](#)

<https://gateoverflow.in/1388>

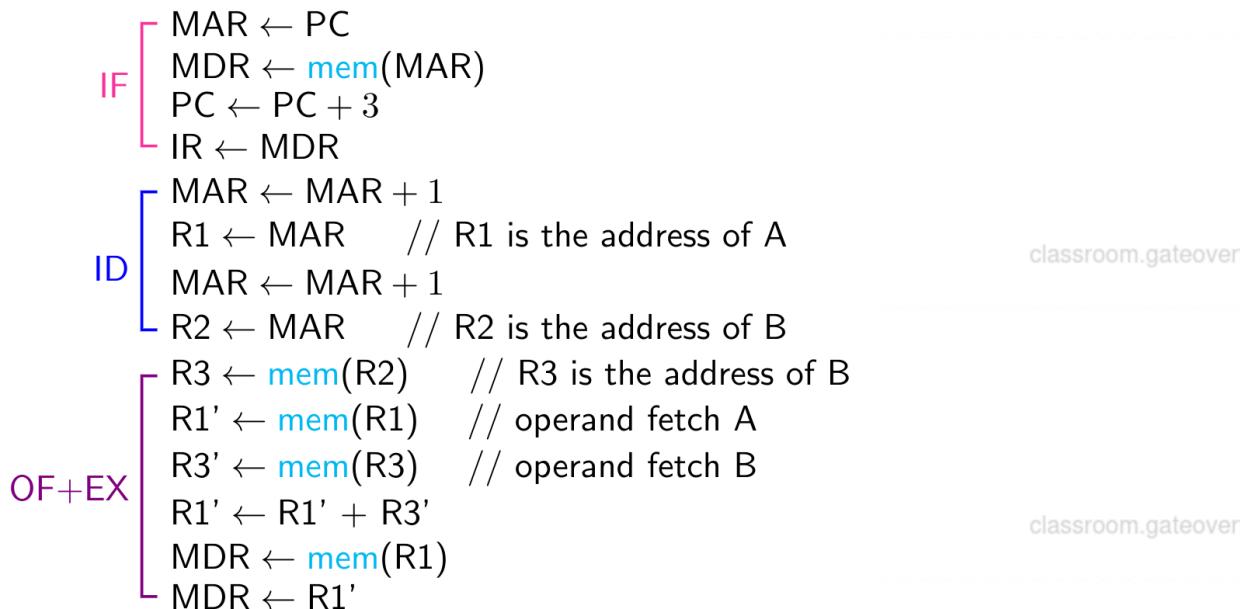


- ✓ 1 memory read to get the first operand from memory address $A + R_0$ (A is given as part of instruction)
1 memory read to get the address of the second operand (since second uses indirect addressing)
1 memory read to get the second operand from the address given by the previous memory read
1 memory write to store to first operand (which is the destination)

So, total of 4 memory cycles once the instruction is fetched.

The second and third words of the instruction are loaded as part of the Instruction fetch and not during the execute stage.

Reference: <http://www.cs.iit.edu/~cs561/cs350/fetch/fetch.html>



Correct Answer: B

References



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121 votes

-- Arjun Suresh (332k points)

1.1.13 Addressing Modes: GATE CSE 2005 | Question: 66 [top](#)

<https://gateoverflow.in/1389>



- ✓ C is the answer.

- $A[i] = B[j]$; Indexed addressing

- while ($*A++$); Auto increment
- temp = $*x$; Indirect addressing

32 votes

-- Arjun Suresh (332k points)

1.1.14 Addressing Modes: GATE CSE 2008 | Question: 33, ISRO2009-80 [top](#)

<https://gateoverflow.in/444>



- ✓ In auto increment addressing mode, the base address is incremented after operand fetch. This is useful in fetching elements from an array. But this has no effect in self-relocating code (where code can be loaded to any address) as this works on the basis of an initial base address.

An additional ALU is desirable for better execution especially with pipelining, but never a necessity.

Amount of increment depends on the size of the data item accessed as there is no need to fetch a part of a data. So, answer must be C only.

79 votes

-- Arjun Suresh (332k points)

1.1.15 Addressing Modes: GATE CSE 2011 | Question: 21 [top](#)

<https://gateoverflow.in/2123>



- ✓ Answer is (D).

Base Index Addressing, as the content of register R2 will serve as the index and 20 will be the Base address.

49 votes

-- Rajarshi Sarkar (27.9k points)

1.1.16 Addressing Modes: GATE CSE 2017 Set 1 | Question: 11 [top](#)

<https://gateoverflow.in/118291>



- ✓ Answer is option (D).

Displacement Mode :-

Similar to index mode, except instead of a index register a base register will be used. Base register contains a pointer to a memory location. An integer (constant) is also referred to as a displacement. The address of the operand is obtained by adding the contents of the base register plus the constant. The difference between index mode and displacement mode is in the number of bits used to represent the constant. When the constant is represented a number of bits to access the memory, then we have index mode. Index mode is more appropriate for array accessing; displacement mode is more appropriate for structure (records) accessing.

Reference:

<http://www.cs.iit.edu/~cs561/cs350/addressing/addsclm.html>

References



50 votes

-- Niraj Raghuvanshi (263 points)

1.1.17 Addressing Modes: GATE IT 2006 | Question: 39, ISRO2009-42 [top](#)

<https://gateoverflow.in/3578>



- is true as instead of absolute address we can use a much smaller relative address in instructions which results in smaller instruction size.
- By using the base address of array as displacement and index in a base register (base relative addressing mode) we can index array elements using relative addressing.
Ref: http://service.scs.carleton.ca/sivarama/asm_book_web/Instructor_copies/ch5_addrmodes.pdf
- is true as we only need to change the base address in case of relocation- instructions remain the same.
- is false. Relative addressing cannot be faster than absolute addressing as absolute address must be calculated from relative address. With specialized hardware unit, this can perform equally as good as absolute addressing but not faster.

Correct Answer: D

References



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71 votes

-- Arjun Suresh (332k points)

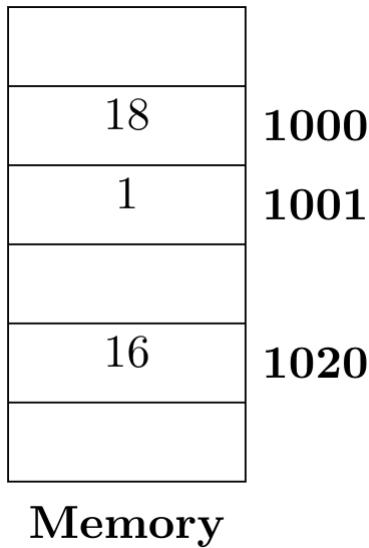
1.1.18 Addressing Modes: GATE IT 2006 | Question: 40 [top](#)

<https://gateoverflow.in/3581>



- ✓ Before the execution of the program, the memory contents are-

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Memory

Now, let's execute the program instructions one by one-

1. **Instruction-01: MOVI R_s, 1**

- This instruction uses immediate addressing mode.
- The instruction is interpreted as $R_s \leftarrow 1$.
- Thus, value = 1 is moved to the register R_s .

2. **Instruction-02: LOAD R_d, 1000 (R_s)**

- This instruction uses indexed addressing mode.
- The instruction is interpreted as $R_d \leftarrow [1000 + [R_s]]$.
- Value of the operand = $[1000 + [R_s]] = [1000 + 1] = [1001] = 1$.
- Thus, value = 1 is moved to the register R_d .

3. **Instruction-03: ADDI R_d, 1000**

- This instruction uses immediate addressing mode.
- The instruction is interpreted as $R_d \leftarrow [R_d] + 1000$.
- Value of the operand = $[R_d] + 1000 = 1 + 1000 = 1001$.
- Thus, value = 1001 is moved to the register R_d .

4. **Instruction-04: STOREI 0(R_d), 20**

- This instruction uses indexed addressing mode.
- The instruction is interpreted as $0 + [R_d] \leftarrow 20$.
- Value of the destination address = $0 + [R_d] = 0 + 1001 = 1001$.
- Thus, value = 20 is moved to the memory location 1001.

Hence, after the program execution is completed, memory location 1001 has a value 20.

Option D is correct.

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39 votes

-- Sambhrant Maurya (2.6k points)

D is the answer. Memory location 1001 has value 20.

$R_s \leftarrow 1$ (Immediate Addressing)

$R_d \leftarrow 1$ (Indexed Addressing, value at memory location $1 + 1000 = 1001$ is loaded to R_d which is 1)

$R_d \leftarrow 1001$ (R_d becomes $1 + 1000$)

store in address $1001 \leftarrow 20$

49 votes

-- Abhinav Rana (723 points)

1.2

Cache Memory (63) top

1.2.1 Cache Memory: GATE CSE 1987 | Question: 4b top

<https://gateoverflow.in/81360>



What is cache memory? What is rationale of using cache memory?

gate1987 co-and-architecture cache-memory descriptive

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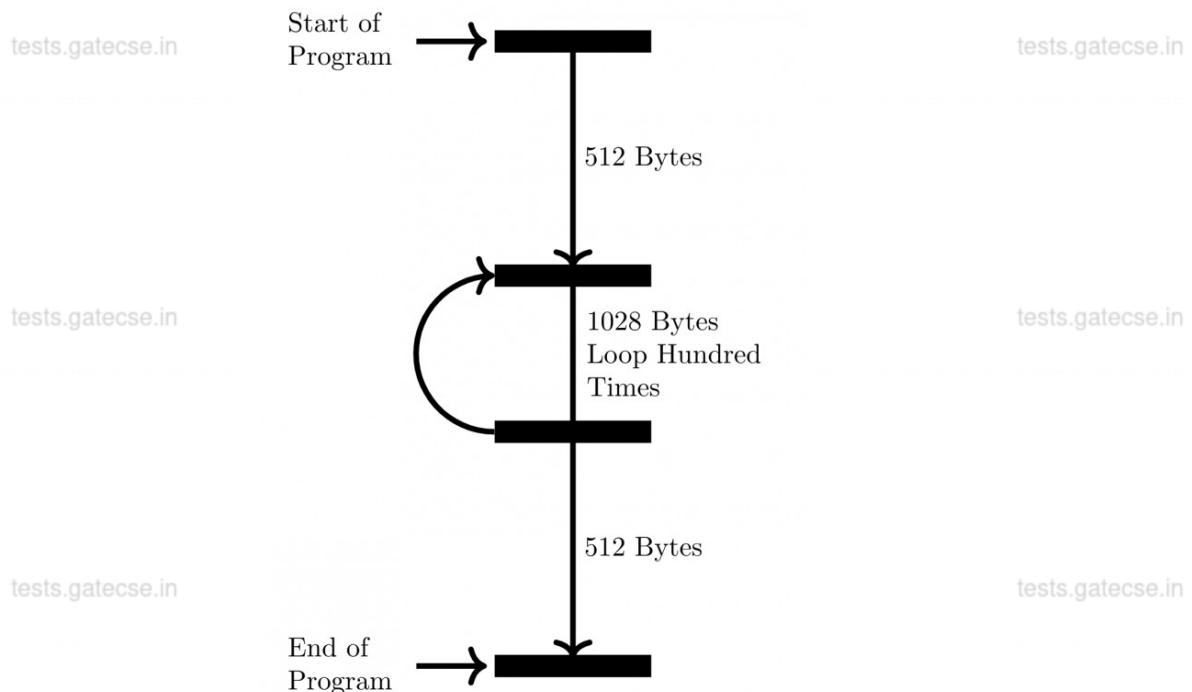
Answer

1.2.2 Cache Memory: GATE CSE 1989 | Question: 6a top

<https://gateoverflow.in/88557>



A certain computer system was designed with cache memory of size 1 Kbytes and main memory size of 256 Kbytes. The cache implementation was fully associative cache with 4 bytes per block. The CPU memory data path was 16 bits and the memory was 2-way interleaved. Each memory read request presents two 16-bit words. A program with the model shown below was run to evaluate the cache design.



Answer the following questions:

- What is the hit ratio?
- Suggest a change in the program size of model to improve the hit ratio significantly.

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Answer



A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight bit words.

1. How many bits are required for addressing the main memory?
2. How many bits are needed to represent the TAG, SET and WORD fields?

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gate1990 descriptive co-and-architecture cache-memory

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Answer



The access times of the main memory and the Cache memory, in a computer system, are 500 n sec and 50 nsec, respectively. It is estimated that 80% of the main memory request are for read the rest for write. The hit ratio for the read access only is 0.9 and a write-through policy (where both main and cache memories are updated simultaneously) is used. Determine the average time of the main memory (in ns).

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Answer



In the three-level memory hierarchy shown in the following table, p_i denotes the probability that an access request will refer to M_i .

Hierarchy Level (M_i)	Access Time (t_i)	Probability of Access (p_i)	Page Transfer Time (T_i)
M_1	10^{-6}	0.99000	0.001 sec
M_2	10^{-5}	0.00998	0.1 sec
M_3	10^{-4}	0.00002	---

If a miss occurs at level M_i , a page transfer occurs from M_{i+1} to M_i and the average time required for such a page swap is T_i . Calculate the average time t_A required for a processor to read one word from this memory system.

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Answer



The principle of locality justifies the use of:

- A. Interrupts
- B. DMA
- C. Polling
- D. Cache Memory

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Answer



A computer system has a $4 K$ word cache organized in block-set-associative manner with 4 blocks per set, 64 words per block. The number of bits in the SET and WORD fields of the main memory address format is:

- A. 15, 40
- B. 6, 4
- C. 7, 2
- D. 4, 6

Answer **1.2.8 Cache Memory: GATE CSE 1996 | Question: 26** top ↺<https://gateoverflow.in/2778>

A computer system has a three-level memory hierarchy, with access time and hit ratios as shown below:

Level 1 (Cache memory) Access time = 50nsec/byte

Size	Hit ratio
8M bytes	0.80
16M bytes	0.90
64M bytes	0.95

Level 2 (Main memory) Access time = 200nsec/byte

Size	Hit ratio
4M bytes	0.98
16M bytes	0.99
64M bytes	0.995

Level 3 Access time = 5μsec/byte

Size	Hit ratio
260M bytes	1.0

- A. What should be the minimum sizes of level 1 and 2 memories to achieve an average access time of less than 100nsec?
- B. What is the average access time achieved using the chosen sizes of level 1 and level 2 memories?

Answer **1.2.9 Cache Memory: GATE CSE 1998 | Question: 18** top ↺<https://gateoverflow.in/1732>

For a set-associative Cache organization, the parameters are as follows:

t_c	Cache Access Time
t_m	Main memory access time
l	Number of sets
b	Block size
$k \times b$	Set size

Calculate the hit ratio for a loop executed 100 times where the size of the loop is $n \times b$, and $n = k \times m$ is a non-zero integer and $1 \leq m \leq l$.

Give the value of the hit ratio for $l = 1$.

Answer **1.2.10 Cache Memory: GATE CSE 1999 | Question: 1.22** top ↺<https://gateoverflow.in/1475>

The main memory of a computer has 2^m blocks while the cache has 2^n blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block k of the main memory maps to the set:

- A. $(k \bmod m)$ of the cache
- B. $(k \bmod n)$ of the cache
- C. $(k \bmod 2^n)$ of the cache
- D. $(k \bmod 2^{m+n})$ of the cache

Answer **1.2.11 Cache Memory: GATE CSE 2001 | Question: 1.7, ISRO2008-18** top ↺<https://gateoverflow.in/700>

More than one word are put in one cache block to:

- A. exploit the temporal locality of reference in a program
- B. exploit the spatial locality of reference in a program
- C. reduce the miss penalty
- D. none of the above

Answer **1.2.12 Cache Memory: GATE CSE 2001 | Question: 9** top ↗<https://gateoverflow.in/750>

A CPU has $32 - bit$ memory address and a $256 KB$ cache memory. The cache is organized as a $4 - way$ set associative cache with cache block size of 16 bytes.

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- A. What is the number of sets in the cache?
- B. What is the size (in bits) of the tag field per cache block?
- C. What is the number and size of comparators required for tag matching?
- D. How many address bits are required to find the byte offset within a cache block?
- E. What is the total amount of extra memory (in bytes) required for the tag bits?

Answer **1.2.13 Cache Memory: GATE CSE 2002 | Question: 10** top ↗<https://gateoverflow.in/863>

In a C program, an array is declared as $\text{float } A[2048]$. Each array element is 4 Bytes in size, and the starting address of the array is $0x00000000$. This program is run on a computer that has a direct mapped data cache of size 8 Kbytes, with block (line) size of 16 Bytes.

- A. Which elements of the array conflict with element $A[0]$ in the data cache? Justify your answer briefly.
- B. If the program accesses the elements of this array one by one in reverse order i.e., starting with the last element and ending with the first element, how many data cache misses would occur? Justify your answer briefly. Assume that the data cache is initially empty and that no other data or instruction accesses are to be considered.

Answer **1.2.14 Cache Memory: GATE CSE 2004 | Question: 65** top ↗<https://gateoverflow.in/1059>

Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is:

8, 12, 0, 12, 8.

- A. 2
- B. 3
- C. 4
- D. 5

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Answer **1.2.15 Cache Memory: GATE CSE 2005 | Question: 67** top ↗<https://gateoverflow.in/1390>

Consider a direct mapped cache of size $32 KB$ with block size $32 bytes$. The CPU generates $32 bit$ addresses. The number of bits needed for cache indexing and the number of tag bits are respectively,

- A. 10, 17
- B. 10, 22
- C. 15, 17
- D. 5, 17

Answer 



Consider two cache organizations. First one is 32 KB 2-way set associative with 32 byte block size, the second is of same size but direct mapped. The size of an address is 32 bits in both cases. A 2-to-1 multiplexer has latency of 0.6 ns while a k -bit comparator has latency of $\frac{k}{10}$ ns. The hit latency of the set associative organization is h_1 while that of direct mapped is h_2 .

The value of h_1 is:

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- A. 2.4 ns
- B. 2.3 ns
- C. 1.8 ns
- D. 1.7 ns

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[Answer](#)



Consider two cache organizations. First one is 32 kB 2-way set associative with 32 byte block size, the second is of same size but direct mapped. The size of an address is 32 bits in both cases. A 2-to-1 multiplexer has latency of 0.6 ns while a k -bit comparator has latency of $\frac{k}{10}$ ns. The hit latency of the set associative organization is h_1 while that of direct mapped is h_2 .

The value of h_2 is:

- A. 2.4 ns
- B. 2.3 ns
- C. 1.8 ns
- D. 1.7 ns

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[Answer](#)



A CPU has a 32KB direct mapped cache with 128 byte-block size. Suppose A is two dimensional array of size 512×512 with elements that occupy 8-bytes each. Consider the following two C code segments, $P1$ and $P2$.

P1:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x += A[i][j];
    }
}
```

P2:

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$P1$ and $P2$ are executed independently with the same initial state, namely, the array A is not in the cache and i ,

j , tests.gatecse.in goclasses.in tests.gatecse.in x are in registers. Let the number of cache misses experienced by $P1$ be M_1 and that for $P2$ be M_2 .

The value of M_1 is:

- A. 0
- B. 2048
- C. 16384
- D. 262144

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[Answer](#)



A CPU has a 32 KB direct mapped cache with 128 byte-block size. Suppose A is two dimensional array of size 512×512 with elements that occupy $8 - bytes$ each. Consider the following two C code segments, $P1$ and $P2$.

P1:

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```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x += A[i][j];
    }
}
```

P2:

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```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x += A[j][i];
    }
}
```

$P1$ and $P2$ are executed independently with the same initial state, namely, the array A is not in the cache and i, j, x are in registers. Let the number of cache misses experienced by $P1$ be M_1 and that for $P2$ be M_2 .

The value of the ratio $\frac{M_1}{M_2}$:

A. 0

B. $\frac{1}{16}$ C. $\frac{1}{8}$

D. 16

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Answer



Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a $20 - bit$ address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively:

- A. 9, 6, 5
- B. 7, 7, 6
- C. 7, 5, 8
- D. 9, 5, 6

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Answer



Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50×50 two-dimensional array of bytes is stored in the main memory starting from memory location $1100H$. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

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How many data misses will occur in total?

- A. 48
- B. 50
- C. 56
- D. 59

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Answer



Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50×50 two-dimensional array of bytes is stored in the main memory starting from memory location $1100H$. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

Which of the following lines of the data cache will be replaced by new blocks in accessing the array for the second time?

- A. line 4 to line 11
- B. line 4 to line 12
- C. line 0 to line 7
- D. line 0 to line 8

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[Answer](#)

1.2.23 Cache Memory: GATE CSE 2008 | Question: 35 [top](#)

<https://gateoverflow.in/446>



For inclusion to hold between two cache levels L_1 and L_2 in a multi-level cache hierarchy, which of the following are necessary?

- I. L_1 must be write-through cache
 - II. L_2 must be a write-through cache
 - III. The associativity of L_2 must be greater than that of L_1
 - IV. The L_2 cache must be at least as large as the L_1 cache
- A. IV only
 - B. I and IV only
 - C. I, II and IV only
 - D. I, II, III and IV

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[Answer](#)

1.2.24 Cache Memory: GATE CSE 2008 | Question: 71 [top](#)

<https://gateoverflow.in/494>



Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array ARR is located in memory starting at the beginning of virtual page $0xFF000$ and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR .

The total size of the tags in the cache directory is:

- A. 32 Kbits
- B. 34 Kbits
- C. 64 Kbits
- D. 68 Kbits

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[Answer](#)

1.2.25 Cache Memory: GATE CSE 2008 | Question: 72 [top](#)

<https://gateoverflow.in/43490>



Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
```

```
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

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The size of double is 8 bytes. Array ARR is located in memory starting at the beginning of virtual page $0xFF000$ and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR .

Which of the following array elements have the same cache index as $ARR[0][0]$?

- A. $ARR[0][4]$
- B. $ARR[4][0]$
- C. $ARR[0][5]$
- D. $ARR[5][0]$

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Answer 

1.2.26 Cache Memory: GATE CSE 2008 | Question: 73 [top](#) <https://gateoverflow.in/43491>

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Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes . The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes . A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array ARR is located in memory starting at the beginning of virtual page $0xFF000$ and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR .

The cache hit ratio for this initialization loop is:

- A. 0%
- B. 25%
- C. 50%
- D. 75%

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Answer 

1.2.27 Cache Memory: GATE CSE 2009 | Question: 29 [top](#) <https://gateoverflow.in/1315>

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Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks are in the following order:

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155.

Which one of the following memory block will NOT be in cache if LRU replacement policy is used?

- A. 3
- B. 8
- C. 129
- D. 216

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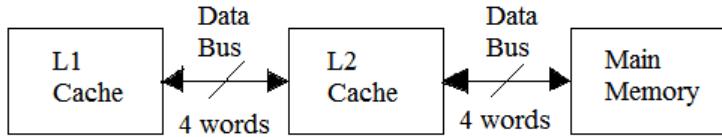
Answer 

1.2.28 Cache Memory: GATE CSE 2010 | Question: 48 [top](#) <https://gateoverflow.in/2352>

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A computer system has an $L1$ cache, an $L2$ cache, and a main memory unit connected as shown below. The block size in $L1$ cache is 4 words. The block size in $L2$ cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for $L1$ cache, $L2$ cache and the main memory unit respectively.



When there is a miss in L_1 cache and a hit in L_2 cache, a block is transferred from L_2 cache to L_1 cache. What is the time taken for this transfer?

- A. 2 nanoseconds
- B. 20 nanoseconds
- C. 22 nanoseconds
- D. 88 nanoseconds

gate2010-cse co-and-architecture cache-memory normal barc2017

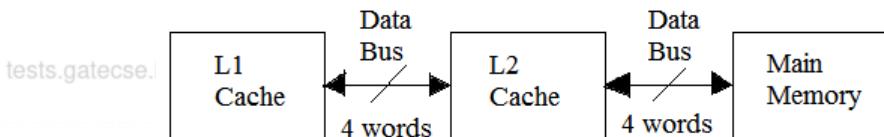
[Answer](#)

1.2.29 Cache Memory: GATE CSE 2010 | Question: 49

<https://gateoverflow.in/43329>



A computer system has an L_1 cache, an L_2 cache, and a main memory unit connected as shown below. The block size in L_1 cache is 4 words. The block size in L_2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L_1 cache, L_2 cache and the main memory unit respectively.



When there is a miss in both L_1 cache and L_2 cache, first a block is transferred from main memory to L_2 cache, and then a block is transferred from L_2 cache to L_1 cache. What is the total time taken for these transfers?

- A. 222 nanoseconds
- B. 888 nanoseconds
- C. 902 nanoseconds
- D. 968 nanoseconds

gate2010-cse co-and-architecture cache-memory normal

[Answer](#)

1.2.30 Cache Memory: GATE CSE 2011 | Question: 43

<https://gateoverflow.in/2145>



An 8KB direct-mapped write-back cache is organized as multiple blocks, each size of 32-bytes. The processor generates 32-bit addresses. The cache controller contains the tag information for each cache block comprising of the following.

- 1 valid bit
- 1 modified bit
- As many bits as the minimum needed to identify the memory block mapped in the cache.

What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

- A. 4864 bits
- B. 6144 bits
- C. 6656 bits
- D. 5376 bits

gate2011-cse co-and-architecture cache-memory normal

[Answer](#)



A computer has a 256-KByte, 4-way set associative, write back data cache with block size of 32-Bytes. The processor sends 32-bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The number of bits in the tag field of an address is

- A. 11
- B. 14
- C. 16
- D. 27

[gate2012-cse](#) [co-and-architecture](#) [cache-memory](#) [normal](#)

[Answer](#)

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A computer has a 256-KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The size of the cache tag directory is:

- A. 160 Kbits
- B. 136 Kbits
- C. 40 Kbits
- D. 32 Kbits

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[normal](#) [gate2012-cse](#) [co-and-architecture](#) [cache-memory](#)

[Answer](#)



In a k -way set associative cache, the cache is divided into v sets, each of which consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set $(s + 1)$. The main memory blocks are numbered 0 onwards. The main memory block numbered j must be mapped to any one of the cache lines from

- A. $(j \bmod v) * k$ to $(j \bmod v) * k + (k - 1)$
- B. $(j \bmod v)$ to $(j \bmod v) + (k - 1)$
- C. $(j \bmod k)$ to $(j \bmod k) + (v - 1)$
- D. $(j \bmod k) * v$ to $(j \bmod k) * v + (v - 1)$

[gate2013-cse](#) [co-and-architecture](#) [cache-memory](#) [normal](#)

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[Answer](#)



An access sequence of cache block addresses is of length N and contains n unique block addresses. The number of unique block addresses between two consecutive accesses to the same block address is bounded above by k . What is the miss ratio if the access sequence is passed through a cache of associativity $A \geq k$ exercising least-recently-used replacement policy?

- A. $\left(\frac{n}{N}\right)$
- B. $\left(\frac{1}{N}\right)$
- C. $\left(\frac{1}{A}\right)$
- D. $\left(\frac{k}{n}\right)$

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[gate2014-cse-set1](#) [co-and-architecture](#) [cache-memory](#) [normal](#)

Answer 

1.2.35 Cache Memory: GATE CSE 2014 Set 2 | Question: 43 [top](#)

► <https://gateoverflow.in/2009>



In designing a computer's cache system, the cache block (or cache line) size is an important parameter. Which one of the following statements is correct in this context?

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- A. A smaller block size implies better spatial locality
- B. A smaller block size implies a smaller cache tag and hence lower cache tag overhead
- C. A smaller block size implies a larger cache tag and hence lower cache hit time
- D. A smaller block size incurs a lower cache miss penalty

gate2014-cse-set2 co-and-architecture cache-memory normal

Answer 

1.2.36 Cache Memory: GATE CSE 2014 Set 2 | Question: 44 [top](#)

► <https://gateoverflow.in/2010>



If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?

- A. Width of tag comparator
- B. Width of set index decoder
- C. Width of way selection multiplexer
- D. Width of processor to main memory data bus

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gate2014-cse-set2 co-and-architecture cache-memory normal

Answer 

1.2.37 Cache Memory: GATE CSE 2014 Set 2 | Question: 9 [top](#)

► <https://gateoverflow.in/1963>



A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is _____.

gate2014-cse-set2 co-and-architecture cache-memory numerical-answers normal

Answer 

1.2.38 Cache Memory: GATE CSE 2014 Set 3 | Question: 44 [top](#)

► <https://gateoverflow.in/2078>



The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is _____.

gate2014-cse-set3 co-and-architecture cache-memory numerical-answers normal

Answer 

1.2.39 Cache Memory: GATE CSE 2015 Set 2 | Question: 24 [top](#)

► <https://gateoverflow.in/8119>



Assume that for a certain processor, a read request takes 50 nanoseconds on a cache miss and 5 nanoseconds on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in a cache hit. The average read access time in nanoseconds is _____.

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gate2015-cse-set2 co-and-architecture cache-memory easy numerical-answers

Answer 

1.2.40 Cache Memory: GATE CSE 2015 Set 3 | Question: 14 [top](#)

► <https://gateoverflow.in/8410>



Consider a machine with a byte addressable main memory of 2^{20} bytes, block size of 16 bytes and a direct mapped cache having 2^{12} cache lines. Let the addresses of two consecutive bytes in main memory be $(E201F)_{16}$ and $(E2020)_{16}$. What are the

tag and cache line addresses (in hex) for main memory address ($E201F$)₁₆?

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- A. E, 201
- B. F, 201
- C. E, E20
- D. 2, 01F

gate2015-cse-set3 co-and-architecture cache-memory normal

Answer 

1.2.41 Cache Memory: GATE CSE 2016 Set 2 | Question: 32 [top](#)

<https://gateoverflow.in/39622>



The width of the physical address on a machine is 40 bits. The width of the tag field in a 512 KB 8-way set associative cache is _____ bits.

gate2016-cse-set2 co-and-architecture cache-memory normal numerical-answers

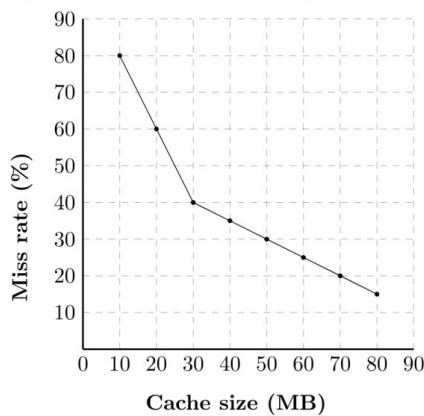
Answer 

1.2.42 Cache Memory: GATE CSE 2016 Set 2 | Question: 50 [top](#)

<https://gateoverflow.in/39592>



A file system uses an in-memory cache to cache disk blocks. The miss rate of the cache is shown in the figure. The latency to read a block from the cache is 1 ms and to read a block from the disk is 10 ms. Assume that the cost of checking whether a block exists in the cache is negligible. Available cache sizes are in multiples of 10 MB.



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The smallest cache size required to ensure an average read latency of less than 6 ms is _____ MB.

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gate2016-cse-set2 co-and-architecture cache-memory normal numerical-answers

Answer 

1.2.43 Cache Memory: GATE CSE 2017 Set 1 | Question: 25 [top](#)

<https://gateoverflow.in/118305>



Consider a two-level cache hierarchy with $L1$ and $L2$ caches. An application incurs 1.4 memory accesses per instruction on average. For this application, the miss rate of $L1$ cache is 0.1; the $L2$ cache experiences, on average, 7 misses per 1000 instructions. The miss rate of $L2$ expressed correct to two decimal places is _____.

gate2017-cse-set1 co-and-architecture cache-memory numerical-answers

Answer 

1.2.44 Cache Memory: GATE CSE 2017 Set 1 | Question: 54 [top](#)

<https://gateoverflow.in/118748>



A cache memory unit with capacity of N words and block size of B words is to be designed. If it is designed as a direct mapped cache, the length of the TAG field is 10 bits. If the cache unit is now designed as a $16 - way$ set-associative cache, the length of the TAG field is _____ bits.

gate2017-cse-set1 co-and-architecture cache-memory normal numerical-answers

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Answer 

1.2.45 Cache Memory: GATE CSE 2017 Set 2 | Question: 29 [top](#) <https://gateoverflow.in/118371>



In a two-level cache system, the access times of L_1 and L_2 caches are 1 and 8 clock cycles, respectively. The miss penalty from the L_2 cache to main memory is 18 clock cycles. The miss rate of L_1 cache is twice that of L_2 . The average memory access time (AMAT) of this cache system is 2 cycles. The miss rates of L_1 and L_2 respectively are

- A. 0.111 and 0.056
- B. 0.056 and 0.111
- C. 0.0892 and 0.1784
- D. 0.1784 and 0.0892

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gate2017-cse-set2 cache-memory co-and-architecture normal

Answer 

1.2.46 Cache Memory: GATE CSE 2017 Set 2 | Question: 45 [top](#) <https://gateoverflow.in/118597>



The read access times and the hit ratios for different caches in a memory hierarchy are as given below:

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Cache	Read access time (in nanoseconds)	Hit ratio
I -cache	2	0.8
D -cache	2	0.9
L_2 -cache	8	0.9

The read access time of main memory is 90 nanoseconds. Assume that the caches use the referred-word-first read policy and the write-back policy. Assume that all the caches are direct mapped caches. Assume that the dirty bit is always 0 for all the blocks in the caches. In execution of a program, 60% of memory reads are for instruction fetch and 40% are for memory operand fetch. The average read access time in nanoseconds (up to 2 decimal places) is _____

gate2017-cse-set2 co-and-architecture cache-memory numerical-answers

Answer 

1.2.47 Cache Memory: GATE CSE 2017 Set 2 | Question: 53 [top](#) <https://gateoverflow.in/118613>



Consider a machine with a byte addressable main memory of 2^{32} bytes divided into blocks of size 32 bytes. Assume that a direct mapped cache having 512 cache lines is used with this machine. The size of the tag field in bits is _____

gate2017-cse-set2 co-and-architecture cache-memory numerical-answers

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Answer 

1.2.48 Cache Memory: GATE CSE 2018 | Question: 34 [top](#) <https://gateoverflow.in/204108>



The size of the physical address space of a processor is 2^P bytes. The word length is 2^W bytes. The capacity of cache memory is 2^N bytes. The size of each cache block is 2^M words. For a K-way set-associative cache memory, the length (in number of bits) of the tag field is

- A. $P - N - \log_2 K$
- B. $P - N + \log_2 K$
- C. $P - N - M - W - \log_2 K$
- D. $P - N - M - W + \log_2 K$

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gate2018-cse co-and-architecture cache-memory normal

Answer 

1.2.49 Cache Memory: GATE CSE 2019 | Question: 1 [top](#) <https://gateoverflow.in/302847>



A certain processor uses a fully associative cache of size 16 kB, The cache block size is 16 bytes. Assume that the main

memory is byte addressable and uses a 32-bit address. How many bits are required for the *Tag* and the *Index* fields respectively in the addresses generated by the processor?

- A. 24 bits and 0 bits
- B. 28 bits and 4 bits
- C. 24 bits and 4 bits
- D. 28 bits and 0 bits

gate2019-cse co-and-architecture cache-memory normal

Answer 

1.2.50 Cache Memory: GATE CSE 2019 | Question: 45 top ↴

<https://gateoverflow.in/302803>



A certain processor deploys a single-level cache. The cache block size is 8 words and the word size is 4 bytes. The memory system uses a 60-MHz clock. To service a cache miss, the memory controller first takes 1 cycle to accept the starting address of the block, it then takes 3 cycles to fetch all the eight words of the block, and finally transmits the words of the requested block at the rate of 1 word per cycle. The maximum bandwidth for the memory system when the program running on the processor issues a series of read operations is _____ $\times 10^6$ bytes/sec

gate2019-cse numerical-answers co-and-architecture cache-memory

Answer 

1.2.51 Cache Memory: GATE CSE 2020 | Question: 21 top ↴

<https://gateoverflow.in/333201>



A direct mapped cache memory of 1 MB has a block size of 256 bytes. The cache has an access time of 3 ns and a hit rate of 94%. During a cache miss, it takes 20 ns to bring the first word of a block from the main memory, while each subsequent word takes 5 ns. The word size is 64 bits. The average memory access time in ns (round off to 1 decimal place) is _____.

gate2020-cse numerical-answers co-and-architecture cache-memory

Answer 

1.2.52 Cache Memory: GATE CSE 2020 | Question: 30 top ↴

<https://gateoverflow.in/333201>



A computer system with a word length of 32 bits has a 16 MB byte-addressable main memory and a 64 KB, 4-way set associative cache memory with a block size of 256 bytes. Consider the following four physical addresses represented in hexadecimal notation.

- $A_1 = 0x42C8A4$,
- $A_2 = 0x546888$,
- $A_3 = 0x6A289C$,
- $A_4 = 0x5E4880$

Which one of the following is TRUE?

- A. A_1 and A_4 are mapped to different cache sets.
- B. A_2 and A_3 are mapped to the same cache set.
- C. A_3 and A_4 are mapped to the same cache set.
- D. A_1 and A_3 are mapped to the same cache set.

gate2020-cse cache-memory

Answer 

1.2.53 Cache Memory: GATE CSE 2021 Set 1 | Question: 22 top ↴

<https://gateoverflow.in/357429>



Consider a computer system with a byte-addressable primary memory of size 2^{32} bytes. Assume the computer system has a direct-mapped cache of size 32 KB (1 KB = 2^{10} bytes), and each cache block is of size 64 bytes.

The size of the tag field is _____ bits.

gate2021-cse-set1 co-and-architecture cache-memory numerical-answers

Answer 



Consider a set-associative cache of size 2KB ($1\text{KB} = 2^{10}$ bytes) with cache block size of 64 bytes. Assume that the cache is byte-addressable and a 32-bit address is used for accessing the cache. If the width of the tag field is 22 bits, the associativity of the cache is _____

[gate2021-cse-set2](#) [numerical-answers](#) [co-and-architecture](#) [cache-memory](#)

Answer



Assume a two-level inclusive cache hierarchy, L_1 and L_2 , where L_2 is the larger of the two. Consider the following statements.

- S_1 : Read misses in a write through L_1 cache do not result in writebacks of dirty lines to the L_2
- S_2 : Write allocate policy *must* be used in conjunction with write through caches and no-write allocate policy is used with writeback caches.

Which of the following statements is correct?

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- A. S_1 is true and S_2 is false
 B. S_1 is false and S_2 is true
 C. S_1 is true and S_2 is true
 D. S_1 is false and S_2 is false

[gate2021-cse-set2](#) [co-and-architecture](#) [cache-memory](#)

Answer



Consider a system with 2 level cache. Access times of Level 1 cache, Level 2 cache and main memory are 1 ns , 10 ns , and 500 ns respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9, respectively. What is the average access time of the system ignoring the search time within the cache?

- A. 13.0
 B. 12.8
 C. 12.6
 D. 12.4

[gate2004-it](#) [co-and-architecture](#) [cache-memory](#) [normal](#) [isro2016](#)

Answer



Consider a fully associative cache with 8 cache blocks (numbered 0 – 7) and the following sequence of memory block requests:

4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7

If LRU replacement policy is used, which cache block will have memory block 7?

- A. 4
 B. 5
 C. 6
 D. 7

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[gate2004-it](#) [co-and-architecture](#) [cache-memory](#) [normal](#)

Answer



Consider a 2-way set associative cache memory with 4 sets and total 8 cache blocks (0 – 7) and a main memory with 128 blocks (0 – 127). What memory blocks will be present in the cache after the following sequence of memory block references if LRU policy is used for cache block replacement. Assuming that initially the cache did not have any memory block from the current

job?
0 5 3 9 7 0 16 55

- A. 0 3 5 7 16 55
- B. 0 3 5 7 9 16 55
- C. 0 5 7 9 16 55
- D. 3 5 7 9 16 55

gate2005-it tests.gatecse.in co-and-architecture cache-memory normal
Answer ↗

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1.2.59 Cache Memory: GATE IT 2006 | Question: 42 top ↗

https://gateoverflow.in/3585



A cache line is 64 bytes. The main memory has latency 32 ns and bandwidth 1 GBytes/s . The time required to fetch the entire cache line from the main memory is:

- A. 32 ns
- B. 64 ns
- C. 96 ns
- D. 128 ns

gate2006-it tests.gatecse.in co-and-architecture cache-memory normal
Answer ↗

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1.2.60 Cache Memory: GATE IT 2006 | Question: 43 top ↗

https://gateoverflow.in/3586



A computer system has a level-1 instruction cache (I -cache), a level-1 data cache (D -cache) and a level-2 cache ($L2$ -cache) with the following specifications:

	Capacity	Mapping Method	Block Size
I -Cache	4K words	Direct mapping	4 words
D -Cache	4K words	2-way set associative mapping	4 words
$L2$ -Cache	64K words	4-way set associative mapping	16 words

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The length of the physical address of a word in the main memory is 30 bits. The capacity of the tag memory in the I -cache, D -cache and $L2$ -cache is, respectively,

- A. $1 \text{ K} \times 18\text{-bit}, 1 \text{ K} \times 19\text{-bit}, 4 \text{ K} \times 16\text{-bit}$
- B. $1 \text{ K} \times 16\text{-bit}, 1 \text{ K} \times 19\text{-bit}, 4 \text{ K} \times 18\text{-bit}$
- C. $1 \text{ K} \times 16\text{-bit}, 512 \times 18\text{-bit}, 1 \text{ K} \times 16\text{-bit}$
- D. $1 \text{ K} \times 18\text{-bit}, 512 \times 18\text{-bit}, 1 \text{ K} \times 18\text{-bit}$

gate2006-it tests.gatecse.in co-and-architecture cache-memory normal
Answer ↗

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1.2.61 Cache Memory: GATE IT 2007 | Question: 37 top ↗

https://gateoverflow.in/3470



Consider a Direct Mapped Cache with 8 cache blocks (numbered 0 – 7). If the memory block requests are in the following order

3, 5, 2, 8, 0, 63, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24.

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Which of the following memory blocks will not be in the cache at the end of the sequence ?

- A. 3
- B. 18
- C. 20
- D. 30

gate2007-it tests.gatecse.in co-and-architecture cache-memory normal
Answer ↗

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Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB.

The number of bits in the TAG, SET and WORD fields, respectively are:

- A. 7, 6, 7
- B. 8, 5, 7
- C. 8, 6, 6
- D. 9, 4, 7

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[gate2008-it](#) [co-and-architecture](#) [cache-memory](#) [normal](#)

Answer



Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB.

While accessing the memory location $0C795H$ by the CPU, the contents of the TAG field of the corresponding cache line is:

- A. 000011000
- B. 110001111
- C. 000110000
- D. 110010101

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[gate2008-it](#) [co-and-architecture](#) [cache-memory](#) [normal](#)

Answer

Answers: Cache Memory



A CPU cache is a hardware cache used by the central processing unit (CPU) of a computer to reduce the average cost (time or energy) to access data from the main memory.

A cache is a smaller, faster memory, located closer to a processor core, which stores copies of the data from frequently used main memory locations. Most CPUs have different independent caches, including instruction and data caches, where the data cache is usually organized as a hierarchy of more cache levels.

Source :- https://en.wikipedia.org/wiki/CPU_cache

References [classroom.gateoverflow.in](#)

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8 votes

-- Satbir Singh (21k points)



$$\text{Total number of block access} = (512/4 + 100 \times 1028/4 + 512/4) = 25956$$

All the blocks above and below the loop region can be assumed to be cache misses.

It is given that the cache is fully associative but the replacement policy is not mentioned. Let's assume it is FIFO. Also, for simplicity let's assume that there's no reuse within a cache block.

In the first loop access every cache access will be a miss. Since the loop body size is 1028 and we assumed FIFO, the last cache block will replace the first one. In the second iteration, first cache block access will be a miss and this will replace the second cache block. Going like this every cache block access will be a miss.

(i) So, hit ratio = 0.

(ii) By just reducing the loop body size by 4 bytes, all the loop accesses from second iteration of the loop will be a hit. So, we can get a hit ratio of $\frac{99 \times 1024}{101 \times 1024} = 98.01\%$

0 votes

-- gatecse (63.3k points)

1.2.3 Cache Memory: GATE CSE 1990 | Question: 7a top

<https://gateoverflow.in/85403>



✓ For main memory, there are 2^{14} blocks and each block size is 2^8 bytes (A byte is an eight-bit word)

1. Size of main memory = $2^{14} \times 2^8 = 4MB$ (22 – bits required for addressing the main memory).
2. For WORD field, we require 8 – bits , as each block contains 2^8 words.

As there are 4 blocks in 1 set, 32 sets will be needed for 128 blocks. Thus SET field requires 5 – bits .

Then, TAG field requires $22 - (5 + 8) = 9$ – bits

9-bits (for tag)	5- bits (for set)	8-bits (for word)
------------------	-------------------	-------------------

46 votes

-- kirti singh (2.6k points)

1.2.4 Cache Memory: GATE CSE 1992 | Question: 5-a top

<https://gateoverflow.in/584>



✓ Average memory access time = Time spend for read + Time spend for write

= Read time when cache hit + Read time when cache miss + Write time when cache hit + Write time when cache miss

$$= 0.8 \times 0.9 \times 50 + 0.8 \times 0.1 \times (500 + 50)$$

(assuming hierarchical read from memory and cache as only simultaneous write is mentioned in question)
 $+ 0.2 \times 0.9 \times 500 + 0.2 \times 0.1 \times 500$ (simultaneous write mentioned in question)

$$= 36 + 44 + 90 + 10 = 180 \text{ ns.}$$

Reference: <http://www.howardhuang.us/teaching/cs232/24-Cache-writes-and-examples.pdf>

References



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61 votes

-- Arjun Suresh (332k points)

1.2.5 Cache Memory: GATE CSE 1993 | Question: 11 top

<https://gateoverflow.in/2308>



✓ We are given the probability of access being a hit in each level (clear since their sum adds to 1).
So, we can get the average access time as:

$$\begin{aligned} t_A &= 0.99 \times 10^{-6} + 0.00998 \times (10^{-6} + 10^{-5} + 0.001) \\ &+ 0.00002 \times (10^{-6} + 10^{-5} + 10^{-4} + 0.1 + 0.001)] \\ &\approx (0.99 + 10 + 2) \times [10^{-6}] = 13\mu s . \end{aligned}$$

We can also use the following formula- for 100% of accesses M_1 is accessed,
whenever M_1 is a miss, M_2 is accessed and when both misses only M_3 is accessed.
So, average memory access time,

$$t_A = 10^{-6} + (1 - 0.99) \times (10^{-5} + 0.001) + 0.00002 \times (10^{-4} + 0.1) = 1 + 10.01 + 2\mu s = 13.01\mu s.$$

37 votes

-- Arjun Suresh (332k points)

Quick Cache Maths:-

Suppose that in 250 memory references there are 30 misses in L1 and 10 misses in L2.

$$\text{Miss rate of L1} = \frac{30}{250}$$

Miss rate of L2 = $\frac{10}{30}$ (In L1 we miss 30 requests, so at L2 we have 30 requests, but it misses 10 out of 30)

See this [question](#).

Here, Probabilities are given, We need to convert it into Hit ratios.

$p_1 = 0.99000$, it says we hit 0.99 times in M_1 but we miss 0.01 times. Here hit rate is same as probability $H_1 = 0.99$

$p_2 = 0.00998$, it says we hit 0.00998 times out of 0.01 requests (0.01 misses from M_1), $H_2 = \frac{0.00998}{0.01} = 0.998$
(H_3 is of course 1. we hit 0.00002 times in M_3 out of 0.00002 misses from M_2)

$H_1 = 0.99$, $H_2 = 0.998$, $H_3 = 1$. t_i is Access time, and T_i is page transfer time.

$t_A = t_1 + (1 - H_1) \times \text{Miss penalty 1}$

Miss penalty 1 = $(t_2 + T_1) + (1 - H_2) \times \text{Miss penalty 2}$

Miss penalty 2 = $(t_3 + T_2)$

Ref: question 3 here

<https://www.cs.utexas.edu/~fussell/courses/cs352.fall98/Homework/old/Solution3.ps>

References



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69 votes

-- Sachin Mittal (15.8k points)

1.2.6 Cache Memory: GATE CSE 1995 | Question: 1.6 top ↗

↗ <https://gateoverflow.in/2593>



✓ Answer is (D).

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Locality of reference is actually the frequent accessing of any storage location or some value. We can say in simple language that whatever things are used more frequently, they are stored in the locality of reference. So we have cache memory for the purpose.

30 votes

-- Gate Keeda (15.9k points)

1.2.7 Cache Memory: GATE CSE 1995 | Question: 2.25 top ↗

↗ <https://gateoverflow.in/2638>



✓

$$\text{Number of sets} = \frac{4K}{(64 \times 4)} = 16$$

So, we need 4-bits to identify a set \Rightarrow SET = 4 bits.

64 words per block mean WORD is 6-bits.

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So, the answer is an option (D).

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29 votes

-- Arjun Suresh (332k points)

1.2.8 Cache Memory: GATE CSE 1996 | Question: 26 top ↗

↗ <https://gateoverflow.in/2778>



✓ The equation for access time can be written as follows (assuming a, b are the hit ratios of level 1 and level 2 respectively).

$$T = T_1 + (1 - a)T_2 + (1 - a) \times (1 - b)T_3$$

Here $T \leq 100$, $T_1 = 50\text{ns}$, $T_2 = 200\text{ns}$ and $T_3 = 5000\text{ns}$. On substituting the a, b for the first case we get

$T = 95\text{ns}$ for $a = 0.8$ and $b = 0.995$. i.e., $L1 = 8M$ and $L2 = 64M$.

$T = 75\text{ns}$ for $a = 0.9$ and $b = 0.99$. i.e., $L1 = 16M$ and $L2 = 4M$

B.

1. $L_1 = 8M, a = 0.8, L_2 = 4M, b = 0.98$. So,
 $T = 50 + 0.2 \times 200 + 0.2 \times 0.02 \times 5000 = 50 + 40 + 20 = 110\text{ns}$
2. $L_1 = 16M, a = 0.9, L_2 = 16M, b = 0.99$. So,
 $T = 50 + 0.1 \times 200 + 0.1 \times 0.01 \times 5000 = 50 + 20 + 5 = 75\text{ns}$
3. $L_1 = 64M, a = 0.95, L_2 = 64M, b = 0.995$. So,
 $T = 50 + 0.05 \times 200 + 0.05 \times 0.005 \times 5000 = 50 + 10 + 1.25 = 61.25\text{ns}$

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23 votes

-- kireeti (1k points)

1.2.9 Cache Memory: GATE CSE 1998 | Question: 18 top

<https://gateoverflow.in/1732>



Size of the loop = $n \times b = k \times m \times b$

Size of a set = $k \times b$ ($k - \text{way}$ associative)

Here, size of the loop is smaller than size of cache as $m \leq l$. So we are guaranteed that the entire loop is in cache without any replacement. (Here we assumed that the memory size of $n \times b$ used by the loop is contiguous, or else we could have a scenario where the entire loop size gets mapped to the same set causing cache replacement).

For the first iteration:

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No. of accesses = $n \times b$

No. of misses = n as each new block access is a miss and loop body has n blocks each of size b for a total size of $n \times b$.

For, the remaining 99 iterations:

No. of accesses = $n \times b$

No. of misses = 0

So, total no. of accesses = $100nb$

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Total no. of hits = Total no. of accesses – Total no. of misses

$$= 100nb - n$$

$$\text{So, hit ratio} = \frac{100nb - n}{100nb} = 1 - \frac{1}{100b}$$

The hit ratio is independent of l , so for $l = 1$ also we have hit ratio = $1 - \frac{1}{100b}$

33 votes

-- Arjun Suresh (332k points)

1.2.10 Cache Memory: GATE CSE 1999 | Question: 1.22 top

<https://gateoverflow.in/1475>



- ✓ Number of cache blocks = $2c$

Number of sets in cache = $\frac{2c}{2} = c$ since each set has 2 blocks. Now, a block of main memory gets mapped to a set (associativity of 2 just means there are space for 2 memory blocks in a cache set), and we have $2cm$ blocks being mapped to c sets. So, in each set $2m$ different main memory blocks can come and block k of main memory will be mapped to $k \bmod c$.

Correct Answer: B.

39 votes

-- Arjun Suresh (332k points)

1.2.11 Cache Memory: GATE CSE 2001 | Question: 1.7, ISRO2008-18 top

<https://gateoverflow.in/700>



- ✓ Exploit the spatial locality of reference in a program as, if the next locality is addressed immediately, it will already be in the cache.

Consider the scenario similar to cooking, where when an ingredient is taken from cupboard, you also take the near by ingredients along with it- hoping that they will be needed in near future.

Correct Answer: B

84 votes

-- Arjun Suresh (332k points)



✓ **What is the number of sets in the cache**

$$\text{Number of sets} = \frac{\text{Cache memory}}{(\text{set associativity} \times \text{cache block size})}$$

$$= \frac{256KB}{(4 \times 16B)}$$

$$= 4096$$

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What is the size (in bits) of the tag field per cache block?

Memory address size = 32-bit

Number of bits required to identify a particular set = 12 (Number of sets = 4096)

Number of bits required to identify a particular location in cache line = 4 (cache block size = 16)

$$\text{Size of tag field} = 32 - 12 - 4 = 16\text{-bit}$$

What is the number and size of comparators required for tag matching?

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We use 4-way set associate cache. So, we need 4 comparators each of size 16-bits

<http://ccce.colorado.edu/~ecen2120/Manual/caches/cache.html>

How many address bits are required to find the byte offset within a cache block?

Cache block size is 16-byte. so 4-bits are required to find the byte offset within a cache block.

What is the total amount of extra memory (in bytes) required for the tag bits?

size of tag = 16-bits

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Number of sets = 4096

Set associativity = 4

Extra memory required to store the tag bits = $16 \times 4096 \times 4\text{-bits} = 2^{18}$ bits = 2^{15} bytes.

References



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42 votes

-- suraj (4.8k points)



A. Data cache size = 8 KB.

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Block line size = 16 B.

Since each array element occupies 4 B, four consecutive array elements occupy a block line (elements are aligned as starting address is 0)

$$\text{Number of cache blocks} = \frac{8KB}{16B} = 512.$$

$$\text{Number of cache blocks needed for the array} = \frac{2048}{4} = 512.$$

So, all the array elements has its own cache block and there is no collision.

We can also explain this with respect to array address.

Starting address is 0x00000000 = 0_b0000...0(32 0's).

Ending address is 0x00001FFF = 0_b0000...0111111111111111 (4 × 2048 = 8192 locations), 0 – 8191 .

Here, the last 4 bits are used as OFFSET bits and the next 9 bits are used as SET bits. So, since the ending address is not extending beyond these 9 bits, all cache accesses are to diff sets.

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- B. If the last element is accessed first, its cache block is fetched. (which should contain the previous 3 elements of the array also since each cache block hold 4 elements of array and 2048 is and exact multiple of 4). Thus, for every 4 accesses, we will have a cache miss \Rightarrow for 2048 accesses we will have 512 cache misses. (This would be same even if we access array in forward order).

46 votes

-- Arjun Suresh (332k points)

1.2.14 Cache Memory: GATE CSE 2004 | Question: 65

<https://gateoverflow.in/1059>



- ✓ We have 4 blocks and 2 blocks in a set

\Rightarrow there are 2 sets. So blocks will go to sets as follows:

Set Number	Block Number
0	0,8,12
1	1,9,10,11

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Since the lowest bit of block address is used for indexing into the set, so 8, 12 and 0 first miss in cache with 0 replacing 8 (there are two slots in each set due to 2 – way set) and then 12 hits in cache and 8 again misses. So, totally 4 misses.

Correct Answer: *C*

25 votes

-- Arjun Suresh (332k points)

1.2.15 Cache Memory: GATE CSE 2005 | Question: 67

<https://gateoverflow.in/1390>



- ✓ Number of blocks = $\frac{\text{cache size}}{\text{block size}} = \frac{32\text{-KB}}{32} = 1024\text{-Bytes.}$

So, indexing requires 10-bits. Number of OFFSET bits required to access 32-bit block = 5.

So, **number of TAG bits** = $32 - 10 - 5 = 17$.

So, answer is (A).

36 votes

-- Arjun Suresh (332k points)

1.2.16 Cache Memory: GATE CSE 2006 | Question: 74

<https://gateoverflow.in/1851>



- ✓ Cache size is 32 KB and cache block size is 32 B. So,

$$\begin{aligned} \text{Number of sets} &= \frac{\text{cache size}}{\text{no. of blocks in a set} \times \text{block size}} \\ &= \frac{32 \text{ KB}}{2 \times 32 \text{ B}} = 512 \end{aligned}$$

So, number of index bits needed = 9 (since $2^9 = 512$). Number of offset bits = 5 (since $2^5 = 32$ B is the block size and assuming byte addressing). So, number of tag bits = $32 - 9 - 5 = 18$ (as memory address is of 32 bits).

So, time for comparing the data

$$= \text{Time to compare the data} + \text{Time to select the block in set} = 0.6 + 18/10 \text{ ns} = 2.4 \text{ ns.}$$

(Two comparisons of tag bits need to be done for each block in a set, but they can be carried out in parallel and the succeeding one multiplexed as the output).

Reference: <https://courses.cs.washington.edu/courses/cse378/09au/lectures/cse378au09-19.pdf>

Correct Answer: *A*

References



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69 votes

-- Arjun Suresh (332k points)

1.2.17 Cache Memory: GATE CSE 2006 | Question: 75 [top](#)

<https://gateoverflow.in/43565>



✓
$$\text{number of sets} = \frac{\text{cache size}}{\text{no. of blocks in a set} \times \text{block size}}$$

$$= \frac{32KB}{1 \times 32B} = 1024$$

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So, number of index bits = 10, and

number of tag bits = $32 - 10 - 5 = 17$.

So, $h2 = \frac{17}{10} = 1.7 \text{ ns}$

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Correct Answer: D

20 votes

-- Arjun Suresh (332k points)

1.2.18 Cache Memory: GATE CSE 2006 | Question: 80 [top](#)

<https://gateoverflow.in/1854>



- ✓ Code being C implies array layout is row-major.
http://en.wikipedia.org/wiki/Row-major_order

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When $A[0][0]$ is fetched, 128 consecutive bytes are moved to cache. So, for the next $\frac{128}{8} - 1 = 15$ memory references there won't be a cache miss.

For the next iteration of i loop also the same thing happens as there is no temporal locality in the code. So, number of cache misses for $P1$ is

$$= \frac{512}{16} \times 512$$

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$$= 32 \times 512$$

$$= 2^{14} = 16384$$

Correct Answer: C

References



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51 votes

-- Arjun Suresh (332k points)

1.2.19 Cache Memory: GATE CSE 2006 | Question: 81 [top](#)

<https://gateoverflow.in/43517>



✓ Number of Cache Lines = $\frac{2^{15}B}{128B} = 256$

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$$\text{In 1 Cache Line} = \frac{128B}{8B} = 16 \text{ elements}$$

$$P_1 = \frac{\text{total elements in array}}{\text{elements in a cache line}}$$

$$= \frac{512 \times 512}{16} = 2^{14} = 16384.$$

$$P_2 = 512 \times 512 = 2^{18}$$

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$$\frac{P_1}{P_2} = \frac{16384}{512 \times 512}$$

$$= 2^{14-18} = 2^{-4} = \frac{1}{16}$$

It is so, because for P_1 for every line there is a miss, and once a miss is processed we get 16 elements in memory. So, another miss happens after 16 elements.

For P_2 for every element there is a miss because storage is row major order(by default) and we are accessing column wise.

Hence, answer is option B.

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41 votes

-- Amar Vashishth (25.2k points)

Code being C implies array layout is row-major.

http://en.wikipedia.org/wiki/Row-major_order

When $A[0][0]$ is fetched, 128 consecutive bytes are moved to cache. So, for the next $128/8 - 1 = 15$ memory references there won't be a cache miss. For the next iteration of i loop also the same thing happens as there is no temporal locality in the code. So, number of cache misses for P_1

$$= \frac{512}{16} \times 512$$

$$= 32 \times 512$$

$$= 2^{14} = 16384$$

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In the case of P_2 , the memory references are not consecutive. After $A[0][0]$, the next access is $A[1][0]$ which is after $512 * 8$ memory locations. Since our cache block can hold only 128 contiguous memory locations, $A[1][0]$ won't be in cache after $a[0][0]$ is accessed. Now, the next location after $A[0][0]$ is $A[0][1]$ which will be accessed only after 512 iterations of the inner loop-after 512 distinct memory block accesses. In our cache we have only space for $32\text{ KB}/128\text{ B} = 256$ memory blocks. So, by the time $A[0][1]$ is accessed, its cache block would be replaced. So, each of the memory access in P_2 results in a cache miss. Total number of cache miss

$$= 512 \times 512$$

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$$\text{So, } \frac{M_1}{M_2} = \frac{32 \times 512}{512 \times 512} = \frac{1}{16}$$

References



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63 votes

-- Arjun Suresh (332k points)

1.2.20 Cache Memory: GATE CSE 2007 | Question: 10

<https://gateoverflow.in/1208>



✓ Number of sets = $\frac{\text{cache size}}{(\text{size of a block} * \text{No. of blocks in a set})}$

$$= \frac{128 * 64}{(64 * 4)} \quad (4 \text{ way set associative means 4 blocks in a set})$$

$$= 32.$$

So, number of index (LINE) bits = 5 and number of WORD bits = 6 since cache block (line) size is 64.

So, number of TAG bits = $20 - 6 - 5 = 9$.

Answer is (D) choice

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27 votes

-- Arjun Suresh (332k points)



- ✓ Bits used to represent the address = $\log_2 2^{16} = 16$

Each cache line size = 64 bytes; means offset requires 6-bits

Total number of lines in cache = 32; means line # requires 5-bits

So, tag bits = $16 - 6 - 5 = 5$

We have a 2D-array each of its element is of size = 1 Byte;

Total size of this array = $50 \times 50 \times 1$ Byte = 2500 Bytes

So, total number of lines it will require to get contain in cache

$$= \frac{2500B}{64B} = 39.0625 \approx 40$$

Starting address of array = $1100H = 00010\ 00100\ 000000$

The group of bits in middle represents Cache Line number \Rightarrow array starts from cache line number 4,

We require 40 cache lines to hold all array elements, but we have only 32 cache lines

Lets group/partition our 2500 array elements in those 40 array lines, we call this first array line as A_0 which will have 64 of its elements.

This line(group of 64 elements) of array will be mapped to cache line number 4 as found by analysis of starting address of array above.

This all means that among those 40 array lines some array lines will be mapped to same cache line, coz there are just 32 cache lines but 40 of array lines.

This is how mapping is:

0	A_{28}	
1	A_{29}	
2	A_{30}	
3	A_{31}	
4	$A_0\ A_{32}$	gateoverflow.in
5	$A_1\ A_{33}$	
6	$A_2\ A_{34}$	
7	$A_3\ A_{35}$	
8	$A_4\ A_{36}$	
9	$A_5\ A_{37}$	
10	$A_6\ A_{38}$	
11	$A_7\ A_{39}$	gateoverflow.in
12	A_8	
:		
30	A_{26}	
31	A_{27}	

So, if we access complete array twice we get = $32 + 8 + 8 + 8 = 56$ miss because only 8 lines from cache line number 4 to 11 are miss operation, rest are **Hits(not counted)** or **Compulsory misses(first 32)**.

Hence, answer is option (C).

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250 votes

-- Amar Vashishth (25.2k points)

$2^{16} = 64$ KB main memory is mapped to 32 lines of 64 bytes. So, number of offset bits = 6 (to identify a byte in a line) and number of indexing bits = 5 (to identify the line).

Size of array = $50 * 50 = 2500$ B. If array is stored in row-major order (first row, second-row..), and if elements are also accessed in row-major order (or stored and accessed in column-major order), for the first 64 accesses, there will be only 1 cache miss, and for 2500 accesses, there will be $2500/64 = 40$ cache misses during the first iteration.

We have 5 index bits and 6 offset bits. So, for 2^{11} ($5 + 6 = 11$) continuous memory addresses there wont be any cache conflicts as the least significant bits are offset bits followed by index bits.

So, number of array elements that can be accessed without cache conflict = 2048 (as element size is a byte). The next 452 elements conflict with the first 452 elements. This means $452/64 = 8$ cache blocks are replaced. (We used ceil, as even if one element from a new block is accessed, the whole block must be fetched).

So, during second iteration we incur misses for the first 8 cache blocks as well as for the last 8 cache blocks. So, total data cache misses across 2 iterations = $40 + 8 + 8 = 56$.

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39 votes

-- Arjun Suresh (332k points)

1.2.22 Cache Memory: GATE CSE 2007 | Question: 81 top

<https://gateoverflow.in/43511>



✓ Cache Organization:

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Starting Address = $1100H = 16^3 + 16^2 + 0 + 0 = 4352B$ is the starting address.

We need to find Starting block = $\frac{4352B}{64B} = 68^{th}$ block in main memory from where array start storing elements.

$50 \times 50B = \text{array size} = 50 \times \frac{50B}{64B} = 39.0625$ blocks needed ≈ 40 blocks

68,69,70....107 block we need = 40 blocks

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Starting block is $68 \pmod{32} = 4^{th}$ cache block and after that in sequence they will be accessed.
As shown in below table, line number 4 to 11 has been replaced by array in second time

Cache Block Number	First Cycle	Second cycle
0	96	
1	97	
2	98	
3	99	
4	68 // 100	68
5	69 // 101	69
6	70 // 102	70
7	71 // 103	71
8	72 // 104	72
9	73 // 105	73
10	74 // 106	74
11	75 // 107	75
12	76	
13	77	
14	78	
15	79	
16	80	
17	81	
18	82	
19	83	
20	84	
21	85	
22	86	
23	87	
24	88	
25	89	
26	90	
27	91	
28	92	
29	93	
30	94	
31	95	

Correct Answer: A

52 votes

-- papesh (18k points)

1.2.23 Cache Memory: GATE CSE 2008 | Question: 35 top



- ✓ 1st is not correct as data need not to be exactly same at the same point of time and so write back policy can be used in this.

2nd is not needed when talking only about L1 and L2.

For 3rd, associativity can be equal.

So, only 4th statement is Necessarily true - (A) choice.

49 votes

-- Shaun Patel (6.1k points)

1.2.24 Cache Memory: GATE CSE 2008 | Question: 71 top



$$\checkmark \text{ Number of sets} = \frac{\text{cache size}}{\text{size of a set}}$$

$$= \frac{64 \text{ KB}}{(16 \text{ B} \times 2)} \text{ (two blocks per set)}$$

$$= 2 \text{ K} = 2^{11}$$

So, we need 11-bits for set indexing.

Number of WORD bits required = 4 as a cache block consists of 16 bytes and we need 4-bits to address each of them.

So, number of tag bits = $32 - 11 - 4 = 17$

Total size of the tag = $17 \times \text{Number of cache blocks}$

$$= 17 \times 2^{11} \times 2 \text{ (since each set has 2 blocks)}$$

$$= 68 \text{ Kbits}$$

Answer is option D) 68 Kbits

We use the top 17-bits for tag and the next 11-bits for indexing and next 4 for offset. So, for two addresses to have the same cache index, their 11 address bits after the 4 offset bits from right must be same.

$ARR[0][0]$ is located at virtual address 0x FF000 000. (FF000 is page address and 000 is page offset).

So, index bits are 000000000000

$$\text{Address of } ARR[0][4] = 0xFF000 + 4 \times \text{sizeof (double)}$$

$$= 0xFF000 000 + 4 \times 8 = 0xFF000 020 \text{ (32 = 20 in hex) (index bits differ)}$$

$$\text{Address of } ARR[4][0] = 0xFF000 + 4 \times 1024 \times \text{sizeof (double)}$$

[since we use row major storage]

$$= 0xFF000 000 + 4096 \times 8 = 0xFF000 000 + 0x8000 = 0xFF008 000$$

(index bits matches that of $ARR[0][0]$ as both read 000 0000 0000)

$$\text{Address of } ARR[0][5] = 0xFF000 + 5 \times \text{sizeof (double)} = 0xFF000 000 + 5 \times 8 = 0xFF000 028 \text{ (40 = 28 in hex)}$$

(index bits differ)

$$\text{Address of } ARR[5][0] = 0xFF000 + 5 \times 1024 \times \text{sizeof (double)} \text{ [since we use row major storage]}$$

$$= 0xFF000 000 + 5120 \times 8 = 0xFF000 000 + 0xA000 = 0xFF00A 000 \text{ (index bits differ)}$$

So, only $ARR[4][0]$ and $ARR[0][0]$ have the same cache index.

The inner loop is iterating from 0 to 1023, so consecutive memory locations are accessed in sequence. Since cache block size is only 16 bytes and our element being double is of size 8 bytes, during a memory access only the next element gets filled in the cache. i.e.; every alternative memory access is a cache miss giving a hit ratio of 50 (If loops i and j are reversed, all accesses will be misses and hit ratio will become 0).

64 votes

-- Arjun Suresh (332k points)

1.2.25 Cache Memory: GATE CSE 2008 | Question: 72 [top](#)

<https://gateoverflow.in/43490>



- ✓ Number of sets = cache size/ size of a set
= $64\text{ KB}/(16\text{ B} \times 2)$ (two blocks per set)
= $2^K = 2^{11}$
So, we need 11 bits for set indexing.

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Number of WORD bits required = 4 as a cache block consists of 16 bytes and we need 4 bits to address each of them.

So, number of tag bits = $32 - 11 - 4 = 17$

$$\begin{aligned}\text{Total size of the tag} &= 17 \times \text{Number of cache blocks} \\ &= 17 \times 2^{11} \times 2 \quad (\text{since each set has 2 blocks})\end{aligned}$$

$$= 68\text{ KB}$$

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We use the top 17 bits for tag and the next 11 bits for indexing and next 4 for offset. So, for two addresses to have the same cache index, their 11 address bits after the 4 offset bits from right must be same.

$ARR[0][0]$ is located at virtual address $0x FF000 000$. ($FF000$ is page address and 000 is page offset). So, index bits are 00000000000

Address of $ARR[0][4] = 0xFF000 + 4 \times \text{sizeof(double)} = 0xFF000000 + 4 \times 8 = 0xFF000 020$ (32 = 20 in hex)
(index bits differ)

Address of $ARR[4][0] = 0xFF000 + 4 \times 1024 \times \text{sizeof(double)}$ [since we use row major storage]
= $0xFF000 000 + 4096 \times 8 = 0xFF000 000 + 0x8000 = 0xFF008 000$ (index bits matches that of $ARR[0][0]$ as both read 000 0000 0000)

Address of $ARR[0][5] = 0xFF000 + 5 \times \text{sizeof(double)} = 0xFF000 000 + 5 \times 8 = 0xFF000 028$ (40 = 28 in hex)
(index bits differ)

Address of $ARR[5][0] = 0xFF000 + 5 \times 1024 \times \text{sizeof(double)}$ [since we use row major storage]
= $0xFF000 000 + 5120 \times 8 = 0xFF000 000 + 0xA000 = 0xFF00A 000$ (index bits differ)

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So, only $ARR[4][0]$ and $ARR[0][0]$ have the same cache index.

The inner loop is iterating from 0 to 1023, so consecutive memory locations are accessed in sequence. Since cache block size is only 16 bytes and our element being double is of size 8 bytes, during a memory access only the next element gets filled in the cache. i.e.; every alternative memory access is a cache miss giving a hit ratio of 50%. (If loops i and j are reversed, all accesses will be misses and hit ratio will become 0).

Correct Answer: B

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53 votes

-- Arjun Suresh (332k points)

1.2.26 Cache Memory: GATE CSE 2008 | Question: 73 [top](#)

<https://gateoverflow.in/43491>



- ✓ Block size = $16B$ and one element = $8B$.
So, in one block 2 elements will be stored.

For 1024×1024 element num of block required = $\frac{1024 \times 1024}{2} = 2^{19}$ blocks required.

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In one block the first element will be a miss and second one is hit(since we are transferring two unit at a time)

$$\Rightarrow \text{hit ratio} = \frac{\text{Total hit}}{\text{Total reference}}$$

$$\begin{aligned}&= \frac{2^{19}}{2^{20}} \\ &= \frac{1}{2} = 0.5\end{aligned}$$

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$$= 0.5 \times 100 = 50\%$$

Correct Answer: C

26 votes

-- asutosh kumar Biswal (8k points)

1.2.27 Cache Memory: GATE CSE 2009 | Question: 29 top

<https://gateoverflow.in/1315>



- ✓ 16 blocks and sets with 4 blocks each means there are 4 sets. So, the lower 2 bits are used for getting a set and 4-way associative means in a set only the last 4 cache accesses can be stored.

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155

mod 4 gives,

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0, 3, 1, 0, 3, 0, 1, 3, 0, 0, 1, 0, 3

Now for each of 0..3, the last 4 accesses will be in cache.

So, {92, 32, 48, 8}, {155, 63, 159, 3}, {73, 129, 133, 1} and {} will be in cache.

So, the missing element from choice is 216.

Correct Answer: D

60 votes

-- Arjun Suresh (332k points)

1.2.28 Cache Memory: GATE CSE 2010 | Question: 48 top

<https://gateoverflow.in/2352>



- ✓ Ideally the answer should be 20 ns as it is the time to transfer a block from L2 to L1 and this time only is asked in question. But there is confusion regarding access time of L2 as this means the time to read data from L2 till CPU but here we need the time till L1 only. So, I assume the following is what is meant by the question.

A block is transferred from L2 to L1. And L1 block size being 4 words (since L1 is requesting we need to consider L1 block size and not L2 block size) and data width being 4 bytes, it requires one L2 access (for read) and one L1 access (for store). So, time = $20 + 2 = 22$ ns.

Correct Answer: C

106 votes

-- Arjun Suresh (332k points)

1.2.29 Cache Memory: GATE CSE 2010 | Question: 49 top

<https://gateoverflow.in/43329>



- ✓ The transfer time should be $4 * 200 + 20 = 820$ ns. But this is not in option. So, I assume the following is what is meant by the question.

L2 block size being 16 words and data width between memory and L2 being 4 words, we require 4 memory accesses(for read) and 4 L2 accesses (for store). Now, we need to send the requested block to L1 which would require one more L2 access (for read) and one L1 access (for store). So, total time

$$= 4 * (200 + 20) + (20 + 2)$$

$$= 880 + 22$$

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$$= 902 \text{ ns}$$

Correct Answer: C

119 votes

-- Arjun Suresh (332k points)

1.2.30 Cache Memory: GATE CSE 2011 | Question: 43 top

<https://gateoverflow.in/2145>



- ✓ Number of cache blocks = $\frac{\text{cache size}}{\text{size of a block}}$
 $= \frac{8 \text{ KB}}{32 \text{ B}}$

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= 256

So, we need 8-bits for indexing the 256 blocks of the cache. And since a block is 32 bytes we need 5 WORD bits to address each byte. So, out of the remaining 19-bits (32 - 8 - 5) should be tag bits.

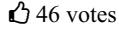
So, a tag entry size = 19 + 1(valid bit) + 1(modified bit) = 21 bits.

Total size of metadata = $21 \times$ Number of cache blocks

$$= 21 \times 256$$

$$= 5376 \text{ bits}$$

Correct Answer: D



46 votes

-- Arjun Suresh (332k points)

1.2.31 Cache Memory: GATE CSE 2012 | Question: 54 top

<https://gateoverflow.in/2192>



- ✓ Total cache size = 256 KB

Cache block size = 32 Bytes

$$\text{So, number of cache entries} = \frac{256 \text{ K}}{32} = 8 \text{ K}$$

Number of sets in cache = $\frac{8 \text{ K}}{4} = 2 \text{ K}$ as cache is 4-way associative.

So, $\log(2048) = 11$ bits are needed for accessing a set. Inside a set we need to identify the cache entry.

$$\text{No. of memory block possible} = \frac{\text{Memory size}}{\text{Cache block size}}$$

$$= \frac{2^{32}}{32} = 2^{27}.$$

So, no. of memory block that can go to a single cache set

$$= \frac{2^{27}}{2^{11}}$$

$$= 2^{16}.$$

So, we need 16 tag bits along with each cache entry to identify which of the possible 2^{16} blocks is being mapped there.

Correct Answer: C



41 votes

-- Arjun Suresh (332k points)

1.2.32 Cache Memory: GATE CSE 2012 | Question: 55 top

<https://gateoverflow.in/43311>



- ✓ Total cache size = 256 KB

Cache block size = 32 Bytes

$$\text{So, number of cache entries} = \frac{256 \text{ K}}{32} = 8 \text{ K}$$

Number of sets in cache = $\frac{8 \text{ K}}{4} = 2 \text{ K}$ as cache is 4-way associative.

So, $\log(2048) = 11$ bits are needed for accessing a set. Inside a set we need to identify the cache entry.

$$\text{Total number of distinct cache entries} = \frac{2^{32}}{\text{cache entry size}} = \frac{2^{32}}{32} = 2^{27}$$

Out of this 2^{27} , each set will be getting only $\frac{2^{27}}{2^{11}} = 2^{16}$ possible distinct cache entries as we use the first 11 bits to identify a set. So, we need 16 bits to identify a cache entry in a set, which is the number of bits in the tag field.

Size of cache tag directory = Size of tag entry \times Number of tag entries

$$= 16 + (2 + 1 + 1) \text{ bits (2 valid, 1 modified, 1 replacement as given in question)} \times 8 \text{ K}$$

= 208 = 160 Kbits

Not needed for this question, still:

Valid bit: Tells if the memory referenced by the cache entry is valid. Initially, when a process is loaded all entries are invalid. Only when a page is loaded, its entry becomes valid.

Modified bit: When processor writes to a cache location its modified bit is made 1. This information is used when a cache entry is replaced- entry 0 means no update to main memory needed. Entry 1 means an update is needed.

Replacement bit: This is needed for the cache replacement policy. Explained in the below link:

<https://www.seas.upenn.edu/~cit595/cit595s10/handouts/LRUreplacementpolicy.pdf>

Correct Answer: A

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References



37 votes

-- Arjun Suresh (332k points)

1.2.33 Cache Memory: GATE CSE 2013 | Question: 20 [top](#)

<https://gateoverflow.in/1442>



- ✓ Number of sets in cache = v .

The question gives a sequencing for the cache lines. For set 0, the cache lines are numbered $0, 1, \dots, k - 1$. Now for set 1, the cache lines are numbered $k, k + 1, \dots, k + k - 1$ and so on.

So, main memory block j will be mapped to set $(j \bmod v)$, which will be any one of the cache lines from $(j \bmod v) * k$ to $(j \bmod v) * k + (k - 1)$.

(Associativity plays no role in mapping- k -way associativity means there are k spaces for a block and hence reduces the chances of replacement.)

Correct Answer: A

80 votes

-- Arjun Suresh (332k points)

1.2.34 Cache Memory: GATE CSE 2014 Set 1 | Question: 44 [top](#)

<https://gateoverflow.in/1922>



- ✓ There are N accesses to cache.
Out of these n are unique block addresses.
Now, we need to find the number of misses. (min. n misses are guaranteed whatever be the access sequence due to n unique block addresses).

We are given that between two consecutive accesses to the same block, there can be only k unique block addresses. So, for a block to get replaced we can assume that all the next k block addresses goes to the same set (given cache is set-associative) which will be the worst case scenario (they may also go to a different set but then there is lesser chance of a replacement). Now, if associativity size is $\geq k$, and if we use LRU (Least Recently Used) replacement policy, we can guarantee that these k accesses won't throw out our previously accessed cache entry (for that we need at least k accesses). So, this means we are at the best-cache scenario for cache replacement -- out of N accesses we miss only n (which are unique and can not be helped from getting missed and there is no block replacement in cache). So, miss ratio is n/N .

PS: In question it is given "bounded above by k ", which should mean k unique block accesses as k is an integer, but to ensure no replacement this must be ' $k - 1$ '. Guess, a mistake in question.

Correct Answer: A

122 votes

-- Arjun Suresh (332k points)

1.2.35 Cache Memory: GATE CSE 2014 Set 2 | Question: 43 [top](#)

<https://gateoverflow.in/2009>



- ✓ A. A smaller block size means during a memory access only a smaller part of near by addresses are brought to cache-

meaning spatial locality is reduced.

- B. A smaller block size means more number of blocks (assuming cache size constant) and hence index bits go up and offset bits go down. But the tag bits remain the same.

- C. A smaller block size implying larger cache tag is true, but this can't lower cache hit time in any way.
- D. A smaller block size incurs a lower cache miss penalty. This is because during a cache miss, an entire cache block is fetched from next lower level of memory. So, a smaller block size means only a smaller amount of data needs to be fetched and hence reduces the miss penalty (Cache block size can go till the size of data bus to the next level of memory, and beyond this only increasing the cache block size increases the cache miss penalty).

Correct Answer: D

111 votes

-- Arjun Suresh (332k points)

1.2.36 Cache Memory: GATE CSE 2014 Set 2 | Question: 44 top

<https://gateoverflow.in/2010>



- ✓ If associativity is doubled, keeping the capacity and block size constant, then the number of sets gets halved. So, width of set index decoder can surely decrease - (B) is false.
Width of way-selection multiplexer must be increased as we have to double the ways to choose from- (C) is false

As the number of sets gets decreased, the number of possible cache block entries that a set maps to gets increased. So, we need more tag bits to identify the correct entry. So, (A) is also false.

(D) is the correct answer- main memory data bus has nothing to do with cache associativity- this can be answered without even looking at other options.

51 votes

-- Arjun Suresh (332k points)

1.2.37 Cache Memory: GATE CSE 2014 Set 2 | Question: 9 top

<https://gateoverflow.in/1963>



✓ Number of sets = $\frac{\text{cache size}}{\text{size of a set}}$

Size of a set = blocksize \times no. of blocks in a set
= 8 words \times 4 (4-way set-associative)
= $8 \times 4 \times 4$ (since a word is 32 bits = 4 bytes)
= 128 bytes.

$$\text{So, number of sets} = \frac{16 \text{ KB}}{(128 \text{ B})} = 128$$

Now, we can divide the physical address space equally between these 128 sets.

So, the number of bytes each set can access

$$= \frac{4 \text{ GB}}{128}$$

$$= 32 \text{ MB}$$

$$= \frac{32}{4} = 8 \text{ M words} = 1 \text{ M blocks. } (2^{20} \text{ blocks})$$

So, we need 20 tag bits to identify these 2^{20} blocks.

47 votes

-- Arjun Suresh (332k points)

1.2.38 Cache Memory: GATE CSE 2014 Set 3 | Question: 44 top

<https://gateoverflow.in/2078>



- ✓ The question is to find the time taken for,

$$\frac{100 \text{ fetch operations and } 60 \text{ operand read operations and } 40 \text{ memory operand write operations}}{\text{total number of instructions}}.$$

$$\text{Total number of instructions} = 100 + 60 + 40 = 200$$

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Time taken for 100 fetch operations(fetch = read) = $100 * ((0.9 * 1) + (0.1 * 5))$

1 corresponds to time taken for read when there is cache hit = 140 ns

0.9 is cache hit rate

Time taken for 60 read operations,

$$= 60 * ((0.9 * 1) + (0.1 * 5)) \\ = 84 \text{ ns}$$

Time taken for 40 write operations

$$= 40 * ((0.9 * 2) + (0.1 * 10)) \\ = 112 \text{ ns}$$

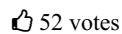
Here, 2 and 10 are the times taken for write when there is cache hit and no cache hit respectively.

So, the total time taken for 200 operations is,

$$= 140 + 84 + 112 \\ = 336 \text{ ns}$$

Average time taken = time taken per operation

$$= \frac{336}{200} \\ = 1.68 \text{ ns}$$

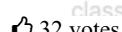


52 votes

-- Divya Bharti (8.8k points)

Fetch is also a memory read operation.

$$\text{Avg access time} = \frac{160(0.9 \times 1 + 0.1 \times 5) + 40(0.9 \times 2 + 0.1 \times 10)}{200} = \frac{160 \times 1.4 + 40 \times 2.8}{200} = \frac{336}{200} = 1.68$$



32 votes

-- aravind90 (389 points)

1.2.39 Cache Memory: GATE CSE 2015 Set 2 | Question: 24 top

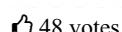
<https://gateoverflow.in/8119>



- ✓ Answer is: $14 \text{ ns} = 0.8(5) + 0.2(50)$

PS: Here instead of cache and main memory access times, time taken on a cache hit and miss are directly given in question. So,

$$\text{Average Access Time} = \text{Hit Rate} \times \text{Hit Time} + \text{Miss Rate} \times \text{Miss Time}$$



48 votes

-- Vikrant Singh (11.2k points)

1.2.40 Cache Memory: GATE CSE 2015 Set 3 | Question: 14 top

<https://gateoverflow.in/8410>

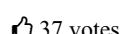


- ✓ Block size of 16 bytes means we need 4 offset bits. (The lowest 4 digits of memory address are offset bits)

Number of sets in cache (cache lines) = 2^{12} so the next lower 12 bits are used for set indexing.

The top 4 bits (out of 20) are tag bits.

So, answer is A.



37 votes

-- Arjun Suresh (332k points)

1.2.41 Cache Memory: GATE CSE 2016 Set 2 | Question: 32 top

<https://gateoverflow.in/39622>



- ✓ Physical Address = 40

- Tag + Set + Block Offset = 40
- $T + S + B = 40 \rightarrow (1)$

We have: Cache Size = number of sets \times blocks per set \times Block size

- $512\ KB = \text{number of sets} \times 8 \times \text{Block size}$
- Number of sets \times Block size = $\frac{512}{8}\ KB = 64\ KB$
- $S + B = 16 \rightarrow (2)$

From (1), (2)

$T = 24$ bits (Ans)

Second way :

$$\text{Cache Size} = 2^{19}$$

$$\text{MM size} = 2^{40}$$

This means, We need to map $\frac{2^{40}}{2^{19}} = 2^{21}$ Blocks to one line. And a set contain 2^3 lines.

Therefore, 2^{24} blocks are mapped to one set.

Using Tag field, I need to identify which one block out of 2^{24} blocks are present in this set. Hence, 24 bits are needed in Tag field.

49 votes

-- Himanshu Agarwal (12.4k points)

In question block size has not been given, so we can assume block size 2^x Byte.

$$\text{Number of Blocks: } \frac{512 \times 2^{10}}{2^x} = 2^{19-x}$$

$$\text{Number of sets: } \frac{2^{19-x}}{8} = 2^{16-x}$$

So number of bits for sets = $16 - x$

Let number of bits for Tag = T

And we have already assumed block size 2^x Byte, therefore number of bits for block size is x

And finally,

$$T + (16 - x) + x = 40$$

$$T + 16 = 40$$

$$T = 24.$$

54 votes

-- ajit (2.5k points)

1.2.42 Cache Memory: GATE CSE 2016 Set 2 | Question: 50

<https://gateoverflow.in/39592>



- ✓ Look aside Cache Latency = 1ms

Main Memory Latency = 10ms

- Lets try with 20 MB

Miss rate = 60%, Hit rate = 40%

$$\text{Avg} = 0.4(1) + 0.6(10)$$

$$= 0.4 + 6 = 6.4\ ms > 6\ ms$$

- Next Take 30 MB

Miss rate = 40%, Hit rate = 60%

$$\text{Avg} = 0.6(1) + 0.4(10)$$

$$= 0.6 + 4 = 4.6 \text{ ms} < 6 \text{ ms}$$

So answer is 30 MB

64 votes

-- Akash Kanase (36k points)

1.2.43 Cache Memory: GATE CSE 2017 Set 1 | Question: 25 top

<https://gateoverflow.in/118305>

- ✓ Answer = 0.05.



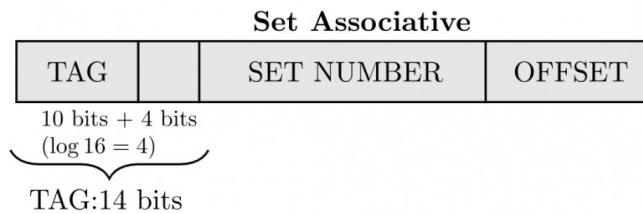
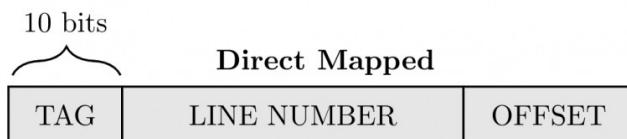
169 votes

-- Debashish Deka (40.8k points)

1.2.44 Cache Memory: GATE CSE 2017 Set 1 | Question: 54 top

<https://gateoverflow.in/118748>

- ✓



In set-associative **1 set = 16 lines**. So the number of index bits will be 4 less than the direct mapped case.
So, Tag bits increased to 14 bits.

65 votes

-- Ahwan Mishra (10.2k points)

1.2.45 Cache Memory: GATE CSE 2017 Set 2 | Question: 29 top

<https://gateoverflow.in/118371>

- ✓ In two-level memory system (hierarchical), it is clear that the second level is accessed only when first level access is a miss. So, we must include the first level access time in all the memory access calculations. Continuing this way for any level, we must include that level access time (without worrying about the hit rate in that level), to all memory accesses coming to that level (i.e., by just considering the miss rate in the previous level). So, for the given question, we can get the following equation:

$$\text{AMAT} = \text{L1 access time}$$

+L1 miss rate × L2 access time
+L1 miss rate × L2 miss rate × Main memory access time

$$2 = 1 + x \times 8 + 0.5x^2 \times 18$$
$$\Rightarrow 9x^2 + 8x - 1 = 0$$

$$\Rightarrow x = \frac{-8 \pm \sqrt{64 + 36}}{18} = \frac{2}{18} = 0.111 .$$

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So, Answer is option (A).

79 votes

-- Arjun Suresh (332k points)

1.2.46 Cache Memory: GATE CSE 2017 Set 2 | Question: 45 top



- ✓ L2 cache is shared between Instruction and Data (is it always?, see below)

So, average read time

= Fraction of Instruction Fetch * Average Instruction fetch time + Fraction of Data Fetch * Average Data Fetch Time

Average Instruction fetch Time = L1 access time + L1 miss rate * L2 access time + L1 miss rate * L2 miss rate * Memory access time

$$= 2 + 0.2 \times 8 + 0.2 \times 0.1 \times 90$$
$$= 5.4 \text{ ns}$$

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Average Data fetch Time = L1 access time + L1 miss rate * L2 access time + L1 miss rate * L2 miss rate * Memory access time

$$= 2 + 0.1 \times 8 + 0.1 \times 0.1 \times 90$$
$$= 3.7 \text{ ns}$$

So, average memory access time

$$= 0.6 \times 5.4 + 0.4 \times 3.7 = 4.72 \text{ ns}$$

Now, why L2 must be shared? Because we can otherwise use it for either Instruction or Data and it is not logical to use it for only 1. Ideally this should have been mentioned in question, but this can be safely assumed also (not enough merit for Marks to All). Some more points in the question:

|| Assume that the caches use the referred-word-first read policy and the writeback policy

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Writeback policy is irrelevant for solving the given question as we do not care for writes. Referred-word-first read policy means there is no extra time required to get the requested word from the fetched cache line.

|| Assume that all the caches are direct mapped caches.

Not really relevant as average access times are given

|| Assume that the dirty bit is always 0 for all the blocks in the caches

Dirty bits are for cache replacement- which is not asked in the given question. But this can mean that there is no more delay when there is a read miss in the cache leading to a possible cache line replacement. (In a write-back cache when a cache line is replaced, if it is dirty then it must be written back to main memory).

96 votes

-- Arjun Suresh (332k points)

1.2.47 Cache Memory: GATE CSE 2017 Set 2 | Question: 53 top



- ✓ No. of blocks of main Memory = $\frac{2^{32}}{2^5} = 2^{27}$

And there are $512 = 2^9$ lines in Cache Memory.

Tag bits tell us to how many blocks does 1 line in Cache memory points to

$$1 \text{ cache line points to } \frac{2^{27}}{2^9} = 2^{18} \text{ lines}$$

So, 18 bits are required as TAG bits.

48 votes

-- Manish Joshi (20.5k points)

1.2.48 Cache Memory: GATE CSE 2018 | Question: 34

<https://gateoverflow.in/204108>



- ✓ Physical Address Space = 2^P Bytes i.e. P bits to represent size of total memory.
Cache Size = 2^N Byte i.e., N bits to represent Cache memory.
Tag size = 2^X Bytes i.e., X bits to represent Tag.
Cache is K -way associative.

$$(\text{Size of Tag}) \times \frac{\text{Cache Size}}{K} = \text{Total Memory Size}$$

$$\begin{aligned} &\Rightarrow 2^X \times \frac{2^N}{K} = 2^P \\ &\Rightarrow 2^{X+N-\log(K)} = 2^P \\ &\Rightarrow 2^X = 2^{P-N+\log(K)} \end{aligned}$$

$$\Rightarrow X(\text{Size of Tag in bits}) = P - N + \log(K)$$

Correct Answer: **B**

34 votes

-- Digvijay (44.9k points)

1.2.49 Cache Memory: GATE CSE 2019 | Question: 1

<https://gateoverflow.in/302847>



- ✓ Given that cache is Fully Associative.

Tag Bits	Block Offset
28	4

There are no index bits in fully associative cache because every main memory block can go to any location in the cache

$$\Rightarrow \text{Index bits} = 0.$$

Given that memory is byte addressable and uses 32-bit address.

Cache Block size is 16 Bytes \Rightarrow Number of bits required for Block Offset = $\lceil \log_2 16 \rceil = 4$ bits

$$\therefore \text{Number of Tag bits} = 32 - 4 = 28.$$

Answer is (D).

50 votes

-- Shaik Masthan (50.4k points)

1.2.50 Cache Memory: GATE CSE 2019 | Question: 45

<https://gateoverflow.in/302803>



- ✓ Time to transfer a cache block = $1 + 3 + 8 = 12$ cycles.

i.e., $4 \text{ bytes} \times 8 = 32 \text{ bytes in 12 cycles.}$

$$\text{So, memory bandwidth} = \frac{32}{12 \text{ cycle time}} = \frac{32}{12/(60 \times 10^6)} = 160 \times 10^6 \text{ bytes/s}$$

44 votes

-- Arjun Suresh (332k points)

Answer : $160 \times 10^6 \frac{\text{Bytes}}{\text{sec}}$

Explanation :

Given frequency = 60 MHz

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This means that the processor completes 60×10^6 cycles in 1 second.

$$\therefore \text{One cycle is completed in } \frac{1}{60 \times 10^6} \text{ seconds}$$

Now,

To service a cache miss, number of cycles needed

$$= 1 \text{ cycle (to accept starting address of the block)} + 3 \text{ cycles (to fetch all the 8 words of the blocks)} + \underbrace{8 \times 1}_{\text{:1 word per cycle}} \text{ cycles (to transmit the data)}$$

Note : Total data is the data which is used for transmitting the words of the requested block at the rate of 1 word per cycle
= 8 words \times 4 Byte (Size of each word)

$$\begin{aligned} \therefore \text{Bandwidth} &= \frac{\text{Total Data}}{12 \text{ cycle time}} \\ &= \frac{8 \times 4 \text{ Bytes}}{12 \text{ cycles} \times 1 \text{ cycle time}} \\ &= \frac{32}{12 \times \frac{1}{60 \times 10^6}} \\ &= \frac{32 \times 60^5 \times 10^6}{12} \\ &= 5 \times 32 \times 10^6 \\ &= 160 \times 10^6 \frac{\text{Bytes}}{\text{sec}} \end{aligned}$$

$\therefore 160 \times 10^6 \frac{\text{Bytes}}{\text{sec}}$ is the correct answer.

16 votes

-- Jeet (15.3k points)



1.2.51 Cache Memory: GATE CSE 2020 | Question: 21

<https://gateoverflow.in/333210>

- Block size is 256 Bytes, word size is 64 bits or 8 bytes. So Block size in words is 8 words.

Number of words per block=32

Time to fetch a word from main-memory to cache is: $20 + 31 \times 5 = 175$ ns because first word takes 20ns and rest each subsequent words take 5ns each.

So average Memory access time is

$$0.94(3) + 0.06(3 + 175) = 13.5 \text{ ns}$$

23 votes

-- Ayush Upadhyaya (28.4k points)



1.2.52 Cache Memory: GATE CSE 2020 | Question: 30

<https://gateoverflow.in/333201>



- Block size is 256 Bytes. Number of sets in cache = 2^6 so Set offset bits=6 and word offset bits=8.

So check for set, check for the rightmost 4 digits of each physical address.(Last two byte denote the word address)

A1=C8A4 = C8 = 11001000

A2=6888 = 68 = 01101000

A3=289C = 28 = 00101000

A4=4880 = 48 = 01001000

Now look for lowest order 6 bits in the highlighted part of Each physical address(corresponds to set number).
8 and 8 match and 6=0110 and 2=0010 two low order bits of 6 and 2 match, So A2 and A3 go to same set.

So answer-B

16 votes

-- Ayush Upadhyaya (28.4k points)

1.2.53 Cache Memory: GATE CSE 2021 Set 1 | Question: 22

<https://gateoverflow.in/357429>



- ✓ Tag bits = $\log_2(\text{Cache Size}) + \log_2(K)$ (where K is associativity)
= $32 - 15 + 0 = 17$ bits

5 votes

-- Nikhil Dhama (2.5k points)

1.2.54 Cache Memory: GATE CSE 2021 Set 2 | Question: 19

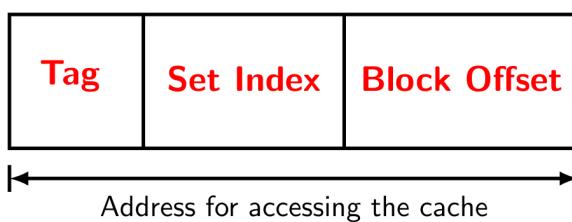
<https://gateoverflow.in/357521>



- ✓ 32 bit address is used for accessing the cache.

It is given that cache is Set-Associative.

The address bits get split as follows:



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Block Size = $64B \Rightarrow$ Block offset = 6 bits.

Given that Tag field width = 22 bits.

Therefore, width of Set Index field = $32 - 22 - 6 = 4 \Rightarrow 2^4 = 16$ sets in the cache.

Cache size is $2KB$ and Block size = $64B \Rightarrow 2^5 = 32$ blocks present in the cache.

16 sets contain 32 blocks \Rightarrow 2 blocks per set or associativity = 2.

Correct Answer: 2

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5 votes

-- Shaik Masthan (50.4k points)

1.2.55 Cache Memory: GATE CSE 2021 Set 2 | Question: 27

<https://gateoverflow.in/357513>



- ✓ S_1 : Read Miss in a write through $L1$ cache results in read allocate. No write back is done here, as in a write through $L1$ cache, both $L1$ and $L2$ caches are updated during a write operation (no dirty blocks and hence no dirty bits as in a write back cache). So during a Read miss it will simply bring in the missed block from $L2$ to $L1$ which may replace one block in $L1$ (this replaced block in $L1$ is already updated in $L2$ and so needs no write back). So, S_1 is TRUE.

S_2 : This statement is FALSE. Both write-through and write-back policies can use either of these write-miss policies, but usually they are paired in this way.

- No write allocation during write through as $L1$ and $L2$ are accessed for each write operation (subsequent writes to same location gives no advantage even if the location is in $L1$ cache).
- In write back we can do write allocate in $L1$ after a write operation hoping for subsequent writes to the same location which will then hit in $L1$ and thus avoiding a more expensive $L2$ access.

Correct Answer: A.

Cache Writing Policies

References



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1 votes

-- Arjun Suresh (332k points)

1.2.56 Cache Memory: GATE IT 2004 | Question: 12, ISRO2016-77 [top](#)

<https://gateoverflow.in/3653>



- ✓ By default we consider hierarchical access - because that is the common implementation and simultaneous access cache has great practical difficulty. But here the question is a bit ambiguous -- it says to ignore search time within the cache - usually search is applicable for an associative cache but here no such information given. So, maybe they are telling to ignore the search time for $L1$ and just consider the time for $L2$ for an $L1$ miss and similarly just consider memory access time for $L2$ miss. This is nothing but simultaneous access.

Access time for hierarchical access,

$$\begin{aligned} &= t_1 + (1 - h_1) \times t_2 + (1 - h_1)(1 - h_2)t_m \\ &= 1 + 0.2 \times 10 + 0.2 \times 0.1 \times 500 \\ &= 13ns. \end{aligned}$$

Access time for simultaneous access,

$$\begin{aligned} &= h_1 \times t_1 + (1 - h_1)h_2 \times t_2 + (1 - h_1)(1 - h_2)t_m \\ &= 0.8 + 0.2 \times 0.9 \times 10 + 0.2 \times 0.1 \times 500 \\ &= 12.6ns. \end{aligned}$$

Both options in choice.

1 votes

-- Arjun Suresh (332k points)

1.2.57 Cache Memory: GATE IT 2004 | Question: 48 [top](#)

<https://gateoverflow.in/3691>



- ✓ When 45 comes, the cache contents are:
4 3 25 8 19 6 16 35

LRU array (first element being least recently used)

[4 3 19 6 25 8 16 35].

So, 45 replaces 4.

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45 3 25 8 19 6 16 35 [3 19 6 25 8 16 35 45]

Similarly, 22 replaces 3 to give:

45 22 25 8 19 6 16 35 [19 6 25 8 16 35 45 22]

8 hits in cache.

45 22 25 8 19 6 16 35 [19 6 25 16 35 45 22 8]

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3 replaces 19

45 22 25 8 3 6 16 35 [6 25 16 35 45 22 8 3]

16 and 25 hits in cache.

45 22 25 8 3 6 16 35 [6 35 45 22 8 3 16 25]

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Finally, 7 replaces 6, which is in block 5.

So, answer is (B).

1 votes

-- Arjun Suresh (332k points)

1.2.58 Cache Memory: GATE IT 2005 | Question: 61 [top](#)

<https://gateoverflow.in/3822>



- ✓ 128 main memory blocks are mapped to 4 sets in cache. So, each set maps 32 blocks each. And in each set there is place for two blocks (2-way set).

Now, we have 4 sets meaning 2 index bits. Also, 32 blocks going to one set means 5 tag bits.

Now, these 7 bits identify a memory block and tag bits are placed before index bits. (otherwise adjacent memory references-spatial locality- will hamper cache performance)

So, based on the two index bits (lower 2 bits) blocks will be going to sets as follows:

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Set Number	Block Numbers
0	0, 16
1	5, 9
2	
3	8, 7, 55

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Since, each set has only 2 places, 3 will be thrown out as it is the least recently used block. So, final content of cache will be

0 5 7 9 16 55 classroom.gateoverflow.in

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(C) choice.

46 votes

-- Arjun Suresh (332k points)

1.2.59 Cache Memory: GATE IT 2006 | Question: 42 top

https://gateoverflow.in/3585



✓ Answer is C.

For 1 sec it is 10^9 bytes (Note - by looking at the options, it can be decided that 1GB should be considered as 10^9 , but not as 2^{30} , and in general, if bandwidth is given, then we consider 1 Giga = 10^9)

So, for 64 bytes?

It is $\frac{64 \times 1}{10^9}$ so it is 64 ns but mm latency is 32.

So, total time required to place cache line is $64 + 32 = 96$ ns.

57 votes

-- K Rajashekhar (997 points)

1.2.60 Cache Memory: GATE IT 2006 | Question: 43 top

https://gateoverflow.in/3586



✓ 1. I-cache

- Number of blocks in cache = $\frac{4K}{4} = 2^{10}$ blocks.
- Bits to represent blocks = 10
- Number of words in a block = 4 = 2^2 words.
- Bits to represent words = 2.
- tag bits = $30 - (10 + 2) = 18$.
- Each block will have its own tag bits. So total tag bits = $1K \times 18$ bits.

2. D-cache

- Number of blocks in cache = $\frac{4K}{4} = 2^{10}$ blocks.
- Number of sets in cache = $\frac{2^{10}}{2} = 2^9$ sets.
- Bits to represent sets = 9.
- Number of words in a block = 4 = 2^2 words.
- Bits to represent words = 2
- tag bits = $30 - (9 + 2) = 19$
- Each block will have its own tag bits. So total tag bits = $1K \times 19$ bits.

3. L2 cache

- Number of blocks in cache = $\frac{64K}{16} = 2^{12}$ blocks.
- Number of sets in cache = $\frac{2^{12}}{4} = 1024$ sets.
- Bits to represent sets = 10

- Number of words in cache = $16 = 2^4$ words.
- Bits to represent words = 4.
- tag bits = $30 - (10 + 4) = 16$
- Each block will have its own tag bits. So total tag bits = $2^{12} \times 16\text{-bits} = 4K \times 16\text{-bits}$.

Option (A).

Up 38 votes

-- Viral Kapoor (1.9k points)

[1.2.61 Cache Memory: GATE IT 2007 | Question: 37](#) top

→ <https://gateoverflow.in/3470>



- ✓ Answer is (B).

Cache location (memory block) = block req mod number of cache blocks. Since each block has only one location (associativity is 1) the last mod 8 request will be in cache (no need of any replacement policy as mapping is direct).

3, 5, 2, 8, 0, 63, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24

Block 0 – 8, 0, 16, 24, 24. At end contains 24.

1- 9, 17, 25, 17.

2- 2, 18, 2, 82.

3- 3.

4- 20.

5- 5, 5.

6- 30.

7- 6363.

So, memory block 18 is not in cache while 3, 20 and 30 are in cache.

Up 23 votes

-- K Rajashekhar (997 points)

[1.2.62 Cache Memory: GATE IT 2008 | Question: 80](#) top

→ <https://gateoverflow.in/3403>



- ✓ Number of cache blocks = $\frac{8KB}{(128 \times 1)} = 64$

$$\text{Number of sets in cache} = \frac{\text{Number of cache blocks}}{4 \text{ (4-way set)}} = \frac{64}{4} = 16$$

So, number of SET bits required = 4(as $2^4 = 16$, and with 4 bits we can get 16 possible outputs)

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We can now straight away choose (D) as answer but for confirmation can proceed further.

Since, only physical memory information is given we can assume cache is physically tagged (which is anyway the common case even in case of virtual memory).

So, we can divide the physical memory into 16 regions so that, each set maps into only its assigned region.

So, size of a region a set can address = $\frac{1MB}{16} = 2^{16}$ Bytes = $\frac{2^{16}}{128} = 2^9$ cache blocks (as cache block size is 128 words = 128 bytes).

So, when an access comes to a cache entry, it must be able to determine which out of the 2^9 possible physical block it is. In short, it needs 9 bits for TAG.

Now, cache block size is 128 words and so to identify a word we need 7 bits for WORD.

Up 26 votes

-- Arjun Suresh (332k points)

[1.2.63 Cache Memory: GATE IT 2008 | Question: 81](#) top

→ https://gateoverflow.in/3403/gate2008-it_80



- ✓ As shown in https://gateoverflow.in/3403/gate2008-it_80

We have 16 sets in cache and correspondingly 16 regions in physical memory to which each set is mapped. Now, WORD bit size is 7 as we need 7 bits to address 128 possible words in a cache block.

So, the lowest 7 bits of 0C795H will be used for this giving us the remaining bits as 0000 1100 0111 1

Of these bits, the lower 4 are used for addressing the 16 possible sets, giving us the tag bits: 0000 1100 0 in (A) choice.

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References



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-- Arjun Suresh (332k points)

1.3

Cisc Risc Architecture (2) top

1.3.1 Cisc Risc Architecture: GATE CSE 1999 | Question: 2.22 top

<https://gateoverflow.in/1499>



The main difference(s) between a CISC and a RISC processor is/are that a RISC processor typically

- A. has fewer instructions
- B. has fewer addressing modes
- C. has more registers
- D. is easier to implement using hard-wired logic

gate1999 co-and-architecture normal cisc-risc-architecture multiple-selects

Answer

1.3.2 Cisc Risc Architecture: GATE CSE 2018 | Question: 5 top

<https://gateoverflow.in/204079>



Consider the following processor design characteristics:

- I. Register-to-register arithmetic operations only
- II. Fixed-length instruction format
- III. Hardwired control unit

Which of the characteristics above are used in the design of a RISC processor?

- A. I and II only
- B. II and III only
- C. I and III only
- D. I, II and III

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Answer

Answers: Cisc Risc Architecture

1.3.1 Cisc Risc Architecture: GATE CSE 1999 | Question: 2.22 top

<https://gateoverflow.in/1499>



- ✓ All are properties of the RISC processor.

- <http://cs.stanford.edu/people/eroberts/courses/soco/projects/risc/whatis/index.html>
- <http://cs.stanford.edu/people/eroberts/courses/soco/projects/risc/riscfc/index.html>
- http://homepage3.nifty.com/alpha-1/computer/Control_E.html

References



Like 26 votes

-- Digvijay (44.9k points)



- ✓ (D) All of these

Hardwired control units are implemented through use of combinational logic units, featuring a finite number of gates that can generate specific results based on the instructions that were used to invoke those responses. Their design uses a **fixed architecture**—it requires changes in the wiring if the instruction set is modified or changed. This architecture is **preferred in reduced instruction set computers (RISC)** as they use a simpler instruction set.

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Instructions length cannot vary in RISC usually it's 32 bit. For CISC it can be between 16 to 64 bits.

The hardwired control unit is used when instructions are fixed.

Register to register operations is always possible in RISC. CISC can have memory to memory instructions also.

References: <https://www-cs-faculty.stanford.edu/~eroberts/courses/soco/projects/2000-01/risc/riscfcisc/>

https://en.wikipedia.org/wiki/Control_unit#Hardwired_control_unit

References



26 votes

-- Subham Mishra (11.4k points)

1.4

Clock Frequency (2) [top](#)

Many microprocessors have a specified lower limit on clock frequency (apart from the maximum clock frequency limit) because _____

[gate1992](#) [normal](#) [co-and-architecture](#) [clock-frequency](#) [fill-in-the-blanks](#)

Answer



The floating point unit of a processor using a design D takes $2t$ cycles compared to t cycles taken by the fixed point unit. There are two more design suggestions D_1 and D_2 . D_1 uses 30% more cycles for fixed point unit but 30% less cycles for floating point unit as compared to design D . D_2 uses 40% less cycles for fixed point unit but 10% more cycles for floating point unit as compared to design D . For a given program which has 80% fixed point operations and 20% floating point operations, which of the following ordering reflects the relative performances of three designs?
($D_i > D_j$ denotes that D_i is faster than D_j)

- A. $D_1 > D > D_2$
- B. $D_2 > D > D_1$
- C. $D > D_2 > D_1$
- D. $D > D_1 > D_2$

[gate2007-it](#) [co-and-architecture](#) [normal](#) [clock-frequency](#)

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Answer

Answers: Clock Frequency



- ✓ Clock frequency becomes low means time period of clock becomes high. When this time period increases beyond the time period in which the volatile memory contents must be refreshed, we lose those contents. So, clock frequency can't go

below this value.

Reference: <https://gateoverflow.in/261/microprocessors-specified-frequency-frequency->

References



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26 votes

-- Rajarshi Sarkar (27.9k points)

1.4.2 Clock Frequency: GATE IT 2007 | Question: 36 [top](#)

<https://gateoverflow.in/3469>



- ✓ (B) is correct.

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$$T = 0.8 \times \text{time taken in fixed point} + 0.2 \times \text{time taken in floating point}$$

$$D = 0.8 \times t + 0.2 \times 2t = 1.2t$$

$$D_1 = 0.8 \times 1.3t + 0.2 \times 0.7 \times 2t = 1.04t + .28t = 1.32t$$

$$D_2 = 0.8 \times 0.6t + 0.2 \times 1.1 \times 2t = 0.48t + .44t = 0.92t$$

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So, D_2 is the best design for this given program followed by D and then D_1 . Option B.

45 votes

-- Vicky Bajoria (4.1k points)

1.5

Conflict Misses (1) [top](#)

1.5.1 Conflict Misses: GATE CSE 2017 Set 1 | Question: 51 [top](#)

<https://gateoverflow.in/118745>



Consider a 2-way set associative cache with 256 blocks and uses *LRU* replacement. Initially the cache is empty. Conflict misses are those misses which occur due to the contention of multiple blocks for the same cache set. Compulsory misses occur due to first time access to the block. The following sequence of access to memory blocks :

$$\{0, 128, 256, 128, 0, 128, 256, 128, 1, 129, 257, 129, 1, 129, 257, 129\}$$

is repeated 10 times. The number of *conflict misses* experienced by the cache is _____.

gate2017-cse-set1

co-and-architecture

cache-memory

conflict-misses

normal

numerical-answers

tests.gatecse.in

Answer

Answers: Conflict Misses

1.5.1 Conflict Misses: GATE CSE 2017 Set 1 | Question: 51 [top](#)

<https://gateoverflow.in/118745>



- ✓ {0, 128, 256, 128, 0, 128, 256, 128, 1, 129, 257, 129, 1, 129, 257, 129}

1st Iteration:

For {0, 128, 256, 128, 0, 128, 256, 128}

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Block ID	Type	Set 0 content
0	Compulsory Miss	0
128	Compulsory Miss	0 128
256	Compulsory Miss	128 256
128	Hit	256 128
0	Conflict miss	128 0
128	Hit	0 128
256	Conflict miss	128 256
128	Hit	256 128

Total number of conflict misses = 2;

Similarly for $\{1, 129, 257, 129, 1, 129, 257, 129\}$, total number of conflict misses in set1 = 2

Total number of conflict misses in 1st iteration = $2 + 2 = 4$

2nd iteration:

for $\{0, 128, 256, 128, 0, 128, 256, 128\}$

Block ID	Type	Set 0 content
0	Conflict Miss	128 0
128	Hit	0 128
256	Conflict miss	128 256
128	Hit	256 128
0	Conflict miss	128 0
128	Hit	0 128
256	Conflict miss	128 256
128	Hit	256 128

Total number of conflict misses = 4.

Similarly for $\{1, 129, 257, 129, 1, 129, 257, 129\}$, total number of conflict misses in set1 = 4

Total Number of conflict misses in 2nd iteration = $4 + 4 = 8$

Note that content of each set is same, before and after 2nd iteration. Therefore each of the remaining iterations will also have 8 conflict misses.

Therefore, overall conflict misses = $4 + 8 * 9 = 76$

104 votes

-- suraj (4.8k points)

1.6

Control Unit (1) [top](#)

1.6.1 Control Unit: GATE CSE 1987 | Question: 1-vi [top](#)

<https://gateoverflow.in/80199>



A microprogrammed control unit

- A. Is faster than a hard-wired control unit.
- B. Facilitates easy implementation of new instruction.
- C. Is useful when very small programs are to be run.
- D. Usually refers to the control unit of a microprocessor.

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[gate1987](#) [co-and-architecture](#) [control-unit](#) [microporgramming](#)

[goclasses.in](#)

[tests.gatecse.in](#)

Answer

1.6.1 Control Unit: GATE CSE 1987 | Question: 1-vi [top](#)<https://gateoverflow.in/80199>

- ✓ A. is wrong. Microprogrammed Control Unit (CU) can never be faster than hardwired CU. Microprogrammed CU it has an extra layer on top of hardwired CU and hence can only be slower than hardwired CU.
 B. is a suitable answer as we can add new instruction by changing the content of control memory.
 C. is not correct as when only small programs are there, hardwired control makes more sense.
 D. control unit can also be hardwired, so this is also not correct.

Reference: [Slides](#)Correct Answer: *B*

References



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27 votes

-- Arjun Suresh (332k points)

1.7

Data Dependences (2) [top](#)1.7.1 Data Dependences: GATE CSE 2015 Set 3 | Question: 47 [top](#)<https://gateoverflow.in/8556>

Consider the following code sequence having five instructions from I_1 to I_5 . Each of these instructions has the following format.

$OP\ R_i, R_j, R_k$

Where operation OP is performed on contents of registers R_j and R_k and the result is stored in register R_i .

I_1 : ADD R_1, R_2, R_3

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I_2 : MUL R_7, R_1, R_3

I_3 : SUB R_4, R_1, R_5

I_4 : ADD R_3, R_2, R_4

I_5 : MUL R_7, R_8, R_9

Consider the following three statements.

S1: There is an anti-dependence between instructions I_2 and I_5

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S2: There is an anti-dependence between instructions I_2 and I_4

S3: Within an instruction pipeline an anti-dependence always creates one or more stalls

Which one of the above statements is/are correct?

- A. Only S1 is true
- B. Only S2 is true
- C. Only S1 and S3 are true
- D. Only S2 and S3 are true

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[gate2015-cse-set3](#) [co-and-architecture](#) [pipelining](#) [data-dependences](#) [normal](#)

Answer

1.7.2 Data Dependences: GATE IT 2007 | Question: 39 [top](#)<https://gateoverflow.in/3472>

Data forwarding techniques can be used to speed up the operation in presence of data dependencies. Consider the following replacements of LHS with RHS.

- i. $R1 \rightarrow Loc, Loc \rightarrow R2 \equiv R1 \rightarrow R2, R1 \rightarrow Loc$
- ii. $R1 \rightarrow Loc, Loc \rightarrow R2 \equiv R1 \rightarrow R2$
- iii. $R1 \rightarrow Loc, R2 \rightarrow Loc \equiv R1 \rightarrow Loc$
- iv. $R1 \rightarrow Loc, R2 \rightarrow Loc \equiv R2 \rightarrow Loc$

In which of the following options, will the result of executing the RHS be the same as executing the LHS irrespective of the instructions that follow ?

- A. i and iii
B. i and iv
C. ii and iii
D. ii and iv

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gate2007-it data-dependences co-and-architecture

Answer ↗

Answers: Data Dependences

1.7.1 Data Dependences: GATE CSE 2015 Set 3 | Question: 47 top ↗

↗ <https://gateoverflow.in/8556>



- ✓ Answer should be (B).

Anti-dependence can be overcome in pipeline using register renaming. So, "always" in S3 makes it false. Also, if I2 is completed before I4 (execution stage of MUL), then also there won't be any stall.

Upvote 55 votes

-- ppm (543 points)

1.7.2 Data Dependences: GATE IT 2007 | Question: 39 top ↗

↗ <https://gateoverflow.in/3472>



- i. is true. Both *LOC* and *R2* are getting the value of *R1* in *LHS* and *RHS*.
ii. is false, because *R2* gets the correct data in both *LHS* and *RHS*, but *LOC* is not updated in *RHS*.
iii. is wrong because *R2* is writing last, not *R1* in *LHS*, but not in *RHS*.
iv. is true. The first write to *LOC* in *LHS* is useless as it is overwritten by the next write.

So, answer is (B).

Upvote 38 votes

-- Vicky Bajoria (4.1k points)

1.8

Data Path (6) top ↗

1.8.1 Data Path: GATE CSE 1990 | Question: 8a top ↗

↗ <https://gateoverflow.in/85669>



A single bus CPU consists of four general purpose register, namely, R_0, \dots, R_3 , ALU, MAR, MDR, PC, SP and IR (Instruction Register). Assuming suitable microinstructions, write a microroutine for the instruction, ADD R_0, R_1 .

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gate1990 descriptive co-and-architecture data-path

Answer ↗

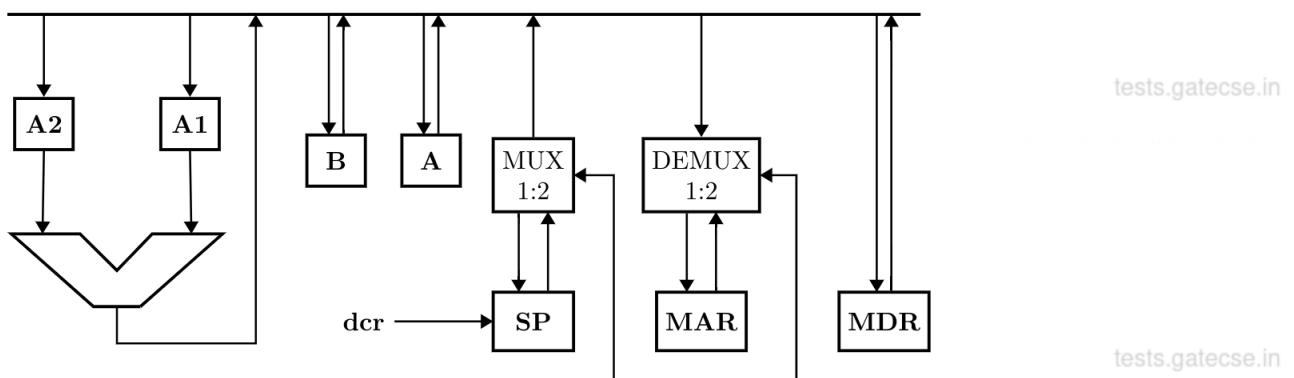
1.8.2 Data Path: GATE CSE 2001 | Question: 2.13 top ↗

↗ <https://gateoverflow.in/731>



Consider the following data path of a simple non-pipelined CPU. The registers A, B, A_1, A_2, MDR , the bus and the ALU are 8-bit wide. SP and MAR are 16-bit registers. The MUX is of size $8 \times (2 : 1)$ and the DEMUX is of size $8 \times (1 : 2)$. Each memory operation takes 2 CPU clock cycles and uses MAR (Memory Address Register) and MDR (Memory Date Register). SP can be decremented locally.

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The CPU instruction "push r" where, $r = A$ or B has the specification

- $M[SP] \leftarrow r$
- $SP \leftarrow SP - 1$

How many CPU clock cycles are required to execute the "push r" instruction?

- A. 2
B. 3
C. 4
D. 5

gate2001-cse co-and-architecture data-path machine-instructions normal

Answer ↗

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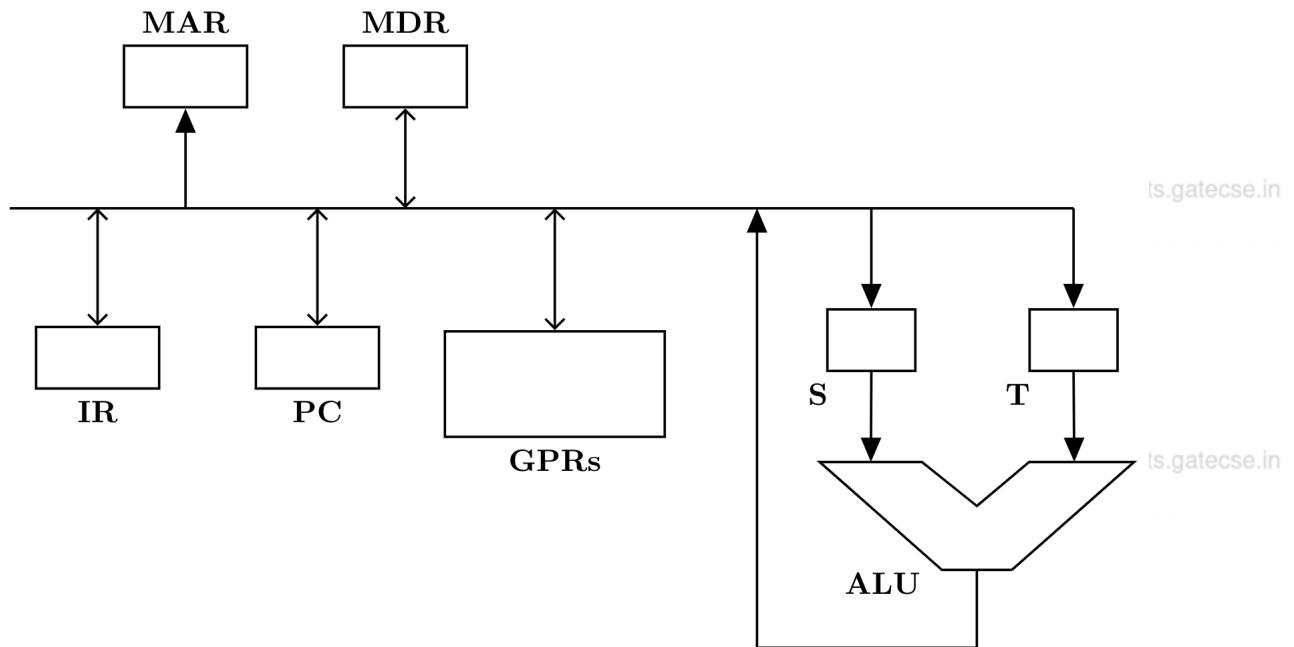
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1.8.3 Data Path: GATE CSE 2005 | Question: 79 top ↵

↗ <https://gateoverflow.in/1402>



Consider the following data path of a CPU.



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The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR.

The instruction "add R0, R1" has the register transfer interpretation $R0 \leftarrow R0 + R1$. The minimum number of clock cycles needed for execution cycle of this instruction is:

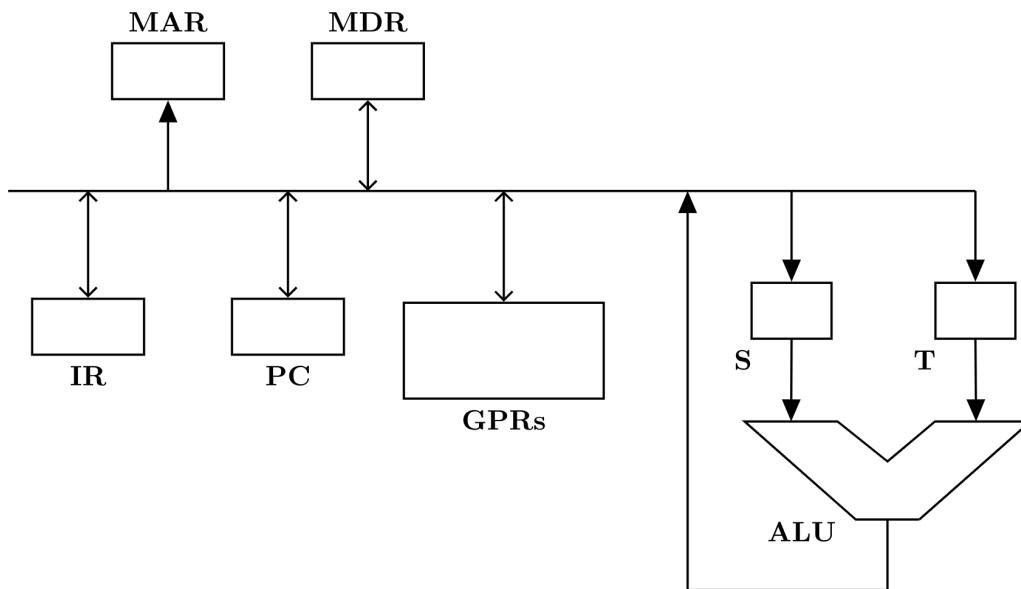
- A. 2
B. 3
C. 4
D. 5

Answer ↗

1.8.4 Data Path: GATE CSE 2005 | Question: 80 top ↗

↗ <https://gateoverflow.in/43568>

Consider the following data path of a CPU.



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The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR.

The instruction "call Rn, sub" is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is

$$Rn \leftarrow PC + 1;$$

$$PC \leftarrow M[PC];$$

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The minimum number of CPU clock cycles needed during the execution cycle of this instruction is:

- A. 2
- B. 3
- C. 4
- D. 5

Answer ↗

1.8.5 Data Path: GATE CSE 2016 Set 2 | Question: 30 top ↗

↗ <https://gateoverflow.in/39627>

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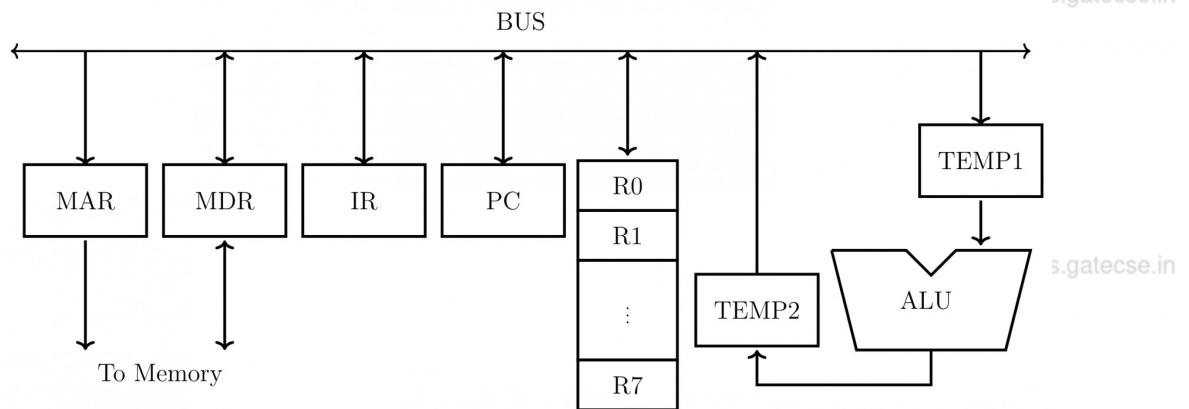
Suppose the functions F and G can be computed in 5 and 3 nanoseconds by functional units U_F and U_G , respectively. Given two instances of U_F and two instances of U_G , it is required to implement the computation $F(G(X_i))$ for $1 \leq i \leq 10$. Ignoring all other delays, the minimum time required to complete this computation is _____ nanoseconds.

Answer ↗

1.8.6 Data Path: GATE CSE 2020 | Question: 4 top ↗

↗ <https://gateoverflow.in/333227>

Consider the following data path diagram.



Consider an instruction: $R0 \leftarrow R1 + R2$. The following steps are used to execute it over the given data path. Assume that PC is incremented appropriately. The subscripts r and w indicate read and write operations, respectively.

1. $R2_r$, TEMP1_r, ALU_{add}, TEMP2_w
2. $R1_r$, TEMP1_w
3. PC_r , MAR_w, MEM_r
4. TEMP2_r, R0_w
5. MDR_r, IR_w

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Which one of the following is the correct order of execution of the above steps?

- A. 2, 1, 4, 5, 3
- B. 1, 2, 4, 3, 5
- C. 3, 5, 2, 1, 4
- D. 3, 5, 1, 2, 4

gate2020-cse co-and-architecture data-path

Answer ↗

Answers: Data Path

1.8.1 Data Path: GATE CSE 1990 | Question: 8a top ↗

↗ <https://gateoverflow.in/85669>



<pre> ✓ MAR ← PC PC ← PC +3 MDR ← MEM[MAR] IR ← MDR MAR ← MAR+1 MDR ← MEM[MAR] R0 ← MDR MAR ← MAR +1 MDR ← MEM[MAR] R1 ← MDR R0 ← R0+R1 </pre>
--

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Reference: [CPU Datapath Diagram from Hamacher](#)

References



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↗ [https://gateoverflow.in/731](#)



1.8.2 Data Path: GATE CSE 2001 | Question: 2.13 top ↗

↗ <https://gateoverflow.in/731>

- ✓ A microinstruction cannot be further broken down into two or more. It can take more than a cycle if it involves a memory access. The first instruction given here is not a microinstruction. It is an assembly language instruction.

It can be broken down as:

$T1, T2 : MAR \leftarrow SP$

$T3 : MDR \leftarrow r, SP \leftarrow SP - 1$ (It is not mandatory to decrement it in this cycle. Anyway, it can be decremented locally)

$T4, T5 : M[MAR] \leftarrow MDR$

The problem says, 8-bit MDR, 8-bit data bus, 8 bit registers. Can't you see that the given CPU is 8-bit? 8 multiplexers transfer 8 bits when selection input is 0 and 1 respectively. During cycle 1, bits in even positions are moved to MAR. During cycle 2, bits in odd positions are transferred to MAR. We certainly need to move 16-bit SP to 16-bit MAR via a 8-bit bus. So, 2 cycles to get SP to MAR.

The given data path has a single bus, which requires r to be carried in a separate cycle. For the contents of r to be moved to MDR during the cycles T1 or T2, address and data bus should be separate. Here, it ain't the case.

Memory read takes 2 more cycles. In total, we need 5 of them clock cycles to execute a push.

<https://www.cise.ufl.edu/~mssz/CompOrg/CDA-proc.html>

Computer organization pal chaudari page 334-335

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Computer architecture by behrooz parahmi exercise 7.6

Correct Answer: D

References



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50 votes

-- Rajaneesh Polavarapu (377 points)



1.8.3 Data Path: GATE CSE 2005 | Question: 79 [top](#)

<https://gateoverflow.in/1402>

- ✓ Instruction fetch requires two cycles but the question asks for the **execution part** only!

Now for execution:

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1. $R1_{out}, S_{in} \quad S \leftarrow R0 \quad - 1^{st}$ cycle
2. $R2_{out}, T_{in} \quad T \leftarrow R1 \quad - 2^{nd}$ cycle
3. $S_{out}, T_{out}, \text{Add } R0_{in} \quad R0 \leftarrow R0 + R1 \quad - 3^{rd}$ cycle

So, 3 cycles for execution.

As it is asked for only execution cycles, no of cycles required = 3.

Had it been asked for instruction cycles, then the answer will be 5.

Hence, option B is correct.

58 votes

-- Pooja Palod (24.1k points)



1.8.4 Data Path: GATE CSE 2005 | Question: 80 [top](#)

<https://gateoverflow.in/43568>



- $MAR \leftarrow PC \rightarrow 1$ cycle
- $S \leftarrow PC$ (Since these two actions are independent they can be done in same cycle)
- $MDR \leftarrow M[MAR] \rightarrow 2^{nd}$ cycle (**System BUS**)
- $Rn \leftarrow S + 1$ (ALU Is free and the two actions are independent.) (**Internal BUS**)
- $PC \leftarrow MDR \rightarrow 3$ rd cycle

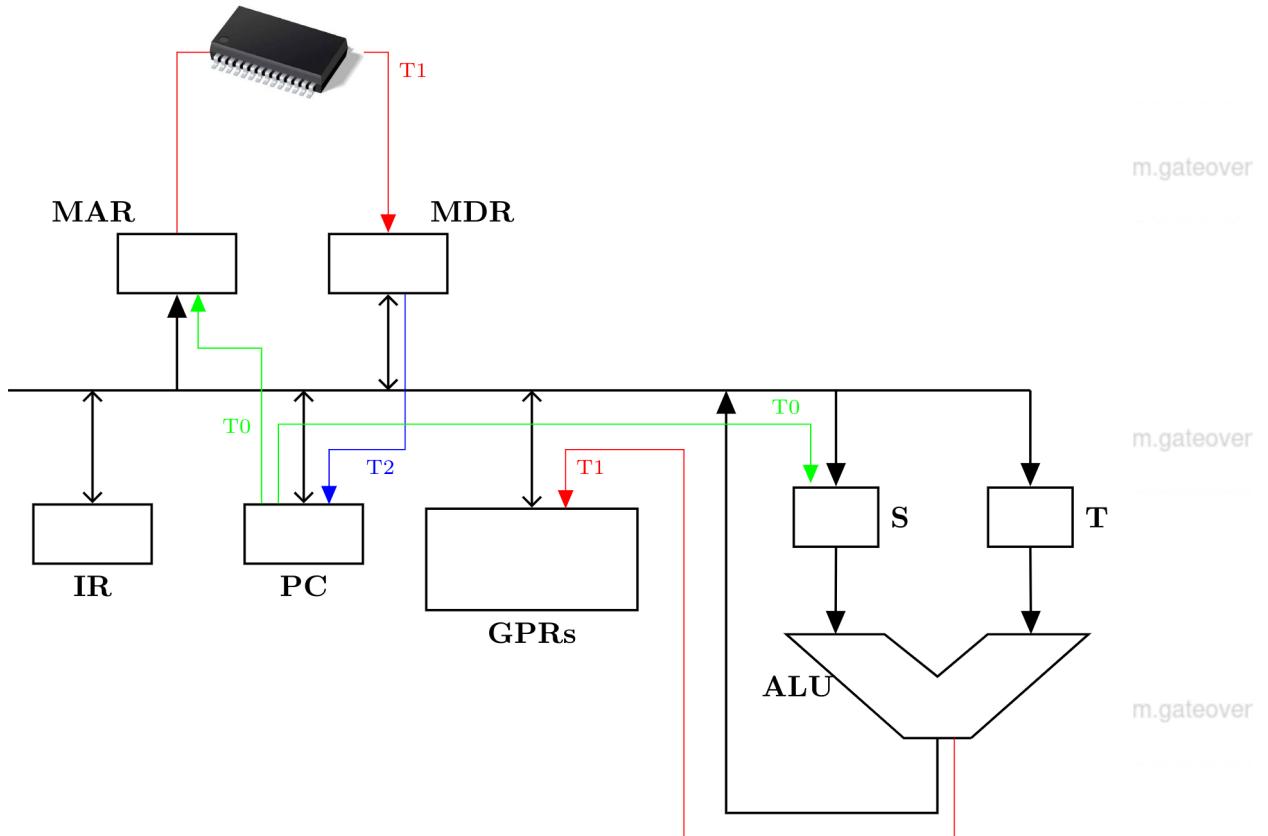
Therefore 3 cycles needed.

A rough sketch:

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Correct Answer: B

66 votes

-- Riya Roy(Arayana) (5.3k points)

1.8.5 Data Path: GATE CSE 2016 Set 2 | Question: 30 top ↗

→ <https://gateoverflow.in/39627>



- ✓ The same concept is used in pipelining. Bottleneck here is U_F as it takes 5 ns while U_G takes 3ns only. We have to do 10 such calculations and we have 2 instances of U_F and U_G respectively. So, U_F can be done in $50/2 = 25$ nano seconds. For the start U_F needs to wait for U_G output for 3 ns and rest all are pipelined and hence no more wait. So, answer is

$$3 + 25 = 28 \text{ ns.}$$

89 votes

-- Arjun Suresh (332k points)

1.8.6 Data Path: GATE CSE 2020 | Question: 4 top ↗

→ <https://gateoverflow.in/333227>



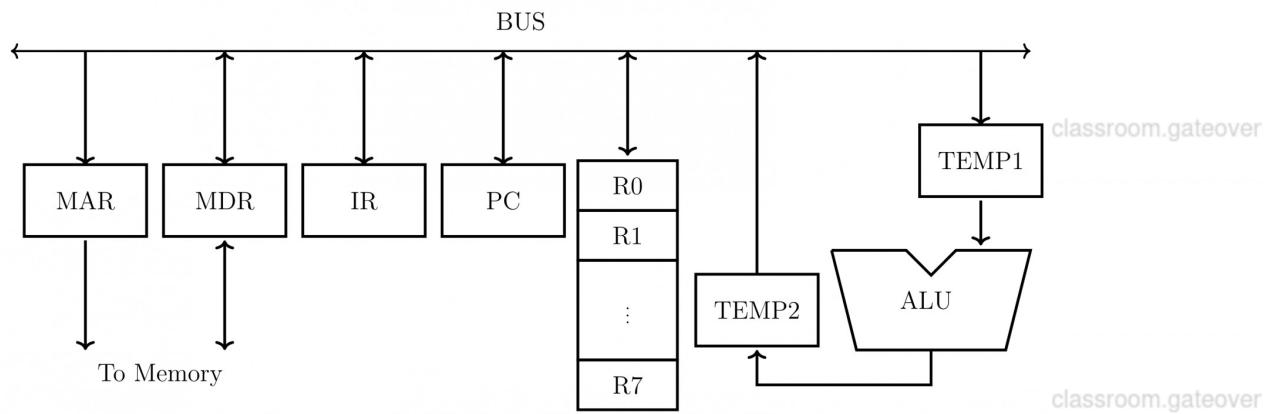
- ✓ 3rd followed by 5th are **Instruction fetch cycle** micro operations and can be elaborated as follows:

$t_1 : \text{MAR}_w \leftarrow \text{PC}_r$

$t_2 : \text{MDR}_w \leftarrow \text{Memory}_r \mid \text{PC} \leftarrow \text{PC} + 1$

$t_3 : \text{IR}_w \leftarrow \text{MDR}_r$

Now we need to perform **Execute cycle** micro operations. Just observe the figure and it will be very easy to identify the sequence between 1st, 2nd, 4th



2^{nd} is clearly stating that we need to move R1 content to some temporary register named as TEMP1 and it is very clear that before performing ALU operation we need the content in TEMP1. Hence 2^{nd} will be performed next after 5^{th} .

$$\text{TEMP1}_w \leftarrow \text{R1}_r$$

Now we can perform ALU operation and can take second operand directly from $R2$ and the figure clearly shows us that we need to put the result of ALU back into TEMP2. All these steps are performed in 1^{st} . So 1^{st} will be next.

$$\text{TEMP2}_w \leftarrow \text{TEMP1}_r +_{\text{ALU}_{\text{add}}} \text{R2}_r$$

Lastly we need to put the result present in TEMP2 into R0. This step is performed by 4^{th} .

$$\text{R0}_w \leftarrow \text{TEMP2}_r$$

Correct Answer (C) : 3, 5, 2, 1, 4

3 votes

-- KUSHAGRA जी (10.5k points)

1.9

Dma (6) top ↴

1.9.1 Dma: GATE CSE 2004 | Question: 68 top ↴

▪ <https://gateoverflow.in/1062>



A hard disk with a transfer rate of 10 Mbytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?

- A. 5.0%
- B. 1.0%
- C. 0.5%
- D. 0.1%

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[gate2004-cse](https://gate2004-cse.gateoverflow.in) [dma](https://gateoverflow.in/dma) [normal](https://gateoverflow.in/normal) [co-and-architecture](https://gateoverflow.in/co-and-architecture)

Answer ↗

1.9.2 Dma: GATE CSE 2005 | Question: 70 top ↴

▪ <https://gateoverflow.in/1393>



Consider a disk drive with the following specifications:

16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one 4 byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is:

- A. 10
- B. 25
- C. 40
- D. 50

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Answer ↗



On a non-pipelined sequential processor, a program segment, which is the part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

```

Initialize the address register
Initialize the count to 500
LOOP:
Load a byte from device
Store in memory at address given by address register
Increment the address register
Decrement the count
If count !=0 go to LOOP
  
```

Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.

The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.

What is the approximate speed up when the DMA controller based design is used in place of the interrupt driven program based input-output?

- A. 3.4
- B. 4.4
- C. 5.1
- D. 6.7

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Answer



The size of the data count register of a DMA controller is 16bits.

The processor needs to transfer a file of 29,154 kilobytes from disk to main memory.

The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____.

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Answer



Consider a computer system with DMA support. The DMA module is transferring one 8-bit character in one CPU cycle from a device to memory through *cycle stealing* at regular intervals. Consider a 2 MHz processor. If 0.5% processor cycles are used for DMA, the data transfer rate of the device is _____ bits per second.

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Answer



The storage area of a disk has the innermost diameter of 10 cm and outermost diameter of 20 cm. The maximum storage density of the disk is 1400 bits/cm. The disk rotates at a speed of 4200 RPM. The main memory of a computer has 64-bit word length and 1 μ s cycle time. If cycle stealing is used for data transfer from the disk, the percentage of memory cycles stolen for transferring one word is

- A. 0.5%
- B. 1%
- C. 5%
- D. 10%

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Answer



✓ Clock cycle time = $\frac{1}{600 \times 10^6}$ [Frequency = 1/Time]

For DMA initiation and completion = $\frac{(900+300)}{600 \times 10^6} = 2$ microsec .

Disk Transfer rate = 10 Mbytes/sec

1 byte = $\frac{1}{10^6}$ sec
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20 Kbytes = 2 milisec = 2000 micro sec

$$\text{Percentage} = \left(\frac{2}{2+2000} \right) \times 100 = 0.0999 \simeq 0.1\%$$

option (D)

% of CPU time consume $\frac{x}{x+y}$

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Now, when, use x = Data preparation time or Total cycle time used by CPU and y = Data transfer time

To calculate the fraction of CPU time to the data transfer time - we use $\frac{x}{x+y}$ it is burst mode.

81 votes

-- Prashant Singh (47.2k points)



512 KB-1/50 sec

4 Byte transfer will take total : $4/(512 \times 50 \times 2^{10}) = 152.58 ns$

DMA will transfer 4B in 40nsec

So, Cpu will be blocked $(40/152.58) = 26\%$ of time

Best matching answer is (B),w.in

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55 votes

-- Anurag Semwal (6.7k points)



✓

	Statement	Clock Cycles(s) Needed
classroom.gateoverflow.in	Initialize the address register	1
	Initialize the count to 500	1
LOOP:	Load a byte from device	2
	Store in memory at address given by address register	2
	Increment the address register	1
	Decrement the count	1
	If count != 0 go to LOOP	1

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Interrupt driven transfer time = $1 + 1 + 500 \times (2 + 2 + 1 + 1 + 1) = 3502$

DMA based transfer time = $20 + 500 \times 2 = 1020$

Speedup = $3502/1020 = 3.4$

Correct Answer: A

90 votes

-- Manu Thakur (34k points)



! Data count register gives the number of words the DMA can transfer in a single cycle..

Here it is 16 bits.. so max 2^{16} words can be transferred in one cycle..

Since memory is byte addressable.. 1 word = 1 byte
so 2^{16} bytes in 1 cycle..

Now for the given file..

$$\text{File size} = 29154 \text{ KB} = 29154 \times 2^{10} \text{ B}$$

1 cylce \rightarrow DMA transfers 2^{16} B

i.e.

$$1 \text{ B transferred by DMA} \rightarrow \frac{1}{2^{16}} \text{ cycles.}$$

Now, for full file of size 29154 KB,

$$\text{minimum number of cylces} = \frac{(29154 \times 2^{10} \text{ B})}{2^{16}} = 455.53$$

But number of cylces is asked so 455.53 \rightarrow 456.

57 votes

-- Abhilash Panicker (7.6k points)



✓ classroom.gateoverflow.in Answer is 80,000.

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To complete one cycle at 2 MHz it will take $\frac{1}{2 \times 10^6}$ seconds. So the total number of CPU cycles in one second will be 2×10^6 .

Now 0.5% of these cycles are taken by DMA to transfer the data.

So total number of cycles taken to transfer the data will be $\frac{0.5}{100} \times 2 \times 10^6 = 10,000$ and in each cycle 8 bits are transferred.

So, data transfer rate in bits per second = $8 \times 10000 = 80,000$

3 votes

-- JATIN MITTAL (2.1k points)



✓ In a disk all tracks have equal capacity and so data density is highest for the innermost track as it has the smallest radius.

- Maximum storage density (hence of innermost track) = 1400 bits per cm
- Track capacity $\pi \times d \times 1400$ bits = $3.14 \times 10 \times 1400 = 43960$ bits

With 4200 rotations per minute, data transfer rate = $\frac{4200 \times 43960}{60}$ bits per second.

Therefore, to transfer 64 bits time required = $\frac{60}{4200 \times 43960} \times 64 = 20.798\mu s$

With $1\mu s$ memory cycle time, the disk will take one memory cycle out of $21 + 1 = \frac{1}{21 + 1} \times 100 \approx 5\%$

(PS: If we consider just one word transfer we add the memory cycle time to the disk transfer time in the denominator but for continuous DMA transfer, this is not required as when data is transferred to main memory, disk can continue reading new data)

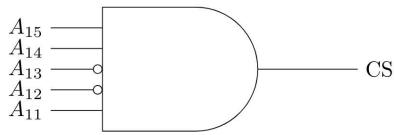
16 votes

-- gatecse (63.3k points)



The chip select logic for a certain DRAM chip in a memory system design is shown below. Assume that the memory system has 16 address lines denoted by A_{15} to A_0 . What is the range of address (in hexadecimal) of the memory system that can get

enabled by the chip select (CS) signal?



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- A. C800 to CFFF
- B. CA00 to CAFF
- C. C800 to C8FF
- D. DA00 to DFFF

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Answer

Answers: Dram

1.10.1 Dram: GATE CSE 2019 | Question: 2 [top](#)

<https://gateoverflow.in/302846>



- ✓ $(A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0)$

According to question: [gateoverflow.in](#)

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$A_{15} = 1, A_{14} = 1, A_{13} = 0, A_{12} = 0, A_{11} = 1$

So the possible range in binary:

(1100100000000000) to (1100111111111111)

Converting to Hexadecimal:

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Option A.

40 votes

-- Ruturaj Mohanty (3.1k points)

The memory system that can be enabled by the chip select signal

→ From this we can understand that, CS should be 1.

→ Note that it is AND gate, \implies all input lines should be 1.

→ $A_{15}.A_{14}.\overline{A_{13}}.\overline{A_{12}}.A_{11} = 1 \implies (A_{15} = 1 \text{ and } A_{14} = 1 \text{ and } \overline{A_{13}} = 1 \text{ and } \overline{A_{12}} = 1 \text{ and } A_{11} = 1)$

→ $\overline{A_{13}} = 1 \implies A_{13} = 0$

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→ $\overline{A_{12}} = 1 \implies A_{12} = 0$

\therefore The address denoted by A_{15} to A_0 is , (Note A_{15} as MSB and A_0 as LSB)

$(1100)(1___) (___) (___)$

→ For starting address, keep all 0's in the blanks, and for ending address keep all 1's in the blanks.

→ Starting address :- 1100 1000 0000 0000 $\implies (C800)_H$

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→ Ending address :- 1100 1111 1111 1111 $\implies (CFFF)_H$

21 votes

-- Shaik Masthan (50.4k points)

1.11

Instruction Execution (7) [top](#)

1.11.1 Instruction Execution: GATE CSE 1990 | Question: 4-iii [top](#)

<https://gateoverflow.in/85391>



State whether the following statements are TRUE or FALSE with reason:

The flags are affected when conditional CALL or JUMP instructions are executed.

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gate1990 true-false co-and-architecture instruction-execution

Answer

1.11.2 Instruction Execution: GATE CSE 1992 | Question: 01-iv [top](#)

<https://gateoverflow.in/548>



Many of the advanced microprocessors prefetch instructions and store it in an instruction buffer to speed up processing. This speed up is achieved because _____

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gate1992 co-and-architecture easy instruction-execution fill-in-the-blanks

Answer

1.11.3 Instruction Execution: GATE CSE 1995 | Question: 1.2 [top](#)

<https://gateoverflow.in/2589>



Which of the following statements is true?

- A. ROM is a Read/Write memory
- B. PC points to the last instruction that was executed
- C. Stack works on the principle of LIFO
- D. All instructions affect the flags

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gate1995 co-and-architecture normal instruction-execution

Answer

1.11.4 Instruction Execution: GATE CSE 2002 | Question: 1.13 [top](#)

<https://gateoverflow.in/817>



Which of the following is not a form of memory

- A. instruction cache
- B. instruction register
- C. instruction opcode
- D. translation look-a-side buffer

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gate2002-cse co-and-architecture easy instruction-execution

Answer

1.11.5 Instruction Execution: GATE CSE 2006 | Question: 43 [top](#)

<https://gateoverflow.in/1819>



Consider a new instruction named branch-on-bit-set (mnemonic bbs). The instruction “bbs reg, pos, label” jumps to label if bit in position pos of register operand reg is one. A register is 32 -bits wide and the bits are numbered 0 to 31, bit in position 0 being the least significant. Consider the following emulation of this instruction on a processor that does not have bbs implemented.

$temp \leftarrow reg \& mask$

Branch to label if temp is non-zero. The variable temp is a temporary register. For correct emulation, the variable mask must be generated by

- A. $mask \leftarrow 0x1 << pos$
- B. $mask \leftarrow 0xffffffff << pos$
- C. $mask \leftarrow pos$
- D. $mask \leftarrow 0xf$

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Answer **1.11.6 Instruction Execution: GATE CSE 2017 Set 1 | Question: 49** top<https://gateoverflow.in/11832>

Consider a RISC machine where each instruction is exactly 4 bytes long. Conditional and unconditional branch instructions use PC-relative addressing mode with Offset specified in bytes to the target location of the branch instruction. Further the Offset is always with respect to the address of the next instruction in the program sequence. Consider the following instruction sequence

Instr. No.	Instruction
i:	add R2, R3, R4
i+1:	sub R5, R6, R7
i+2:	goclasses.in cmp R1, R9, R10
i+3:	beq R1, Offset

If the target of the branch instruction is i , then the decimal value of the Offset is _____.

Answer **1.11.7 Instruction Execution: GATE CSE 2021 Set 2 | Question: 53** top<https://gateoverflow.in/35748>

Consider a pipelined processor with 5 stages, Instruction Fetch(IF), Instruction Decode(ID), Execute (EX), Memory Access (MEM), and Write Back (WB). Each stage of the pipeline, except the EX stage, takes one cycle. Assume that the ID stage merely decodes the instruction and the register read is performed in the EX stage. The EX stage takes one cycle for ADD instruction and the register read is performed in the EX stage. The EX stage takes one cycle for ADD instruction and two cycles for MUL instruction. Ignore pipeline register latencies.

Consider the following sequence of 8 instructions:

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ADD, MUL, ADD, MUL, ADD, MUL, ADD, MUL

Assume that every MUL instruction is data-dependent on the ADD instruction just before it and every ADD instruction (except the first ADD) is data-dependent on the MUL instruction just before it. The *speedup* defined as follows.

$$\text{Speedup} = \frac{\text{Execution time without operand forwarding}}{\text{Execution time with operand forwarding}}$$

The *Speedup* achieved in executing the given instruction sequence on the pipelined processor (rounded to 2 decimal places) is

Answer **Answers: Instruction Execution****1.11.1 Instruction Execution: GATE CSE 1990 | Question: 4-iii** top<https://gateoverflow.in/85391>

False. Flags are tested during conditional call and jump not affected or changed

 15 votes

-- khush tak (5.9k points)

1.11.2 Instruction Execution: GATE CSE 1992 | Question: 01-iv top<https://gateoverflow.in/548>

- ✓ Because CPU is faster than memory. Fetching instructions from memory would require considerable amount of time while CPU is much faster. So, prefetching the instructions to be executed can save considerable amount of waiting time.

 23 votes

-- Arjun Suresh (332k points)

1.11.3 Instruction Execution: GATE CSE 1995 | Question: 1.2 top<https://gateoverflow.in/2589>

- ✓ It is (C).

Only the top of the stack can be accessed at any time. You can imagine a stack to be opened from only one side data structure. So that if we put one thing over the other, we are able to access the last thing we inserted first. That is Last in First Out (LIFO).

- ROM is Read-Only Memory.
- PC points to the next instruction to be executed.
- Not all instructions affect the flags.

19 votes

-- Gate Keeda (15.9k points)

1.11.4 Instruction Execution: GATE CSE 2002 | Question: 1.13 top

<https://gateoverflow.in/817>



- ✓ The instruction opcode is a part of the instruction which tells the processor what operation is to be performed so it is not a form of memory while the others are

26 votes

-- Bhagirathi Nayak (11.7k points)

1.11.5 Instruction Execution: GATE CSE 2006 | Question: 43 top

<https://gateoverflow.in/1819>



A. $mask \leftarrow 0x1 << pos$

We want to check for a particular bit position say 2 (third from right). Let the number be $0xA2A7$ (last 4 bits being 0111). Here, the bit at position 2 from right is 1. So, we have to AND this with $0x0004$ as any other flag would give wrong value (may count other bits or discard the bit at position "pos"). And $0x0004$ is obtained by $0x1 << 2$ (by shifting 1 "pos" times to the left we get a flag with 1 being set only for the "pos" bit position).

45 votes

-- Arjun Suresh (332k points)

1.11.6 Instruction Execution: GATE CSE 2017 Set 1 | Question: 49 top

<https://gateoverflow.in/118332>



- ✓ Answer is **-16**.

Program Counter is updated with the address of next instruction even before the current instruction is executed.

That is why the question says that the address of the next instruction is updated with next instruction in sequence.

Before executing instruction $i + 3$, the current state looks as under:

Please note: BEQ instruction is for Branch Equal

Address		
2000	i	add R2, R3, R4
2004	i+1	sub R5, R6, R7
2008	i+2	cmp R1, R9, R10
2012	i+3	beq R1, Offset
2016		Next instruction

Program Counter is pointing here →

Question says that the target of branch instruction is 'i' which is at 2000 in our example.

So, we need to go to address **2000** from address 2016 (which is currently pointed by PC)

2016 – 2000 = 16

So, we have to specify Offset as **-16** which would mean that 16 should be subtracted from next address instruction (2016).

51 votes

-- Arunav Khare (3.9k points)

1.11.7 Instruction Execution: GATE CSE 2021 Set 2 | Question: 53 top

<https://gateoverflow.in/357484>



- ✓ Correct Answer: **1.875**

$$\text{Speedup(def in question)} = \frac{\text{Time without Operand Forwarding}}{\text{Time with Operand Forwarding}}$$

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Without Operand Forwarding:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
ADD	IF	ID	EX	MEM	WB																					
MUL	IF	ID			EX	EX	MEM	WB																		
ADD		IF			ID				EX	MEM	WB															
MUL					IF				ID			EX	EX	MEM	WB											
ADD									IF			ID								EX	MEM	WB				
MUL												IF							ID			EX	EX	MEM	WB	
ADD																			IF		ID			EX	MEM	WB
MUL																				IF					ID	

Time taken without Operand Forwarding = 30

With Operand Forwarding:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ADD	IF	ID	EX	MEM	WB											
MUL	IF	ID	EX	EX	MEM	WB										
ADD		IF	ID		EX	MEM	WB									
MUL			IF		ID	EX	EX	MEM	WB							
ADD					IF	ID		EX	MEM	WB						
MUL						IF		ID	EX	EX	MEM	WB				
ADD								IF	ID		EX	MEM	WB			
MUL									IF		ID	EX	EX	MEM	WB	

Time taken with Operand Forwarding = 16

$$\text{Speedup} = \frac{\text{Time without Operand Forwarding}}{\text{Time with Operand Forwarding}} = \frac{30}{16} = 1.875$$

7 votes

-- Cringe is my middle name... (885 points)

1.12

Instruction Format (7) [top](#)

1.12.1 Instruction Format: GATE CSE 1988 | Question: 2-ii [top](#)

<https://gateoverflow.in/91676>



Using an expanding opcode encoding for instructions, is it possible to encode all of the following in an instruction format shown in the below figure. Justify your answer.

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- 14 double address instructions
- 127 single address instructions
- 60 no address (zero address) instructions

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← 4 bits →	← 6 bits →	← 6 bits →
Opcode	Operand 1 Address	Operand 2 Address

[gate1988](#) [normal](#) [co-and-architecture](#) [instruction-format](#) [descriptive](#)

Answer [ask](#)

1.12.2 Instruction Format: GATE CSE 1992 | Question: 01-vi [top](#)

<https://gateoverflow.in/551>



In an 11-bit computer instruction format, the size of address field is 4-bits. The computer uses expanding OP code technique and has 5 two-address instructions and 32 one-address instructions. The number of zero-address instructions it can support is _____

[gate1992](#) [co-and-architecture](#) [machine-instructions](#) [instruction-format](#) [normal](#) [numerical-answers](#)

Answer [ask](#)

1.12.3 Instruction Format: GATE CSE 1994 | Question: 3.2 [top](#)

<https://gateoverflow.in/2479>



State True or False with one line explanation

Expanding opcode instruction formats are commonly employed in RISC. (Reduced Instruction Set Computers) machines.

Answer

1.12.4 Instruction Format: GATE CSE 2014 Set 1 | Question: 9 [top](#)<https://gateoverflow.in/1767>

A machine has a $32-bit$ architecture, with $1-word$ long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is _____.

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Answer

1.12.5 Instruction Format: GATE CSE 2016 Set 2 | Question: 31 [top](#)<https://gateoverflow.in/39601>

Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is _____.

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Answer

1.12.6 Instruction Format: GATE CSE 2018 | Question: 51 [top](#)<https://gateoverflow.in/204126>

A processor has 16 integer registers (R_0, R_1, \dots, R_{15}) and 64 floating point registers (F_0, F_1, \dots, F_{63}). It uses a 2-byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3, and Type-4. Type-1 category consists of four instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of fourteen instructions, each with one integer register operand and one floating point register operand (1R+1F). Type-4 category consists of N instructions, each with a floating point register operand (1F).

The maximum value of N is _____.

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Answer

1.12.7 Instruction Format: GATE CSE 2020 | Question: 44 [top](#)<https://gateoverflow.in/333187>

A processor has 64 registers and uses 16-bit instruction format. It has two types of instructions: I-type and R-type. Each I-type instruction contains an opcode, a register name, and a 4-bit immediate value. Each R-type instruction contains an opcode and two register names. If there are 8 distinct I-type opcodes, then the maximum number of distinct R-type opcodes is _____.

Answer

Answers: Instruction Format

1.12.1 Instruction Format: GATE CSE 1988 | Question: 2-ii [top](#)<https://gateoverflow.in/91676>

- ✓ 4 bits are for the opcode so number of 2 address instructions will be $2^4 = 16$ – so 14 double instructions are possible.

But out of 16 only 14 are used so 2 are still left which can be used for 1 address instruction. For 1 address instruction we can use not only the 2 left over but also the 6 bits of operand 1 (to make it one address) – so 6 bits that is 64. So, total 2×64 single address instructions can be supported – So, 127 single instructions are possible

But out of 128, 127 are used so 1 left which can be used for zero-address instruction. To make number of zero address we can use the operand 2 address (we already included operand 1 address) – 6 bits. So, total number possible is 64. So, total $1 \times 64 = 64$ zero address instructions are possible.

So, all encoding are possible.

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24 votes

-- Pavan Kumar Munnam (7.4k points)

1.12.2 Instruction Format: GATE CSE 1992 | Question: 01-vi [top](#)

<https://gateoverflow.in/551>



- ✓ No. of possible instruction encoding = $2^{11} = 2048$

No. of encoding taken by two-address instructions = $5 \times 2^4 \times 2^4 = 1280$

No. of encoding taken by one-address instructions = $32 \times 2^4 = 512$

So, no. of possible zero-address instructions = $2048 - (1280 + 512) = 256$

64 votes

-- Arjun Suresh (332k points)

1.12.3 Instruction Format: GATE CSE 1994 | Question: 3.2 [top](#)

<https://gateoverflow.in/2479>



- ✓ I think the answer is **TRUE**.

RISC systems use fixed length instruction to simplify pipeline.

eg: MIPS, PowerPC: Instructions are 4 bytes long.

CISC systems use Variable-length instructions.

eg: Intel 80X86: Instructions vary from 1 to 17 bytes long.

Now the challenge is: How to fit multiple sets of instruction types into same (limited) number of bits (Fixed size instruction)?

Here comes Expanding opcode into the picture.

RISC systems commonly uses Expanding opcode technique to have fixed size instructions.

39 votes

-- Sachin Mittal (15.8k points)

1.12.4 Instruction Format: GATE CSE 2014 Set 1 | Question: 9 [top](#)

<https://gateoverflow.in/1767>



- ✓ 64 registers means 6 bits ($\lceil \log_2 64 \rceil = 6$) for a register operand. So, 2 registers operand requires 12 bits. Now, 45 instructions require another 6 bits for opcode ($\lceil \log_2 45 \rceil = 6$). So, totally 18 bits. So, we have $32 - 18 = 14$ bits left for the immediate operand. So, the max value will be $2^{14} - 1 = 16383$ (as the operand is unsigned we do not need a sign bit and with 14 bits we can represent from 0 to $2^{14} - 1$)

82 votes

-- Arjun Suresh (332k points)

1.12.5 Instruction Format: GATE CSE 2016 Set 2 | Question: 31 [top](#)

<https://gateoverflow.in/39601>



- ✓ Answer: 500 bytes

Number of registers = 64

Number of bits to address register = $\lceil \log_2 64 \rceil = 6$ bits

Number of Instructions = 12

Opcode size = $\lceil \log_2 12 \rceil = 4$

Opcode(4)	reg1(6)	reg2(6)	reg3(6)	Immediate(12)
-----------	---------	---------	---------	---------------

Total bits per instruction = 34

Total bytes per instruction = 4.25

Due to byte alignment we cannot store 4.25 bytes, without wasting 0.75 bytes.

So, total bytes per instruction = 5

Total number of instructions = 100

Total size = Number of instructions × Size of an instruction

$$= 100 \times 5 = 500 \text{ bytes}$$

95 votes

-- Akash Kanase (36k points)

1.12.6 Instruction Format: GATE CSE 2018 | Question: 51 [top](#)

<https://gateoverflow.in/204126>



- ✓ We have 2-byte instruction format. So, total number of instruction encodings = 2^{16}

PS: This is not the number of different instructions but different encodings; a single instruction can have different encodings when the address part differs.

No. of bits taken by an integer operand (16 possible integer registers) = $\log_2 16 = 4$.

No. of bits taken by a floating point operand (64 possible floating point registers) = $\log_2 64 = 6$.

No. of encodings consumed by Type 1 instructions = $4 \times 2^{3 \times 4} = 2^{14}$.

No. of encodings consumed by Type 2 instructions = $8 \times 2^{2 \times 6} = 2^{15}$.

No. of encodings consumed by Type 3 instructions = $14 \times 2^{(4+6)} = 14336$.

No. of encodings left for Type 4 = $2^{16} - (2^{14} + 2^{15} + 14336) = 2048$.

No. of different instructions of Type 4 = $\frac{2048}{64} = 32$.

83 votes

-- Arjun Suresh (332k points)

Answer: 32 Instructions

Explanation:

Given,

16 Integer registers. So, we need 4 bits to address any one of them.

64 Floating point registers. This requires 6 bits to uniquely identify them.

Each instruction is 16 bits long.

Type 1 Instructions:

4 instructions, each with 3 integer operands.

The 3 integers, each requires 4 bits. So, $4 * 3$ bits for operands. We are left with $16 - 12 = 4$ bits.

With 4 bits, $2^4 = 16$ opcodes are possible. Out of these we used 4 opcodes. i.e 2 bits. Let's say first two bits are fixed to 00 and next two bits are used for 4 different Type1 instructions.

00 00 ...

00 01 ...

00 10 ...

00 11 ...

Type 2 Instructions:

8 instructions, each with 2 floating point register operands.

Here we need $6 * 2$ bits for operands, and remaining $16 - 12 = 4$ bits are left for opcodes.

So using these 4 bits, we need to get 8 opcodes.

Here we can't use 00 ... for any opcode since it will not distinguish Type 2 from Type 1. So, we are left with 12 opcodes. And we are going to use 8 out of these 12 for type 2 instructions.

01 00 ...

01 01 ...

01 10 ...

01 11 ...

10 00 ...

10 01 ...

10 10 ...

10 11 ...

Type 3 Instructions:

14 instructions, with 1 integer and 1 floating type operand.

$4 + 6 = 10$ bits required for opcodes, remaining $16 - 10 = 6$ bits available for use in opcode.

The only valid combination left for this first 2 bits is 11 Rest have been used in Type1 and Type2 instructions.

So, we are left with 4 bits for opcodes. With these 4 bits we can have $2^4 = 16$ opcodes, out of which 14 are required. So, we use all except last two opcodes:

11 00 00 ...

11 ...

11 11 01 ...

These two opcodes are still left unassigned.

11 11 10 ...

11 11 11 ...

Type 4 Instructions:

N instructions, each with 1 floating point operand.

We have $16 - 6 = 10$ bits for opcode. Out of 10 bits, first 6 bits can be either one of the two left opcodes(above). And any combination for remaining 4 bits.

So we have $2 * 2^4$ opcodes. So, N = 32.

103 votes

-- Rishabh Gupta (12.5k points)

1.12.7 Instruction Format: GATE CSE 2020 | Question: 44 top

<https://gateoverflow.in/333187>



- ✓ Instruction Length: 16 bits

To distinguish among 64 registers, we need $\log_2(64) = 6$ bits

I-type instruction format:

Opcode	Register	Immediate Value
--------	----------	-----------------

R-type instruction format:

Opcode	Register	Register
--------	----------	----------

Maximum possible encodings = 2^{16}

It is given that there are 8 I-type instructions. Let's assume the maximum R-type instructions to be x.

$$\text{Therefore, } (8 \times 2^6 \times 2^4) + (x \times 2^6 \times 2^6) = 2^{16}$$

$$\implies x = 16 - 2 = 14$$

32 votes

-- Debasish Das (1.5k points)

1.13

Interrupts (7) top

<https://gateoverflow.in/80274>



1.13.1 Interrupts: GATE CSE 1987 | Question: 1-viii top

<https://gateoverflow.in/80274>

<a href="https://gateoverflow



In a vectored interrupt:

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- A. The branch address is assigned to a fixed location in memory
- B. The interrupting source supplies the branch information to the processor through an interrupt vector
- C. The branch address is obtained from a register in the processor
- D. None of the above

[gate1995](#) [co-and-architecture](#) [interrupts](#) [normal](#)

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Answer



Which of the following is true?

- A. Unless enabled, a CPU will not be able to process interrupts.
- B. Loop instructions cannot be interrupted till they complete.
- C. A processor checks for interrupts before executing a new instruction.
- D. Only level triggered interrupts are possible on microprocessors.

[gate1998](#) [co-and-architecture](#) [interrupts](#) [normal](#)

Answer



A device employing INTR line for device interrupt puts the CALL instruction on the data bus while:

- A. \overline{INTA} is active
- B. HOLD is active
- C. READY is inactive
- D. None of the above

[gate2002-cse](#) [co-and-architecture](#) [interrupts](#) [normal](#)

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Answer

A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be $4\mu\text{sec}$. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program-controlled mode?

- A. 15
- B. 25
- C. 35
- D. 45

[gate2005-cse](#) [co-and-architecture](#) [interrupts](#)

Answer



A CPU generally handles an interrupt by executing an interrupt service routine:

- A. As soon as an interrupt is raised.
- B. By checking the interrupt register at the end of fetch cycle.
- C. By checking the interrupt register after finishing the execution of the current instruction.

D. By checking the interrupt register at fixed time intervals.

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gate2009-cse co-and-architecture interrupts normal ugcnetjune2012iii

Answer 

1.13.7 Interrupts: GATE CSE 2020 | Question: 3 top ↗

→ <https://gateoverflow.in/333228>



Consider the following statements.

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- I. Daisy chaining is used to assign priorities in attending interrupts.
- II. When a device raises a vectored interrupt, the CPU does polling to identify the source of interrupt.
- III. In polling, the CPU periodically checks the status bits to know if any device needs its attention.
- IV. During DMA, both the CPU and DMA controller can be bus masters at the same time.

Which of the above statements is/are TRUE?

- A. I and II only
- B. I and IV only
- C. I and III only
- D. III only

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Answer 

Answers: Interrupts

1.13.1 Interrupts: GATE CSE 1987 | Question: 1-viii top ↗

→ <https://gateoverflow.in/80274>



- ✓ Answer should be (D) i.e branches off to ISR after completing current instruction.

CPU checks the status bit of interrupt at the completion of each current instruction running when there is a interrupt it service the interrupt using ISR.

<https://gateoverflow.in/18581/isro2009-78>

References



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 17 votes

-- Gate Mission (2.8k points)

1.13.2 Interrupts: GATE CSE 1995 | Question: 1.3 top ↗

→ <https://gateoverflow.in/2590>



- ✓ Answer: B [Answer](#) [Bn.gateoverflow.in](#)

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A vectored interrupt is a processing technique in which the interrupting device directs the processor to the appropriate interrupt service routine. This is in contrast to a polled interrupt system, in which a single interrupt service routine must determine the source of the interrupt by checking all potential interrupt sources, a slow and relatively laborious process.

 33 votes

-- Rajarshi Sarkar (27.9k points)

1.13.3 Interrupts: GATE CSE 1998 | Question: 1.20 top ↗

→ <https://gateoverflow.in/1657>



- ✓ Answer is (A).

Options (B) and (D) are obviously false.

A processor checks for the interrupt before FETCHING an instruction, so option (C) is also false.

 44 votes

-- Hardi Shah (281 points)



- ✓ INTR is a signal which if enabled then microprocessor has interrupt enabled it receives high INR signal & activates INTA signal, so another request can't be accepted till CPU is busy in servicing interrupt. Hence (A) is correct option.

22 votes

-- Tejas Jaiswal (559 points)



- ✓ In Programmed I/O, the CPU issues a command and waits for I/O operations to complete.

So here, CPU will wait for 1 sec to transfer 10 KB of data.

overhead in programmed I/O = 1 sec

In Interrupt mode , data is transferred word by word (here word size is 1 byte as mentioned in question "Data is transferred byte-wise").

So to transfer 1 byte of data overhead is 4×10^{-6} sec

Thus to transfer 10 KB of data overhead is= $4 \times 10^{-6} \times 10^4$ sec

$$\text{Performance gain} = \frac{1}{4 \times 10^{-6} \times 10^4} = \frac{1}{4 \times 10^{-2}} = 25$$

Thus, (b) is correct answer.

91 votes

-- ashwini anand (231 points)



- ✓ It will be (C).

After finishing the execution of each instruction the CPU reads the interrupt pins to recognize the interrupts.

INTR = 1 = Interrupt is present.(Service the Interrupt)

INTERRUPT = 0 = Interrupt is not present.(Goto next Instruction fetch from user program)

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29 votes

-- Gate Keeda (15.9k points)



- ✓ Answer : C

I is true

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- The **daisy-chaining** method of establishing **priority** consists of a serial connection of all devices that request an interrupt. The device with the highest **priority** is placed in the first position, followed by lower-**priority** devices up to the device with the lowest **priority**, which is placed last in the **chain**.

II. is false

- Vectored interrupts are achieved by assigning each interrupting device a unique code, typically four to eight bits in length. When a device interrupts, it sends its unique code over the data bus to the processor, telling the processor which interrupt service routine to execute.

III. is true

- The process of **periodically checking status bits** to see if it is time for the next I/O operation, is called **polling**. **Polling** is the simplest way for an I/O device to communicate with the processor the processor.

IV. is false

- Since CPU release bus only after getting request from DMA and get after DMA release the BUS.

8 votes

-- Prashant Singh (47.2k points)

1.14.1 Io Handling: GATE CSE 1987 | Question: 2a [top](#)<https://gateoverflow.in/80572>

State whether the following statements are TRUE or FALSE

In a microprocessor-based system, if a bus (DMA) request and an interrupt request arrive simultaneously, the microprocessor attends first to the bus request.

[gate1987](#) [co-and-architecture](#) [interrupts](#) [io-handling](#) [true-false](#)

[Answer](#)

1.14.2 Io Handling: GATE CSE 1987 | Question: 2b [top](#)<https://gateoverflow.in/80576>

State whether the following statements are TRUE or FALSE:

Data transfer between a microprocessor and an I/O device is usually faster in memory-mapped-I/O scheme than in I/O-mapped -I/O scheme.

[gate1987](#) [co-and-architecture](#) [io-handling](#) [true-false](#)

[Answer](#)

1.14.3 Io Handling: GATE CSE 1990 | Question: 4-ii [top](#)<https://gateoverflow.in/85390>

State whether the following statements are TRUE or FALSE with reason:

The data transfer between memory and I/O devices using programmed I/O is faster than interrupt-driven I/O.

[gate1990](#) [true-false](#) [co-and-architecture](#) [io-handling](#) [interrupts](#)

[Answer](#)

1.14.4 Io Handling: GATE CSE 1996 | Question: 1.24 [top](#)<https://gateoverflow.in/278>

For the daisy chain scheme of connecting I/O devices, which of the following statements is true?

- A. It gives non-uniform priority to various devices
- B. It gives uniform priority to all devices
- C. It is only useful for connecting slow devices to a processor device
- D. It requires a separate interrupt pin on the processor for each device

[gate1996](#) [co-and-architecture](#) [io-handling](#) [normal](#)

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[Answer](#)

1.14.5 Io Handling: GATE CSE 1996 | Question: 25 [top](#)<https://gateoverflow.in/2777>

A hard disk is connected to a 50 MHz processor through a DMA controller. Assume that the initial set-up of a DMA transfer takes 1000 clock cycles for the processor, and assume that the handling of the interrupt at DMA completion requires 500 clock cycles for the processor. The hard disk has a transfer rate of 2000 Kbytes/sec and average block transferred is 4 K bytes. What fraction of the processor time is consumed by the disk, if the disk is actively transferring 100% of the time?

[gate1996](#) [co-and-architecture](#) [io-handling](#) [dma](#) [numerical-answers](#) [normal](#)

[Answer](#)

1.14.6 Io Handling: GATE CSE 1997 | Question: 2.4 [top](#)<https://gateoverflow.in/2230>

The correct matching for the following pairs is:

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- | | |
|--|--|
| (A) DMA I/O
(B) Cache
(C) Interrupt I/O
(D) Condition Code Register | (1) High speed RAM
(2) Disk
(3) Printer
(4) ALU |
|--|--|

- A. $A - 4 \quad B - 3 \quad C - 1 \quad D - 2$
 B. $A - 2 \quad B - 1 \quad C - 3 \quad D - 4$
 C. $A - 4 \quad B - 3 \quad C - 2 \quad D - 1$
 D. $A - 2 \quad B - 3 \quad C - 4 \quad D - 1$

gate1997 co-and-architecture normal io-handling

Answer 

1.14.7 Io Handling: GATE CSE 2008 | Question: 64, ISRO2009-13 [top](#)

<https://gateoverflow.in/487>



Which of the following statements about synchronous and asynchronous I/O is NOT true?

- A. An ISR is invoked on completion of I/O in synchronous I/O but not in asynchronous I/O
- B. In both synchronous and asynchronous I/O, an ISR (Interrupt Service Routine) is invoked after completion of the I/O
- C. A process making a synchronous I/O call waits until I/O is complete, but a process making an asynchronous I/O call does not wait for completion of the I/O
- D. In the case of synchronous I/O, the process waiting for the completion of I/O is woken up by the ISR that is invoked after the completion of I/O

gate2008-cse operating-system io-handling normal isro2009

Answer 

Answers: Io Handling

1.14.1 Io Handling: GATE CSE 1987 | Question: 2a [top](#)

<https://gateoverflow.in/80572>



The HOLD input has a higher priority than the INTR or NMI interrupt inputs.

So the answer is true.

 5 votes

-- mystylecse (1.8k points)

1.14.2 Io Handling: GATE CSE 1987 | Question: 2b [top](#)

<https://gateoverflow.in/80576>



True

it will take extra time in IO mapped IO because of control signal.

 0 votes

-- Arnabh Gangwar (307 points)

1.14.3 Io Handling: GATE CSE 1990 | Question: 4-ii [top](#)

<https://gateoverflow.in/85390>



- ✓ False because in programmed I/O, CPU will check the I/O devices' status according to written program. Suppose CPU requested 5 I/O devices and the program is written to check sequentially and 5th device is ready before 2nd device, then also CPU will come to check at its turn.

So, programmed I/O doesn't care about availability status of devices. it blindly works according to written program. That's why it is slow.

Interrupt driven I/O : Here, if any device is ready then it won't wait for CPU, it will say to CPU that "I am ready" by sending interrupt request and the delay here will be only "time taken in servicing the interrupt" which is less than programmed I/O.

So, the answer is **FALSE**.

 40 votes

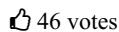
-- bharti (2.3k points)



- ✓ Daisy chaining approach tells the processor in which order the interrupt should be handled by providing priority to the devices.

In daisy-chaining method, all the devices are connected in serial. The device with the highest priority is placed in the first position, followed by lower priority devices. The interrupt pin is common to all.

So answer is option (A).



46 votes

-- Ravi Singh (11.8k points)



- ✓ 2000 KB is transferred in 1 second

$$4 KB \text{ transfer is } (4/2000) * 1000 \text{ ms} = 2 \text{ ms}$$

Total cycle required for locking and handling of interrupts after DMA transfer control

$$= (1000 + 500) \text{ clock cycle} = 1500 \text{ clock cycle}$$

$$\text{Now, } 50 \text{ Mhz} = 50 * 10^6 = 0.02 \text{ microsecond}$$

$$\text{So, } (1500 * 0.02) = 30 \text{ microsecond}$$

$30\mu s$ for initialization and termination and $2ms$ for data transfer.

The CPU time is consumed only for initialization and termination.

$$\text{Fraction of CPU time consumed} = \frac{30\mu s}{(30\mu s + 2ms)} = 0.015$$



45 votes

-- Pooja Palod (24.1k points)



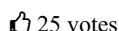
- ✓ Correct Option: B. A – 2, B – 1, C – 3, D – 4

A.	DMA I/O	2.	Disk
B.	Cache	1.	High-speed RAM
C.	Interrupt I/O	3.	Printer
D.	Condition Code Register	4.	ALU

Reason:

- **DMA I/O** - For high speed, high volume data transfer from disk without affecting the processor(in most cases).
- Cache-A high speed & low memory version of a RAM.
- **Interrupt I/O** - The printer sends an interrupt signal when it is ready for use.
- **Condition Code Register** - Part of the ALU, as a special purpose register, to store flag bits.

[Source - Google/Wikipedia]



25 votes

-- Siddharth Mahapatra (1.2k points)



- ✓ Answer is (B).

In synchronous I/O process performing I/O operation will be placed in blocked state till the I/O operation is completed. An ISR will be invoked after the completion of I/O operation and it will place process from block state to ready state.

In asynchronous I/O, Handler function will be registered while performing the I/O operation. The process will not be placed in

the block state and process continues to execute the remaining instructions. when the I/O operation completed signal mechanism is used to notify the process that data is available.

72 votes

1 vote

-- gate_asp (615 points)

1.15

Machine Instructions (19) [top](#)

1.15.1 Machine Instructions: GATE CSE 1988 | Question: 9i [top](#)

<https://gateoverflow.in/94384>



The following program fragment was written in an assembly language for a single address computer with one accumulator register:

```
LOAD B
MULT C
STORE T1
ADD A
STORE T2
MULT T2
ADD T1
STORE Z
```

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Give the arithmetic expression implemented by the fragment.

gate1988 normal descriptive co-and-architecture machine-instructions

Answer

1.15.2 Machine Instructions: GATE CSE 1994 | Question: 12 [top](#)

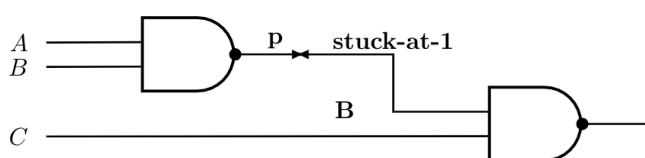
<https://gateoverflow.in/2508>



- A. Assume that a CPU has only two registers R_1 and R_2 and that only the following instruction is available $XOR R_i, R_j; \{R_j \leftarrow R_i \oplus R_j, \text{ for } i, j = 1, 2\}$

Using this XOR instruction, find an instruction sequence in order to exchange the contents of the registers R_1 and R_2

- B. The line p of the circuit shown in figure has stuck at 1 fault. Determine an input test to detect the fault.



gate1994 co-and-architecture machine-instructions normal descriptive

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Answer

1.15.3 Machine Instructions: GATE CSE 1999 | Question: 17 [top](#)

<https://gateoverflow.in/1516>



Consider the following program fragment in the assembly language of a certain hypothetical processor. The processor has three general purpose registers $R1$, $R2$ and $R3$. The meanings of the instructions are shown by comments (starting with ;) after the instructions.

```
X: CMP R1, 0; Compare R1 and 0, set flags appropriately in status register
JZ Z; Jump if zero to target Z
MOV R2, R1; Copy contents of R1 to R2
SHR R1; Shift right R1 by 1 bit
SHL R1; Shift left R1 by 1 bit
CMP R2, R1; Compare R2 and R1 and set flag in status register
JZ Y; Jump if zero to target Y
INC R3; Increment R3 by 1;
Y: SHR R1; Shift right R1 by 1 bit
JMP X; Jump to target X
Z:...
```

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- A. Initially $R1$, $R2$ and $R3$ contain the values 5,0 and 0 respectively, what are the final values of $R1$ and $R3$ when control reaches Z?
- B. In general, if $R1$, $R2$ and $R3$ initially contain the values n, 0, and 0 respectively. What is the final value of $R3$ when control reaches Z?

gate1999 co-and-architecture machine-instructions normal descriptive

Answer ↗

1.15.4 Machine Instructions: GATE CSE 2003 | Question: 48 top ↗

↗ <https://gateoverflow.in/938>



Consider the following assembly language program for a hypothetical processor A, B , and C are 8-bit registers. The meanings of various instructions are shown as comments.

```
MOV B, #0      ;          B ← 0
MOV C, #8      ;          C ← 8
Z:  CMP C, #0   ;          compare C with 0
     JZ X       ;          jump to X if zero flag is set
     SUB C, #1   ;          C ← C – 1
     RRC A, #1   ;          right rotate A through carry by one bit. Thus:
                         ; If the initial values of A and the carry flag are  $a_7 \dots a_0$  and
                         ;  $c_0$  respectively, their values after the execution of this
                         ; instruction will be  $c_0a_7 \dots a_1$  and  $a_0$  respectively.
     JC Y       ;          jump to Y if carry flag is set
tests.gatecse.in JMP Z   ;          jump to Z
Y:  ADD B, #1   ;          B ← B + 1
     JMP Z       ;          jump to Z
X:  ;
```

If the initial value of register A is A_0 the value of register B after the program execution will be

- A. the number of 0 bits in A_0
- B. the number of 1 bits in A_0
- C. A_0
- D. 8

gate2003-cse co-and-architecture machine-instructions normal

Answer ↗

1.15.5 Machine Instructions: GATE CSE 2003 | Question: 49 top ↗

↗ <https://gateoverflow.in/43577>



Consider the following assembly language program for a hypothetical processor A, B , and C are 8 bit registers. The meanings of various instructions are shown as comments.

```
MOV B, #0      ; B ← 0
MOV C, #8      ; C ← 8
Z:  CMP C, #0   ; compare C with 0
     JZ X       ; jump to X if zero flag is set
     SUB C, #1   ; C ← C – 1
     RRC A, #1   ; right rotate A through carry by one bit. Thus:
                         ; If the initial values of A and the carry flag are  $a_7 \dots a_0$  and
                         ;  $c_0$  respectively, their values after the execution of this
                         ; instruction will be  $c_0a_7 \dots a_1$  and  $a_0$  respectively.
     JC Y       ; jump to Y if carry flag is set
tests.gatecse.in JMP Z   ; jump to Z
Y:  ADD B, #1   ; B ← B + 1
     JMP Z       ; jump to Z
X:  ;
```

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X:

Which of the following instructions when inserted at location X will ensure that the value of the register A after program execution is as same as its initial value?

- A. RRC A, #1
- B. NOP; no operation
- C. LRC A, #1; left rotate A through carry flag by one bit
- D. ADD A, #1

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gate2003-cse co-and-architecture machine-instructions normal

Answer ↗

1.15.6 Machine Instructions: GATE CSE 2004 | Question: 63 [top](#)

↗ <https://gateoverflow.in/1058>



Consider the following program segment for a hypothetical CPU having three user registers R_1, R_2 and R_3 .

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Instruction	Operation	Instruction size (in words)
MOV $R_1, 5000$	$R_1 \leftarrow \text{Memory}[5000]$	2
MOV $R_2, (R_1)$	$R_2 \leftarrow \text{Memory}[(R_1)]$	1
ADD R_2, R_3	$R_2 \leftarrow R_2 + R_3$	1
MOV 6000, R_2	$\text{Memory}[6000] \leftarrow R_2$	2
HALT	Machine Halts	1

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Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address (in decimal) saved in the stack will be

- A. 1007
- B. 1020
- C. 1024
- D. 1028

gate2004-cse co-and-architecture machine-instructions normal

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Answer ↗

1.15.7 Machine Instructions: GATE CSE 2004 | Question: 64 [top](#)

↗ <https://gateoverflow.in/43570>



Consider the following program segment for a hypothetical CPU having three user registers R_1, R_2 and R_3 .

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Instruction	Operation	Instruction size (in Words)
MOV $R_1, 5000$	$R_1 \leftarrow \text{Memory}[5000]$	2
MOV $R_2, (R_1)$	$R_2 \leftarrow \text{Memory}[(R_1)]$	1
ADD R_2, R_3	$R_2 \leftarrow R_2 + R_3$	1
MOV 6000, R_2	$\text{Memory}[6000] \leftarrow R_2$	2
Halt	Machine Halts	1

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Let the clock cycles required for various operations be as follows:

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Register to/from memory transfer	3 clock cycles
ADD with both operands in register	1 clock cycles
Instruction fetch and decode	2 clock cycles

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The total number of clock cycles required to execute the program is

- A. 29
- B. 24
- C. 23
- D. 20

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Answer **1.15.8 Machine Instructions: GATE CSE 2006 | Question: 09, ISRO2009-35** top<https://gateoverflow.in/888>

A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

- A. 400
- B. 500
- C. 600
- D. 700

Answer **1.15.9 Machine Instructions: GATE CSE 2007 | Question: 54** top<https://gateoverflow.in/1252>

In a simplified computer the instructions are:

OP R_j, R_i	Perform $R_j \text{OP } R_i$ and store the result in register R_j
OP m, R_i	Perform $\text{val OP } R_i$ and store the result in register R_i val denotes the content of the memory location m
MOV m, R_i	Moves the content of memory location m to register R_i
MOV R_i, m	Moves the content of register R_i to memory location m

The computer has only two registers, and OP is either ADD or SUB. Consider the following basic block:

- $t_1 = a + b$
- $t_2 = c + d$
- $t_3 = e - t_2$
- $t_4 = t_1 - t_3$

Assume that all operands are initially in memory. The final value of the computation should be in memory. What is the minimum number of MOV instructions in the code generated for this basic block?

- A. 2
- B. 3
- C. 5
- D. 6

Answer **1.15.10 Machine Instructions: GATE CSE 2007 | Question: 71** top<https://gateoverflow.in/1269>

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	$R1 \leftarrow M[3000]$	2
LOOP:	MOV R2,(R3)	$R2 \leftarrow M[R3]$	1
	ADD R2,R1	$R2 \leftarrow R1 + R2$	1
	MOV (R3),R2	$M[R3] \leftarrow R2$	1
	INC R3	$R3 \leftarrow R3 + 1$	1
	DEC R1	$R1 \leftarrow R1 - 1$	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

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- A. 10
- B. 11
- C. 20
- D. 21

gate2007-cse co-and-architecture machine-instructions interrupts normal

Answer ↗

1.15.11 Machine Instructions: GATE CSE 2007 | Question: 72 top ↗

↗ <https://gateoverflow.in/43515>



Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	R1 ← M[3000]	2
LOOP:	MOV R2,(R3)	R2 ← M[R3]	1
	ADD R2,R1	R2 ← R1 + R2	1
	MOV (R3),R2	M[R3] ← R2	1
	INC R3	R3 ← R3 + 1	1
	DEC R1	R1 ← R1 - 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is:

- A. 100
- B. 101
- C. 102
- D. 110

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Answer ↗

1.15.12 Machine Instructions: GATE CSE 2007 | Question: 73 top ↗

↗ <https://gateoverflow.in/43516>



Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	R1 ← M[3000]	2
LOOP:	MOV R2,(R3)	R2 ← M[R3]	1
	ADD R2,R1	R2 ← R1 + R2	1
	MOV (R3),R2	M[R3] ← R2	1
	INC R3	R3 ← R3 + 1	1
	DEC R1	R1 ← R1 - 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

decimal.

Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction “INC R3”, what return address will be pushed on to the stack?

- A. 1005
- B. 1020
- C. 1024
- D. 1040

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Answer 

1.15.13 Machine Instructions: GATE CSE 2008 | Question: 34 top ↴

<https://gateoverflow.in/445>



Which of the following must be true for the RFE (Return From Exception) instruction on a general purpose processor?

- I. It must be a trap instruction
 - II. It must be a privileged instruction
 - III. An exception cannot be allowed to occur during execution of an RFE instruction
-
- A. I only
 - B. II only
 - C. I and II only
 - D. I, II and III only

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gate2008-cse co-and-architecture machine-instructions normal

Answer 

1.15.14 Machine Instructions: GATE CSE 2015 Set 2 | Question: 42 top ↴

<https://gateoverflow.in/8215>



Consider a processor with byte-addressable memory. Assume that all registers, including program counter (PC) and Program Status Word (PSW), are size of two bytes. A stack in the main memory is implemented from memory location $(0100)_{16}$ and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is $(016E)_{16}$. The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

- Store the current value of PC in the stack
- Store the value of PSW register in the stack
- Load the starting address of the subroutine in PC

The content of PC just before the fetch of a CALL instruction is $(5FA0)_{16}$. After execution of the CALL instruction, the value of the stack pointer is:

- A. $(016A)_{16}$
- B. $(016C)_{16}$
- C. $(0170)_{16}$
- D. $(0172)_{16}$

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gate2015-cse-set2 co-and-architecture machine-instructions easy

Answer 

1.15.15 Machine Instructions: GATE CSE 2016 Set 2 | Question: 10 top ↴

<https://gateoverflow.in/39547>



A processor has 40 distinct instruction and 24 general purpose registers. A 32-bit instruction word has an opcode, two registers operands and an immediate operand. The number of bits available for the immediate operand field is _____.

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Answer 



Consider the following instruction sequence where registers R1, R2 and R3 are general purpose and $\text{MEMORY}[X]$ denotes the content at the memory location X.

Instruction	Semantics	Instruction Size (bytes)
MOV R1, (5000)	$R1 \leftarrow \text{MEMORY}[5000]$	4
MOV R2, (R3)	$R2 \leftarrow \text{MEMORY}[R3]$	4
ADDR2, R1	$R2 \leftarrow R1 + R2$	2
MOV (R3), R2	$\text{MEMORY}[R3] \leftarrow R2$	4
INC R3	$R3 \leftarrow R3 + 1$	2
DEC R1	$R1 \leftarrow R1 - 1$	2
BNZ 1004	Branch if not zero to the given absolute address	2
HALT	Stop	1

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Assume that the content of the memory location 5000 is 10, and the content of the register R3 is 3000. The content of each of the memory locations from 3000 to 3020 is 50. The instruction sequence starts from the memory location 1000. All the numbers are in decimal format. Assume that the memory is byte addressable.

After the execution of the program, the content of memory location 3010 is _____

[gate2021-cse-set1](#) [co-and-architecture](#) [machine-instructions](#) [numerical-answers](#)

Answer



If we use internal data forwarding to speed up the performance of a CPU (R1, R2 and R3 are registers and $M[100]$ is a memory reference), then the sequence of operations

$$\begin{aligned} R1 &\rightarrow M[100] \\ M[100] &\rightarrow R2 \\ M[100] &\rightarrow R3 \end{aligned}$$

can be replaced by

- A. $R1 \rightarrow R3$
 $R2 \rightarrow M[100]$
- B. $M[100] \rightarrow R2$
 $R1 \rightarrow R2$
 $R1 \rightarrow R3$
- C. $R1 \rightarrow M[100]$
 $R2 \rightarrow R3$
- D. $R1 \rightarrow R2$
 $R1 \rightarrow R3$
 $R1 \rightarrow M[100]$

[gate2004-it](#) [co-and-architecture](#) [machine-instructions](#) [easy](#)

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Answer



Following table indicates the latencies of operations between the instruction producing the result and instruction using the result.

Instruction producing the result	Instruction using the result	Latency
ALU Operation	ALU Operation	2
ALU Operation	Store	2
Load	ALU Operation	1
Load	Store	0

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Consider the following code segment:

```
Load R1, Loc 1; Load R1 from memory location Loc1
```

```

Load R2, Loc 2; Load R2 from memory location Loc 2
Add R1, R2, R1; Add R1 and R2 and save result in R1
Dec R2;
Dec R1;
Mpy R1, R2, R3; Multiply R1 and R2 and save result in R3
Store R3, Loc 3; Store R3 in memory location Loc 3

```

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What is the number of cycles needed to execute the above code segment assuming each instruction takes one cycle to execute?

- A. 7
- B. 10
- C. 13
- D. 14

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Answer 

1.15.19 Machine Instructions: GATE IT 2008 | Question: 38 top ↗

<https://gateoverflow.in/3348>



Assume that $EA = (X)^+$ is the effective address equal to the contents of location X, with X incremented by one word length after the effective address is calculated; $EA = -(X)$ is the effective address equal to the contents of location X, with X decremented by one word length before the effective address is calculated; $EA = (X)^-$ is the effective address equal to the contents of location X, with X decremented by one word length after the effective address is calculated. The format of the instruction is (opcode, source, destination), which means (destination \leftarrow source op destination). Using X as a stack pointer, which of the following instructions can pop the top two elements from the stack, perform the addition operation and push the result back to the stack.

- A. ADD $(X)^-, (X)$
- B. ADD $(X), (X)^-$
- C. ADD $-(X), (X)^+$
- D. ADD $-(X), (X)$

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Answer 

Answers: Machine Instructions

1.15.1 Machine Instructions: GATE CSE 1988 | Question: 9i top ↗

<https://gateoverflow.in/94384>



✓ $Z = [BC + A]^2 + (BC)$

12 votes

-- Yash wadhwani (831 points)

1.15.2 Machine Instructions: GATE CSE 1994 | Question: 12 top ↗

<https://gateoverflow.in/2508>



- $R_1 \leftarrow R_1 \text{ XOR } R_2$
- $R_2 \leftarrow R_2 \text{ XOR } R_1$
- $R_1 \leftarrow R_1 \text{ XOR } R_2$

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Stuck at 0 fault: A stuck-at fault is a particular fault model used by fault simulators and automatic test pattern generation (ATPG) tools to mimic a manufacturing defect within an integrated circuit. Individual signals and pins are assumed to be stuck at Logical '1', '0', and 'X'.

Stuck at line 1 means no matter whatever input we provide to the line the output is always 1.

Now, when we take $A = 1, B = 1, C = 1$ the required output, if no fault is there should be 1.

But, since line p is stuck at logic 1 final output of $A \text{ NAND } B$ will be 1 only. So, final circuit output becomes 0. (which is wrong)

Reference : https://www.tutorialspoint.com/digital_electronics/stuckat1_fault_in_logic_circuit.asp

References

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20 votes

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-- Vidhi Sethi (8.3k points)

1.15.3 Machine Instructions: GATE CSE 1999 | Question: 17<https://gateoverflow.in/1516>

- ✓ SHR R1 (Lower bit is lost and upper bit becomes 0 and all other bits shift right by 1)
SHL R1 (Upper bit is lost and lower bit becomes 0 and all other bits shift left by 1)

These two operations change the value of $R1$ if its lower bit is 1. So, the given program checks the lowest bit of $R1$ in each iteration and if its 1 then only increment $R3$ and loop terminates when $R1$ becomes 0. Thus at end, $R3$ will have the count of the number of bits set to 1 in $R1$.

- $R1 = 0, R3 = 2$ as 101 has two 1's
- $R3 = \#1$ in $R1$.

27 votes

-- Arjun Suresh (332k points)

1.15.4 Machine Instructions: GATE CSE 2003 | Question: 48<https://gateoverflow.in/938>

- ✓ Option (B). The code is counting the number of 1 bits in A_0 . When a 1 is moved to carry, B is incremented.

30 votes

-- Arjun Suresh (332k points)

1.15.5 Machine Instructions: GATE CSE 2003 | Question: 49<https://gateoverflow.in/43577>

- ✓ Option (A) RRC $a, \#1$. As the 8 bit register is rotated via carry 8 times.

- $a_7a_6a_5a_4a_3a_2a_1a_0$
- $c_0a_7a_6a_5a_4a_3a_2a_1$, now a_0 is the new carry. So, after next rotation,
- $a_0c_0a_7a_6a_5a_4a_3a_2$

So, after 8 rotations, $a_6a_5a_4a_3a_2a_1a_0c_0$ and carry is a_7 .

Now, one more rotation will restore the original value of A_0 .

43 votes

-- Arjun Suresh (332k points)

1.15.6 Machine Instructions: GATE CSE 2004 | Question: 63<https://gateoverflow.in/1058>

- ✓ Option is D.

Word size is 32 bits (4 bytes). Interrupt occurs **after execution of HALT** instruction NOT **during**. So address of next instruction will be saved on to the stack which is 1028.

(We have 5 instructions starting from address 1000, each of size 2, 1, 1, 2, 1 totaling 7 words = $7 * 4 = 28$ bytes).

1000 + 28 = 1028

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1028 is the starting address of NEXT Instruction .

After HALT instruction CPU enters a HALT state and if an interrupt happens the return address will be **that of the instruction after the HALT**.

References :

1. https://x86.puri.sm/html/file_module_x86_id_134.html [X86 Instructors Manual]
2. <http://electronics.stackexchange.com/questions/277735/what-happens-if-the-interrupt-occurs-during-the-execution-of-halt-instruction>
3. [https://en.wikipedia.org/wiki/HLT_\(x86_instruction\)](https://en.wikipedia.org/wiki/HLT_(x86_instruction))

References



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👍 85 votes

-- Vikrant Singh (11.2k points)

1.15.7 Machine Instructions: GATE CSE 2004 | Question: 64 top ↗

↗ <https://gateoverflow.in/43570>



- ✓ B. 24 cycles

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Instruction	Size	Fetch and Decode + Execute
MOV	2	$2 \times 2 + 3 = 7$
MOV	1	$2 \times 1 + 3 = 5$
ADD	1	$2 \times 1 + 1 = 3$
MOV	2	$2 \times 2 + 3 = 7$
HALT	1	$2 \times 1 + 0 = 2$
Total		24 Cycles

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👍 107 votes

-- Vikrant Singh (11.2k points)

1.15.8 Machine Instructions: GATE CSE 2006 | Question: 09, ISRO2009-35 top ↗

↗ <https://gateoverflow.in/888>



- ✓ Option (C). 24 bits = 3 bytes instructions. So, PC will have multiples of 3 in it.

👍 40 votes

-- anshu (2.7k points)

1.15.9 Machine Instructions: GATE CSE 2007 | Question: 54 top ↗

↗ <https://gateoverflow.in/1269>



- MOV a, R_1
- ADD b, R_1
- MOV c, R_2
- ADD d, R_2
- SUB e, R_2
- SUB R_1, R_2
- MOV R_2, m

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Total number of MOV instructions = 3

Correct Answer: B

👍 75 votes

-- Gate Keeda (15.9k points)

1.15.10 Machine Instructions: GATE CSE 2007 | Question: 71 top ↗

↗ <https://gateoverflow.in/1269>



- ✓ Loop is executed 10 times and there are two memory reference in the loop (each MOV is loading 1 word, so 1 memory reference for each MOV inside the loop). So number of memory reference inside loop is

$2(\text{MOV}) \times 10 (\text{times iteration}) \times 1(\text{1 word access/ MOV}) = 20 \text{ memory accesses.}$

One memory access is outside the loop for the first instruction

MOV R1, (3000)

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So, totally $20 + 1 = 21$

Correct Answer: D

45 votes

-- Vicky Bajoria (4.1k points)

1.15.11 Machine Instructions: GATE CSE 2007 | Question: 72 [top](#)

<https://gateoverflow.in/43515>



- ✓ The loop runs 10 times.

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1. When $R1 = 10$, $\text{Memory}[2000] = 110$,
2. When $R1 = 9$, $\text{Memory}[2001] = 109$,
3. When $R1 = 8$, $\text{Memory}[2002] = 108$,
4. When $R1 = 7$, $\text{Memory}[2003] = 107$,
5. When $R1 = 6$, $\text{Memory}[2004] = 106$,
6. When $R1 = 5$, $\text{Memory}[2005] = 105$,
7. When $R1 = 4$, $\text{Memory}[2006] = 104$,
8. When $R1 = 3$, $\text{Memory}[2007] = 103$,
9. When $R1 = 2$, $\text{Memory}[2008] = 102$,
10. When $R1 = 1$, $\text{Memory}[2009] = 101$,

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When $R1 = 0$ the loop breaks., $\text{Memory}[2010] = 100$

Correct Answer: A

54 votes

-- Arnab Bhadra (3.7k points)

1.15.12 Machine Instructions: GATE CSE 2007 | Question: 73 [top](#)

<https://gateoverflow.in/43516>



- ✓ An interrupt is checked for after the execution of the current instruction and the contents of PC (address of next instruction to be executed) is pushed on to stack.

Here, address of INC, $R3 = 1000 + \frac{(2+1+1+1) \times 32}{8} = 1020$ and

next instruction address = $1020 + 4 = 1024$ which is pushed on to stack.

Reference: http://www.ece.utep.edu/courses/web3376/Notes_files/ee3376-interrupts_stack.pdf

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Correct Answer: C

References



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38 votes

-- Vicky Bajoria (4.1k points)

1.15.13 Machine Instructions: GATE CSE 2008 | Question: 34 [top](#)

<https://gateoverflow.in/445>



- ✓ RFE (Return From Exception) is a privileged trap instruction that is executed when exception occurs, so an exception is not allowed to execute. (D) is the correct option.

Reference: http://www.cs.rochester.edu/courses/252/spring2014/notes/08_exceptions

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References



28 votes

-- Vikrant Singh (11.2k points)

1.15.14 Machine Instructions: GATE CSE 2015 Set 2 | Question: 42 [top](#)

<https://gateoverflow.in/8215>

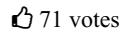


- ✓ First we have to consider here memory is byte-addressable

The CALL instruction is implemented as follows:

- Store the current value of PC in the stack
PC is 2 bytes it means when we store pc in stack it will increase by 2
So current value of SP is $(016E)_{16} + 2$
- Store the value of PSW register in the stack
PSW is 2 byte it means when we store psw in stack it will increase by 2
So current value of SP is $(016E)_{16} + 2 + 2 = (0172)_{16}$

Correct Answer: D



71 votes

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-- Anoop Sonkar (4.1k points)

1.15.15 Machine Instructions: GATE CSE 2016 Set 2 | Question: 10 top

<https://gateoverflow.in/39547>



- ✓ Instruction Opcode Size = $\log_2 40 = 6$

Register operand size = $\log_2 24 = 5$

Total bits available = 32

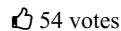
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Bits required for opcode + two register operands = $6 + 2 \times 5 = 16$

Bits available for immediate operand = $32 - 16 = 16$.



54 votes

-- Akash Kanase (36k points)

1.15.16 Machine Instructions: GATE CSE 2021 Set 1 | Question: 55 top

<https://gateoverflow.in/35739>



- ✓ The given code is iterating 10 times and incrementing the contents of locations 3000 to $3000 + i$ by $10 - i$, for $i < 10$. Location 3010 is left untouched.

So, correct answer: 50.



7 votes

-- Arjun Suresh (332k points)

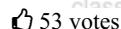
1.15.17 Machine Instructions: GATE IT 2004 | Question: 46 top

<https://gateoverflow.in/3689>



- ✓ Data forwarding means if CPU writes to a memory location and subsequently reads from the same memory location, the second instruction can fetch the value directly from the register used to do the write than waiting for the memory. So, this increases the performance.

Here, choices A, B and C doesn't really make any sense as the data was in R1 and it must be moved to R2, R3 and M[100]. So, (D) is the answer.



53 votes

-- Arjun Suresh (332k points)

1.15.18 Machine Instructions: GATE IT 2007 | Question: 41 top

<https://gateoverflow.in/3476>



- ✓ In the given question there are 7 instructions each of which takes 1 clock cycle to complete. (Pipelining may be used) If an instruction is in execution phase and any other instructions can not be in the execution phase. So, at least 7 clock cycles will be taken.

Now, it is given that between two instructions latency or delay should be there based on their operation. Ex- 1st line of the table says that between two operations in which first is producing the result of an ALU operation and the 2nd is using the result there should be a delay of 2 clock cycles.

Clock cycle	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
	I1	I2		I3	I4		I5			I6			I7

1. Load R1, Loc 1; Load R1 from memory location Loc1
Takes 1 clock cycle, simply loading R1 on loc1.

2. Load R2, Loc 2; Load R2 from memory location Loc2

Takes 1 clock cycle, simply loading r2 on loc2.

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3. (Add R1, R2, R1; Add R1 and R2 and save result in R1

$$R1=R1+R2;$$

Hence, this instruction is using the result of R1 and R2, i.e. result of Instruction 1 and Instruction 2.

As instruction 1 is load operation and instruction 3 is ALU operation. So, there should be a delay of 1 clock cycle between instruction 1 and instruction 3, which is already there due to I2.

As instruction 2 is load operation and instruction 3 is ALU operation. So, there should be a delay of 1 clock cycle between instruction 2 and instruction 3.

4. Dec R2; Decrement R2

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This instruction is dependent on instruction 2 and there should be a delay of one clock cycle between Instruction 2 and Instruction 4. As instruction 2 is load and 4 is ALU, which is already there due to Instruction 3.

5. Dec R1 Decrement R1

This instruction is dependent on Instruction 3

As Instruction I3 is ALU and I5 is also ALU so a delay of 2 clock cycles should be there between them of which 1 clock cycle delay is already there due to I4 so one clock cycle delay between I4 and I5.

6. MPY R1, R2, R3; Multiply R1 and R2 and save result in R3

$$R3=R1*R2;$$

This instruction uses the result of Instruction 5, as both instruction 5 and 6 are ALU so there should be a delay of 2 clock cycles.

7. Store R3, Loc 3 Store R3 in memory location Loc3

This instruction is dependent on instruction 6 which is ALU and instruction 7 is store so there should be a delay of 2 clock cycles between them.

Hence, a total of 13 clock cycles will be there.

Correct Answer: C

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146 votes

-- Madhab Paul Choudhury (2.8k points)

1.15.19 Machine Instructions: GATE IT 2008 | Question: 38 top

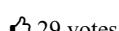
<https://gateoverflow.in/3348>



It should be A as $998 \leftarrow 1000 + 998$. (I am writing only memory locations for sake of brevity)

Lets say SP is 1000 initially then after it calculates the EA of source (which is 1000 as it decrements after the EA) the destination becomes 998 and that is where we want to store the result as stack is decrementing.

In case of C and D it becomes $998 \leftarrow 998 + 998$.



-- Shaun Patel (6.1k points)

1.16

Memory Interfacing (2) top

1.16.1 Memory Interfacing: GATE CSE 2016 Set 1 | Question: 09 top

<https://gateoverflow.in/39632>



A processor can support a maximum memory of $4GB$, where the memory is word-addressable (a word consists of two bytes). The size of address bus of the processor is at least _____ bits.

gate2016-cse-set1 co-and-architecture easy numerical-answers memory-interfacing

Answer

1.16.2 Memory Interfacing: GATE CSE 2018 | Question: 23 top

<https://gateoverflow.in/204097>



A $32-bit$ wide main memory unit with a capacity of $1 GB$ is built using $256 M \times 4-bit$ DRAM chips. The number of rows of memory cells in the DRAM chip is 2^{14} . The time taken to perform one refresh operation is 50 nanoseconds . The refresh period is 2 milliseconds. The percentage (rounded to the closest integer) of the time available for performing the memory read/write operations in the main memory unit is _____.

gate2018-cse co-and-architecture memory-interfacing normal numerical-answers

Answer

Answers: Memory Interfacing

1.16.1 Memory Interfacing: GATE CSE 2016 Set 1 | Question: 09 [top](#)

<https://gateoverflow.in/39632>



- ✓ Size of Memory = No of words (Addresses) \times No of bits per word

$$2^{32}B \equiv \text{No of words (Addresses)} \times 2B$$

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$$\text{No of words (Addresses)} = 2^{31}$$

$$\text{Number of Address lines} = 31$$

Like 54 votes

-- Praveen Saini (41.9k points)

1.16.2 Memory Interfacing: GATE CSE 2018 | Question: 23 [top](#)

<https://gateoverflow.in/204097>



- ✓ One refresh operation takes 50ns.

$$\text{Total number of rows} = 2^{14}$$

$$\text{Total time to refresh all Rows} = 2^{14} \times 50 \text{ ns} = 819200 \text{ ns} = 0.819200 \text{ ms}$$

The Refresh Period is 2ms.

$$\% \text{ Time spent in refresh} = \frac{\text{Total time to Refresh all Rows}}{\text{Refresh period}} * 100 \\ = \frac{0.8192ms}{2.0ms} * 100 = 40.96\%$$

$$\% \text{ Time spent in Read/Write} = 100 - 40.96 = 59.04\%$$

= 59% (Rounded to the closest Integer)

Reference: https://en.wikipedia.org/wiki/Memory_refresh

References



Like 86 votes

-- Digvijay (44.9k points)

1.17

Microporgramming (12) [top](#)

1.17.1 Microporgramming: GATE CSE 1987 | Question: 4a [top](#)

<https://gateoverflow.in/81359>



Find out the width of the control memory of a horizontal microporgrammed control unit, given the following specifications:

- 16 control lines for the processor consisting of ALU and 7 registers.
- Conditional branching facility by checking 4 status bits.
- Provision to hold 128 words in the control memory.

gate1987 co-and-architecture microporgramming descriptive

Answer

1.17.2 Microporgramming: GATE CSE 1996 | Question: 2.25 [top](#)

<https://gateoverflow.in/2754>



A micro program control unit is required to generate a total of 25 control signals. Assume that during any micro instruction, at most two control signals are active. Minimum number of bits required in the control word to generate the required control signals will be:

- A. 2
- B. 2.5
- C. 10
- D. 12

gate1996 co-and-architecture microporgramming normal

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Answer 

1.17.3 Microprogramming: GATE CSE 1997 | Question: 5.3 [top](#) <https://gateoverflow.in/2254>



A micro instruction is to be designed to specify:

- a. none or one of the three micro operations of one kind and
- b. none or upto six micro operations of another kind

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The minimum number of bits in the micro-instruction is:

- A. 9
- B. 5
- C. 8
- D. None of the above

[gate1997](https://gate1997.gateoverflow.in) [co-and-architecture](https://co-and-architecture.gateoverflow.in) [microporogramming](https://microporogramming.gateoverflow.in) [normal](https://normal.gateoverflow.in)

Answer 

1.17.4 Microprogramming: GATE CSE 1999 | Question: 2.19 [top](#) <https://gateoverflow.in/1497>



Arrange the following configuration for CPU in decreasing order of operating speeds:

Hard wired control, Vertical microprogramming, Horizontal microprogramming.

- A. Hard wired control, Vertical microprogramming, Horizontal microprogramming.
- B. Hard wired control, Horizontal microprogramming, Vertical microprogramming.
- C. Horizontal microprogramming, Vertical microprogramming, Hard wired control.
- D. Vertical microprogramming, Horizontal microprogramming, Hard wired control.

[gate1999](https://gate1999.gateoverflow.in) [co-and-architecture](https://co-and-architecture.gateoverflow.in) [microporogramming](https://microporogramming.gateoverflow.in) [normal](https://normal.gateoverflow.in)

Answer 

1.17.5 Microprogramming: GATE CSE 2002 | Question: 2.7 [top](#) <https://gateoverflow.in/837>



Horizontal microprogramming:

- A. does not require use of signal decoders
- B. results in larger sized microinstructions than vertical microprogramming
- C. uses one bit for each control signal
- D. all of the above

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[gate2002-cse](https://gate2002-cse.gateoverflow.in) [co-and-architecture](https://co-and-architecture.gateoverflow.in) [microporogramming](https://microporogramming.gateoverflow.in)

Answer 

1.17.6 Microprogramming: GATE CSE 2004 | Question: 67 [top](#) <https://gateoverflow.in/1061>

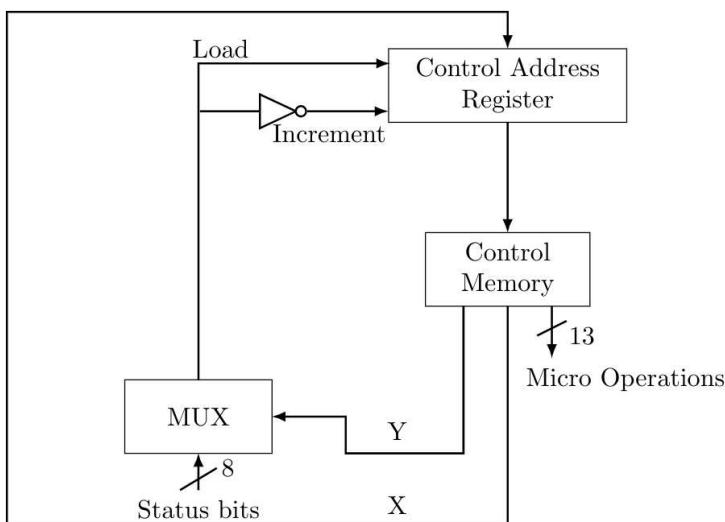


The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the input of the MUX.

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How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?

- A. 10, 3, 1024
- B. 8, 5, 256
- C. 5, 8, 2048
- D. 10, 3, 512

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gate2004-cse co-and-architecture microprogramming normal

Answer

1.17.7 Microprogramming: GATE CSE 2013 | Question: 28 top ↺

<https://gateoverflow.in/1539>



Consider the following sequence of micro-operations.

MBR ← PC MAR ← X PC ← Y Memory → MBR

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Which one of the following is a possible operation performed by this sequence?

- A. Instruction fetch
- B. Operand fetch
- C. Conditional branch
- D. Initiation of interrupt service

gate2013-cse co-and-architecture microprogramming normal

Answer

1.17.8 Microprogramming: GATE IT 2004 | Question: 49 top ↺

<https://gateoverflow.in/3692>



A CPU has only three instructions I_1 , I_2 and I_3 , which use the following signals in time steps $T_1 - T_5$:

$I_1 : T_1 : \text{Ain}, \text{Bout}, \text{Cin}$
 $T_2 : \text{PCout}, \text{Bin}$
 $T_3 : \text{Zout}, \text{Ain}$
 $T_4 : \text{Bin}, \text{Cout}$
 $T_5 : \text{End}$

$I_2 : T_1 : \text{Cin}, \text{Bout}, \text{Din}$
 $T_2 : \text{Aout}, \text{Bin}$
 $T_3 : \text{Zout}, \text{Ain}$
 $T_4 : \text{Bin}, \text{Cout}$
 $T_5 : \text{End}$

$I_3 : T_1 : \text{Din}, \text{Aout}$
 $T_2 : \text{Ain}, \text{Bout}$
 $T_3 : \text{Zout}, \text{Ain}$
 $T_4 : \text{Dout}, \text{Ain}$

T5 : End

Which of the following logic functions will generate the hardwired control for the signal Ain ?

- A. $T1.I1 + T2.I3 + T4.I3 + T3$
- B. $(T1 + T2 + T3).I3 + T1.I1$
- C. $(T1 + T2).I1 + (T2 + T4).I3 + T3$
- D. $(T1 + T2).I2 + (T1 + T3).I1 + T3$

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gate2004-it co-and-architecture microporogramming normal

Answer ↗

1.17.9 Microprogramming: GATE IT 2005 | Question: 45 [top](#)

▪ <https://gateoverflow.in/3806>



A hardwired CPU uses 10 control signals S_1 to S_{10} , in various time steps T_1 to T_5 , to implement 4 instructions I_1 to I_4 as shown below:

	T₁	T₂	T₃	T₄	T₅
I₁	S_1, S_3, S_5	S_2, S_4, S_6	S_1, S_7	S_{10}	S_3, S_8
I₂	S_1, S_3, S_5	S_8, S_9, S_{10}	S_5, S_6, S_7	S_6	S_{10}
I₃	S_1, S_3, S_5	S_7, S_8, S_{10}	S_2, S_6, S_9	S_{10}	S_1, S_3
I₄	S_1, S_3, S_5	S_2, S_6, S_7	S_5, S_{10}	S_6, S_9	S_{10}

Which of the following pairs of expressions represent the circuit for generating control signals S_5 and S_{10} respectively?

(($I_j + I_k$) T_n) indicates that the control signal should be generated in time step T_n if the instruction being executed is I_j or I_k)

- A. $S_5 = T_1 + I_2 \cdot T_3$ and
 $S_{10} = (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$
- B. $S_5 = T_1 + (I_2 + I_4) \cdot T_3$ and
 $S_{10} = (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$
- C. $S_5 = T_1 + (I_2 + I_4) \cdot T_3$ and
 $S_{10} = (I_2 + I_3 + I_4) \cdot T_2 + (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$
- D. $S_5 = T_1 + (I_2 + I_4) \cdot T_3$ and
 $S_{10} = (I_2 + I_3) \cdot T_2 + I_4 \cdot T_3 + (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$

gate2005-it co-and-architecture microporogramming normal

Answer ↗

1.17.10 Microprogramming: GATE IT 2005 | Question: 49 [top](#)

▪ <https://gateoverflow.in/3810>



An instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows:

Group 1 : 20 signals, Group 2 : 70 signals, Group 3 : 2 signals, Group 4 : 10 signals, Group 5 : 23 signals.

How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming?

- A. 0
- B. 103
- C. 22
- D. 55

gate2005-it co-and-architecture microporogramming normal

Answer ↗

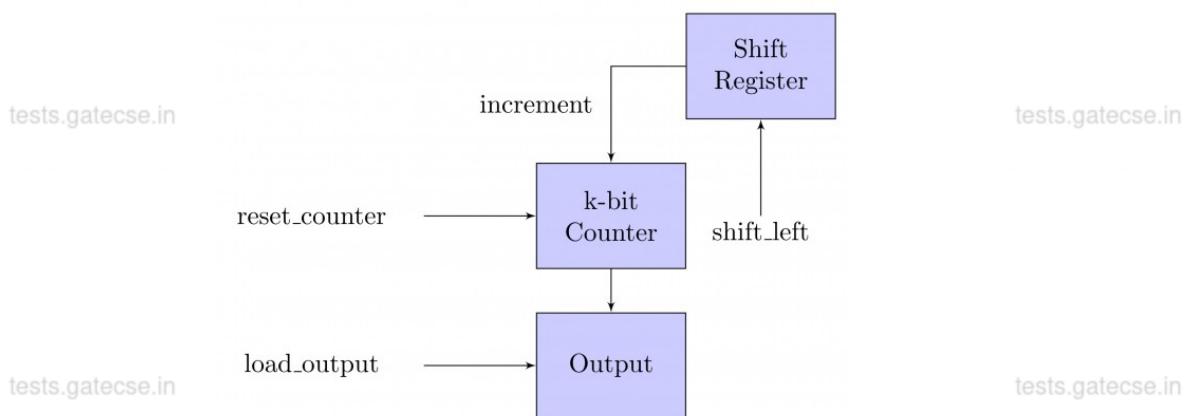
1.17.11 Microprogramming: GATE IT 2006 | Question: 41 [top](#)

▪ <https://gateoverflow.in/3584>



The data path shown in the figure computes the number of 1s in the 32-bit input word corresponding to an unsigned even integer stored in the shift register.

The unsigned counter, initially zero, is incremented if the most significant bit of the shift register is 1.



The microprogram for the control is shown in the table below with missing control words for microinstructions I_1, I_2, \dots, I_n .

Microinstruction	Reset_Counter	Shift_left	Load_output
BEGIN	1	0	0
I1	?	?	?
:	:	:	:
In	?	?	?
END	0	0	1

The counter width (k), the number of missing microinstructions (n), and the control word for microinstructions I_1, I_2, \dots, I_n are, respectively,

- A. 32, 5, 010
- B. 5, 32, 010
- C. 5, 31, 011
- D. 5, 31, 010

gate2006-it co-and-architecture microporgramming normal

Answer

1.17.12 Microporgramming: GATE IT 2008 | Question: 39 top ↺

<https://gateoverflow.in/3349>



Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125 control signals are needed to be generated by the control unit. While designing the horizontal microporgrammed control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?

- A. 125, 7
- B. 125, 10
- C. 135, 9
- D. 135, 10

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gate2008-it co-and-architecture microporgramming normal

Answer

Answers: Microporgramming

1.17.1 Microporgramming: GATE CSE 1987 | Question: 4a top ↺

<https://gateoverflow.in/81359>



Width of the control memory = size of a control word

- Control word = [Condition bits + control signal bits + next address]
- Condition bits = 4 $\implies \log_2 4$ -bits
- 128 words $\implies 7$ -bits for address.

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In the case of horizontal micro-programming, there is 1-bit for each control signal. It is given there are 16 control signals.

\Rightarrow Length of control word = $2 + 16 + 7 = 25$ - bits.

18 votes

-- agoh (1.2k points)

1.17.2 Microprogramming: GATE CSE 1996 | Question: 2.25 [top](#)

<https://gateoverflow.in/2754>



- ✓ The best sense I can make of this question is that you want to transmit up to 2 simultaneous signals out of a choice of 25, and ask how many bits you need for that.

One solution would be to have 2 groups of 5 - bits, each can send one of 31 signals (or the absence of signal). But it is not optimal. The number of different states is

$$1(\text{no signal}) + 25(\text{one signal}) + (25 \times 24/2)(\text{two signals}) = 326 \text{ states.}$$

You can transmit any of these states over 9 - bits. But it is more complex to encode/ decode, adding an extra bit would probably cost less.

Hence C is correct option.

Reference: https://www.ocf.berkeley.edu/~wwu/cgi-bin/yabb/YaBB.cgi?board=riddles_cs;action=display;num=1354778770

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30 votes

-- vnc (2.1k points)

1.17.3 Microprogramming: GATE CSE 1997 | Question: 5.3 [top](#)

<https://gateoverflow.in/2254>



- ✓ Actually the given question incorporates the concept of horizontal microprogramming (also known as decoded form of control signals) and vertical microprogramming (also known as encoded form of control signals)

The (a) part says :

none or one of the three micro operations of one kind

This is referred to encoding form of vertical one since at most one signal can be active in vertical microprogramming since it involves use of external decoder to select one control signal out of the given control signals..

No of bits required for vertical microprogramming given n number of control signals = $\lceil (\log_2 n) \rceil$

Here, $n = 3$

So, no of bits required for part (a) = $\lceil (\log_2 3) \rceil = 2$

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Now coming to (b) part , it says :

none or upto six micro operations of another kind

at maximum we can have at most 6 microoperations of another kind at a time. To accommodate that we need decoded form of control signals which is horizontal signals.

So, no of bits required for (b) part

= No of control signals of (b) kind = 6

Therefore overall bits required to accommodate both (a) and (b),
 $= 2 + 6 = 8$ - bits

Besides this, address field, flags etc are also there in a control word. That is why it is asked in the question :

minimum number of bits in the micro-instruction required

Hence, minimum no of bits required = $8 - bits$

C is the correct answer.

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Like 60 votes

-- HABIB MOHAMMAD KHAN (67.5k points)

1.17.4 Microprogramming: GATE CSE 1999 | Question: 2.19 top

<https://gateoverflow.in/1497>



- ✓ Hard wired control involves only hardware, whereas microprogramming is software approach. So, hardwire control should be faster than both microprogramming approaches.

Between vertical and horizontal microprogramming. Horizontal is faster because in this control signals are not encoded whereas in vertical microprogramming to save memory signals are encoded. So, it takes less time in horizontal microprogramming because decoding of signals is not required. Therefore, final order is :

hard wired control > horizontal microprogramming > vertical microprogramming

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Correct Answer: B

Like 33 votes

-- Shikhar Vashishth (3.1k points)

1.17.5 Microprogramming: GATE CSE 2002 | Question: 2.7 top

<https://gateoverflow.in/837>



- ✓ Option (D). All statements are true.

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Reference: <http://www.cs.virginia.edu/~cs333/notes/microprogramming.pdf>

References



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Like 27 votes

-- Suvojit Mondal (291 points)

1.17.6 Microprogramming: GATE CSE 2004 | Question: 67 top

<https://gateoverflow.in/1061>



- ✓ $x + y + 13 = 26 \rightarrow (1)$
 $y = 3$ (y) is no of bits used to represent 8 different states of multiplexer $\rightarrow (2)$
 x is no of bits required represent size of control memory
 $x = 10$ from (1) and (2)

\therefore Size of control memory = $2^x = 2^{10} = 1024$

Correct Answer: A

Like 48 votes

-- Digvijay (44.9k points)

1.17.7 Microprogramming: GATE CSE 2013 | Question: 28 top

<https://gateoverflow.in/1539>



- ✓ Here PC value is being stored in memory which is done when either CALL RETURN involved or there is Interrupt. As, we will have to come back to execute current instruction.

So, options (A), (B) are clearly incorrect.

Option (C) is incorrect because conditional branch does not require to save PC contents.

Option (D) is correct as it matches the generic Interrupt Cycle :

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Interrupt Cycle:

- t_1 : MBR \leftarrow (PC)
 t_2 : MAR \leftarrow (save-address)
 PC \leftarrow (routine-address)
 t_3 : Memory \leftarrow (MBR)

52 votes

-- Himanshu Agarwal (12.4k points)

1.17.8 Microprogramming: GATE IT 2004 | Question: 49 [top](#)

<https://gateoverflow.in/3692>



- ✓ We just have to see which all options give 1 whenever A_{in} is 1 and 0 otherwise.

So, A_{in} is 1 in $T3$ of $I1$, $I2$ and $I3$. Also during $T1$ of $I1$, and $T2$ and $T4$ of $I3$. So, answer will be

$$T1.I1 + T2.I3 + T4.I3 + T3.I1 + T3.I2 + T3.I3$$

Since CPU is having only 3 instructions, $T3.I1 + T3.I2 + T3.I3$ can be replaced with $T3$ (we don't need to see which instruction and A_{in} will be activated in time step 3 of all the instructions).

$$\text{So, } T1.I1 + T2.I3 + T4.I3 + T3$$

The answer is Option (A).

46 votes

-- Arjun Suresh (332k points)

1.17.9 Microprogramming: GATE IT 2005 | Question: 45 [top](#)

<https://gateoverflow.in/3806>



- ✓ D. is the correct option for this question.

If we look at the table, we need to find those time-stamps and instructions which are using these control signals.

For example, $S_5 = T_1$ has used control signal S_5 for all the instructions, or we can say irrespective of the instructions. Also, S_5 is used by instructions I_2 and I_4 for the time stamp T_3 so that comes to:

$$S_5 = T_1 + I_2 \cdot T_3 + I_4 \cdot T_3 = T_1 + (I_2 + I_4) \cdot T_3$$

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In the same way, we'll calculate for S_{10} .

It's an example of Hardwired CU Programming used in RISC processors. It gives accurate result, but isn't good for debugging since minor change will cause to restructure the control unit.

31 votes

-- Manu Thakur (34k points)

1.17.10 Microprogramming: GATE IT 2005 | Question: 49 [top](#)

<https://gateoverflow.in/3810>



- ✓ In horizontal microprogramming we need 1 bit for every control word, therefore total bits in

$$\text{Horizontal Microprogramming} = 20 + 70 + 2 + 10 + 23 = 125$$

Now lets consider vertical microprogramming. In vertical microprogramming we use Decoder (n to 2^n) and output lines are equal to number of control words. A input is given according to what control word we have to select.

Now in this question these 5 groups contains mutually exclusive signals, i.e, they can be activated one at a time for a given group, we can safely use decoder.

group 1 = $\lceil \log_2 20 \rceil = 5$ (Number of input bits for decoder, given output is number of control word in given group)

$$\text{group 2} = \lceil \log_2 70 \rceil = 7$$

$$\text{group 3} = \lceil \log_2 2 \rceil = 1$$

$$\text{group 4} = \lceil \log_2 10 \rceil = 4$$

$$\text{group 5} = \lceil \log_2 23 \rceil = 5$$

$$\text{Total bits required in vertical microprogramming} = 5 + 7 + 1 + 4 + 5 = 22$$

$$\text{So number of control words saved} = 125 - 22 = 103$$

Hence, (B) is answer.

47 votes

-- Prateeksha Keshari (1.7k points)

1.17.11 Microprogramming: GATE IT 2006 | Question: 41 [top](#)

<https://gateoverflow.in/3584>



- ✓ Answer I_1 to I_n are microinstructions and reset_counter, shift_left and load_output are control signals to activate corresponding hardware (e.g. Shift register or load output).

Counter width (k) is 5 bits as shift register uses 32 bit data Only.

The number of missing micro instructions (n) should be 31 as shift register contain Only unsigned EVEN integer. LSB Will be always 0 so no need to shift for LSB.

Control word contains:-

1 for active/enable. 0 for inactive or disabled.

Reset counter is to reset the counter so it must be 0 for all microns.

Shift_left CS should be 1 to shift the given data in shift reg.

And load output has no meaning to make **output** active for all microinstructions as it will be used in the END only so it should be 0.

32 votes

-- khush tak (5.9k points)

1.17.12 Microprogramming: GATE IT 2008 | Question: 39 [top](#)

<https://gateoverflow.in/3349>



- ✓ Its answer should be (D) because 140 instructions, each requiring 7 cycles means 980 cycles which will take 10 bits.

Since it is horizontal for control word, 125 control signals + 10 bits = 135 bits will be required.

38 votes

-- nagendra2016 (349 points)

1.18

Pipelining (36) [top](#)

1.18.1 Pipelining: GATE CSE 1999 | Question: 13 [top](#)

<https://gateoverflow.in/1512>



An instruction pipeline consists of 4 stages – Fetch (F), Decode field (D), Execute (E) and Result Write (W). The 5 instructions in a certain instruction sequence need these stages for the different number of clock cycles as shown by the table below

Instruction	F	D	E	W
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1
5	1	2	1	2

Find the number of clock cycles needed to perform the 5 instructions.

gate1999 co-and-architecture pipelining normal numerical-answers

Answer

1.18.2 Pipelining: GATE CSE 2000 | Question: 1.8 [top](#)

<https://gateoverflow.in/631>



Comparing the time T_1 taken for a single instruction on a pipelined CPU with time T_2 taken on a non-pipelined but identical CPU, we can say that

- A. $T_1 \leq T_2$
- B. $T_1 \geq T_2$
- C. $T_1 < T_2$
- D. T_1 and T_2 plus the time taken for one instruction fetch cycle

gate2000-cse pipelining co-and-architecture easy

Answer



An instruction pipeline has five stages where each stage take 2 nanoseconds and all instruction use all five stages. Branch instructions are not overlapped. i.e., the instruction after the branch is not fetched till the branch instruction is completed. Under ideal conditions,

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- Calculate the average instruction execution time assuming that 20% of all instructions executed are branch instruction. Ignore the fact that some branch instructions may be conditional.
 - If a branch instruction is a conditional branch instruction, the branch need not be taken. If the branch is not taken, the following instructions can be overlapped. When 80% of all branch instructions are conditional branch instructions, and 50% of the conditional branch instructions are such that the branch is taken, calculate the average instruction execution time.



Consider a 5-stage pipeline - IF (Instruction Fetch), ID (Instruction Decode and register read), EX (Execute), MEM (memory), and WB (Write Back). All (memory or register) reads take place in the second phase of a clock cycle and all writes occur in the first phase. Consider the execution of the following instruction sequence:

tests.gatecse.in	I1: sub r2, r3, r4	/* $r2 \leftarrow r3 - r4$ */
goclasses.in	I2: sub r4, r2, r3	/* $r4 \leftarrow r2 - r3$ */
tests.gatecse.in	I3: sw r2, 100(r1)	/* $M[r1 + 100] \leftarrow r2$ */
tests.gatecse.in	I4: sub r3, r4, r2	/* $r3 \leftarrow r4 - r2$ */

- Show all data dependencies between the four instructions.
- Identify the data hazards.
- Can all hazards be avoided by forwarding in this case.



The performance of a pipelined processor suffers if:

- the pipeline stages have different delays
- consecutive instructions are dependent on each other
- the pipeline stages share hardware resources
- All of the above



For a pipelined CPU with a single ALU, consider the following situations

- The $j + 1^{st}$ instruction uses the result of the j^{th} instruction as an operand
- The execution of a conditional jump instruction
- The j^{th} and $j + 1^{st}$ instructions require the ALU at the same time.

Which of the above can cause a hazard

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- I and II only
 - II and III only
 - III only
 - All the three

Answer **1.18.7 Pipelining: GATE CSE 2004 | Question: 69** top<https://gateoverflow.in/1063>

A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 *nanoseconds*, respectively. Registers that are used between the stages have a delay of 5 *nanoseconds* each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be:

- A. 120.4 microseconds
- B. 160.5 microseconds
- C. 165.5 microseconds
- D. 590.0 microseconds

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Answer **1.18.8 Pipelining: GATE CSE 2005 | Question: 68** top<https://gateoverflow.in/1391>

A 5 stage pipelined CPU has the following sequence of stages:

- IF – instruction fetch from instruction memory
- RD – Instruction decode and register read
- EX – Execute: ALU operation for data and address computation
- MA – Data memory access – for write access, the register read at RD state is used.
- WB – Register write back

Consider the following sequence of instructions:

- $I_1: L R0, loc\ 1; R0 \leftarrow M[loc1]$
- $I_2: A R0, R0; R0 \leftarrow R0 + R0$
- $I_3: S R2, R0; R2 \leftarrow R2 - R0$

Let each stage take one clock cycle.

What is the number of clock cycles taken to complete the above sequence of instructions starting from the fetch of I_1 ?

- A. 8
- B. 10
- C. 12
- D. 15

Answer **1.18.9 Pipelining: GATE CSE 2006 | Question: 42** top<https://gateoverflow.in/1818>

A CPU has a five-stage pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 10^9 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, the total execution time of the program is:

- A. 1.0 second
- B. 1.2 seconds
- C. 1.4 seconds
- D. 1.6 seconds

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Answer 



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Consider a pipelined processor with the following four stages:

- IF: Instruction Fetch
- ID: Instruction Decode and Operand Fetch
- EX: Execute
- WB: Write Back

The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD	R2, R1, R0	$R2 \leftarrow R1 + R0$
MUL	R4, R3, R2	$R4 \leftarrow R3 * R2$
SUB	R6, R5, R4	$R6 \leftarrow R5 - R4$

- A. 7
B. 8
C. 10
D. 14

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[gate2007-cse](#) [co-and-architecture](#) [pipelining](#) [normal](#) [isro2009](#)

Answer



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Which of the following are NOT true in a pipelined processor?

- I. Bypassing can handle all RAW hazards
 - II. Register renaming can eliminate all register carried WAR hazards
 - III. Control hazard penalties can be eliminated by dynamic branch prediction
- A. I and II only
B. I and III only
C. II and III only
D. I, II and III

[gate2008-cse](#) [pipelining](#) [co-and-architecture](#) [normal](#)

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Answer



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Delayed branching can help in the handling of control hazards

For all delayed conditional branch instructions, irrespective of whether the condition evaluates to true or false,

- A. The instruction following the conditional branch instruction in memory is executed
- B. The first instruction in the fall through path is executed
- C. The first instruction in the taken path is executed
- D. The branch takes longer to execute than any other instruction

[gate2008-cse](#) [co-and-architecture](#) [pipelining](#) [normal](#)

Answer



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Delayed branching can help in the handling of control hazards

The following code is to run on a pipelined processor with one branch delay slot:

I1: ADD $R2 \leftarrow R7 + R8$

I2: Sub $R4 \leftarrow R5 - R6$

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I3: ADD $R1 \leftarrow R2 + R3$

I4: STORE Memory $[R4] \leftarrow R1$

BRANCH to Label if $R1 == 0$

Which of the instructions I1, I2, I3 or I4 can legitimately occupy the delay slot without any program modification?

A. I1

B. I2

C. I3

D. I4

gate2008-cse co-and-architecture pipelining normal

Answer ↗

1.18.14 Pipelining: GATE CSE 2009 | Question: 28 top ↗

↗ <https://gateoverflow.in/1314>



Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions $I1, I2, I3, I4$ in stages $S1, S2, S3, S4$ is shown below:

	S_1	S_2	S_3	S_4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

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What is the number of cycles needed to execute the following loop?

For ($i = 1$ to 2) {I1; I2; I3; I4;}

A. 16

B. 23

C. 28

D. 30

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gate2009-cse co-and-architecture pipelining normal

Answer ↗

1.18.15 Pipelining: GATE CSE 2010 | Question: 33 top ↗

↗ <https://gateoverflow.in/2207>



A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions?

Instruction	Meaning of instruction
$t_0: MUL R_2, R_0, R_1$	$R_2 \leftarrow R_0 * R_1$
$t_1: DIV R_5, R_3, R_4$	$R_5 \leftarrow R_3 / R_4$
$t_2: ADD R_2, R_5, R_2$	$R_2 \leftarrow R_5 + R_2$
$t_3 : SUB R_5, R_2, R_6$	$R_5 \leftarrow R_2 - R_6$

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A. 13

B. 15

C. 17

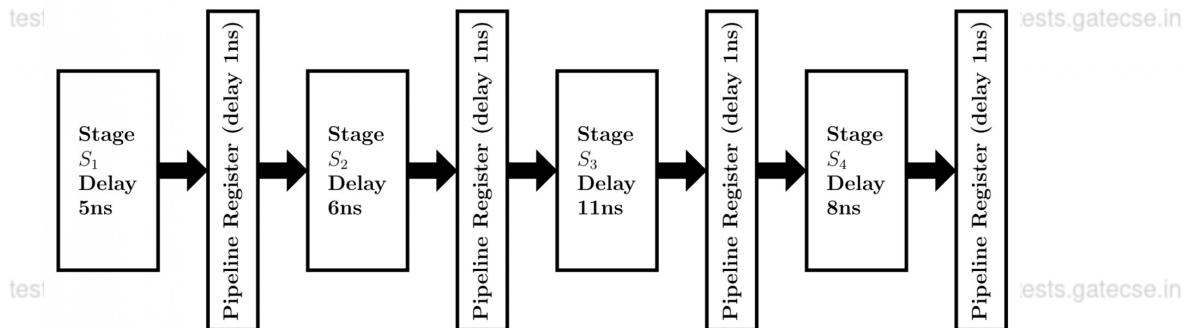
D. 19

gate2010-cse co-and-architecture pipelining normal

Answer 

1.18.16 Pipelining: GATE CSE 2011 | Question: 41 [top](#) <https://gateoverflow.in/2143> 

Consider an instruction pipeline with four stages (S_1, S_2, S_3 and S_4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure.



What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

- A. 4.0
- B. 2.5
- C. 1.1
- D. 3.0

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[gate2011-cse](#) [co-and-architecture](#) [pipelining](#) [normal](#)

Answer 

1.18.17 Pipelining: GATE CSE 2012 | Question: 20, ISRO2016-23 [top](#) <https://gateoverflow.in/52> 

Register renaming is done in pipelined processors:

- A. as an alternative to register allocation at compile time
- B. for efficient access to function parameters and local variables
- C. to handle certain kinds of hazards
- D. as part of address translation

[gate2012-cse](#) [co-and-architecture](#) [pipelining](#) [easy](#) [isro2016](#)

Answer 

1.18.18 Pipelining: GATE CSE 2013 | Question: 45 [top](#) <https://gateoverflow.in/330> 

Consider an instruction pipeline with five stages without any branch prediction:

Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions $I_1, I_2, I_3, \dots, I_{12}$ is executed in this pipelined processor. Instruction I_4 is the only branch instruction and its branch target is I_9 . If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is

- A. 132
- B. 165
- C. 176
- D. 328

[gate2013-cse](#) [normal](#) [co-and-architecture](#) [pipelining](#)

Answer 



Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 25% of the instructions incur 2 pipeline stall cycles is _____

[gate2014-cse-set1](#) [co-and-architecture](#) [pipelining](#) [numerical-answers](#) [normal](#)

Answer



An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode and register fetch (ID/RF), instruction execution (EX), memory access (MEM), and register writeback (WB) with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns, respectively (ns stands for nanoseconds). To gain in terms of frequency, the designers have decided to split the ID/RF stage into three stages (ID, RF1, RF2) each of latency 2.2/3 ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages. A program has 20% branch instructions which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are P and Q nanoseconds, respectively. The value of P/Q is _____.

[gate2014-cse-set3](#) [co-and-architecture](#) [pipelining](#) [numerical-answers](#) [normal](#)

Answer



Consider the following processors (ns stands for nanoseconds). Assume that the pipeline registers have zero latency.

- P1: Four-stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns.
- P2: Four-stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns.
- P3: Five-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns.
- P4: Five-stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns.

Which processor has the highest peak clock frequency? [goclasses.in](#)

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- A. P1
B. P2
C. P3
D. P4

[gate2014-cse-set3](#) [co-and-architecture](#) [pipelining](#) [normal](#)

Answer



Consider a non-pipelined processor with a clock rate of 2.5 GHz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 GHz. Assume that there are no stalls in the pipeline. The speedup achieved in this pipelined processor is _____.

[gate2015-cse-set1](#) [co-and-architecture](#) [pipelining](#) [normal](#) [numerical-answers](#)

Answer



Consider the sequence of machine instruction given below:

MUL	R5, R0, R1
DIV	R6, R2, R3
ADD	R7, R5, R6
SUB	R8, R7, R4

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In the above sequence, $R0$ to $R8$ are general purpose registers. In the instructions shown, the first register shows the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: (1) Instruction Fetch and Decode (*IF*), (2) Operand Fetch (*OF*), (3) Perform Operation (*PO*) and (4) Write back the result (*WB*). The *IF*, *OF* and *WB* stages take 1 clock cycle each for any instruction. The *PO* stage takes 1 clock cycle for ADD and SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the *PO* stage to the *OF* stage. The number of clock cycles taken for the execution of the above sequence of instruction is _____.

[gate2015-cse-set2](#) [co-and-architecture](#) [pipelining](#) [normal](#) [numerical-answers](#)

Answer 

1.18.24 Pipelining: GATE CSE 2015 Set 3 | Question: 51 top ↗

<https://gateoverflow.in/8560>



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Consider the following reservation table for a pipeline having three stages S_1 , S_2 and S_3 .

Time →	1	2	3	4	5
S_1	X			X	
S_2		X		X	
S_3			X		

The minimum average latency (MAL) is _____

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[gate2015-cse-set3](#) [co-and-architecture](#) [pipelining](#) [difficult](#) [numerical-answers](#)

Answer 

1.18.25 Pipelining: GATE CSE 2016 Set 1 | Question: 32 top ↗

<https://gateoverflow.in/39691>



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The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionality equivalent design involving two stages with respective delays 600 and 350 picoseconds. The throughput increase of the pipeline is _____ percent.

[gate2016-cse-set1](#) [co-and-architecture](#) [pipelining](#) [normal](#) [numerical-answers](#)

Answer 

1.18.26 Pipelining: GATE CSE 2016 Set 2 | Question: 33 top ↗

<https://gateoverflow.in/39580>



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Consider a 3 GHz (gigahertz) processor with a three stage pipeline and stage latencies τ_1 , τ_2 and τ_3 such that $\tau_1 = \frac{3\tau_2}{4} = 2\tau_3$.

If the longest pipeline stage is split into two pipeline stages of equal latency , the new frequency is _____ GHz, ignoring delays in the pipeline registers.

[gate2016-cse-set2](#) [co-and-architecture](#) [pipelining](#) [normal](#) [numerical-answers](#)

Answer 

1.18.27 Pipelining: GATE CSE 2017 Set 1 | Question: 50 top ↗

<https://gateoverflow.in/118719>



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Instruction execution in a processor is divided into 5 stages, *Instruction Fetch* (IF), *Instruction Decode* (ID), *Operand fetch* (OF), *Execute* (EX), and *Write Back* (WB). These stages take 5, 4, 20, 10 and 3 nanoseconds (ns) respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of 2 ns. Two pipelined implementation of the processor are contemplated:

- i. a naive pipeline implementation (NP) with 5 stages and
- ii. an efficient pipeline (EP) where the OF stage is divided into stages OF1 and OF2 with execution times of 12 ns and 8 ns respectively.

The speedup (correct to two decimal places) achieved by EP over NP in executing 20 independent instructions with no hazards is _____.

Answer

1.18.28 Pipelining: GATE CSE 2018 | Question: 50 top<https://gateoverflow.in/204125>

The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (*IF*), Instruction Decode (*ID*), Operand Fetch (*OF*), Perform Operation (*PO*) and Writeback (*WB*). The *IF*, *ID*, *OF* and *WB* stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the *PO* stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards.

The number of clock cycles required for completion of execution of the sequence of instruction is _____.

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Answer

1.18.29 Pipelining: GATE CSE 2020 | Question: 43 top<https://gateoverflow.in/333188>

Consider a non-pipelined processor operating at 2.5 GHz. It takes 5 clock cycles to complete an instruction. You are going to make a 5- stage pipeline out of this processor. Overheads associated with pipelining force you to operate the pipelined processor at 2 GHz. In a given program, assume that 30% are memory instructions, 60% are ALU instructions and the rest are branch instructions. 5% of the memory instructions cause stalls of 50 clock cycles each due to cache misses and 50% of the branch instructions cause stalls of 2 cycles each. Assume that there are no stalls associated with the execution of ALU instructions. For this program, the speedup achieved by the pipelined processor over the non-pipelined processor (round off to 2 decimal places) is _____.

Answer

1.18.30 Pipelining: GATE CSE 2021 Set 1 | Question: 53 top<https://gateoverflow.in/357398>

A five-stage pipeline has stage delays of 150, 120, 150, 160 and 140 nanoseconds. The registers that are used between the pipeline stages have a delay of 5 nanoseconds each.

The total time to execute 100 independent instructions on this pipeline, assuming there are no pipeline stalls, is _____ nanoseconds.

Answer

1.18.31 Pipelining: GATE IT 2004 | Question: 47 top<https://gateoverflow.in/3690>

Consider a pipeline processor with 4 stages *S*₁ to *S*₄. We want to execute the following loop:

```
for (i = 1; i <= 1000; i++)
    {I1, I2, I3, I4}
```

where the time taken (in ns) by instructions *I*₁ to *I*₄ for stages *S*₁ to *S*₄ are given below:

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	<i>S</i> ₁	<i>S</i> ₂	<i>S</i> ₃	<i>S</i> ₄
I1	1	2	1	2
I2	2	1	2	1
I3	1	1	2	1
I4	2	1	2	1

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The output of *I*₁ for *i* = 2 will be available after

- A. 11 ns
- B. 12 ns
- C. 13 ns
- D. 28 ns

Answer



We have two designs D_1 and D_2 for a synchronous pipeline processor. D_1 has 5 pipeline stages with execution times of 3 nsec, 2 nsec, 4 nsec, 2 nsec and 3 nsec while the design D_2 has 8 pipeline stages each with 2 nsec execution time. How much time can be saved using design D_2 over design D_1 for executing 100 instructions?

- A. 214 nsec
- B. 202 nsec
- C. 86 nsec
- D. -200 nsec

[gate2005-it](#) [co-and-architecture](#) [pipelining](#) [normal](#)

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[Answer](#)



A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement $X = (S - R * (P + Q)) / T$ is given below. The values of variables P, Q, R, S and T are available in the registers $R0, R1, R2, R3$ and $R4$ respectively, before the execution of the instruction sequence.

ADD	R5, R0, R1	; R5 \leftarrow R0 + R1
MUL	R6, R2, R5	; R6 \leftarrow R2 * R5
SUB	R5, R3, R6	; R5 \leftarrow R3 - R6
DIV	R6, R5, R4	; R6 \leftarrow R5/R4
STORE	R6, X	; X \leftarrow R6

The number of Read-After-Write (RAW) dependencies, Write-After-Read (WAR) dependencies, and Write-After-Write (WAW) dependencies in the sequence of instructions are, respectively,

- A. 2, 2, 4
- B. 3, 2, 3
- C. 4, 2, 2
- D. 3, 3, 2

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[Answer](#)



A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement $X = (S - R * (P + Q)) / T$ is given below. The values of variables P, Q, R, S and T are available in the registers $R0, R1, R2, R3$ and $R4$ respectively, before the execution of the instruction sequence.

ADD	R5, R0, R1	; R5 \leftarrow R0 + R1
MUL	R6, R2, R5	; R6 \leftarrow R2 * R5
SUB	R5, R3, R6	; R5 \leftarrow R3 - R6
DIV	R6, R5, R4	; R6 \leftarrow R5/R4
STORE	R6, X	; X \leftarrow R6

The IF, ID and WB stages take 1 clock cycle each. The EX stage takes 1 clock cycle each for the ADD, SUB and STORE operations, and 3 clock cycles each for MUL and DIV operations. Operand forwarding from the EX stage to the ID stage is used. The number of clock cycles required to complete the sequence of instructions is

- A. 10
- B. 12
- C. 14
- D. 16

Answer

1.18.35 Pipelining: GATE IT 2007 | Question: 6, ISRO2011-25 [top](#)<https://gateoverflow.in/3437>

A processor takes 12 cycles to complete an instruction I. The corresponding pipelined processor uses 6 stages with the execution times of 3, 2, 5, 4, 6 and 2 cycles respectively. What is the asymptotic speedup assuming that a very large number of instructions are to be executed?

- A. 1.83
B. 2
C. 3
D. 6

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Answer

1.18.36 Pipelining: GATE IT 2008 | Question: 40 [top](#)<https://gateoverflow.in/3350>

A non pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 nsec , 1.5 nsec , 2 nsec , 1.5 nsec and 2.5 nsec , respectively. The delay of the latches is 0.5 nsec . The speedup of the pipeline processor for a large number of instructions is:

- A. 4.5
B. 4.0
C. 3.33
D. 3.0

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Answer

Answers: Pipelining

1.18.1 Pipelining: GATE CSE 1999 | Question: 13 [top](#)<https://gateoverflow.in/1512>

- ✓ Answer: 15 cycles are required.

	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	t_{13}	t_{14}	t_{15}
I_1	F	D	D	E	W										
I_2		F	—	D	D	E	E	W							
I_3			F	F	D	—	E	E	E	W	W				
I_4				F	—	D	D	D	E	E	W				
I_5					F	—	—	D	D	E	W	W			

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37 votes

-- Amar Vashishth (25.2k points)

1.18.2 Pipelining: GATE CSE 2000 | Question: 1.8 [top](#)<https://gateoverflow.in/631>

- ✓ Here we are comparing the execution time of only a single instruction. Pipelining in no way improves the execution time of a single instruction (the time from its start to end). It increases the overall performance by splitting the execution to multiple pipeline stages so that the following instructions can use the finished stages of the previous instructions. But in doing so, pipelining causes some problems also as given in the below link, which might slow some instructions. So, (B) is the answer.

<http://www.cs.wvu.edu/~jdm/classes/cs455/notes/tech/instrpipe.html>

References



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54 votes

-- Arjun Suresh (332k points)

1.18.3 Pipelining: GATE CSE 2000 | Question: 12 top<https://gateoverflow.in/683>

- ✓ Each stage is 2ns. So, after 5 time units each of 2ns, the first instruction finishes (i.e., after 10ns), in every 2ns after that a new instruction gets finished. This is assuming no branch instructions. Now, once the pipeline is full, we can assume that the initial fill time doesn't matter our calculations and average execution time for each instruction is 2ns assuming no branch instructions.

- A. Now, we are given that 20% of instructions are branch (like JMP) and when a branch instruction is executed, no further instruction enters the pipeline. So, we can assume every 5th instruction is a branch instruction. So, with this assumption, total time to finish 5 instruction will be $5 * 2 + 8 = 18$ ns (as when a branch instruction enters the pipeline and before it finishes, 4 pipeline stages will be empty totaling $4 * 2 = 8$ ns, as it is mentioned in question that the next instruction fetch starts only when branch instruction completes). And this is the same for every set of 5 instructions, and hence the average instruction execution time $= 18/5 = 3.6$ ns
- B. This is just a complex statement. But what we need is to identify the % of branch instructions which cause a branch to be taken as others will have no effect on the pipeline flow.
20% of instructions are branch instructions. 80% of branch instructions are conditional.
That means $.2 * .8 = 16\%$ of instructions are conditional branch instructions and it is given that 50% of those result in a branch being taken.
So, 8% of instructions are conditional branches being taken and we also have $20\% \text{ of } 20\% = 4\%$ of unconditional branch instructions which are always taken.

So, percentage of instructions where a branch is taken is $8 + 4 = 12\%$ instead of 20% in (A) part.

So, in 100 instructions there will be 12 branch instructions. We can do a different calculation here as compared to (A) as 12 is not a divisor of 100. Each branch instruction causes a pipeline delay of $4 * 2 = 8$ ns. So, 12 instructions will cause a delay of $12 * 8 = 96$ ns. For 100 instructions, we need $100 * 2 = 200$ ns without any delay and with delay we require $200 + 96 = 296$ ns for 100 instructions.

So, average instruction execution time $= 296/100 = 2.96$ ns

(We can also use this method for part (A) which will give $100 * 2 + 20 * 8 = 360$ ns for 100 instructions)

64 votes

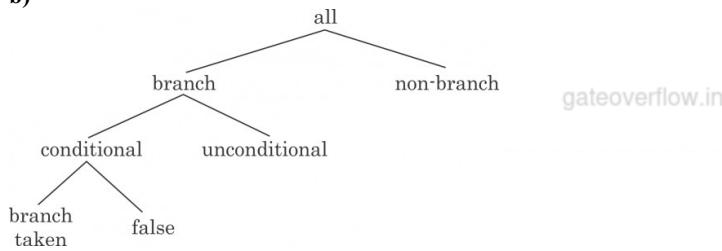
-- Arjun Suresh (332k points)

if an instruction branches then it takes $2ns \times 5 = 10ns$, coz if branch is taken then the instruction after that branch instruction is not fetched until entire current branch instruction is completed, this means it will go through all stages.

if an instruction is non-branch or branching does not happen then, it takes $2ns$ to get completed.

a) average time taken $= 0.8 \times 2ns + 0.2 \times 10ns = 3.6ns$

b)



Average time taken,

$$= 0.8 \times 2ns + 0.2(0.2 \times 10ns + 0.8((0.5 \times 10ns + 0.5 \times 2ns)))$$

$$= 2.96ns$$

74 votes

-- Amar Vashishth (25.2k points)

1.18.4 Pipelining: GATE CSE 2001 | Question: 12 top

<https://gateoverflow.in/753>



- ✓ RAW dependencies:

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1. $I_1 \leftarrow I_2$
2. $I_1 \leftarrow I_3$
3. $I_1 \leftarrow I_4$
4. $I_2 \leftarrow I_4$

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WAR dependencies:

1. $I_2 \leftarrow I_1$
2. $I_4 \leftarrow I_1$
3. $I_4 \leftarrow I_2$

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Consider a normal pipeline execution:

	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈
I ₁	IF	ID	EX	MEM	WB			
I ₂		IF	ID	EX	MEM	WB		
I ₃			IF	ID	EX	MEM	WB	
I ₄				IF	ID	EX	MEM	WB

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So, there are RAW hazards for I_2 and I_3 with I_1 and for I_4 with I_2 . (Not all dependencies cause a hazard. Only if a dependency causes a stall in the given pipeline structure, we get a hazard) These hazards cause the following stalls in the pipeline:

	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈	t ₉	t ₁₀	t ₁₁
I ₁	IF	ID	EX	MEM	WB						
I ₂		IF	—	—	ID	EX	MEM	WB			
I ₃			—	—	IF	ID	EX	MEM	WB		
I ₄				—	—	IF	—	ID	EX	MEM	WB

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Now, with operand forwarding from EX – EX stage we can do as follows:

	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈
I ₁	IF	ID	EX ₁	MEM	WB			
I ₂		IF	ID	EX ₁	MEM	WB		
I ₃			IF	ID	EX ₁	MEM	WB	
I ₄				IF	ID	EX ₃	MEM	WB

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Thus all hazards are eliminated.

Ref: <http://cseweb.ucsd.edu/classes/wi05/cse240a/pipe2.pdf>

References



40 votes

-- Arjun Suresh (332k points)

1.18.5 Pipelining: GATE CSE 2002 | Question: 2.6, ISRO2008-19 top

<https://gateoverflow.in/836>



- ✓ Answer is D.

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A: Yes. Total delay = Max (All delays) + Register Delay.

B: Yes, if data forwarding is not there.

C: Yes, like ID and EX shares ID/EX register.

35 votes

-- Rajarshi Sarkar (27.9k points)

1.18.6 Pipelining: GATE CSE 2003 | Question: 10, ISRO-DEC2017-41 [top](#)

<https://gateoverflow.in/901>



- ✓ 1. Data hazard
- 2. Control hazard
- 3. Structural hazard as only one ALU is there

So, (D) .

<http://www.cs.iastate.edu/~prabhu/Tutorial/PIPELINE/hazards.html>

References



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56 votes

-- Arjun Suresh (332k points)

1.18.7 Pipelining: GATE CSE 2004 | Question: 69 [top](#)

<https://gateoverflow.in/1063>



- ✓ Pipelining requires all stages to be synchronized meaning, we have to make the delay of all stages equal to the maximum pipeline stage delay which here is 160. We also have to add the intermediate register delay which here is 5ns which makes the clock period as 165ns .

Time for execution of the first instruction = $165 * 4 = 660$ ns.

Now, in every 165 ns, an instruction can be completed. So,

Total time for 1000 instructions = $660 + 999 * 165 = 165.495$ microseconds

Correct Answer: C

57 votes

-- Arjun Suresh (332k points)

1.18.8 Pipelining: GATE CSE 2005 | Question: 68 [top](#)

<https://gateoverflow.in/1391>



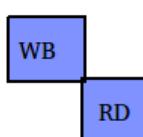
- ✓ Answer is option A.

Without data forwarding:

13 clock - WB and RD state non overlapping.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
IF	RD	EX	MA	WB								
	IF				RD	EX	MA	WB				
					IF				RD	EX	MA	WB

Here, WB and RD stage operate in Non-Overlapping mode.

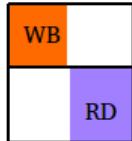


11 clock - WB and RD states overlapping.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11
IF	RD	EX	MA	WB	overlap	flow.in				
	IF			RD	EX	MA	WB			
				IF			RD	EX	MA	WB

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Split Phase access between WB and RD means:



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WB stage produce the output during the rising edge of the clock and RD stage fetch the output during the falling edge.

In Question it is mentioned

for write access, the register read at RD state is used.

This means that for writing operands back to memory, register read at RD state is used (no operand forward for STORE instructions).

Note

- As in any question in any subject unless otherwise stated we always consider the best case. So, do overlap - unless otherwise stated. But this is for only WB/RD

1. Why there is stall for I2 in T3 and T4 ?

RD is instruction decode and register read. If we execute RD of I2 in T3, data from memory will not get stored to R0 hence proper operands are not available at T3. Perhaps I2 has to wait until I1 write values to memory.

2. WB of I1 and RD of I2 are operating in same clock why it is so ?

If nothing has mentioned in question. This scenario is taken into consideration by default. It is because after MA operands will be available in register so RD and WB could overlap .

With data forwarding

(Should be the case here as question says no operand forwarding for memory register for STORE instructions)

8 clock cycles

1	2	3	4	5	6	7	8	9
IF	RD	EX	MA	WB				
	IF	RD		EX	MA	WB		
	IF	RD	EX	MA	MM	WB		

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1. Why there is a stall I2 in T4 ?

Data is being forwarded from MA of I1 EX of I2 .MA operation of I1 must complete so that correct data will be available in register .

2. Why RD of I2 in T3 ? Will it not fetch incorrect information if executed before Operand are forwarded from MA of I1 ?

Yes. RD of I2 will definitely fetch INCORRECT data at T3 . But don't worry about it Operand Forwarding technique will take care of it .

3. Why can't RD of I2 be placed in T4 ?

Yes . We can place RD of I2 in T4 as well. But what is the fun in that ? pipeline is a technique used to reduce the execution time of instructions . Why do we need to make an extra stall ? Moreover there is one more problem which is discussed just below .After reading the below point Just think if we had created a stall at T3 !

4. Why can't RD of I3 be placed at T4 ?

This cannot be done . I3 cannot use RD because Previous instruction I2 should start next stage (EX) before current (I3) could utilize that(RD) stage . It is because data will be residing in buffers.

5. Can an operand being forwarded from one clock cycle to same clock cycle ?

No, the previous clock cycle must complete before data being forwarded . Unless split phase technique is used

6. Cant there be a forwarding from EX stage(T3) of I1 to EX stage(T4) of I2 ?

This is not possible . See what is happening in I1 . It is Memory Read .So data will be available in register after memory read only .So data cannot be forwarded from EX of I1 .

7. In some case data is forwarded from MA and some case data is forwarded from EX Why it is so ?

Data is forwarded when it is ready . It solely depends on the type of instruction .

8. When to use Split-Phase ?

We can use split phase if data is readily available like between WB/RD and also when operand forwarding happens from EX-ID stage, but not from EX-EX stage. We cannot do split phase access between EX-EX because here the instruction execution may not be possible in the first phase. (This is not mentioned in any standard resource but said by Arjun Suresh by considering practical implementation and how previous year GATE questions have been formed)

[Mostly it is given in question that there is operand forwarding from A stage to B stage eg:https://gateoverflow.in/8218/gate2015-2_44]

Split-Phase can be used even when no Operand Forwarding because they aren't related.

References

- <http://web.cs.iastate.edu/~prabhu/Tutorial/PIPELINE/forward.html>

Similar Questions

- https://gateoverflow.in/8218/gate2015-2_44
- <https://gateoverflow.in/2207/gate2010-33>
- <https://gateoverflow.in/34735/pipelining-without-operand-forwarding>

Discussions

- <https://gateoverflow.in/102565/operand-forwarding-in-pipeline>
- <https://gateoverflow.in/113244/doubts-in-pipelining>

References



-- Akhil Nadh PC (16.5k points)

1.18.9 Pipelining: GATE CSE 2006 | Question: 42 [top](#)

<https://gateoverflow.in/1818>



- ✓ Delay slots in the pipeline caused due to a branch instruction is 2 as after the 3rd stage of current instruction (during 4th stage) IF of next begins.
Ideally, this should be during 2nd stage.

So, for total no. of instructions = 10^9 and 20% branch,
we have $0.2 \times 2 \times 10^9 = 4 \times 10^8$ cycle penalty.

Since clock speed is 1 GHz and each instruction on average takes 1 cycle,
total execution time in seconds will be

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$$= \frac{10^9}{10^9} + 4 \times \frac{10^8}{10^9}$$

$$= 1.4$$

Correct Answer: C

126 votes

-- Arjun Suresh (332k points)



✓ Answer: option B.

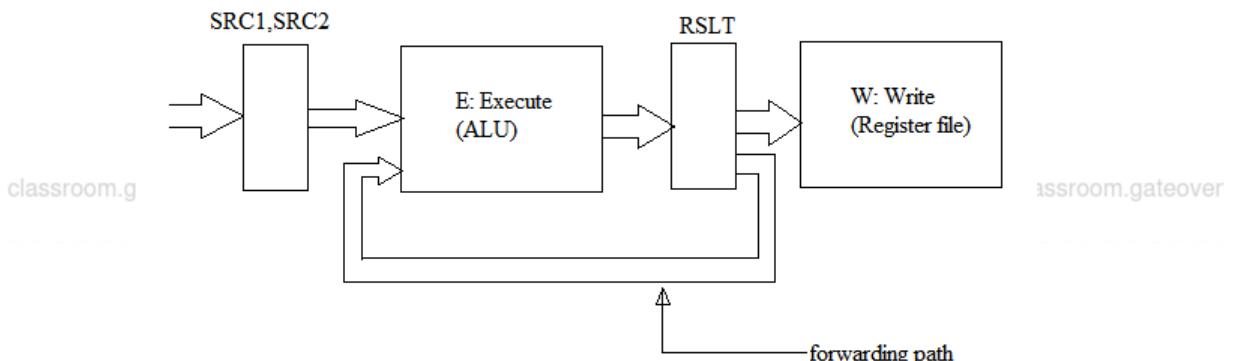
Considering EX to EX data forwarding.

	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8
ADD	IF	ID	EX	WB				
MUL		IF	ID	EX	EX	EX	WB	
SUB			IF	ID	-	EX	WB	WB

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EX to EX data Forwarding:



Position of the source and result registers in the processor pipeline

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47 votes

-- Rajarshi Sarkar (27.9k points)



✓ (B) I and III

I - False Bypassing can't handle all RAW hazard, consider when any instruction depends on the result of LOAD instruction, now LOAD updates register value at Memory Access Stage (MA), so data will not be available directly on Execute stage.

II - True, register renaming can eliminate all WAR Hazard.

III- False, It cannot completely eliminate, though it can reduce Control Hazard Penalties

81 votes

-- Prateeksha Keshari (1.7k points)



✓ Answer is A. In order to avoid the pipeline delay due to conditional branch instruction, a suitable instruction is placed below the conditional branch instruction such that the instruction will be executed irrespective of whether branch is taken or not and won't affect the program behaviour.

60 votes

-- Arjun Suresh (332k points)



✓ What is Delayed Branching?

One way to maximize the use of the pipeline, is to find an instruction that can be safely executed whether the branch is taken or not, and execute that instruction. So, when a branch instruction is encountered, the hardware puts the instruction following the branch into the pipe and begins executing it, just as in predict-not-taken. However, unlike in predict-not-taken, we do not need to worry about whether the branch is taken or not, we do not need to clear the pipe because no matter whether the branch is taken or not, we know the instruction is safe to execute.

Moving I_1 after branch

- I_1 is updating the value of $R2$

- $R2$ which is used to determine branch condition $R1$

- Value of $R2$ is available after branch
⇒ Cannot be moved

Moving I_3 after branch

- value of $R1$ is computed in this instruction
- $R1$ is the branch condition
⇒ Cannot be moved

Moving I_4 after branch

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- I_4 is simple store instruction used to store $R1$ in memory
- program execution will have no effect if this is placed after conditional branch
⇒ Can be moved

Moving I_2 after branch

- It update the memory location to place the storing of conditional branch instruction $R1$
- If moved after branch , when compiler reaches I_4 program execution will stop
⇒ Cannot be moved

Hence, **option D is answer.**

拇指 60 votes

-- Akhil Nadh PC (16.5k points)

1.18.14 Pipelining: GATE CSE 2009 | Question: 28 top

→ <https://gateoverflow.in/1314>



- ✓ Here bound of the loop are constants, therefore compiler will do the loop unrolling(If compiler won't then prefetcher will do) to increase the instruction level parallelism. And after loop unrolling 23 cycles are required for execution. Therefore, correct answer would be **(B)**.

PS: We assume the buffers between the pipeline stages can store multiple results in the form of a queue.

	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}	C_{17}	C_{18}	C_{19}	C_{20}	C_{21}	C_{22}	C_{23}	
I_1	S_1	S_1	S_2	S_3	S_4																			
I_2			S_1	S_2	S_2	S_2	S_3	S_3	S_4	S_4														
I_3				S_1	S_1	—	S_2	—	S_3	—	S_4	S_1	S_1	S_1										
I_4						S_1	—	S_2	S_2	S_3	S_3	—	—	—	S_4	S_4								
I_1						S_1	S_1	—	S_2	S_2	S_3	—	—	—	—	—	—	—	—	—	—	—	—	
I_2								S_1	—	S_2	S_2	S_3	S_3	S_4	—	—	S_4							
I_3									S_1	S_1	—	—	S_2	—	S_3	—	S_4	—	S_4	S_4	S_4	S_4	S_4	
I_4										S_1	—	S_2	S_2	S_3	S_3	S_4	—	—	—	—	—	—	—	

拇指 56 votes

-- suraj (4.8k points)

1.18.15 Pipelining: GATE CSE 2010 | Question: 33 top

→ <https://gateoverflow.in/2207>



	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	t_{13}	t_{14}	t_{15}
MUL	IF	ID	OF	PO	PO	PO	WO								
DIV	IF	ID	OF	—	—	PO	PO	PO	PO	PO	PO	WO			
ADD		IF	ID	—	—	OF	—	—	—	—	—	PO	WO		
SUB		IF	IF	—	—	ID	—	—	—	—	—	OF	PO	WO	

Operand forwarding allows an output to be passed for the next instruction. Here from the output of PO stage of DIV instruction operand is forwarded to the PO stage of ADD instruction and similarly between ADD and SUB instructions. Hence, 15cycles required.

<http://www.cs.iastate.edu/~prabhu/Tutorial/PIPELINE/forward.html>

Correct Answer: **B**

References



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64 votes

-- Arjun Suresh (332k points)

1.18.16 Pipelining: GATE CSE 2011 | Question: 41 [top](#)

<https://gateoverflow.in/2143>



- ✓ Answer is (B) 2.5

In pipeline system, Time taken is determined by the max delay at any stage i.e., 11 ns plus the delay incurred by pipeline stages i.e., $1 \text{ ns} = 12 \text{ ns}$. In non-pipeline system,

$$\text{Delay} = 5 \text{ ns} + 6 \text{ ns} + 11 \text{ ns} + 8 \text{ ns} = 30 \text{ ns}.$$

$$\therefore \text{The speedup is } \frac{30}{12} = 2.5 \text{ ns.}$$

53 votes

-- Sona Praneeth Akula (3.4k points)

1.18.17 Pipelining: GATE CSE 2012 | Question: 20, ISRO2016-23 [top](#)

<https://gateoverflow.in/52>



- ✓ Register renaming is done to eliminate WAR (Write after Read) and WAW (Write after Write) dependency between instructions which could have caused pipeline stalls. Hence, (C) is the answer.

Example:

I1: Read A to B

I2: Write C to A

Here, there is a WAR dependency and pipeline would need stalls. In order to avoid it register renaming is done and

Write C to A

will be

Write C to A'

WAR dependency is actually called anti-dependency and there is no real dependency except the fact that both uses same memory location. Register renaming can avoid this. Similarly WAW also.

<http://people.ee.duke.edu/~sorin/ece252/lectures/4.2-tomasulo.pdf>

References



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52 votes

-- Arjun Suresh (332k points)

1.18.18 Pipelining: GATE CSE 2013 | Question: 45 [top](#)

<https://gateoverflow.in/330>



- ✓ After pipelining we have to adjust the stage delays such that no stage will be waiting for another to ensure smooth pipelining (continuous flow). Since we can not easily decrease the stage delay, we can increase all the stage delays to the maximum delay possible. So, here maximum delay is 10 ns. Buffer delay given is 1ns. So, each stage takes 11 ns in total.

FI of I9 can start only after the EI of I4. So, the total execution time will be

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$15 \times 11 = 165$

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	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	t_{13}	t_{14}	t_{15}
I1	FI	DI	FO	EI	WO										
I2		FI	DI	FO	EI	WO									
I3			FI	DI	FO	EI	WO								
I4				FI	DI	FO	EI	WO							
						stall	stall	stall							
I9								FI	DI	FO	EI	WO			
I10									FI	DI	FO	EI	WO		
I11									FI	DI	FO	EI	WO		
I12										FI	DI	FO	EI	WO	

Correct Answer: B
122 votes -- gatecse (63.3k points)

1.18.19 Pipelining: GATE CSE 2014 Set 1 | Question: 43

<https://gateoverflow.in/1921>



- Time without pipeline = 6 stages = 6 cycles

Time with pipeline = 1 + stall frequency × stall cycle

$$= 1 + .25 \times 2 \\ = 1.5$$

$$\text{Speed up} = \frac{6}{1.5} = 4$$

64 votes

-- aravind90 (389 points)

1.18.20 Pipelining: GATE CSE 2014 Set 3 | Question: 43

<https://gateoverflow.in/2077>



- Five stages:

(IF), instruction decode and register fetch (ID/RF),
instruction execution (EX),
memory access (MEM), and register writeback (WB)

P old design:

with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns

$\text{MAX}(1 \text{ ns}, 2.2 \text{ ns}, 2 \text{ ns}, 1 \text{ ns}, \text{ and } 0.75 \text{ ns}) = 2.2 \text{ nsec}$

AVG instruction execution time is

$T_{avg} = (1 + \text{no of stalls} \times \text{branch penalty}) \times \text{cycle time}$

$= (1 + 0.20 \times 2)2.2 \quad \{ \text{branch peanlity is 2 because the next instruction pointer at the end of the EX stage in the old design.} \}$

$$= 3.08 \text{ nsec}$$

Q :new DESIGN:

the designers decided to split the ID/RF stage into three stages (ID, RF1, RF2)

each of latency $\frac{2.2}{3}$ ns. Also, the EX stage is split into two stages

(EX1, EX2) each of latency 1 ns.

The new design has a total of eight pipeline stages.

Time of stages in new design = {1 ns, 0.73ns, 0.73ns, 0.73ns , 1ns, 1ns, 1 ns, and 0.75 ns}

(IF), instruction decode

register fetch (ID/RF) → further divided into 3 ie with latency 0.73 of each

instruction execution (EX) → further divided int 1 nsec of each)

memory access (MEM)

register writeback (WB)

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MAX(1 ns, 0.73ns, 0.73ns, 0.73ns , 1ns, 1ns, 1 ns, and 0.75 ns) =1 nsec

AVG instruction execution time is

$$T_{avg} = (1 + \text{no of stalls} \times \text{branch penalty}) \times \text{cycle time}$$

$$= (1 + 0.20 \times 5)1 \quad \{ \text{branch penalty is 5 because the next instruction pointer at the end of the } EX2 \text{ stage in the new design.}\}$$

$$= 2 \text{nsec}$$

final result

$$\frac{P}{Q} = \frac{3.08}{2} = 1.54$$

Upvote 59 votes

-- kunal chalota (13.6k points)



1.18.21 Pipelining: GATE CSE 2014 Set 3 | Question: 9

<https://gateoverflow.in/2043>

✓ frequency = $\frac{1}{\max(\text{time in stages})}$
for P_3 , it is $\frac{1}{1}$ GHz

for P_1 , it is $\frac{1}{2} = 0.5$ GHz

for P_2 , it is $\frac{1}{1.5} = 0.67$ GHz

for P_4 , it is $\frac{1}{1.1}$ GHz

Correct Answer: C

Upvote 41 votes

-- Arpit Dhuriya (2.9k points)



1.18.22 Pipelining: GATE CSE 2015 Set 1 | Question: 38

<https://gateoverflow.in/8288>

✓ Answer = 3.2.

To compute cycle time, we know that a 2.5 GHz processor means it completes 2.5 billion cycles in a second. So, for an instruction which on an average takes 4 cycles to get completed, it will take $\frac{4}{2.5}$ nanoseconds.

On a perfect pipeline (i.e., one which has no stalls) CPI = 1 as during it an instruction takes just one cycle time to get completed.

So,

$$\text{Speed Up} = \frac{\text{Old Execution Time of an Instruction}}{\text{New Execution Time of an Instruction}}$$

$$= \frac{CPI_{old}/CF_{old}}{CPI_{new}/CF_{new}}$$

$$= \frac{4/2.5 \text{ GHz}}{1/2 \text{ GHz}}$$

$$= 3.2$$

Upvote 87 votes

-- naresh1845 (1.1k points)

$$\text{Speed up} = \frac{\text{Old execution time}}{\text{New execution time}}$$

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$$\text{Old execution time} = \frac{\text{CPI}}{2.5} = \frac{4}{2.5} = 1.6 \text{ ns}$$

With pipelining,

$$= \frac{\text{each instruction needs old execution time} \times \text{old frequency}}{\text{new frequency (without pipelining)}}$$

$$= \frac{1.6 \times 2.5}{2} = 2 \text{ ns}$$

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There are 5 stages and when there is no pipeline stall, this can give a speed up of up to 5 (happens when all stages take same number of cycles).

In our case this time will be $\frac{2}{5} = 0.4 \text{ ns.}$

But clock frequency being 2 GHz, clock cycle is $\frac{1}{2} \text{ GHz} = 0.5 \text{ ns}$

and a pipeline stage cannot be faster than this.

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So, average instruction execution time after pipelining = $\max(0.4, 0.5) = 0.5 \text{ ns.}$

So, speed up compared to non-pipelined version = $\frac{1.6}{0.5} = 3.2$

👍 35 votes

-- Arjun Suresh (332k points)

1.18.23 Pipelining: GATE CSE 2015 Set 2 | Question: 44 top ↗

↗ <https://gateoverflow.in/8218>



	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈	t ₉	t ₁₀	t ₁₁	t ₁₂	t ₁₃	t ₁₄	t ₁₅
I1	IF	OF	PO	PO	PO	WB									
I2		IF	OF	—	—	PO	PO	PO	PO	PO	WB				
I3			IF	—	—	—	—	—	—	—	OF	PO	WB		
I4				—	—	—	—	—	—	—	IF	—	OF	PO	WB

It is mentioned in the question that operand forwarding takes place from PO stage to OF stage and not to PO stage. So, 15 clock cycles.

But since operand forwarding is from PO-OF, we can do like make the PO stage produce the output during the rising edge of the clock and OF stage fetch the output during the falling edge. This would mean the final PO stage and OF stage can be done in one clock cycle making the total number of cycles = 13. And 13 is the answer given in GATE key.

	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈	t ₉	t ₁₀	t ₁₁	t ₁₂	t ₁₃	
I1	IF	OF	PO	PO	PO	WB								
I2		IF	OF	—	—	PO	PO	PO	PO	PO	WB			
I3			IF	—	—	—	—	—	—	—	OF	PO	WB	
I4				—	—	—	—	—	—	—	IF	OF	PO	WB

Reference: <http://www.cs.iastate.edu/~prabhu/Tutorial/PIPELINE/forward.html>

References



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👍 92 votes

-- Arjun Suresh (332k points)



- Reference: Page 24 <http://www2.cs.siu.edu/~cs401/Textbook/ch3.pdf>

S_1 is needed at time 1 and 5, so its forbidden latency is $5 - 1 = 4$.

S_2 is needed at time 2 and 4, so its forbidden latency is $4 - 2 = 2$.

So, forbidden latency = (2, 4, 0) (0 by default is forbidden)

Allowed latency = (1, 3, 5) (any value more than 5 also).

Collision vector (4, 3, 2, 1, 0) = 10101 which is the initial state as well.

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From initial state we can have a transition after “1” or “3” cycles and we reach new states with collision vectors ($10101 >> 1 + 10101 = 11111$) and ($10101 >> 3 + 10101 = 10111$) respectively.

These 2 becomes states 2 and 3 respectively. For “5” cycles we come back to state 1 itself.

From state 2 (11111), the new collision vector is 11111. We can have a transition only when we see the first 0 from the right. So, here it happens on 5th cycle only which goes to the initial state. (Any transition after 5 or more cycles goes to initial state as we have 5 time slices).

From state 3 (10111), the new collision vector is 10111. So, we can have a transition on 3, which will give (10111 >> 3 + 10101 = 10111) third state itself. For 5, we get the initial state. Thus all the transitions are complete.

State \ Time	1	3	5
1(10101)	2	3	1
2(11111)	-	-	1
3(10111)	-	3	1

So, minimum length cycle is of **length 3** either from 3-3 or from 1-3,3-1.

Not asked in the question, still.

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Pipeline throughput is the number of instructions initiated per unit time.

So, with $MAL = 3$, we have 2 initiations in $1 + 3 = 4$ units of time (one at time unit 1 and another at time unit 4). So,

$$\text{throughput} = \frac{2}{4} = 0.5.$$

Pipeline efficiency is the % of time every stage of the pipeline is being used.

For the given question we can extend the reservation table and taking $MAL = 3$, we can initiate new tasks after every 3 cycles.

So, we can consider the time interval from 4-6 in the below figure. (The red color shows a stage not being used- affects efficiency).

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Time →	1	2	3	4	5	6	7	8	9	10	11
S_1	X			Y	X	×	Z	Y	×	A	Z
S_2		X		X	Y	×	Y	Z		Z	A
S_3			X	×	×	Y			Z		

Here (during cycles 4–6), stage 1 is used $\frac{2}{3}$, stage 2 is used $\frac{2}{3}$ and stage 3 is used $\frac{1}{3}$.

$$\text{So, total stage utilization} = \frac{(2+2+1)}{9} = \frac{5}{9} \text{ and efficiency} = \frac{500}{9}\% = 55.55\%.$$

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For simulation, Reference: <http://www.ecs.umass.edu/ece/koren/architecture/ResTable/SimpRes/>

Similar Question

- <https://gateoverflow.in/77125/advanced-computer-architecture-collision-vector-pipeline>

References

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44 votes

-- Arjun Suresh (332k points)



- ✓ In pipeline ideally $CPI = 1$

So in 1 cycle 1 instruction gets completed

Throughout is instructions in unit time

In pipeline 1, cycle time=max stage delay = 800 psec

In 800 psec, we expect to finish 1 instruction

So, in $\frac{1}{800}$ instructions are expected to be completed, which is also the throughput for pipeline 1.

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Similarly pipeline 2, throughput= $\frac{1}{600}$

Throughput increase in percentage

$$= \frac{\text{new-old}}{\text{old}} \times 100$$

$$= \frac{\frac{1}{600} - \frac{1}{800}}{\frac{1}{800}} \times 100$$

$$= \frac{200}{600} \times 100$$

$$= 33.33\%$$

116 votes

-- Anurag Semwal (6.7k points)



Maximum throughput of a Pipeline i.e in best case without any stalls is equal to Clock Frequency of the pipeline

In first case Clock cycle time = Max Stage Delay = Max(800,500,400 and 300) = 800.

So clock Frequency = $\frac{1}{800}$ (Ignore the units as we have to calculate percentage only)

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In Second Case Clock cycle time = Max(600,350,500,400 and 300) = 600.

So clock Frequency = $\frac{1}{600}$.

Percentage increase in throughput of pipeline = percentage in Clock Frequency

$$= \frac{\left(\frac{1}{600} - \frac{1}{800}\right)}{\frac{1}{800}} \times 100 = 33.33\%$$

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40 votes

-- Mehak Sharma (1.2k points)



- ✓ Answer is 4 GHz.

Given 3 stage pipeline , with 3 GHz processor.

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Given , $e_1 = \frac{3e_2}{4} = 2e_3$

Put $e_1 = 6x$

we get, $e_2 = 8x$, $e_3 = 3x$

Now largest stage time is $8x$.

So, frequency is $\frac{1}{8x}$

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$$\Rightarrow \frac{1}{8x} = 3\text{GHz}$$

$$\Rightarrow \frac{1}{x} = 24 \text{ GHz} \dots (1)$$

Now, we divide e_2 into two stages of $4x$ & $4x$.

New processor has 4 stages -

$6x, 4x, 4x, 3x$.

Now largest stage time is $6x$.

So, new frequency is

$$\frac{1}{6x} = \frac{24}{6} = 4 \text{ GHz (Ans)} \dots \text{from (1)}$$

131 votes

-- Himanshu Agarwal (12.4k points)

1.18.27 Pipelining: GATE CSE 2017 Set 1 | Question: 50 top

<https://gateoverflow.in/118719>



✓ CASE 1

Stages 5, max delay = 22 (after adding buffer delay), number of instructions = 20

CASE 2

Stages 6, (since OF is split), max delay = 14, number of instructions = 20

So, execution time is $(K + N - 1) \times \text{Max delay}$

$$\text{Speed Up} = \frac{528}{350} = 1.508 \text{ (Execution time case 1/Execution time case 2)}$$

So, answer is **1.508**

42 votes

-- sriv_shubham (2.8k points)

1.18.28 Pipelining: GATE CSE 2018 | Question: 50 top

<https://gateoverflow.in/204125>



✓ Total Instruction = 100

Number of stages = 5

In normal case total cycles = $100 + 5 - 1 = 104$ cycles

Now, For PO stage 40 instructions take 3 cycles, 35 take 2 cycles and rest of the 25 take 1 cycle.
That means all other stages are perfectly fine and working with *CPI* (Clock Cycle Per Instruction)= 1

PO stage:

40 instructions take 3 cycles i.e. these instructions are suffering from 2 stall cycle,
35 instructions take 2 cycles i.e. these instructions are suffering from 1 stall cycle,
25 instructions take 1 cycles i.e. these instructions are suffering from 0 stall cycle,

So, extra cycle would be $40 * 2 + 35 * 1 + 25 * 0 = 80 + 35 = 115$ cycle.

Total cycles = $104 + 115 = 219$

114 votes

-- Digvijay (44.9k points)

1.18.29 Pipelining: GATE CSE 2020 | Question: 43 top

<https://gateoverflow.in/333188>



✓ Time taken by non-pipelined processor to finish executing the n instructions : $\frac{5n}{2.5} = 2n$ ns

Now, for pipelined processor,

Execution time for Pipeline = $(K + n - 1) * \text{execution_time}$ where k = no of stages in pipeline, n = no of instructions
Execution time = max(all stages execution time)

$$D_1 = (5 + 100 - 1) * 4 = 416$$

$$D_2 = (8 + 100 - 1) * 2 = 214$$

Time saved using $D_2 = 416 - 214 = 202$

拇指图标 30 votes

-- Manu Thakur (34k points)

1.18.33 Pipelining: GATE IT 2006 | Question: 78 [top](#)

<https://gateoverflow.in/3622>



- ✓ (C) is the correct option for this question:

RAW

1. I1 - I2 (R5)
2. I2 - I3 (R6)
3. I3 - I4 (R5)
4. I4 - I5 (R6)

WAR

1. I2 - I3 (R5)
2. I3 - I4 (R6)

WAW

1. I1 - I3 (R5)
2. I2 - I4 (R6)

拇指图标 51 votes

-- Manu Thakur (34k points)

1.18.34 Pipelining: GATE IT 2006 | Question: 79 [top](#)

<https://gateoverflow.in/3623>



	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
ADD	IF	ID	EX ①	WB								
MUL		IF	ID ①	EX	EX	EX ①	WB					
SUB			IF	—	—	ID ①	EX ①	WB				
DIV						IF	ID ①	EX	EX	EX ①	WB	
STORE							IF	—	—	ID ①	EX	WB

— Stalls

① Operand forwarding from EX-ID using split phase

So, answer is **12**.

Correct Answer: **B**

拇指图标 75 votes

-- Manu Thakur (34k points)

1.18.35 Pipelining: GATE IT 2007 | Question: 6, ISRO2011-25 [top](#)

<https://gateoverflow.in/3437>



- ✓ For non pipeline processor we have n instruction and each instruction take 12 cycle so total $12n$ instruction.

For pipeline processor we have each stage strict to $6ns$ so time to complete

the n instruction is $6 \times 6 + (n - 1) \times 6$.

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$$\lim_{n \rightarrow \infty} \frac{12n}{36 + (n - 1) \times 6} = \frac{12}{6} = 2.$$

Correct Answer: **B**

Like 62 votes

-- Arpit Dhuriya (2.9k points)

1.18.36 Pipelining: GATE IT 2008 | Question: 40 top

https://gateoverflow.in/3350



- Here we have to keep in mind the phrase:

A non-pipelined single cycle processor

This signifies that instruction in a non pipelined scenario is incurring only a single cycle to execute entire instruction. Hence no concept of stage comes in case of single cycle non pipelined system.

The cycle time can be calculated from clock frequency given in non pipelined system = 100 MHz

$$\text{Therefore clock cycle time in non pipelined system} = \frac{1}{(100 \times 10^6)} \text{ sec}$$

$$= 10 \text{ ns}$$

Now cycle time in pipelined system = max(stage delay + interface delay)

$$= 2.5 + 0.5 = 3 \text{ ns}$$

Therefore,

$$\text{Speedup} = \frac{CPI_{\text{non pipeline}} \times \text{Cycle time}_{\text{non pipeline}}}{(CPI_{\text{pipeline}} \times \text{Cycle time}_{\text{pipeline}})}$$
$$= \frac{1 \times 10}{(1 \times 3)} = 3.33$$

[Since in case of non pipeline we have single cycle processor, so $CPI_{\text{non pipeline}} = 1$ and CPI_{pipeline} by default = 1]

Hence, (C) is the correct answer.

Like 63 votes

-- HABIB MOHAMMAD KHAN (67.5k points)

1.19

Runtime Environments (2) top

1.19.1 Runtime Environments: GATE CSE 2001 | Question: 1.10, UGCNET-Dec2012-III: 36 top

https://gateoverflow.in/703



Suppose a processor does not have any stack pointer registers, which of the following statements is true?

- A. It cannot have subroutine call instruction
- B. It cannot have nested subroutines call
- C. Interrupts are not possible
- D. All subroutine calls and interrupts are possible

gate2001-cse co-and-architecture normal ugcnetdec2012iii runtime-environments

Answer

1.19.2 Runtime Environments: GATE CSE 2008 | Question: 37, ISRO2009-38 top

https://gateoverflow.in/448



The use of multiple register windows with overlap causes a reduction in the number of memory accesses for:

- I. Function locals and parameters
 - II. Register saves and restores
 - III. Instruction fetches
- A. I only

- B. *II* only
 C. *III* only
 D. *I, II and III*

gate2008-cse co-and-architecture normal isro2009 runtime-environments

Answer 

Answers: Runtime Environments

1.19.1 Runtime Environments: GATE CSE 2001 | Question: 1.10, UGCNET-Dec2012-III: 36 [top](#) 

<https://gateoverflow.in/703> 

- ✓ A stack pointer is a small register that stores the address of the **last program request in a stack**.

And a nested function (or nested procedure or subroutine) is a function which is defined **within another function**, the enclosing function. So if there is no stack pointer register then No nested subroutine call possible, hence option B is correct.

classroom.gateoverflow.in  40 votes

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classroom.gateoverver  -- Bikram (58.4k points)

1.19.2 Runtime Environments: GATE CSE 2008 | Question: 37, ISRO2009-38 [top](#) 

<https://gateoverflow.in/448> 

- ✓ I. Functions locals and parameters
 this is true because overlapped registers eliminates the need for memory accesses. we here got to use registers instead.
- II. Register saves and restores
 this is false bc we need to see where memory accesses are reduced here before also we were using register as it says
 c Register saves.. later also (i.e. after using multiple register windows) registers will be referred. So NO memory accesses ver are reduced here.
- III. Instruction fetches
 it has nothing to do with reduction in memory accesses.

Hence, **option (A)** is correct.

38 votes

-- Amar Vashishth (25.2k points)

1.20

Speedup (2) [top](#) 

1.20.1 Speedup: GATE CSE 2014 Set 1 | Question: 55 [top](#) 

<https://gateoverflow.in/1935> 

Consider two processors P_1 and P_2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P_2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P_1 . If the clock frequency of P_1 is 1GHz, then the clock frequency of P_2 (in GHz) is _____. [tests.gatecse.in](#)

gate2014-cse-set1 co-and-architecture numerical-answers normal speedup

Answer 

1.20.2 Speedup: GATE IT 2004 | Question: 50 [top](#) 

<https://gateoverflow.in/790> 

In an enhancement of a design of a CPU, the speed of a floating point unit has been increased by 20% and the speed of a fixed point unit has been increased by 10%. What is the overall speedup achieved if the ratio of the number of floating point operations to the number of fixed point operations is 2 : 3 and the floating point operation used to take twice the time taken by the fixed point operation in the original design? [tests.gatecse.in](#)

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- A. 1.155
 B. 1.185
 C. 1.255
 D. 1.285

gate2004-it normal co-and-architecture speedup

Answer 

Answers: Speedup



- ✓ CPU TIME (T) = No. of Instructions (I) x No. of Cycles Per Instruction (c) x Cycle Time (t)

OR

$$\text{CPU TIME (T)} = \frac{\text{No. of Instructions (I)} \times \text{No. of Cycles Per Instruction (c)}}{\text{Clock frequency (f)}}$$

$$\rightarrow T = I_c \times CPI \times F^{-1}$$

$$\rightarrow \frac{T \times F}{CPI} = I_c$$

P_1 & P_2 executing same instruction set So,
No. of Instructions same for both = $I_1 = I_2 = I$

If P_1 takes T_1 time,

$$\rightarrow T_2 = 0.75 \times T_1 \rightarrow \frac{T_2}{T_1} = 0.75$$

If P_1 incurs C_1 clock cycles per instruction,

$$\rightarrow C_2 = 1.2 \times C_1 \rightarrow \frac{C_2}{C_1} = 1.2$$

Since I is same for both,

$$\rightarrow \frac{(f_1 \times T_1)}{c_1} = \frac{(f_2 \times T_2)}{c_2} \text{ and } f_1 = 1 \text{ GHz}$$

$$\rightarrow F_2 = \left(\frac{C_2}{C_1} \right) \times \left(\frac{T_1}{T_2} \right) \times F_1$$

$$= \frac{1.2 \times 1 \text{ GHz}}{0.75} = 1.6 \text{ GHz}$$

Hence, the clock frequency of P_2 is = 1.6 GHz.

85 votes

-- Suraj Kaushal (273 points)

Execution time (T) = CPI * #instructions * time for a clock
= CPI * #instructions / clock frequency (F)

Given P1 and P2 execute the same set of instructions and

$T_2 = 0.75 T_1$,

$CPI_2 = 1.2 CPI_1$ and

$F_1 = 1 \text{ GHz}$.

So,

$$\frac{T_1}{CPI_1} \times F_1 = \frac{T_2}{CPI_2} \times F_2$$

$$\frac{T_1}{CPI_1} \times 1 \text{ GHz} = \frac{0.75 T_1}{1.2 CPI_1} \times F_2$$

$$\implies F_2 = \frac{1.2}{0.75} \text{ GHz}$$

$$= 1.6 \text{ GHz}$$

37 votes

-- Arjun Suresh (332k points)



✓ SpeedUp = $\frac{\text{Original time taken}}{\text{new time taken}}$

Let x be the time for a fixed point operation,

$$\begin{aligned}\text{Original time taken} &= \frac{(3x + 2 \times 2x)}{5} = \frac{7x}{5} \\ \text{New time taken} &= \frac{\left(\frac{3x}{1.1} + \frac{4x}{1.2}\right)}{5} = \frac{8x}{1.32 \times 5} \\ \text{So, SpeedUp} &= \frac{7 \times 1.32}{8} = 1.155\end{aligned}$$

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Correct Answer: A

56 votes

-- gatecse (63.3k points)

1.21

Virtual Memory (3) top

1.21.1 Virtual Memory: GATE CSE 1991 | Question: 03,iii top

<https://gateoverflow.in/517>



The total size of address space in a virtual memory system is limited by:

- A. the length of MAR
- B. the available secondary storage
- C. the available main memory
- D. all of the above
- E. none of the above

gate1991 co-and-architecture virtual-memory normal multiple-selects

Answer

1.21.2 Virtual Memory: GATE CSE 2004 | Question: 47 top

<https://gateoverflow.in/318>



Consider a system with a two-level paging scheme in which a regular memory access takes 150 nanoseconds, and servicing a page fault takes 8 milliseconds. An average instruction takes 100 nanoseconds of CPU time, and two memory accesses. The TLB hit ratio is 90%, and the page fault rate is one in every 10,000 instructions. What is the effective average instruction execution time?

- A. 645 nanoseconds
- B. 1050 nanoseconds
- C. 1215 nanoseconds
- D. 1230 nanoseconds

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gate2004-cse co-and-architecture virtual-memory normal

Answer

1.21.3 Virtual Memory: GATE CSE 2008 | Question: 38 top

<https://gateoverflow.in/449>



In an instruction execution pipeline, the earliest that the data TLB (Translation Lookaside Buffer) can be accessed is:

- A. before effective address calculation has started
- B. during effective address calculation
- C. after effective address calculation has completed
- D. after data cache lookup has completed

gate2008-cse co-and-architecture virtual-memory normal

Answer

Answers: Virtual Memory



- ✓ classroom.gateoverflow.in
The answer is (A) and (B).

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Virtual memory concept is independent of size of main memory and depends only on the availability of the secondary storage.

MAR holds the address generated by CPU and this obviously limits the total virtual memory address space.

Like 34 votes

-- Kalpana Bhargav (2.5k points)



- ✓ Average Instruction execution time

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= Average CPU execution time + Average time for getting data(instruction operands from memory for each instruction)

= Average CPU execution time
+ Average address translation time for each instruction
+ Average memory fetch time for each instruction
+ Average page fault time for each instruction

$$= 100 + 2 \left((0.9(0) + 0.1(2 \times 150)) \right) + 2 \times 150 + \frac{1}{10000} \times 8 \times 10^6$$

(Page Fault Rate per 10,000 instruction is directly given in question.Two memory accesses per instruction and hence we need 2 × address translation time for average instruction execution time)

[TLB access time assumed as 0 and 2 page tables need to be accessed in case of TLB miss as the system uses two-level paging]

$$= 100 + 60 + 300 + 800$$

$$= 1260 \text{ ns}$$

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Like 140 votes

-- Arjun Suresh (332k points)



- ✓ C is the answer here.

Effective address is the address after applying the addressing mode like indexed, immediate etc. But this resulting address is still the virtual address, the physical address is invisible to the CPU and will be given only by the MMU when given the corresponding virtual address. Virtual address is given for TLB look up. TLB -Translation Lookaside Buffer, here Lookaside means during Address translation (from Virtual to Physical). But virtual address must be there before we look into TLB.

https://gateoverflow.in/?qa=blob&qa_blobid=15279338060050073946

References



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Answer Keys

1.1.1	C	1.1.2	N/A	1.1.3	N/A	1.1.4	N/A	1.1.5	B
1.1.6	D	1.1.7	A;B;C;D	1.1.8	C	1.1.9	A	1.1.10	B

1.1.11	C	1.1.12	B	1.1.13	C	1.1.14	C	1.1.15	D
1.1.16	D	1.1.17	D	1.1.18	D	1.2.1	N/A	1.2.2	N/A
1.2.3	22	1.2.4	180	1.2.5	N/A	1.2.6	D	1.2.7	D
1.2.8	61.25	1.2.9	N/A	1.2.10	B	1.2.11	B	1.2.12	N/A
1.2.13	N/A	1.2.14	C	1.2.15	A	1.2.16	A	1.2.17	D
1.2.18	C	1.2.19	B	1.2.20	D	1.2.21	C	1.2.22	A
1.2.23	A	1.2.24	D	1.2.25	B	1.2.26	C	1.2.27	D
1.2.28	C	1.2.29	C	1.2.30	D	1.2.31	C	1.2.32	A
1.2.33	A	1.2.34	A	1.2.35	D	1.2.36	D	1.2.37	20
1.2.38	1.68	1.2.39	14	1.2.40	A	1.2.41	24	1.2.42	30
1.2.43	0.05	1.2.44	14	1.2.45	A	1.2.46	4.7 : 4.8	1.2.47	18
1.2.48	B	1.2.49	D	1.2.50	160	1.2.51	13.49:13.59	1.2.52	B
1.2.53	17 : 17	1.2.54	2 : 2	1.2.55	A	1.2.56	C	1.2.57	B
1.2.58	C	1.2.59	C	1.2.60	A	1.2.61	B	1.2.62	D
1.2.63	A	1.3.1	A;B;C;D	1.3.2	D	1.4.1	N/A	1.4.2	B
1.5.1	76	1.6.1	B	1.7.1	B	1.7.2	B	1.8.1	N/A
1.8.2	D	1.8.3	B	1.8.4	B	1.8.5	28	1.8.6	C
1.9.1	D	1.9.2	B	1.9.3	A	1.9.4	456	1.9.5	80000 : 80000
1.9.6	C	1.10.1	A	1.11.1	False	1.11.2	N/A	1.11.3	C
1.11.4	C	1.11.5	A	1.11.6	-16.0	1.11.7	1.87 : 1.88	1.12.1	N/A
1.12.2	256	1.12.3	True	1.12.4	16383	1.12.5	500	1.12.6	32
1.12.7	14	1.13.1	D	1.13.2	B	1.13.3	A	1.13.4	A
1.13.5	B	1.13.6	C	1.13.7	C	1.14.1	True	1.14.2	True
1.14.3	False	1.14.4	A	1.14.5	1.4 : 1.5	1.14.6	B	1.14.7	B
1.15.1	N/A	1.15.2	N/A	1.15.3	N/A	1.15.4	B	1.15.5	A
1.15.6	D	1.15.7	B	1.15.8	C	1.15.9	B	1.15.10	D
1.15.11	A	1.15.12	C	1.15.13	D	1.15.14	D	1.15.15	16
1.15.16	50 : 50	1.15.17	D	1.15.18	C	1.15.19	A	1.16.1	31
1.16.2	59 : 60	1.17.1	N/A	1.17.2	C	1.17.3	C	1.17.4	B
1.17.5	D	1.17.6	A	1.17.7	D	1.17.8	A	1.17.9	D
1.17.10	B	1.17.11	D	1.17.12	D	1.18.1	15	1.18.2	B
1.18.3	N/A	1.18.4	N/A	1.18.5	D	1.18.6	D	1.18.7	C
1.18.8	A	1.18.9	C	1.18.10	B	1.18.11	B	1.18.12	A
1.18.13	D	1.18.14	B	1.18.15	B	1.18.16	B	1.18.17	C

1.18.18	B	1.18.19	4	1.18.20	1.50 : 1.60	1.18.21	C	1.18.22	3.2
1.18.23	13	1.18.24	3	1.18.25	33.0 : 34.0	1.18.26	4	1.18.27	1.50 : 1.51
1.18.28	219	1.18.29	2.161:2.169	1.18.30	17160 : 17160	1.18.31	C	1.18.32	B
1.18.33	C	1.18.34	B	1.18.35	B	1.18.36	C	1.19.1	X
1.19.2	A	1.20.1	1.6	1.20.2	A	1.21.1	A;B	1.21.2	D

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Concept of layering.OSI and TCP/IP Protocol Stacks; Basics of packet, circuit and virtual circuit-switching; Data link layer: framing, error detection, Medium Access Control, Ethernet bridging; Routing protocols: shortest path, flooding, distance vector and link state routing; Fragmentation and IP addressing, IPv4, CIDR notation, Basics of IP support protocols (ARP, DHCP, ICMP), Network Address Translation (NAT); Transport layer: flow control and congestion control, UDP, TCP, sockets; Application layer protocols: DNS, SMTP, HTTP, FTP, Email.

Mark Distribution in Previous GATE

Year	2021-1	2021-2	2020	2019	2018	2017-1	2017-2	2016-1	2016-2	Minimum	Average	Maximum
1 Mark Count	1	1	2	1	3	2	3	2	3	1	2	3
2 Marks Count	4	3	2	4	2	3	1	4	3	1	2.8	4
Total Marks	9	7	6	9	7	8	5	10	9	5	7.7	10

2.1

Application Layer Protocols (10) [top ↴](#)2.1.1 Application Layer Protocols: GATE CSE 2008 | Question: 14, ISRO2016-74 [top ↴](#)

tests.gatecse.in goclasses.in tests.gatecse.in What is the maximum size of data that the application layer can pass on to the TCP layer below?

- A. Any size
- B. 2^{16} bytes - size of TCP header
- C. 2^{16} bytes
- D. 1500 bytes

gate2008-cse easy computer-networks application-layer-protocols isro2016

Answer

2.1.2 Application Layer Protocols: GATE CSE 2011 | Question: 4 [top ↴](#)

tests.gatecse.in goclasses.in tests.gatecse.in Consider the different activities related to email.

- m_1 : Send an email from mail client to mail server
- m_2 : Download an email from mailbox server to a mail client
- m_3 : Checking email in a web browser

Which is the application level protocol used in each activity?

- A. m_1 : HTTP m_2 : SMTP m_3 : POP
- B. m_1 : SMTP m_2 : FTP m_3 : HTTP
- C. m_1 : SMTP m_2 : POP m_3 : HTTP
- D. m_1 : POP m_2 : SMTP m_3 : IMAP

gate2011-cse computer-networks application-layer-protocols easy

Answer

2.1.3 Application Layer Protocols: GATE CSE 2012 | Question: 10 [top ↴](#)

tests.gatecse.in goclasses.in tests.gatecse.in The protocol data unit (PDU) for the application layer in the Internet stack is:

- A. Segment
- B. Datagram
- C. Message
- D. Frame

gate2012-cse computer-networks application-layer-protocols easy

Answer



Which of the following is/are example(s) of stateful application layer protocol?

- i. HTTP
- ii. FTP
- iii. TCP
- iv. POP3

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 A. (i) and (ii) only
 B. (ii) and (iii) only
 C. (ii) and (iv) only
 D. (iv) only

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gate2016-cse-set1 computer-networks application-layer-protocols normal

[Answer](#)



Which of the following protocol pairs can be used to send and retrieve e-mails (in that order)?

- A. IMAP POP3
- B. SMTP, POP3
- C. SMTP MIME
- D. IMAP, SMTP

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gate2019-cse computer-networks application-layer-protocols

[Answer](#)



Assume that you have made a request for a web page through your web browser to a web server. Initially the browser cache is empty. Further, the browser is configured to send HTTP requests in non-persistent mode. The web page contains text and five very small images. The minimum number of TCP connections required to display the web page completely in your browser is _____.

gate2020-cse numerical-answers computer-networks application-layer-protocols

[Answer](#)



Consider the three commands : PROMPT, HEAD and RCPT. Which of the following options indicate a correct association of these commands with protocols where these are used?

- A. HTTP, SMTP, FTP
- B. FTP, HTTP, SMTP
- C. HTTP, FTP, SMTP
- D. SMTP, HTTP, FTP

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gate2005-it computer-networks application-layer-protocols normal

[Answer](#)



Assume that "host1.mydomain.dom" has an IP address of 145.128.16.8. Which of the following options would be most appropriate as a subsequence of steps in performing the reverse lookup of 145.128.16.8 ? In the following options "NS" is an abbreviation of "nameserver".

- A. Query a NS for the root domain and then NS for the "dom" domains
- B. Directly query a NS for "dom" and then a NS for "mydomain.dom" domains
- C. Query a NS for in-addr.arpa and then a NS for 128.145.in-addr.arpa domains
- D. Directly query a NS for 145.in-addr.arpa and then a NS for 128.145.in-addr.arpa domains

Answer**2.1.9 Application Layer Protocols: GATE IT 2006 | Question: 18**<https://gateoverflow.in/3557>

HELO and PORT, respectively, are commands from the protocols:

- A. FTP and HTTP
- B. TELNET and POP3
- C. HTTP and TELNET
- D. SMTP and FTP

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Answer**2.1.10 Application Layer Protocols: GATE IT 2008 | Question: 20**<https://gateoverflow.in/3280>

Provide the best matching between the entries in the two columns given in the table below:

I.	Proxy Server	a.	Firewall
II.	Kazaa, DC++	b.	Caching
III.	Slip	c.	P2P
IV.	DNS	d.	PPP

- A. I-a, II-d, III-c, IV-b
- B. I-b, II-d, III-c, IV-a
- C. I-a, II-c, III-d, IV-b
- D. I-b, II-c, III-d, IV-a

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Answer**Answers: Application Layer Protocols****2.1.1 Application Layer Protocols: GATE CSE 2008 | Question: 14, ISRO2016-74**<https://gateoverflow.in/412>**✓ OPTION A**

Its transport layers responsibility to divide data into fragments/ packets. Application layer need not worry about it.

Like 52 votes

-- Desert_Warrior (6k points)

2.1.2 Application Layer Protocols: GATE CSE 2011 | Question: 4<https://gateoverflow.in/2106>**✓ Answer is (C)**

Sender/Client send mail from client mailbox to server mail box with the help of SMTP protocol whereas Receiver or Server retrieve the mail from its mail box to reading using POP3 protocol.

When we want to take the help process to see email in browser in that case we HTTP. Because It creates beautiful page of mailbox with the help of process.

Like 29 votes

-- Paras Singh (8.9k points)

2.1.3 Application Layer Protocols: GATE CSE 2012 | Question: 10<https://gateoverflow.in/42>**✓ (C) Message is the answer.**

For Application, Presentation and Session layers, the PDU is message

For Transport layer, PDU is segment for TCP and datagram for UDP

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For Network layer, PDU is packet

For Datalink layer, PDU is frames

For physical layer, PDU is stream of bits

73 votes

-- gatecse (63.3k points)

2.1.4 Application Layer Protocols: GATE CSE 2016 Set 1 | Question: 25 [top](#)

<https://gateoverflow.in/39628>



✓ **Answer is (C) part**

Stateless protocol is a [communications protocol](#) in which no information is retained by either sender or receiver. (Note: The remembered information is called as the state)

HTTP([Stateless | Application Layer | Uses TCP \(80\)](#)) - No information is maintained. If in some case state maintenance is required then cookies are used. Now HTTPS is HTTP over a secure connection So it is also stateless.

FTP ([Stateful | Application Layer | Uses TCP \(20 and 21\)](#)) server that conducts an interactive session with the user. During the session, a user is provided a means to be authenticated and set various variables (working directory, transfer mode), all stored on the server as part of the user's state.

TCP ([Stateful / Transport Layer](#)) various information related to connection is maintained.

BGP ([Stateful / Application Layer / Uses TCP](#)) Finite state Automata is used to describe the state.

POP3 ([Stateful / Application Layer / Uses TCP\(110\)](#))

In General if [some authorization is required then stateful design is used](#).

Refer ->

- [Link 1](#)
- [Link 2](#)

References

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55 votes

-- Chhotu Ram Chauhan (12k points)



2.1.5 Application Layer Protocols: GATE CSE 2019 | Question: 16 [top](#)

<https://gateoverflow.in/302832>



✓ Simple Mail Transfer Protocol (SMTP) is the standard protocol for [sending emails](#) across the Internet.

IMAP and POP3 are the Internet mail protocols used for [retrieving emails](#).

MIME allows the users to exchange different(non-ASCII) kinds of data files in an email : audio, video, images, etc

So from the given options, [option B is the correct](#) one i.e. SMTP to send e-mail and POP3 to retrieve e-mail.

17 votes

-- NabilSayyad (761 points)

2.1.6 Application Layer Protocols: GATE CSE 2020 | Question: 25 [top](#)

<https://gateoverflow.in/333206>



✓ In HTTP non-persistent connection, each time a request is served by the server, the connection is automatically closed by the server.

So we need 1 connection for web page and 5 for images. Thus, in total we need 6 TCP connections to fetch web page completely.

Answer: 6

20 votes

-- Ayush Upadhyaya (28.4k points)

2.1.7 Application Layer Protocols: GATE IT 2005 | Question: 25 top

<https://gateoverflow.in/3770>



- ✓ **RCPT:** Recipient to, As the name suggests it is used in **SMTP**(Simple Mail Transfer Protocol)

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HEAD: this is used in **HTTP** to get the meta-information, to decide the category of the packet.

PROMPT: turns off prompting for individual files when using the mget or mput commands. Use this command if you do not want to be prompted for each file transfer when transferring multiple files.

Correct Answer: **B**

53 votes

-- nagalla pruthvi (675 points)

2.1.8 Application Layer Protocols: GATE IT 2005 | Question: 77 top

<https://gateoverflow.in/3840>



- ✓ The answer is (C)

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A & B are clearly wrong as we are doing Reverse lookup.

C is the closest answer to the process given in RFC 1033. We need to get NS for in-addr.arpa before doing a query to 8.16.128.145.in-addr.arpa

D is not correct, it is not close to the process.

Relevant stuff from <https://tools.ietf.org/html/rfc1033>

IN-ADDR.ARPA

The structure of names in the domain system is set up in a hierarchical way such that the address of a name can be found by tracing down the domain tree contacting a server for each label of the name. Because of this 'indexing' based on name, there is no easy way to translate a host address back into its host name.

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In order to do the reverse translation easily, a domain was created that uses hosts' addresses as part of a name that then points to the data for that host. In this way, there is now an 'index' to hosts' RRs based on their address. This address mapping domain is called IN-ADDR.ARPA. Within that domain are subdomains for each network, based on network number. Also, for consistency and natural groupings, the 4 octets of a host number are reversed.

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For example, the ARPANET is net 10. That means there is a domain called 10.IN-ADDR.ARPA. Within this domain there is a PTR RR at 51.0.0.10.IN-ADDR that points to the RRs for the host SRI-NIC.ARPA (who's address is 10.0.0.51). Since the NIC is also on the MILNET (Net 26, address 26.0.0.73), there is also a PTR RR at 73.0.0.26.IN-ADDR.ARPA that points to the same RR's for SRI-NIC.ARPA. The format of these special pointers is defined below along with the examples for the NIC.

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The PTR record is used to let special names point to some other location in the domain tree. They are mainly used in the IN-ADDR.ARPA records for translation of addresses to names. PTR's should use official names and not aliases.

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For example, host SRI-NIC.ARPA with addresses 10.0.0.51 and 26.0.0.73 would have the following records in the respective zone files for net 10 and net 26:

```
51.0.0.10.IN-ADDR.ARPA. PTR SRI-NIC.ARPA.  
73.0.0.26.IN-ADDR.ARPA. PTR SRI-NIC.ARPA.
```

References



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36 votes

-- Akash Kanase (36k points)



✓ Answer is D.

References:

- http://en.wikipedia.org/wiki/Simple_Mail_Transfer_Protocol#SMTP_transport_example
- http://en.wikipedia.org/wiki/File_Transfer_Protocol#Protocol_overview

References



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25 votes

-- Rajarshi Sarkar (27.9k points)



✓ Answer is C) I-a, II-c, III-d, IV-b

- Proxy Server \Rightarrow Proxy Server and Firewall can be combined. — a. Firewall
- Kazaa, DC++ \Rightarrow These are P2P application. — c. P2P
- Slip \Rightarrow P2P Slip is a predecessor of PPP. — d. PPP
- DNS \Rightarrow DNS responses are often called — b. Caching

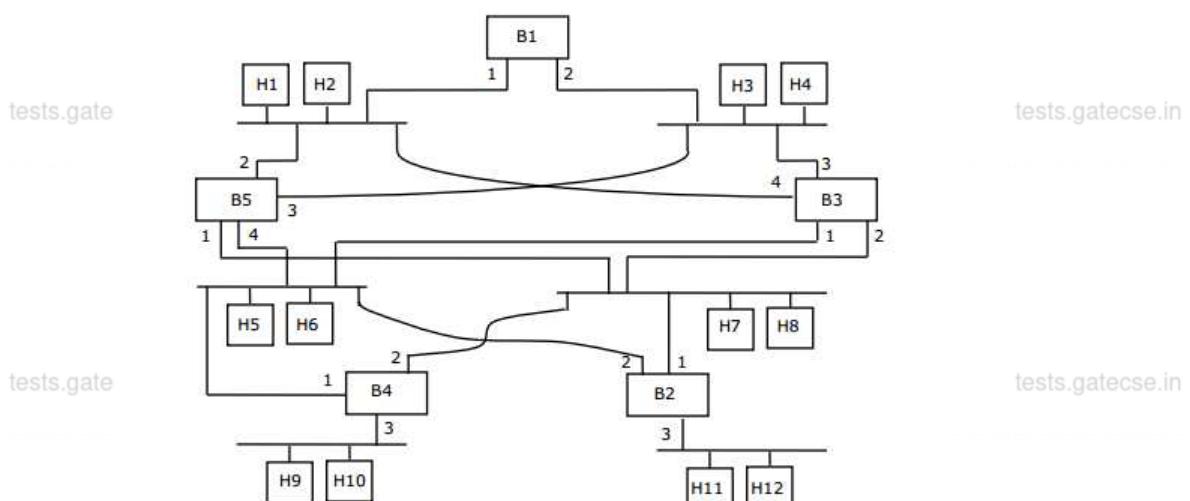
27 votes

-- Akash Kanase (36k points)



Consider the diagram shown below where a number of LANs are connected by (transparent) bridges. In order to avoid packets looping through circuits in the graph, the bridges organize themselves in a spanning tree. First, the root bridge is identified as the bridge with the least serial number. Next, the root sends out (one or more) data units to enable the setting up of the spanning tree of shortest paths from the root bridge to each bridge.

Each bridge identifies a port (the root port) through which it will forward frames to the root bridge. Port conflicts are always resolved in favour of the port with the lower index value. When there is a possibility of multiple bridges forwarding to the same LAN (but not through the root port), ties are broken as follows: bridges closest to the root get preference and between such bridges, the one with the lowest serial number is preferred.



For the given connection of LANs by bridges, which one of the following choices represents the depth first traversal of the spanning tree of bridges?

- A. B1, B5, B3, B4, B2
 B. B1, B3, B5, B2, B4
 C. B1, B5, B2, B3, B4
 D. B1, B3, B4, B5, B2

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Answer ↗

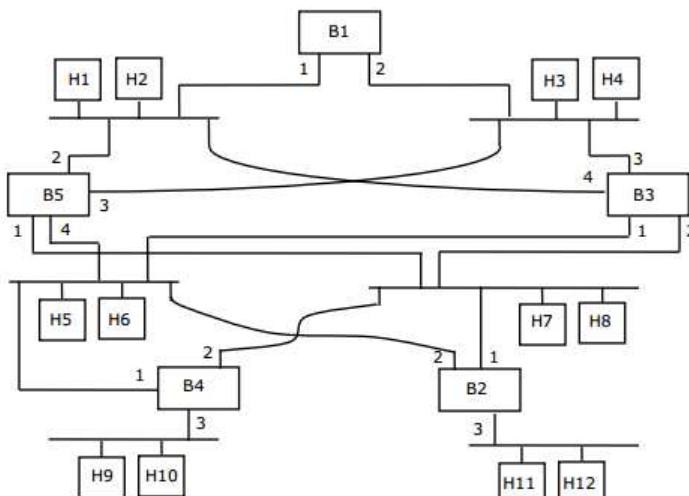
2.2.2 Bridges: GATE CSE 2006 | Question: 83 [top ↵](#)

↪ <https://gateoverflow.in/79790>



Consider the diagram shown below where a number of LANs are connected by (transparent) bridges. In order to avoid packets looping through circuits in the graph, the bridges organize themselves in a spanning tree. First, the root bridge is identified as the bridge with the least serial number. Next, the root sends out (one or more) data units to enable the setting up of the spanning tree of shortest paths from the root bridge to each bridge.

Each bridge identifies a port (the root port) through which it will forward frames to the root bridge. Port conflicts are always resolved in favour of the port with the lower index value. When there is a possibility of multiple bridges forwarding to the same LAN (but not through the root port), ties are broken as follows: bridges closest to the root get preference and between such bridges, the one with the lowest serial number is preferred.



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Consider the spanning tree $B1, B5, B3, B4, B2$ for the given connection of LANs by bridges. Let host $H1$ send out a broadcast ping packet. Which of the following options represents the correct forwarding table on $B3$?

Hosts	Port
H1, H2, H3, H4	3
H5, H6, H9, H10	1
H7, H8, H11, H12	2

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Hosts	Port
H1, H2	4
H3, H4	3
H5, H6	1
H7, H8, H9, H10, H11, H12	2

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Hosts	Port
H3, H4	3
H5, H6, H9, H10	1
H1, H2	4
H7, H8, H11, H12	2

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Hosts	Port
H1, H2, H3, H4	3
H5, H7, H9, H10	1
H7, H8, H11, H12	4

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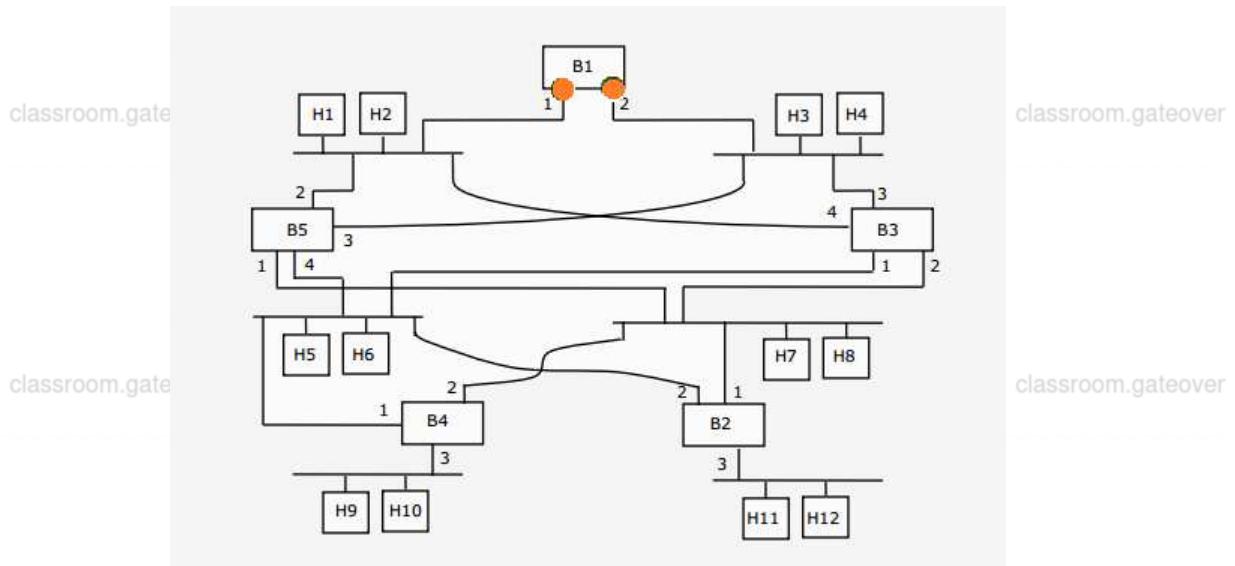
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Answer 

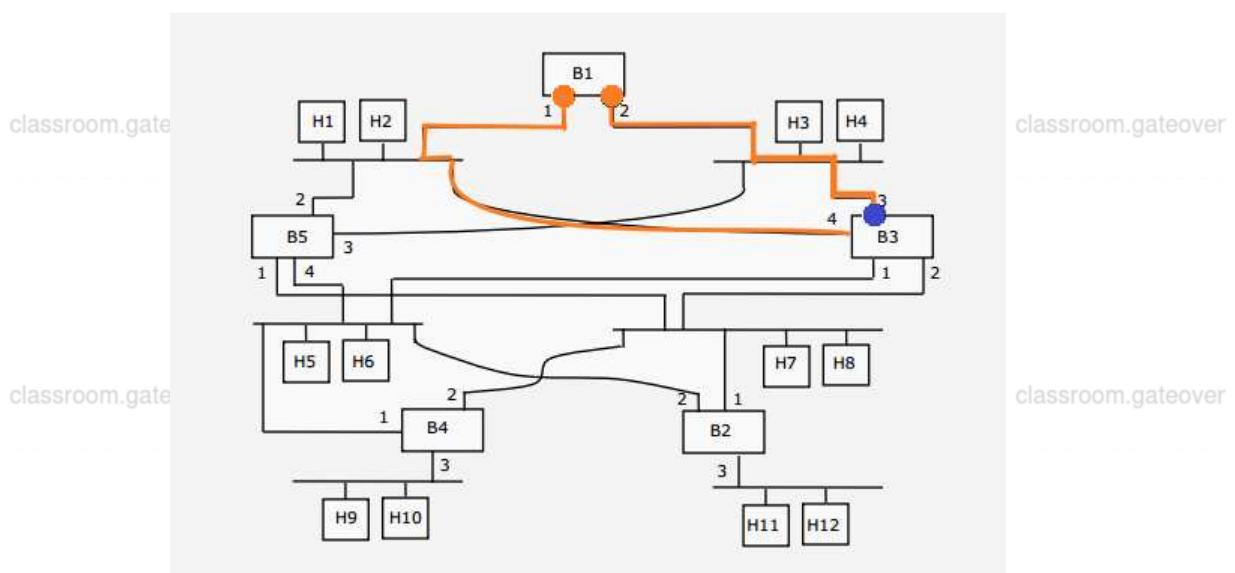
Answers: Bridges

2.2.1 Bridges: GATE CSE 2006 | Question: 82 [top](#)<https://gateoverflow.in/1855>

- First select B_1 as the root bridge. This selection is based on lower serial ID as given in the question.
- All ports of root bridge are **designated ports** and they are in **forwarding state**.



- Every non-root bridge must have a root port. All root ports are placed in **forwarding state**.
- Root port is the port that is closest to the root bridge**
- For example, we observe bridge B_3 .
- It has two ports leading to the root bridge. If we assume bridge-to-bridge cost as 1 unit, both these paths have the same cost. Then we will select the **lower port index** as given in the question as the root port for the bridge B_3 .
- port 3** of B_3 becomes the root port.

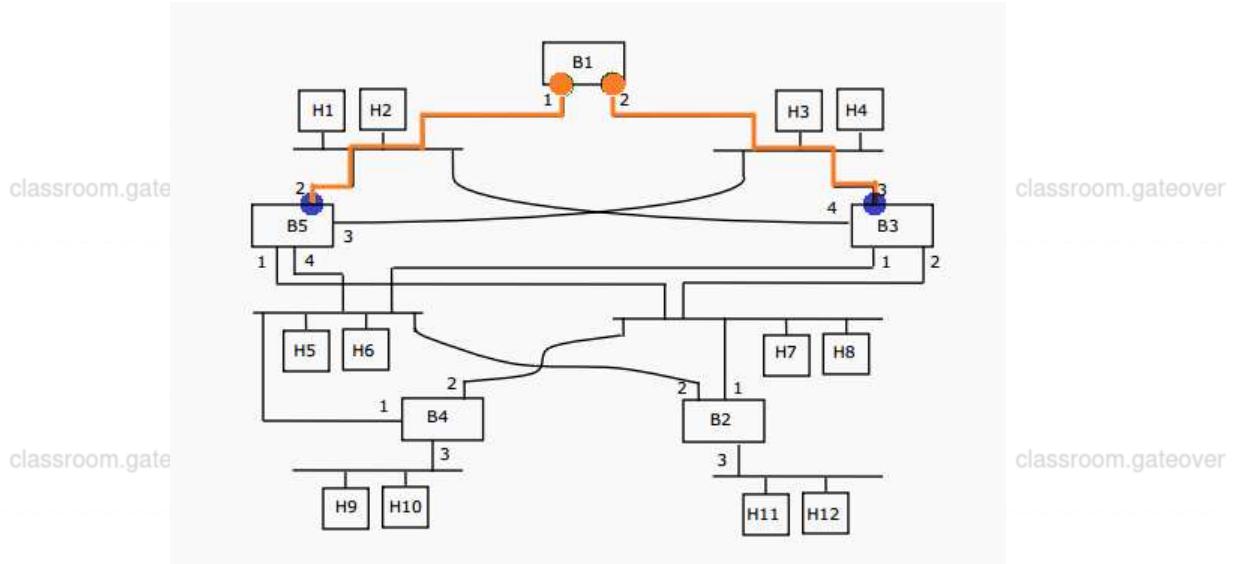


- Using the same logic we will find out the root ports for B_5 also.

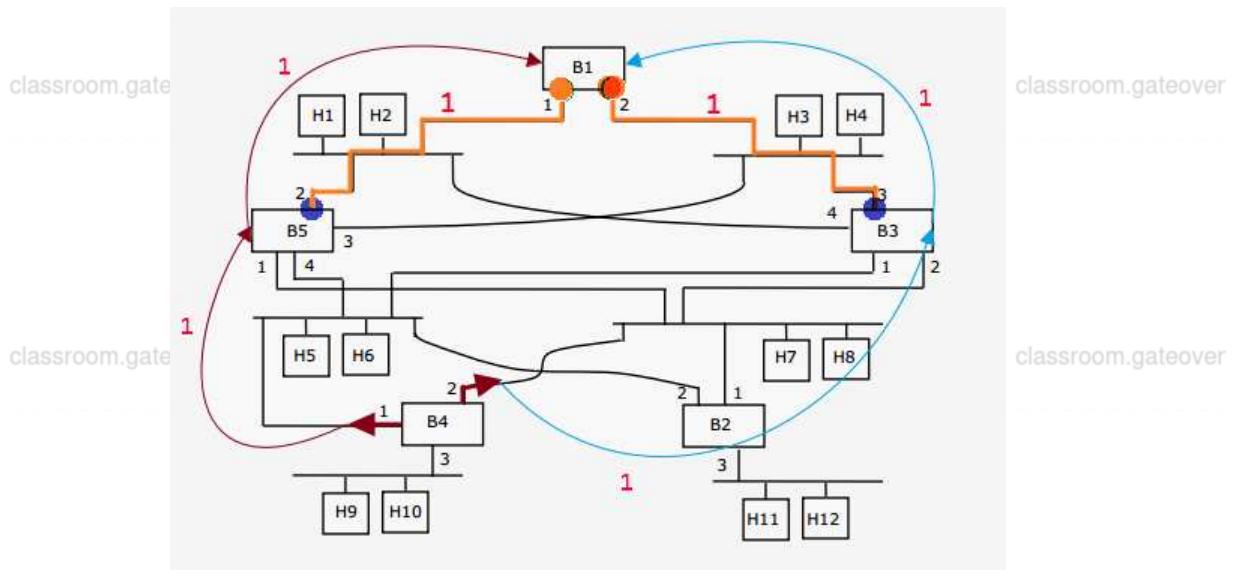
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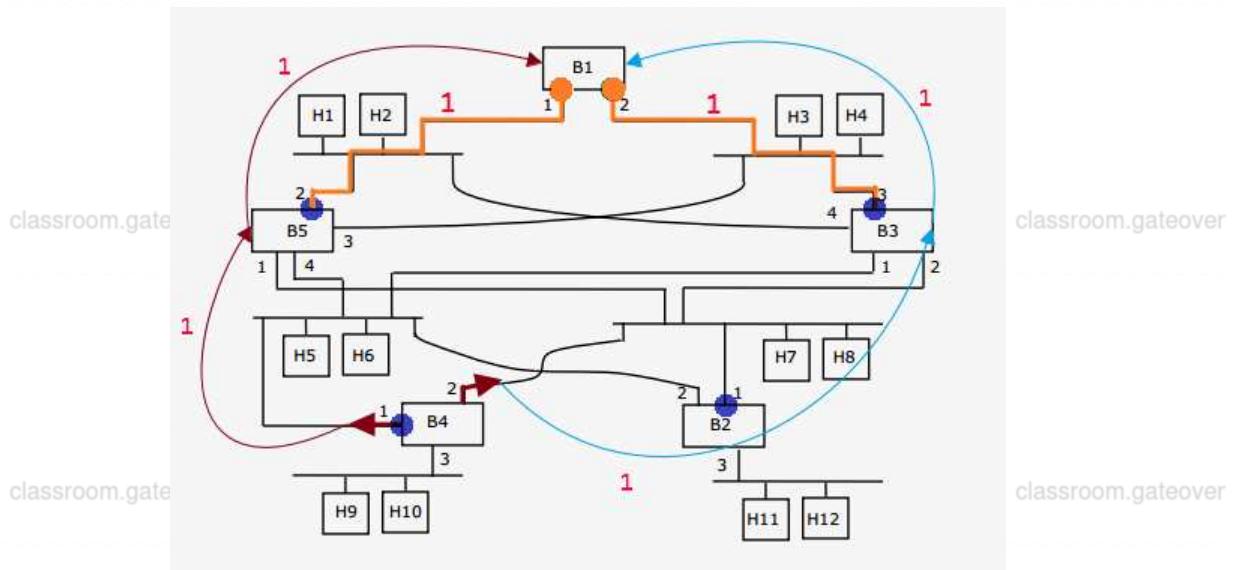
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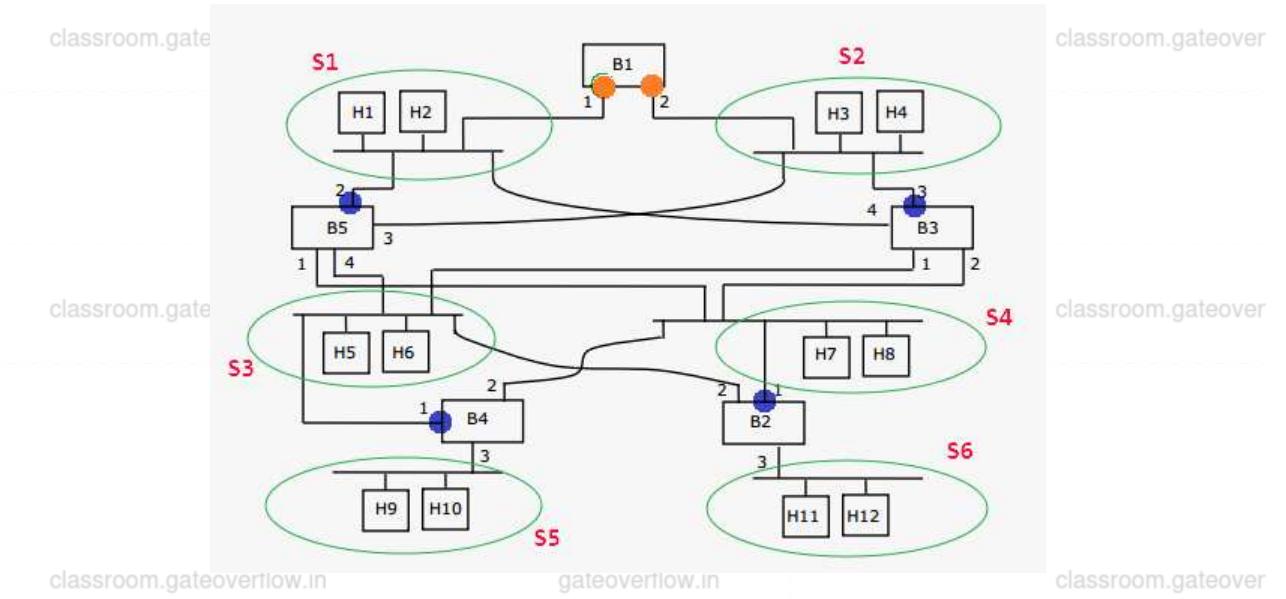
- Coming to B_4 for root port selection.



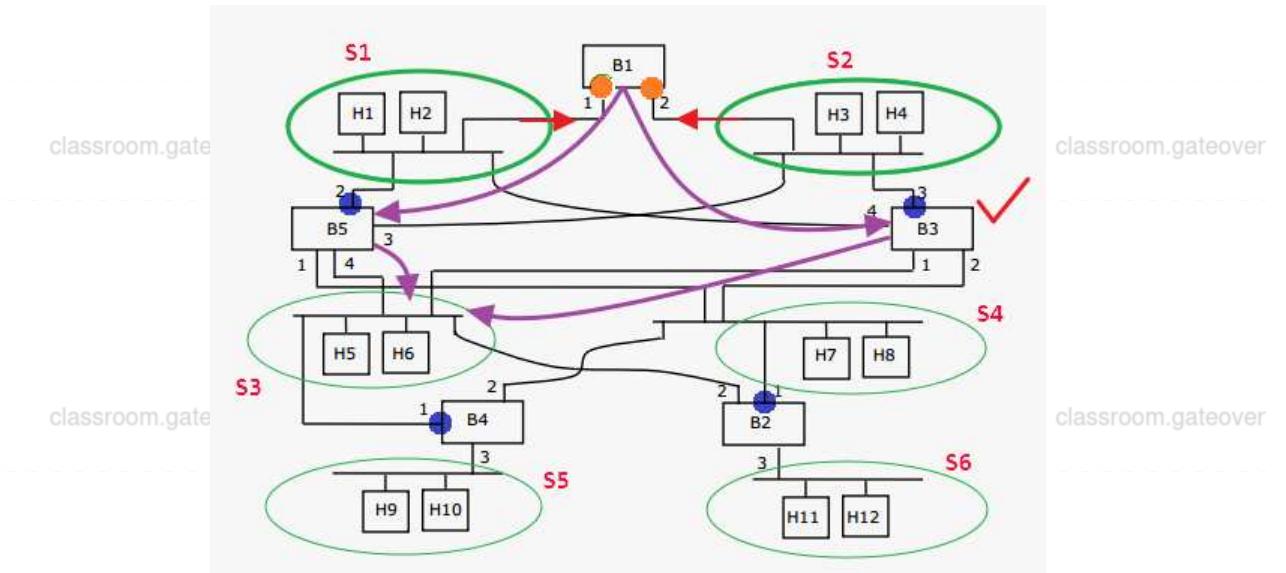
- We have again two different paths with the same cost. We will select port 1 as the root port for B_4 .
- Using the same logic port 1 is selected as root port for B_2 as well.



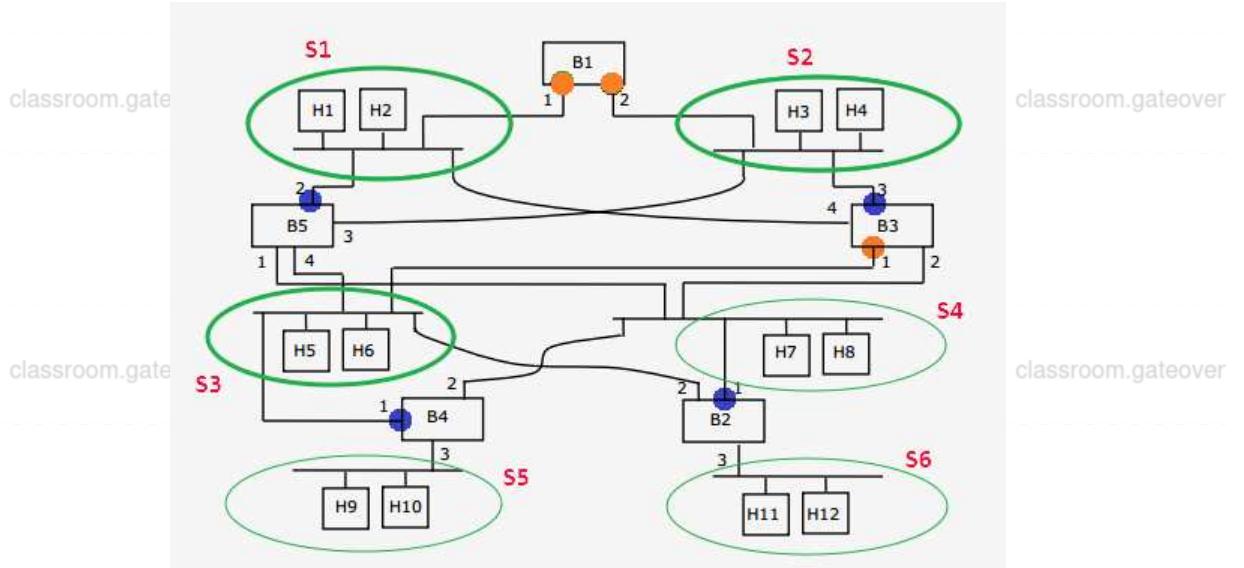
- Now we have to consider the **designated ports**
- The designated ports are the ports responsible for **forwarding traffic onto a network segment**
- We have total 6 network segments or **LAN's**. Each segment will have **one** designated ports.



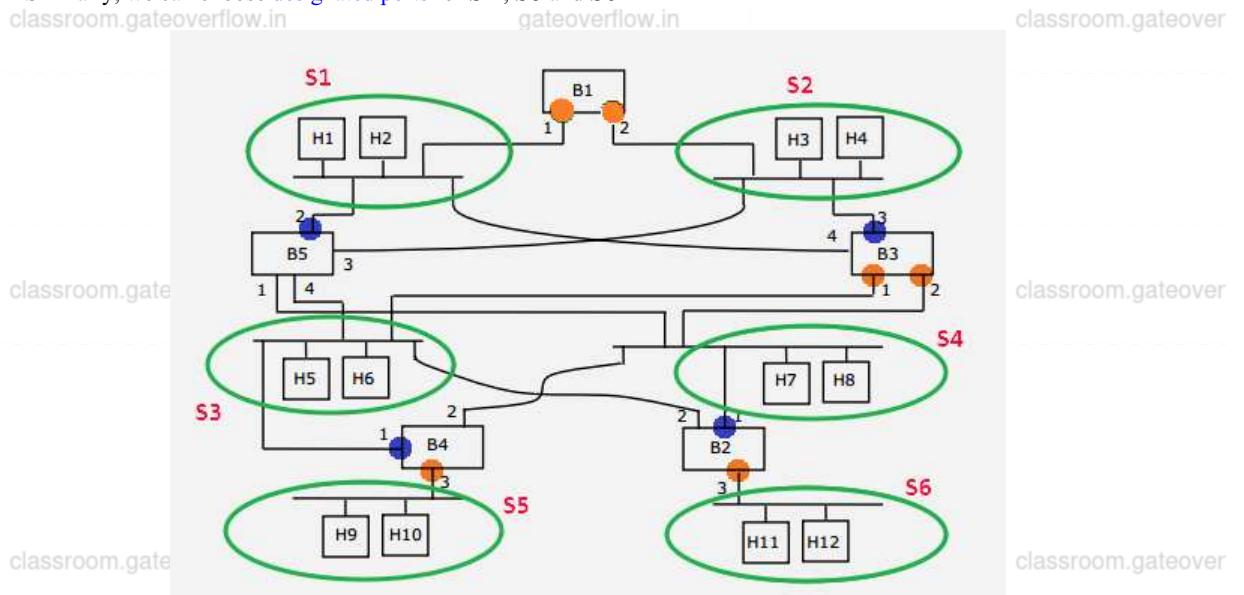
- S1 and S2 are connected to the root bridge itself via two designated ports. So no issue with segments S1 and S2 traffic.
- Let's consider other segments.
- For example S3.



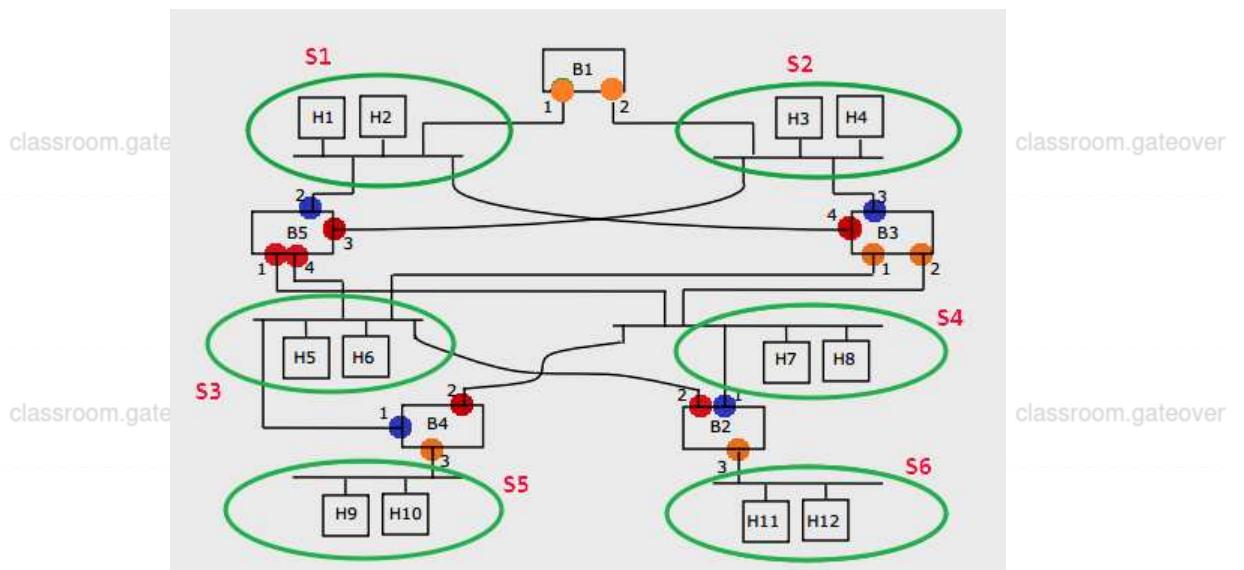
- B2, B3, B4, B5 all can **forward** traffic to this segment S3
- According to the question in this situation, we will consider only those bridges which are **nearer to the root** bridge B1.
- B5 and B3 are both nearer to the root bridge.
- Then we will break this tie by selecting the **lower bridge serial ID** i.e. B3 is selected and designated port is **port 1** of B3 for the segment S3



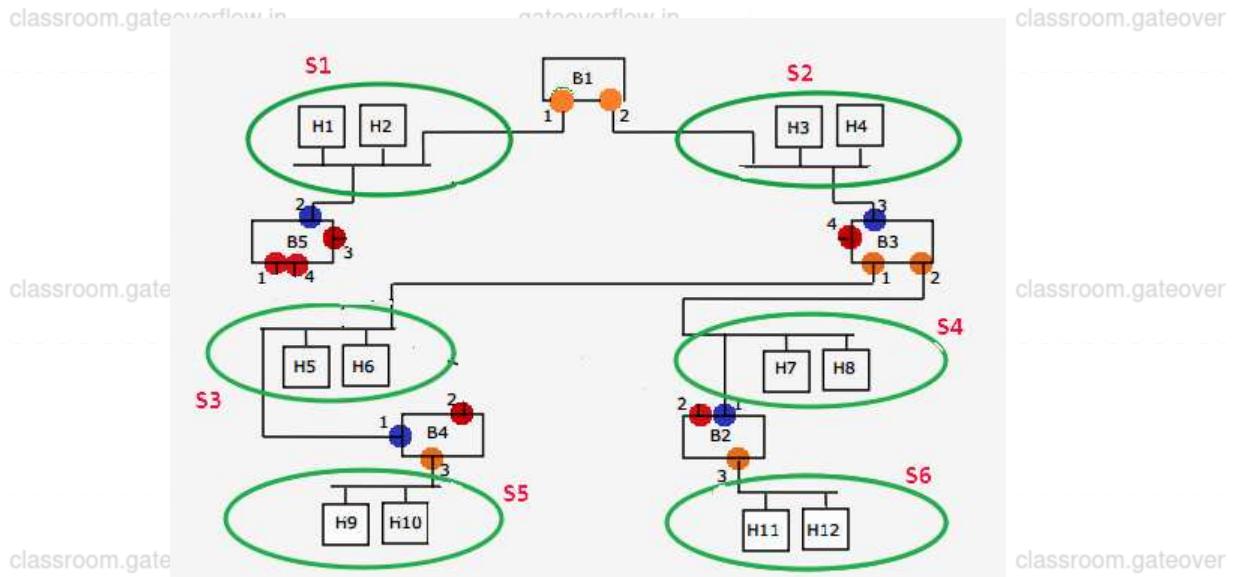
- Similarly, we can choose **designated ports** for S_4 , S_5 and S_6



- Remaining all ports are **blocked ports**.



- This is the final spanning Tree



- DFS traversal will give answer as A



PLEASE check the following two videos. [IITB lectures]

- <https://www.youtube.com/embed/JgApAnUQ1Ss>
- https://www.youtube.com/embed/s_xSIIdBjagc

References



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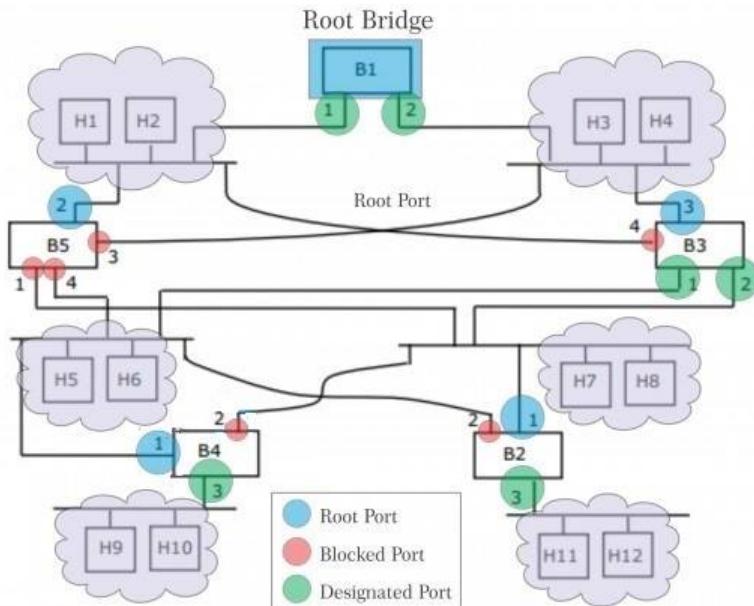
-- Debashish Deka (40.8k points)

2.2.2 Bridges: GATE CSE 2006 | Question: 83 [top](#)

<https://gateoverflow.in/79790>



- ✓ Option is A. see this as we go with options, option A match only with this picture.



👉 25 votes

-- Bikram (58.4k points)

2.3

Communication (3) top ↗2.3.1 Communication: GATE CSE 2012 | Question: 44 top ↗<https://gateoverflow.in/2153>

Consider a source computer (S) transmitting a file of size 10^6 bits to a destination computer (D) over a network of two routers (R_1 and R_2) and three links (L_1 , L_2 , and L_3). L_1 connects S to R_1 ; L_2 connects R_1 to R_2 ; and L_3 connects R_2 to D . Let each link be of length 100 km. Assume signals travel over each link at a speed of 10^8 meters per second. Assume that the link bandwidth on each link is 1 Mbps. Let the file be broken down into 1000 packets each of size 1000 bits. Find the total sum of transmission and propagation delays in transmitting the file from S to D ?

- A. 1005 ms
- B. 1010 ms
- C. 3000 ms
- D. 3003 ms

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Answer ↗

2.3.2 Communication: GATE IT 2007 | Question: 62 top ↗<https://gateoverflow.in/3506>

Let us consider a statistical time division multiplexing of packets. The number of sources is 10. In a time unit, a source transmits a packet of 1000 bits. The number of sources sending data for the first 20 time units is 6, 9, 3, 7, 2, 2, 2, 3, 4, 6, 1, 10, 7, 5, 8, 3, 6, 2, 9, 5 respectively. The output capacity of multiplexer is 5000 bits per time unit. Then the average number of backlogged of packets per time unit during the given period is

- A. 5
- B. 4.45
- C. 3.45
- D. 0

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Answer ↗

2.3.3 Communication: GATE IT 2007 | Question: 64 top ↗<https://gateoverflow.in/3509>

A broadcast channel has 10 nodes and total capacity of 10 Mbps. It uses polling for medium access. Once a node finishes transmission, there is a polling delay of 80 μ s to poll the next node. Whenever a node is polled, it is allowed to transmit a maximum of 1000 bytes. The maximum throughput of the broadcast channel is:

- A. 1 Mbps

- B. 100/11 Mbps
C. 10 Mbps
D. 100 Mbps

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gate2007-it computer-networks communication normal

Answer 

Answers: Communication

2.3.1 Communication: GATE CSE 2012 | Question: 44 [top](#) [https://gateoverflow.in/2153](#)



- ✓ routers are store and forward devices.

$$\text{Propagation time} = \frac{100 \text{ km}}{10^8 \text{ m/s}} = 1 \text{ millisecond}$$

$$\text{Transmission time for a packet} = \frac{1000}{10^6} = 1 \text{ millisecond}$$

Packets will be forwarded in a pipelined manner after the first packet reaches the receiver, in every 1 ms a new one arrives.

now Time taken by packet no 1 to reach destination is :

$$1 \text{ ms (TT at sender)} + 1 \text{ ms (PT from sender to R1)} + 1 \text{ ms (TT at R1)} \\ + 1 \text{ ms (PT from R1 to R2)} + 1 \text{ ms (TT at R2)} + 1 \text{ ms (PT from R2 to destination)} = 6 \text{ ms}$$

So, time for packet,

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$$1000 = 6 \text{ ms} + 999 \text{ ms} \\ = 1005 \text{ ms}$$

Correct Answer: A

 106 votes

-- Digvijay (44.9k points)

First all data needs to be transmitted from source and after all packets transmission from source, just focus on last packet journey, and u will get it.

$$\text{Transmission time for all packets from Source} := \frac{10^6}{1 \times 10^6} = 1 \text{ sec} = 1000 \text{ ms.}$$

(Now the last packet is our main focus, bcoz the moment last packet reaches, all previous are already reached to Destination)

$$\text{Last packet time} = 3 \times \text{propagation time of link} + 2 \times \text{transmission time of router} \quad (\text{Transmission time for source is already included in above 1000 msec}) \\ = (3 \times 1) + (2 \times 1) = 5 \text{ ms}$$

$$\text{Total time} = 1000 + 5 = 1005 \text{ ms}$$

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 65 votes

-- Sachin Mittal (15.8k points)

2.3.2 Communication: GATE IT 2007 | Question: 62 [top](#) [https://gateoverflow.in/3506](#)



- ✓ Answer is B.

Here, we can send at max 5 packets per Time unit $\frac{5000}{1000}$.

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So, whatever which is not sent is backlog.

So,

First Time Unit \Rightarrow 6,

Backlog in First time unit \Rightarrow 6 - 5 \Rightarrow 1 This one gets added to next Time units load

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Second time unit \Rightarrow 9 + 1 (One from Previous Time Unit)

Backlog in Second time Unit = $10 - 5 \Rightarrow 5$ (This one gets added to next Time Units load.)

Total Backlog this way = $1 + 5 + 3 + 5 + 2 + 0 + 0 + 0 + 0 + 1 + 0 + 5 + 7 + 7 + 10 + 8 + 9 + 6 + 10 + 10 = 89$

$$\text{Avg Backlog} = \frac{89}{20} = 4.45$$

The average number of backlogged of packets per time unit during the given period is 4.45.

75 votes

-- Akash Kanase (36k points)

2.3.3 Communication: GATE IT 2007 | Question: 64 top



- ✓ Propagation time is not given so that's negligible here.

$$\text{efficiency} = \frac{\text{transmission time}}{(\text{transmission time} + \text{polling time})}$$

$$Tx = \frac{1000 \text{ bytes}}{10 \text{ Mbps}} = 800 \mu\text{s}.$$

Delay because of polling is = $80 \mu\text{s}$

$$\text{Efficiency of channel, } e = \frac{\text{transmission - delay}}{\text{total - delay}}$$

$$= \frac{800}{800 + 80} = \frac{10}{11}$$

$$\text{Maximum throughput is } \frac{10}{11} \times 10 \text{ Mbps} = \frac{100}{11} \text{ Mbps}$$

Correct Answer: B

64 votes

-- Manu Thakur (34k points)

2.4

Congestion Control (7) top



2.4.1 Congestion Control: GATE CSE 2008 | Question: 56 top

In the slow start phase of the TCP congestion algorithm, the size of the congestion window:

- A. does not increase
- B. increase linearly
- C. increases quadratically
- D. increases exponentially

gate2008-cse computer-networks congestion-control normal

Answer ↗

2.4.2 Congestion Control: GATE CSE 2012 | Question: 45 top



Consider an instance of TCP's Additive Increase Multiplicative Decrease (AIMD) algorithm where the window size at the start of the slow start phase is 2 MSS and the threshold at the start of the first transmission is 8 MSS. Assume that a timeout occurs during the fifth transmission. Find the congestion window size at the end of the tenth transmission.

- A. 8 MSS
- B. 14 MSS
- C. 7 MSS
- D. 12 MSS

gate2012-cse computer-networks congestion-control normal

Answer 

2.4.3 Congestion Control: GATE CSE 2014 Set 1 | Question: 27 [top](#)

<https://gateoverflow.in/1794>



Let the size of congestion window of a TCP connection be 32 KB when a timeout occurs. The round trip time of the connection is 100 msec and the maximum segment size used is 2 KB. The time taken (in msec) by the TCP connection to get back to 32 KB congestion window is _____.

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gate2014-cse-set1 computer-networks tcp congestion-control numerical-answers normal

Answer 

2.4.4 Congestion Control: GATE CSE 2015 Set 1 | Question: 29 [top](#)

<https://gateoverflow.in/8253>



Consider a LAN with four nodes S_1, S_2, S_3 , and S_4 . Time is divided into fixed-size slots, and a node can begin its transmission only at the beginning of a slot. A collision is said to have occurred if more than one node transmits in the same slot. The probabilities of generation of a frame in a time slot by S_1, S_2, S_3 , and S_4 are 0.1, 0.2, 0.3 and 0.4 respectively. The probability of sending a frame in the first slot without any collision by any of these four stations is _____.

gate2015-cse-set1 computer-networks normal numerical-answers congestion-control

Answer 

2.4.5 Congestion Control: GATE CSE 2018 | Question: 14 [top](#)

<https://gateoverflow.in/204088>



Consider the following statements regarding the slow start phase of the TCP congestion control algorithm. Note that $cwnd$ stands for the TCP congestion window and MSS window denotes the Maximum Segments Size:

- The $cwnd$ increases by 2 MSS on every successful acknowledgment
- The $cwnd$ approximately doubles on every successful acknowledgment
- The $cwnd$ increases by 1 MSS every round trip time
- The $cwnd$ approximately doubles every round trip time

Which one of the following is correct?

- A. Only (ii) and (iii) are true
- B. Only (i) and (iii) are true
- C. Only (iv) is true
- D. Only (i) and (iv) are true

gate2018-cse computer-networks tcp congestion-control normal

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Answer 

2.4.6 Congestion Control: GATE CSE 2018 | Question: 55 [top](#)

<https://gateoverflow.in/204130>



Consider a simple communication system where multiple nodes are connected by a shared broadcast medium (like Ethernet or wireless). The nodes in the system use the following carrier-sense based medium access protocol. A node that receives a packet to transmit will carrier-sense the medium for 5 units of time. If the node does not detect any other transmission, it starts transmitting its packet in the next time unit. If the node detects another transmission, it waits until this other transmission finishes, and then begins to carrier-sense for 5 time units again. Once they start to transmit, nodes do not perform any collision detection and continue transmission even if a collision occurs. All transmissions last for 20 units of time. Assume that the transmission signal travels at the speed of 10 meters per unit time in the medium.

Assume that the system has two nodes P and Q , located at a distance d meters from each other. P starts transmitting a packet at time $t = 0$ after successfully completing its carrier-sense phase. Node Q has a packet to transmit at time $t = 0$ and begins to carrier-sense the medium.

The maximum distance d (in meters, rounded to the closest integer) that allows Q to successfully avoid a collision between its proposed transmission and P 's ongoing transmission is _____.

gate2018-cse computer-networks congestion-control numerical-answers

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Answer 



On a TCP connection, current congestion window size is Congestion Window = 4 KB. The window size advertised by the receiver is Advertise Window = 6 KB. The last byte sent by the sender is LastByteSent = 10240 and the last byte acknowledged by the receiver is LastByteAcked = 8192. The current window size at the sender is:

- A. 2048 bytes
- B. 4096 bytes
- C. 6144 bytes
- D. 8192 bytes

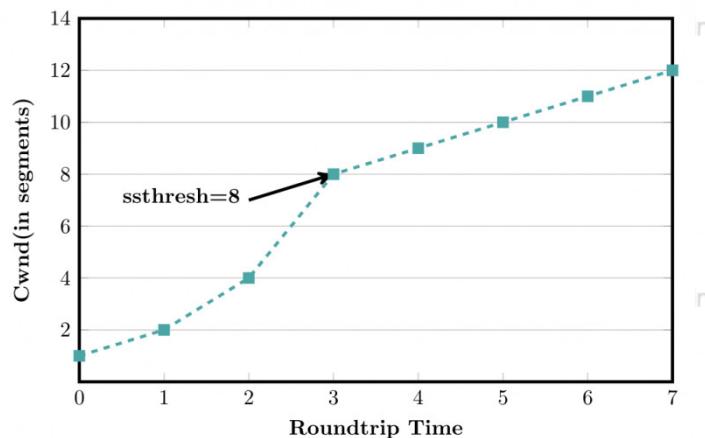
[gate2005-it](#) [computer-networks](#) [congestion-control](#) [normal](#)

[Answer](#)

Answers: Congestion Control



- ✓ Assume that ssthresh = 8.



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Increase is exponential in the Slow Start Phase.

Answer is **option D.**

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30 votes

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-- Amar Vashishth (25.2k points)



- ✓ At:

$$t = 1, \Rightarrow 2MSS$$

$$t = 2, \Rightarrow 4MSS$$

$$t = 3, \Rightarrow 8MSS$$

$$t = 4, \Rightarrow 9MSS \text{ (after threshold additive increase)}$$

$$t = 5, \Rightarrow 10MSS \text{ (fails)}$$

Threshold will be reduced to $\frac{n}{2}$ i.e. $\frac{10}{2} = 5$.

$$t = 6, \Rightarrow 1MSS,$$

(There is an ambiguity here if the window size will be 1MSS or 2 MSS as given in the question and due to this GATE gave marks to all. Assuming window size to be 1 MSS)

$$t = 7 \Rightarrow 2MSS$$

$$t = 8, \Rightarrow 4MSS$$

$$t = 9, \Rightarrow 5MSS$$

$$t = 10, \Rightarrow 6MSS.$$

So, at the end of 10th successful transmission ,

The the congestion window size will be $(6 + 1) = 7 \text{ MSS}$.

98 votes

-- Harsh181996 (3k points)

2.4.3 Congestion Control: GATE CSE 2014 Set 1 | Question: 27 [top](#)

<https://gateoverflow.in/1794>



- ✓ **Answer:** Given that at the time of Time Out, Congestion Window Size is $32KB$ and $\text{RTT} = 100ms$,

When Time Out occurs, for the next round of Slow Start,

$$\text{Threshold} = \frac{\text{size of congestion window}}{2},$$

$$\text{Threshold} = 16KB$$

Suppose we have a **slow start** $\Rightarrow 2KB | 4KB | 8KB | 16KB$

(As the threshold is reached, Additive increase starts)

$|18KB | 20KB | 22KB | 24KB | 26KB | 28KB | 30KB | 32KB$

Here | (vertical line) is representing **RTT** so the total number of vertical lines is $11 \times 100ms = 1100msec$ and so this is the answer.

157 votes

-- Jay (831 points)

2.4.4 Congestion Control: GATE CSE 2015 Set 1 | Question: 29 [top](#)

<https://gateoverflow.in/8253>



$$\begin{aligned} P &= P(S1)P(\neg S2)P(\neg S3)P(\neg S4) \\ &\quad + P(\neg S1)P(S2)P(\neg S3)P(\neg S4) \\ &\quad + P(\neg S1)P(\neg S2)P(S3)P(\neg S4) \\ &\quad + P(\neg S1)P(\neg S2)P(\neg S3)P(S4) \end{aligned}$$

$$= 0.1 * 0.8 * 0.7 * 0.6 + 0.9 * 0.2 * 0.7 * 0.6 + 0.9 * 0.8 * 0.3 * 0.6 + 0.9 * 0.8 * 0.7 * 0.4$$

$$= 0.4404$$

71 votes

-- Arjun Suresh (332k points)

2.4.5 Congestion Control: GATE CSE 2018 | Question: 14 [top](#)

<https://gateoverflow.in/204088>



- ✓ Each time an **ACK** is received by the sender, the congestion window is increased by 1 segment:
 $CWND = CWND + 1$.

$CWND$ increases exponentially on every **RTT**.

Hence, correct answer is **C**.

<https://www.utdallas.edu/~venky/acn/CongestionControl.pdf>

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References



36 votes

-- Prashant Kumar (1k points)

2.4.6 Congestion Control: GATE CSE 2018 | Question: 55 [top](#)

<https://gateoverflow.in/204130>



- ✓ P starts transmission at $t = 0$. If P's first bit reaches Q within Q's sensing window, then Q won't transmit and there shall be no collision.

Q senses carrier till $t = 5$. At $t = 6$ it starts its transmission.

If the first bit of P reaches Q by $t = 5$, collision can be averted. Since signal speed is 10 m/time (given), we can conclude that max distance between P and Q can be 50 meters.

67 votes

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-- Abhishek Sarkar (281 points)

2.4.7 Congestion Control: GATE IT 2005 | Question: 73 top



✓ Answer should be (B).

Current Sender window = min(Congestion Window, Advertised Window)

$$= \min(4KB, 6KB)$$

$$= 4KB.$$

81 votes

https://gateoverflow.in/3836

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-- srestha (85.2k points)

2.5

Crc Polynomial (4) top

2.5.1 Crc Polynomial: GATE CSE 2007 | Question: 68, ISRO2016-73 top



The message 11001001 is to be transmitted using the CRC polynomial $x^3 + 1$ to protect it from errors. The message that should be transmitted is:

- A. 11001001000
- B. 11001001011
- C. 11001010
- D. 110010010011

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gate2007-cse computer-networks error-detection crc-polynomial normal isro2016

Answer ↗

2.5.2 Crc Polynomial: GATE CSE 2017 Set 1 | Question: 32 top

https://gateoverflow.in/11831



A computer network uses polynomials over $GF(2)$ for error checking with 8 bits as information bits and uses $x^3 + x + 1$ as the generator polynomial to generate the check bits. In this network, the message 01011011 is transmitted as:

- A. 01011011010
- B. 01011011011
- C. 01011011101
- D. 01011011100

gate2017-cse-set1 computer-networks crc-polynomial normal

Answer ↗

2.5.3 Crc Polynomial: GATE CSE 2021 Set 2 | Question: 34 top

https://gateoverflow.in/357506



Consider the cyclic redundancy check (CRC) based error detecting scheme having the generator polynomial $X^3 + X + 1$. Suppose the message $m_4m_3m_2m_1m_0 = 11000$ is to be transmitted. Check bits $c_2c_1c_0$ are appended at the end of the message by the transmitter using the above CRC scheme. The transmitted bit string is denoted by $m_4m_3m_2m_1m_0c_2c_1c_0$. The value of the checkbit sequence $c_2c_1c_0$ is

- A. 101
- B. 110
- C. 100
- D. 111

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gate2021-cse-set2 computer-networks crc-polynomial

Answer ↗



Consider the following message $M = 1010001101$. The cyclic redundancy check (CRC) for this message using the divisor polynomial $x^5 + x^4 + x^2 + 1$ is :

- A. 01110
- B. 01011
- C. 10101
- D. 10110

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[gate2005-it](https://gate2005-it.com) [computer-networks](https://computer-networks.com) [crc-polynomial](https://crc-polynomial.com) [normal](https://normal.com)

Answer

Answers: Crc Polynomial



- ✓ Answer - B.

Degree of generator polynomial is 3 hence 3-bits are appended before performing division

After performing division using 2's complement arithmetic remainder is 011

The remainder is appended to original data bits and we get $M' = 11001001011$ from $M = 11001001$.

$$\begin{array}{r}
 1001 \left| \begin{array}{r} 11001001001000 \\ 1001 \downarrow \\ \hline 1011 \\ 1001 \downarrow \\ \hline 1000 \\ 1001 \downarrow \\ \hline 1100 \\ 1001 \downarrow \\ \hline 1010 \\ 1001 \\ \hline 011
 \end{array} \right.
 \end{array}$$

Courtesy, **Anurag Pandey**

49 votes

-- Ankit Rokde (6.9k points)



- ✓ The generator polynomial has degree 3. So, we append 3 zeroes to the original message.

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$$\begin{array}{r}
 1\ 0\ 1\ 1 \\
 \left| \begin{array}{r}
 0\ 1\ 0\ 1\ 1\ 0\ 1\ 1\ 0\ 0\ 0 \\
 0\ 0\ 0\ 0 \\
 \hline
 1\ 0\ 1\ 1 \\
 1\ 0\ 1\ 1 \\
 \hline
 0\ 0\ 1\ 1\ 0\ 0 \\
 1\ 0\ 1\ 1 \\
 \hline
 1\ 1\ 1\ 0 \\
 1\ 0\ 1\ 1 \\
 \hline
 1\ 0\ 1
 \end{array} \right. \\
 M' = 0\ 1\ 0\ 1\ 1\ 0\ 1\ 1\ \underline{\textcolor{red}{1\ 0\ 1}}
 \end{array}$$

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Correct Answer: C

46 votes

-- Smriti012 (2.8k points)

2.5.3 Crc Polynomial: GATE CSE 2021 Set 2 | Question: 34 top

<https://gateoverflow.in/357506>



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The given polynomial $x^3 + x + 1$ is written as 1011, which consists of 4 bits so, append 3 bits of 0s to the message.

$M = 11000000$

$$\begin{array}{r}
 1011)11000000 \\
 \underline{1011} \\
 1110 \\
 \underline{1011} \\
 1010 \\
 \underline{1011} \\
 100
 \end{array}$$

There the check bits sequence is: **100**.

1 votes

-- Cringe is my middle name... (885 points)

2.5.4 Crc Polynomial: GATE IT 2005 | Question: 78 top

<https://gateoverflow.in/3842>



✓ Degree of generator polynomial is 5. Hence, 5 zeroes are appended before division.

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The diagram illustrates the division process for calculating a CRC:

$$\begin{array}{r}
 110101 \\
 \overline{101000110} \\
 110101 \\
 \hline
 1110110 \\
 110101 \\
 \hline
 111110 \\
 110101 \\
 \hline
 101100 \\
 110101 \\
 \hline
 01110
 \end{array}$$

EXOR

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$$M' = 1010001101\boxed{01110}$$

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In CRC calculation, we add the remainder to the original message to get $M' = 1010001101\textbf{01110}$.

Answer is A.

45 votes

-- kvkumar (4k points)

2.6

Csma Cd (5) [top](#)

2.6.1 Csma Cd: GATE CSE 2015 Set 3 | Question: 6 [top](#)

<https://gateoverflow.in/8400>



Consider a CSMA/CD network that transmits data at a rate of $100 Mbps$ (10^8 bits per second) over a $1 km$ (kilometre) cable with no repeaters. If the minimum frame size required for this network is $1250 bytes$, What is the signal speed (km/sec) in the cable?

- A. 8000
- B. 10000
- C. 16000
- D. 20000

[gate2015-cse-set3](#) [computer-networks](#) [congestion-control](#) [csma-cd](#) [normal](#)

Answer

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2.6.2 Csma Cd: GATE CSE 2016 Set 2 | Question: 53 [top](#)

<https://gateoverflow.in/3959>



A network has a data transmission bandwidth of 20×10^6 bits per second. It uses CSMA/CD in the MAC layer. The maximum signal propagation time from one node to another node is 40 microseconds. The minimum size of a frame in the network is _____ bytes.

[gate2016-cse-set2](#) [computer-networks](#) [csma-cd](#) [numerical-answers](#) [normal](#)

Answer

2.6.3 Csma Cd: GATE IT 2005 | Question: 27 [top](#)

<https://gateoverflow.in/3773>



Which of the following statements is TRUE about CSMA/CD:

- A. IEEE 802.11 wireless LAN runs CSMA/CD protocol
- B. Ethernet is not based on CSMA/CD protocol
- C. CSMA/CD is not suitable for a high propagation delay network like satellite network

D. There is no contention in a CSMA/CD network

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Answer 

2.6.4 Csma Cd: GATE IT 2005 | Question: 71 [top](#) 

<https://gateoverflow.in/3834>



A network with CSMA/CD protocol in the MAC layer is running at 1Gbps over a 1km cable with no repeaters. The signal speed in the cable is 2×10^8 m/sec. The minimum frame size for this network should be:

- A. 10000bits
- B. 10000bytes
- C. 5000 bits
- D. 5000bytes

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Answer 

2.6.5 Csma Cd: GATE IT 2008 | Question: 65 [top](#) 

<https://gateoverflow.in/3376>



The minimum frame size required for a CSMA/CD based computer network running at 1Gbps on a 200m cable with a link speed of 2×10^8 m/sec is:

- A. 125bytes
- B. 250bytes
- C. 500bytes
- D. None of the above

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Answer 

Answers: Csma Cd

2.6.1 Csma Cd: GATE CSE 2015 Set 3 | Question: 6 [top](#) 

<https://gateoverflow.in/8400>



- ✓ For collision to be detected, the frame size should be such that the transmission time of the frame should be greater than twice the propagation delay (So, before the frame is completely sent, any possible collision will be discovered).

$$\text{So, } \frac{1250 \times 8}{10^8} \geq \frac{2 \times 1}{x}$$

$$\Rightarrow x = 2 \times 10^4 = 20000$$

Correct Answer: D

 47 votes

-- Arjun Suresh (332k points)

2.6.2 Csma Cd: GATE CSE 2016 Set 2 | Question: 53 [top](#) 

<https://gateoverflow.in/39589>



- ✓ Since, CSMA/CD
Transmission Delay = RTT

Hence,

$$L = B \times \text{RTT}$$

$$\Rightarrow L = B \times 2 \times T_{\text{propagation}}$$

$$\Rightarrow L = (20 \times 10^6) \times 2 \times 40 \times 10^{-6}$$

$$= 20 \times 2 \times 40$$

$$= 1600 \text{ bits}$$

$$= 200 \text{ bytes}$$

Hence, 200 Bytes is the answer.

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43 votes

-- Shashank Chavan (2.4k points)

2.6.3 Csma Cd: GATE IT 2005 | Question: 27 [top](#)

<https://gateoverflow.in/3773>



- ✓ Answer is C.

CSMA/CD was used in early days, 802.3 not in 802.11

There will be contention in this protocol.

Ethernet is based on csma/cd early in 1980s.

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-- nagalla pruthvi (675 points)

2.6.4 Csma Cd: GATE IT 2005 | Question: 71 [top](#)

<https://gateoverflow.in/3834>



- ✓ Answer is(A)

Minimum frame size is needed to ensure that collisions are detected properly. The minimum frame size ensures that before a frame is completely send, it would be notified of any possible collision and hence collision detection works perfectly.

In CSMA/CD a sender won't send a packet if it senses that another sender is using it. So, assume a sender A and a receiver B. When sender sends a packet, receiver might use the cable until it is notified that a packet is being send to it. The receiver will be notified as soon as the first bit arrives that a packet is coming and it won't send any packet after this until that packet is finished. So, in the worst case for collision, receiver will transmit a packet back to the sender just before the first bit of the packet reaches it. (If t_d is the propagation delay of the channel, this time would be just t_d). In this case, surely there will be collision. But for the sender to detect it, it should be notified of B's packet before the sending of the first packet finishes. i.e., when B's packet arrives at A (takes another t_d time), A shouldn't have finished transmission of the first packet for it to detect a collision. i.e., A should be still continuing the sending of the packet in this time interval of $2 \times t_d$. Thus,

The amount of bits that can be transmitted by A in $2 \times t_d$ time should be less than the frame size (S) (sending of the frame shouldn't finish in this time)

Amount of bits transmitted in time t is bandwidth $\times t$ and propagation delay- t_d is $\frac{\text{distance}}{\text{link speed}}$

So, $S \geq 2 \times \text{bandwidth} \times t_d$

$$\geq 2 \times 10^9 \times \frac{1000}{2 \times 10^8}$$

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≥ 10000 bits

54 votes

-- Arjun Suresh (332k points)

2.6.5 Csma Cd: GATE IT 2008 | Question: 65 [top](#)

<https://gateoverflow.in/3376>



- ✓ Minimum frame size is needed to ensure that collisions are detected properly. The minimum frame size ensures that before a frame is completely send, it would be notified of any possible collision and hence collision detection works perfectly.

In CSMA/CD a sender won't send a packet if it senses that another sender is using it. So, assume a sender A and a receiver B. When sender sends a packet, receiver might use the cable until it is notified that a packet is being send to it. The receiver will be notified as soon as the first bit arrives that a packet is coming and it won't send any packet after this until that packet is finished. So, in the worst case for collision, receiver will transmit a packet back to the sender just before the first bit of the packet reaches it. (If t_d is the propagation delay of the channel, this time would be just t_d). In this case, surely there will be collision. But for the sender to detect it, it should be notified of B's packet before the sending of the first packet finishes. i.e., when B's packet arrives at A (takes another t_d time), A shouldn't have finished transmission of the first packet for it to detect a collision. i.e., A should be still continuing the sending of the packet in this time interval of $2 \times t_d$. Thus,

The amount of bits that can be transmitted by A in $2 \times t_d$ time should be less than the frame size (S) (sending of the frame shouldn't finish in this time)

Amount of bits transmitted in time t is bandwidth $\times t$ and propagation delay- t_d is $\frac{\text{distance}}{\text{link speed}}$

So, $S \geq 2 \times \text{bandwidth} \times t_d$

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$$\geq 2 \times 10^9 \times \frac{200}{2 \times 10^8}$$

≥ 2000 bits

≥ 250 bytes

Correct Answer: **B**

35 votes

-- Arjun Suresh (332k points)

2.7

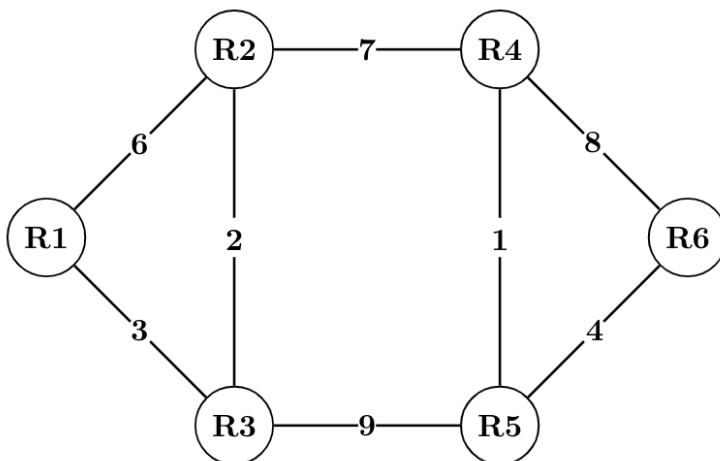
Distance Vector Routing (7) top ↗

2.7.1 Distance Vector Routing: GATE CSE 2010 | Question: 54 top ↗

<https://gateoverflow.in/2362>



Consider a network with 6 routers **R1** to **R6** connected with links having weights as shown in the following diagram.



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All the routers use the distance vector based routing algorithm to update their routing tables. Each router starts with its routing table initialized to contain an entry for each neighbor with the weight of the respective connecting link. After all the routing tables stabilize, how many links in the network will never be used for carrying any data?

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- A. 4
- B. 3
- C. 2
- D. 1

[gate2010-cse](#) [computer-networks](#) [routing](#) [distance-vector-routing](#) [normal](#)

Answer

2.7.2 Distance Vector Routing: GATE CSE 2010 | Question: 55 top ↗

<https://gateoverflow.in/43326>



Consider a network with 6 routers *R1* to *R6* connected with links having weights as shown in the following diagram.

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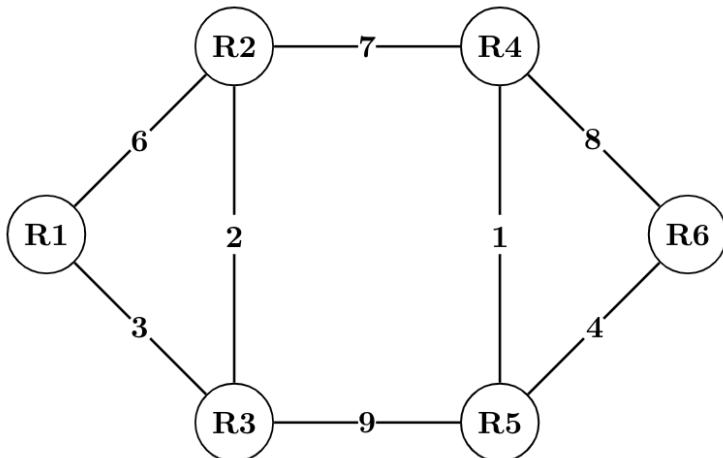
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Suppose the weights of all unused links are changed to 2 and the distance vector algorithm is used again until all routing tables stabilize. How many links will now remain unused?

- A. 0
- B. 1
- C. 2
- D. 3

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gate2010-cse computer-networks routing distance-vector-routing normal

Answer

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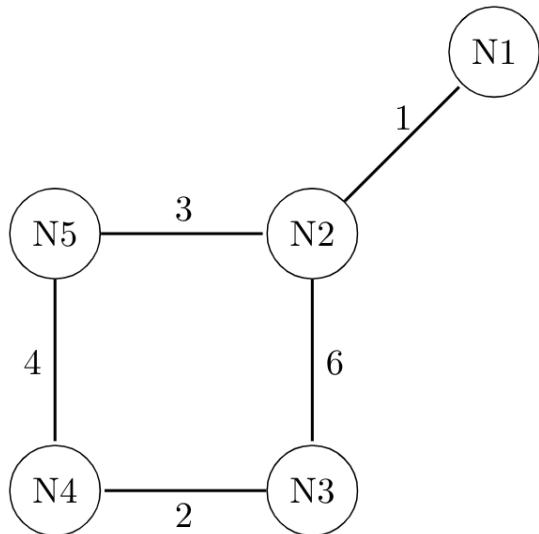
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2.7.3 Distance Vector Routing: GATE CSE 2011 | Question: 52

<https://gateoverflow.in/2160>



Consider a network with five nodes, N_1 to N_5 , as shown as below.



The network uses a Distance Vector Routing protocol. Once the routes have been stabilized, the distance vectors at different nodes are as follows.

$N_1: (0, 1, 7, 8, 4)$

$N_2: (1, 0, 6, 7, 3)$

$N_3: (7, 6, 0, 2, 6)$

$N_4: (8, 7, 2, 0, 4)$

$N_5: (4, 3, 6, 4, 0)$

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Each distance vector is the distance of the best known path at that instance to nodes, N_1 to N_5 , where the distance to itself is 0. Also, all links are symmetric and the cost is identical in both directions. In each round, all nodes exchange their distance vectors

with their respective neighbors. Then all nodes update their distance vectors. In between two rounds, any change in cost of a link will cause the two incident nodes to change only that entry in their distance vectors.

The cost of link $N2 - N3$ reduces to 2 (in both directions). After the next round of updates, what will be the new distance vector at node, $N3$?

- A. $(3, 2, 0, 2, 5)$
- B. $(3, 2, 0, 2, 6)$
- C. $(7, 2, 0, 2, 5)$
- D. $(7, 2, 0, 2, 6)$

gate2011-cse computer-networks routing distance-vector-routing normal

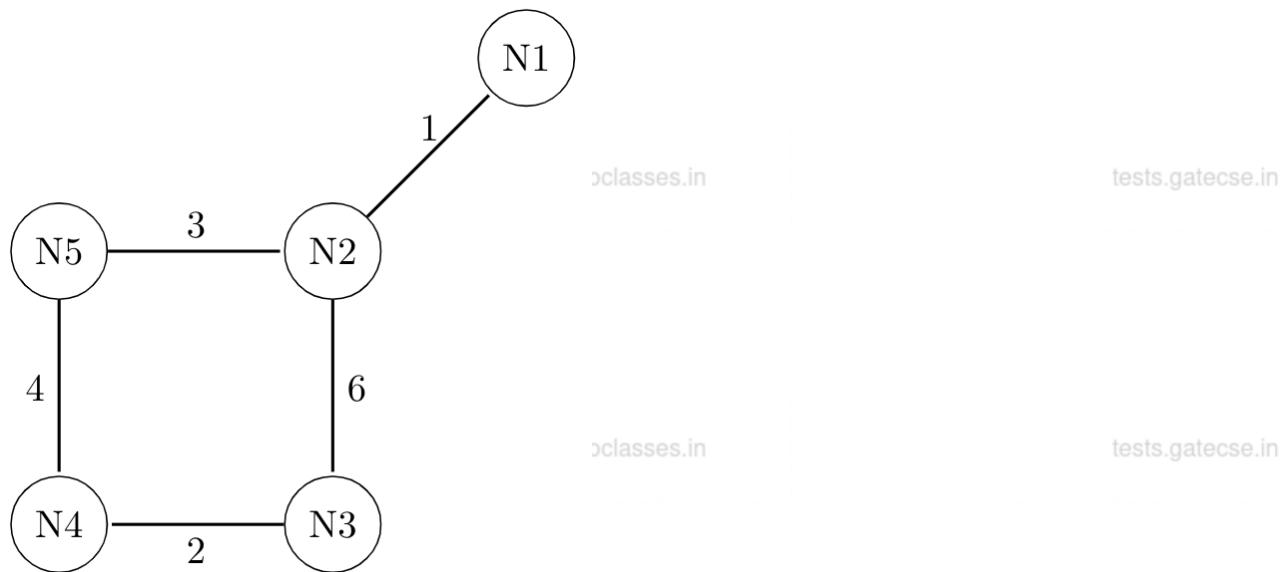
Answer ↗

2.7.4 Distance Vector Routing: GATE CSE 2011 | Question: 53 top ↺

↗ <https://gateoverflow.in/43317>



Consider a network with five nodes, $N1$ to $N5$, as shown as below.



The network uses a Distance Vector Routing protocol. Once the routes have been stabilized, the distance vectors at different nodes are as follows.

- $N1: (0, 1, 7, 8, 4)$
- $N2: (1, 0, 6, 7, 3)$
- $N3: (7, 6, 0, 2, 6)$
- $N4: (8, 7, 2, 0, 4)$
- $N5: (4, 3, 6, 4, 0)$

Each distance vector is the distance of the best known path at that instance to nodes, $N1$ to $N5$, where the distance to itself is 0. Also, all links are symmetric and the cost is identical in both directions. In each round, all nodes exchange their distance vectors with their respective neighbors. Then all nodes update their distance vectors. In between two rounds, any change in cost of a link will cause the two incident nodes to change only that entry in their distance vectors.

The cost of link $N2 - N3$ reduces to 2 (in both directions). After the next round of updates, the link $N1 - N2$ goes down. $N2$ will reflect this change immediately in its distance vector as cost, ∞ . After the **NEXT ROUND** of update, what will be the cost to $N1$ in the distance vector of $N3$?

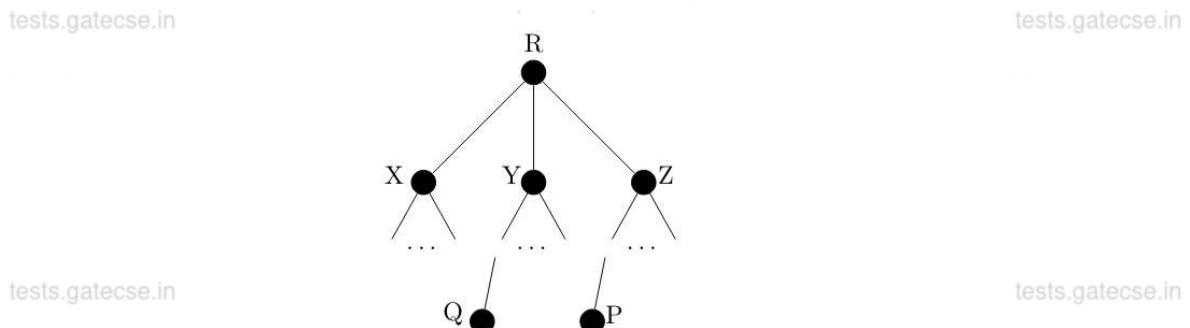
- A. 3
- B. 9
- C. 10
- D. ∞

gate2011-cse computer-networks routing distance-vector-routing normal

Answer ↗



Consider a computer network using the distance vector routing algorithm in its network layer. The partial topology of the network is shown below.



The objective is to find the shortest-cost path from the router R to routers P and Q . Assume that R does not initially know the shortest routes to P and Q . Assume that R has three neighbouring routers denoted as X , Y and Z . During one iteration, R measures its distance to its neighbours X , Y , and Z as 3, 2 and 5, respectively. Router R gets routing vectors from its neighbours that indicate that the distance to router P from routers X , Y and Z are 7, 6 and 5, respectively. The routing vector also indicates that the distance to router Q from routers X , Y and Z are 4, 6 and 8 respectively. Which of the following statement(s) is/are correct with respect to the new routing table of R , after updation during this iteration?

- A. The distance from R to P will be stored as 10
- B. The distance from R to Q will be stored as 7
- C. The next hop router for a packet from R to P is Y
- D. The next hop router for a packet from R to Q is Z

[gate2021-cse-set2](#) [multiple-selects](#) [computer-networks](#) [distance-vector-routing](#)

Answer



Count to infinity is a problem associated with:

- A. link state routing protocol
- B. distance vector routing protocol
- C. DNS while resolving host name
- D. TCP for congestion control

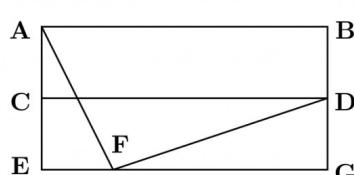
[gate2005-it](#) [computer-networks](#) [routing](#) [distance-vector-routing](#) [normal](#)

Answer



For the network given in the figure below, the routing tables of the four nodes A , E , D and G are shown. Suppose that F has estimated its delay to its neighbors, A , E , D and G as 8, 10, 12 and 6 msec respectively and updates its routing table using distance vector routing technique.

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Routing Table of A		Routing Table of D		Routing Table of E		Routing Table of G	
A	0	A	20	A	24	A	21
B	40	B	8	B	27	B	24
C	14	C	30	C	7	C	22
D	17	D	0	D	20	D	19
E	21	E	14	E	0	E	22
F	9	F	7	F	11	F	10
G	24	G	22	G	22	G	0

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Routing Table of A		Routing Table of D		Routing Table of E		Routing Table of G	
A	8	A	21	A	21	A	21
B	20	B	8	B	8	B	8
C	17	C	7	C	7	C	7
D	12	D	19	D	19	D	12
E	10	E	14	E	14	E	10
F	0	F	0	F	0	F	0
G	6	G	22	G	22	G	6

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Routing Table of A		Routing Table of D		Routing Table of E		Routing Table of G	
A	8	A	21	A	21	A	21
B	20	B	8	B	8	B	8
C	17	C	7	C	7	C	7
D	12	D	19	D	19	D	12
E	10	E	14	E	14	E	10
F	16	F	0	F	0	F	16
G	6	G	22	G	22	G	6

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Routing Table of A		Routing Table of D		Routing Table of E		Routing Table of G	
A	8	A	21	A	21	A	21
B	8	B	8	B	8	B	8
C	7	C	7	C	7	C	7
D	12	D	12	D	12	D	12
E	10	E	10	E	10	E	10
F	0	F	0	F	0	F	0
G	6	G	6	G	6	G	6

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gate2007-it computer-networks distance-vector-routing normal

Answer ↗

Answers: Distance Vector Routing

2.7.1 Distance Vector Routing: GATE CSE 2010 | Question: 54 top ↗

↗ <https://gateoverflow.in/2362>



✓ Answer (C)

Following will be distance vectors of all nodes.

Shortest Distances from R_1 to R_2, R_3, R_4, R_5 and R_6
 $R_1(5, 3, 12, 12, 16)$

Links used: $R_1 - R_3, R_3 - R_2, R_2 - R_4, R_3 - R_5, R_5 - R_6$
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Shortest Distances from R_2 to R_3, R_4, R_5 and R_6
 $R_2(2, 7, 8, 12)$
Links used: $R_2 - R_3, R_2 - R_4, R_4 - R_5, R_5 - R_6$

Shortest Distances from R_3 to R_4, R_5 and R_6
 $R_3(9, 9, 13)$
Links used: $R_3 - R_2, R_2 - R_4, R_3 - R_5, R_5 - R_6$

Shortest Distances from R_4 to R_5 and R_6
 $R_4(1, 5)$
Links used: $R_4 - R_5, R_5 - R_6$

Shortest Distance from R_5 to R_6
 $R_5(4)$
Links Used: $R_5 - R_6$

If we mark, all the used links one by one, we can see that following links are never used.

$R_1 - R_2$
 $R_4 - R_6$

50 votes

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-- Akhil Nadh PC (16.5k points)



2.7.2 Distance Vector Routing: GATE CSE 2010 | Question: 55 [top](#)

<https://gateoverflow.in/4336>

- ✓ First we need to find which are the unused links in the graph
For that we need not make distance vector tables,
We can do this by simply looking into the graph or else DVT can also give the answer.
So, $R_1 - R_2$ and $R_4 - R_6$ will remain unused.

Now If We changed the unused links to value 2.
 $R_5 - R_6$ will Now remain unused.

So, the correct answer is option **B**).

41 votes

-- saif ahmed (3.2k points)



2.7.3 Distance Vector Routing: GATE CSE 2011 | Question: 52 [top](#)

<https://gateoverflow.in/2160>

- ✓ Answer is **(A)**.

1. As soon as $N_2 - N_3$ reduces to 2, both N_2 and N_3 instantly updates their distance to N_3 and N_2 to 2 respectively. So, N_2 : $(1, 0, 2, 7, 3)$, N_3 : $(7, 2, 0, 2, 6)$ becomes this.

After this starts first round of update in which each node shares its table with their respective neighbors ONLY. BUT KEEP IN MIND THAT ONLY OLD TABLES WILL BE SHARED. What I mean is tables that will be used for updation at this moment contain the values as N_1 : $(0, 1, 7, 8, 4)$, N_2 : $(1, 0, 2, 7, 3)$, N_3 : $(7, 2, 0, 2, 6)$, N_4 : $(8, 7, 2, 0, 4)$, N_5 : $(4, 3, 6, 4, 0)$.
SEE at this time all the entries are old EXCEPT in N_2 and N_3 where value changes to 2 instead of 6.

Question asks for N_3 . So focus on that.

N_3 receives tables from N_2 : $(1, 0, 2, 7, 3)$ and N_4 : $(8, 7, 2, 0, 4)$. Using THIS ONLY original N_3 : $(7, 2, 0, 2, 6)$ updates to $N_3(3, 2, 0, 2, 5)$. (For updation and forming the tables for this refer FOROUZAN.)

So, answer is **(A)**.

68 votes

-- Sandeep_Uniyal (6.5k points)



2.7.4 Distance Vector Routing: GATE CSE 2011 | Question: 53 [top](#)

<https://gateoverflow.in/4337>

- ✓ First, as soon as $N_1 - N_2$ goes down, N_2 and N_1 both update that entry in their tables as infinity. So N_2 at this moment will be $N_2(\inf, 0, 2, _, _)$. I have left blank coz that details are not important.

Now for N_3 to get updated in the subsequent round it will get tables from N_2 and N_4 only. But first we need to find the N_4 calculated in previous update. So in previous question N_4 received updates from N_3 and N_5 which are N_3 : $(7, 6, 0, 2, 6)$, N_5 : $(4, 3, 6, 4, 0)$.

NOW THIS IS VERY IMPORTANT AS WHY N4 DID NOT GET UPDATED TABLES FROM N3. SO ANSWER IS THAT these tables were shared at the same moment and so in a particular round of update old values of all the tables are used and not the updated values.

N3 was updates AFTER IT PASSED ITS OLD table to its neighbors AS WHY WOULD N4 WAIT FOR N3 to GET UPDATED first !!! So N4 will update its table (in prev question) to N4(8,7,2,0,4).

See here path to N1 exists via N5 and not via N3 bcoz when table was shared by N3 it contained path to N1 as 7 and N1 via N3 sums to $7+2=9$. Now when N3 receives tables from N2(inf,0,_,_,_) and N4(8,7,2,0,4).

At first it will see its distance to N1 as "Inf" and NOT 3 because "inf" is the new distance with the same Next hop N2 (**If next hop is same, new entry is updated even though it is larger than previous entry for the same NEXT HOP**).

But at the same time it sees distance to N1 from N4 as 8 and so updates with the value $(N3-N4 + N4-N1) = (2+8)=10$. So N3-N1 distance in N3(10,_,0,_,_) is 10.

So, answer is (C)

Reference: <http://www.cs.princeton.edu/courses/archive/spr11/cos461/docs/lec14-distvector.pdf>

References



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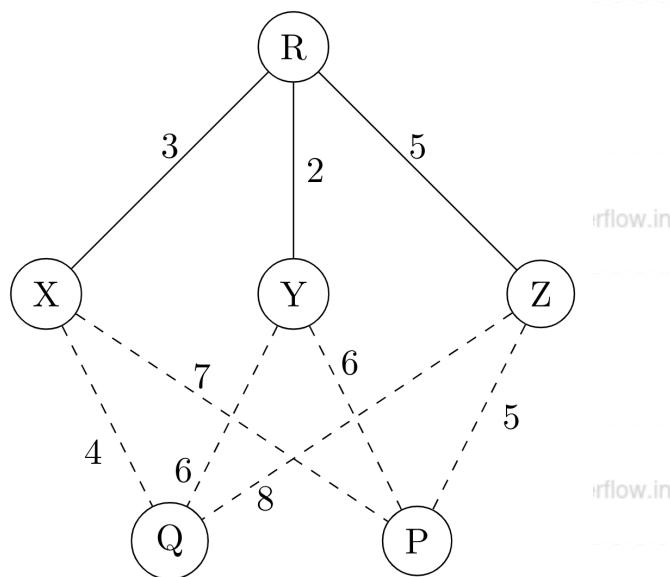
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49 votes

-- Sandeep_Uniyal (6.5k points)

2.7.5 Distance Vector Routing: GATE CSE 2021 Set 2 | Question: 45 [top](#)

<https://gateoverflow.in/357495>



As per Distance Vector Routing Algorithm,

$$R \text{ to } P = \min \{R - X - P, R - Y - P, R - Z - P\} = \min\{10, 8, 11\} = 8 \text{ through } Y.$$

$$R \text{ to } Q = \min \{R - X - Q, R - Y - Q, R - Z - Q\} = \min\{7, 8, 13\} = 7 \text{ through } X.$$

Hence Options (B) and (C) are correct

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3 votes

-- Ashwani Kumar (13k points)

2.7.6 Distance Vector Routing: GATE IT 2005 | Question: 29 [top](#)

<https://gateoverflow.in/3775>



✓ Answer is B.

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Distance vector routing.

14 votes

-- nagalla pruthvi (675 points)

2.7.7 Distance Vector Routing: GATE IT 2007 | Question: 60 [top](#)

<https://gateoverflow.in/3504>



✓ Answer: (A)

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Distance from F to F is 0 which eliminates option (C).

Using distance vector routing protocol, $F \rightarrow D \rightarrow B$ yields distance as 20 which eliminates options (B) and (D).

38 votes

-- Rajarshi Sarkar (27.9k points)

2.8

Error Detection (8) [top](#)

2.8.1 Error Detection: GATE CSE 1992 | Question: 01,ii [top](#)

<https://gateoverflow.in/546>



Consider a 3-bit error detection and 1-bit error correction hamming code for 4-bit data. The extra parity bits required would be _____ and the 3-bit error detection is possible because the code has a minimum distance of _____.

gate1992 computer-networks error-detection normal fill-in-the-blanks

Answer

2.8.2 Error Detection: GATE CSE 1995 | Question: 1.12 [top](#)

<https://gateoverflow.in/2599>



What is the distance of the following code 000000, 010101, 000111, 011001, 111111?

- A. 2
- B. 3
- C. 4
- D. 1

gate1995 computer-networks error-detection normal

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Answer

2.8.3 Error Detection: GATE CSE 2009 | Question: 48 [top](#)

<https://gateoverflow.in/1334>



Let $G(x)$ be the generator polynomial used for CRC checking. What is the condition that should be satisfied by $G(x)$ to detect odd number of bits in error?

- A. $G(x)$ contains more than two terms
- B. $G(x)$ does not divide $1 + x^k$, for any k not exceeding the frame length
- C. $1 + x$ is a factor of $G(x)$
- D. $G(x)$ has an odd number of terms.

gate2009-cse computer-networks error-detection normal

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Answer

2.8.4 Error Detection: GATE CSE 2014 Set 3 | Question: 24 [top](#)

<https://gateoverflow.in/2058>



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A bit-stuffing based framing protocol uses an 8-bit delimiter pattern of 01111110. If the output bit-string after stuffing is 01111100101, then the input bit-string is:

- A. 0111110100
- B. 0111110101
- C. 0111111101
- D. 0111111111

gate2014-cse-set3 computer-networks error-detection

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Answer



In a communication network, a packet of length L bits takes link L_1 with a probability of p_1 or link L_2 with a probability of p_2 . Link L_1 and L_2 have bit error probability of b_1 and b_2 respectively. The probability that the packet will be received without error via either L_1 or L_2 is

- A. $(1 - b_1)^L p_1 + (1 - b_2)^L p_2$
- B. $[1 - (b_1 + b_2)^L] p_1 p_2$
- C. $(1 - b_1)^L (1 - b_2)^L p_1 p_2$
- D. $1 - (b_1^L p_1 + b_2^L p_2)$

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[gate2005-it](#) [computer-networks](#) [error-detection](#) [probability](#) [normal](#)

Answer



An error correcting code has the following code words: 00000000, 00001111, 01010101, 10101010, 11110000 . What is the maximum number of bit errors that can be corrected?

- A. 0
- B. 1
- C. 2
- D. 3

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[gate2007-it](#) [computer-networks](#) [error-detection](#) [normal](#)

Answer



Data transmitted on a link uses the following 2D parity scheme for error detection:

Each sequence of 28 bits is arranged in a 4×7 matrix (rows r_0 through r_3 , and columns d_7 through d_1) and is padded with a column d_0 and row r_4 of parity bits computed using the Even parity scheme. Each bit of column d_0 (respectively, row r_4) gives the parity of the corresponding row (respectively, column). These 40 bits are transmitted over the data link.

	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0
r_0	0	1	0	1	0	0	1	1
r_1	1	1	0	0	1	1	1	0
r_2	0	0	0	1	0	1	0	0
r_3	0	1	1	0	1	0	1	0
r_4	1	1	0	0	0	1	1	0

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The table shows data received by a receiver and has n corrupted bits. What is the minimum possible value of n ?

- A. 1
- B. 2
- C. 3
- D. 4

[gate2008-it](#) [computer-networks](#) [normal](#) [error-detection](#)

Answer



Match the pairs in the following questions:

(A) Cyclic Redundancy Code	(p) Error Correction
(B) Serial Communication	(q) Wired-OR
(C) Open Collector	(r) Error detection
(D) Hamming Code	(s) RS-232-C

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Answer 

Answers: Error Detection

2.8.1 Error Detection: GATE CSE 1992 | Question: 01,ii top<https://gateoverflow.in/546>

- ✓ The Hamming distance between two-bit strings is the number of bits that would have to be flipped to make the strings identical.

To detect

 d errors we require a minimum Hamming distance of $d + 1$.Correcting d bit flips requires a minimum Hamming distance of $2 \times d + 1$, where d is number of bit in errors.

For the first blank, each error detection we need 1 parity bit

For 3 bit error detection we need 3 parity bits. So, 3 parity bits requires here.

Also, we can calculate this way, formula is $d + p + 1 \leq 2^p$ where, d = data bits, p = parity bits, $d = 4$ bits given.According to 1st question, $d = 4$ so $4 + p + 1 \leq 2^p$ $p + 5 \leq 2^p$ now if $p = 2$ it becomes $7 \leq 4$, Not possible.If $p = 3$ it becomes $8 \leq 8$, which is possible.So, p must be 3. [Minimum value of p is 3]The second blank the 3-bit error detection is possible because the code has a minimum distance of ____ answer is $3 + 1 = 4$, where $d = 3$. Formula used is $d + 1$.

The answer for

2 blanks is
[3, 4]. 31 votes

-- Bikram (58.4k points)

2.8.2 Error Detection: GATE CSE 1995 | Question: 1.12 top<https://gateoverflow.in/2599>

- ✓ Distance (also called min-distance) of a block code is the minimum number of positions in which any two distinct codes differ. Here, min-distance occurs for the codes 2 and 3 and they differ only in 2 positions. So, $d = 2$.

https://en.wikipedia.org/wiki/Block_code

Correct Answer: A

References



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 35 votes

-- Arjun Suresh (332k points)

2.8.3 Error Detection: GATE CSE 2009 | Question: 48 top<https://gateoverflow.in/1334>

- ✓ Let me first explain building blocks to this problem. Before answering this, we should know the relationship between Sent codeword, Received codeword, CRC generator and error polynomial.

let's take an example:

Sent codeword = 10010 ($= x^4 + x$)Received codeword = 10110 (error at 2nd bit) ($= x^4 + x^2 + x$)Now, I can write Sent codeword = Received codeword + error
 $(10010 = 10110 + 00100)$, here we do modulo 2 arithmetic

i.e $1 + 1 = 0$ without carry)

in polynomial also we can see $x^4 + x = x^4 + x^2 + x + x^2 = x^4 + 2x^2 + x = x^4 + x$

(here multiplying with 2 means 0 because it corresponds to binary modulo 2 arithmetic which is $1+1 = 0$ (not 2))

OR

We can also write,

Received codeword = Sent codeword + error (Check it using same method as above)

Sent codeword $C(x)$, Received codeword $R(x)$ and error $E(x)$.

Now we have $R(x) = C(x) + E(x)$. and let CRC polynomial be $G(x)$.

$G(x)$ always divides $C(x)$, and if there is an error then $G(x)$ should not divide $R(x)$.

Lets check -

$R(x) \bmod G(x) = (C(x) + E(x)) \bmod G(x)$ (for simplicity i am writing mod as division)

$$\frac{R(x)}{G(x)} = \frac{C(x)}{G(x)} + \frac{E(x)}{G(x)}$$

$G(x)$ always divides $C(x)$

$$\Rightarrow \frac{R(x)}{G(x)} = 0 + \frac{E(x)}{G(x)}$$

If $G(x)$ divides $E(x)$ also this would mean $G(x)$ divides $R(x)$. We know that, if $G(x)$ does not properly divide $R(x)$ then there is an error but we are never sure if there is error or not when $G(x)$ divides $R(X)$.

As we saw, $G(x)$ divides $R(x)$ or not totally depends on $G(x)$ divides $E(x)$ or not.

Whole strength of $G(x)$ lies if it does not divide any possible $E(x)$.

Lets see again $E(x)$, if there is an error in 3rd and 4th bit from left (LSB is 0th bit) then $E(X) = x^4 + x^3$.(it does not matter error is from toggling 1 to 0 or 0 to 1) **Check with above example.**

Now come to question. it says $G(x)$ should detect odd number of bits in error?.

If number of bits are odd then terms in $E(x)$ would be odd.

for instance if 1st, 2nd and 5th bit got corrupted then $E(x) = x^5 + x^2 + x$.

It is clear that if any function $f(x)$ has a factor of $x - k$, then at $x=k$, $f(x)$ would be zero. I.e. $f(x) = 0$ at $x = k$.

- We want to detect odd number of bits that means received message $R(x)$ contains an odd number of inverted bits, then $E(x)$ must contain an odd number of terms with coefficients equal to 1.
 - As a result, $E(1)$ must equal to 1 (**remember $1+1 = 0$, $1+1+1 = 1$**).
- Any Odd number of times sum of one's is = 1.** $E(1)$ is not zero, this means $x + 1$ is not a factor of $E(x)$.
- Now I want $G(x)$ not to be a factor of $E(x)$, So that $G(x)$ wont divide $E(x)$ and i would happily detect odd number of bits.
 - So, if we make sure that $G(1) = 0$, we can conclude that $G(x)$ does not divide any $E(x)$ corresponding to an odd number of error bits. In this case, a CRC based on $G(x)$ will detect any odd number of errors.
 - As long as $1 + x$ is a factor of $G(x)$, $G(x)$ can never divide $E(x)$. Because we know $E(x)$ dont have factor of $1 + x$.

Option C.

(**Option B** might confuse you, If $G(x)$ has some factor of the form $x^k + 1$ then also $G(x)$ would detect all odd number of errors, **But in Option B**, language is changed, and that too we should not have any upper bound on k)

77 votes

-- Sachin Mittal (15.8k points)



2.8.4 Error Detection: GATE CSE 2014 Set 3 | Question: 24 top

https://gateoverflow.in/2058

- ✓ 011111 *one zero emitted here* 0101

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Correct Answer: B

38 votes

-- abhishek1317 (267 points)



2.8.5 Error Detection: GATE IT 2005 | Question: 74 top

https://gateoverflow.in/3837

- ✓ Probability of choosing link $L_1 = p_1$

Probability for no bit error (for any single bit)= $(1 - b_1)$

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Similarly for link L_2

$$\text{Probability of no bit error} = (1 - b_2)$$

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Packet can go either through link L_1 or L_2 they are mutually exclusive events (means one event happens other won't be happening and so we can simply add their respective probabilities for the favorable case).

Probability packet will be received without any error = Probability of L_1 being chosen and no error in any of the L bits + Probability of L_2 being chosen and no error in any of the L bits

$$= (1 - b_1)^L p_1 + (1 - b_2)^L p_2.$$

Hence, answer is option A.

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Why option D is not correct choice here?

Option D here is giving the probability of a frame being arrived with at least one bit correctly - i.e., all the bits are not errors.

79 votes

-- Pooja Palod (24.1k points)

2.8.6 Error Detection: GATE IT 2007 | Question: 43 top

<https://gateoverflow.in/3478>



✓ Answer: B

$$\text{For correction: } \left\lceil \frac{(\text{Hamming Distance} - 1)}{2} \right\rceil \\ = \lfloor 1.5 \rfloor = 1 \text{ bit error.}$$

For detection: Hamming Distance - 1 = 3 bit error .

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54 votes

-- Rajarshi Sarkar (27.9k points)

2.8.7 Error Detection: GATE IT 2008 | Question: 66 top

<https://gateoverflow.in/3380>



✓

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	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0
r_0	0	1	0	1	0	0	1	1
r_1	1	1	0	0	1	1	1	0
r_2	0	0	0	1	0	1	0	0
r_3	0	1	1	0	1	0	1	0
r_4	1	1	0	0	0	0	1	1

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Here, we need to change minimum 3 bits, and by doing it we get correct parity column wise and row wise (Correction marked by boxed number)

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C is answer

38 votes

-- Prashant Singh (47.2k points)

2.8.8 Error Detection: GATE1987-2-i top

<https://gateoverflow.in/87074>



✓

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(A) Cyclic Redundancy Code	(r) Redundancy checking technique (error detection)
(B) Serial Communication	(s) RS-232-C
(C) Open Collector	(q) Wired OR
(D) Hamming Code	(p) Error Correction Method

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Explanation:

- A. A **cyclic redundancy check** (CRC) is an error-detecting code commonly used in digital networks and storage devices to

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- detect accidental changes to raw data
- B. RS-232C is the physical interface that your computer uses to talk to and exchange data with your modem and other serial devices
 - C. Reference <http://www.ni.com/white-paper/3544/en/>
 - D. The Hamming code is an error correction method using redundant bits. By rearranging the order of bit transmission of the data units, the Hamming code can correct burst errors.

References



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13 votes

-- Lokesh Dafale (8.2k points)

2.9

Ethernet (4) [top](#)

2.9.1 Ethernet: GATE CSE 2004 | Question: 54 [top](#)

<https://gateoverflow.in/1050>



A and *B* are the only two stations on an Ethernet. Each has a steady queue of frames to send. Both *A* and *B* attempt to transmit a frame, collide, and *A* wins the first backoff race. At the end of this successful transmission by *A*, both *A* and *B* attempt to transmit and collide. The probability that *A* wins the second backoff race is:

- A. 0.5
- B. 0.625
- C. 0.75
- D. 1.0

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[gate2004-cse](#) [computer-networks](#) [ethernet](#) [probability](#) [normal](#)

Answer

2.9.2 Ethernet: GATE CSE 2013 | Question: 36 [top](#)

<https://gateoverflow.in/1547>



Determine the maximum length of the cable (in km) for transmitting data at a rate of 500 Mbps in an Ethernet LAN with frames of size 10,000 bits. Assume the signal speed in the cable to be 2,00,000 km/s.

- A. 1
- B. 2
- C. 2.5
- D. 5

[gate2013-cse](#) [computer-networks](#) [ethernet](#) [normal](#)

Answer

2.9.3 Ethernet: GATE CSE 2016 Set 2 | Question: 24 [top](#)

<https://gateoverflow.in/39543>



In an Ethernet local area network, which one of the following statements is **TRUE**?

- A. A station stops to sense the channel once it starts transmitting a frame.
- B. The purpose of the jamming signal is to pad the frames that are smaller than the minimum frame size.
- C. A station continues to transmit the packet even after the collision is detected.
- D. The exponential back off mechanism reduces the probability of collision on retransmissions.

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Answer

2.9.4 Ethernet: GATE IT 2006 | Question: 19 [top](#)

<https://gateoverflow.in/3558>



Which of the following statements is **TRUE**?

- A. Both Ethernet frame and IP packet include checksum fields
- B. Ethernet frame includes a checksum field and IP packet includes a CRC field

- C. Ethernet frame includes a CRC field and IP packet includes a checksum field
 D. Both Ethernet frame and IP packet include CRC fields

gate2006-it computer-networks normal ethernet

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Answer 

Answers: Ethernet

2.9.1 Ethernet: GATE CSE 2004 | Question: 54 [top](#) 

<https://gateoverflow.in/1050>



- ✓ [Exponential back-off algorithm](#) is in use here. Here, when a collision occurs:

- each sender sends a jam signal and waits (back-offs) $k \times 51.2\mu s$, where 51.2 is the fixed slot time and k is chosen randomly from 0 to $2^N - 1$ where N is the current transmission number and $1 \leq N \leq 10$. For $11 \leq N \leq 15$, k is chosen randomly from 0 to 1023. For $N = 16$, the sender gives up.

For this question $N = 1$ for A as this is A' s first re-transmission and $N = 2$ for B as this is its second re-transmission. So, possible values of k for A are $\{0, 1\}$ and that for B are $\{0, 1, 2, 3\}$, giving 8 possible combinations of values. Here, A wins the back-off if its k value is lower than that of B as this directly corresponds to the waiting time. This happens for the k value pairs $\{(0, 1), (0, 2), (0, 3), (1, 2), (1, 3)\}$ which is 5 out of 8. So, probability of A winning the second back-off race is $\frac{5}{8} = 0.625$.

Correct Answer: **B**

References



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 39 votes

-- Arjun Suresh (332k points)



2.9.2 Ethernet: GATE CSE 2013 | Question: 36 [top](#) 

<https://gateoverflow.in/1547>

- ✓ transmission time \geq round trip time of 1 bit

transmission time $\geq 2 \times$ propagation time

$$\frac{10,000 \text{ bits}}{500 \text{ Mbps}} \geq 2 \times \frac{d}{2 \times 10^5 \text{ km per sec}}$$

$2 \text{ km} \geq d$

Option B is correct.

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 42 votes

-- Amar Vashishth (25.2k points)



2.9.3 Ethernet: GATE CSE 2016 Set 2 | Question: 24 [top](#) 

<https://gateoverflow.in/39543>

- ✓ On Ethernet:

A. This is false because station need not stop to listen to stuff !

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B. No, this is not purpose of jamming signal.

C. **No, stations sends jamming signal if collision is detected. This is reason why (B) is false.**

So, answer is (D).

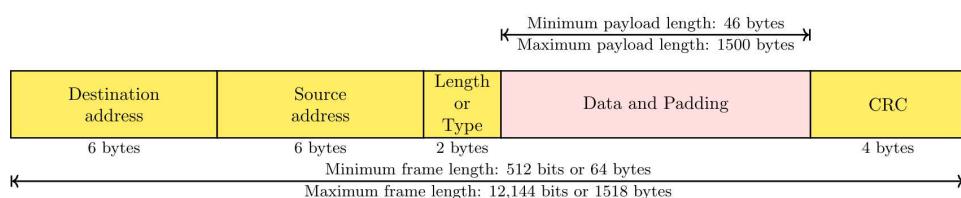
 34 votes

-- Akash Kanase (36k points)



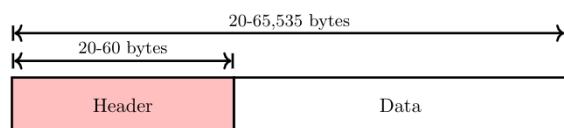
- ✓ The answer is (C).

Ethernet frame



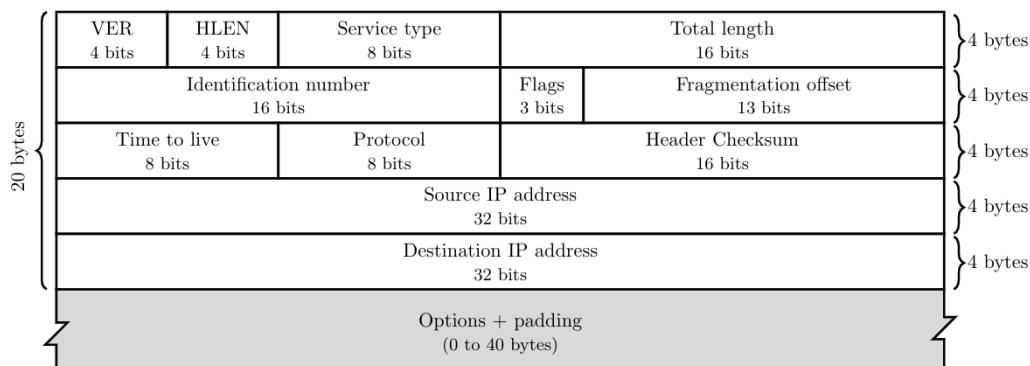
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IP packet



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Fig: IP datagram



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Fig: IP Header format

👍 24 votes

-- Prateek kumar (6.7k points)

2.10

Hamming Code (2) [top](#)

Following 7 bit single error correcting hamming coded message is received.

7	6	5	4	3	2	1	bit No.
1	0	0	0	1	1	0	X

Determine if the message is correct (assuming that at most 1 bit could be corrupted). If the message contains an error find the bit which is erroneous and gives correct message.

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Answer



Assume that a 12-bit Hamming codeword consisting of 8-bit data and 4 check bits is $d_8d_7d_6d_5c_8d_4d_3d_2c_4d_1c_2c_1$, where the data bits and the check bits are given in the following tables:

Data bits							
d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1
1	1	0	x	0	1	0	1

Check bits			
c_8	c_4	c_2	c_1
y	0	1	0

Which one of the following choices gives the correct values of x and y ?

- A. x is 0 and y is 0
- B. x is 0 and y is 1
- C. x is 1 and y is 0
- D. x is 1 and y is 1

gate2021-cse-set1 computer-networks hamming-code

Answer 

Answers: Hamming Code

2.10.1 Hamming Code: GATE CSE 1994 | Question: 9 [top](#)

<https://gateoverflow.in/2505>



- ✓ Here, answer is yes. There is error in This message. Error is in bit 6.

How to calculate it? First of all reverse given input to get it in correct position from 1 to 7.

0110001

Bit-1, Bit-2 & Bit-4 are parity bits.

Calculating position of error \Rightarrow

$c_4 c_2 c_1$

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1 1 0

Here, $c_4 = \text{bit}4 \oplus \text{bit}5 \oplus \text{bit}6 \oplus \text{bit}7 = 0 \oplus 0 \oplus 0 \oplus 1 = 1$
(Taking Even parity)

$c_2 = \text{bit}2 \oplus \text{bit}3 \oplus \text{bit}6 \oplus \text{bit}7 = 1 \oplus 1 \oplus 0 \oplus 1 = 1$

$c_1 = \text{bit}1 \oplus \text{bit}3 \oplus \text{bit}5 \oplus \text{bit}7 = 0 \oplus 1 \oplus 0 \oplus 1 = 0$

Reference: <https://en.wikipedia.org/wiki/Hamming%287,4%29>

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When you correct bit 6.

You get a message as 0110011.

If you calculate c_4, c_2, c_1 all will be 0 now!

References



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21 votes

-- Akash Kanase (36k points)

2.10.2 Hamming Code: GATE CSE 2021 Set 1 | Question: 29 [top](#)

<https://gateoverflow.in/357422>



- ✓ First I wanna point out a mistake here, it says hamming codeword is 12-bit long, but given codeword sequence is of 13-bit due to repetition of d_4 twice (I believe this is a typing error, either they should have write a 13-bit codeword, or d_4 occurs only once in this codeword), also 13-bit codeword is very unlikely as it is given in this question, reason: we put check bits at $2^i \forall i \in N$,

But in the given codeword c_8 is at 9th position taken from RHS)

Case 1: assume it's a 12-bit codeword and d_4 is repeated twice by mistake,

12	11	10	9	8	7	6	5	4	3	2	1
d8	d7	d6	d5	c8	d4	d3	d2	c4	d1	c2	c1
1	c1	1	s	r	0	g	a	v	y	o	u

(1) $c_1 + d_1 + d_2 + d_4 + d_5 + d_7$ should be of even parity

$$= 0 + 1 + 0 + 0 + x + 1 = x + 2,$$

x must be 0 for even parity.

(2) $c_2 + d_1 + d_3 + d_4 + d_6 + d_7$ should be even

$$= 1 + 1 + 1 + 0 + 0 + 1 = 4 \text{ (yes)}$$

(3) $c_4 + d_2 + d_3 + d_4 + d_8$ should be even

$$= 0 + 0 + 1 + 0 + 1 = 2 \text{ (yes even)}$$

(4) $c_8 + d_5 + d_6 + d_7 + d_8$ should be even

$$= y + x + 0 + 1 + 1 = y + 2 \text{ (taking } x=0\text{), for even parity, } y \text{ should be 0}$$

Hence if code work is of 12-bit, both x and y are 0.

A is correct here

Case 2: It's a 13-bit codeword, (I don't think this will be the case, because c_8 should be at position 8), but let's try anyway

13	12	11	10	9	8	7	6	5	4	3	2	1
d8	d7	d6	d5	c8	d4	d4	d3	d2	c4	d1	c2	c1
1	1	0	x	y	0	0	1	0	0	1	1	0

$$(1) c_1 + d_1 + d_2 + d_4 + c_8 + d_6 + d_8 = 0 + 1 + 0 + 0 + y + 0 + 1 = y+2, y \text{ will be 0.}$$

$$(2) c_2 + d_1 + d_3 + d_4 + d_5 + d_6 = 1 + 1 + 1 + 0 + x + 0 = x + 3, x \text{ will be 1}$$

We may conclude C is correct in this case. but I just wanna check it further for other parity bits whether they hold good or not

$$(3) c_4 + d_2 + d_3 + d_4 + d_7 + d_8 = 0 + 0 + 1 + 0 + 1 + 1 = 3 \text{ (odd parity), } c_4 \text{ should be 1 for this to be true, which it isn't)$$

This case fails, so C is definitely not the answer.

5 votes

-- Nikhil Dhamo (2.5k points)

2.11

Icmp (1) [top](#)

2.11.1 Icmp: GATE IT 2005 | Question: 26 [top](#)

<https://gateoverflow.in/3772>



Traceroute reports a possible route that is taken by packets moving from some host A to some other host B. Which of the following options represents the technique used by traceroute to identify these hosts:

- A. By progressively querying routers about the next router on the path to B using ICMP packets, starting with the first router
- B. By requiring each router to append the address to the ICMP packet as it is forwarded to B. The list of all routers en-route to B is returned by B in an ICMP reply packet
- C. By ensuring that an ICMP reply packet is returned to A by each router en-route to B, in the ascending order of their hop distance from A
- D. By locally computing the shortest path from A to B

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[gate2005-it](#) [computer-networks](#) [icmp](#) [application-layer-protocols](#) [normal](#)

Answer

Answers: Icmp

2.11.1 Icmp: GATE IT 2005 | Question: 26 [top](#)

<https://gateoverflow.in/3772>



- ✓ (A) Traceroute works by sending packets with gradually increasing TTL value, starting with TTL value of 1. The first router receives the packet, decrements the TTL value and drops the packet because it then has TTL value zero. The router sends an ICMP Time Exceeded message back to the source. The next set of packets are given a TTL value of 2, so the first router forwards the packets, but the second router drops them and replies with ICMP Time Exceeded. Proceeding in this way, traceroute uses the returned ICMP Time Exceeded messages to build a list of routers that packets traverse, until the destination is reached and returns an ICMP Echo Reply message.

References



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36 votes

-- Shaun Patel (6.1k points)

2.12

Ip Addressing (8) [top](#)



Which of the following assertions is FALSE about the Internet Protocol (IP)?

- A. It is possible for a computer to have multiple IP addresses
- B. IP packets from the same source to the same destination can take different routes in the network
- C. IP ensures that a packet is discarded if it is unable to reach its destination within a given number of hops
- D. The packet source cannot set the route of an outgoing packets; the route is determined only by the routing tables in the routers on the way

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[Answer](#)

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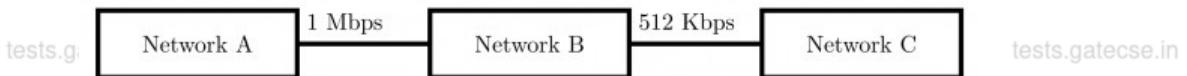


Consider three IP networks A , B and C . Host H_A in network A sends messages each containing 180 bytes of application data to a host H_C in network C . The TCP layer prefixes 20 byte header to the message.

This passes through an intermediate network B . The maximum packet size, including 20 byte IP header, in each network is:

- A: 1000 bytes
- B: 100 bytes
- C: 1000 bytes

The network A and B are connected through a 1 Mbps link, while B and C are connected by a 512 Kbps link (bps = bits per second).



Assuming that the packets are correctly delivered, how many bytes, including headers, are delivered to the IP layer at the destination for one application message, in the best case? Consider only data packets.

- A. 200
- B. 220
- C. 240
- D. 260

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 gate2004-cse computer-networks ip-addressing tcp normal
[Answer](#)

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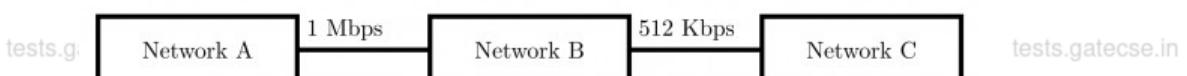


Consider three IP networks A , B and C . Host H_A in network A sends messages each containing 180 *bytes* of application data to a host H_C in network C . The TCP layer prefixes 20 byte header to the message. This passes through an intermediate network B . The maximum packet size, including 20 byte IP header, in each network, is:

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- $A : 1000$ bytes
- $B : 100$ bytes
- $C : 1000$ bytes

The network A and B are connected through a 1 *Mbps* link, while B and C are connected by a 512 *Kbps* link (bps = bits per second).



What is the rate at which application data is transferred to host H_C ? Ignore errors, acknowledgments, and other overheads.

- A. 325.5 Kbps
- B. 354.5 Kbps
- C. 409.6 Kbps
- D. 512.0 Kbps

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Answer **2.12.4 Ip Addressing: GATE CSE 2012 | Question: 23** top  <https://gateoverflow.in/1606>

In the IPv4 addressing format, the number of networks allowed under Class *C* addresses is:

- A. 2^{14}
- B. 2^7
- C. 2^{21}
- D. 2^{24}

Answer **2.12.5 Ip Addressing: GATE CSE 2013 | Question: 37** top  <https://gateoverflow.in/1548>

In an IPv4 datagram, the *M* bit is 0, the value of *HLEN* is 10, the value of total length is 400 and the fragment offset value is 300. The position of the datagram, the sequence numbers of the first and the last bytes of the payload, respectively are:

- A. Last fragment, 2400 and 2789
- B. First fragment, 2400 and 2759
- C. Last fragment, 2400 and 2759
- D. Middle fragment, 300 and 689

Answer **2.12.6 Ip Addressing: GATE CSE 2014 Set 3 | Question: 27** top  <https://gateoverflow.in/2061>

Every host in an IPv4 network has a $1 - \text{second}$ resolution real-time clock with battery backup. Each host needs to generate up to 1000 unique identifiers per second. Assume that each host has a globally unique IPv4 address. Design a 50-bit globally unique ID for this purpose. After what period (in seconds) will the identifiers generated by a host wrap around?

Answer **2.12.7 Ip Addressing: GATE CSE 2017 Set 2 | Question: 20** top  <https://gateoverflow.in/118427>

The maximum number of IPv4 router addresses that can be listed in the record route (RR) option field of an IPv4 header is _____.

Answer **2.12.8 Ip Addressing: GATE CSE 2018 | Question: 54** top  <https://gateoverflow.in/204129>

Consider an IP packet with a length of 4,500 bytes that includes a 20-byte IPv4 header and 40-byte TCP header. The packet is forwarded to an IPv4 router that supports a Maximum Transmission Unit (MTU) of 600 bytes. Assume that the length of the IP header in all the outgoing fragments of this packet is 20 bytes. Assume that the fragmentation offset value stored in the first fragment is 0.

The fragmentation offset value stored in the third fragment is _____.

Answer **Answers: Ip Addressing**



- ✓ In computer networking, source routing, also called path addressing, allows a sender of a packet to partially or completely specify the route of the packet takes through the network. In contrast, in non-source routing protocols, routers in the network determine the path based on the packet's destination.

http://en.wikipedia.org/wiki/Source_routing

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Answer is D.

References



35 votes

-- Priya_das (603 points)



- ✓ Packet A sends an IP packet of 180 bytes of data +20 bytes of TCP header +20 bytes of IP header to B.

IP layer of B now removes 20 bytes of IP header and has 200 bytes of data. So, it makes 3 IP packets - [80 + 20, 80 + 20, 40 + 20] and sends to C as the IP packet size of B is 100. So, C receives 260 bytes of data which includes 60 bytes of IP headers and 20 bytes of TCP header.

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For data rate, we need to consider only the slowest part of the network as data will be getting accumulated at that sender (data rate till that slowest part, we need to add time if a faster part follows a slower part).

So, here 180 bytes of application data are transferred from A to C and this causes 260 bytes to be transferred from B to C.

Correct Answer: D

70 votes

-- Arjun Suresh (332k points)



- ✓ Packet A sends an IP packet of 180 bytes of data + 20 bytes of TCP header + 20 bytes of IP header to B .

IP layer of B now removes 20 bytes of IP header and has 200 bytes of data. So, it makes 3 IP packets - [80 + 20, 80 + 20, 40 + 20] and sends to C as the IP packet size of B is 100. So, C receives 260 bytes of data which includes 60 bytes of IP headers and 20 bytes of TCP header.

For data rate, we need to consider only the slowest part of the network as data will be getting accumulated at that sender (data rate till that slowest part, we need to add time if a faster part follows a slower part).

So, here 180 bytes of application data are transferred from A to C and this causes 260 bytes to be transferred from B to C.

$$\text{Time to transfer 260 bytes from B-C} = \frac{260 \times 8}{(512 \times 1000)}$$

$$= \frac{65}{16000} = \frac{13}{3200}.$$

$$\text{So, data rate} = \frac{180 \times 3200}{13} = 44.3 \text{ kBps} = 44.3 \times 8 = 354.46 \text{ kbps.}$$

Correct Answer: B

67 votes

-- Arjun Suresh (332k points)



- ✓ Answer is (c)

Class	Leading Bits	Size of network number bit field	Size of rest bit field	Number of networks	Addresses per network	Total Addresses in class	Start address	End address
Class A	0	8	24	128 (2^7)	16,777,216 (2^{24})	2,147,483,648 (2^{31})	0.0.0.0	127.255.255.255
Class B	10	16	16	16,384 (2^{14})	65,536 (2^{16})	1,073,741,824 (2^{30})	128.0.0.0	191.255.255.255
Class C	110	24	8	2,097,152 (2^{21})	256 (2^8)	536,870,912 (2^{29})	192.0.0.0	223.255.255.255
Class D	1110	Not defined	Not defined	Not defined	Not defined	268,435,456 (2^{28})	224.0.0.0	239.255.255.255
Class E	1111	Not defined	Not defined	Not defined	Not defined	268,435,456 (2^{28})	240.0.0.0	255.255.255.255

We have 32 bits in the IPv4 network

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Class A = 8 network bits + 24 Host bits

Class B = 16 network bits + 16 Host bits

Class C = 24 network bits + 8 host bits

Class D ([multicast](#))

Now for Class C we have 3 bits reserved for the network id.

Hence remaining bits are 21. Therefore total number of networks possible are 2^{21} .

Similarly in Class B we have 2 bits reserved.

Hence, total number of networks in Class B are 2^{14} .

And we have 1 bit reserved in Class A, therefore there are 2^7 networks.

A better reasoning for the bit reservation is given at: https://en.wikipedia.org/wiki/Classful_network

References



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53 votes

-- Gate Keeda (15.9k points)

2.12.5 Ip Addressing: GATE CSE 2013 | Question: 37 top

→ <https://gateoverflow.in/1548>



- ✓ $M = 0$ meaning no more fragments after this. Hence, its the last fragment.

IHL = internet header length = $10 \times 4 = 40B$ coz 4 is the scaling factor for this field.

Total Length = $400B$

Payload size = Total length - Header length = $400 - 40 = 360B$

fragment offset = $300 \times 8 = 2400B$ = represents how many Bytes are before this. 8 is the scaling factor here.
 \therefore the first byte # = 2400

Last byte # = first byte # + total bytes in payload - 1 = $2400 + 360 - 1 = 2759$

Option C is correct.

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76 votes

-- Amar Vashishth (25.2k points)

2.12.6 Ip Addressing: GATE CSE 2014 Set 3 | Question: 27 top

→ <https://gateoverflow.in/2061>



- ✓ Each host needs to generate 1000 unique identifiers per second which requires $\lceil \lg 1000 \rceil = 10$ bits.

Now, these 10 bits along with 32 bit globally unique IP address will give a globally unique 42 bit IDs which stays constant.

Since we are allowed 50 bits we can use the next 8 bits using the clock which changes every second. Thus our IDs will wrap around once in $2^8 = 256$ seconds.

12 votes

-- gatecse (63.3k points)



- ✓ A record-route (RR) option is used to record the Internet routers that handle the datagram. It is listed in OPTIONS of IPv4.

According to RFC 791, there are two cases for the format of an option:

- Case 1: A single octet of option-type.
- Case 2: An option-type octet, an option-length octet, and the actual option-data octets.

In both the cases, first 16 bits of OPTIONS field is used. Therefore, out of 40 Bytes only 38 Bytes are remaining for storing IPv4 addresses. In 38 Bytes we can store 9 IPv4 addresses as each IPv4 address is of 4 Bytes.

$\therefore 9$ should be answer.

Reference: <https://tools.ietf.org/html/rfc791>

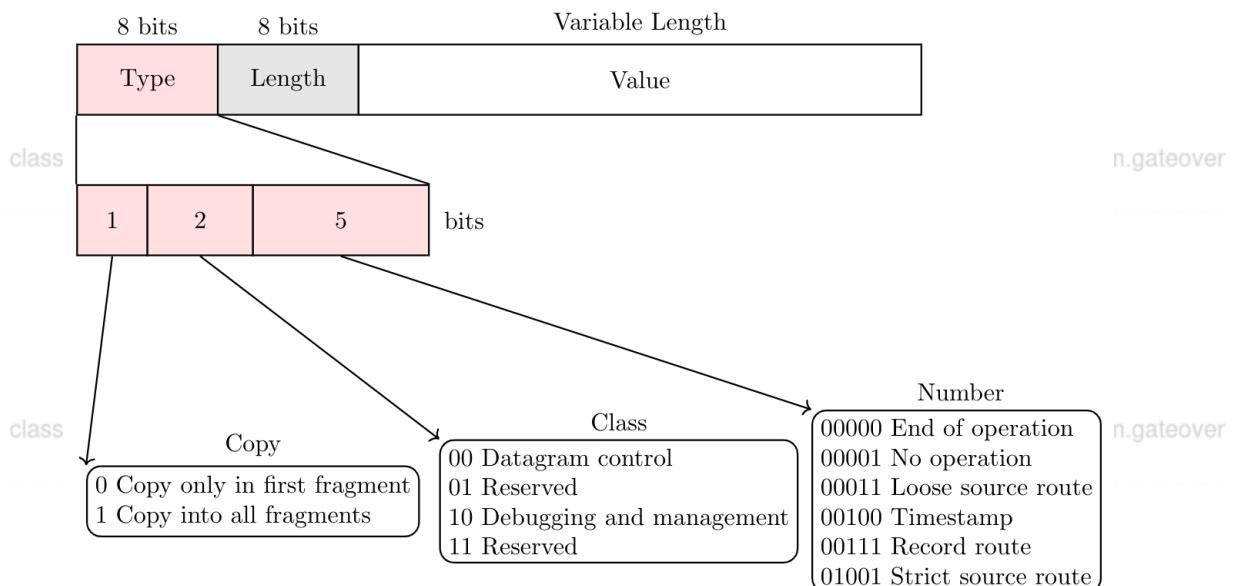


Fig: Option format

References



58 votes

-- Kantikumar (3.4k points)



- ✓ Packet Length = $4500B$
IP Payload = $4500 - 20 = 4480B$

$$\text{MTU} = 600B$$

$$\text{MTU Payload} = 600B - 20B = 580B$$

But payload should be multiple of 8 so number nearest to 580 and multiple of 8 is 576, so MTU payload = $576B$

$$\text{IP Packet size} = 576 + 20B = 596B$$

$$\text{Size of Offset} = \frac{576}{8} = 72$$

$$1^{\text{st}} \text{ fragment offset} = 0$$

$$2^{\text{nd}} \text{ fragment offset} = 72$$

$$3^{\text{rd}} \text{ fragment offset} = 144$$

62 votes

-- Digvijay (44.9k points)

IP Packet = Data + Header

i.e $4500 \text{ bytes} = 4480 \text{ (Data)} + 20 \text{ (Header) bytes}$ [Given]

Now **MTU** is 600 bytes.

MTU includes Data + Header

∴ Max data that can be sent is 580 bytes.

However, the total length should be a multiple of 8 (except for the last fragment), because this number will be stored in the Fragmentation offset, which specifies the number of bytes ahead of this fragment.

The nearest number to 580 which is a multiple of 8 is 576

Therefore, the fragmentation will be done in this way ⇒

Fragment#	1	2	3	4	5	6	7	8
Data(B)	576	576	576	576	576	576	576	448
Header Length(B)	20	20	20	20	20	20	20	20
Total Length(B)	596	596	596	596	596	596	596	468
Fragment Offset(B)	0	72	144	216	288	360	432	504
More Fragment	1	1	1	1	1	1	1	0

Since they have mentioned that the first fragment has an offset of 0, the third fragment has an offset value of 144.

1 like 31 votes

-- Neelay Upadhyaya (1.1k points)

2.13

Ip Packet (8) [top](#)

2.13.1 Ip Packet: GATE CSE 2006 | Question: 5 [top](#)

<https://gateoverflow.in/884>



For which one of the following reasons does internet protocol(IP) use the time-to-live(TTL) field in IP datagram header?

- A. Ensure packets reach destination within that time
- B. Discard packets that reach later than that time
- C. Prevent packets from looping indefinitely
- D. Limit the time for which a packet gets queued in intermediate routers

[gate2006-cse](#) [computer-networks](#) [ip-addressing](#) [ip-packet](#) [easy](#)

Answer

2.13.2 Ip Packet: GATE CSE 2010 | Question: 15. PGEE 2018 [top](#)

<https://gateoverflow.in/2188>



One of the header fields in an IP datagram is the Time-to-Live (TTL) field. Which of the following statements best explains the need for this field?

- A. It can be used to prioritize packets.
- B. It can be used to reduce delays.
- C. It can be used to optimize throughput.
- D. It can be used to prevent packet looping.

[gate2010-cse](#) [computer-networks](#) [ip-packet](#) [easy](#)

Answer

2.13.3 Ip Packet: GATE CSE 2014 Set 3 | Question: 25 [top](#)

<https://gateoverflow.in/2059>



Host A (on TCP/IP v4 network A) sends an IP datagram D to host B (also on TCP/IP v4 network B). Assume that no error occurred during the transmission of D. When D reaches B, which of the following IP header field(s) may be different from that of the original datagram D?

- i. TTL
 - ii. Checksum
 - iii. Fragment Offset
- A. i only

- B. i and ii only
 C. ii and iii only
 D. i, ii and iii

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Answer ↗

2.13.4 Ip Packet: GATE CSE 2014 Set 3 | Question: 28 top ↵

↗ <https://gateoverflow.in/2062>



An IP router with a Maximum Transmission Unit (MTU) of 1500 bytes has received an IP packet of size 4404 bytes with an IP header of length 20 bytes. The values of the relevant fields in the header of the third IP fragment generated by the router for this packet are:

- A. MF bit: 0, Datagram Length: 1444; Offset: 370
 B. MF bit: 1, Datagram Length: 1424; Offset: 185
 C. MF bit: 1, Datagram Length: 1500; Offset: 370
 D. MF bit: 0, Datagram Length: 1424; Offset: 2960

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Answer ↗

2.13.5 Ip Packet: GATE CSE 2015 Set 1 | Question: 22 top ↵

↗ <https://gateoverflow.in/8220>



Which of the following fields of an IP header is NOT modified by a typical IP router?

- A. Check sum
 B. Source address
 C. Time to Live (TTL)
 D. Length

gate2015-cse-set1 computer-networks ip-packet easy

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Answer ↗

2.13.6 Ip Packet: GATE CSE 2015 Set 2 | Question: 52 top ↵

↗ <https://gateoverflow.in/8255>



Host A sends a UDP datagram containing 8880 bytes of user data to host B over an Ethernet LAN. Ethernet frames may carry data up to 1500 bytes (i.e. MTU = 1500 bytes). Size of UDP header is 8 bytes and size of IP header is 20 bytes. There is no option field in IP header. How many total number of IP fragments will be transmitted and what will be the contents of offset field in the last fragment?

- A. 6 and 925
 B. 6 and 7400
 C. 7 and 1110
 D. 7 and 8880

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tests.gatecse.in

Answer ↗

2.13.7 Ip Packet: GATE CSE 2016 Set 1 | Question: 53 top ↵

↗ <https://gateoverflow.in/39712>



An IP datagram of size 1000 bytes arrives at a router. The router has to forward this packet on a link whose MTU (maximum transmission unit) is 100 bytes. Assume that the size of the IP header is 20 bytes.

The number of fragments that the IP datagram will be divided into for transmission is _____.

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Answer ↗



In the TCP/IP protocol suite, which one of the following is NOT part of the IP header?

- A. Fragment Offset
- B. Source IP address
- C. Destination IP address
- D. Destination port number

[gate2004-it](#) [computer-networks](#) [ip-packet](#) [normal](#)

[Answer](#)

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Answers: Ip Packet



- ✓ Answer: C

The standard header that is used in *IPv4* contains key information about an Internet Protocol (IP) packet. Information includes the source and destination IP addresses of the datagram, fragmentation control parameters, and packet length. Another key element of this header is the TTL field. The TTL field consists of a single byte and is capable of holding a value from 0–255.

Because IP is connectionless, the TTL field was included in the IP header by the original designers as a mechanism to limit the life span of packets within the network. A routing loop is the most common example used to illustrate why this functionality is required. Without such a control mechanism, a routing loop could cause a packet to circle a network infinitely, depleting bandwidth and eventually destabilizing the network. As insurance against this outcome, the TTL value of an IP datagram is decremented by a value of one each time the packet is forwarded by a network device. Thus, an IP packet can never be forwarded more than 254 times, preventing the infinite packet loop problem.

https://tools.cisco.com/security/center/resources/ttl_expiry_attack.html

References



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9 votes

-- Deepak Poonia (23.4k points)

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- ✓ Answer is (D). It can be used to prevent packet looping.

31 votes

-- Sankaranarayanan P.N (8.5k points)



- ✓ The answer is OPTION D.

Whenever an IP packet is transmitted, the value in Time to Live (TTL) field will be decremented on every single hop. Hence, TTL is changed on every hop.

Now, since TTL changes, hence the Checksum of the packet will also change.

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For the Fragmentation offset, A packet will be fragmented if the packet has a size greater than the Maximum Transmission Unit (MTU) of the network. Hence, Fragmentation offset can also be changed.

77 votes

-- saurabhrk (1k points)



- ✓ IP packet length is given 4404 which includes ip header of length 20
So, data is 4384.

Now, router divide this data in 3 parts
1480 1480 1424

After adding ip header in last packet size is: 1444 and since its the last packet therefore $MF = 0$

And offset is $\frac{2960}{8} = 370$

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Correct Answer: A



61 votes

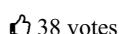
-- anmolgate (207 points)



2.13.5 Ip Packet: GATE CSE 2015 Set 1 | Question: 22 [top](#) [b](#)

<https://gateoverflow.in/8220>

✓ Source Address.



38 votes

-- Arjun Suresh (332k points)



2.13.6 Ip Packet: GATE CSE 2015 Set 2 | Question: 52 [top](#) [b](#)

<https://gateoverflow.in/8255>

✓ Answer is C.

$$\text{Number of fragments} = \left\lceil \frac{8888}{1480} \right\rceil = 7$$

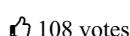
$$\text{Offset of last fragment} = \frac{(1500 - 20) \times 6}{8} = 1110$$

(scaling factor of 8 is used in offset field).

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TCP or UDP header will be added to the DataUnit received from Transport Layer to Network Layer. And fragmentation happens at Network Layer. So no need to add TCP or UDP header into each fragment.



108 votes

-- Vikrant Singh (11.2k points)



2.13.7 Ip Packet: GATE CSE 2016 Set 1 | Question: 53 [top](#) [b](#)

<https://gateoverflow.in/3972>

✓ IP Datagram size = 1000B

MTU = 100B

IP header size = 20B

So, each packet will have 20B header + 80B payload.

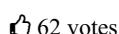
Therefore, $80 \times 12 = 960$

now remaining 20B data could be sent in next fragment.

So, total $12 + 1 = 13$ fragments.

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62 votes

-- Monanshi Jain (7k points)

MTU (M) is $80 + 20$ bytes

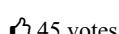
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Datagram size (DS) is $980 + 20$

$$\text{No. of fragments} = \frac{\text{DS}}{\text{M}} = \frac{980}{80} = 12.25$$

So Answer is 13.



45 votes

-- G VENKATESWARLU (461 points)



2.13.8 Ip Packet: GATE IT 2004 | Question: 86 [top](#) [b](#)

<https://gateoverflow.in/3730>

✓ Answer is D: Destination Port number.

Why? Because the IP header has nothing to do with the port number.

Port numbers are used by the transport layer to ensure process to process delivery.

2.14

Lan Technologies (6) [top](#)

2.14.1 Lan Technologies: GATE CSE 2003 | Question: 83 [top](#)

<https://gateoverflow.in/966>



A 2 km long broadcast LAN has 10^7 bps bandwidth and uses CSMA/CD. The signal travels along the wire at 2×10^8 m/s. What is the minimum packet size that can be used on this network?

- A. 50 bytes
- B. 100 bytes
- C. 200 bytes
- D. None of the above

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gate2003-cse computer-networks lan-technologies normal

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[Answer](#)

2.14.2 Lan Technologies: GATE CSE 2007 | Question: 65 [top](#)

<https://gateoverflow.in/1263>



There are n stations in slotted LAN. Each station attempts to transmit with a probability p in each time slot. What is the probability that **ONLY** one station transmits in a given time slot?

- A. $np(1-p)^{n-1}$
- B. $(1-p)^{n-1}$
- C. $p(1-p)^{n-1}$
- D. $1 - (1-p)^{n-1}$

gate2007-cse computer-networks lan-technologies probability normal

[Answer](#)

2.14.3 Lan Technologies: GATE CSE 2019 | Question: 49 [top](#)

<https://gateoverflow.in/302799>



tests.gatecse.in Consider that 15 machines need to be connected in a LAN using 8-port Ethernet switches. Assume that these switches do not have any separate uplink ports. The minimum number of switches needed is _____

gate2019-cse numerical-answers computer-networks lan-technologies

[Answer](#)

2.14.4 Lan Technologies: GATE IT 2004 | Question: 27 [top](#)

<https://gateoverflow.in/3668>



A host is connected to a Department network which is part of a University network. The University network, in turn, is part of the Internet. The largest network in which the Ethernet address of the host is unique is

- A. the subnet to which the host belongs
- B. the Department network
- C. the University network
- D. the Internet

gate2004-it computer-networks lan-technologies ethernet normal

[Answer](#)

2.14.5 Lan Technologies: GATE IT 2005 | Question: 28 [top](#)

<https://gateoverflow.in/3774>



Which of the following statements is FALSE regarding a bridge?

- A. Bridge is a layer 2 device
- B. Bridge reduces collision domain
- C. Bridge is used to connect two or more LAN segments
- D. Bridge reduces broadcast domain

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Answer **2.14.6 Lan Technologies: GATE IT 2006 | Question: 66** top ↗<https://gateoverflow.in/3610>

A router has two full-duplex Ethernet interfaces each operating at 100 Mb/s. Ethernet frames are at least 84 bytes long (including the Preamble and the Inter-Packet-Gap). The maximum packet processing time at the router for wirespeed forwarding to be possible is (in microseconds)

- A. 0.01
- B. 3.36
- C. 6.72
- D. 8

<tests.gatecse.in><goclasses.in><tests.gatecse.in>Answer **Answers: Lan Technologies****2.14.1 Lan Technologies: GATE CSE 2003 | Question: 83** top ↗<https://gateoverflow.in/966>

- ✓ In CSMA/CD, to detect a collision the transmission time (which depends on the packet size) must be greater than twice the propagation delay.

$$\text{Propagation delay here} = \frac{2km}{2 \times 10^8 m/s} = 10 \text{ microseconds}$$

$$\text{Now, transmission time for } x \text{ bytes} = \frac{x \times 8}{10^7} = 0.8x \text{ microseconds}$$

So, $0.8x > 2 \times 10 \implies x > 25 \text{ bytes}$

So, None of these.

Correct Answer: **D**

 33 votes

-- Arjun Suresh (332k points)

2.14.2 Lan Technologies: GATE CSE 2007 | Question: 65 top ↗<https://gateoverflow.in/1263>

- ✓ Probability that only one station transmits in a given slot = $\binom{n}{1} p^1 (1-p)^{n-1}$

Answer is **option A**.

p for 1 transmitting and $(1-p)$ for $n-1$ non transmitting and n ways to choose 1 from n .

 42 votes

-- Aditi Dan (4k points)

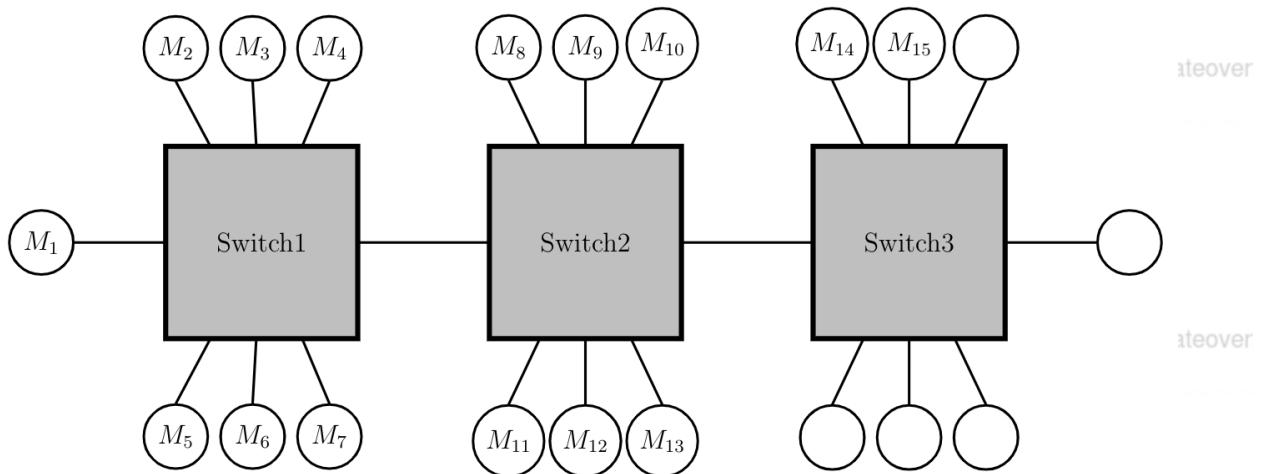
2.14.3 Lan Technologies: GATE CSE 2019 | Question: 49 top ↗<https://gateoverflow.in/302799>

- ✓ Answer is 3.

Using 3 switches we can connect maximum 20 machines together.

∴ We require at least 3 switches to connect 15 machines.

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32 votes

-- Tuhin Dutta (9.2k points)

2.14.4 Lan Technologies: GATE IT 2004 | Question: 27 top

<https://gateoverflow.in/3668>



- ✓ Answer is D, Ethernet address is nothing but MAC Address which is present on NIC and it is unique for every network device (a single system might have multiple network cards and each can have its own MAC address).

PS: We can never say Ethernet address is unique only in a network -- because it is independent of the network a device is connected to. That is, if we move a device from one network to another, MAC address remains same. Of course we can do spoofing, but this is not relevant to the asked question.

53 votes

-- Pradyumna Paralikar (297 points)

2.14.5 Lan Technologies: GATE IT 2005 | Question: 28 top

<https://gateoverflow.in/3774>



- ✓ Bridges are DataLink layer devices used to connect LANs. Bridges are collision domain separator but unable to separate Broadcast domain.

21 votes

-- Digvijay (44.9k points)

2.14.6 Lan Technologies: GATE IT 2006 | Question: 66 top

<https://gateoverflow.in/3610>



- ✓ Two full-duplex Ethernet interfaces operating at 100 Mbps means the total data transfer rate to the router is 200 Mbps. (Whether full duplex or half, we just need to consider the bandwidth as that determines the speed of data arrival to the router.)

Maximum packet processing time allowed for wirespeed (no delay) forwarding = $\frac{84 \times 8}{200} \mu s = 3.36 \mu s$.

(The router operating at wirespeed means it should be fast enough to process the incoming traffic without causing a delay for transmission)

10 votes

-- gatecse (63.3k points)

Here router has two incoming/outgoing hardware that is full-duplex which means we can send and receive at the same time.

Transmission time is 6.72 (How to get this Transmission time = Packet size / Bandwidth)

Transmission time is time for a packet to get out/in of wire. Also, assume even though the router has two incoming/outgoing hardware but it has a single processing unit.

Now assume that at $t = 0$ router is free. At $t = 6.72$ two packets, p_1 & p_2 arrived from two incoming/outgoing hardware. Now next slot of two packets will arrive at $6.72 + 6.72$ before that processing of these two packets must be completed so that there will not be any kind of delay. Hence we just have 6.72 maximum times to process each packet, hence for each packet, we can devote a maximum of 3.36.

Hence the answer is 3.36.

Now for further explanation, I will show when the first two packets are processed. At $t = 0$ both packets start coming out of

wire, at $t = 6.72$ both packets completely coming out of wire, and we start the processing of one of them (let's say p_1) and next packets p_3, p_4 starts coming out.

At $t = 6.72 + 3.36$ processing of p_1 done, start transmitting it through port 1.

At $t = 6.72 + 6.72$ processing of p_2 done start transmitting it through port 2.

At this time next packets p_3 & p_4 arrived, and we start processing one of them (let's say p_3), at $t=6.72+6.72+3.36$ p_1 completely transmitted., processing of p_3 done, start transmitting it through port 1 (as port 2 is busy in transmitting packet 2)

At $t = 6.72 + 6.72 + 6.72$ transmitting of p_2 done. processing of p_4 done starts transmitting it through port 2, next packets p_5 & p_6 arrived.

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124 votes

-- mehul vaidya (3.8k points)

2.15

Link State Routing (1) [top](#)

2.15.1 Link State Routing: GATE CSE 2014 Set 1 | Question: 23 [top](#)

<https://gateoverflow.in/1790>



Consider the following three statements about link state and distance vector routing protocols, for a large network with 500 network nodes and 4000 links.

[S1]: The computational overhead in link state protocols is higher than in distance vector protocols.

[S2]: A distance vector protocol (with split horizon) avoids persistent routing loops, but not a link state protocol.

[S3]: After a topology change, a link state protocol will converge faster than a distance vector protocol.

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Which one of the following is correct about S1, S2, and S3?

- A. S1, S2, and S3 are all true.
- B. S1, S2, and S3 are all false.
- C. S1 and S2 are true, but S3 is false.
- D. S1 and S3 are true, but S2 is false.

gate2014-cse-set1 computer-networks routing distance-vector-routing link-state-routing normal

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Answer

Answers: Link State Routing

2.15.1 Link State Routing: GATE CSE 2014 Set 1 | Question: 23 [top](#)

<https://gateoverflow.in/1790>



✓ The computational overhead in link state protocols is higher than in distance vector protocols. Bcz LSR is based upon global knowledge whereas DVR is based upon Local info .

Persistent looping can be avoid with the help of split horizon in DVR.But there is no concept of persistent looping in LSR, in LSR only temporary loop exist and can automatically solved by system or router. S2 is false.

And, after a topology change, a link state protocol will converge faster than a distance vector protocol. S3 is true.

Answer is option D.

53 votes

-- Paras Singh (8.9k points)

2.16

Mac Protocol (4) [top](#)

2.16.1 Mac Protocol: GATE CSE 2005 | Question: 74 [top](#)

<https://gateoverflow.in/1397>



Suppose the round trip propagation delay for a 10 Mbps Ethernet having 48-bit jamming signal is $46.4 \mu s$. The minimum frame size is:

- A. 94
- B. 416

- C. 464
D. 512

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gate2005-cse computer-networks mac-protocol ethernet

Answer ↗

2.16.2 Mac Protocol: GATE CSE 2015 Set 2 | Question: 8 [top ↗](#)

↗ <https://gateoverflow.in/8056>



A link has transmission speed of 10^6 bits/sec. It uses data packets of size 1000 bytes each. Assume that the acknowledgment has negligible transmission delay and that its propagation delay is the same as the data propagation delay. Also, assume that the processing delays at nodes are negligible. The efficiency of the stop-and-wait protocol in this setup is exactly 25%. The value of the one way propagation delay (in milliseconds) is _____.

gate2015-cse-set2 computer-networks mac-protocol stop-and-wait normal numerical-answers

Answer ↗

2.16.3 Mac Protocol: GATE IT 2004 | Question: 85 [top ↗](#)

↗ <https://gateoverflow.in/3729>



Consider a simplified time slotted MAC protocol, where each host always has data to send and transmits with probability $p = 0.2$ in every slot. There is no backoff and one frame can be transmitted in one slot. If more than one host transmits in the same slot, then the transmissions are unsuccessful due to collision. What is the maximum number of hosts which this protocol can support if each host has to be provided a minimum throughput of 0.16 frames per time slot?

- A. 1
B. 2
C. 3
D. 4

gate2004-it computer-networks congestion-control mac-protocol normal

Answer ↗

2.16.4 Mac Protocol: GATE IT 2005 | Question: 75 [top ↗](#)

↗ <https://gateoverflow.in/3838>



In a TDM medium access control bus LAN, each station is assigned one time slot per cycle for transmission. Assume that the length of each time slot is the time to transmit 100 bits plus the end-to-end propagation delay. Assume a propagation speed of $2 \times 10^8 \text{ m/sec}$. The length of the LAN is 1 km with a bandwidth of 10 Mbps. The maximum number of stations that can be allowed in the LAN so that the throughput of each station can be $2/3$ Mbps is

- A. 3
B. 5
C. 10
D. 20

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gate2005-it computer-networks mac-protocol normal

Answer ↗

Answers: Mac Protocol

2.16.1 Mac Protocol: GATE CSE 2005 | Question: 74 [top ↗](#)

↗ <https://gateoverflow.in/1397>



- ✓ The sender must be able to detect a collision before completely sending a frame.
So, the minimum frame length must be such that, before the frame completely leaves the sender any collision must be detected.

Now, the worst case for collision detection is when the start of the frame is about to reach the receiver and the receiver starts sending. Collision happens and a jam signal is produced and this signal must travel to the sender.

The time for this will be the time for the start of the frame to reach near the receiver + time for the jam signal to reach the sender + transmission time for the jam signal.

(We do not need to include transmission time for the frame as soon as the first bit of the frame arrives, the receiver will have detected it). Time for the start of the frame to reach near the receiver + Time for the jam signal to reach the sender = Round trip propagation delay = $46.4\mu\text{s}$. So,

$$46.4 + \frac{48}{10} (48 \text{ bits at } 10 \text{ Mbps takes } 4.8 \text{ micro sec.}) = 51.2 \mu\text{s}.$$

Now, the frame length must be such that its transmission time must be more than $51.2 \mu\text{s}$.

So, minimum frame length = $51.2 \times 10^{-6} \times 10 \times 10^6 = 512 \text{ bits}$.

- <http://gatcse.in/w/images/3/32/3-MACSublayer.ppt>

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A reference question from Peterson Davie:

43. Suppose the round-trip propagation delay for Ethernet is $46.4 \mu\text{s}$. This yields a minimum packet size of 512 bits (464 bits corresponding to propagation delay +48 bits of jam signal).

- What happens to the minimum packet size if the delay time is held constant, and the signaling rate rises to 100 Mbps?
- What are the drawbacks to so large a minimum packet size?
- If compatibility were not an issue, how might the specifications be written so as to permit a smaller minimum packet size?

Another reference for requiring jam signal bits to be included for minimum frame size.

- <http://intronetworks.cs.luc.edu/current/html/ethernet.html>

Can collision be detected by the source without getting the full jam signal (by a change in current)?

Probably yes. But to be safe (from signal loss) the source waits for the entire jam signal. See below link

- <http://superuser.com/questions/264171/collisions-in-csma-cd-etherne>

Correct Answer: D.

References



108 votes

-- Arjun Suresh (332k points)

2.16.2 Mac Protocol: GATE CSE 2015 Set 2 | Question: 8

• <https://gateoverflow.in/8056>



- ✓ In stop and wait, a frame is sent and next frame will be sent only after ACK is received.

$$\text{Efficiency} = \frac{\text{Amount of data sent}}{\text{Amount of data that could be sent}}$$

$$= \frac{\text{Amount of data sent}}{\text{RTT} \times 10^6}$$

$$= \frac{\text{Amount of data sent}}{(\text{Prop. delay for data} + \text{Prop. delay for ACK} + \text{Transmission time for data} + \text{Transmission time for ACK}) \times 10^6}$$

$$= \frac{1000 \times 8}{\left(p + p + 1000 \times \frac{8}{10^6} + 0\right) \times 10^6}$$

$$= \frac{8}{2p + 8ms} \text{ (where p is the prop. delay in milli seconds)}$$

$$= \frac{4}{p + 4} = 0.25 \text{ (given in question)}$$

$$\text{So, } p + 4 = 16, p = 12ms.$$

41 votes

-- Arjun Suresh (332k points)

2.16.3 Mac Protocol: GATE IT 2004 | Question: 85 top ↗

→ <https://gateoverflow.in/3729>



- ✓ Let there be N such hosts.

Then when one host is transmitting then others must be silent for successful transmission.
So the throughput per host

$$0.16 = 0.2 \times 0.8^{N-1}$$

$$\implies 0.8 = 0.8^{N-1}$$

on comparing the exponents, since base are identical

$$N - 1 = 1, N = 2.$$

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Correct Answer: *B*

42 votes

-- Shreyans Dhankhar (2.1k points)

2.16.4 Mac Protocol: GATE IT 2005 | Question: 75 top ↗

→ <https://gateoverflow.in/3838>



- ✓ $T_t = 10$ micro secs

$$T_p = 5 \text{ micro secs}$$

$$\text{Efficiency of the network} = \frac{T_t}{(T_t + T_p)} = \frac{10}{15} = \frac{2}{3}.$$

Total throughput available for the entire network = Efficiency \times Bandwidth

$$= \frac{2}{3} \times 10 \text{ Mbps} = \frac{20}{3} \text{ Mbps}$$

Let, No. of stations = N (each wants a Throughput of $\frac{2}{3}$ Mbps),

$$N \times \frac{2}{3} \text{ Mbps} = \frac{20}{3} \text{ Mbps} \Rightarrow N = 10.$$

\Rightarrow 10 stations can be connected in the channel at max.

Correct Answer: *C*

42 votes

-- Ravi Ranjan (3k points)

2.17

Network Flow (5) top ↗

2.17.1 Network Flow: GATE CSE 1992 | Question: 01, v top ↗

→ <https://gateoverflow.in/550>



A simple and reliable data transfer can be accomplished by using the 'handshake protocol'. It accomplishes reliable data transfer because for every data item sent by the transmitter _____.

gate1992 computer-networks network-flow easy fill-in-the-blanks

Answer

2.17.2 Network Flow: GATE CSE 2017 Set 2 | Question: 35 top ↗

→ <https://gateoverflow.in/118537>



Consider two hosts X and Y , connected by a single direct link of rate 10^6 bits/sec . The distance between the two hosts is $10,000 \text{ km}$ and the propagation speed along the link is $2 \times 10^8 \text{ m/sec}$. Host X sends a file of $50,000 \text{ bytes}$ as one large message to host Y continuously. Let the transmission and propagation delays be p milliseconds and q milliseconds respectively. Then the value of p and q are

- A. $p = 50$ and $q = 100$
- B. $p = 50$ and $q = 400$
- C. $p = 100$ and $q = 50$

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D. $p = 400$ and $q = 50$

gate2017-cse-set2 computer-networks network-flow

Answer 

2.17.3 Network Flow: GATE IT 2004 | Question: 80 [top](#) <https://gateoverflow.in/3724> 

In a data link protocol, the frame delimiter flag is given by 0111. Assuming that bit stuffing is employed, the transmitter sends the data sequence 01110110 as

- A. 01101011
- B. 011010110
- C. 011101100
- D. 0110101100

gate2004-it computer-networks network-flow normal

Answer 

2.17.4 Network Flow: GATE IT 2004 | Question: 87 [top](#) <https://gateoverflow.in/3731> 

A TCP message consisting of 2100 bytes is passed to IP for delivery across two networks. The first network can carry a maximum payload of 1200 bytes per frame and the second network can carry a maximum payload of 400 bytes per frame, excluding network overhead. Assume that IP overhead per packet is 20 bytes. What is the total IP overhead in the second network for this transmission?

- A. 40 bytes
- B. 80 bytes
- C. 120 bytes
- D. 160 bytes

gate2004-it computer-networks network-flow normal

Answer 

2.17.5 Network Flow: GATE IT 2006 | Question: 67 [top](#) <https://gateoverflow.in/3611> 

A link of capacity 100 Mbps is carrying traffic from a number of sources. Each source generates an on-off traffic stream; when the source is on, the rate of traffic is 10 Mbps, and when the source is off, the rate of traffic is zero. The duty cycle, which is the ratio of on-time to off-time, is 1 : 2. When there is no buffer at the link, the minimum number of sources that can be multiplexed on the link so that link capacity is not wasted and no data loss occurs is $S1$. Assuming that all sources are synchronized and that the link is provided with a large buffer, the maximum number of sources that can be multiplexed so that no data loss occurs is $S2$. The values of $S1$ and $S2$ are, respectively,

- A. 10 and 30
- B. 12 and 25
- C. 5 and 33
- D. 15 and 22

gate2006-it computer-networks network-flow normal

Answer 

Answers: Network Flow

2.17.1 Network Flow: GATE CSE 1992 | Question: 01,v [top](#) <https://gateoverflow.in/550> 

- ✓ The receiver responds that it is ready to receive the data item.

Reference: http://www.sqa.org.uk/e-learning/NetInf101CD/page_28.htm
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References



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👉 9 votes

-- Rajarshi Sarkar (27.9k points)

2.17.2 Network Flow: GATE CSE 2017 Set 2 | Question: 35<https://gateoverflow.in/118537>

✓ $T_t = \frac{\text{Length}}{\text{Bandwidth}}$
 $= \frac{50000 \times 8}{10^6}$
 $= \frac{40}{100} = 0.4s = 400 \text{ ms}$

$T_p = \frac{\text{Distance}}{\text{Velocity}}$
 $= \frac{10000 \times 10^3}{2 \times 10^8}$
 $= \frac{1}{20} = 0.05s = 50 \text{ ms}$

Hence, answer **(D)** $p = 400, q = 50$.

👉 30 votes

-- Arnabi Bej (5.8k points)

2.17.3 Network Flow: GATE IT 2004 | Question: 80<https://gateoverflow.in/3724>

- ✓ The answer will be option **D**.

The bit stuffing is done after every two ‘11’(as the flag is 0111) to differentiate the data part from the flag- there must not be “111 ” in the data so after every 11 a ‘0’ is added. The receiver also knows this and so, it decodes every “110 ” as “11 ”. Therefore, option **D is the answer.**

- http://web.nchu.edu.tw/~pcwang/computer_networks/data_link_layer.pdf
- https://en.wikipedia.org/wiki/High-Level_Data_Link_Control

References

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👉 44 votes

-- Gate Keeda (15.9k points)

2.17.4 Network Flow: GATE IT 2004 | Question: 87<https://gateoverflow.in/3731>

- ✓ At source : TCP passes 2100B to IP layer. IP appends 20B header and sends it to DLL and so on. (We are interested in IP overhead, So lets consider DLL header to be negligible)

A router on the way has highest layer as Network Layer, So, complete TCP segment is fragmented. And in question 1200 and 400 are given as **maximum payload without network overhead**, means we are directly given the amount of data part of IP datagram a Frame can hold. [1200 doesn't contain IP header]

Router-1: 2120B reach R'_1 's network layer. It removes original IP header, fragments data part at IP and then appends IP header to all fragments and forwards. So, it divides 2100 Bytes into two fragments of size 1200 and 900. And Both fragments are sent to R_2 .

Router-2: Both fragments that reach R_2 exceed MTU at R_2 . So, both are fragmented. First packet of 1200B is fragmented into 3 packets of 400, 400 and 400 Bytes respectively and Second packet of 900B is fragmented into three fragments of 400, 400 and 100 Bytes respectively.

Original data during fragmentation should not change. Only additional IP headers are added. So totally 6 *packets* reach destination. And IP header is also an overhead because our main aim is to send data only.

$$\text{Total IP Overhead} = 6 * 20 = 120 \text{ B}$$

Hence, (C) is correct answer.

<http://quiz.geeksforgeeks.org/gate-gate-it-2004-question-87/>

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References



44 votes

-- Manish Joshi (20.5k points)

2.17.5 Network Flow: GATE IT 2006 | Question: 67

<https://gateoverflow.in/3611>



- Since there is no buffer and constraint given is there should not be any data lost, and no wastage of capacity as well.

Since data should not be lost, we calculate for the extreme case when all sources are on (that is transmitting).

$$10 \text{ Mbps} \times n\text{-station} \leq 100 \text{ Mbps}$$

[n-station](#)

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In the next part of the question it is given that the link is provided with large buffer and we are asked to find out the maximum number of stations.

For this we'll calculate the expected value of bandwidth usage (if more data comes we store in buffer and due to expectation, the buffer will be emptied soon or in other words buffer space will never run out):

$$E = \frac{1}{3} \times 10 + \frac{1}{3} \times 10 + \dots n\text{-station times} \leq 100 \text{ Mbps}$$

[total time is $(1+2)=3$ then on time is 1 so $\frac{1}{3}$ of BW]

$$\Rightarrow \frac{1}{3} \times 10 \times n\text{-station} \leq 100 \text{ Mbps}$$

$$\Rightarrow n\text{-station} = 30$$

So, option (A) is answer.

49 votes

-- Vicky Bajoria (4.1k points)

2.18

Network Layering (6)

<https://gateoverflow.in/918>



2.18.1 Network Layering: GATE CSE 2003 | Question: 28

<https://gateoverflow.in/918>

Which of the following functionality *must* be implemented by a transport protocol over and above the network protocol?

- A. Recovery from packet losses
- B. Detection of duplicate packets
- C. Packet delivery in the correct order
- D. End to end connectivity

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Answer

2.18.2 Network Layering: GATE CSE 2004 | Question: 15

<https://gateoverflow.in/1012>



Choose the best matching between Group 1 and Group 2

Group-1	Group-2
P. Data link layer	1. Ensures reliable transport of data over a physical point-to-point link
Q. Network layer	2. Encodes/decodes data for physical transmission
R. Transport layer	3. Allows end-to-end communication between two processes
	4. Routes data from one network node to the next

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- A. P-1, Q-4, R-3
 B. P-2, Q-4, R-1
 C. P-2, Q-3, R-1
 D. P-1, Q-3, R-2

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Answer **2.18.3 Network Layering: GATE CSE 2007 | Question: 70** <https://gateoverflow.in/1268>

Match the following:

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- | | | | |
|-----|------|-----|-------------------|
| (P) | SMTP | (1) | Application layer |
| (Q) | BGP | (2) | Transport layer |
| (R) | TCP | (3) | Data link layer |
| (S) | PPP | (4) | Network layer |
| | | (5) | Physical layer |

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- A. P - 2, Q - 1, R - 3, S - 5
 B. P - 1, Q - 4, R - 2, S - 3
 C. P - 1, Q - 4, R - 2, S - 5
 D. P - 2, Q - 4, R - 1, S - 3

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Answer **2.18.4 Network Layering: GATE CSE 2013 | Question: 14** <https://gateoverflow.in/1436>

Assume that source S and destination D are connected through two intermediate routers labeled R. Determine how many times each packet has to visit the network layer and the data link layer during a transmission from S to D.

- A. Network layer – 4 times and Data link layer – 4 times
 B. Network layer – 4 times and Data link layer – 3 times
 C. Network layer – 4 times and Data link layer – 6 times
 D. Network layer – 2 times and Data link layer – 6 times

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Answer **2.18.5 Network Layering: GATE CSE 2014 Set 3 | Question: 23** <https://gateoverflow.in/2057>In the following pairs of OSI protocol layer/sub-layer and its functionality, the **INCORRECT** pair is

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- A. Network layer and Routing
 B. Data Link Layer and Bit synchronization
 C. Transport layer and End-to-end process communication
 D. Medium Access Control sub-layer and Channel sharing

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Answer 



Match the following:

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Field	Length in bits
P. UDP Header's Port Number	I. 48
Q. Ethernet MAC Address	II. 8
R. IPv6 Next Header	III. 32
S. TCP Header's Sequence Number	IV. 16

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- A. P-III, Q-IV, R-II, S-I
- B. P-II, Q-I, R-IV, S-III
- C. P-IV, Q-I, R-II, S-III
- D. P-IV, Q-I, R-III, S-II

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Answer

Answers: Network Layering



- ✓ **Answer(D)** TCP and UDP are transport layer protocols.

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Question is asking which service must be provided by transport layer so that source can successfully communicate to destination. UDP is a connection-less protocol but it's a transport layer protocol so that from here we can say that reliability is not a service that MUST be provided by transport layer protocols. with that same argument cut all those options in which such a service is mentioned which UDP doesn't provide so only (D) remain so it's the answer..

other way to answer is ' for Process to Process delivery transport layer service is MUST otherwise there is no way to deliver the data to right process'.. if reliability is in danger data can survive (Data link layer also take care about errors so we can compromise error recovery at transport layer), if there are duplicate packets , yet data can survive ,only bandwidth is wasted, if packets are delivered out of order data can survive but if data of process A is delivered to process B , data can't survive.... "to Assigning port numbers" Transport layer service is MUST...

64 votes

-- Rupendra Choudhary (11.4k points)



- ✓ Answer is A.

21 votes

-- Aditi Dan (4k points)



- ✓ Answer is B.

- [SMTP](#) is an application layer protocol used for e-mail transmission.
- [TCP](#) is a core transport layer protocol.
- [BGP](#) is a network layer protocol backing the core routing decisions on the Internet.
- [PPP](#) is a data link layer protocol commonly used in establishing a direct connection between two networking.

References



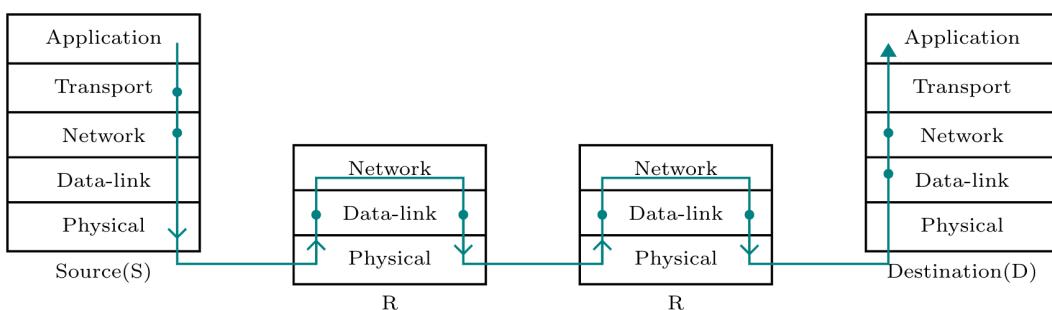
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33 votes

-- naga praveen (2.8k points)



C is the Answer.

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68 votes

-- Mithlesh Upadhyay (4.3k points)



- A. One of the main functionality of Network Layer is Routing. So, option (A) is CORRECT.
- B. Bit Synchronization is always handled by Physical Layer of OSI model but not Data Link Layer. So, option (B) is INCORRECT.
- C. End – to – End Process Communication is handled by Transport Layer. So, option (C) is CORRECT.
- D. MAC sub layer have 3 types of protocols (Random, Controlled and Channelized Access).

So, option (B) is incorrect pair.

33 votes

-- Çse çate (1.7k points)



✓ UDP header - 16 bits

MAC address: 48 bits

IPv6 next header: 8 bits

TCP Sequence No.: 32 bits

Answer: (C) P:IV, Q:I, R:II, S:III

29 votes

-- Prateek Kumar (1.1k points)



The address resolution protocol (ARP) is used for:

- A. Finding the IP address from the DNS
- B. Finding the IP address of the default gateway
- C. Finding the IP address that corresponds to a MAC address
- D. Finding the MAC address that corresponds to an IP address

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Answer



Which one of the following uses UDP as the transport protocol?

- A. HTTP

- B. Telnet
C. DNS
D. SMTP

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Answer 

2.19.3 Network Protocols: GATE CSE 2015 Set 1 | Question: 17 top ↺

◀ <https://gateoverflow.in/8214>



In one of the pairs of protocols given below , both the protocols can use multiple TCP connections between the same client and the server. Which one is that?

- A. HTTP, FTP
B. HTTP, TELNET
C. FTP, SMTP
D. HTTP, SMTP

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Answer 

2.19.4 Network Protocols: GATE CSE 2016 Set 1 | Question: 24 top ↺

◀ <https://gateoverflow.in/39639>



Which one of the following protocols is NOT used to resolve one form of address to another one?

- A. DNS
B. ARP
C. DHCP
D. RARP

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Answer 

2.19.5 Network Protocols: GATE CSE 2019 | Question: 29 top ↺

◀ <https://gateoverflow.in/302819>



Suppose that in an IP-over-Ethernet network, a machine X wishes to find the MAC address of another machine Y in its subnet. Which one of the following techniques can be used for this?

- A. X sends an ARP request packet to the local gateway's IP address which then finds the MAC address of Y and sends to X
B. X sends an ARP request packet to the local gateway's MAC address which then finds the MAC address of Y and sends to X
C. X sends an ARP request packet with broadcast MAC address in its local subnet
D. X sends an ARP request packet with broadcast IP address in its local subnet

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Answer 

2.19.6 Network Protocols: GATE CSE 2021 Set 1 | Question: 49 top ↺

◀ <https://gateoverflow.in/357402>



Consider the sliding window flow-control protocol operating between a sender and a receiver over a full-duplex error-free link. Assume the following:

- The time taken for processing the data frame by the receiver is negligible.
- The time taken for processing the acknowledgement frame by the sender is negligible.
- The sender has infinite number of frames available for transmission.
- The size of the data frame is 2,000 bits and the size of the acknowledgement frame is 10 bits.
- The link data rate in each direction is 1 Mbps ($= 10^6$ bits per second).
- One way propagation delay of the link is 100 milliseconds.

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The minimum value of the sender's window size in terms of the number of frames, (rounded to the nearest integer) needed to achieve a link utilization of 50% is _____.

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Answer 

2.19.7 Network Protocols: GATE CSE 2021 Set 1 | Question: 8 [top](#) 

<https://gateoverflow.in/357444>



Consider the following two statements.

- S_1 : Destination MAC address of an ARP reply is a broadcast address.
- S_2 : Destination MAC address of an ARP request is a broadcast address.

Which one of the following choices is correct?

- A. Both S_1 and S_2 are true
B. S_1 is true and S_2 is false
C. S_1 is false and S_2 is true
D. Both S_1 and S_2 are false

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[gate2021-cse-set1](#) [computer-networks](#) [network-protocols](#)

Answer 

2.19.8 Network Protocols: GATE IT 2007 | Question: 69 [top](#) 

<https://gateoverflow.in/3514>



Consider the following clauses:

- Not inherently suitable for client authentication.
- Not a state sensitive protocol.
- Must be operated with more than one server.
- Suitable for structured message organization.
- May need two ports on the serve side for proper operation.

The option that has the maximum number of correct matches is [classes.in](#)

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- A. IMAP-i; FTP-ii; HTTP-iii; DNS-iv; POP3-v
B. FTP-i; POP3-ii; SMTP-iii; HTTP-iv; IMAP-v
C. POP3-i; SMTP-ii; DNS-iii; IMAP-iv; HTTP-v
D. SMTP-i; HTTP-ii; IMAP-iii; DNS-iv; FTP-v

[gate2007-it](#) [computer-networks](#) [network-protocols](#) [normal](#)

Answer 

2.19.9 Network Protocols: GATE IT 2008 | Question: 68 [top](#) 

<https://gateoverflow.in/3382>



Which of the following statements are TRUE?

- **S1:** TCP handles both congestion and flow control
- **S2:** UDP handles congestion but not flow control
- **S3:** Fast retransmit deals with congestion but not flow control
- **S4:** Slow start mechanism deals with both congestion and flow control

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- A. S_1 , S_2 and S_3 only
B. S_1 and S_3 only
C. S_3 and S_4 only
D. S_1 , S_3 and S_4 only

[gate2008-it](#) [computer-networks](#) [network-protocols](#) [normal](#)

Answer 

Answers: Network Protocols

2.19.1 Network Protocols: GATE CSE 2005 | Question: 24 [top](#) 

<https://gateoverflow.in/1360>



- ✓ The address resolution protocol (**ARP**) is a protocol used by the Internet Protocol (IP) specifically IPv4, to map IP network addresses to the hardware addresses used by a data link protocol.

Show that option D is correct.

Ref: <http://www.erg.abdn.ac.uk/users/gorry/course/inet-pages/arp.html>

References



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16 votes

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-- Brij Mohan Gupta (1.7k points)

2.19.2 Network Protocols: GATE CSE 2007 | Question: 20 [top](#)

<https://gateoverflow.in/1218>



- ✓ The answer is C.

Where quick response is needed, there UDP is preferred.

33 votes

-- Gate Keeda (15.9k points)

2.19.3 Network Protocols: GATE CSE 2015 Set 1 | Question: 17 [top](#)

<https://gateoverflow.in/8214>



- ✓ **SMTP:** only one TCP connection.

Reference: <https://tools.ietf.org/html/rfc821>

TELNET: only one TCP connection.

Reference: <https://tools.ietf.org/html/rfc854>

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HTTP: Multiple connections can be used for each resource.

Reference: <http://www.w3.org/Protocols/rfc2616/rfc2616-sec1.html#sec1>

FTP: FTP uses Telnet protocol for Control info on a TCP connection and another TCP connection for data exchange

Reference: <https://tools.ietf.org/html/rfc959> (See page 8)

So, answer is A.

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61 votes

-- Arjun Suresh (332k points)

2.19.4 Network Protocols: GATE CSE 2016 Set 1 | Question: 24 [top](#)

<https://gateoverflow.in/39639>



- ✓ A) DNS - host name to IP address
- B) ARP - IP to MAC
- C) RARP - MAC to IP

So ANSWER is C

34 votes

-- Abhilash Panicker (7.6k points)

2.19.5 Network Protocols: GATE CSE 2019 | Question: 29 [top](#)

<https://gateoverflow.in/302819>



- ✓ Steps in ARP Operation :

1. The sender (X) knows its own IP address and MAC address. X also knows the IP address of the target (Y). It needs to find MAC address of Y

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2. IP asks ARP to create an ARP request message, filling in X's IP and MAC address and Y's IP address. **The destination MAC address is set to all 0s.**
3. The message is passed to Data Link layer where it is encapsulated in a frame using MAC address of X as the source address and **physical broadcast address (all 1s)** as the destination address.
4. Every host in subnet receives the request message because we have used broadcast MAC address in the destination address. All machines except Y (we have specified Y's IP address in our ARP request message) drop the ARP request message.
5. Y replies with an ARP reply message that contains its MAC address.
6. When X receives this message, it gets to know the MAC address of Y.

Please note that, a host uses its own IP address and network mask to decide if target IP address is in its own network or not.

If it is in its network, it uses ARP to resolve the MAC address.

If target IP address is not in its network, it takes the help of default gateway to resolve MAC address using ARP.

Since in question it is clearly mentioned that X (source) and Y (destination) both are in the same subnet, we need not send ARP request message targeted at gateway and then expect it to give the MAC address of Y to X.

So the correct answer is option C.

56 votes

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-- NabilSayyad (761 points)

2.19.6 Network Protocols: GATE CSE 2021 Set 1 | Question: 49 [top](#)

<https://gateoverflow.in/357402>



- ✓ Let the sender window size be N .

One way propagation delay = $100 \text{ ms} = 0.1 \text{ s}$

$$\text{Transmission delay}_{\text{packet}} = \frac{\text{Size of data frame}}{\text{Link bit rate}} = \frac{2000}{10^6} = 0.002 \text{ s}$$

$$\text{Transmission delay}_{\text{ACK}} = \frac{\text{Size of ACK frame}}{\text{Link bit rate}} = \frac{10}{10^6} = 0.00001 \text{ s}$$

$$\text{Link Utilization}(\eta) = \frac{\text{Useful Data Transfer time}}{\text{Total time}}$$

$$\Rightarrow \eta = \frac{N \cdot (T_f)}{T_f + 2(T_p) + T_{ACK}}$$

$$\Rightarrow N = \left\lceil \frac{\eta \cdot (T_f + 2(T_p) + T_{ACK})}{T_f} \right\rceil = \left\lceil \frac{0.5(0.002 + 0.2 + 0.00001)}{0.002} \right\rceil = \lceil 50.5025 \rceil = 51$$

Correct Answer: 51

4 votes

-- Konan-kun (191 points)

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2.19.7 Network Protocols: GATE CSE 2021 Set 1 | Question: 8 [top](#)

<https://gateoverflow.in/357444>



- ✓ In ARP, source broadcasts an ARP request to all devices in local subnet.

The destination which has the matching IP address then sends an ARP response which includes the MAC address of the source and hence is a unicast message.

Option (C) S1 is false and S2 is true

2 votes

-- Ashwani Kumar (13k points)

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2.19.8 Network Protocols: GATE IT 2007 | Question: 69 [top](#)

<https://gateoverflow.in/3514>



- ✓ They are asking for maximum correct matches so

- i. Should be HTTP thus we use HTTPS.
- ii. HTTP as it does not depend on state of device or operating system.
- iii. IMAP or DNS*Not sure but they may involve multiple servers.
- iv. POP3 is suitable for structuring or arranging the folders.
- v. FTP needs two ports, 20 for data and 21 for control.

Thus, **Option D**, As it's matching with HTTP-2,IMAP-3,FTP-5 .

26 votes

-- Shashank Chavan (2.4k points)

2.19.9 Network Protocols: GATE IT 2008 | Question: 68 [top](#)

<https://gateoverflow.in/3382>



- ✓ (S1) TCP handles both congestion and flow control \Rightarrow True.
It uses congestion window for congestion control & Advertisement window for flow control
(S2) UDP handles congestion but not flow control \Rightarrow UDP does not handle congestion but also not handle flow control.
(S3) Fast retransmit deals with congestion but not flow control \Rightarrow Yes.
Fast Retransmit is technique for detecting out of Order Datagram & Sending it.
It is congestion control technique and has no relation with Flow control
(S4) Slow start mechanism deals with both congestion and flow control \Rightarrow False.
It has nothing to do with Flow control. Flow control is taken care by Advertisement window.
Slow start is way Sender tries to gauge network capacity !

Answer (B) S1 and S3 only.

68 votes

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-- Akash Kanase (36k points)

2.20

Network Switching (4) [top](#)

2.20.1 Network Switching: GATE CSE 2005 | Question: 73 [top](#)

<https://gateoverflow.in/1396>



In a packet switching network, packets are routed from source to destination along a single path having two intermediate nodes. If the message size is 24 bytes and each packet contains a header of 3 bytes, then the optimum packet size is: <tests.gatecse.in>

- A. 4
- B. 6
- C. 7
- D. 9

gate2005-cse computer-networks network-switching normal

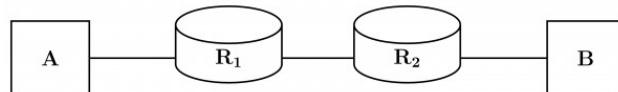
Answer

2.20.2 Network Switching: GATE CSE 2014 Set 2 | Question: 26 [top](#)

<https://gateoverflow.in/1985>



Consider the store and forward packet switched network given below. Assume that the bandwidth of each link is 10^6 bytes / sec. A user on host A sends a file of size 10^3 bytes to host B through routers R1 and R2 in three different ways. In the first case a single packet containing the complete file is transmitted from A to B. In the second case, the file is split into 10 equal parts, and these packets are transmitted from A to B. In the third case, the file is split into 20 equal parts and these packets are sent from A to B. Each packet contains 100 bytes of header information along with the user data. Consider only transmission time and ignore processing, queuing and propagation delays. Also assume that there are no errors during transmission. Let T1, T2 and T3 be the times taken to transmit the file in the first, second and third case respectively. Which one of the following is CORRECT? <tests.gatecse.in>



- A. $T_1 < T_2 < T_3$
- B. $T_1 > T_2 > T_3$
- C. $T_2 = T_3, T_3 < T_1$
- D. $T_1 = T_3, T_3 > T_2$

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gate2014-cse-set2 computer-networks network-switching normal

Answer

2.20.3 Network Switching: GATE CSE 2015 Set 3 | Question: 36 [top](#)

<https://gateoverflow.in/8495>



Two hosts are connected via a packet switch with 10^7 bits per second links. Each link has a propagation delay of 20 microseconds. The switch begins forwarding a packet 35 microseconds after it receives the same. If 10000 bits of data are to be transmitted between the two hosts using a packet size of 5000 bits, the time elapsed between the transmission of the first bit of data and the reception of the last bit of the data in microseconds is _____.

Answer **2.20.4 Network Switching: GATE IT 2004 | Question: 22** <https://gateoverflow.in/3663>

Which one of the following statements is FALSE?

- A. Packet switching leads to better utilization of bandwidth resources than circuit switching
- B. Packet switching results in less variation in delay than circuit switching
- C. Packet switching requires more per-packet processing than circuit switching
- D. Packet switching can lead to reordering unlike in circuit switching

Answer **Answers: Network Switching****2.20.1 Network Switching: GATE CSE 2005 | Question: 73** <https://gateoverflow.in/1396>✓ **Correct answer should be option D.**

As we know in packet switching- dividing message into packets decrease the transmission time due to pipelined transmission.

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but if there are many packets beyond some threshold then transmission time may increase. So, we can do by option checking

1. packet size = 4 = packet data + header size = 1 + 3

$$\text{So no. of packets will be} = \frac{\text{message}}{\text{packet data}}$$

$$= \frac{24}{1} = 24 \text{ packets.}$$

So, time to reach at receiver for 1st packet will be,

$$= 3 (\text{source} + \text{two intermediate node}) \times \text{transmission time}$$

$$TT = \frac{L}{BW} \dots \text{Here, } L \text{ will be changed according to option and } BW \text{ will remain same ..}$$

$$\text{So time to reach at receiver for 1st packet will be} = \frac{3 \times 4}{BW} = \frac{12}{BW}$$

$$\text{and for remaining 23 packets will take time} = 23 \times TT = \frac{23 \times 4}{BW} = \frac{92}{BW}$$

$$\text{TOTAL TIME} = \frac{104}{BW}$$

2. packet size = 6 = 3 + 3 (packet data + header size) so no of packets will be 8.

$$\text{Time to reach at receiver for 1st packet will be} = \frac{3 \times 6}{BW} = \frac{18}{BW}$$

$$\text{and for remaining 7 packet will take time} = \frac{7 \times 6}{BW} = \frac{42}{BW}$$

$$\text{Total time} = \frac{60}{BW}$$

$$\text{3. packet size} = 7 = 4 + 3, \text{ so no of packets} = \frac{24}{4} = 6 \text{ packets}$$

$$\text{For 1st packet time will be} = \frac{3 \times 7}{BW} = \frac{21}{BW}$$

$$\text{For remaining 5 packet will take time} = \frac{5 \times 7}{BW} = \frac{35}{BW}$$

$$\text{Total time} = \frac{56}{BW}.$$

4. packet size = 9 = 6 + 3, so no of packet will be 4.

For 1st packet time will be = $\frac{3 \times 9}{BW} = \frac{27}{BW}$

For remaining 3 packets will take time = $\frac{3 \times 9}{BW} = \frac{27}{BW}$

TOTAL time = $\frac{54}{BW}$

So, optimal packet size will be 9 byte due to less total transmission time.

Alternate method (thanks to sachin)

In that case we can do it using minimisation of a variable.

Let, 24 byte data is divided into number of packets each have x bytes of data.

Therefore, packet size = $x + 3$, and Number of packets (k) = $\frac{24}{x}$.

(it is ceil, if 24 is not multiple of x)

Total time = $3(x + 3) + (k - 1)(x + 3)$ (assumed $BW = 1$, just to avoid writing 'BW' again and again)

(ignoring propagation delay as it has nothing to do with packet size, if one wish he/she can add that too but later he will realize it will anyway become zero while differentiating.)

\Rightarrow Total time = $2x + 3k + kx + 6$ (k is equal to $24/x$)

\Rightarrow Total time = $2x + \left(\frac{3 \times 24}{x}\right) + \left(\frac{24 * x}{x}\right) + 6$

\Rightarrow Total time = $2x + \frac{72}{x} + 30$

to minimise this time, differentiation should give 0.

that gives, $2 - \frac{72}{x^2} = 0$

$\Rightarrow x = 6$.

including 3 bytes of header, packet size = 9 Bytes.

Option is D.

103 votes

-- minal (13.1k points)

option D

packet size $P = p + h$. where, h is header size and

$p = \sqrt{\frac{hx}{k-1}}$ where, x is message size and k is no. of hops.

so $p = \sqrt{\frac{3 \times 24}{2}} = \sqrt{\frac{72}{2}} = \sqrt{36} = 6$

so Optimum packet size is $6 + 3 = 9$.

31 votes

-- skrahul (655 points)

2.20.2 Network Switching: GATE CSE 2014 Set 2 | Question: 26

<https://gateoverflow.in/1985>



- ✓ In this question we have used the concept of pipelining.

In second and Third case, First packet will take $3 \times T_t$ time and all subsequent packets will be delivered in one T_t time.

$$T_1 = 3 \times T_t = 3 \times \frac{(1000 + 100)}{B}$$

$$T_t = \frac{(\text{data} + \text{header})}{\text{Bandwidth}}$$

data = 1000 Bytes; header = 100 Bytes

$$T_1 = \frac{3300}{B} \text{ seconds}$$

$$T_2 = 3 \times T_t' + 9 \times T_t' = 12 \times T_t'$$

$$T_t' = \frac{(\text{data} + \text{header})}{\text{Bandwidth}}$$

$$T_2 = \frac{12 \times (100 + 100)}{B} = \frac{2400}{B} \text{ seconds}$$

$$T_3 = 3 \times T_t'' + 19 \times T_t'' = 22 \times T_t''$$

$$T_t'' = \frac{(50 + 100)}{B}$$

$$T_3 = \frac{22 \times 150}{B} = \frac{3300}{B}$$

So $T_1 = T_3$ and $T_3 > T_2$;

option D

92 votes

-- Vikrant Singh (11.2k points)

2.20.3 Network Switching: GATE CSE 2015 Set 3 | Question: 36 top

→ <https://gateoverflow.in/8495>



$$\text{No. of packets sent} = \frac{10000}{5000} = 2.$$

Time for the first packet to reach switch = Transmission time + Propagation delay

$$= \left(\frac{5000}{10^7} \right) \times 10^6 \mu s + 20 \mu s$$

$$= 520 \mu s$$

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(Another $520 \mu s$ is required for the same packet to reach the destination from the switch and in between there is a forwarding delay of $35 \mu s$. So, first packet is received at destination at $2 \times 520 + 35 = 1075 \mu s$.)

After $520 \mu s$, the switch can start receiving the second packet and at $520 + 500 = 1020 \mu s$, second frame is completely received by the switch (we don't need to add propagation time here as packet 2 can just follow packet 1).

So, at $1055 \mu s$ from the start the switch starts sending the second packet and this will be received at destination after another $520 \mu s = 1575 \mu s$. Since we added transmission time, this ensures that the last bit of data is received at the sender.

EDIT:-

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(Alternate solution)

We can think the same question in terms of last packet, argument here is: The moment last packet reaches to destination, all other packets are already reached.

Total time = Transmission time of all packets + Propagation time for first link
+ Switch Delay + Transmission time of last packet for Switch
+ propagation time for 2nd link.

$$= \left(\frac{10^4}{10^7} \text{ sec} = 1 \text{ ms} = 1000 \mu s \right) 1000 + 20 + 35 + 500 + 20 = 1575 \mu s.$$

90 votes

-- Arjun Suresh (332k points)

2.20.4 Network Switching: GATE IT 2004 | Question: 22 top

→ <https://gateoverflow.in/3663>



Answer is B.

In circuit switching, a fix bandwidth is allocated to each connection, e.g. 64 Kb/s allocated to each each phone call.

In circuit switching each connection has a dedicated circuit or channel all the way along the path and the circuit is not shared with anyone else.

Thus in circuit switching each call has its own private, guaranteed, isolated data rate from end to end. So we can say that every connection or flow is independent of others.

In the case of packet switching, all flows share the full channel capacity by statistical multiplexing.

So, the bandwidth allocated to each flow depends upon the number of concurrent flows & network traffic.

In packet switching if we know the type of link we are using, the bandwidth allocated, the packet size for any flow then we can calculate the Propagation Delay & Transmission Delays.

But, **Queueing Delay is a random variable that depends upon the number of packets arriving at the same time at any switch.**

It is the only random variable in our end to end delay expression. All other delays can be calculated precisely if we have enough information about the flows.

So, queueing adds unpredictable & variable delays in the packet switching.

There are delays like propagation delay etc. in circuit switching but they have a very small variance because of independence, privacy & bandwidth guarantees.

49 votes

-- Anurag Pandey (10.5k points)

2.21

Pure Aloha (1) [top](#)

2.21.1 Pure Aloha: GATE CSE 2021 Set 2 | Question: 54 [top](#)

<https://gateoverflow.in/357483>



Consider a network using the pure ALOHA medium access control protocol, where each frame is of length 1,000 bits. The channel transmission rate is 1 Mbps ($= 10^6$ bits per second). The aggregate number of transmissions across all the nodes (including new frame transmissions and retransmitted frames due to collisions) is modelled as a Poisson process with a rate of 1,000 frames per second. Throughput is defined as the average number of frames successfully transmitted per second. The throughput of the network (rounded to the nearest integer) is _____

[gate2021-cse-set2](#) [computer-networks](#) [mac-protocol](#) [pure-aloha](#) [numerical-answers](#)

Answer

Answers: Pure Aloha

2.21.1 Pure Aloha: GATE CSE 2021 Set 2 | Question: 54 [top](#)

<https://gateoverflow.in/357483>



- ✓ Frame Transmission Time : $T_{fr} = L/B = 1000/10^6 = 1\text{ms}$

System generates 1000 frames in 1 second.

Now, G is defined as average no of frames generated by the system in one frame transmission time.

- 1 second \rightarrow 1000 frames
- $\therefore 1\text{ms} \rightarrow 1 \text{frame}$

Therefore, $G = 1$

Average number of successful transmissions, $S = G * e^{-2G} = 1 * e^{-2} = 0.13534$

Throughput is defined in question as the average number of frames successfully transmitted per second.

$\therefore \text{Throughput} = 0.13534 * 1000 = 135.34 \approx 135.$

3 votes

-- sjoshis07 (169 points)

2.22

Routers Bridge Hubs Switches (1) [top](#)

2.22.1 Routers Bridge Hubs Switches: GATE CSE 2004 | Question: 16 [top](#)

<https://gateoverflow.in/1013>



Which of the following is NOT true with respect to a transparent bridge and a router?

- A. Both bridge and router selectively forward data packets
- B. A bridge uses IP addresses while a router uses MAC addresses
- C. A bridge builds up its routing table by inspecting incoming packets
- D. A router can connect between a LAN and a WAN

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Answer ↗

Answers: Routers Bridge Hubs Switches

2.22.1 Routers Bridge Hubs Switches: GATE CSE 2004 | Question: 16 top ↗

↗ <https://gateoverflow.in/1013>



- ✓ A. Both bridge and router selectively forward data packets ⇒ **True.**
Bridge can drop packets not meant for other side, so can router.
- B. A bridge uses IP addresses while a router uses MAC addresses ⇒ **False .**
A bridge operate at layer 2 (data link layer) so it uses MAC address, while router at layer 3 (network layer) so it using IP address
- C. A bridge builds up its routing table by inspecting incoming packets ⇒ **True.**
Self Learning Bridges
- D. A router can connect between a LAN and a WAN ⇒ **True.**
Router connecting home LAN To internet !

Correct Answer: **B**

42 votes

-- Akash Kanase (36k points)

2.23

Routing (9) top ↗

2.23.1 Routing: GATE CSE 2005 | Question: 26 top ↗

↗ <https://gateoverflow.in/1362>



In a network of LANs connected by bridges, packets are sent from one LAN to another through intermediate bridges. Since more than one path may exist between two LANs, packets may have to be routed through multiple bridges. Why is the *spanning tree algorithm* used for bridge-routing?

- A. For shortest path routing between LANs
- B. For avoiding loops in the routing paths
- C. For fault tolerance
- D. For minimizing collisions

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Answer ↗

2.23.2 Routing: GATE CSE 2014 Set 2 | Question: 23 top ↗

↗ <https://gateoverflow.in/1981>



Which of the following is TRUE about the interior gateway routing protocols – Routing Information Protocol (*RIP*) and Open Shortest Path First (*OSPF*)

- A. RIP uses distance vector routing and OSPF uses link state routing
- B. OSPF uses distance vector routing and RIP uses link state routing
- C. Both RIP and OSPF use link state routing
- D. Both RIP and OSPF use distance vector routing

gate2014-cse-set2 computer-networks routing normal

Answer ↗

2.23.3 Routing: GATE CSE 2014 Set 3 | Question: 26 top ↗

↗ <https://gateoverflow.in/2060>



An IP router implementing Classless Inter-domain Routing (CIDR) receives a packet with address 131.23.151.76. The router's routing table has the following entries:

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Prefix	Outer Interface Identifier
131.16.0.0/12	3
131.28.0.0/14	5
131.19.0.0/16	2
131.22.0.0/15	1

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The identifier of the output interface on which this packet will be forwarded is _____.

[gate2014-cse-set3](#) [computer-networks](#) [routing](#) [normal](#) [numerical-answers](#)
[Answer](#)

2.23.4 Routing: GATE CSE 2017 Set 2 | Question: 09 [top](#)

<https://gateoverflow.in/118338>


Consider the following statements about the routing protocols. Routing Information Protocol (RIP) and Open Shortest Path First (OSPF) in an IPv4 network.

- I. RIP uses distance vector routing
- II. RIP packets are sent using UDP
- III. OSPF packets are sent using TCP
- IV. OSPF operation is based on link-state routing

Which of the above statements are CORRECT?

- A. I and IV only
- B. I, II and III only
- C. I, II and IV only
- D. II, III and IV only

[gate2017-cse-set2](#) [computer-networks](#) [routing](#)
[Answer](#)

2.23.5 Routing: GATE CSE 2020 | Question: 15 [top](#)

<https://gateoverflow.in/333216>


Consider the following statements about the functionality of an IP based router.

- I. A router does not modify the IP packets during forwarding.
- II. It is not necessary for a router to implement any routing protocol.
- III. A router should reassemble IP fragments if the MTU of the outgoing link is larger than the size of the incoming IP packet.

Which of the above statements is/are TRUE?

- A. I and II only
- B. I only
- C. II and III only
- D. II only

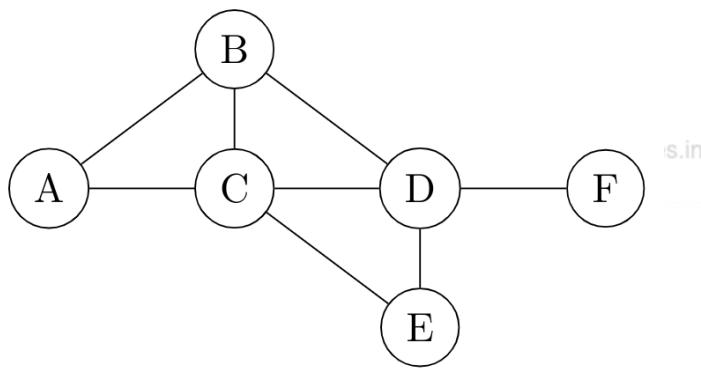
[gate2020-cse](#) [computer-networks](#) [routing](#)
[Answer](#)

2.23.6 Routing: GATE IT 2005 | Question: 85a [top](#)

<https://gateoverflow.in/3858>


Consider a simple graph with unit edge costs. Each node in the graph represents a router. Each node maintains a routing table indicating the next hop router to be used to relay a packet to its destination and the cost of the path to the destination through that router. Initially, the routing table is empty. The routing table is synchronously updated as follows. In each updated interval, three tasks are performed.

- i. A node determines whether its neighbours in the graph are accessible. If so, it sets the tentative cost to each accessible neighbour as 1. Otherwise, the cost is set to ∞ .
- ii. From each accessible neighbour, it gets the costs to relay to other nodes via that neighbour (as the next hop).
- iii. Each node updates its routing table based on the information received in the previous two steps by choosing the minimum cost.



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For the graph given above, possible routing tables for various nodes after they have stabilized, are shown in the following options. Identify the correct table.

Table for node A

A	-	-
B	B	1
C	C	1
D	B	3
E	C	3
F	C	4

A.

Table for node C

A	A	1
B	B	1
C	-	-
D	D	1
E	E	1
F	E	3

B.

Table for node B

A	A	1
B	-	-
C	C	1
D	D	1
E	C	2
F	D	2

C.

Table for node D

A	B	3
B	B	1
C	C	1
D	-	-
E	E	1
F	F	1

D.

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Answer ↗

2.23.7 Routing: GATE IT 2005 | Question: 85b top ↗

↗ <https://gateoverflow.in/3859>



Consider a simple graph with unit edge costs. Each node in the graph represents a router. Each node maintains a routing table indicating the next hop router to be used to relay a packet to its destination and the cost of the path to the destination through that router. Initially, the routing table is empty. The routing table is synchronously updated as follows. In each updated interval, three tasks are performed.

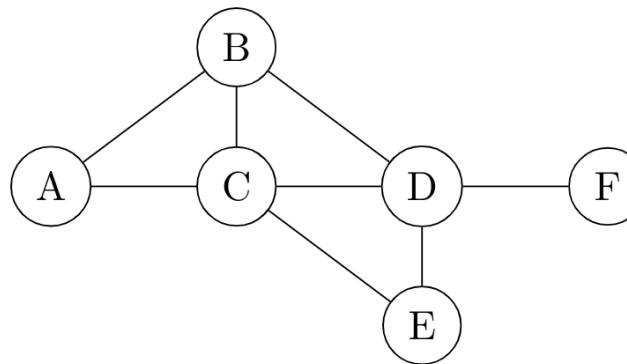
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- A node determines whether its neighbors in the graph are accessible. If so, it sets the tentative cost to each accessible neighbor as 1. Otherwise, the cost is set to ∞ .
- From each accessible neighbor, it gets the costs to relay to other nodes via that neighbor (as the next hop).
- Each node updates its routing table based on the information received in the previous two steps by choosing the minimum

cost.



Continuing from the earlier problem, suppose at some time t , when the costs have stabilized, node A goes down. The cost from node F to node A at time $(t + 100)$ is :

- A. > 100 but finite
- B. ∞
- C. 3
- D. > 3 and ≤ 100

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Answer ↗

2.23.8 Routing: GATE IT 2007 | Question: 63 top ↵

↗ <https://gateoverflow.in/3508>



A group of 15 routers is interconnected in a centralized complete binary tree with a router at each tree node. Router i communicates with router j by sending a message to the root of the tree. The root then sends the message back down to router j . The mean number of hops per message, assuming all possible router pairs are equally likely is

- A. 3
- B. 4.26
- C. 4.53
- D. 5.26

gate2007-it computer-networks routing binary-tree normal

Answer ↗

2.23.9 Routing: GATE IT 2008 | Question: 67 top ↵

↗ <https://gateoverflow.in/3381>



Two popular routing algorithms are Distance Vector(DV) and Link State (LS) routing. Which of the following are true?

- (S1): Count to infinity is a problem only with DV and not LS routing
- (S2): In LS, the shortest path algorithm is run only at one node
- (S3): In DV, the shortest path algorithm is run only at one node
- (S4): DV requires lesser number of network messages than LS

- A. S1, S2 and S4 only
- B. S1, S3 and S4 only
- C. S2 and S3 only
- D. S1 and S4 only

gate2008-it computer-networks routing normal

Answer ↗

Answers: Routing

2.23.1 Routing: GATE CSE 2005 | Question: 26 top ↵

↗ <https://gateoverflow.in/1362>



- ✓ The answer is (B).

Since, in a spanning tree, there is a unique path from a source to the destination, which avoids loops, since it is a tree, and contains all the nodes, since it is a spanning tree.

28 votes

-- saurabhrk (1k points)

2.23.2 Routing: GATE CSE 2014 Set 2 | Question: 23 top

<https://gateoverflow.in/1981>



- ✓ Both Routing Information Protocol (RIP) and Open Shortest Path First (OSPF) are Interior Gateway Protocol, i.e., they are both used within an autonomous system. RIP is an old protocol (not used anymore) based on distance vector routing. OSPF is based Link State Routing.

Correct Answer: A

17 votes

-- Divya Bharti (8.8k points)

2.23.3 Routing: GATE CSE 2014 Set 3 | Question: 26 top

<https://gateoverflow.in/2060>



- ✓ Answer is Interface 1.

Given address 133.23.151.76 coming to the first field of given routing table
 $\Rightarrow 131.16.0.0/12$

131.0001 0111.151.76

131.0001 0000.0.0 (\because given mask bits = 12)

$\Rightarrow 131.16.0.0$ Matched

Coming to the 2nd field of the given Routing table

$\Rightarrow 131.28.0.0/14$

131.0001 0111.151.76

131.0001 0100.0.0 (\because given mask bits = 14)

$\Rightarrow 131.20.0.0$ Not matched.

Coming to the 3rd field of the given Routing table
 Error! Not a valid link. 131.19.0.0/16

131.0001 0111.151.76

131.0001 0111.0.0 (\because given mask bits = 16)

$\Rightarrow 131.23.0.0$ Not matched

Coming to the 4th field of given Routing table

$\Rightarrow 131.22.0.0/15$

131.0001 0111.151.76

131.0001 0110.0.0 (\because given mask bits = 15)

$\Rightarrow 131.22.0.0$ Matched.

We are getting 1st and 4th entries are matched so among them we have to pick up longest mask bit, so output interface identifier is 1.

45 votes

-- saurabhrk (1k points)

2.23.4 Routing: GATE CSE 2017 Set 2 | Question: 09 top

<https://gateoverflow.in/11838>



- ✓ Statement 1 is **CORRECT** Bcoz RIP is one of the Oldest DVR(Distance Vector Routing) Protocols which employ the

hop count as a routing metric.

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Statement 2 is **CORRECT** Bcoz RIP uses the UDP as its transport protocol with port no 520.

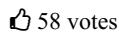
Statement 3 is **INCORRECT** Bcoz OSPF doesnot use a transport protocol such as UDP or TCP but encapsulates its data directly into IP Packets.

Statement 4 is **CORRECT** Bcoz OSPF is a routing protocol which uses Link State Routing(LSR) and works within a single Autonomous System.

PS:

OSPF needs to perform reliable multicasting because it needs to talk to multiple possible neighbors on the same network segment. Now, TCP does not support multicast and UDP is not reliable Therefore, OSPF implements its own transport mechanism that allows both for reliability (acknowledgements and retransmissions of lost segments) and multicasting, bypassing both TCP and UDP.

Hence, Option C is **CORRECT**.



58 votes

-- G VENKATESWARLU (461 points)



- ✓ Answer: D. II Only

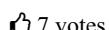
Explanation

Taking the given statements one by one:

I. (**FALSE**) Router needs to fragment the incoming IP packets if the connecting line has smaller MTU (Maximum Transmission Unit) than size of incoming packets.

II. (**TRUE**) That's the case of static routing where forward paths are pre-loaded/downloaded to routers.

III. (**FALSE**) This is not possible in case of cut-through-switching where IP packet is forwarded as it arrives.



7 votes

-- dhruvacks (609 points)



2.23.6 Routing: GATE IT 2005 | Question: 85a

https://gateoverflow.in/3858

Table for Node A		
A	-	-
B	B	1
C	C	1
D	B	2
E	C	2
F	C	3

Table for Node D		
A	B	2
B	B	1
C	C	1
D	-	-
E	E	1
F	F	1

Table for Node C		
A	A	1
B	B	1
C	-	-
D	D	1
E	E	1
F	D	2

Table for Node B		
A	A	1
B	-	-
C	C	1
D	D	1
E	C	2
F	D	2

Correct tables are as above.

Only **option C** is matching.



21 votes

-- Prashant Singh (47.2k points)



2.23.7 Routing: GATE IT 2005 | Question: 85b

https://gateoverflow.in/3859

- ✓ We consider **A B D F** at t they are:

The distance between A and the nodes **B,D,F** respectively are:

- $t : 123$
- $t + 1 : 323$
- $t + 2 : 343$
- $t + 3 : 545$
- $t + 4 : 565$
- $t + 5 : 767$
- $t + 6 : 787$
- $t + 7 : 989$
- $t + 8 : 9109$

and this continues...

So, in every two steps, they get incremented by 2

So at $t + 99$, F is 101

At $t + 100$, F is 101

So, count to infinity problem.

So, option A.

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-- Shreya Roy (3.8k points)

43 votes

2.23.8 Routing: GATE IT 2007 | Question: 63 [top](#)

<https://gateoverflow.in/3508>



✓ **OPTION is C.**

Here, we have to count average hops per message.

Steps:

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1) Message goes up from sender to root

2) Message comes down from root to destination

$$1) \text{ Average hops message goes to root} - \frac{(3 \times 8) + (2 \times 4) + (1 \times 2) + (0 \times 1)}{15} = 2.267$$

Here 3×8 represents 3 hops & 8 routers for Bottommost level & So on..

$$2) \text{ Similarly average hops when message comes down} - \frac{(3 \times 8) + (2 \times 4) + (1 \times 2) + (0 \times 1)}{15}$$

{Same as above}

So, Total Hops = $2 \times 2.267 = 4.53$ (**Answer**)

171 votes

-- Himanshu Agarwal (12.4k points)

2.23.9 Routing: GATE IT 2008 | Question: 67 [top](#)

<https://gateoverflow.in/3381>



✓ **S1 is true, S2 and S3 are false and S4 is true.**

Link State: <https://cseweb.ucsd.edu/classes/fa10/cse123/lectures/123-fa10-l12.pdf>

Distance Vector: <http://cseweb.ucsd.edu/classes/fa10/cse123/lectures/123-fa10-l13.pdf>

Correct Answer: D

References



gateoverflow.in

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26 votes

-- Arjun Suresh (332k points)

2.24

Serial Communication (I) [top](#)

2.24.1 Serial Communication: GATE CSE 1992 | Question: 02,v [top](#)

<https://gateoverflow.in/560>



Start and stop bits do not contain any 'information' but are used in serial communication

- a. Error detection
- b. Error correction
- c. Synchronization
- d. Slowing down the communications

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gate1992 easy computer-networks serial-communication multiple-selects

Answer

Answers: Serial Communication

2.24.1 Serial Communication: GATE CSE 1992 | Question: 02 top ↵

↗ <https://gateoverflow.in/560>



✓ Answer is C.

The start and stop bits are used to synchronize the serial receivers.

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Reference: <http://esd.cs.ucr.edu/labs/serial/serial.html>

References



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9 votes

-- Rajarshi Sarkar (27.9k points)

2.25

Sliding Window (15) top ↵

2.25.1 Sliding Window: GATE CSE 2003 | Question: 84 top ↵

↗ <https://gateoverflow.in/967>



Host A is sending data to host B over a full duplex link. A and B are using the sliding window protocol for flow control. The send and receive window sizes are 5 packets each. Data packets (sent only from A to B) are all 1000 bytes long and the transmission time for such a packet is $50 \mu s$. Acknowledgment packets (sent only from B to A) are very small and require negligible transmission time. The propagation delay over the link is $200 \mu s$. What is the maximum achievable throughput in this communication?

- A. 7.69×10^6 Bps
- B. 11.11×10^6 Bps
- C. 12.33×10^6 Bps
- D. 15.00×10^6 Bps

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gate2003-cse computer-networks sliding-window normal

Answer

2.25.2 Sliding Window: GATE CSE 2005 | Question: 25 top ↵

↗ <https://gateoverflow.in/1361>



The maximum window size for data transmission using the selective reject protocol with n -bit frame sequence numbers is:

- A. 2^n
- B. 2^{n-1}
- C. $2^n - 1$
- D. 2^{n-2}

gate2005-cse computer-networks sliding-window easy

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Answer

2.25.3 Sliding Window: GATE CSE 2006 | Question: 44 top ↵

↗ <https://gateoverflow.in/1820>



Station A uses 32 byte packets to transmit messages to Station B using a sliding window protocol. The round trip delay between A and B is 80 milliseconds and the bottleneck bandwidth on the path between A and B is 128 kbps. What is the optimal window size that A should use?

- A. 20
- B. 40
- C. 160
- D. 320

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gate2006-cse computer-networks sliding-window normal

Answer ↗

2.25.4 Sliding Window: GATE CSE 2006 | Question: 46 top ↵

↗ <https://gateoverflow.in/1822>



Station A needs to send a message consisting of 9 packets to Station B using a sliding window (window size 3) and go-back- n error control strategy. All packets are ready and immediately available for transmission. If every 5th packet that A transmits gets lost (but no acks from B ever get lost), then what is the number of packets that A will transmit for sending the message to B ?

- A. 12
- B. 14
- C. 16
- D. 18

gate2006-cse computer-networks sliding-window normal

Answer ↗

2.25.5 Sliding Window: GATE CSE 2007 | Question: 69 top ↵

↗ <https://gateoverflow.in/1267>



The distance between two stations M and N is L kilometers. All frames are K bits long. The propagation delay per kilometer is t seconds. Let R bits/second be the channel capacity. Assuming that the processing delay is negligible, the minimum number of bits for the sequence number field in a frame for maximum utilization, when the sliding window protocol is used, is:

- A. $\lceil \log_2 \frac{2LtR+2K}{K} \rceil$
- B. $\lceil \log_2 \frac{2LtR}{K} \rceil$
- C. $\lceil \log_2 \frac{2LtR+K}{K} \rceil$
- D. $\lceil \log_2 \frac{2LtR+2K}{2K} \rceil$

gate2007-cse computer-networks sliding-window normal

Answer ↗

2.25.6 Sliding Window: GATE CSE 2009 | Question: 57, ISRO2016-75 top ↵

↗ <https://gateoverflow.in/1340>



Frames of 1000 bits are sent over a 10^6 bps duplex link between two hosts. The propagation time is 25 ms. Frames are to be transmitted into this link to maximally pack them in transit (within the link).

What is the minimum number of bits (I) that will be required to represent the sequence numbers distinctly? Assume that no time gap needs to be given between transmission of two frames.

- A. $I = 2$
- B. $I = 3$
- C. $I = 4$
- D. $I = 5$

gate2009-cse computer-networks sliding-window normal isro2016

Answer ↗

2.25.7 Sliding Window: GATE CSE 2009 | Question: 58 top ↵

↗ <https://gateoverflow.in/43470>



Frames of 1000 bits are sent over a 10^6 bps duplex link between two hosts. The propagation time is 25ms. Frames are to be transmitted into this link to maximally pack them in transit (within the link).

Let I be the minimum number of bits (I) that will be required to represent the sequence numbers distinctly assuming that no time gap needs to be given between transmission of two frames.

Suppose that the sliding window protocol is used with the sender window size of 2^I , where I is the numbers of bits as mentioned earlier and acknowledgements are always piggy backed. After sending 2^I frames, what is the minimum time the sender will have to wait before starting transmission of the next frame? (Identify the closest choice ignoring the frame processing time)

- A. 16ms
- B. 18ms
- C. 20ms
- D. 22ms

gate2009-cse computer-networks sliding-window normal

Answer **2.25.8 Sliding Window: GATE CSE 2014 Set 1 | Question: 28** top ↗<https://gateoverflow.in/1795>

Consider a selective repeat sliding window protocol that uses a frame size of 1 KB to send data on a 1.5 Mbps link with a one-way latency of 50 msec. To achieve a link utilization of 60%, the minimum number of bits required to represent the sequence number field is _____.

gate2014-cse-set1 computer-networks sliding-window numerical-answers normal

Answer **2.25.9 Sliding Window: GATE CSE 2015 Set 3 | Question: 28** top ↗<https://gateoverflow.in/8481>

Consider a network connecting two systems located 8000 Km apart. The bandwidth of the network is 500×10^6 bits per second. The propagation speed of the media is 4×10^6 meters per second. It needs to design a Go-Back-N sliding window protocol for this network. The average packet size is 10^7 bits. The network is to be used to its full capacity. Assume that processing delays at nodes are negligible. Then, the minimum size in bits of the sequence number field has to be _____.

gate2015-cse-set3 computer-networks sliding-window normal numerical-answers

Answer **2.25.10 Sliding Window: GATE CSE 2016 Set 2 | Question: 55** top ↗<https://gateoverflow.in/39577>

Consider a 128×10^3 bits/second satellite communication link with one way propagation delay of 150 milliseconds. Selective retransmission (repeat) protocol is used on this link to send data with a frame size of 1 kilobyte. Neglect the transmission time of acknowledgement. The minimum number of bits required for the sequence number field to achieve 100% utilization is _____.

gate2016-cse-set2 computer-networks sliding-window normal numerical-answers

Answer **2.25.11 Sliding Window: GATE IT 2004 | Question: 81** top ↗<https://gateoverflow.in/3725>

In a sliding window ARQ scheme, the transmitter's window size is N and the receiver's window size is M . The minimum number of distinct sequence numbers required to ensure correct operation of the ARQ scheme is

- A. $\min(M, N)$
- B. $\max(M, N)$
- C. $M + N$
- D. MN

gate2004-it computer-networks sliding-window normal

Answer **2.25.12 Sliding Window: GATE IT 2004 | Question: 83** top ↗<https://gateoverflow.in/3727>

A 20 Kbps satellite link has a propagation delay of 400 ms. The transmitter employs the "go back n ARQ" scheme with n set to 10. Assuming that each frame is 100 byte long, what is the maximum data rate possible?

- A. 5 Kbps
- B. 10 Kbps
- C. 15 Kbps
- D. 20 Kbps

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gate2004-it computer-networks sliding-window normal

Answer 



Suppose that the maximum transmit window size for a TCP connection is 12000 bytes. Each packet consists of 2000 bytes. At some point in time, the connection is in slow-start phase with a current transmit window of 4000 bytes. Subsequently, the transmitter receives two acknowledgments. Assume that no packets are lost and there are no time-outs. What is the maximum possible value of the current transmit window?

- A. 4000 bytes
- B. 8000 bytes
- C. 10000 bytes
- D. 12000 bytes

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normal

Answer



Suppose that it takes 1 unit of time to transmit a packet (of fixed size) on a communication link. The link layer uses a window flow control protocol with a window size of N packets. Each packet causes an ack or a nak to be generated by the receiver, and ack/nak transmission times are negligible. Further, the round trip time on the link is equal to N units. Consider time $i > N$. If only acks have been received till time i (no naks), then the goodput evaluated at the transmitter at time i (in packets per unit time) is

- A. $1 - \frac{N}{i}$
- B. $\frac{i}{(N+i)}$
- C. 1
- D. $1 - e^{\left(\frac{i}{N}\right)}$

gate2006-it

computer-networks

sliding-window

normal

Answer



A 1 Mbps satellite link connects two ground stations. The altitude of the satellite is 36,504 km and speed of the signal is 3×10^8 m/s. What should be the packet size for a channel utilization of 25% for a satellite link using go-back-127 sliding window protocol? Assume that the acknowledgment packets are negligible in size and that there are no errors during communication.

- A. 120 bytes
- B. 60 bytes
- C. 240 bytes
- D. 90 bytes

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gate2008-it

computer-networks

sliding-window

normal

Answer

Answers: Sliding Window



- ✓ We need the maximum throughput, and for that we need to send as much data as possible to fully utilize the bandwidth.

so, maximum packets that can be sent = $1 + 2a = 9$ (after calculation) for 100% efficiency.

But we have a window size of 5 only, so we can send only 5 packets at max.

$$\text{Efficiency} = \frac{5}{9}$$

Now, $\frac{A}{Q}$, Bandwidth of the channel (BW) = $\frac{L}{T_t}$
 $= \frac{1000}{(50 \times 10^{-6})}$
 $= 20 \times 10^6$ bytes/sec.

So, max. throughput achievable = Efficiency \times BW

$= \frac{5}{9} \times 20 \times 10^6 = 11.11 \times 10^6$ bytes/sec.

Correct Answer: B

130 votes

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-- Ravi Ranjan (3k points)

I think options are given in bytes per sec instead of bits per sec.

Transmission time = 50 micro sec
Propagation time = 200 micro sec

RTT = $50 + 2 \times 200 = 450$ microsec

(Receiver can send an ACK as soon as the first packet is received)

Total number of bits transmitted before first ACK is received,
 $= 1000 \times 5 \times 8$ bits = 40000 bits

After first ACK is received, the same cycle of action repeats.

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So, Throughput = $\left(\frac{40000}{450}\right) \times 10^6$ bits

$= 88.88 \times 10^6$ bits per sec

$= 11.11 \times 10^6$ bytes per sec

47 votes

-- Parul Agarwal (661 points)

2.25.2 Sliding Window: GATE CSE 2005 | Question: 25

<https://gateoverflow.in/1361>



Answer is b)

In selective reject protocol, the maximum window size must be half the Sequence number space = $\frac{2^n}{2} = 2^{n-1}$.

For Go-back n, the maximum window size can be $2^n - 1$.

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<http://webmuseum.mi.fh-offenburg.de/index.php?view=exh&src=73> or [archive](#)

References



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48 votes

-- Aditi Dan (4k points)

2.25.3 Sliding Window: GATE CSE 2006 | Question: 44

<https://gateoverflow.in/1820>



Round trip delay = 80 ms.

Quoting from Wikipedia

the round-trip delay time (RTD) or round-trip time (RTT) is the length of time it takes for a signal to be sent plus the length of time it takes for an acknowledgment of that signal to be received.

Now, in many books including standard ones, they have used RTT to mean just the 2-way propagation delay by considering the signal/packet as of the smallest possible quantity so that its transmission time is negligible. The given question is following the first definition as given by Wikipedia which is clear from the choices.

During this time the first ACK arrives and so sender can continue sending frames.

So, for maximum utilization sender should have used the full bandwidth during this time.

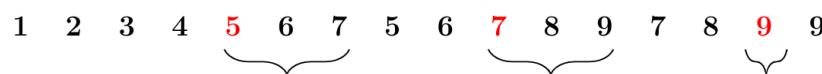
i.e., it should have sent $128 \text{ kbps} \times 80 \text{ ms}$ amount of data and a packet being of size 32 bytes, we get

$$\text{no. of packets} = \frac{128 \times 80}{32 \times 8} = 40.$$

Correct Answer: *B*

55 votes

-- Arjun Suresh (332k points)



Total 16 packet Transmission

Correct Answer: *C*

57 votes

-- riki_nitdgp_17 (143 points)

2.25.5 Sliding Window: GATE CSE 2007 | Question: 69 top

<https://gateoverflow.in/1267>



✓ **Answer: C**

We can send $\frac{\text{RTT}}{\text{Transmission Time}}$ number of packets

for maximum utilization of the channel, as in this time, we get the first ACK back and till that time, we can continue sending packets.

So, $\frac{\text{Transmission Time} + 2 \times \text{Propagation Time}}{\text{Transmission Time}}$ number of packets should be sent.

Therefore, bits required for the sequence number field:

$$\left\lceil \log_2 \left(\frac{\frac{K}{R} + 2Lt}{\frac{K}{R}} \right) \right\rceil = \left\lceil \log_2 \left(\frac{K + 2LtR}{K} \right) \right\rceil$$

Edit : here it is asked for general sliding window protocol not GBN nor SR .

In general sliding window protocol:

Sequence number bit = $\log(\text{sender window size})$

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65 votes

-- Rajarshi Sarkar (27.9k points)

2.25.6 Sliding Window: GATE CSE 2009 | Question: 57, ISRO2016-75 top

<https://gateoverflow.in/1340>



✓ Bandwidth won't be halved in full duplex.

<http://superuser.com/questions/335979/does-1-gbit-s-port-in-full-duplex-mean-1-gbit-s-send-and-1-gbit-s-receive>

Propagation time is given as 25 ms.

Bandwidth = 10^6 bps .

So, to fully utilize the channel, we must send 10^6 bits into the channel in a second, which will be 1000 frames per second as each frame is 1000 bits.

Now, since the propagation time is 25 ms, to fully pack the link we need to send at least $1000 \times 25 \times 10^{-3} = 25$ frames.

So, we need $\lceil \log_2 25 \rceil = 5$ bits.

Correct Answer: D

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References

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114 votes

-- Arjun Suresh (332k points)

2.25.7 Sliding Window: GATE CSE 2009 | Question: 58 top

<https://gateoverflow.in/43470>



- ✓ Bandwidth won't be halved in full duplex. <http://superuser.com/questions/335979/does-1-gbit-s-port-in-full-duplex-mean-1-gbit-s-send-and-1-gbit-s-receive>

Propagation time is given as 25 ms.

Bandwidth = 10^6 bps,

So, to fully utilize the channel, we must send 10^6 bits into the channel in a second, which will be 1000 frames per second as each frame is 1000 bits. Now, since the propagation time is 25 ms, to fully pack the link we need to send at least $1000 \times 25 \times 10^{-3} = 25$ frames. So, we need $\lceil \log_2 25 \rceil = 5$ bits.

$I = 5$, so $2^I = 32$ frames are sent.

Now, we need to get RTT (which is the time between which a frame is sent and its ACK is received), to determine the waiting time.

Transmission time (for a frame of size 1000 bits) = $1000/10^6 = 1$ ms.

So, transmission time for 32 frames = 32 ms.

RTT = Propagation time for frame + Transmission time for frame + Propagation time for ACK + Transmission time for ACK

$$= 25 \text{ ms} + 1 \text{ ms} + 25 \text{ ms} + 1 \text{ ms} \quad (\text{ACK is piggy backed and assuming frame size for piggy backing is also 1000 bits}) \\ = 52 \text{ ms}$$

So, waiting time = $52 - 32 = 20$ ms. (For the 32 ms, the sender was transmitting and not waiting)

Correct Answer: C

References



105 votes

-- Arjun Suresh (332k points)

2.25.8 Sliding Window: GATE CSE 2014 Set 1 | Question: 28 top

<https://gateoverflow.in/1795>



✓
$$\eta_{SR} = \frac{N}{1 + 2a}$$

$$B = 1.5 \text{ Mbps}$$

$$T_p = 50 \text{ ms}$$

$$L = 1 \text{ KB} = 1024 \times 8 \text{ bits}$$

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$$\eta_{SR} = 60\%$$

$$\therefore 0.6 = \frac{N}{1+2a}$$

$$\implies N = 0.6(1+2a)$$

$$a = \frac{T_p}{T_t} = \frac{T_p}{L} \cdot B = \frac{50 \times 10^{-3} \times 1.5 \times 10^6}{1024 \times 8} = 9.155$$

$$\therefore N = 0.6 \times (1 + 2 \times 9.155) = 11.58$$

$$w_s + w_R \leq \text{ASN}$$

$$\implies 2N \leq \text{ASN}$$

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$$\implies 2 \times 11.58 \leq \text{ASN}$$

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$$\implies \text{ASN} \geq \lceil 23.172 \rceil$$

$$\implies \text{ASN} \geq 24$$

\therefore Minimum number of bits required for sequence number field = $\lceil \log_2 24 \rceil = 5$.

126 votes

-- Vikrant Singh (11.2k points)

A frame is 1 KB and takes $\frac{8 \times 10^3}{1.5 \times 10^6} s = 5.33 ms$

to reach the destination. (8 is used to convert byte to bits)

Adding the propagation delay of 50 ms, the total time will be $50 + 5.33 = 55.33 ms$

Now, we need the ACK to reach back also, so the time between a packet is sent and an ACK is received = $55.33 + 50$ (transmission time of ACK neglected) = 105.33 ms

The channel band width is 1.5 Mbps, so in 1 ms, $1.5K$ bits can be transferred and so in 105.33 ms, $1.5 \times 105.33 \times 1.5K$ bits can be transferred.

To, ensure 60% utilization, amount of bits to be transferred in

$$1 ms = 1.5 \times 105.33 \times 1.5K \times 0.6 = 94.797 Kb = \frac{94.797}{(8 \times 1000)} \text{ frames}$$

= 11.849 frames ≈ 12 frames.

(we bounded up to ensure at least 60% utilization)

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So, we need a minimum window size of 12.

Now, in selective repeat protocol, the window size must be less than half the sequence number space.

<http://stackoverflow.com/questions/3999065/why-is-window-size-less-than-or-equal-to-half-the-sequence-number-in-sr-protocol>

So, this means sequence number space must be larger than $2 \times 12 = 24$.

To have a sequence number space of 24, sequence bits must be at least $\log_2 24 = 5$

References



44 votes

-- Arjun Suresh (332k points)

2.25.9 Sliding Window: GATE CSE 2015 Set 3 | Question: 28 [top](#)

→ <https://gateoverflow.in/8481>



✓ Answer = 8 bits.

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In order to achieve full utilization, sender has to keep on sending frames till the acknowledgement arrives for the first frame.

Time taken for acknowledgement to arrive is 2 times propagation delay + transmission time for a frame.

$$\text{One way propagation delay} = \frac{8000 \times 10^3}{(4 \times 10^6)} = 2s$$

$$\text{Time taken to transmit one frame} = \frac{10^7}{(500 \times 10^6)} = 0.02s$$

$$\text{So, RTT} = 2 \times 2 + 0.02 = 4.02s$$

$$\text{No. of frames that can be transmitted in 4.02 secs} = \frac{4.02}{0.02} = 201$$

Being Go-Back-N protocol this means $W_s = 201$ and $W_r = 1$. So, total number of sequence numbers required = $201 + 1 = 202$.

Hence, minimum number of bits required for sequence numbers till 202 is $\lceil \log_2 202 \rceil = 8$.

47 votes

-- overtomana (945 points)

2.25.10 Sliding Window: GATE CSE 2016 Set 2 | Question: 55

<https://gateoverflow.in/39577>



✓ Answer is 4 bits.

As we want 100% efficiency(μ), $w_s = 1 + 2a$

$$\begin{aligned} a &= \frac{\text{propagation time}}{\text{transmission time}} \\ &= \frac{150}{1024 \times \frac{8}{128}} = \frac{150}{64} = 2.34, \end{aligned}$$

$$\Rightarrow w_s = 1 + 2a = 5.6875 \approx 6$$

Available seq numbers $\geq w_s + w_r$

In Selective Repeat,

$w_s = w_r$ (let it be n)

$$2 \times n = 2 \times 6 = 12$$

avail seq numbers ≥ 12

So, minimum seq numbers are 12.

Number of bits for that is $\lceil \log_2 12 \rceil = 4$.

78 votes

-- Sreyas S (1.6k points)

2.25.11 Sliding Window: GATE IT 2004 | Question: 81

<https://gateoverflow.in/3725>



✓ C) M+N

Because $W_s + W_r \leq$ Sequence numbers (as the maximum number of unacknowledged packets at sender will be W_s and at the receiver it will be W_r , similar to the sequence numbering in Selective Repeat)

where W_s is size of sender window and W_r is receiver window size.

39 votes

-- Parul Agarwal (661 points)



✓ **Answer: B**

$$\text{Transmission Time} = \frac{100 \times 8\text{bits}}{20 \text{ Kbps}} = 40 \text{ ms}$$

Propagation Time = 400 ms

$$\text{Efficiency} = \frac{\text{Window Size} \times \text{Transmission Time}}{(\text{Transmission Time} + 2 \times \text{Propagation Time})}$$

$$= \frac{10 \times 40}{(40 + 2 \times 400)} = 0.476$$

Maximum Data Rate = $0.476 \times 20 \text{ Kbps} = 9.52 \text{ Kbps}$

which is close to option B.

51 votes

-- Rajarshi Sarkar (27.9k points)



- ✓ In slow-start phase, for each ACK, the sender increases the current transmit window by Maximum Segment Size (MSS). In the question it is given a packet consists of 2000 bytes and that can be taken as MSS. So, after two ACKs, current transmit window
 $= 4000 + 2000 + 2000$
 $= 8000$

<http://www.ece.virginia.edu/~mv/edu/ee136/Lectures/congestion-control/tcp-congestion-control.pdf> or [archive](#)

Correct Answer: B

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References



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65 votes

-- Arjun Suresh (332k points)



- ✓ In [computer networks](#), **goodput** is the application level [throughput](#), i.e. the number of useful information [bits](#) delivered by the network to a certain destination per unit of time. (From wikipedia).

So, successful delivery of packet can be assured if ACK has been received for it.

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So till time ' i' ' we would have transmitted ' i' ' packets but only $(i - N)$ can be acknowledged as minimum time for a packet to get Acknowledged is N (since RTT is N which is equal to the window size, there is no waiting time for the sender).

So, successfully delivered packets = $(i - N)$

Time for transmission = i

$$\text{Goodput} = \frac{\text{Successfully delivered data}}{\text{Time}}$$

$$= \frac{(i - N)}{i}$$

$$= 1 - \frac{N}{i}$$

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Therefore (A)

References



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88 votes

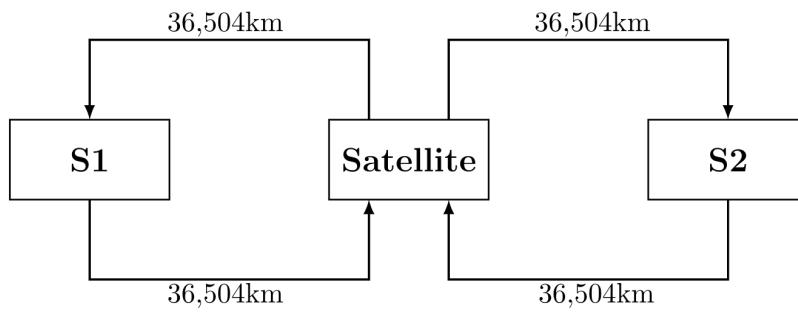
-- Sandeep_Uniyal (6.5k points)

2.25.15 Sliding Window: GATE IT 2008 | Question: 64 [top](#)

- ✓ Distance from Station A to Satellite = 36504×10^3 m

$$\text{Time to reach satellite} = \frac{36504000}{300000000} = 0.12168\text{s}$$

RTT (for a bit) = $4 \times \text{Time to reach satellite}(S1 \rightarrow \text{Satellite}, \text{Satellite} \rightarrow S2, S2 \rightarrow \text{Satellite}, \text{Satellite} \rightarrow S1)$



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Efficiency is the ratio of the amount of data sent to the maximum amount of data that could be sent. Let X be the packet size.

In Go-Back-N, within RTT we can send n packets. So, useful data is $n \times X$, where X is the packet size. Now, before we can send another packet ACK must reach back. Time for this is transmission time for a packet (other packets are pipelined and we care only for first ACK), and RTT for a bit, (propagation times for the packet + propagation time for ACK + transmission time for ACK – neglected as per question)

$$\text{Efficiency} = \frac{\text{Transmitted Data Size}}{\text{Packet Size} + \text{RTT}_{bit} \times \text{Bandwidth}}$$

$$\Rightarrow 0.25 = \frac{127 \times X}{X + 4 \times 0.12168 \times B}$$

$$\Rightarrow 0.25X + 0.25 \times 4 \times 0.12168 \times B = 127X$$

$$\Rightarrow 0.25X + 0.12168 \times 10^6 = 127X$$

$$\Rightarrow 121680 = 126.75X$$

$$\Rightarrow X = 9.6 \times 10^{-4} \times 10^6 = 960$$

\therefore Packet Size = 960 bits = 120 Bytes

So, option (A) is the answer.

84 votes

-- Danish (3.4k points)

2.26

Sockets (4) [top](#)2.26.1 Sockets: GATE CSE 2008 | Question: 17 [top](#)<https://gateoverflow.in/415>

Which of the following system calls results in the sending of SYN packets?

- A. socket
- B. bind

- C. listen
D. connect

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Answer 

2.26.2 Sockets: GATE CSE 2008 | Question: 59 [top](#)

<https://gateoverflow.in/482>



A client process P needs to make a TCP connection to a server process S. Consider the following situation: the server process S executes a socket(), a bind() and a listen() system call in that order, following which it is preempted. Subsequently, the client process P executes a socket() system call followed by connect() system call to connect to the server process S. The server process has not executed any accept() system call. Which one of the following events could take place?

- A. connect() system call returns successfully
B. connect() system call blocks
C. connect() system call returns an error
D. connect() system call results in a core dump

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Answer 

2.26.3 Sockets: GATE CSE 2014 Set 2 | Question: 24 [top](#)

<https://gateoverflow.in/1982>



Which of the following socket API functions converts an unconnected active TCP socket into a passive socket?

- A. connect
B. bind
C. listen
D. accept

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Answer 

2.26.4 Sockets: GATE CSE 2015 Set 2 | Question: 20 [top](#)

<https://gateoverflow.in/8108>



Identify the correct order in which a server process must invoke the function calls accept, bind, listen, and recv according to UNIX socket API.

- A. listen, accept, bind, recv
B. bind, listen, accept, recv
C. bind, accept, listen, recv
D. accept, listen, bind, recv

gate2015-cse-set2 | computer-networks | sockets | easy

Answer 

Answers: Sockets

2.26.1 Sockets: GATE CSE 2008 | Question: 17 [top](#)

<https://gateoverflow.in/415>



✓ Answer is (D).

- **socket()** creates a new socket of a certain socket type, identified by an integer number, and allocates system resources to it.
- **bind()** is typically used on the server side, and associates a socket with a socket address structure, i.e. a specified local port number and IP address.
- **listen()** is used on the server side, and causes a bound TCP socket to enter listening state.
- **connect()** is used on the client side, and assigns a free local port number to a socket. In case of a TCP socket, it causes an attempt to establish a new TCP connection.

When `connect()` is called by client, following three way handshake happens to establish the connection in TCP.

1. The client requests a connection by sending a SYN (synchronize) message to the server.
2. The server acknowledges this request by sending SYN-ACK back to the client.
3. The client responds with an ACK, and the connection is established.

58 votes

-- minal (13.1k points)

2.26.2 Sockets: GATE CSE 2008 | Question: 59 [top](#)

<https://gateoverflow.in/482>



- ✓ First thing to note: All the sockets are by default in BLOCKING mode. What do we mean by blocking ??

Blocking mode means that when we make a system call, it blocks the caller for the time "when call() is made till the job is done OR an error returns ". We can set each socket to Non-blocking explicitly. Setting to Non-Blocking means we are telling the kernel that "If the system call cant be completed without putting process to sleep then DON'T put the process to sleep . Instead return with an ERROR immediately and continue the process" which can be checked for the completion by the caller in between the execution of other tasks.

Now coming to this question:

Suppose `connect()` is in default blocking mode then calling `connect()` sends SYN packet to the server. Since server has not executed any `accept()` call it can not acknowledge the SYN packet. `Connect()` in blocking mode keep sending SYN packets at fixed intervals(first after 6 sec, second after 24 sec typically until 75 sec latest). This is done until an error ETIMEDOUT is returned by the TCP.(in this case,else there are several other type of errors returned in case No port exists for that connection or server id not listening etc.)

Here, option **(B)** saying that `connect()` blocks is not entirely wrong but since we know that `accept()` call is not made by server, `connect()` WILL NOT WAIT FOREVER and SO IT CAN NOT BLOCK. It will ultimately return with an ERROR message.

So, option **(C)** is CORRECT.

Core dump thing I don't know about!

But once `connect()` returns error that socket can not be reused and must be CLOSED.

And a non-blocking `connect()` is never blocked and immediately returns with an error if connection is not successful although IT CONTINUES WITH TRYING TO CONNECT .Error here just means that it returns a message saying "I could not connect immediately BUT i am trying AND you can check it in between.

Hope it clears a bit.

98 votes

-- Sandeep_Uniyal (6.5k points)



2.26.3 Sockets: GATE CSE 2014 Set 2 | Question: 24 [top](#)

<https://gateoverflow.in/1982>

- ✓ **(C)** is ans listen converts unconnected socket into passive connect i.e it is waiting for request from client

35 votes

-- Pooja Palod (24.1k points)

2.26.4 Sockets: GATE CSE 2015 Set 2 | Question: 20 [top](#)

<https://gateoverflow.in/8108>



- ✓ Answer: **(B)**

Bind: Binds the socket to an address

Listen: Waits for connections to the socket

Accept: Accepts a connection to the socket

Recv: Receives data from connection

From Man page of accept:

It extracts the first connection request on the queue of pending connections for the listening socket, creates a new connected socket, and returns a new file descriptor referring to that socket. The newly created socket is not in the listening state. The original socket is unaffected by this call

35 votes

-- Rajarshi Sarkar (27.9k points)

2.27

Stop And Wait (5) [top](#)

2.27.1 Stop And Wait: GATE CSE 2015 Set 1 | Question: 53 [top](#)

▪ <https://gateoverflow.in/8363>



Suppose that the stop-and-wait protocol is used on a link with a bit rate of 64 kilobits per second and 20 milliseconds propagation delay. Assume that the transmission time for the acknowledgment and the processing time at nodes are negligible. Then the minimum frame size in bytes to achieve a link utilization of at least 50 % is _____.

gate2015-cse-set1 computer-networks stop-and-wait normal numerical-answers

Answer

2.27.2 Stop And Wait: GATE CSE 2016 Set 1 | Question: 55 [top](#)

▪ <https://gateoverflow.in/39696>



A sender uses the Stop-and-Wait ARQ protocol for reliable transmission of frames. Frames are of size 1000 bytes and the transmission rate at the sender is 80 Kbps (1 Kbps = 1000 bits/second). Size of an acknowledgment is 100 bytes and the transmission rate at the receiver is 8 Kbps. The one-way propagation delay is 100 milliseconds.

Assuming no frame is lost, the sender throughput is _____ bytes/ second.

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Answer

2.27.3 Stop And Wait: GATE CSE 2017 Set 1 | Question: 45 [top](#)

▪ <https://gateoverflow.in/118328>



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The values of parameters for the Stop-and-Wait ARQ protocol are as given below:

- Bit rate of the transmission channel = 1 Mbps.
- Propagation delay from sender to receiver = 0.75 ms.
- Time to process a frame = 0.25 ms.
- Number of bytes in the information frame = 1980.
- Number of bytes in the acknowledge frame = 20.
- Number of overhead bytes in the information frame = 20.

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Assume there are no transmission errors. Then, the transmission efficiency (expressed in percentage) of the Stop-and-Wait ARQ protocol for the above parameters is _____ (correct to 2 decimal places).

gate2017-cse-set1 computer-networks stop-and-wait numerical-answers normal

Answer

2.27.4 Stop And Wait: GATE IT 2005 | Question: 72 [top](#)

▪ <https://gateoverflow.in/3835>



A channel has a bit rate of 4 kbps and one-way propagation delay of 20 ms. The channel uses stop and wait protocol. The transmission time of the acknowledgment frame is negligible. To get a channel efficiency of at least 50%, the minimum frame size should be

- A. 80 bytes
- B. 80 bits
- C. 160 bytes
- D. 160 bits

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Answer

2.27.5 Stop And Wait: GATE IT 2006 | Question: 68 [top](#)

▪ <https://gateoverflow.in/3612>



On a wireless link, the probability of packet error is 0.2. A stop-and-wait protocol is used to transfer data across the link. The channel condition is assumed to be independent of transmission to transmission. What is the average number of transmission attempts required to transfer 100 packets?

- A. 100
- B. 125
- C. 150
- D. 200

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Answer 

Answers: Stop And Wait

2.27.1 Stop And Wait: GATE CSE 2015 Set 1 | Question: 53 top ↗<https://gateoverflow.in/8363>

✓ Link Utilization = $\frac{\text{Amount of data sent}}{\text{Max. amount of data that could be sent}}$

Let x be the frame size in bits.

In stop-and-wait protocol, once a frame is sent, next frame won't be sent until ACK is received.

Time for this,

$$\begin{aligned} \text{RTT} &= \text{Propagation delay for frame} + \text{Transmission time for frame} \\ &\quad + \text{Propagation delay for ACK} + \text{Transmission time for ACK} \\ &= 20 \text{ ms} + \frac{x}{64 \text{ ms}} + 20 \text{ ms} + 0 \quad (\text{as given in question}) \\ &= \left(40 + \frac{x}{64}\right) \text{ ms}. \end{aligned}$$

Amount of data sent during RTT = x

$$\text{Max. amount of data that could be sent} = \left(40 + \frac{x}{64}\right) \times 64 = 2560 + x \text{ bits}.$$

$$\text{So, link utilization, } 0.5 = \frac{x}{(2560 + x)}$$

$$x = 2560 \text{ bits} = 320 \text{ bytes}.$$

Alternative Approach ,

Link utilization or efficiency of stop and wait protocol is ,

$$\text{efficiency} = \frac{T_x}{(T_x + 2T_p)} = \frac{1}{\left(1 + 2\left(\frac{T_p}{T_x}\right)\right)} = \frac{1}{(1 + 2a)},$$

$$\text{where , Transmission time} = T_x = \frac{\text{packet size}}{\text{bandwidth}} = \frac{L}{B}$$

$$\text{Propagation time} = T_p = \frac{\text{distance}}{\text{speed}} = \frac{d}{v}, \text{ and}$$

$$a = \frac{\text{Propagation time}}{\text{Transmission time}} = \frac{T_p}{T_x},$$

Now for 50% efficiency ,

$$\text{efficiency} = \frac{1}{(1 + 2a)}$$

$$50\% = \frac{1}{(1 + 2a)}$$

$$\frac{1}{2} = \frac{1}{(1 + 2a)}$$

$$2 = (1 + 2a)$$

$$2 - 1 = 2a$$

$$1 = 2\left(\frac{T_p}{T_x}\right)$$

$$T_x = 2 \times T_p$$

$$\frac{L}{B} = 2 \times 20 \text{ ms}$$

$$\begin{aligned}
 L &= 2 \times 20 \text{ ms} \times B = 2 \times 20 \times 10^{-3} \times 64 \text{ k bits} \\
 &= 2 \times 20 \times 10^{-3} \times 64 \times 10^3 \text{ bits} \\
 L &= 40 \times 64 \text{ bits} = 40 \times \frac{64}{8} \text{ bytes} = 40 \times 8 \text{ bytes} = 320 \text{ bytes (answer)}
 \end{aligned}$$

59 votes

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-- Arjun Suresh (332k points)

2.27.2 Stop And Wait: GATE CSE 2016 Set 1 | Question: 55 [top](#)

<https://gateoverflow.in/39696>



- ✓ Answer is 2500 bytes per second.

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Throughput is number of bytes we are able to send per second.

Calculate the transmission time of sender $T_{t(Recv)}$, calculate one way propagation delay T_p , Calculate the transmission time of receiver $T_{t(Recv)}$

We get $T_{t(Recv)}$ here as $\frac{1}{10}$ seconds,

T_p as $\frac{1}{10}$ seconds (given in question as 100 ms),

$T_{t(Recv)}$ as $\frac{1}{10}$ seconds.

So, total time taken to send a frame from sender to destination,

$$= T_{t(Recv)} + 2 \times T_p + T_{t(Recv)} = \frac{4}{10} \text{ seconds}$$

So, we can send 1000 bytes (frame size) in $\frac{4}{10}$ seconds.
in 1 second, we can send 2500 bytes. So throughput is 2500 bytes per second.

62 votes

-- Sreyas S (1.6k points)

Answer is 2500.

$$\text{Sender transmission time} = \frac{1000 \times 8}{(80 \times 1000)} = 0.1 \text{ sec} = 100 \text{ ms}$$

$$\text{Receiver transmission time} = \frac{100 \times 8}{(8 \times 1000)} = 0.1 \text{ sec} = 100 \text{ ms}$$

$$\text{RTT} = 2 \times 100 = 200 \text{ ms}$$

$$\text{So, Total time} = 400 \text{ ms}$$

In 400 ms, we send only 1000 bytes so,

$$\text{Throughput} = \frac{1000}{(400 \times 10^{-3})} = 2500 \text{ bytes / sec}$$

44 votes

-- Deepak Sharma (545 points)

2.27.3 Stop And Wait: GATE CSE 2017 Set 1 | Question: 45 [top](#)

<https://gateoverflow.in/118328>



- ✓ Efficiency is usually calculated as, $\frac{\text{InfoFrame Transmit Time}}{\text{TotalTime}}$

$$\text{Efficiency} = \frac{\text{InfoFrame Transmit Time}}{\text{InfoFrame Transmit Time} + \text{InfoFrame Process Time} + 2 \times \text{Prop Delay} + \text{AckFrame Transmit Time} + \text{AckFrame Process Time}}$$

Reference to calculate efficiency formula:

http://nptel.ac.in/courses/106106091/pdf/Lecture13_StopAndWaitAnalysis.pdf

<http://spinlab.wpi.edu/courses/ece230x/lec14-15.pdf>

From the question it is not very clear whether frame processing time is mentioned about InfoFrame or AckFrame or Combined. It is also explicitly not mentioned whether to consider Frame Processing time for ACK or not. Thus, following are the different inferences that could be made from the question -

1. As Size of InfoFrame (1980-2000 Bytes) is very large as compared to AckFrame (20 Bytes) one could assume the given processing time is for InfoFrame and processing time for AckFrame is negligible. The processing time does depend on size of frame for various parameters one of them is checksum calculation.
Check the below reference for more details -
http://rp-www.cs.usyd.edu.au/~suparerk/Research/Doc/Stop-and-Wait_Simulation.pdf
2. It is also mentioned in the question that there are no transmission errors. One can also think as an hint that since frames are successfully transmitted there is no need for ACK processing at sender Side
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3. Considering frame processing time given is combined both ACK+Info Frame
4. Considering frame processing time individually and which is the Ans in Official key (**86.5 - 87.5**)

The below answers could be due to cases 1,2,3 -

No. of Bytes in the Information frame = 1980 Bytes

(Not very clear from question whether it implies total bytes or data bytes)

No of OverHead Bytes = 20 Bytes

Assuming they have explicitly mentioned Overhead bytes -

Total Frame Size = No of Bytes in the Information frame + No of OverHead Bytes = 2000 B

$$\text{InfoTransmission Time} = \frac{\text{InfoFrame Size}}{\text{Bandwidth}}$$

$$= \frac{2000 \times 8}{1 \times 10^6} = 16 \text{ ms}$$

$$\text{AckTransmissionTime} = \frac{20 \times 8}{1 \times 10^6} = 0.16 \text{ ms}$$

$$\text{Efficiency} = \frac{16}{16 + 2 \times 0.75 + 0.25 + 0.16}$$

$$= 89.34\% \text{ (After round-off)}$$

Assuming bytes in information includes Overhead bytes -

InfoFrameTranmission Time = 15.84

Efficiency = 89.23 %

Range could be 87.5 - 89.34

Reference to the similar questions:

<https://gateoverflow.in/43981/isro-2013-41>

<https://gateoverflow.in/39696/gate-2016-1-55>

More Efficiency Concept Reference:

<http://nptel.ac.in/courses/Webcourse-contents/IIT%20Kharagpur/Computer%20networks/pdf/M3L3.pdf>

References



57 votes

-- yg92 (2.3k points)

2.27.4 Stop And Wait: GATE IT 2005 | Question: 72 top

<https://gateoverflow.in/3835>



- ✓ For 50% utilization with Stop-and-wait,

$$\frac{t_t}{t_t + 2t_p} \geq \frac{1}{2},$$

where, t_t – Transmission time, t_p – propagation delay. Here, $t_t = \frac{L}{B}$, where L is the frame length in bits and B is the bitrate of the channel.

$$2t_t \geq t_t + 2t_p$$

$$t_t \geq 2t_p$$

$$\frac{L}{B} \geq 2 \times t_p$$

$$L \geq 2 \times t_p \times B$$

$$\Rightarrow L = 2 \times 20 \times 10^{-3} \times 4 \times 10^3 = 160 \text{ bits}$$

So, answer is D.

32 votes

-- Pooja Palod (24.1k points)

2.27.5 Stop And Wait: GATE IT 2006 | Question: 68 [top](#)

<https://gateoverflow.in/3612>



- ✓ Consider that we have to send N packets and p is the error probability rate. Error rate p implies that if we are sending N packets then $N \times p$ packets will be lost and thus we have to resend those $N \times p$ packets. But the error is still there, so again while resending those $N \times p$ packets, $N \times p \times p$ will be further lost and so on. Hence, this forms a series as follows:

$$\begin{aligned} & N + N \times p + N \times p^2 + \dots \\ &= N(1 + p + p^2 + \dots) \\ &= \frac{N}{1-p} \text{(Sum to infinite GP series)} \end{aligned}$$

Now we are having $N = 100$ and $p = 0.2$, which implies 125 packets have to be sent on average.

Correct Answer: B

46 votes

-- AAKASH SAINI (1.6k points)

2.28

Subnetting (18) [top](#)

2.28.1 Subnetting: GATE CSE 2003 | Question: 82, ISRO2009-1 [top](#)

<https://gateoverflow.in/965>



The subnet mask for a particular network is 255.255.31.0. Which of the following pairs of IP addresses could belong to this network?

- 172.57.88.62 and 172.56.87.23
- 10.35.28.2 and 10.35.29.4
- 191.203.31.87 and 191.234.31.88
- 128.8.129.43 and 128.8.161.55

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[gate2003-cse](#) [computer-networks](#) [subnetting](#) [normal](#) [isro2009](#)

Answer

2.28.2 Subnetting: GATE CSE 2004 | Question: 55 [top](#)

<https://gateoverflow.in/1051>



The routing table of a router is shown below:

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Destination	Subnet Mask	Interface
128.75.43.0	255.255.255.0	Eth0
128.75.43.0	255.255.255.128	Eth1
192.12.17.5	255.255.255.255	Eth3
Default		Eth2

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On which interface will the router forward packets addressed to destinations 128.75.43.16 and 192.12.17.10 respectively?

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- Eth1 and Eth2
- Eth0 and Eth2

- C. Eth0 and Eth3
D. Eth1 and Eth3

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Answer ↗

2.28.3 Subnetting: GATE CSE 2005 | Question: 27 top ↗

↗ <https://gateoverflow.in/1363>



An organization has a class *B* network and wishes to form subnets for 64 departments. The subnet mask would be:

- A. 255.255.0.0
- B. 255.255.64.0
- C. 255.255.128.0
- D. 255.255.252.0

gate2005-cse computer-networks subnetting normal

Answer ↗

2.28.4 Subnetting: GATE CSE 2006 | Question: 45 top ↗

↗ <https://gateoverflow.in/1821>



Two computers *C1* and *C2* are configured as follows. *C1* has IP address 203.197.2.53 and netmask 255.255.128.0. *C2* has IP address 203.197.75.201 and netmask 255.255.192.0. Which one of the following statements is true?

- A. *C1* and *C2* both assume they are on the same network
- B. *C2* assumes *C1* is on same network, but *C1* assumes *C2* is on a different network
- C. *C1* assumes *C2* is on same network, but *C2* assumes *C1* is on a different network
- D. *C1* and *C2* both assume they are on different networks.

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Answer ↗

2.28.5 Subnetting: GATE CSE 2007 | Question: 67, ISRO2016-72 top ↗

↗ <https://gateoverflow.in/1265>



The address of a class *B* host is to be split into subnets with a 6-bit subnet number. What is the maximum number of subnets and the maximum number of hosts in each subnet?

- A. 62 subnets and 262142 hosts.
- B. 64 subnets and 262142 hosts.
- C. 62 subnets and 1022 hosts.
- D. 64 subnets and 1024 hosts.

gate2007-cse computer-networks subnetting easy isro2016

Answer ↗

2.28.6 Subnetting: GATE CSE 2008 | Question: 57 top ↗

↗ <https://gateoverflow.in/480>



If a class *B* network on the Internet has a subnet mask of 255.255.248.0, what is the maximum number of hosts per subnet?

- A. 1022
- B. 1023
- C. 2046
- D. 2047

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Answer ↗



Suppose computers A and B have IP addresses 10.105.1.113 and 10.105.1.91 respectively and they both use same netmask N . Which of the values of N given below should not be used if A and B should belong to the same network?

- A. 255.255.255.0
- B. 255.255.255.128
- C. 255.255.255.192
- D. 255.255.255.224

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Answer



An Internet Service Provider (ISP) has the following chunk of CIDR-based IP addresses available with it: 245.248.128.0/20. The ISP wants to give half of this chunk of addresses to Organization A , and a quarter to Organization B , while retaining the remaining with itself. Which of the following is a valid allocation of addresses to A and B ?

- A. 245.248.136.0/21 and 245.248.128.0/22
- B. 245.248.128.0/21 and 245.248.128.0/22
- C. 245.248.132.0/22 and 245.248.132.0/21
- D. 245.248.136.0/24 and 245.248.132.0/21

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Answer



Consider the following routing table at an IP router:

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Network No	Net Mask	Next Hop
128.96.170.0	255.255.254.0	Interface 0
128.96.168.0	255.255.254.0	Interface 1
128.96.166.0	255.255.254.0	R2
128.96.164.0	255.255.252.0	R3
0.0.0.0	Default	R4

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For each IP address in Group I Identify the correct choice of the next hop from Group II using the entries from the routing table above.

Group I	Group II
i) 128.96.171.92	a) Interface 0
ii) 128.96.167.151	b) Interface 1
iii) 128.96.163.151	c) R2
iv) 128.96.164.121	d) R3
	e) R4

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- A. i-a, ii-c, iii-e, iv-d
- B. i-a, ii-d, iii-b, iv-e
- C. i-b, ii-c, iii-d, iv-e
- D. i-b, ii-c, iii-e, iv-d

gate2015-cse-set2 computer-networks subnetting easy

Answer



In the network 200.10.11.144/27, the *fourth* octet (in decimal) of the last IP address of the network which can be assigned

to a host is _____.

gate2015-cse-set3 computer-networks subnetting normal numerical-answers

Answer 

2.28.11 Subnetting: GATE CSE 2019 | Question: 28 [top](#) 

<https://gateoverflow.in/302820>



Consider three machines M, N, and P with IP addresses 100.10.5.2, 100.10.5.5, and 100.10.5.6 respectively. The subnet mask is set to 255.255.255.252 for all the three machines. Which one of the following is true?

- A. M, N, and P all belong to the same subnet
- B. Only M and N belong to the same subnet
- C. Only N and P belong to the same subnet
- D. M, N, and P belong to three different subnets

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gate2019-cse computer-networks subnetting

Answer 

2.28.12 Subnetting: GATE CSE 2020 | Question: 38 [top](#) 

<https://gateoverflow.in/333193>



An organization requires a range of IP address to assign one to each of its 1500 computers. The organization has approached an Internet Service Provider (ISP) for this task. The ISP uses CIDR and serves the requests from the available IP address space 202.61.0.0/17. The ISP wants to assign an address space to the organization which will minimize the number of routing entries in the ISP's router using route aggregation. Which of the following address spaces are potential candidates from which the ISP can allot any one of the organization?

- I. 202.61.84.0/21
- II. 202.61.104.0/21
- III. 202.61.64.0/21
- IV. 202.61.144.0/21

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- A. I and II only
- B. II and III only
- C. III and IV only
- D. I and IV only

gate2020-cse computer-networks subnetting

Answer 

2.28.13 Subnetting: GATE IT 2004 | Question: 26 [top](#) 

<https://gateoverflow.in/3667>



A subnet has been assigned a subnet mask of 255.255.255.192. What is the maximum number of hosts that can belong to this subnet?

- A. 14
- B. 30
- C. 62
- D. 126

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gate2004-it computer-networks subnetting normal

Answer 

2.28.14 Subnetting: GATE IT 2005 | Question: 76 [top](#) 

<https://gateoverflow.in/3839>



A company has a class C network address of 204.204.204.0. It wishes to have three subnets, one with 100 hosts and two with 50 hosts each. Which one of the following options represents a feasible set of subnet address/subnet mask pairs?

- A. 204.204.204.128/255.255.255.192
204.204.204.0/255.255.255.128
204.204.204.64/255.255.255.128
- B. 204.204.204.0/255.255.255.192
204.204.204.192/255.255.255.128

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- 204.204.204.64/255.255.255.128
 C. 204.204.204.128/255.255.255.128
 204.204.204.192/255.255.255.192
 204.204.204.224/255.255.255.192
 D. 204.204.204.128/255.255.255.128
 204.204.204.64/255.255.255.192
 204.204.204.0/255.255.255.192

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gate2005-it computer-networks subnetting normal

Answer ↗

2.28.15 Subnetting: GATE IT 2006 | Question: 63, ISRO2015-57 top ↺



A router uses the following routing table:

Destination	Mask	Interface
144.16.0.0	255.255.0.0	eth0
144.16.64.0	255.255.224.0	eth1
144.16.68.0	255.255.255.0	eth2
144.16.68.64	255.255.255.224	eth3

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Packet bearing a destination address 144.16.68.117 arrives at the router. On which interface will it be forwarded?

- A. eth0
 B. eth1
 C. eth2
 D. eth3

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gate2006-it computer-networks subnetting normal isro2015

Answer ↗

2.28.16 Subnetting: GATE IT 2006 | Question: 70 top ↺



A subnetted Class B network has the following broadcast address: 144.16.95.255

Its subnet mask

- A. is necessarily 255.255.224.0
 B. is necessarily 255.255.240.0
 C. is necessarily 255.255.248.0
 D. could be any one of 255.255.224.0, 255.255.240.0, 255.255.248.0

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gate2006-it computer-networks subnetting normal

Answer ↗

2.28.17 Subnetting: GATE IT 2008 | Question: 84 top ↺



Host X has IP address 192.168.1.97 and is connected through two routers R1 and R2 to another host Y with IP address 192.168.1.80. Router R1 has IP addresses 192.168.1.135 and 192.168.1.110. R2 has IP addresses 192.168.1.67 and 192.168.1.155. The netmask used in the network is 255.255.255.224.

Given the information above, how many distinct subnets are guaranteed to already exist in the network?

- A. 1
 B. 2
 C. 3
 D. 6

gate2008-it computer-networks subnetting normal

Answer ↗



Host X has IP address 192.168.1.97 and is connected through two routers $R1$ and $R2$ to another host Y with IP address 192.168.1.80. Router $R1$ has IP addresses 192.168.1.135 and 192.168.1.110. $R2$ has IP addresses 192.168.1.67 and 192.168.1.155. The netmask used in the network is 255.255.255.224.

Which IP address should X configure its gateway as?

- A. 192.168.1.67
- B. 192.168.1.110
- C. 192.168.1.135
- D. 192.168.1.155

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[gate2008-it](#) [computer-networks](#) [subnetting](#) [normal](#)

[Answer](#)

Answers: Subnetting



- ✓ (A) and (C) are not the answers as the second byte of IP differs and subnet mask has 255 for second byte.

Consider (B), (& for bitwise AND)

$$10.35.28.2 \& 255.255.31.0 = 10.35.28.0 (28 = 11100_2)$$

$$10.35.29.4 \& 255.255.31.0 = 10.35.29.0 (29 = 11101_2)$$

So, we get different subnet numbers

Consider (D).

$$128.8.129.43 \& 255.255.31.0 = 128.8.1.0 (129 = 10000001_2)$$

$$128.8.161.55 \& 255.255.31.0 = 128.8.1.0 (161 = 10100001_2)$$

The subnet number matches. So, (D) is the answer.

113 votes

-- Arjun Suresh (332k points)



- ✓ The answer must be A.

(Using \wedge to denote bitwise AND)

For 1st packet,

$$(128.75.43.16) \wedge (255.255.255.0) = (128.75.43.0) \text{ since } \{16 \wedge 0 = 0\}, \text{ as well as}$$

$$(128.75.43.16) \wedge (255.255.255.128) = (128.75.43.0) \text{ since } \{16 \wedge 128 = 0\}.$$

Now, since both these subnet masks are producing the same Network ID, hence The one with greater number of ones will be selected, and the packet will be forwarded there. Hence packet 1 will be forwarded to Eth1.

For 2nd packet,

(192.12.17.10) when ANDed with each of the subnet masks does not match with any of the network ID, since:

$$(192.12.17.10) \wedge (255.255.255.0) = (192.12.17.0) \text{ \{Does not match with any of the network addresses\}}$$

$$(192.12.17.10) \wedge (255.255.255.128) = (192.12.17.0) \text{ \{Does not match with any of the network addresses\}}$$

$$(192.12.17.10) \wedge (255.255.255.255) = (192.12.17.10) \text{ \{Does not match with any of the network addresses\}}$$

Hence, default interface must be selected for packet 2, i.e., Interface Eth2.

57 votes

-- saurabhrk (1k points)



- ✓ D is correct answer.

To form subnet for 64 departments we need 6 continuous bit and the value of **11111100 = 252**.

Organization has class *B* network so subnet mask would be **255.255.252.0**

2.28.4 Subnetting: GATE CSE 2006 | Question: 45 top

https://gateoverflow.in/1821



- ✓ Subnetmask for C1 is 255.255.128.0. So, it finds the network ID as:

$$203.197.2.53 \text{ AND } 255.255.128.0 = 203.197.0.0$$
$$203.197.75.201 \text{ AND } 255.255.128.0 = 203.197.0.0$$

Both same.

Now subnetmask for C2 is 255.255.192.0. So, the respective network IDs are:

$$203.197.2.53 \text{ AND } 255.255.192.0 = 203.197.0.0$$
$$203.197.75.201 \text{ AND } 255.255.192.0 = 203.197.64.0$$

Both not same. So, option C.

51 votes

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-- Arjun Suresh (332k points)

2.28.5 Subnetting: GATE CSE 2007 | Question: 67, ISRO2016-72 top

https://gateoverflow.in/1265



In class B .. first 2 octet are reserved for NID and remaining for HID .. so first 6 bits of 3rd octet are used for subnet and remaining 10 bits for hosts ..

$$\text{Maximum number of subnets} = 2^6 - 2 = 62$$

Note that 2 is subtracted because subnet values consisting of all zeros and all ones (broadcast), reducing the number of available subnets by two in classic subnetting. In modern networks, we can have 64 as well. See here: <http://www.weird.com/~woods/classb.html>

$$\text{and no of hosts} = 2^{10} - 2 = 1022.$$

2 is subtracted for Number of hosts is also. The address with all bits as 1 is reserved as broadcast address and address with all host id bits as 0 is used as network address of subnet.

So option (C) is correct..

References



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57 votes

-- minal (13.1k points)

This question is asking **maximum no of subnets and hosts/subnet**...NOT **how many hosts are configurable**. So, no need to Subtract 2 in either case.

Subnet bits = 6

means 2^6 or 64 subnets are possible..

and, total hosts = 2^{10} or 1024 hosts..again no need to subtract 2 since question is asking maximum no of hosts possible not how much we can configure.

So, **option d should be right** according to what they mean by maximum.

EDIT:

This is becoming a very debatable question now....firstly whatever explanation i have given is right according to question formation...people are arguing that we should subtract 2 hosts from the available, for use..i agree..but this question was about maximum possible and one option also matched..so i gone with this...

Now what to do if something like this happens again in future?

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From all previous year questions over this topic it seems like we have to mind read them as what they actually mean...means for the gate questions **they are treating maximum possible hosts and available hosts all as same**....so go only according to that

else it would be very difficult to prove their thoughts wrong..

Now if asked **how many maximum subnets** we can use..**don't subtract anything**. This at least i can prove easily but mind it. **GATE still uses previous conventions of subtracting 2 subnets..atleast this is what shown here in 2007..**

If they ask **maximum hosts** or **configurable hosts**, anything. They actually wants us to subtract 2 from the hosts and then answer. **For gate questions i think English doesnt matter..u should answer according to the past experiences and questions they have asked.**

At last, for this question **maximum subnets are 64** and **hosts are 1022** is the actual answer but according to old conventions **62 and 1022**. So, go with.

Option C(closest). Choose wisely in the exam. I have explained each aspect of the question. I rest here and there should not be any more confusion regarding this!!

54 votes

-- Shobhit (13.5k points)

2.28.6 Subnetting: GATE CSE 2008 | Question: 57 [top](#)

<https://gateoverflow.in/480>



- ✓ a number of zeros are to be counted for calculating the total number of possible hosts per subnet.

$255-248 = 7$ can be represented using **3 bits**

these **3bits + 8bits more = 11 bits**

So, possible subnets $= 2^{11}$ out of these 2 are reserved as subnet **ID** and **DBA**

Therefore, we have maximum possible usable hosts $= 2^{11} - 2 = 2046$

Correct Answer: **C**

35 votes

-- Amar Vashishth (25.2k points)

2.28.7 Subnetting: GATE CSE 2010 | Question: 47 [top](#)

<https://gateoverflow.in/2349>



- ✓ **D** is correct answer because:

When we perform **AND** operation between **IP address 10.105.1.113** and **255.255.255.224** result is **10.105.1.96**

When we perform **AND** operation between **IP address 10.105.1.91** and **255.255.255.224** result is **10.105.1.64**

10.105.1.96 and **10.105.1.64** are different network so **D** is correct answer.

37 votes

-- R.B. Tiwari (257 points)

2.28.8 Subnetting: GATE CSE 2012 | Question: 34, ISRO-DEC2017-32 [top](#)

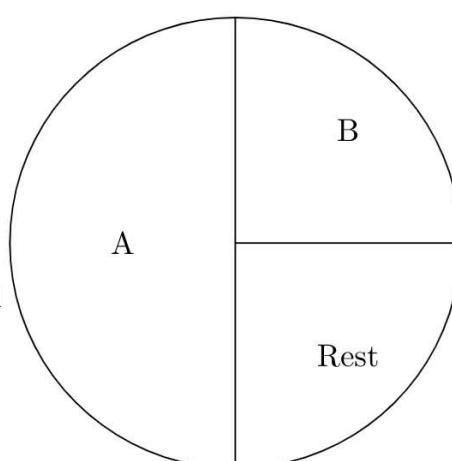
<https://gateoverflow.in/1752>



class

A
254.248.136.0/21
To
254.248.143.255/21

class



B
254.248.128.0/22
To
254.248.131.255/22

Rest
254.248.132.0/22
To
254.248.135.255/22

Correct option will be A

44 votes

-- Ashish Patel (297 points)

2.28.9 Subnetting: GATE CSE 2015 Set 2 | Question: 41 top

<https://gateoverflow.in/829>



✓ **Taking the 1st IP Address: 128.96.171.92**

Bitwise AND between 128.96.171.92 and 255.255.254.0 we get the subnet ID as follows:

255	255	11111110	0
128	96	10101011	92
128	96	10101010	0

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∴ Subnet ID = 128.96.170.0

∴ 128.96.171.92 will forward to interface 0

Taking the 2nd IP Address: 128.96.167.151

Bitwise AND between 128.96.167.151 and 255.255.254.0 we get,

255	255	11111110	0
128	96	10100111	151
128	96	10100110	0

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∴ Subnet ID = 128.96.166.0

∴ 128.96.167.151 will forward to interface R2

Taking the 3rd IP Address: 128.96.163.151

Bitwise AND between 128.96.167.151 and 255.255.254.0 we get,

255	255	11111110	0
128	96	10100011	151
128	96	10100010	0

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∴ Subnet ID = 128.96.162.0 (Doesn't match with any given interface)

Now, Bitwise AND between 128.96.167.151 and 255.255.252.0 we get,

255	255	11111100	0
128	96	10100011	151
128	96	10100000	0

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∴ Subnet ID = 128.96.160.0 (Doesn't match with any given interface)

∴ 128.96.163.151 will forward to default interface R4

Taking the last IP Address: 128.96.164.121

Bitwise AND between 128.96.164.121 and 255.255.254.0 we get,

255	255	11111110	0
128	96	10100100	121
128	96	10100100	0

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∴ Subnet ID = 128.96.164.0

∴ 128.96.167.151 will forward to interface R3

∴ Option (a) is the correct answer

16 votes

-- Pritha Majumder (487 points)

2.28.10 Subnetting: GATE CSE 2015 Set 3 | Question: 38 top

<https://gateoverflow.in/849>



✓ Answer= 158

144 in binary = 10010000

out of this 3 bits in left are subnet bits. (27 bits are used for subnet, which means top 3 bytes and leftmost 3 bits from the last byte)

So, the 4th octet in the last IP address of the network which can be assigned to a host is 10011110. (its not 10011111 because its network broadcast address)

So, 10011110 is 158 in decimal.

1 like 66 votes

-- overtomana (945 points)

2.28.11 Subnetting: GATE CSE 2019 | Question: 28 [top](#)

<https://gateoverflow.in/302820>



- ✓ First derive the network address of those machines, then we can decide !

Finding network address for a M/C :- Perform Bitwise AND between m/c address and given subnet mask.

Subnet Mask: keep 1's in Network part + subnet part and keep 0's in Host part.

$255.255.255.252 = 11111111.11111111.11111111.11111100$
= 24(from first 3 octets) + 6(in last octet)
= 30bits in Network+ subnet portion and last 2 bits represent the Host part.

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Subnet Mask = 255.255.255.252 and $M = 100.10.5.2$ but keep all zero's in HOST part !

100 = 01100100	10 = 00001010	5 = 00000101	2 = 00000000
255 = 11111111	255 = 11111111	255 = 11111111	252 = 11111100
100	10	5	0

Subnet Mask = 255.255.255.252 and $N = 100.10.5.5$ but keep all zero's in HOST part !

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100 = 01100100	10 = 00001010	5 = 00000101	5 = 00000100
255 = 11111111	255 = 11111111	255 = 11111111	252 = 11111100
100	10	5	4

Subnet Mask = 255.255.255.252 and $P = 100.10.5.6$ but keep all zero's in HOST part !

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100 = 01100100	10 = 00001010	5 = 00000101	6 = 00000100
255 = 11111111	255 = 11111111	255 = 11111111	252 = 11111100
100	10	5	4

.: only N and P are belong to same network (100.10.5.4/30)

1 like 20 votes

-- Shaik Masthan (50.4k points)

2.28.12 Subnetting: GATE CSE 2020 | Question: 38 [top](#)

<https://gateoverflow.in/333193>



- ✓ (B) II and III only

Given IP address space: 202.61.0.0/17, 17 bits are in network ID bits(NID) and rest will be host ID bits(HID).

$\underbrace{202.61}_{17 \text{ NID bits}}.\underbrace{0.0.0}_{4 \text{ SID bits}}.\underbrace{0.0.0.0}_{11 \text{ HID bits}}$

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In order to assign 1500 hosts we need minimum 11 bits

$\underbrace{202.61.0}_{17 \text{ NID bits}}.\underbrace{0.0.0}_{4 \text{ SID bits}}.\underbrace{0.0.0.0}_{11 \text{ HID bits}}$

We have 4 subnet bits, eligible networks are those which belongs among possible 16 subnets.

If we expand the given Network bits we can see:

- $202.61.84.0/21 = 202.61.0\mathbf{1}0\mathbf{1}0100.0$

- Not possible as all Host Bits should be zero
- $202.61.104.0/21 = 202.61.01101000.0$
 - $202.61.64.0/21 = 202.61.01000000.0$
Possible
 - $202.61.144.0/21 = 202.61.10010000.0$
Not possible as 16th bit from right (part of NID is 0 and not 1)

30 votes

-- Ashwani Kumar (13k points)

2.28.13 Subnetting: GATE IT 2004 | Question: 26 top

<https://gateoverflow.in/3667>



- ✓ (C) is answer since you have 6 zeroes so you can make $64 - 2$ hosts

25 votes

-- Shreyans Dhankhar (2.1k points)

2.28.14 Subnetting: GATE IT 2005 | Question: 76 top

<https://gateoverflow.in/3839>



- ✓ classroom.gateoverflow.in
Answer is D.

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MSB in last 8 bits helps us to get two subnets

- 10000000 → subnet1
- 00000000 → subnet2

subnet2 is divided into 2 more subnets using 7th bit

- 00000000 → subnet2(0)
- 01000000 → subnet2(1)

29 votes

-- nagalla pruthvi (675 points)

2.28.15 Subnetting: GATE IT 2006 | Question: 63, ISRO2015-57 top

<https://gateoverflow.in/3607>



- ✓ Firstly start with **Longest mask**

~~144.16.68.117~~ = 144.16.68.01110101 AND gateoverflow.in

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255.255.255.224 = 255.255.255.11100000

= 144.16.68.96 (**Not matching with Destination**)

Now, take 255.255.255.0

144.16.68.117 AND 255.255.255.0 = 144.16.68.0 (**matched**)

So, interface chosen is **eth2 OPTION (C)**.

54 votes

-- Himanshu Agarwal (12.4k points)

2.28.16 Subnetting: GATE IT 2006 | Question: 70 top

<https://gateoverflow.in/3614>



- ✓ Option (D) is correct. In the broadcast address for a subnet, all the host bits are set to 1. So as long as all the bits to the right are 1, bits left to it can be taken as possible subnet.

Broadcast address for subnet is .95.255 .01011111.11111111 (as in Class B, 16 bits each are used for network and host)

So, we can take minimum 3 bits (from left) as subnet and make rest as host bits(as they are 1).

.224.0 11100000.00000000 (leftmost 3 bits for subnet)

.240.0 11110000.00000000 (leftmost 4 bits for subnet)

.248.0 11111000.00000000 (... 5 bits for subnet)

50 votes

-- Sandeep_Uniyal (6.5k points)

2.28.17 Subnetting: GATE IT 2008 | Question: 84 [top](#)

<https://gateoverflow.in/3408>



- ✓ $255.255.255.224 = 11111111.11111111.11111111.11100000$

192.168.1.97
192.168.1.80
192.168.1.135
192.168.1.110
192.168.1.67
192.168.1.155

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We need to do bitwise AND with subnet mask.
the last 5 bits are going to be 0 when ANDED.

No need to waste time in finding binary.
Only focus on 1st 3 bits of binary.

(From left side, 1st bit is 128,next one is 64,next one is 32..it goes like that you know.)

97: $0 + 64 + 32 + \text{something}$ so 1st 3 bits will contain 011
80: $0 + 64 + 0 + \text{something}$ so 010
135: $128 + 0 + 0 + \text{something}$ so 100
110: $0 + 64 + 32 + \text{something}$ so 011
67: $0 + 64 + 0 + \text{something}$ so 010
155: $128 + 0 + 0 + \text{something}$ so 100

So we got 011, 010, 100
3 subnets.... subnet id are...

192.168.1.96
192.168.1.64
192.168.1.128

Correct Answer: C

51 votes

-- Ahwan Mishra (10.2k points)

2.28.18 Subnetting: GATE IT 2008 | Question: 85 [top](#)

<https://gateoverflow.in/3409>



- ✓ X must be able to reach the gateway using the net mask.
Subnet number of host $X = 192.168.1.97 \& 255.255.255.224 = 192.168.1.96$

Now, the gateway must also have the same subnet number. Lets take IP 192.168.1.110 of R1. 192.168.1.110 & 255.255.255.224 = 192.168.1.96 and hence this can be used by X .

(To quickly identify the matching mask divide the last part of mask (224 here) into powers of 2. So, $224 = 128 + 64 + 32$. Now, our host X has 97 as the last part of IP = $64 + 32 + 1$. So, the last part of subnet number becomes $64 + 32 = 96$. Now, we need to consider only those IPs whose last part will contain 64 as well as 32)

http://courses.washington.edu/css432/joemcc/slides/03_cidr.ppt

Correct Answer: B

References



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58 votes

-- Arjun Suresh (332k points)

2.29

Tcp (17) [top](#)



While opening a *TCP* connection, the initial sequence number is to be derived using a time-of-day (ToD) clock that keeps running even when the host is down. The low order 32 bits of the counter of the ToD clock is to be used for the initial sequence numbers. The clock counter increments once per milliseconds. The maximum packet lifetime is given to be 64s.

Which one of the choices given below is closest to the minimum permissible rate at which sequence numbers used for packets of a connection can increase?

- A. 0.015/s
- B. 0.064/s
- C. 0.135/s
- D. 0.327/s

[gate2009-cse](#) [computer-networks](#) [tcp](#) [difficult](#) [ambiguous](#)

[Answer](#)

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Which of the following transport layer protocols is used to support electronic mail?

- A. SMTP
- B. IP
- C. TCP
- D. UDP

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[Answer](#)



Suppose two hosts use a TCP connection to transfer a large file . Which of the following statements is/are FALSE with respect to the TCP connection?

- I. If the sequence number of a segment is m, then the sequence number of the subsequent segment is always m+1.
 - II. If the estimated round trip time at any given point of time is t sec, the value of the retransmission timeout is always set to greater than or equal to t sec.
 - III. The size of the advertised window never changes during the course of the TCP connection.
 - IV. The number of unacknowledged bytes at the sender is always less than or equal to the advertised window.
- A. III only
 - B. I and III only
 - C. I and IV only
 - D. II and IV only

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[gate2015-cse-set1](#) [computer-networks](#) [tcp](#) [normal](#)

[Answer](#)



Assume that the bandwidth for a *TCP* connection is 1048560 bits/sec. Let α be the value of RTT in milliseconds (rounded off to the nearest integer) after which the *TCP* window scale option is needed. Let β be the maximum possible window size with window scale option. Then the values of α and β are

- A. 63 milliseconds, 65535×2^{14}
- B. 63 milliseconds, 65535×2^{16}
- C. 500 milliseconds, 65535×2^{14}
- D. 500 milliseconds, 65535×2^{16}

[gate2015-cse-set2](#) [computer-networks](#) [difficult](#) [tcp](#)

[Answer](#)

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Consider the following statements.

- I. TCP connections are full duplex
 - II. TCP has no option for selective acknowledgement
 - III. TCP connections are message streams
- A. Only I is correct
 B. Only I and III are correct
 C. Only II and III are correct
 D. All of I, II and III are correct

[gate2015-cse-set3](#) [computer-networks](#) [tcp](#) [normal](#)

[Answer](#)

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Identify the correct sequence in which the following packets are transmitted on the network by a host when a browser requests a webpage from a remote server, assuming that the host has just been restarted.

- A. HTTP GET request, DNS query, TCP SYN
- B. DNS query, HTTP GET request, TCP SYN
- C. DNS query, TCP SYN, HTTP GET request.
- D. TCP SYN, DNS query, HTTP GET request.

[gate2016-cse-set2](#) [computer-networks](#) [normal](#) [tcp](#)

[Answer](#)

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Consider a TCP client and a TCP server running on two different machines. After completing data transfer, the TCP client calls close to terminate the connection and a FIN segment is sent to the TCP server. Server-side TCP responds by sending an ACK, which is received by the client-side TCP. As per the TCP connection state diagram (*RFC 793*), in which state does the client-side TCP connection wait for the FIN from the server-side TCP?

- A. LAST-ACK
- B. TIME-WAIT
- C. FIN-WAIT-1
- D. FIN-WAIT-2

[gate2017-cse-set1](#) [computer-networks](#) [tcp](#)

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[Answer](#)



Consider a long-lived *TCP* session with an end-to-end bandwidth of 1 Gbps (10^9 bits-per-second). The session starts with a sequence number of 1234. The minimum time (in seconds, rounded to the closest integer) before this sequence number can be used again is _____

[gate2018-cse](#) [computer-networks](#) [tcp](#) [normal](#) [numerical-answers](#)

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[Answer](#)



Consider a *TCP* connection between a client and a server with the following specifications; the round trip time is 6 ms, the size of the receiver advertised window is 50 KB, slow-start threshold at the client is 32 KB, and the maximum segment size is 2 KB. The connection is established at time $t = 0$. Assume that there are no timeouts and errors during transmission. Then the size of the congestion window (in KB) at time $t + 60$ ms after all acknowledgements are processed is _____

[gate2020-cse](#) [numerical-answers](#) [computer-networks](#) [tcp](#)

Answer ↗

2.29.10 Tcp: GATE CSE 2021 Set 1 | Question: 44 [top ↵](#)

↗ <https://gateoverflow.in/357407>



A TCP server application is programmed to listen on port number P on host S . A TCP client is connected to the TCP server over the network.

Consider that while the TCP connection was active, the server machine S crashed and rebooted. Assume that the client does not use the TCP keepalive timer. Which of the following behaviors is/are possible?

- A. If the client was waiting to receive a packet, it may wait indefinitely
- B. The TCP server application on S can listen on P after reboot
- C. If the client sends a packet after the server reboot, it will receive a RST segment
- D. If the client sends a packet after the server reboot, it will receive a FIN segment

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[gate2021-cse-set1](#) [multiple-selects](#) [computer-networks](#) [tcp](#)

Answer ↗

2.29.11 Tcp: GATE CSE 2021 Set 1 | Question: 45 [top ↵](#)

↗ <https://gateoverflow.in/357406>



Consider two hosts P and Q connected through a router R . The maximum transfer unit (MTU) value of the link between P and R is 1500 bytes, and between R and Q is 820 bytes.

A TCP segment of size 1400 bytes was transferred from P to Q through R , with IP identification value as 0x1234. Assume that the IP header size is 20 bytes. Further, the packet is allowed to be fragmented, i.e., Don't Fragment (DF) flag in the IP header is not set by P .

Which of the following statements is/are correct?

- A. Two fragments are created at R and the IP datagram size carrying the second fragment is 620 bytes.
- B. If the second fragment is lost, R will resend the fragment with the IP identification value 0x1234.
- C. If the second fragment is lost, P is required to resend the whole TCP segment.
- D. TCP destination port can be determined by analysing *only* the second fragment.

[gate2021-cse-set1](#) [computer-networks](#) [tcp](#)

Answer ↗

2.29.12 Tcp: GATE CSE 2021 Set 2 | Question: 7 [top ↵](#)

↗ <https://gateoverflow.in/357533>



Consider the three-way handshake mechanism followed during TCP connection establishment between hosts P and Q . Let X and Y be two random 32-bit starting sequence numbers chosen by P and Q respectively. Suppose P sends a TCP connection request message to Q with a TCP segment having SYN bit = 1, SEQ number = X , and ACK bit = 0. Suppose Q accepts the connection request. Which one of the following choices represents the information present in the TCP segment header that is sent by Q to P ?

- A. SYN bit = 1, SEQ number = $X + 1$, ACK bit = 0, ACK number = Y , FIN bit = 0
- B. SYN bit = 0, SEQ number = $X + 1$, ACK bit = 0, ACK number = Y , FIN bit = 1
- C. SYN bit = 1, SEQ number = Y , ACK bit = 1, ACK number = $X + 1$, FIN bit = 0
- D. SYN bit = 1, SEQ number = Y , ACK bit = 1, ACK number = X , FIN bit = 0

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[gate2021-cse-set2](#) [computer-networks](#) [tcp](#)

Answer ↗

2.29.13 Tcp: GATE IT 2004 | Question: 23 [top ↵](#)

↗ <https://gateoverflow.in/3664>



Which one of the following statements is FALSE?

- A. TCP guarantees a minimum communication rate
- B. TCP ensures in-order delivery
- C. TCP reacts to congestion by reducing sender window size
- D. TCP employs retransmission to compensate for packet loss

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Answer**2.29.14 Tcp: GATE IT 2004 | Question: 28**<https://gateoverflow.in/3669>

In TCP, a unique sequence number is assigned to each

- A. byte
- B. word
- C. segment
- D. message

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Answer**2.29.15 Tcp: GATE IT 2007 | Question: 13**<https://gateoverflow.in/3446>

Consider the following statements about the timeout value used in TCP.

- i. The timeout value is set to the RTT (Round Trip Time) measured during TCP connection establishment for the entire duration of the connection.
- ii. Appropriate RTT estimation algorithm is used to set the timeout value of a TCP connection.
- iii. Timeout value is set to twice the propagation delay from the sender to the receiver.

Which of the following choices hold?

- A. (i) is false, but (ii) and (iii) are true
- B. (i) and (iii) are false, but (ii) is true
- C. (i) and (ii) are false, but (iii) is true
- D. (i), (ii) and (iii) are false

Answer**2.29.16 Tcp: GATE IT 2007 | Question: 14**<https://gateoverflow.in/3447>

Consider a *TCP* connection in a state where there are no outstanding *ACKs*. The sender sends two segments back to back. The sequence numbers of the first and second segments are 230 and 290 respectively. The first segment was lost, but the second segment was received correctly by the receiver. Let X be the amount of data carried in the first segment (in bytes), and Y be the *ACK* number sent by the receiver.

The values of X and Y (in that order) are

- A. 60 and 290
- B. 230 and 291
- C. 60 and 231
- D. 60 and 230

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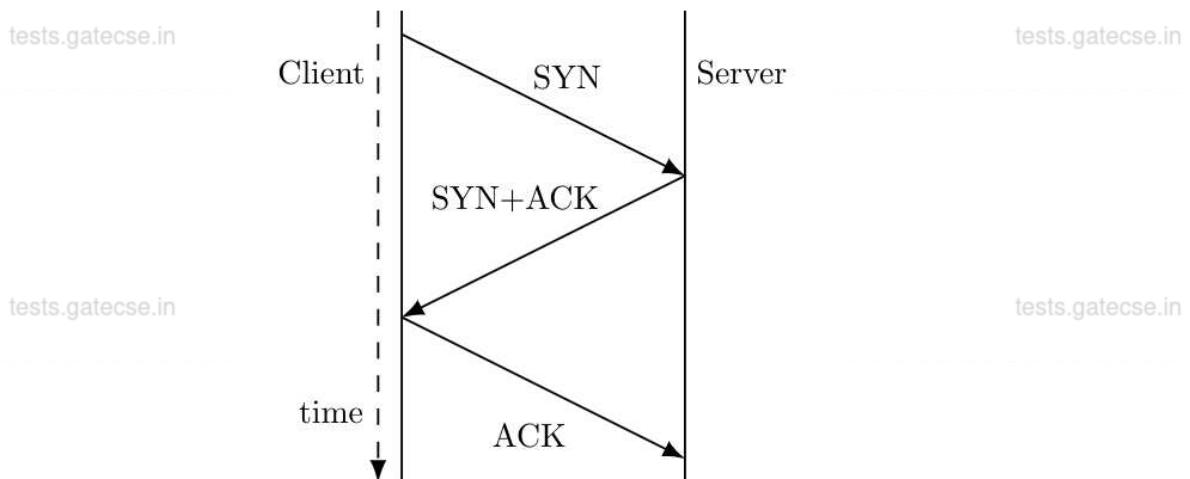
Answer**2.29.17 Tcp: GATE IT 2008 | Question: 69**<https://gateoverflow.in/3383>

The three way handshake for TCP connection establishment is shown below.

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Which of the following statements are TRUE?

- S1 : Loss of SYN + ACK from the server will not establish a connection
 - S2 : Loss of ACK from the client cannot establish the connection
 - S3 : The server moves LISTEN → SYN_RCVD → SYN_SENT → ESTABLISHED in the state machine on no packet loss
 - S4 : The server moves LISTEN → SYN_RCVD → ESTABLISHED in the state machine on no packet loss
- A. S2 and S3 only
B. S1 and S4 only
C. S1 and S3 only
D. S2 and S4 only

[gate2008-it](#) [computer-networks](#) [tcp](#) [normal](#)

[goclasses.in](#)

[tests.gatecse.in](#)

[Answer](#)

Answers: Tep



2.29.1 Tcp: GATE CSE 2009 | Question: 47 [top](#)

<https://gateoverflow.in/1333>

- ✓ One of the very rare ambiguous question in GATE. It is ambiguous what the question asks for

! minimum permissible rate at which sequence numbers used for packets of a connection can increase

It is not meaningful to use "minimum" with "can increase" - should be either "maximum" with "can" or "minimum" with "should/must"

Now the second problem,

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! rate at which sequence numbers used for packets of a connection

In TCP, once the Initial Sequence Number(ISN) is set, the increase in sequence number is determined by the data sent rate - for every 8 bits, it increases by 1. If the question is asking for this rate, then it is independent of the ISN and depends on the packet lifetime and number of possible sequence numbers. With 32 bits we have 2^{32} sequence numbers possible and to avoid using the same sequence number while a packet with one is still alive, we should ensure no more than 2^{32} sequence numbers in a packet lifetime which is given as 64s. So, maximum increase possible for sequence number will be 2^{32} in 64s which will be $2^{26}/s = 64M/s$ corresponding to a data rate of $64 \times 8 = 512Mbps$. This is not in the option.

Now the other possible meaning of the question is the rate at which the ISN of a packet can increase. This problem comes when a connection gets aborted and re-established (i.e., same IP and Port addresses at sender and receiver) very soon. In this case, receiver might get confused if it gets any sequence number which might have been used by the old connection. To, avoid this the new sequence number must be used only after all previous ones are dead. i.e., only after Maximum Life time of a packet which is 64s. ([Page 29, TCP Specification](#)) This ensure that ISN can change only once in 64s giving the rate change as $1/64 = 0.015/s$ which is option A. (Even though, the ISN is changing only once, as per the question the new ISN is not old ISN +1 but old ISN + time passed in milliseconds)

Option A.

References



48 votes

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-- Arjun Suresh (332k points)

2.29.2 Tcp: GATE CSE 2012 | Question: 22 [top](#)

<https://gateoverflow.in/1605>



- ✓ Answer is option C: TCP.

There are three primary TCP/IP protocols for E-Mail management:

- Post Office Protocol (POP)
- Simple Mail Transfer Protocol (SMTP)
- Internet Message Access Protocol (IMAP)

They all are Application Layer Protocols

Once a client connects to the E-mail Server, there may be 0(zero) or more SMTP transactions. If the client has no mail to send, then there are no SMTP transactions. Every e-mail message sent is an SMTP transfer.

SMTP is only used to send (push) messages to the server. POP and IMAP are used to receive messages as well as manage the mailbox contents(which includes tasks such as deleting, moving messages etc.).

44 votes

-- Amar Vashishth (25.2k points)

2.29.3 Tcp: GATE CSE 2015 Set 1 | Question: 19 [top](#)

<https://gateoverflow.in/8217>



- ✓ Option B

III. False. It is the size of the receiver's buffer that's never changed. RcvWindow is the part of the receiver's buffer that's changing all the time depending on the processing capability at the receiver's side and the network traffic.

http://web.eecs.utk.edu/~qi/teaching/ece453f06/hw/hw7_sol.htm

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References



31 votes

-- GATERush (917 points)

2.29.4 Tcp: GATE CSE 2015 Set 2 | Question: 34 [top](#)

<https://gateoverflow.in/8154>



- ✓ In TCP when the **bandwidth delay product** increases beyond 64K receiver window scaling is needed.

The bandwidth delay product is the maximum amount of data on the network circuit at any time and is measured as RTT * Bandwidth. This is not the time for sending data rather just the time for sending data without acknowledgement.

So, here, we have bandwidth delay product = $(1048560 / 8) B * \alpha = 64 K$
 $\alpha = (64 K * 8) / 1048560 = 0.5$ s = 500 milliseconds.

When window scaling happens, a 14 bit shift count is used in *TCP* header. So, the maximum possible window size gets increased from $2^{16}-1$ to $(2^{16}-1) * 2^{14}$ or from 65535 to $65535 * 2^{14}$

http://en.wikipedia.org/wiki/TCP_window_scale_option

References

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thumb up 87 votes

-- Arjun Suresh (332k points)

2.29.5 Tep: GATE CSE 2015 Set 3 | Question: 22 top ↗

↗ <https://gateoverflow.in/8425>



- ✓ Answer is (A). Since, TCP has options for selective ACK and TCP uses byte streams that is every byte that is send using TCP is numbered.

http://repo.hackerzvoice.net/depot_madchat/ebooks/TCP-IP_Illustrated/tcp_tran.htm or [archive](#)

References



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thumb up 38 votes

-- Tamojit Chatterjee (1.9k points)

2.29.6 Tep: GATE CSE 2016 Set 2 | Question: 25 top ↗

↗ <https://gateoverflow.in/39572>



- ✓ Here,

C) Seems correct answer.

Say you type www.google.com

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First you send DNS request to get IP address. Then you establish connection with IP of google using TCP. Finally you start talking in HTTP !

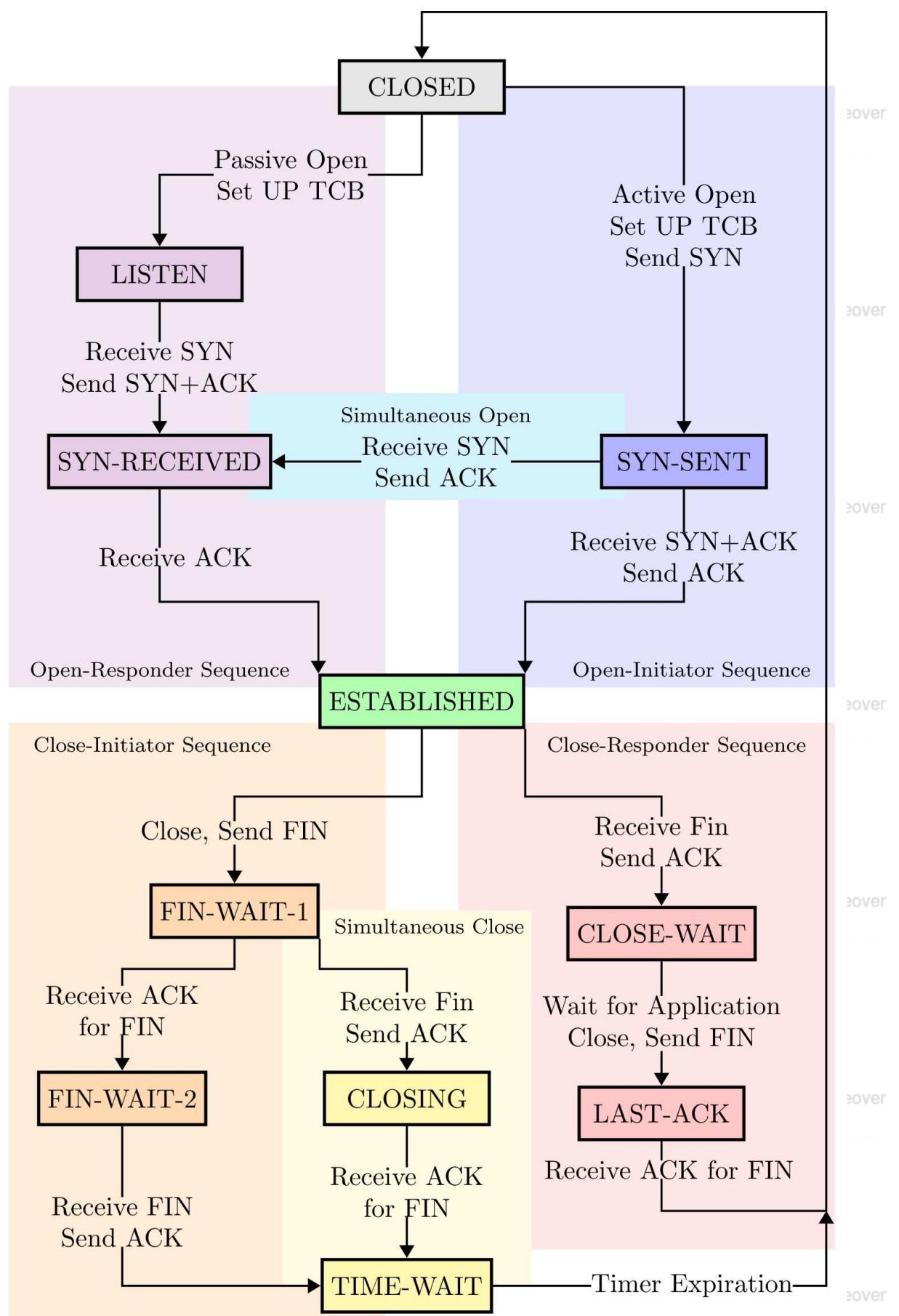
thumb up 62 votes

-- Akash Kanase (36k points)

2.29.7 Tep: GATE CSE 2017 Set 1 | Question: 14 top ↗

↗ <https://gateoverflow.in/118194>





Close Initiator Represents the agent which first sent the request for closing the connection when previously it was in established

state(Usually client).

Close Responder represents the agent which responds to FIN Segments(Usually the server).

Now, as we see in the diagram,

When the client sends the FIN segment to server,it moves to FIN-WAIT1 state where it waits for an Acknowledgement from the server for its own FIN segment.

Now when the client receives ACK for its OWN FIN Segment, it moves to FIN-WAIT2. This state represents that the connection from client to server has been terminated but still the connection from server to client is open.(TCP supports full duplex connections).

Hence, answer is D.

Reference:

[1] http://tcpipguide.com/free/t_TCPOperationalOverviewandtheTCPFiniteStateMachineF-2.htm

References



39 votes

-- Ayush Upadhyaya (28.4k points)

2.29.8 Tcp: GATE CSE 2018 | Question: 25 top

<https://gateoverflow.in/204099>



- ✓ in another words qsn is asking to find Wrap-around time

$$T_{\text{minimum}} = T_{\text{wrap-around}} = \frac{2^{32} \times 8}{10^9} = 34.35s$$

rounding to closest integer, we will get **34**

Note: Answer has been Modified in the Final Answer Key from GATE officials and now it is in Range from 34 to 35.

39 votes

-- NITISH JOSHI (24.4k points)

2.29.9 Tcp: GATE CSE 2020 | Question: 55 top

<https://gateoverflow.in/333176>



- ✓ In Case of AIMD :-

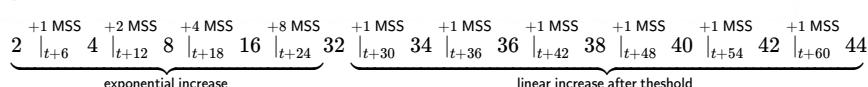
1. Start with Given MSS (Min Seq Size)
2. Increase the Window size in multiples of MSS till the threshold occurs
3. Once the threshold reached , increase the window size by 1 MSS till the timeout occurs
4. Once the timeout occurs , reduce threshold to half of current window size and again start from Given Start MSS.

$t = 0$

$1 \text{ MSS} = 2 \text{ KB}$

$W_{\text{threshold}} = 32 \text{ KB}$

| → denotes 1 RTT



∴ The size of the congestion window(in KB) at time $t + 60$ ms after all acknowledgements are processed is 44 KB

5 votes

-- Satbir Singh (21k points)

The state of congestion window changes as below

Note : As specified in question, there are no errors and timeouts

- At $t : 1 \text{ MSS}$

- At $t + 6$: 2 MSS
- At $t + 12$: 4 MSS
- At $t + 18$: 8 MSS
- At $t + 24$: 16 MSS

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Now here since threshold value is reached, it is no longer in slow start phase and enters congestion avoidance phase

- At $t + 30$: 17 MSS
- At $t + 36$: 18 MSS
- At $t + 42$: 19 MSS
- At $t + 48$: 20 MSS
- At $t + 54$: 21 MSS
- At $t + 60$: 22 MSS

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So at time $t + 60$, the congestion window size is 22 MSS i.e., 44 KB.

14 votes

-- NabilSayyad (761 points)

2.29.10 Tcp: GATE CSE 2021 Set 1 | Question: 44 top ↗

↗ <https://gateoverflow.in/357407>



Option A is correct, because client doesn't have a keepalive timer, and the server after a reboot forgets any connection with the client existed.

As for option C and D, option D is wrong because there is no reason for a FIN segment to be sent because there is no established connection which can be closed **according to the recently rebooted server**.

As for option C, scroll down to read the paragraph from page 35*** of the documentation, which proves that it is in fact correct.

Now, for option B, during the exam i reasoned that there is a distinction between a server machine being rebooted, and a tcp application/process being restarted.

For instance, whenever your computer crashes and reboots when you were browsing on google chrome (this was the case atleast a few years ago), did your computer automatically also restart the google chrome application? Obviously not.

There are some processes which the computer automatically starts on boot, **but those are the exceptions and not the norm**.

A client or server won't simply restart its previous processes after a crash and reboot, **unless it has been configured** to do so, and nowhere in the question do i see that the server was a dedicated server running only the said tcp application.

The question asks what **behaviour** is possible on reboot. When such wording is used, it is natural to assume that it means what happens after the reboot **without any external interference**, human or otherwise. Because if we don't assume this to be true, then a whole lot of things are possible after a system restarts.

Here is some supporting text from the standard tcp documentation which you can access following this: Wikipedia
→ Transmission Control Protocol → RFC Documents → [STD 7](#) - Transmission Control Protocol, Protocol specification
(<https://tools.ietf.org/html/std7>) → Page 32 → Half-Open Connections and Other Anomalies.

An established connection is said to be "half-open" if one of the TCPs has closed or aborted the connection at its end without the knowledge of the other, or if the two ends of the connection have become desynchronized owing to a crash that resulted in loss of memory. Such connections will automatically become reset if an attempt is made to send data in either direction. However, half-open connections are expected to be unusual, and the recovery procedure is mildly involved.

If at site A the connection no longer exists, then an attempt by the user at site B to send any data on it will result in the site B TCP receiving a reset control message. Such a message indicates to the site B TCP that something is wrong, and it is expected to abort the connection.

Assume that two user processes A and B are communicating with one another when a crash occurs causing loss of memory to A's TCP. **Depending on the operating system** supporting A's TCP, it is **likely** that some error recovery mechanism exists. **When the TCP is up again**, A is **likely** to start again from the beginning **or** from a **recovery point**. As a result, A **will probably try** to OPEN the connection again or try to SEND on the connection it believes open. In the latter case, it receives the error message "connection not open" from the local (A's) TCP. In an attempt to establish the connection, A's TCP will send a segment containing SYN. This scenario leads to the example shown in figure 10.

The highlighted words indicate that **it isn't always necessary** that the tcp process will restart after a crash, and that it is

dependent upon the operating system.

Given that we don't know what the TCP process is exactly, it could as well be an unimportant process on a non well-known port, which was used for a private connection between the client and the server, which has no specific reason to restart after the server reboots.

And until and unless the process restarts, it won't start listening on its configured port number.

***Also on Page 35 →

Reset Generation

As a general rule, reset (RST) must be sent whenever a segment arrives which apparently is not intended for the current connection. A reset must not be sent if it is not clear that this is the case.

References



4 votes

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-- Rishabh Gupta (511 points)

2.29.11 TcP: GATE CSE 2021 Set 1 | Question: 45 top

<https://gateoverflow.in/357406>



- ✓ A is correct as you can follow the process of IPv4 fragmentation and you will get 620B fragments as described in the statement.

C is correct as fragmentation happened at the router and the sender has no way of knowing what kind of fragmentation occurred, so it will resend the whole TCP segment.

For B to be true, the original sender must retransmit the packet data in a datagram with the *same* IPv4 ID field as before, i.e. 0X1234. Take a look at [RFC 1122](#) to see what they say about retransmitting with the same ID field (text below).

First of all, it says that retaining the ID field is optional. Secondly, it says that due to certain constraints, this is not practical, and therefore not believed to be useful (so it does not really happen in practice).

B's statement implies that the router will definitely resend a fragment with 0X1234 ID, which can only happen if the sender resends the whole segment with the same ID number, but there is no such guarantee. Therefore B is **false**.

When sending an identical copy of an earlier datagram, a host **MAY** optionally retain the same Identification field in the copy.

Some Internet protocol experts have maintained that when a host sends an identical copy of an earlier datagram, the new copy should contain the same Identification value as the original. There are two suggested advantages: (1) if the datagrams are fragmented and some of the fragments are lost, the receiver may be able to reconstruct a complete datagram from fragments of the original and the copies; (2) a congested gateway might use the IP Identification field (and Fragment Offset) to discard duplicate datagrams from the queue.

However, the observed patterns of datagram loss in the Internet do not favor the probability of retransmitted fragments filling reassembly gaps, while other mechanisms (e.g., TCP repacketizing upon retransmission) tend to prevent retransmission of an identical datagram [IP:9]. Therefore, **we believe that retransmitting the same Identification field is not useful.**

References



7 votes

-- Prithish C (2k points)

2.29.12 Tcp: GATE CSE 2021 Set 2 | Question: 7 [top](#)

<https://gateoverflow.in/357533>



- ✓ Host P sends the first SYN packet with SEQ number = X , SYN flag = 1 and ACK flag = 0 as it's a connection request.

Host Q will reply back with a SYN packet and acknowledging the arrival of P' s SYN packet.

Host Q will send a packet with

SYN flag =1,

SEQ number = Y , to synchronize and establish the connection,

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ACK flag = 1 to acknowledge the P' s SYN packet, with

ACK number = X+1 because ACK number denotes the sequence number of next expecting Byte.

Then P will reply back with an ACK packet to complete the three-way handshake. (not asked here)

FIN flag is used to terminate the connection, and will not be used here, **FIN flag = 0**.

Hence **C is correct**.

2 votes

-- Nikhil Dhama (2.5k points)

2.29.13 Tcp: GATE IT 2004 | Question: 23 [top](#)

<https://gateoverflow.in/3664>



- ✓ Option B: "Sequence numbers allow receivers to discard duplicate packets and properly sequence reordered packets."
- Option C: "When congestion is detected, the transmitter decreases the transmission rate by a multiplicative factor; for example, cut the congestion window in half after loss." (Additive Increase/multiplicative decrease)
- Option D: "Acknowledgments allow senders to determine when to retransmit lost packets."

So, **(A)** is answer.

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http://en.wikipedia.org/wiki/Transmission_Control_Protocol#Error_detection

http://en.wikipedia.org/wiki/Additive_increase/multiplicative_decrease

References



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27 votes

-- Arjun Suresh (332k points)

2.29.14 Tcp: GATE IT 2004 | Question: 28 [top](#)

<https://gateoverflow.in/3669>



- ✓ a) it should be byte

http://www.industrialethernetu.com/courses/202_2.htm

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References

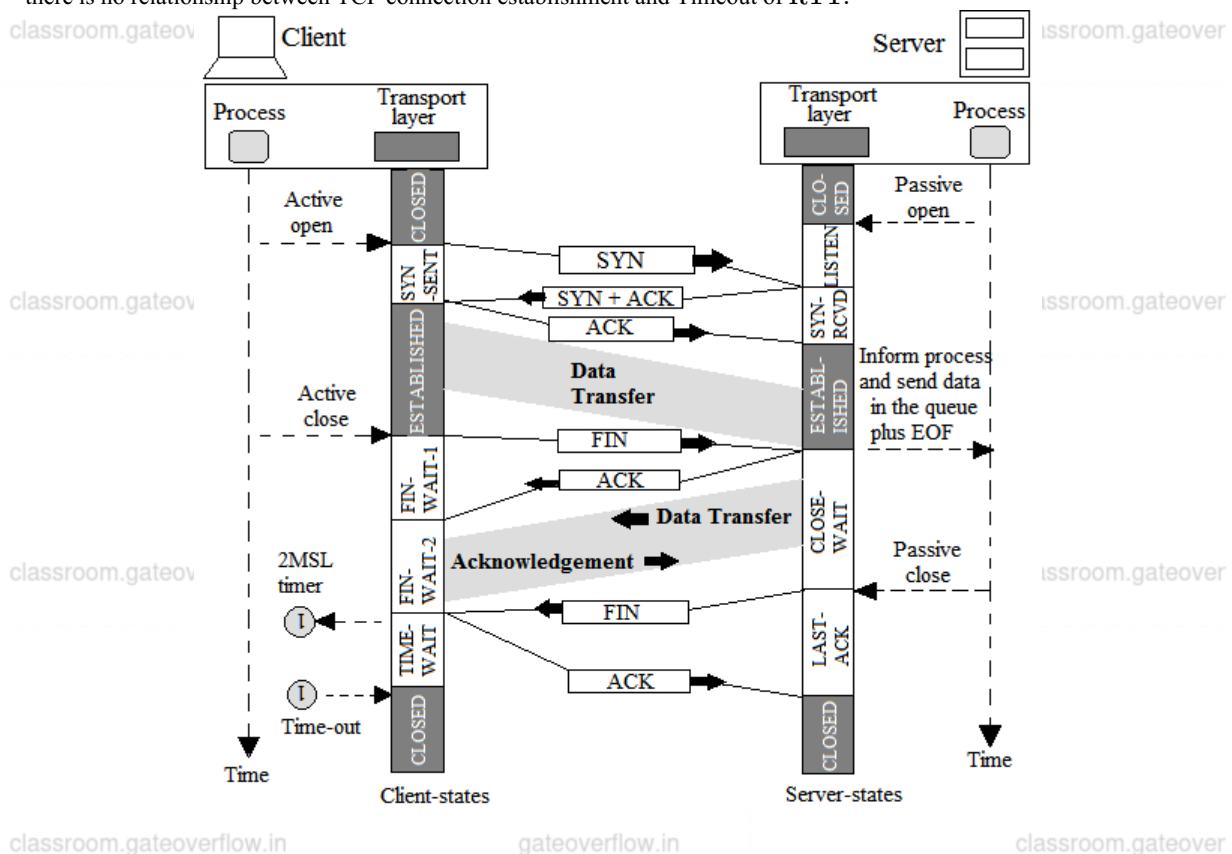


28 votes

-- Parul Agarwal (661 points)



- i. (i) TCP connection established in 3 phase between SYN send and SYN received (SYN, SYN + ACK, ACK). After this connection establishment, data transfer takes place. Now, FIN flag is called to close the connection. FIN flag can close the connection after getting the ACK from the receiver. If ACK is not received, a timer is set which wait for the time out. So, there is no relationship between TCP connection establishment and Timeout of RTT.



- ii. This is Jacobson's algorithm (Thanks @Anirudh)

$$\text{ERTT} = p \times \text{IRTT} + (1 - p) \times \text{NRTT}$$

p is scaling factor

IRTT initial RTT

NRTT is new RTT

[Link here](#)

- iii. Actually timeout value is more than twice the propagation delay from sender to receiver. Because after connection establishment and data transfer complete, then only timeout occurs. So, if we start timer at the beginning of transaction, Time Out occurs after RTT completes and after final ACK comes. So, Time Out time must be more than RTT.

So, only (ii) is TRUE. **Answer (B).**

References



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34 votes

-- srestha (85.2k points)



- ✓ Answer is D.

Because it is said that the connection is *TCP* and the sender has sent first two segments which is clear from the text "The sequence numbers of the first and second segments are 230 and 290 respectively." That means there must be 3 Way handshaking

that has been done before the connection has been established and when sender has sent SYN packet then receiver must have ACKED him with next packet .In response to it receiver only received only 1 packet so he will come to know that 1st packet has been lost and again he will send ACK for lost packet

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36 votes -- Aditi Tiwari (879 points)

2.29.17 Tcp: GATE IT 2008 | Question: 69 top

<https://gateoverflow.in/3383>



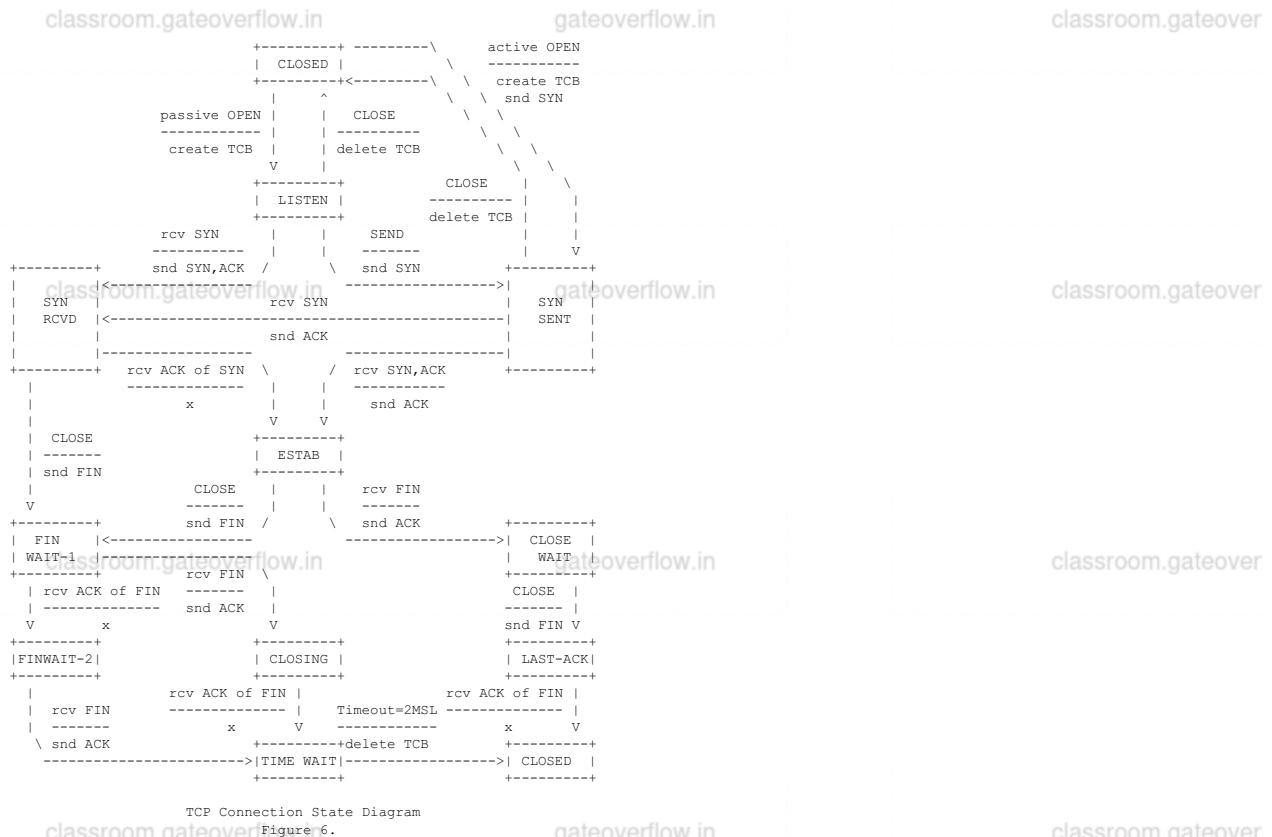
- ✓ (S1) Loss of SYN + ACK from the server will not establish a connection => True.
- (S2) Loss of ACK from the client cannot establish the connection => No this is not true. Detail reasoning: <http://stackoverflow.com/questions/16259774/what-if-a-tcp-handshake-segment-is-lost> If after ACK client immediately sends data then everything goes on without worry. (Though if along with ACK, first data packet is dropped, connection is reset)
- (S3) The server moves LISTEN → SYN_RECV → SYN_SENT → ESTABLISHED in the state machine on no packet loss => False .
- (S4) The server moves LISTEN → SYN_RECV → ESTABLISHED in the state machine on no packet loss. => True

Answer is (B) => S1 and S4 are true.

Reference for S4 => <https://www.rfc-editor.org/rfc/rfc793.txt>

September 1981

Transmission Control Protocol
Functional Specification



References



42 votes

-- Akash Kanase (36k points)

2.30

Token Bucket (2) top



A computer on a 10 Mbps network is regulated by a token bucket. The token bucket is filled at a rate of 2 Mbps . It is initially filled to capacity with 16 Megabits . What is the maximum duration for which the computer can transmit at the full 10 Mbps ?

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- A. 1.6 seconds
- B. 2 seconds
- C. 5 seconds
- D. 8 seconds

[gate2008-cse](#) [computer-networks](#) [token-bucket](#)

[Answer](#)



For a host machine that uses the token bucket algorithm for congestion control, the token bucket has a capacity of 1 megabyte and the maximum output rate is $20 \text{ megabytes per second}$. Tokens arrive at a rate to sustain output at a rate of $10 \text{ megabytes per second}$. The token bucket is currently full and the machine needs to send 12 megabytes of data. The minimum time required to transmit the data is _____ seconds.

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[gate2016-cse-set1](#) [computer-networks](#) [token-bucket](#) [normal](#) [numerical-answers](#)

[Answer](#)

Answers: Token Bucket



- ✓ New tokens are added at the rate of r bits/sec which is 2 Mbps in the given question.

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Capacity of the [token bucket](#) (b) = 16 Mbits

Maximum possible transmission rate (M) = 10 Mbps

So, the maximum burst time = $b/(M-r) = 16/(10-2) = 2 \text{ seconds}$

Here is the [animation](#) for token bucket hope this will help us to understand the concept.

Correct Answer: **B**

References



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45 votes

-- Vikrant Singh (11.2k points)



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Initially token bucket is full.

Rate at which it is emptying is $(20 - 10) \text{ MBps}$.

Time taken to empty token bucket of 1 MB is $\frac{1}{10}$ i.e. 0.1 sec .

Data send in this time is $0.1 * 20 = 2 \text{ MB}$ (**rate at which bucket is emptying is different from rate at which data is send**).

Data left to send is $12 - 2 = 10 \text{ MB}$.

Now bucket is empty and rate of token arriving is less than that of going out so effective data speed will be **10MBps**.

Time to send remaining **10MB** will be 1 sec . So total time is $1 + 0.1 = 1.1 \text{ sec}$

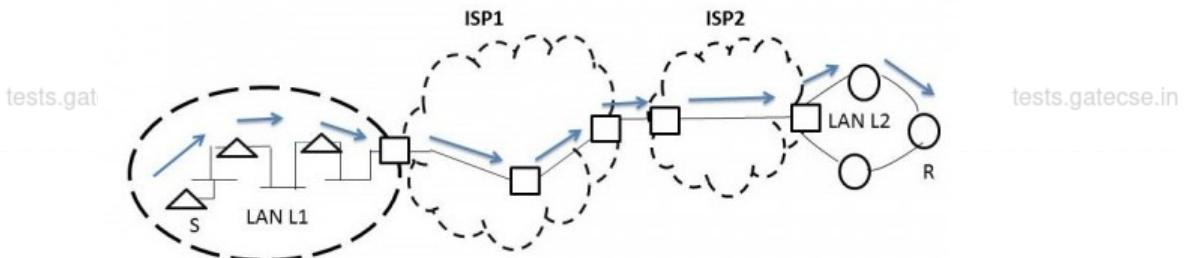
118 votes

-- Vaibhav Singh (445 points)

2.31

Token Ring (1) [top](#)2.31.1 Token Ring: GATE CSE 2014 Set 2 | Question: 25 [top](#)<https://gateoverflow.in/1983>

In the diagram shown below, $L1$ is an Ethernet LAN and $L2$ is a Token-Ring LAN. An IP packet originates from sender S and traverses to R , as shown. The links within each ISP and across the two ISPs, are all point-to-point optical links. The initial value of the TTL field is 32. The maximum possible value of the TTL field when R receives the datagram is _____.



[gate2014-cse-set2](#) [computer-networks](#) [numerical-answers](#) [lan-technologies](#) [ethernet](#) [token-ring](#) [normal](#)

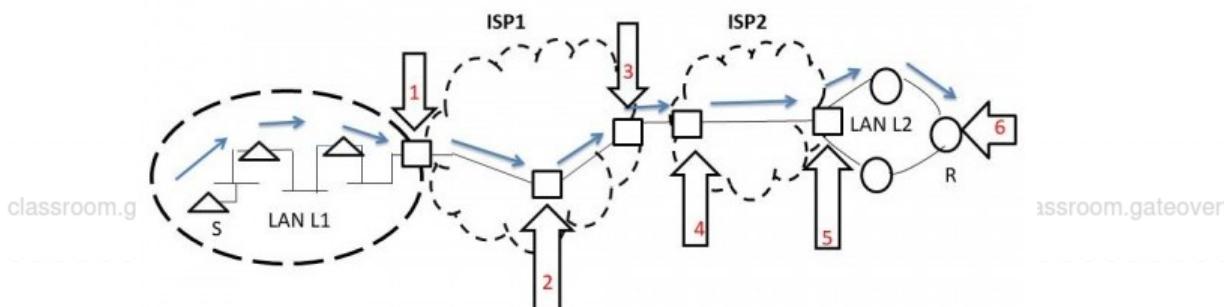
tests.gatecse.in

Answer [p](#)

Answers: Token Ring

2.31.1 Token Ring: GATE CSE 2014 Set 2 | Question: 25 [top](#)<https://gateoverflow.in/1983>

- Each time a packet visits network layer it decrements its TTL field. Source initializes it and others decrements it. Inside LAN it never goes to network layer, it is forwarded from data link layer itself.. in routers it goes upto network layer to make a routing decision.. and the router decrements it because the packet has visited the network layer.. and at the receiver too, the packet has visited the network layer and network layer will do its job and decrements the TTL value.



There are 5 routers, So Network Layer will be visited 5 times and 1 time on the destination

So, TTL = 26

PS:) A receiver decrements TTL value and then checks whether it is 0 (or) not. So, 26 is the answer (not 27)

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103 votes

-- Kalpish Singhal (1.6k points)

2.32

Udp (4) [top](#)2.32.1 Udp: GATE CSE 2005 | Question: 23 [top](#)<https://gateoverflow.in/1359>

Packets of the same session may be routed through different paths in:

- TCP, but not UDP
- TCP and UDP
- UDP, but not TCP
- Neither TCP nor UDP

[gate2005-cse](#) [tests.gatecse.in](#) [computer-networks](#) [tcp](#) [udp](#) [easy](#)

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tests.gatecse.in

Answer ↗

2.32.2 Udp: GATE CSE 2013 | Question: 12 top ↗

↗ <https://gateoverflow.in/1421>



The transport layer protocols used for real time multimedia, file transfer, DNS and email, respectively are

- A. TCP, UDP, UDP and TCP
- B. UDP, TCP, TCP and UDP
- C. UDP, TCP, UDP and TCP
- D. TCP, UDP, TCP and UDP

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[gate2013-cse](#) [computer-networks](#) [tcp](#) [udp](#) [easy](#)

Answer ↗

2.32.3 Udp: GATE CSE 2017 Set 2 | Question: 18 top ↗

↗ <https://gateoverflow.in/118209>



Consider socket API on a Linux machine that supports connected UDP sockets. A connected UDP socket is a UDP socket on which *connect* function has already been called. Which of the following statements is/are CORRECT?

- I. A connected UDP socket can be used to communicate with multiple peers simultaneously.
 - II. A process can successfully call *connect* function again for an already connected UDP socket.
-
- A. I only
 - B. II only
 - C. Both I and II
 - D. Neither I nor II

[gate2017-cse-set2](#) [computer-networks](#) [udp](#)

Answer ↗

2.32.4 Udp: GATE IT 2006 | Question: 69 top ↗

↗ <https://gateoverflow.in/3613>



A program on machine *X* attempts to open a *UDP* connection to port 5376 on a machine *Y*, and a *TCP* connection to port 8632 on machine *Z*. However, there are no applications listening at the corresponding ports on *Y* and *Z*. An *ICMP* Port Unreachable error will be generated by

- A. *Y* but not *Z*
- B. *Z* but not *Y*
- C. Neither *Y* nor *Z*
- D. Both *Y* and *Z*

[gate2006-it](#) [computer-networks](#) [tcp](#) [udp](#) [normal](#)

Answer ↗

Answers: Udp

2.32.1 Udp: GATE CSE 2005 | Question: 23 top ↗

↗ <https://gateoverflow.in/1359>



- ✓ b) TCP and UDP.

Routing happens in Network layer and hence has no dependency with the the transport layer protocols TCP and UDP. The transport layer protocol- whether TCP or UDP is hidden to the router and the routing path is determined based on the the network configuration at the time and hence can change even during a session.

Reference: <http://stackoverflow.com/questions/15601389/if-tcp-is-connection-oriented-why-do-packets-follow-different-paths>

References



65 votes

-- Arjun Suresh (332k points)

2.32.2 Udp: GATE CSE 2013 | Question: 12 [top](#)

<https://gateoverflow.in/1421>



- ✓ **Real Time Multimedia:** Data packets should be delivered faster. Also it can be unreliable. Therefore UDP.
- File Transfer:** For example downloading a file. It should be secure and reliable. Therefore TCP.
- DNS:** uses both UDP and TCP for its transport. But to achieve efficiency DNS uses UDP. To start a TCP connection a minimum of three packets are required (SYN out, SYN+ACK back, ACK out). UDP uses a simple transmission model with a minimum of protocol mechanism. UDP has no handshaking dialogues.
- Email:** uses SMTP protocol which uses TCP protocol.

Therefore, **C** is the answer.

43 votes

-- Pyuri sahu (1.5k points)

2.32.3 Udp: GATE CSE 2017 Set 2 | Question: 18 [top](#)

<https://gateoverflow.in/118209>



- ✓ **Calling connect Multiple Times for a UDP Socket**

A process with a connected UDP socket can call connect again for that socket for one of two reasons:

1. To specify a new IP address and port
2. To unconnect the socket

The first case specifying a new peer for a connected UDP socket differs from the use of connect with a TCP socket. Connect can be called only one time for a TCP socket. To unconnect a UDP socket, we call Connect but set the family member of the socket address structure to AT_UNSPEC.

Also, a UDP client or server can call Connect only if that process uses the UDP socket to communicate with **exactly one** peer.

http://www.masterraghlu.com/subjects/np/introduction/unix_network_programming_v1.3/ch08lev1sec11.html

So, option **B** should be answer.

For 1st part if "NOT connected" then it'll be true <http://stackoverflow.com/questions/3329641/how-do-multiple-clients-connect-simultaneously-to-one-port-say-80-on-a-server>

References



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34 votes

-- 2018 (5.5k points)

2.32.4 Udp: GATE IT 2006 | Question: 69 [top](#)

<https://gateoverflow.in/3613>



- ✓ Answer should be (**D**),

An ICMP packet with a message type 3 (Destination Unreachable) and a message code 3 (Port Unreachable) lets you know that the machine you tried to reach is not listening on this port. When you nmap a machine on a port it's not listening on, it sends back an ICMP packet like this to let you know that it's not listening on that port (if the port is not firewalled). If it is, then what happens depends on the config of your firewall).

ref @ <http://www.linuxchix.org/content/courses/security/icmp>

http://www.tcpipguide.com/free/t_ICMPv4DestinationUnreachableMessages-3.htm

http://en.wikipedia.org/wiki/Internet_Control_Message_Protocol#Destination_unreachable

Port Unreachable

Unlike the Network Unreachable and Host Unreachable messages which come from routers, the **Port Unreachable** message comes from a host. The primary implication for troubleshooting is that the frame was successfully routed across the communications infrastructure, the last router ARP'ed for the host, got the response, and sent the frame. Furthermore, the intended destination host was on-line and willing to accept the frame into its communications buffer. The frame was then processed by, say, TCP or, perhaps UDP, RIP, OSPF, or some other protocol. The protocol (TCP or UDP) tried to send the data up to the destination port number (TCP or UDP port) and the port process didn't exist. The protocol handler then

reports **Destination Unreachable - Port Unreachable**.

ref @ http://www.wildpackets.com/resources/compendium/tcp_ip/unreachable

- Port Unreachable - generated if the designated transport protocol (e.g., UDP) is unable to demultiplex the datagram in the transport layer of the final destination but has no protocol mechanism to inform the sender

<http://support.microsoft.com/en-us/kb/325122>

Port unreachable is a code 3 within type 3 @ <http://tools.ietf.org/html/rfc792>

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<http://www.iana.org/assignments/icmp-parameters/icmp-parameters.xhtml>

<http://www.faqs.org/rfcs/rfc792.html>

References



thumb up 28 votes

-- Mithlesh Upadhyay (4.3k points)

2.33

Wifi (1) top

2.33.1 Wifi: GATE CSE 2016 Set 2 | Question: 54 top

<https://gateoverflow.in/39593>



For the IEEE 802.11 MAC protocol for wireless communication, which of the following statements is/are TRUE?

- I. At least three non-overlapping channels are available for transmissions.
- II. The RTS-CTS mechanism is used for collision detection.
- III. Unicast frames are ACKed.

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- A. All I, II, and III
- B. I and III only
- C. II and III only
- D. II only

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Answer

Answers: Wifi

2.33.1 Wifi: GATE CSE 2016 Set 2 | Question: 54 top

<https://gateoverflow.in/39593>



✓ 802.11 MAC = Wifi

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- I. This is true, maximum 3 overlapping channels are possible in Wifi !
- II. This is false. Collision detection is not really possible in Wireless, because signal strength of sending & receiving signal need not be same ! So Wifi uses **collision Avoidance** instead ! In this RTS-CTS are used to announce to all nodes, that for which node wireless channel is reserved for communication. So this is collision avoidance, not detection
- III. This is true. Every frame in Wifi is acked, because Wifi station do not use collision detection, in Ethernet we use collision detection, in which it is possible for us to listen channel for collision & use exponential back off in case of collision detection. As in case of wifi, due to more error rate and not using collision detection strategy , we instead use ACK frame, in case of not getting ACK Host will retransmit after Random back off period

Answer is (B).

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Source: Kurose & Ross Top down approach to internet

Answer Keys

2.1.1	A	2.1.2	C	2.1.3	C	2.1.4	C	2.1.5	B
2.1.6	6	2.1.7	B	2.1.8	C	2.1.9	D	2.1.10	C
2.2.1	A	2.2.2	A	2.3.1	A	2.3.2	B	2.3.3	B
2.4.1	D	2.4.2	C	2.4.3	1100 : 1300	2.4.4	0.4404	2.4.5	C
2.4.6	50	2.4.7	B	2.5.1	B	2.5.2	C	2.5.3	C
2.5.4	A	2.6.1	D	2.6.2	200	2.6.3	C	2.6.4	A
2.6.5	B	2.7.1	C	2.7.2	B	2.7.3	A	2.7.4	C
2.7.5	B;C	2.7.6	B	2.7.7	A	2.8.1	3 : 4	2.8.2	A
2.8.3	C	2.8.4	B	2.8.5	A	2.8.6	B	2.8.7	C
2.8.8	N/A	2.9.1	B	2.9.2	B	2.9.3	D	2.9.4	C
2.10.1	N/A	2.10.2	A	2.11.1	A	2.12.1	D	2.12.2	D
2.12.3	B	2.12.4	C	2.12.5	C	2.12.6	256	2.12.7	9
2.12.8	144	2.13.1	C	2.13.2	D	2.13.3	D	2.13.4	A
2.13.5	B	2.13.6	C	2.13.7	13	2.13.8	D	2.14.1	D
2.14.2	A	2.14.3	3	2.14.4	D	2.14.5	D	2.14.6	B
2.15.1	D	2.16.1	D	2.16.2	12	2.16.3	B	2.16.4	C
2.17.1	N/A	2.17.2	D	2.17.3	D	2.17.4	C	2.17.5	A
2.18.1	D	2.18.2	A	2.18.3	B	2.18.4	C	2.18.5	B
2.18.6	C	2.19.1	D	2.19.2	C	2.19.3	A	2.19.4	C
2.19.5	C	2.19.6	50 : 52	2.19.7	C	2.19.8	D	2.19.9	B
2.20.1	D	2.20.2	D	2.20.3	1575	2.20.4	B	2.21.1	130 : 140
2.22.1	B	2.23.1	B	2.23.2	A	2.23.3	1	2.23.4	C
2.23.5	D	2.23.6	C	2.23.7	A	2.23.8	C	2.23.9	D
2.24.1	C	2.25.1	B	2.25.2	B	2.25.3	B	2.25.4	C
2.25.5	C	2.25.6	D	2.25.7	C	2.25.8	5	2.25.9	8
2.25.10	4	2.25.11	C	2.25.12	B	2.25.13	B	2.25.14	A
2.25.15	A	2.26.1	D	2.26.2	C	2.26.3	C	2.26.4	B
2.27.1	320	2.27.2	2500	2.27.3	86.5 : 89.5	2.27.4	D	2.27.5	B
2.28.1	D	2.28.2	A	2.28.3	D	2.28.4	C	2.28.5	C
2.28.6	C	2.28.7	D	2.28.8	A	2.28.9	A	2.28.10	158
2.28.11	C	2.28.12	B	2.28.13	C	2.28.14	D	2.28.15	C
2.28.16	D	2.28.17	C	2.28.18	B	2.29.1	A	2.29.2	C
2.29.3	B	2.29.4	C	2.29.5	A	2.29.6	C	2.29.7	D

2.29.8	34 : 35	2.29.9	44	2.29.10	A;B;C	2.29.11	A;C	2.29.12	C
2.29.13	A	2.29.14	A	2.29.15	B	2.29.16	D	2.29.17	B
2.30.1	B	2.30.2	1.10:1.19	2.31.1	26	2.32.1	B	2.32.2	C
2.32.3	B	2.32.4	D	2.33.1	B				



ER-model. Relational model: Relational algebra, Tuple calculus, SQL. Integrity constraints, Normal forms. File organization, Indexing (e.g., B and B+ trees). Transactions and concurrency control.

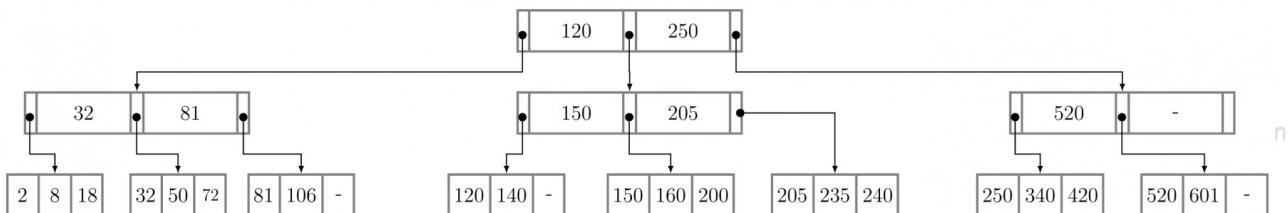
Mark Distribution in Previous GATE

Year	2021-1	2021-2	2020	2019	2018	2017-1	2017-2	2016-1	2016-2	Minimum	Average	Maximum
1 Mark Count	2	1	2	2	2	2	2	3	2	1	2	3
2 Marks Count	3	3	3	3	2	3	3	1	2	1	2.5	3
Total Marks	8	7	8	8	6	8	8	5	6	6	7.1	8

3.1

B Tree (28) top ↗3.1.1 B Tree: GATE CSE 1989 | Question: 12a top ↗
<https://gateoverflow.in/91199>


The below figure shows a B^+ tree where only key values are indicated in the records. Each block can hold upto three records. A record with a key value 34 is inserted into the B^+ tree. Obtain the modified B^+ tree after insertion.

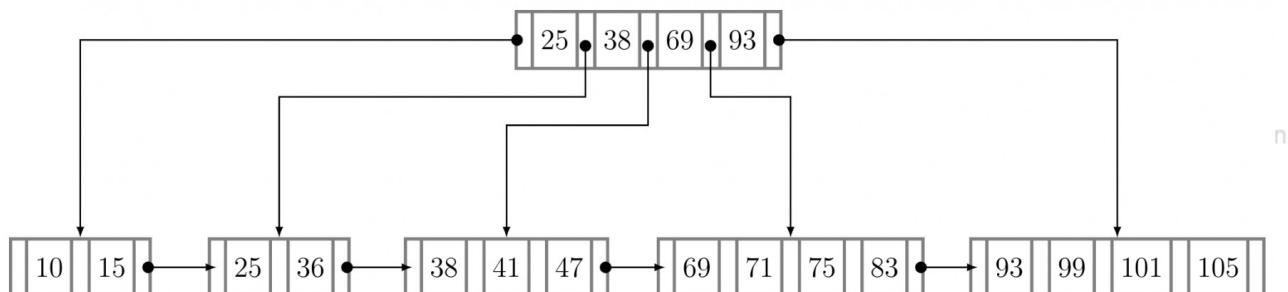

[descriptive](#) [gate1989](#) [databases](#) [b-tree](#)

Answer

3.1.2 B Tree: GATE CSE 1994 | Question: 14a top ↗
<https://gateoverflow.in/2510>


Consider B^+ - tree of order d shown in figure. (A B^+ - tree of order d contains between d and $2d$ keys in each node)

Draw the resulting B^+ - tree after 100 is inserted in the figure below.


[gate1994](#) [databases](#) [b-tree](#) [normal](#) [descriptive](#)

Answer

3.1.3 B Tree: GATE CSE 1994 | Question: 14b top ↗
<https://gateoverflow.in/360163>


For a B^+ - tree of order d with n leaf nodes, the number of nodes accessed during a search is $O(\dots)$.

[gate1994](#) [databases](#) [b-tree](#) [normal](#) [descriptive](#)

Answer

3.1.4 B Tree: GATE CSE 1997 | Question: 19 top ↗
<https://gateoverflow.in/2279>


A B^+ - tree of order d is a tree in which each internal node has between d and $2d$ key values. An internal node with M key values has $M + 1$ children. The root (if it is an internal node) has between 1 and $2d$ key values. The distance of a node from the root is the length of the path from the root to the node. All leaves are at the same distance from the root. The height of the tree is the distance of a leaf from the root.

- What is the total number of key values in the internal nodes of a B^+ -tree with l leaves ($l \geq 2$)?
- What is the maximum number of internal nodes in a B^+ -tree of order 4 with 52 leaves?
- What is the minimum number of leaves in a B^+ -tree of order d and height h ($h \geq 1$)?

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[gate1997](#) [databases](#) [b-tree](#) [normal](#) [descriptive](#)

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Answer 

3.1.5 B Tree: GATE CSE 1999 | Question: 1.25 [top](#)  <https://gateoverflow.in/1478>



Which of the following is correct?

- B-trees are for storing data on disk and B^+ trees are for main memory.
- Range queries are faster on B^+ trees.
- B-trees are for primary indexes and B^+ trees are for secondary indexes.
- The height of a B^+ tree is independent of the number of records.

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[gate1999](#) [databases](#) [b-tree](#) [normal](#)

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Answer 

3.1.6 B Tree: GATE CSE 1999 | Question: 21 [top](#)  <https://gateoverflow.in/1520>



Consider a B-tree with degree m , that is, the number of children, c , of any internal node (except the root) is such that $m \leq c \leq 2m - 1$. Derive the maximum and minimum number of records in the leaf nodes for such a B-tree with height h , $h \geq 1$. (Assume that the root of a tree is at height 0).

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[gate1999](#) [databases](#) [b-tree](#) [normal](#) [descriptive](#)

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Answer 

3.1.7 B Tree: GATE CSE 2000 | Question: 1.22, UGCNET-June2012-II: 11 [top](#)  <https://gateoverflow.in/646>



B^+ -trees are preferred to binary trees in databases because

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[gate2000-cse](#) [databases](#) [b-tree](#) [normal](#) [ugcnetjune2012ii](#)
- goclasses.in
- tests.gatecse.in
- Disk capacities are greater than memory capacities
 - Disk access is much slower than memory access
 - Disk data transfer rates are much less than memory data transfer rates
 - Disks are more reliable than memory

Answer 

3.1.8 B Tree: GATE CSE 2000 | Question: 21 [top](#)  <https://gateoverflow.in/692>



(a) Suppose you are given an empty B^+ tree where each node (leaf and internal) can store up to 5 key values. Suppose values 1, 2, ..., 10 are inserted, in order, into the tree. Show the tree pictorially

- after 6 insertions, and
- after all 10 insertions

Do NOT show intermediate stages.

(b) Suppose instead of splitting a node when it is full, we try to move a value to the left sibling. If there is no left sibling, or the left sibling is full, we split the node. Show the tree after values 1, 2, ..., 9 have been inserted. Assume, as in (a) that each node can hold up to 5 keys.

(c) In general, suppose a B^+ tree node can hold a maximum of m keys, and you insert a long sequence of keys in increasing order. Then what approximately is the average number of keys in each leaf level node.

- in the normal case, and
- with the insertion as in (b).

Answer 3.1.9 B Tree: GATE CSE 2001 | Question: 22 [top](#)<https://gateoverflow.in/763>

We wish to construct a B^+ tree with fan-out (the number of pointers per node) equal to 3 for the following set of key values:

80, 50, 10, 70, 30, 100, 90.in

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Assume that the tree is initially empty and the values are added in the order given.

- Show the tree after insertion of 10, after insertion of 30, and after insertion of 90. Intermediate trees need not be shown.
- The key values 30 and 10 are now deleted from the tree in that order show the tree after each deletion.

Answer 3.1.10 B Tree: GATE CSE 2002 | Question: 17 [top](#)<https://gateoverflow.in/870>

- The following table refers to search items for a key in B -trees and B^+ trees.

B-tree		B^+ -tree	
Successful search	Unsuccessful search	Successful search	Unsuccessful search
tests.gatecse.in X_1	X_2 goclasses.in	X_3	X_4 tests.gatecse.in

A successful search means that the key exists in the database and unsuccessful means that it is not present in the database. Each of the entries X_1, X_2, X_3 and X_4 can have a value of either Constant or Variable. Constant means that the search time is the same, independent of the specific key value, where variable means that it is dependent on the specific key value chosen for the search.

Give the correct values for the entries X_1, X_2, X_3 and X_4 (for example $X_1 = \text{Constant}$, $X_2 = \text{Constant}$, $X_3 = \text{Constant}$, $X_4 = \text{Constant}$)

- Relation $R(A, B)$ has the following view defined on it:

```
CREATE VIEW V AS
(SELECT R1.A, R2.B
FROM R AS R1, R AS R2
WHERE R1.B=R2.A)
```

- The current contents of relation R are shown below. What are the contents of the view V ?

A	B
1	2
2	3
2	4
4	5
6	7
6	8
9	10

- The tuples $(2, 11)$ and $(11, 6)$ are now inserted into R . What are the additional tuples that are inserted in V ?

Answer 3.1.11 B Tree: GATE CSE 2002 | Question: 2.23, UGCNET-June2012-II: 26 [top](#)<https://gateoverflow.in/853>

A B^+ - tree index is to be built on the *Name* attribute of the relation *STUDENT*. Assume that all the student names are of length 8 bytes, disk blocks are of size 512 bytes, and index pointers are of size 4 bytes. Given the scenario, what would be the best choice of the degree (i.e. number of pointers per node) of the B^+ - tree?

- A. 16
B. 42
C. 43
D. 44

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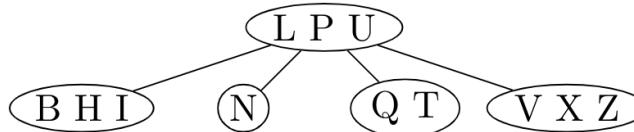
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gate2002-cse [databases](#) [b-tree](#) [normal](#) [ugcnetjune2012ii](#)

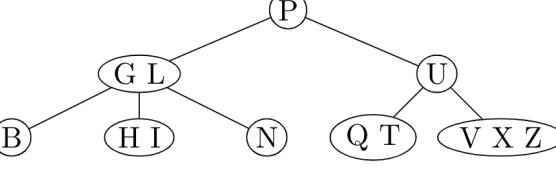
Answer 

3.1.12 B Tree: GATE CSE 2003 | Question: 65 [top](#) [!\[\]\(c1423bb1677993ab0ac74d454a6421c1_img.jpg\)](https://gateoverflow.in/952)

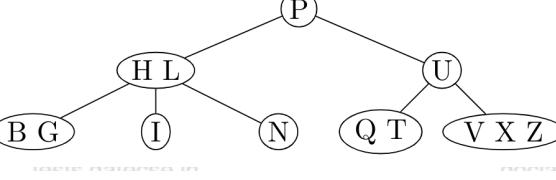
Consider the following 2 – 3 – 4 tree (i.e., B-tree with a minimum degree of two) in which each data item is a letter. The usual alphabetical ordering of letters is used in constructing the tree.



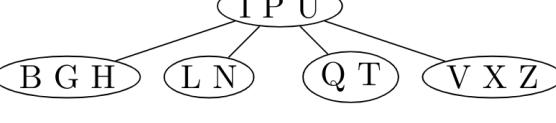
What is the result of inserting G in the above tree?

- A. 

```

graph TD
    P((P)) --- GL((G L))
    P --- U((U))
    GL --- B((B))
    GL --- HI((H I))
    GL --- N((N))
    U --- QT((Q T))
    U --- VXZ((V X Z))
  
```
- B. 

```

graph TD
    P((P)) --- HL((H L))
    P --- U((U))
    HL --- BG((B G))
    HL --- I((I))
    HL --- N((N))
    U --- QT((Q T))
    U --- VXZ((V X Z))
  
```
- C. 

```

graph TD
    IPU((I P U)) --- BGH((B G H))
    IPU --- LN((L N))
    IPU --- QT((Q T))
    IPU --- VXZ((V X Z))
  
```
- D. None of the above

gate2003-cse [databases](#) [b-tree](#) [normal](#)

Answer 

3.1.13 B Tree: GATE CSE 2004 | Question: 52 [top](#) [!\[\]\(e98c3d17d57b947fde1534aa705444fb_img.jpg\)](https://gateoverflow.in/1048)

The order of an internal node in a $B+$ tree index is the maximum number of children it can have. Suppose that a child pointer takes 6 bytes, the search field value takes 14 bytes, and the block size is 512 bytes. What is the order of the internal node?

- A. 24
B. 25
C. 26
D. 27

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gate2004-cse [databases](#) [b-tree](#) [normal](#)

Answer 

3.1.14 B Tree: GATE CSE 2005 | Question: 28 [top](#) [!\[\]\(c082100588c9398d66a34bae99b78ad0_img.jpg\)](https://gateoverflow.in/1364)

Which of the following is a key factor for preferring B^+ -trees to binary search trees for indexing database relations?

- A. Database relations have a large number of records

- B. Database relations are sorted on the primary key
C. B^+ -trees require less memory than binary search trees
D. Data transfer from disks is in blocks

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gate2005-cse databases b-tree normal

Answer ↗

3.1.15 B Tree: GATE CSE 2007 | Question: 63, ISRO2016-59 top ↵

↗ <https://gateoverflow.in/1261>



The order of a leaf node in a B^+ -tree is the maximum number of (value, data record pointer) pairs it can hold. Given that the block size is $1K$ bytes, data record pointer is 7 bytes long, the value field is 9 bytes long and a block pointer is 6 bytes long, what is the order of the leaf node?

- A. 63
B. 64
C. 67
D. 68

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gate2007-cse databases b-tree normal isro2016

Answer ↗

3.1.16 B Tree: GATE CSE 2008 | Question: 41 top ↵

↗ <https://gateoverflow.in/453>



A B-tree of order 4 is built from scratch by 10 successive insertions. What is the maximum number of node splitting operations that may take place?

- A. 3
B. 4
C. 5
D. 6

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gate2008-cse databases b-tree normal

Answer ↗

3.1.17 B Tree: GATE CSE 2009 | Question: 44 top ↵

↗ <https://gateoverflow.in/1330>



The following key values are inserted into a B^+ -tree in which order of the internal nodes is 3, and that of the leaf nodes is 2, in the sequence given below. The order of internal nodes is the maximum number of tree pointers in each node, and the order of leaf nodes is the maximum number of data items that can be stored in it. The B^+ -tree is initially empty

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10, 3, 6, 8, 4, 2, 1

The maximum number of times leaf nodes would get split up as a result of these insertions is

- A. 2
B. 3
C. 4
D. 5

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gate2009-cse databases b-tree normal

Answer ↗

3.1.18 B Tree: GATE CSE 2010 | Question: 18 top ↵

↗ <https://gateoverflow.in/2191>



Consider a B^+ -tree in which the maximum number of keys in a node is 5. What is the minimum number of keys in any non-root node?

- A. 1
B. 2
C. 3
D. 4

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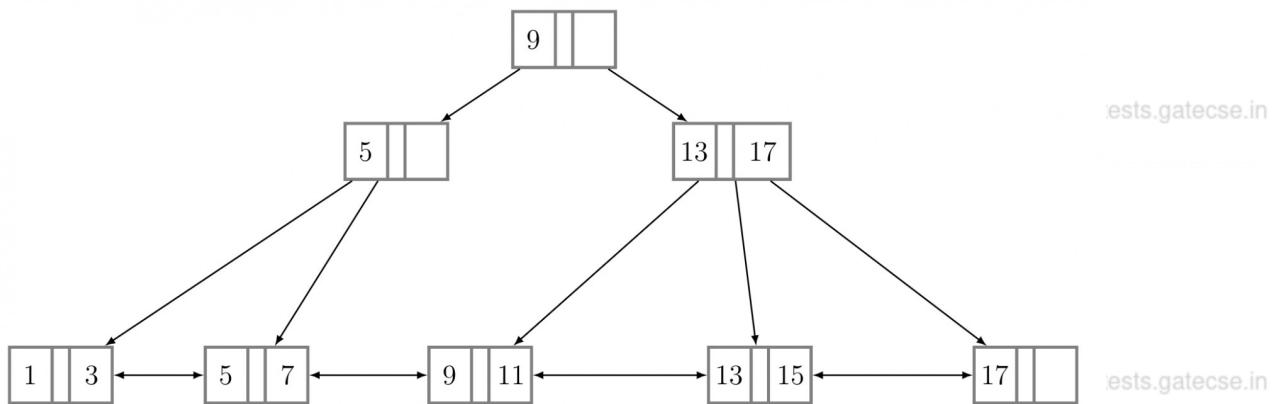
goclasses.in

tests.gatecse.in

Answer ↗

3.1.19 B Tree: GATE CSE 2015 Set 2 | Question: 6 top ↗<https://gateoverflow.in/8052>

With reference to the B+ tree index of order 1 shown below, the minimum number of nodes (including the Root node) that must be fetched in order to satisfy the following query. "Get all records with a search key greater than or equal to 7 and less than 15" is _____.



Answer ↗

3.1.20 B Tree: GATE CSE 2015 Set 3 | Question: 46 top ↗<https://gateoverflow.in/8555>

Consider a B+ tree in which the search key is 12 byte long, block size is 1024 byte, recorder pointer is 10 byte long and the block pointer is 8 byte long. The maximum number of keys that can be accommodated in each non-leaf node of the tree is _____.

Answer ↗

3.1.21 B Tree: GATE CSE 2016 Set 2 | Question: 21 top ↗<https://gateoverflow.in/3959>

B+ Trees are considered BALANCED because.

- The lengths of the paths from the root to all leaf nodes are all equal.
- The lengths of the paths from the root to all leaf nodes differ from each other by at most 1.
- The number of children of any two non-leaf sibling nodes differ by at most 1.
- The number of records in any two leaf nodes differ by at most 1.

Answer ↗

3.1.22 B Tree: GATE CSE 2017 Set 2 | Question: 49 top ↗<https://gateoverflow.in/118561>

In a B⁺ Tree , if the search-key value is 8 bytes long , the block size is 512 bytes and the pointer size is 2 B , then the maximum order of the B⁺ Tree is _____

Answer ↗

3.1.23 B Tree: GATE CSE 2019 | Question: 14 top ↗<https://gateoverflow.in/302834>

Which one of the following statements is NOT correct about the B+ tree data structure used for creating an index of a

relational database table?

- A. B+ Tree is a height-balanced tree
- B. Non-leaf nodes have pointers to data records
- C. Key values in each node are kept in sorted order
- D. Each leaf node has a pointer to the next leaf node

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gate2019-cse databases b-tree

Answer 

3.1.24 B Tree: GATE IT 2004 | Question: 79 [top](#) 

Consider a table T in a relational database with a key field K . A B -tree of order p is used as an access structure on K , where p denotes the maximum number of tree pointers in a B -tree index node. Assume that K is 10 bytes long; disk block size is 512 bytes; each data pointer P_D is 8 bytes long and each block pointer P_B is 5 bytes long. In order for each B -tree node to fit in a single disk block, the maximum value of p is

- A. 20
- B. 22
- C. 23
- D. 32

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gate2004-it databases b-tree normal

Answer 

3.1.25 B Tree: GATE IT 2005 | Question: 23, ISRO2017-67 [top](#) 

A B -Tree used as an index for a large database table has four levels including the root node. If a new key is inserted in this index, then the maximum number of nodes that could be newly created in the process are

- A. 5
- B. 4
- C. 3
- D. 2

gate2005-it databases b-tree normal isro2017

Answer 

3.1.26 B Tree: GATE IT 2006 | Question: 61 [top](#) 

In a database file structure, the search key field is 9 bytes long, the block size is 512 bytes, a record pointer is 7 bytes and a block pointer is 6 bytes. The largest possible order of a non-leaf node in a B^+ tree implementing this file structure is

- A. 23
- B. 24
- C. 34
- D. 44

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gate2006-it databases b-tree normal

Answer 

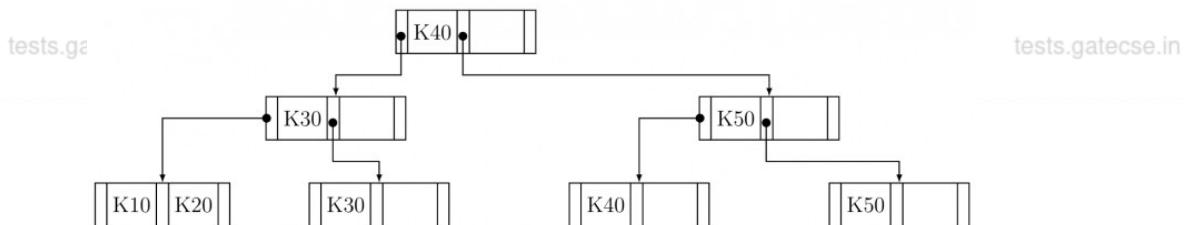
3.1.27 B Tree: GATE IT 2007 | Question: 84 [top](#) 

Consider the B^+ tree in the adjoining figure, where each node has at most two keys and three links.

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Keys K_{15} and then K_{25} are inserted into this tree in that order. Exactly how many of the following nodes (disregarding the links) will be present in the tree after the two insertions?

- A. 1
- B. 2
- C. 3
- D. 4

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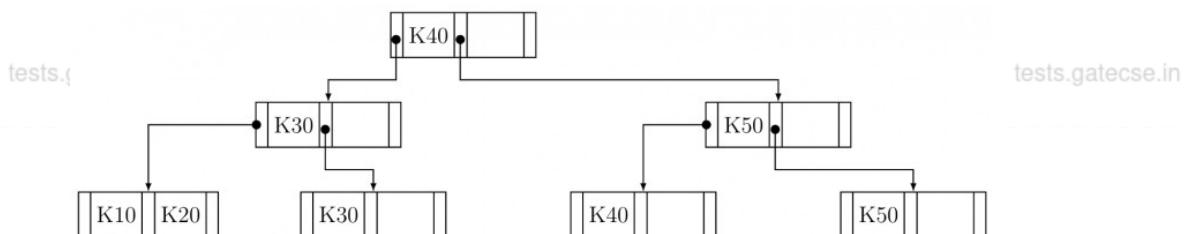
Answer

3.1.28 B Tree: GATE IT 2007 | Question: 85 [top](#)

<https://gateoverflow.in/3537>



Consider the B^+ tree in the adjoining figure, where each node has at most two keys and three links.



Keys K_{15} and then K_{25} are inserted into this tree in that order. Now the key K_{50} is deleted from the B^+ tree resulting after the two insertions made earlier. Consider the following statements about the B^+ tree resulting after this deletion.

- i. The height of the tree remains the same.
- ii. The node (disregarding the links) is present in the tree.
- iii. The root node remains unchanged (disregarding the links).

Which one of the following options is true?

- A. Statements (i) and (ii) are true
- B. Statements (ii) and (iii) are true
- C. Statements (iii) and (i) are true
- D. All the statements are false

gate2007-it databases b-tree normal goclasses.in tests.gatecse.in

Answer

Answers: B Tree

3.1.1 B Tree: GATE CSE 1989 | Question: 12a [top](#)

<https://gateoverflow.in/91199>



- ✓ B^+ tree [Reference](#).

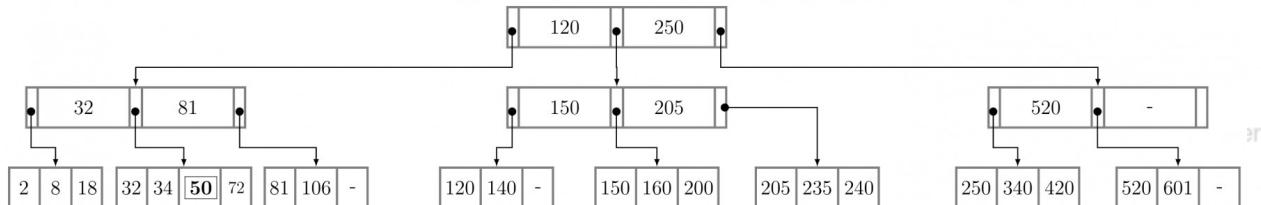
In a B^+ tree only the leaf nodes have a pointer to actual data (record pointers) whereas internal nodes points to index blocks.

In the given question we have

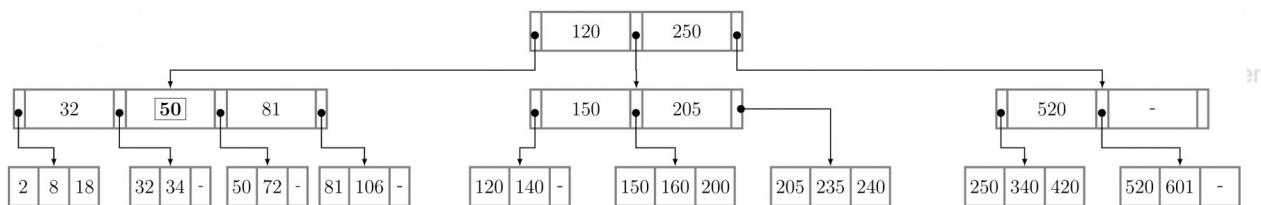
- M : Number of pointers in internal nodes = 3.

- L : Number of data items in a leaf node = 3.
- Further we can see that right biasing is used while splitting a node (same key value moving to the right, in a B^+ tree all internal key values will be present in leaf node as only the leaf node actually points to the data record)

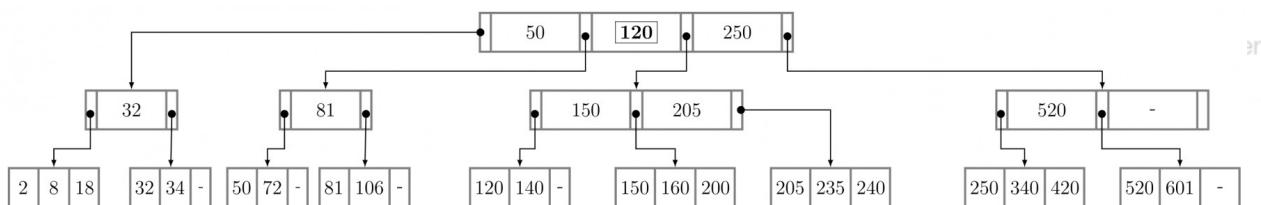
To insert 34 we'll first place it in the sorted order among the leaf nodes.



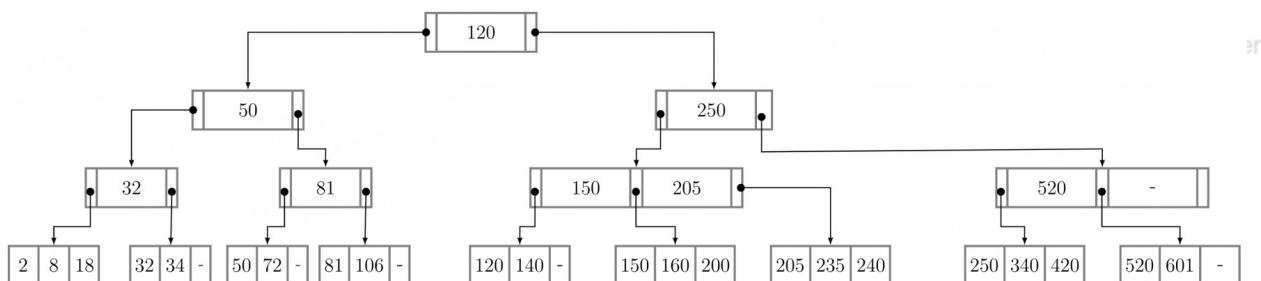
Now, we see that the block (being the leaf node the pointers here are record pointers) having 34 is overflowing and so we'll split it and move the center element to the parent block. There might be a confusion as to whether 34 or 50 should move up, but if we see the question it is following right biasing (same key value is going to the right) and so 50 must move up.



Now, we have an overflow in the internal node as the maximum capacity of an internal node is 3 block pointers but we are having 4 here. So we must again split and move 50 upwards.



Now we have an overflow in the root node and so we must again split and move 120 upwards making a new root.



Now all the B^+ tree requirements are satisfied and so the insertion algorithm terminates.

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References



0 votes

-- Arjun Suresh (332k points)

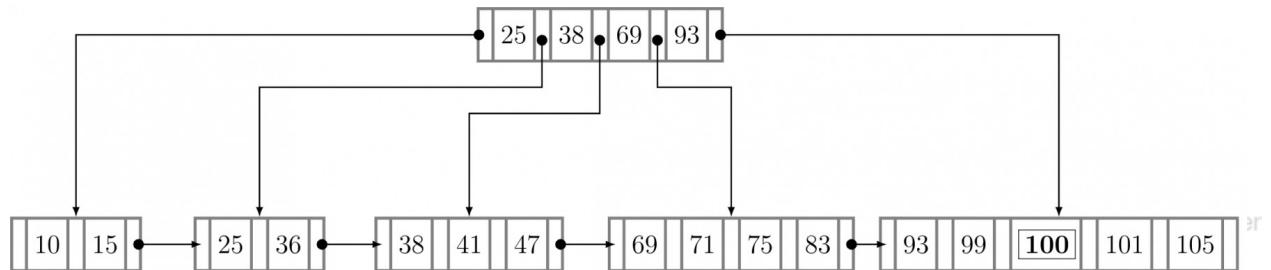
3.1.2 B Tree: GATE CSE 1994 | Question: 14a top

→ <https://gateoverflow.in/2510>

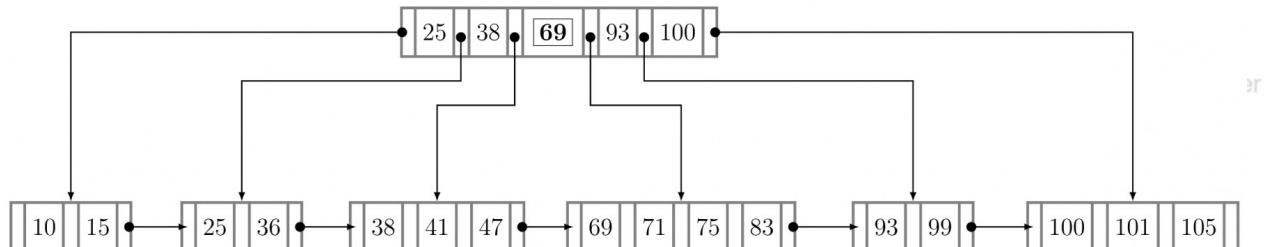


- ✓ For the given B^+ tree, $d = 2 \implies 2d = 4$. Also right biasing is followed as 69 is to the right of 69 in the parent node.

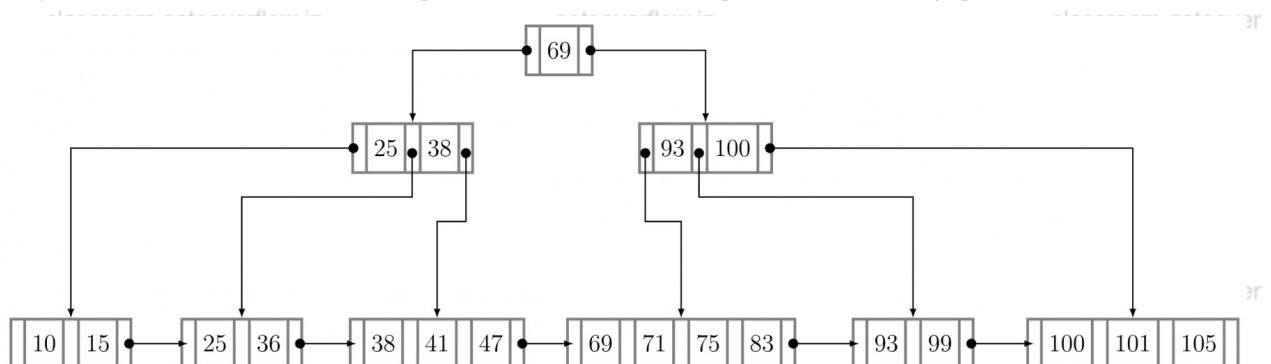
We'll insert 100 in the sorted position among the leaf nodes.



This causes an overflow and so the node will split into 2 by moving the element at position $\left\lceil \frac{2d+1}{2} \right\rceil = \left\lceil \frac{5}{2} \right\rceil = 3$, which is 100. Thus we get.



This again causes an overflow at the root node and 69 needs to be moved up forming a new root. Here, 69 is not a record pointer (only leaf nodes in B^+ tree contains record pointers) and so we need not replicate it while moving up.



Now all the property of B^+ tree is satisfied and the insertion algorithm terminates.

1 like 31 votes

-- Bikram (58.4k points)

3.1.3 B Tree: GATE CSE 1994 | Question: 14b top

<https://gateoverflow.in/360163>



- For n leaves we have $n - 1$ keys in the internal node. (see 'part a' of this [question](#))

Total keys in internal nodes = $n - 1$, each node can have keys between d and $2d$.

For $n - 1$ keys there will be minimum $\left\lceil \frac{n-1}{2d} \right\rceil$ internal nodes, and maximum $\left\lceil \frac{n-1}{d} \right\rceil$ internal nodes.

To calculate Big-Omega I am taking maximum everywhere.

If every node contains $d + 1$ pointers (d keys) then height will be maximum, because number of nodes to be accommodated are fixed $\left(\left\lceil \frac{n-1}{d} \right\rceil \right)$.

If height is h then equation becomes

$$\begin{aligned}
 1 + (d+1) + (d+1)^2 + (d+1)^3 + \dots + (d+1)^{h-1} &= \frac{n-1}{d} \\
 \Rightarrow \frac{(d+1)^h - 1}{(d+1)-1} &= \frac{n-1}{d} \\
 \Rightarrow (d+1)^h &= n \\
 \Rightarrow h &= \log_{(d+1)} n
 \end{aligned}$$

This is the maximum height possible or says the maximum number of levels possible.

Now using h traverse we can get to the leaf node :

Answer is $O(h)$ i.e., $O(\log_{(d+1)} n) = O(\log_d n)$

References



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-- Sachin Mittal (15.8k points)

3.1.4 B Tree: GATE CSE 1997 | Question: 19 [top](#)

<https://gateoverflow.in/2279>



- ✓ Let us understand specification of B^+ tree first

For a non-root node

- Minimum number of keys = $d \implies$ minimum number of children = $d + 1$
- Maximum number of keys = $2d \implies$ maximum number of children = $2d + 1$

For a root node

- Minimum number of keys = 1 so, minimum number of children = 2
- Maximum number of keys = $2d$ so, maximum number of children = $2d + 1$

Now, coming to our actual question

Part (A). For a given no of leaf node ($L \geq 2$) what will be the total no of keys in internal nodes?

Will solve this in three ways:

1. Assuming maximum nodes at each level

Height	#nodes	#keys
0	1	$2d$
1	$2d + 1$	$2d(2d + 1)$
:	:	:
h	$(2d + 1)^h$	$2d[(2d + 1)^h]$

$$\text{No. of leaf nodes} = (2d + 1)^h = L$$

$$\begin{aligned}\text{Total no. of keys in internal nodes} &= 2d + 2d(2d + 1) + 2d(2d + 1)^2 + \dots + 2d(2d + 1)^{h-1} \\ &= (2d + 1)^h - 1 = L - 1\end{aligned}$$

2. Assuming minimum nodes at each level

Height	#nodes	#keys
0	1	1
1	2	$2d$
:	:	:
h	$2(d + 1)^{h-1}$	$2d[(d + 1)^{h-1}]$

$$\text{So, no. of leaf nodes} = 2(d + 1)^{h-1} = L$$

$$\begin{aligned}\text{Total no of keys in internal nodes} &= 1 + 2d + 2d(d + 1) + \dots + 2d(d + 1)^{h-2} \\ &= 2(d + 1)^{h-1} - 1 = L - 1\end{aligned}$$

3. Whenever there is an overflow in a leaf node (or whenever no of leaf node increases by one), then we move a key in the internal node (or we can say, no of internal keys increases by one).

Now, let's start with the base case. Only 2 leaf nodes (as given $L \geq 2$). So, no. of keys in root node = 1 or $L - 1$.

Once there is an overflow in a single leaf node then no of leaf nodes now would become 3 and at the same time we will have one more key in our root node.

Part (B) Maximum number of internal nodes in a B^+ tree of order 4 with 52 leaves?

Using Bulk loading approach, here we will use minimum fill factor ($d = 4$ hence, min keys = $d = 4$ and min children/block pointer = $d + 1 = 5$)

So, we have 52 leaves so and need total 52 block pointers and one node should have minimum 5 block pointers.

So, for 52 leaves we require $\lceil 52/5 \rceil = 10$ nodes

For 11 block pointers we require $\lfloor 10/5 \rfloor = 2$ nodes
For 2 block pointers we require 1 node "it is root node"
So, max no of internal nodes= $10 + 2 + 1 = 13$ nodes

Part (C) Minimum number of leaves in a B+ tree of order d and height h ($h \geq 1$)?

By part (A) "assuming minimum nodes at each level" case

$$\text{Minimum no. of leaves} = 2(d+1)^{h-1}$$

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42 votes

-- saurabh rai (9k points)

3.1.5 B Tree: GATE CSE 1999 | Question: 1.25 top



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- A. False. Both r stored in disk
- B. True. By searching leaf level linearly in B^+ tree, we can say a node is present or not in B^+ tree. But for B tree we have to traverse the whole tree
- C. False. B tree and B^+ tree uses dynamic multilevel indexes <http://home.iitj.ac.in/~ramana/ch10-storage-2.pdf>
- D. False. Height depends on number of record and also max no of keys in each node (order of tree)

Correct Answer: B

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References



49 votes

-- srestha (85.2k points)

3.1.6 B Tree: GATE CSE 1999 | Question: 21 top



Given a B tree :

- max children at a node : $2m - 1 \implies$ max keys : $2m - 2$
- min children at a node : $m \implies$ min keys : $m - 1$

At Root node : min keys : 1 \implies min children : 2

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Here, leaf level is at level h (because root is at level 0)

Now, we have to find

1. Minimum keys at leaf level(complete bottommost level, not just a node) -
 - For this, we have to consider minimum everywhere.
 - Firstly we will count the minimum possible nodes at the leaf level.
 - At Root Node (level 0) : It can have minimum 2 child (mean 2 nodes minimum for next level)
 - At level 1: It has 2 nodes, each can have a minimum of m child (so, this gives $2 * m$ minimum possible nodes at next level)
 - At level 2 : min $2 * m^2$ Child and so on.
 - At level $(h - 1) : 2 * (m)^{h-1}$ child (these are min number of leaf nodes possible)
 - At level h (leaf level) : $2 * (m)^{h-1}$ nodes each having minimum $(m - 1)$ keys. So, this gives the answer as $2 * (m)^{h-1} * (m - 1)$ minimum keys possible at leaf level.
2. Maximum keys at leaf level(complete bottommost level, not just a node) -
 - For this, we have to count max everywhere.
 - At root (level 0) : max child possible $2m - 1$ (nodes for next level)
 - At level 1 ; $2m - 1$ nodes give $(2m - 1)^2$ child
 - At level $(h - 1) : (2m - 1)^{h-1}$ child (these are maximum possible nodes at leaf level)
 - At level h (leaf level) : $(2m - 1)^h$ nodes each having a maximum of $(2m - 2)$ keys. Giving a total of - $(2m - 1)^h * (2m - 2)$ maximum keys at leaf level.

43 votes

-- Himanshu Agarwal (12.4k points)



- ✓ Answer is (B). The major advantage of $B+$ tree is in reducing the number of last level access which would be from disk in case of large data size.

<http://stackoverflow.com/questions/15485220/advantage-of-b-trees-over-bsts>

References



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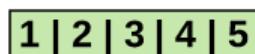
46 votes

-- Arjun Suresh (332k points)

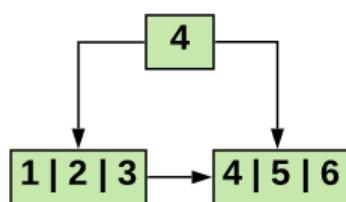


A.i)

i) Inserting 1-5 is straight forward :



then we Insert 6 :



A.ii)

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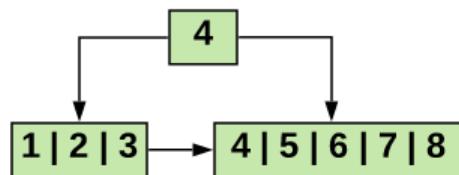
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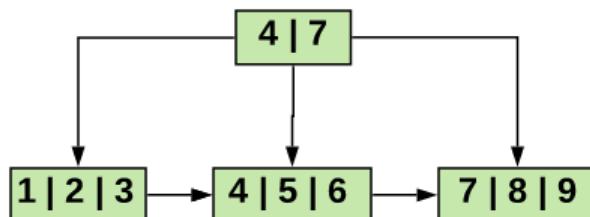
ii) After Inserting 7,8:

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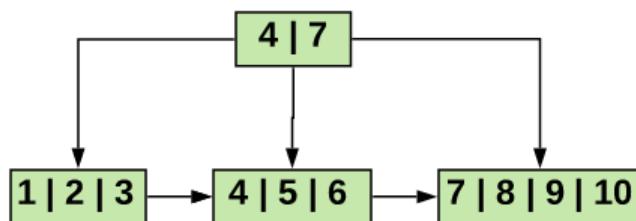
Insert 9 :

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Insert 10 :



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B)

B) Inserting 1-5 is same as previous

1

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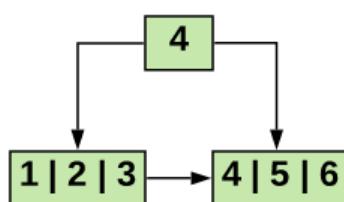
1 | 2 | 3 | 4 | 5

then we Insert 6 :

1

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there is no left sibling we
split the node.



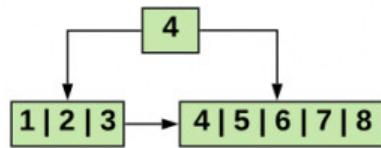
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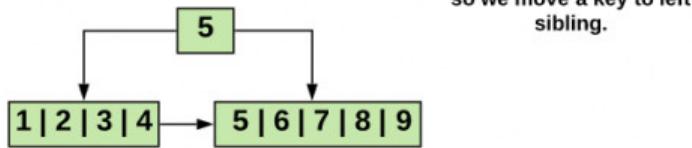
Insert 7.8:



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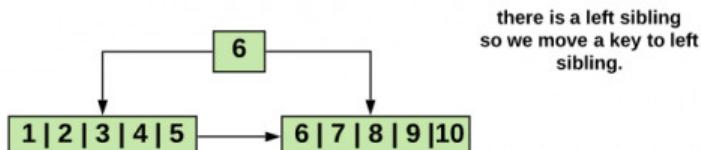
Insert 9 :



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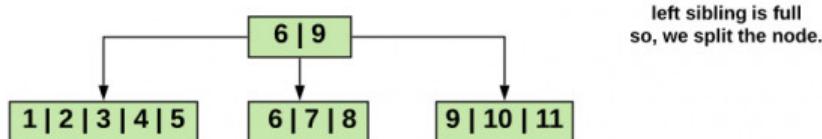
The next 2 insertions weren't asked in the question but will help you to understand part C of this question.

Insert 10 :



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Insert 11 :



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C. Insert a LONG SEQUENCE of keys in INCREASING ORDER

- In normal case: Insertion always will be done at the rightmost leaf node, and all nodes will have exactly $\lfloor \frac{m+1}{2} \rfloor$ keys except this rightmost leaf (no of keys can vary from $\lfloor \frac{m+1}{2} \rfloor$ to m for rightmost leaf).

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For a long sequence, we can say the average is approximately $\lfloor \frac{m+1}{2} \rfloor$ (This is the answer).

(There are two possible answers for this part, I left it on the reader to find out the second one)

Because all nodes will have

$\lfloor \frac{m+1}{2} \rfloor$ keys except 1 rightmost node.

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we can also find the exact average in this case:

Let there are n keys in total (inserted in increasing order),

$$\text{No of leaf nodes will be exactly } \left\lceil \frac{n}{\lfloor \frac{m+1}{2} \rfloor} \right\rceil$$

Average number of keys in leaf would be: $\frac{n}{\left\lceil \frac{n}{\lfloor \frac{m+1}{2} \rfloor} \right\rceil}$

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- ii. With insertion as in (B): In this case, we can observe until the left sibling is full, we are shifting a key to the left leaf. As we insert more and more keys all leaf nodes are filled except the rightmost two leaves, the rightmost 2 leaves can have any number of in $\lfloor \frac{m+1}{2} \rfloor$ to m each.

For a long sequence, we can say the average is approximately
_{classroom.gateoverflow.in}
_m (Same reasoning as case i)

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we can find the actual average in this case as well,

Let there are n keys in total (inserted in increasing order),

Number of leaf nodes in this case will be $\lceil \frac{n}{m} \rceil$,

so average number of keys would be: $\frac{n}{\lceil \frac{n}{m} \rceil}$



4 votes

-- Nikhil Dhamu (2.5k points)

3.1.9 B Tree: GATE CSE 2001 | Question: 22

<https://gateoverflow.in/763>

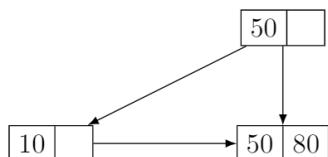


(a) B^+ tree insertion: 80, 50, 10, 70, 30, 100, 90

Order of $B^+ = p = 3$

- Overflow: When number of key values exceed $p - 1 = 3 - 1 = 2$

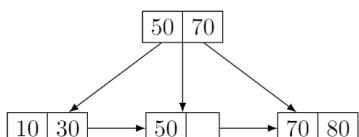
Tree after insertion of 10 :



Tree after insertion of 30 :

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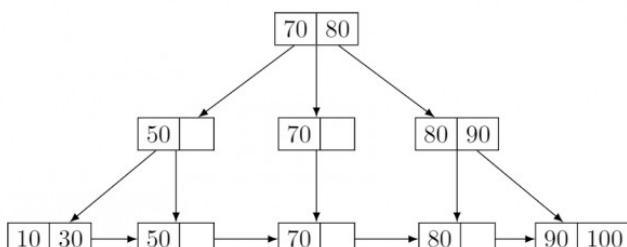
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Tree after insertion of 90 :

flow.in

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(b) classroom.gateoverflow.in

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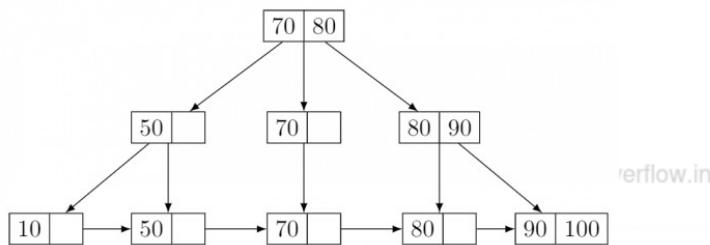
- Underflow: if leaf node contain $\lceil \frac{p}{2} \rceil - 1 = 2 - 1 = 1$ key values.

Deletion of key-value 30 :

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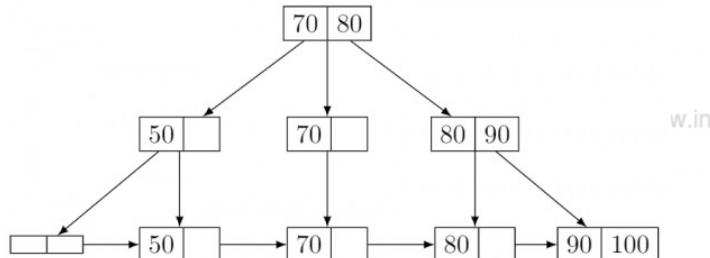
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Deletion of key-value 10 :



w.in classroom.gateoverflow.in

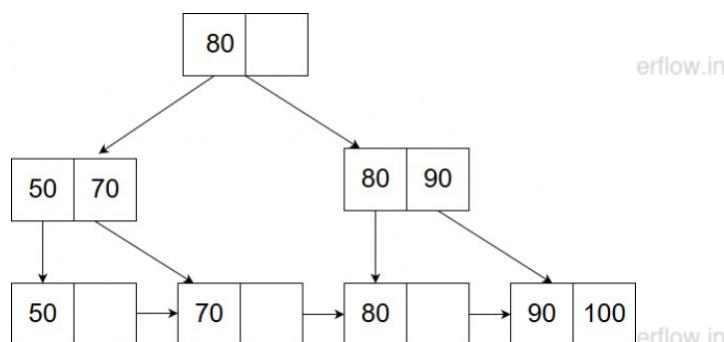
Here when we delete the key-value 10 then underflow happened, so we can merge this node with the right sibling.

When we merge two nodes then the parent node one value needs to come down i.e. 50 here.

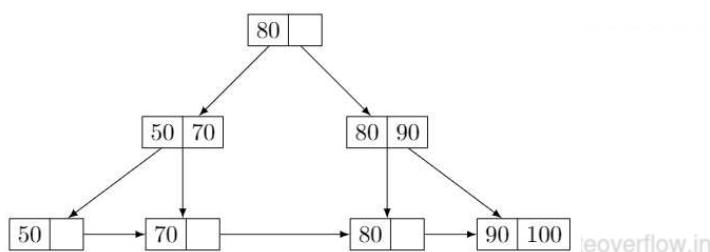
Now if we try to bring 50 down then that node will again suffer from underflow as it will become empty. classroom.gateoverflow.in
so we will try to merge this node it with its right sibling i.e. the node which contains 70

Again, When we merge two nodes(nodes in the 2nd level that contain 50 and 70) then one value of the parent node (i.e. node having 50, 70) needs to come down

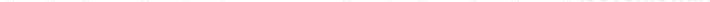
So we will bring 70 down and merge it with 50 since bringing 70 down will not cause underflow as 80 is present in the parent node.



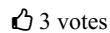
erflow.in classroom.gateover



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3 votes

-- Lakshman Patel (65.7k points)

3.1.10 B Tree: GATE CSE 2002 | Question: 17 top

<https://gateoverflow.in/870>



For A)

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X1 = Variable (Key can be found @ Internal nodes at various levels)

X2 = Constant

X3 = Variable, We need to just check where key is present/absent, not to access Data. (A successful search means that the key

exists in the database and unsuccessful means that it is not present in the database.) So Variable **X4** = Constant

For Part B) i) Write down two copies of the same table for comparison side by side. Just map **B** of first to A of the second copy. Those matching tuples take **A** of first table & **B** of seconds.

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Content of View A

A	B
1	3
1	4
2	5

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For Part B) ii)

Additional tuples getting inserted:

A	B
11	7
11	8
2	6
1	11

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30 votes

-- Akash Kanase (36k points)



✓ Answer: C

In a B^+ tree we want entire node content to be in a disk block. A node can contain up to p pointers to child nodes and up to $p - 1$ key values for a B^+ tree of order p . Here, key size is 8 bytes and index pointer size is 4 bytes. Now a B^+ tree has different structure for internal node and leaf nodes. While internal nodes can have upto $p - 1$ key values and p child pointers, leaf node will have one sibling pointer in addition to maximum $p - 1$ keys and $p - 1$ record pointers. Since our key is Name attribute which is not assumed to be unique it must be a secondary index and hence the record pointer must be an index pointer to primary index. This will ensure size of a leaf node is same as the size of a non-leaf node. Hence for a maximum sized node we can write

$$(8 + 4)(p - 1) + 4 \leq 512 \implies 12p \leq 520 \implies p = 43.$$

<http://www.cchurch.com/cs/340/reading/btree/index.html> gateoverflow.in

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References



49 votes

-- Rajarshi Sarkar (27.9k points)



✓ (B) is the correct answer.

Once we add G , the leaf node becomes $B G H I$, since we can have only 3 keys. the node has to split at G or H , and G or H will be added to parent node.

Since P is the parent node in options 1 and 2, its evident the 3rd element i.e. H should be selected for splitting (because after adding any key from the leftmost child node, P becomes the 3rd element in the node)

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Now parent node becomes $H L P U$, select P as for splitting, and you get option B.

Hence, answer is B.

22 votes

-- ryan sequeira (3k points)



✓ Answer: C [classroom.gateoverflow.in](#)

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$$\begin{aligned}14(p - 1) + 6p &\leq 512 \\20p - 14 &\leq 512 \\20p &\leq 526 \\ \text{Therefore, } p &= 26.\end{aligned}$$

👍 32 votes

-- Rajarshi Sarkar (27.9k points)



✓ Answer: D

- A. Cannot compare both the trees solely on basis of this.
- B. Both trees are BST.
- C. False. High fanout in B+ ensures that it takes more memory than BST.
- D. True. Records are stored in disk blocks.

👍 40 votes

-- Rajarshi Sarkar (27.9k points)



✓ The answer is **option A.**

$$B_p + P(R_p + \text{Key}) \leq \text{BlockSize}$$

$$\implies 1 \times 6 + n(7 + 9) \leq 1024$$

$$\implies n \leq 63.625.$$

So, 63 is the answer.

👍 62 votes

-- Gate Keeda (15.9k points)



✓ **Total 5 splitting** will occur during 10 successive insertions

Let's take 10 successive key values as $\{1, 2, 3, \dots, 10\}$ which can cause maximum possible splits.

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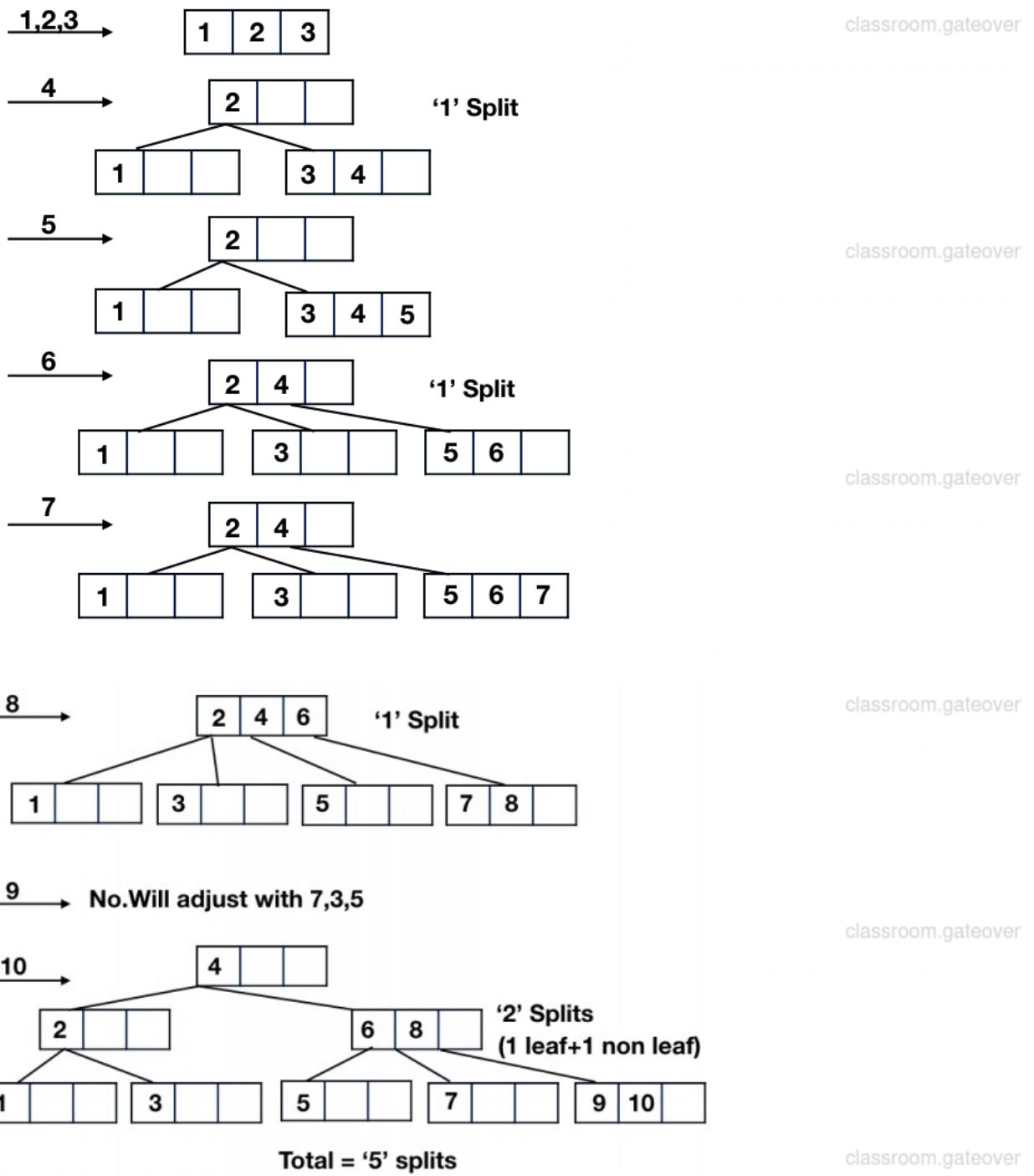
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60 votes

-- Prateek kumar (6.7k points)



- In this question they have asked only to count leaf node splits.

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So, after discussing with my friends on Facebook, I found that you will get two different answers depending on which convention you follow.

Convention 1: put the middle element in the left node, if you follow this you will get 4 as answer.

Convention 2: put the middle element in the right node, if you follow this you will get 3 as answer.

4 splits:

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1. after inserting 6
2. after inserting 4
3. after inserting 2 (there will be an internal node split and a leaf node split)
4. after inserting 1

Correct Answer: C

63 votes

-- Vikrant Singh (11.2k points)

3.1.18 B Tree: GATE CSE 2010 | Question: 18

<https://gateoverflow.in/2191>



- ✓ Answer: B

Order = $5+1 = 6$

Minimum children in a non root node = $\lceil \frac{Order}{2} \rceil = \lceil \frac{6}{2} \rceil = 3$

Keys = Minimum children in a non root node - 1 = 2

62 votes

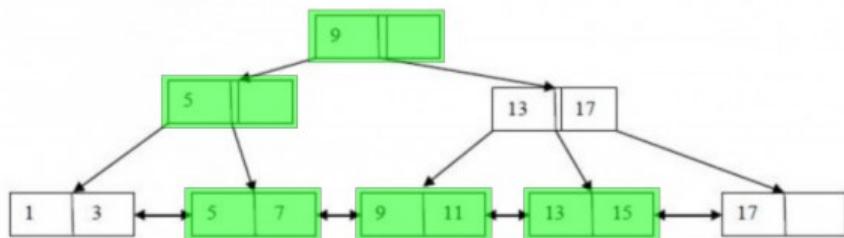
-- Rajarshi Sarkar (27.9k points)

3.1.19 B Tree: GATE CSE 2015 Set 2 | Question: 6

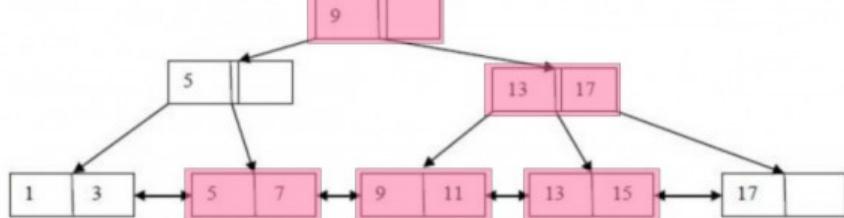
<https://gateoverflow.in/8052>



- ✓ whichever way you go from the root to leaves, you'll always end up counting 5 nodes.



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60 votes

-- Amar Vashishth (25.2k points)

3.1.20 B Tree: GATE CSE 2015 Set 3 | Question: 46

<https://gateoverflow.in/8555>



- ✓ $(n-1)12 + n \times 8 \leq 1024$

$n \leq 51$

In non leaf node number of keys = $n - 1$

$$= 51 - 1 = 50$$

63 votes

-- ppm (543 points)

✓ **Option A: In****B⁺ Tree all leaves are at same level.**

In both B Tree and B^+ trees, depth (length of root to leaf paths) of all leaf nodes is same. This is made sure by the insertion and deletion operations. In these trees, we do insertions in a way that if we have increase height of tree after insertion, we increase height from the root. This is different from BST where height increases from leaf nodes. Similarly, if we have to decrease height after deletion, we move the root one level down. This is also different from BST which shrinks from the bottom. The above ways of insertion and deletion make sure that depth of every leaf node is same.

41 votes

-- ukn (543 points)



✓ Let order of B^+ tree is p then maximum number of child pointers = p and maximum number of keys = $p - 1$.

To accommodate all child pointers and search key, total size of these together can not exceed 512 bytes.

$$2(p) + 8(p - 1) \leq 512$$

$$\Rightarrow p \leq 52$$

Therefore, maximum order must be 52.

52 votes

-- Sachin Mittal (15.8k points)

✓ Properties of B^+ trees:

1. B^+ tree is height balance tree.
2. Key value is in sorted order.
3. Leaf node has pointer to next leaf node.
4. Non leaf node has pointer to a node (leaf or non leaf) and not pointer to data record.

Option B is not correct.

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26 votes

-- Digvijay (44.9k points)



✓ It is 23.

$$(p - 1)(\text{key_ptr_size} + \text{record_ptr_size}) + p \cdot (\text{block_ptr_size}) \leq 512$$

$$\Rightarrow (p - 1)(10 + 8) + p \times 5 \leq 512$$

$$\Rightarrow 23p \leq 530$$

$$\Rightarrow p \leq 23.04$$

So, maximum value of p possible will be 23.

42 votes

-- Sandeep_Unyal (6.5k points)



✓ Suppose all nodes are completely full means every node has $n - 1$ keys. tree has 4 levels if a new key is inserted then at every level there will be created a new node. and in worst case root node will also be broken into two parts. and we have 4 levels so, answer should be 5 because tree will be increased with one more level.

Correct Answer: A

79 votes

-- Manu Thakur (34k points)



✓ Answer is (C).

From the structure of $B+$ tree we can get this equation:

$$n \times p + (n - 1) \times k \leq B \text{ (for non leaf node)}$$

Here, n=order, p=tree/block/index pointer, B=size of block

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I non leaf node no record pointer is there in $B+$ tree.

$$\text{So, } n \times p + (n - 1)k \leq B$$

$$n \times 6 + (n - 1) \times 9 \leq 512$$

$$\implies n \leq 34.77$$

Largest possible value for n is 34.

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1 35 votes

-- jayendra (6.7k points)

3.1.27 B Tree: GATE IT 2007 | Question: 84 top 5

<https://gateoverflow.in/3536>



✓ Option (A) is correct.

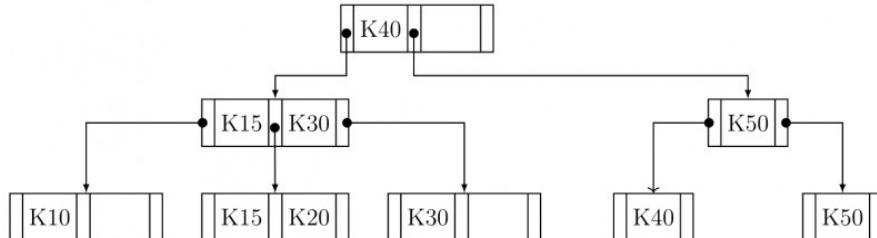
It is a B^+ Tree.

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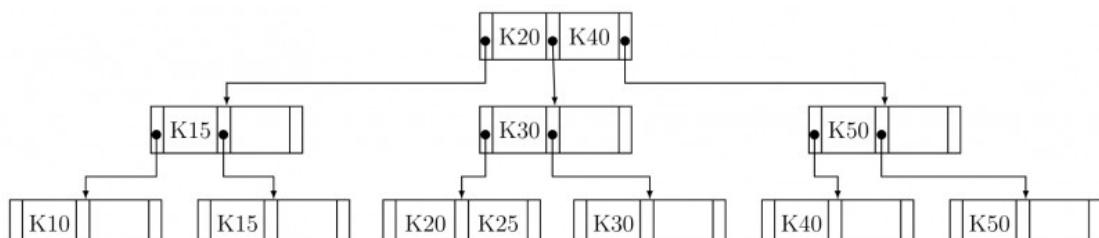
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After inserting K_{15} we get



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Now, we insert K_{25} , which gives -



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So, we see in the final tree only (K_{20}, K_{25}) is present. Hence, 1 (Ans).

1 55 votes

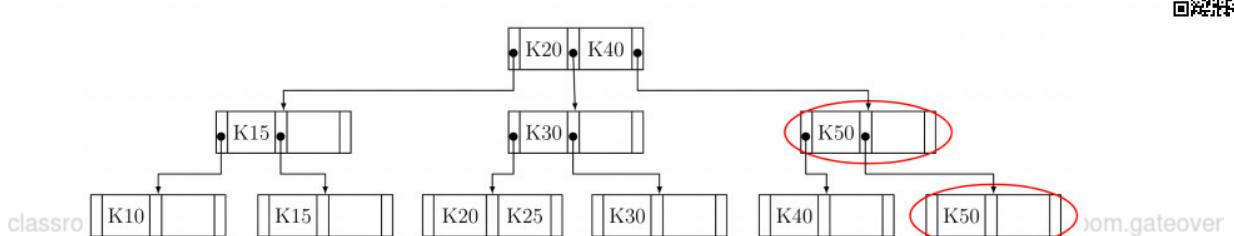
-- Himanshu Agarwal (12.4k points)

3.1.28 B Tree: GATE IT 2007 | Question: 85 top 5

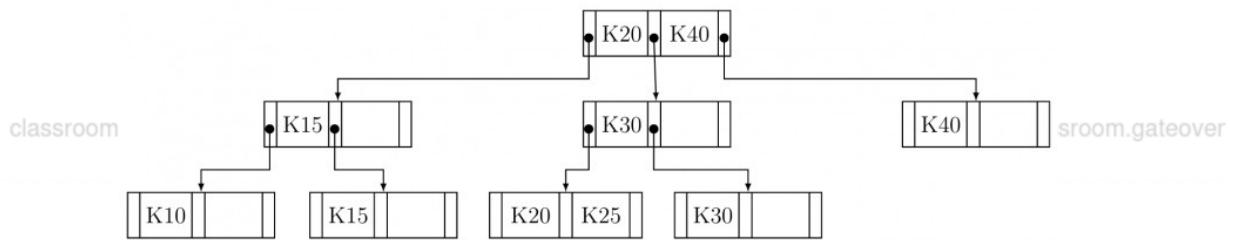
<https://gateoverflow.in/3537>



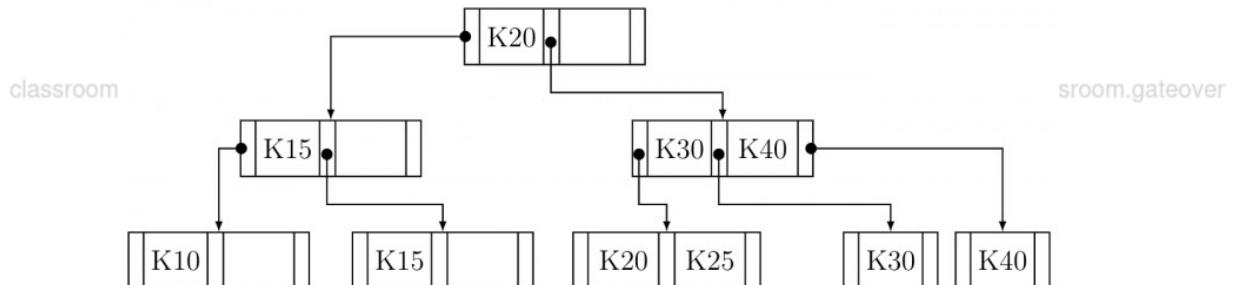
✓



Now merge 40 in upper level.



Now redistribute:



So, the answer is A.

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-- srestha (85.2k points)

139 votes

3.2

Candidate Keys (5) [top](#)

3.2.1 Candidate Keys: GATE CSE 1994 | Question: 3.7 [top](#)

<https://gateoverflow.in/2493>



An instance of a relational scheme $R(A, B, C)$ has distinct values for attribute A . Can you conclude that A is a candidate key for R ? tests.gatecse.in goclasses.in tests.gatecse.in

[gate1994](#)

[databases](#)

[easy](#)

[database-normalization](#)

[candidate-keys](#)

[descriptive](#)

Answer

3.2.2 Candidate Keys: GATE CSE 2011 | Question: 12 [top](#)

<https://gateoverflow.in/2114>



Consider a relational table with a single record for each registered student with the following attributes:

1. Registration_Num: Unique registration number for each registered student tests.gatecse.in
2. UID: Unique identity number, unique at the national level for each citizen
3. BankAccount_Num: Unique account number at the bank. A student can have multiple accounts or joint accounts. This attribute stores the primary account number.
4. Name: Name of the student
5. Hostel_Room: Room number of the hostel

Which of the following options is **INCORRECT**?

- A. BankAccount_Num is a candidate key
- B. Registration_Num can be a primary key goclasses.in tests.gatecse.in
- C. UID is a candidate key if all students are from the same country
- D. If S is a superkey such that $S \cap \text{UID}$ is NULL then $S \cup \text{UID}$ is also a superkey

[gate2011-cse](#)

[databases](#)

[normal](#)

[candidate-keys](#)

Answer

3.2.3 Candidate Keys: GATE CSE 2014 Set 2 | Question: 21 [top](#)

<https://gateoverflow.in/1978>



The maximum number of superkeys for the relation schema $R(E, F, G, H)$ with E as the key is _____. [numerical-answers](#)

[gate2014-cse-set2](#)

[databases](#)

[numerical-answers](#)

[easy](#)

[candidate-keys](#)

Answer



Given an instance of the STUDENTS relation as shown as below

StudentID	StudentName	StudentEmail	StudentAge	CPI
2345	Shankar	shankar@math	X	9.4
1287	Swati	swati@ee	19	9.5
7853	Shankar	shankar@cse	19	9.4
9876	Swati	swati@mech	18	9.3
8765	Ganesh	ganesh@civil	19	8.7

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For (StudentName, StudentAge) to be a key for this instance, the value X should NOT be equal to _____.

[gate2014-cse-set2](#) [databases](#) [numerical-answers](#) [easy](#) [candidate-keys](#)

Answer



A prime attribute of a relation scheme R is an attribute that appears

- A. in all candidate keys of R
- B. in some candidate key of R
- C. in a foreign key of R
- D. only in the primary key of R

[gate2014-cse-set3](#) [databases](#) [easy](#) [candidate-keys](#)

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Answer

Answers: Candidate Keys



✓ No.

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A	B	C
1	5	6
2	4	7
3	4	5

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Suppose this is the relational instance at any point of time.

Now we can see that $A \rightarrow BC$ holds for this instance, hence $A^+ = \{A, B, C\}$. (For every unique value of A , values of B and C are distinct).

But FDs are defined on the schema and not on any instance. So, based on the state of any instance we cannot say what holds for schema (there can be other instances too for R). At the best we can say that $A \rightarrow BC$ MAY hold for R .

PS: If we have a single instance where $A \rightarrow BC$ is not holding, it is enough to say $A \rightarrow BC$ does not hold for the relation R .

👉 58 votes

-- Sourav Roy (2.9k points)



✓ Answer is (A)

A relation is given (**Registration_Num**, **UID**, **BankAccount_Num**, **Name**, **Hostel_Room**).

Now, **Registration_Num** is unique for each student. So with this, we can identify each student. Hence, this can be the primary key.

UID: It's an identification number for a person in a country. (Say you're in India and your **UID** is 0243. Someone in Pakistan

may also have the same **UID** as 0243). So, if all students are from India (that is, the same country) then their **UID** will be different and then **UID** will be a Candidate key.

If **S** is a super key then $S \cup \text{UID}$ will be a Super key. e.g. **R(A, B, C, D)**, If **AB** is a superkey then **ABC, ABCD** are also superkey.

BankAccount_Num is not a candidate key, because a student can have multiple accounts or joint accounts. We can not identify each student uniquely with **BankAccount_Num**.

1 56 votes

-- Pranay Datta (7.8k points)

3.2.3 Candidate Keys: GATE CSE 2014 Set 2 | Question: 21 top

→ <https://gateoverflow.in/1978>



- ✓ Super Key is any set of attributes that uniquely determines a tuple in a relation.

Since **E** is **the only key**, **E** should be present in any super key.

Excluding **E**, there are three attributes in the relation, namely **F, G, H**. Hence, if we add **E** to any subset of those three attributes, then the resulting set is a super key. Number of subsets of $\{F, G, H\}$ is 8. **Hence the answer is**

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The following are Super Keys:

$$\left\{ \begin{array}{l} E \\ EF \\ EG \\ EH \\ EFG \\ EFH \\ EGH \\ EFGH \end{array} \right\}$$

1 50 votes

-- Sankaranarayanan P.N (8.5k points)

3.2.4 Candidate Keys: GATE CSE 2014 Set 2 | Question: 22 top

→ <https://gateoverflow.in/1980>



- ✓ Should not equal to 19.

Since if it is equal the same key will have two different values for "StudentEmail" which cannot be true by the definition of candidate/primary/super key.

1 43 votes

-- Aravind (2.8k points)

3.2.5 Candidate Keys: GATE CSE 2014 Set 3 | Question: 22 top

→ <https://gateoverflow.in/2056>



- ✓ Answer (B).

The attributes of a candidate key are called the prime attributes. Suppose **ABC** is one candidate key of a Relation **R(ABCDEFGH)**. Then the attributes **A, B** and **C** all are prime attributes. Similarly if **ABD** is also another candidate key in the same relation **R**, then **D** is also a prime attribute. And conversely, an attribute that does not occur in ANY candidate key is called a non-prime attribute.

1 18 votes

-- Divya Bharti (8.8k points)

3.3

Conflict Serializable (3) top

3.3.1 Conflict Serializable: GATE CSE 2017 Set 2 | Question: 44 top

→ <https://gateoverflow.in/118640>



Two transactions T_1 and T_2 are given as

$T_1 : r_1(X)w_1(X)r_1(Y)w_1(Y)$

$T_2 : r_2(Y)w_2(Y)r_2(Z)w_2(Z)$

where $r_i(V)$ denotes a *read* operation by transaction T_i on a variable V and $w_i(V)$ denotes a *write* operation by transaction T_i on a variable V . The total number of conflict serializable schedules that can be formed by T_1 and T_2 is _____

Answer ↗

3.3.2 Conflict Serializable: GATE CSE 2021 Set 1 | Question: 32 top ↗

↗ <https://gateoverflow.in/357419>



Let $r_i(z)$ and $w_i(z)$ denote read and write operations respectively on a data item z by a transaction T_i . Consider the following two schedules.

- $S_1 : r_1(x)r_1(y)r_2(x)r_2(y)w_2(y)w_1(x)$
- $S_2 : r_1(x)r_2(x)r_2(y)w_2(y)r_1(y)w_1(x)$

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Which one of the following options is correct?

- A. S_1 is conflict serializable, and S_2 is not conflict serializable
- B. S_1 is not conflict serializable, and S_2 is conflict serializable
- C. Both S_1 and S_2 are conflict serializable
- D. Neither S_1 nor S_2 is conflict serializable

gate2021-cse-set1 ↗ databases ↗ transaction-and-concurrency ↗ conflict-serializable

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Answer ↗

3.3.3 Conflict Serializable: GATE CSE 2021 Set 2 | Question: 32 top ↗

↗ <https://gateoverflow.in/357508>



Let S be the following schedule of operations of three transactions T_1 , T_2 and T_3 in a relational database system:

$$R_2(Y), R_1(X), R_3(Z), R_1(Y)W_1(X), R_2(Z), W_2(Y), R_3(X), W_3(Z)$$

Consider the statements P and Q below:

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- P : S is conflict-serializable.
- Q : If T_3 commits before T_1 finishes, then S is recoverable.

Which one of the following choices is correct?

- A. Both P and Q are true
- B. P is true and Q is false
- C. P is false and Q is true
- D. Both P and Q are false

gate2021-cse-set2 ↗ databases ↗ transaction-and-concurrency ↗ conflict-serializable

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Answer ↗

Answers: Conflict Serializable

3.3.1 Conflict Serializable: GATE CSE 2017 Set 2 | Question: 44 top ↗

↗ <https://gateoverflow.in/118640>



- ✓ There is only one way to have (conflict) serializable schedule as $T_1 \rightarrow T_2$, because last operation of T_1 and first operation of T_2 conflicts each other.

Now See How many schedules are conflict serializable to $T_2 \rightarrow T_1$.

I am writing T_1 –

$$R(A) \quad W(A) \quad R(B) \quad W(B)$$

If you notice, I wrote T_1 with space in between operation.

Now See T_2 from right, if we see T_2 from right, then tell me first operation of T_2 that conflicts with any operation of T_1 .

$W(C)$ and $R(C)$ do not have any conflict with any operation, but $W(B)$ has.

Pick $W(B)$ and see, at how many places it can be there.

Case1: $W(B) \quad R(A) \quad W(A) \quad R(B) \quad W(B)$

Case2: $R(A) \quad W(B) \quad W(A) \quad R(B) \quad W(B)$

Case3: $R(A) \quad W(A) \quad W(B) \quad R(B) \quad W(B)$

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Pick each case and see, how many positions other operation of T_2 can take.

Case1: $\mathbf{W(B)}$ $R(A)$ $W(A)$ $R(B)$ $W(B)$

How many positions $W(C)$ and $R(C)$ can take ?

(note that these $W(C)$ and $R(C)$ cant come before $\mathbf{W(B)}$)

that is $5C1 + 5C2 = 15$ (either both can take same space or two different spaces)

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Now see, for each of these 15 positions, how many can $R(B)$ take ?

Obliviously $R(B)$ cant come before $W(B)$ therefore one position.

$15 \times 1 = 15$ total possible schedules from case 1.

Case2: $R(A)$ $\mathbf{W(B)}$ $W(A)$ $R(B)$ $W(B)$

How many positions $W(C)$ and $R(C)$ can take ?

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that is $4C1 + 4C2 = 10$ (either both can take same space or two different spaces)

Now see, for each of these 10 positions, how many can $R(B)$ take ?

Only 2 positions, because it has to come before $\mathbf{W(B)}$.

$10 \times 2 = 20$ total possible schedules from case 2.

Case3: $R(A)$ $W(A)$ $\mathbf{W(B)}$ $R(B)$ $W(B)$

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How many positions $W(C)$ and $R(C)$ can take ?

that is $3C1 + 3C2 = 6$

Now see, for each of these 6 positions, how many can $R(B)$ take ?

Only 3 positions, because it has to come before $\mathbf{W(B)}$.

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$6 \times 3 = 18$ total possible schedules from case 3.

total schedules that are conflict serializable as $T2 \rightarrow T1 = 15 + 20 + 18 = 53$.

total schedules that are conflict serializable as $T1 \rightarrow T2 = 1$.

total schedules that are conflict serializable as either $T2 \rightarrow T1$ or $T1 \rightarrow T2 = 53 + 1 = 54$.

158 votes

– Sachin Mittal (15.8k points)

3.3.2 Conflict Serializable: GATE CSE 2021 Set 1 | Question: 32 top

<https://gateoverflow.in/357419>



T_1	T_2
$r_1(x)$	
$r_1(y)$	
	$r_2(x)$
	$r_2(y)$
	$w_2(y)$
$w_1(x)$	

Here $r_1(y)$ and $w_2(y)$ are conflicting pairs, giving $T_1 \rightarrow T_2$ and $r_2(x)$ and $w_1(x)$ giving $T_2 \rightarrow T_1$, so the schedule is not conflict serializable.

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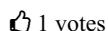
T₁	T₂
$r_1(x)$	
	$r_2(x)$
	$r_2(y)$
$w_2(y)$	gateoverflow.in
$r_1(y)$	
$w_1(x)$	

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Here $r_2(x)$ and $w_2(y)$ are conflicting pairs giving $T_2 \rightarrow T_1$, and $w_2(y)$ and $r_1(y)$ also giving $T_2 \rightarrow T_1$, therefore this schedule is conflict serializable.

Correct Option B



1 votes

-- zxy123 (2.8k points)

3.3.3 Conflict Serializable: GATE CSE 2021 Set 2 | Question: 32 top

<https://gateoverflow.in/357508>

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T₁	T₂	T₃
$R(X)$	$R(Y)$	
$R(Y)$		$R(Z)$
$W(X)$	$R(Z)$	
	$W(Y)$	$R(X)$
		$W(Z)$

- $T_1 \rightarrow T_2$ due to $R_1(Y)$ being before $W_2(Y)$
- $T_1 \rightarrow T_3$ due to $W_1(X)$ being before $R_3(X)$
- $T_2 \rightarrow T_3$ due to $R_2(Z)$ is being $W_3(Z)$ in the schedule.

There are no other conflicts and the discovered conflicts are not forming the cycle.

Therefore, the given schedule is Conflict Serializable.

Statement Q : If T_3 commits, before T_1 finishes, then S is recoverable.

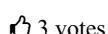


Schedule S is recoverable, if T_j creating the dirty read by reading the written data by T_i and T_j commits after T_i commits.

ver

By the above definition, Q is wrong.

Option B is correct.



3 votes

-- Shaik Masthan (50.4k points)

3.4

Data Independence (1) top

3.4.1 Data Independence: GATE CSE 1994 | Question: 3.11 top

<https://gateoverflow.in/2497>

State True or False with reason

Logical data independence is easier to achieve than physical data independence.

tags: gate1994, databases, normal, data-independence, true-false

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Answer

Answers: Data Independence



✓ classroom.gateoverflow.in
This is **False**.

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Generally, physical data independence exists in most databases and file environments where physical details are hidden from the user and applications remain unaware of these details. On the other hand, logical data independence is harder to achieve because of a much stricter requirement - it allows structural and constraint changes without affecting application programs.

[27 votes](#)

-- Akash Kanase (36k points)

3.5

Database Normalization (49) [top](#)

State whether the following statements are TRUE or FALSE:

A relation r with schema (X, Y) satisfies the function dependency $X \rightarrow Y$, The tuples $\langle 1, 2 \rangle$ and $\langle 2, 2 \rangle$ can both be in r simultaneously.

gate1987 databases database-normalization true-false

goclasses.intests.gatecse.in[Answer](#)

What are the three axioms of functional dependency for the relational databases given by Armstrong.

gate1988 normal descriptive databases database-normalization

[Answer](#)

Using Armstrong's axioms of functional dependency derive the following rules:

$$\{x \rightarrow y, x \rightarrow z\} \models x \rightarrow yz$$

(Note: $x \rightarrow y$ denotes y is functionally dependent on x , $z \subseteq y$ denotes z is subset of y , and \models means derives).

gate1988 easy descriptive databases database-normalization

goclasses.intests.gatecse.in[Answer](#)

Using Armstrong's axioms of functional dependency derive the following rules:

$$\{x \rightarrow y, wy \rightarrow z\} \models xw \rightarrow z$$

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(Note: $x \rightarrow y$ denotes y is functionally dependent on x , $z \subseteq y$ denotes z is subset of y , and \models means derives).

gate1988 normal descriptive databases database-normalization

[Answer](#)

Using Armstrong's axioms of functional dependency derive the following rules:

$$\{x \rightarrow y, z \subset y\} \models x \rightarrow z$$

(Note: $x \rightarrow y$ denotes y is functionally dependent on x , $z \subseteq y$ denotes z is subset of y , and \models means derives).

gate1988 normal descriptive databases database-normalization

Answer 

3.5.6 Database Normalization: GATE CSE 1990 | Question: 2-iv top

<https://gateoverflow.in/83977>



Match the pairs in the following questions:

(a)	Secondary index	(p)	Function dependency
(b)	Non-procedural query language	(q)	B-tree
(c)	Closure of a set of attributes	(r)	Domain calculus
(d)	Natural join	(s)	Relational algebraic operations

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gate1990 match-the-following database-normalization databases

Answer 

3.5.7 Database Normalization: GATE CSE 1990 | Question: 3-ii top

<https://gateoverflow.in/84054>



Indicate which of the following statements are true:

A relational database which is in 3NF may still have undesirable data redundancy because there may exist:

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- A. Transitive functional dependencies
- B. Non-trivial functional dependencies involving prime attributes on the right-side.
- C. Non-trivial functional dependencies involving prime attributes only on the left-side.
- D. Non-trivial functional dependencies involving only prime attributes.

gate1990 normal databases database-normalization multiple-selects

Answer 

3.5.8 Database Normalization: GATE CSE 1994 | Question: 3.6 top

<https://gateoverflow.in/2492>



State True or False with reason

There is always a decomposition into Boyce-Codd normal form (BCNF) that is lossless and dependency preserving.

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gate1994 databases database-normalization easy true-false

Answer 

3.5.9 Database Normalization: GATE CSE 1995 | Question: 26 top

<https://gateoverflow.in/2665>



Consider the relation scheme $R(A, B, C)$ with the following functional dependencies:

- $A, B \rightarrow C$,
- $C \rightarrow A$

- A. Show that the scheme R is in 3NF but not in BCNF.
- B. Determine the minimal keys of relation R .

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gate1995 databases database-normalization normal descriptive

Answer 

3.5.10 Database Normalization: GATE CSE 1997 | Question: 6.9 top

<https://gateoverflow.in/2265>



For a database relation $R(a, b, c, d)$, where the domains a, b, c, d include only atomic values, only the following functional dependencies and those that can be inferred from them hold

- $a \rightarrow c$
- $b \rightarrow d$

This relation is

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- A. in first normal form but not in second normal form
 B. in second normal form but not in first normal form
 C. in third normal form
 D. none of the above

gate1997 databases database-normalization normal

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Answer ↗

3.5.11 Database Normalization: GATE CSE 1998 | Question: 1.34 top ↵



Which normal form is considered adequate for normal relational database design?

- A. 2NF
 B. 5NF
 C. 4NF
 D. 3NF

gate1998 databases database-normalization easy

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Answer ↗

3.5.12 Database Normalization: GATE CSE 1998 | Question: 26 top ↵



Consider the following database relations containing the attributes

- Book_id
- Subject_Category_of_book
- Name_of_Author
- Nationality_of_Author

With Book_id as the primary key.

- What is the highest normal form satisfied by this relation?
- Suppose the attributes Book_title and Author_address are added to the relation, and the primary key is changed to {Name_of_Author, Book_title}, what will be the highest normal form satisfied by the relation?

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gate1998 databases database-normalization normal descriptive

Answer ↗

3.5.13 Database Normalization: GATE CSE 1999 | Question: 1.24 top ↵



Let $R = (A, B, C, D, E, F)$ be a relation scheme with the following dependencies $C \rightarrow F, E \rightarrow A, EC \rightarrow D, A \rightarrow B$. Which one of the following is a key for R ?

- A. CD
 B. EC
 C. AE
 D. AC

gate1999 databases database-normalization easy

Answer ↗

3.5.14 Database Normalization: GATE CSE 1999 | Question: 2.7, UGCNET-June2014-III: 25 top ↵



Consider the schema $R = (S, T, U, V)$ and the dependencies $S \rightarrow T, T \rightarrow U, U \rightarrow V$ and $V \rightarrow S$. Let $R = (R1 \text{ and } R2)$ be a decomposition such that $R1 \cap R2 \neq \emptyset$. The decomposition is

- A. not in 2NF
 B. in 2NF but not 3NF
 C. in 3NF but not in 2NF
 D. in both 2NF and 3NF

Answer 3.5.15 Database Normalization: GATE CSE 2000 | Question: 2.24 top<https://gateoverflow.in/671>

Given the following relation instance.

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X	Y	Z
1	4	2
1	5	3
1	6	3
3	2	2

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Which of the following functional dependencies are satisfied by the instance?

- A. $XY \rightarrow Z$ and $Z \rightarrow Y$
- B. $YZ \rightarrow X$ and $Y \rightarrow Z$
- C. $YZ \rightarrow X$ and $X \rightarrow Z$
- D. $XZ \rightarrow Y$ and $Y \rightarrow X$

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Answer 3.5.16 Database Normalization: GATE CSE 2001 | Question: 2.23 top<https://gateoverflow.in/741> $R(A, B, C, D)$ is a relation. Which of the following does not have a lossless join, dependency preserving BCNF decomposition?

- A. $A \rightarrow B, B \rightarrow CD$
- B. $A \rightarrow B, B \rightarrow C, C \rightarrow D$
- C. $AB \rightarrow C, C \rightarrow AD$
- D. $A \rightarrow BCD$

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Answer 3.5.17 Database Normalization: GATE CSE 2002 | Question: 1.19 top<https://gateoverflow.in/824>Relation R with an associated set of functional dependencies, F , is decomposed into BCNF. The redundancy (arising out of functional dependencies) in the resulting set of relations is

- A. Zero tests.gatecse.in
- B. More than zero but less than that of an equivalent 3NF decomposition
- C. Proportional to the size of F^+
- D. Indeterminate

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Answer 3.5.18 Database Normalization: GATE CSE 2002 | Question: 16 top<https://gateoverflow.in/869>For relation $R=(L, M, N, O, P)$, the following dependencies hold:

$$M \rightarrow O, NO \rightarrow P, P \rightarrow L \text{ and } L \rightarrow MN$$

R is decomposed into $R_1 = (L, M, N, P)$ and $R_2 = (M, O)$.

- A. Is the above decomposition a lossless-join decomposition? Explain.
- B. Is the above decomposition dependency-preserving? If not, list all the dependencies that are not preserved.
- C. What is the highest normal form satisfied by the above decomposition?

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Answer 3.5.19 Database Normalization: GATE CSE 2002 | Question: 2.24 top ↺<https://gateoverflow.in/854>

Relation R is decomposed using a set of functional dependencies, F , and relation S is decomposed using another set of functional dependencies, G . One decomposition is definitely BCNF, the other is definitely $3NF$, but it is not known which is which. To make a guaranteed identification, which one of the following tests should be used on the decompositions? (Assume that the closures of F and G are available).

- A. Dependency-preservation
- B. Lossless-join
- C. BCNF definition
- D. $3NF$ definition

Answer 3.5.20 Database Normalization: GATE CSE 2002 | Question: 2.25 top ↺<https://gateoverflow.in/855>

From the following instance of a relation schema $R(A, B, C)$, we can conclude that:

A	B	C
1	1	1
1	1	0
2	3	2
2	3	2

- A. A functionally determines B and B functionally determines C
- B. A functionally determines B and B does not functionally determine C
- C. B does not functionally determine C
- D. A does not functionally determine B and B does not functionally determine C

Answer 3.5.21 Database Normalization: GATE CSE 2003 | Question: 85 top ↺<https://gateoverflow.in/368>

Consider the following functional dependencies in a database.

Date_of_Birth \rightarrow Age	Age \rightarrow Eligibility
Name \rightarrow Roll_number	Roll_number \rightarrow Name
Course_number \rightarrow Course_name	Course_number \rightarrow Instructor
(Roll_number, Course_number) \rightarrow Grade	

The relation (Roll_number, Name, Date_of_birth, Age) is

- A. in second normal form but not in third normal form
- B. in third normal form but not in BCNF
- C. in BCNF
- D. in none of the above

Answer 3.5.22 Database Normalization: GATE CSE 2004 | Question: 50 top ↺<https://gateoverflow.in/1046>

The relation scheme Student Performance (name, courseNo, rollNo, grade) has the following functional dependencies:

- name, courseNo, \rightarrow grade
- rollNo, courseNo \rightarrow grade
- name \rightarrow rollNo
- rollNo \rightarrow name

The highest normal form of this relation scheme is

- A. 2NF
B. 3NF
C. BCNF
D. 4NF

gate2004-cse databases database-normalization normal

Answer ↗

3.5.23 Database Normalization: GATE CSE 2005 | Question: 29, UGCNET-June2015-III: 9 top ↗

tests.gatecse.in ↗ https://gateoverflow.in/1365



Which one of the following statements about normal forms is FALSE?

- A. BCNF is stricter than 3NF
B. Lossless, dependency-preserving decomposition into 3NF is always possible
C. Lossless, dependency-preserving decomposition into BCNF is always possible
D. Any relation with two attributes is in BCNF

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gate2005-cse databases database-normalization easy ugcnetjune2015iii

Answer ↗

3.5.24 Database Normalization: GATE CSE 2005 | Question: 78 top ↗

tests.gatecse.in ↗ https://gateoverflow.in/1401



Consider a relation scheme $R = (A, B, C, D, E, H)$ on which the following functional dependencies hold: $\{A \rightarrow B, BC \rightarrow D, E \rightarrow C, D \rightarrow A\}$. What are the candidate keys R?

- A. AE, BE
B. AE, BE, DE
C. AEH, BEH, BCH
D. AEH, BEH, DEH

gate2005-cse databases database-normalization easy

Answer ↗

3.5.25 Database Normalization: GATE CSE 2006 | Question: 70 top ↗

tests.gatecse.in ↗ https://gateoverflow.in/1848



The following functional dependencies are given:

$$AB \rightarrow CD, AF \rightarrow D, DE \rightarrow F, C \rightarrow G, F \rightarrow E, G \rightarrow A$$

Which one of the following options is false?

- A. $\{CF\}^* = \{ACDEFG\}$
B. $\{BG\}^* = \{ABCDG\}$
C. $\{AF\}^* = \{ACDEFG\}$
D. $\{AB\}^* = \{ABCDG\}$

gate2006-cse databases database-normalization normal

Answer ↗

3.5.26 Database Normalization: GATE CSE 2007 | Question: 62, UGCNET-June2014-II: 47 top ↗

tests.gatecse.in ↗ https://gateoverflow.in/1260



Which one of the following statements is FALSE?

- A. Any relation with two attributes is in BCNF
 B. A relation in which every key has only one attribute is in 2NF
 C. A prime attribute can be transitively dependent on a key in a 3 NF relation
 D. A prime attribute can be transitively dependent on a key in a BCNF relation

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gate2007-cse databases database-normalization normal ugcnetjune2014ii

Answer 

3.5.27 Database Normalization: GATE CSE 2008 | Question: 69 top ↗

↗ <https://gateoverflow.in/492>



Consider the following relational schemes for a library database:
 Book (Title, Author, Catalog_no, Publisher, Year, Price)
 Collection (Title, Author, Catalog_no)

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with the following functional dependencies:

- I. Title Author → Catalog_no
- II. Catalog_no → Title Author Publisher Year
- III. Publisher Title Year → Price

Assume { Author, Title } is the key for both schemes. Which of the following statements is true?

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- A. Both Book and Collection are in BCNF
- B. Both Book and Collection are in 3NF only
- C. Book is in 2NF and Collection in 3NF
- D. Both Book and Collection are in 2NF only

gate2008-cse databases database-normalization normal

Answer 

3.5.28 Database Normalization: GATE CSE 2009 | Question: 56 top ↗

↗ <https://gateoverflow.in/43474>



Consider the following relational schema:

Suppliers(sid:integer, sname:string, city:string, street:string)

Parts(pid:integer, pname:string, color:string)

Catalog(sid:integer, pid:integer, cost:real)

Assume that, in the suppliers relation above, each supplier and each street within a city has unique name, and (sname, city) forms a candidate key. No other functional dependencies are implied other than those implied by primary and candidate keys. Which one of the following is TRUE about the above schema?

- A. The schema is in BCNF
- B. The schema is in 3NF but not in BCNF
- C. The schema is in 2NF but not in 3NF
- D. The schema is not in 2NF

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gate2009-cse databases sql database-normalization normal

Answer 

3.5.29 Database Normalization: GATE CSE 2012 | Question: 2 top ↗

↗ <https://gateoverflow.in/34>



Which of the following is TRUE?

- A. Every relation in 3NF is also in BCNF
- B. A relation R is in 3NF if every non-prime attribute of R is fully functionally dependent on every key of R
- C. Every relation in BCNF is also in 3NF
- D. No relation can be in both BCNF and 3NF

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Answer 3.5.30 Database Normalization: GATE CSE 2013 | Question: 54 top ↴<https://gateoverflow.in/1558>

Relation R has eight attributes ABCDEFGH. Fields of R contain only atomic values. $F = \{CH \rightarrow G, A \rightarrow BC, B \rightarrow CFH, E \rightarrow A, F \rightarrow EG\}$ is a set of functional dependencies (FDs) so that F^+ is exactly the set of FDs that hold for R .

How many candidate keys does the relation R have?

- A. 3 tests.gatecse.in
- B. 4 goclasses.in
- C. 5 tests.gatecse.in
- D. 6 tests.gatecse.in

Answer 3.5.31 Database Normalization: GATE CSE 2013 | Question: 55 top ↴<https://gateoverflow.in/43290>

Relation R has eight attributes ABCDEFGH. Fields of R contain only atomic values. $F = \{CH \rightarrow G, A \rightarrow BC, B \rightarrow CFH, E \rightarrow A, F \rightarrow EG\}$ is a set of functional dependencies (FDs) so that F^+ is exactly the set of FDs that hold for R .

The relation R is

- A. in $1NF$, but not in $2NF$. goclasses.in
- B. in $2NF$, but not in $3NF$. tests.gatecse.in
- C. in $3NF$, but not in $BCNF$. tests.gatecse.in
- D. in $BCNF$. tests.gatecse.in

Answer 3.5.32 Database Normalization: GATE CSE 2014 Set 1 | Question: 21 top ↴<https://gateoverflow.in/1788>

Consider the relation scheme $R = (E, F, G, H, I, J, K, L, M, N)$ and the set of functional dependencies

$$\{\{E, F\} \rightarrow \{G\}, \{F\} \rightarrow \{I, J\}, \{E, H\} \rightarrow \{K, L\}, \{K\} \rightarrow \{M\}, \{L\} \rightarrow \{N\}\}$$

on R . What is the key for R ?

- A. $\{E, F\}$ goclasses.in
- B. $\{E, F, H\}$ tests.gatecse.in
- C. $\{E, F, H, K, L\}$ tests.gatecse.in
- D. $\{E\}$ tests.gatecse.in

Answer 3.5.33 Database Normalization: GATE CSE 2014 Set 1 | Question: 30 top ↴<https://gateoverflow.in/1797>

Given the following two statements:

S1: Every table with two single-valued attributes is in $1NF$, $2NF$, $3NF$ and $BCNF$. tests.gatecse.in

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S2: $AB \rightarrow C, D \rightarrow E, E \rightarrow C$ is a minimal cover for the set of functional dependencies $AB \rightarrow C, D \rightarrow E, AB \rightarrow E, E \rightarrow C$.

Which one of the following is **CORRECT**?

- A. S1 is TRUE and S2 is FALSE. goclasses.in
- B. Both S1 and S2 are TRUE. tests.gatecse.in
- C. S1 is FALSE and S2 is TRUE. tests.gatecse.in
- D. Both S1 and S2 are FALSE. tests.gatecse.in

Answer **3.5.34 Database Normalization: GATE CSE 2015 Set 3 | Question: 20** top ↗<https://gateoverflow.in/8420>

Consider the relation $X(P, Q, R, S, T, U)$ with the following set of functional dependencies

$$F = \{ \{P, R\} \rightarrow \{S, T\}, \{P, S, U\} \rightarrow \{Q, R\} \}$$

Which of the following is the trivial functional dependency in F^+ , where F^+ is closure to F?

- A. $\{P, R\} \rightarrow \{S, T\}$
- B. $\{P, R\} \rightarrow \{R, T\}$
- C. $\{P, S\} \rightarrow \{S\}$
- D. $\{P, S, U\} \rightarrow \{Q\}$

Answer **3.5.35 Database Normalization: GATE CSE 2016 Set 1 | Question: 21** top ↗<https://gateoverflow.in/39637>

Which of the following is NOT a superkey in a relational schema with attributes

V, W, X, Y, Z and primary key
 $V Y?$

- A. $VXYZ$
- B. $VWXZ$
- C. $VWXY$
- D. $VWXYZ$

Answer **3.5.36 Database Normalization: GATE CSE 2016 Set 1 | Question: 23** top ↗<https://gateoverflow.in/39646>

A database of research articles in a journal uses the following schema.

(VOLUME, NUMBER, STARTPAGE, ENDPAGE, TITLE, YEAR, PRICE)

The primary key is '(VOLUME, NUMBER, STARTPAGE, ENDPAGE)

and the following functional dependencies exist in the schema.

$$\begin{array}{lcl} (\text{VOLUME}, \text{NUMBER}, \text{STARTPAGE}, \text{ENDPAGE}) & \rightarrow & \text{TITLE} \\ \text{tests}(\text{VOLUME}, \text{NUMBER}) & \rightarrow & \text{YEAR} \\ (\text{VOLUME}, \text{NUMBER}, \text{STARTPAGE}, \text{ENDPAGE}) & \rightarrow & \text{PRICE} \end{array}$$

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The database is redesigned to use the following schemas

(VOLUME, NUMBER, STARTPAGE, ENDPAGE, TITLE, PRICE)(VOLUME, NUMBER, YEAR)

Which is the weakest normal form that the new database satisfies, but the old one does not?

- A. 1NF
- B. 2NF
- C. 3NF
- D. BCNF

Answer 



The following functional dependencies hold true for the relational schema $R\{V, W, X, Y, Z\}$:

$$\begin{aligned} V &\rightarrow W \\ VW &\rightarrow X \\ Y &\rightarrow VX \\ Y &\rightarrow Z \end{aligned}$$

Which of the following is irreducible equivalent for this set of functional dependencies?

- A. $V \rightarrow W$
 $V \rightarrow X$
 $Y \rightarrow V$
 $Y \rightarrow Z$
- B. $V \rightarrow W$
 $W \rightarrow X$
 $Y \rightarrow V$
 $Y \rightarrow Z$
- C. $V \rightarrow W$
 $V \rightarrow X$
 $Y \rightarrow V$
 $Y \rightarrow X$
 $Y \rightarrow Z$
- D. $V \rightarrow W$
 $W \rightarrow X$
 $Y \rightarrow V$
 $Y \rightarrow X$
 $Y \rightarrow Z$

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Answer



Consider the following four relational schemas. For each schema , all non-trivial functional dependencies are listed, The **bolded** attributes are the respective primary keys.

Schema I: Registration(**rollno**, courses)

Field ‘courses’ is a set-valued attribute containing the set of courses a student has registered for.

Non-trivial functional dependency

$$\text{rollno} \rightarrow \text{courses}$$

Schema II: Registration (**rollno**, **coursid**, email)

Non-trivial functional dependencies:

$$\text{rollno}, \text{courseid} \rightarrow \text{email}$$

$$\text{email} \rightarrow \text{rollno}$$

Schema III: Registration (**rollno**, **courseid**, marks, grade)

Non-trivial functional dependencies:

$$\text{rollno}, \text{courseid}, \rightarrow \text{marks, grade}$$

$$\text{marks} \rightarrow \text{grade}$$

Schema IV: Registration (**rollno**, **courseid**, credit)

Non-trivial functional dependencies:

$$\text{rollno}, \text{courseid} \rightarrow \text{credit}$$

$$\text{courseid} \rightarrow \text{credit}$$

Which one of the relational schemas above is in 3NF but not in BCNF?

- A. Schema I
- B. Schema II
- C. Schema III
- D. Schema IV

Answer 3.5.39 Database Normalization: GATE CSE 2019 | Question: 32 [top](#)<https://gateoverflow.in/302816>

Let the set of functional dependencies $F = \{QR \rightarrow S, R \rightarrow P, S \rightarrow Q\}$ hold on a relation schema $X = (PQRS)$. X is not in BCNF. Suppose X is decomposed into two schemas Y and Z , where $Y = (PR)$ and $Z = (QRS)$.

Consider the two statements given below.

- I. Both Y and Z are in BCNF
- II. Decomposition of X into Y and Z is dependency preserving and lossless

Which of the above statements is/are correct?

- A. Both I and II
- B. I only
- C. II only
- D. Neither I nor II

Answer 3.5.40 Database Normalization: GATE CSE 2020 | Question: 36 [top](#)<https://gateoverflow.in/333195>

Consider a relational table R that is in $3NF$, but not in BCNF. Which one of the following statements is TRUE?

- A. R has a nontrivial functional dependency $X \rightarrow A$, where X is not a superkey and A is a prime attribute.
- B. R has a nontrivial functional dependency $X \rightarrow A$, where X is not a superkey and A is a non-prime attribute and X is not a proper subset of any key.
- C. R has a nontrivial functional dependency $X \rightarrow A$, where X is not a superkey and A is a non-prime attribute and X is a proper subset of some key.
- D. A cell in R holds a set instead of an atomic value.

Answer 3.5.41 Database Normalization: GATE CSE 2021 Set 1 | Question: 33 [top](#)<https://gateoverflow.in/357418>

Consider the relation $R(P, Q, S, T, X, Y, Z, W)$ with the following functional dependencies.

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$$PQ \rightarrow X; \quad P \rightarrow YX; \quad Q \rightarrow Y; \quad Y \rightarrow ZW$$

Consider the decomposition of the relation R into the constituent relations according to the following two decomposition schemes.

- $D_1 : R = [(P, QS, T); (P, T, X); (Q, Y); (Y, Z, W)]$
- $D_2 : R = [(P, Q, S); (T, X); (Q, Y); (Y, Z, W)]$

Which one of the following options is correct?

- A. D_1 is a lossless decomposition, but D_2 is a lossy decomposition
- B. D_1 is a lossy decomposition, but D_2 is a lossless decomposition
- C. Both D_1 and D_2 are lossless decompositions
- D. Both D_1 and D_2 are lossy decompositions

Answer 3.5.42 Database Normalization: GATE CSE 2021 Set 2 | Question: 40 [top](#)<https://gateoverflow.in/357500>

Suppose the following functional dependencies hold on a relation U with attributes P, Q, R, S , and T :

- $P \rightarrow QR$
- $RS \rightarrow T\$$

Which of the following functional dependencies can be inferred from the above functional dependencies?

- A. $PS \rightarrow T$
 B. $R \rightarrow T$
 C. $P \rightarrow R$
 D. $PS \rightarrow Q$

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gate2021-cse-set2 multiple-selects databases database-normalization

Answer 

3.5.43 Database Normalization: GATE IT 2004 | Question: 75 top ↺

<https://gateoverflow.in/3719>



A relation Empdtl is defined with attributes empcode (unique), name, street, city, state and pincode. For any pincode, there is only one city and state. Also, for any given street, city and state, there is just one pincode. In normalization terms, Empdtl is a relation in

- A. 1NF only
 B. 2NF and hence also in 1NF
 C. 3NF and hence also in 2NF and 1NF
 D. BCNF and hence also in 3NF, 2NF and 1NF

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gate2004-it databases database-normalization normal

Answer 

3.5.44 Database Normalization: GATE IT 2005 | Question: 22 top ↺

<https://gateoverflow.in/3767>



A table has fields F_1, F_2, F_3, F_4, F_5 with the following functional dependencies

- $F_1 \rightarrow F_3, F_2 \rightarrow F_4, (F_1, F_2) \rightarrow F_5$

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In terms of Normalization, this table is in

- A. 1 NF
 B. 2 NF
 C. 3 NF
 D. None of these

gate2005-it databases database-normalization easy

Answer 

3.5.45 Database Normalization: GATE IT 2005 | Question: 70 top ↺

<https://gateoverflow.in/3833>



In a schema with attributes A, B, C, D and E following set of functional dependencies are given

- $A \rightarrow B$
- $A \rightarrow C$
- $CD \rightarrow E$
- $B \rightarrow D$
- $E \rightarrow A$

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Which of the following functional dependencies is NOT implied by the above set?

- A. $CD \rightarrow AC$
 B. $BD \rightarrow CD$
 C. $BC \rightarrow CD$
 D. $AC \rightarrow BC$

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gate2005-it databases database-normalization normal

Answer 



Consider a relation R with five attributes V, W, X, Y , and Z . The following functional dependencies hold:

$$VY \rightarrow W, WX \rightarrow Z, \text{ and } ZY \rightarrow V.$$

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Which of the following is a candidate key for R ?

- A. VXZ
- B. VXY
- C. $VWXY$
- D. $VWXYZ$

[gate2006-it](#) [databases](#) [database-normalization](#) [normal](#)

Answer



Let $R(A, B, C, D)$ be a relational schema with the following functional dependencies :

$$A \rightarrow B, B \rightarrow C, C \rightarrow D \text{ and } D \rightarrow B.$$

- The decomposition of R into $(A, B), (B, C), (B, D)$
- A. gives a lossless join, and is dependency preserving
 - B. gives a lossless join, but is not dependency preserving
 - C. does not give a lossless join, but is dependency preserving
 - D. does not give a lossless join and is not dependency preserving

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[gate2008-it](#) [databases](#) [database-normalization](#) [normal](#)

Answer



Let $R(A, B, C, D, E, P, G)$ be a relational schema in which the following functional dependencies are known to hold: $AB \rightarrow CD, DE \rightarrow P, C \rightarrow E, P \rightarrow C$ and $B \rightarrow G$. The relational schema R is

- A. in BCNF
- B. in 3NF, but not in BCNF
- C. in 2NF, but not in 3NF
- D. not in 2NF

[gate2008-it](#) [databases](#) [database-normalization](#) [normal](#)

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Answer



Consider a schema $R(A, B, C, D)$ and functional dependencies $A \rightarrow B$ and $C \rightarrow D$. Then the decomposition of R into $R_1(A, B)$ and $R_2(C, D)$ is

- A. dependency preserving and lossless join
- B. lossless join but not dependency preserving
- C. dependency preserving but not lossless join
- D. not dependency preserving and not lossless join

[gate1998](#) [databases](#) [ugcnetjune2012iii](#) [database-normalization](#)

Answer

Answers: Database Normalization



✓ True is answer [gateoverflow.in](#)

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$X \rightarrow Y$ says when X repeats, Y will be also repeat. Since, X is not repeated, Y **may or may not** repeat.

X	Y
1	2
2	2

1 like 30 votes

-- Prashant Singh (47.2k points)

3.5.2 Database Normalization: GATE CSE 1988 | Question: 12i top

<https://gateoverflow.in/94398>



- ✓ 1. AXIOM OF REFLEXIVITY

If $Y \subseteq X$ then $X \rightarrow Y$

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- 2. AXIOM OF AUGMENTATION

If $X \rightarrow Y$ then $XZ \rightarrow YZ$ for any Z

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- 3. AXIOM OF TRANSITIVITY

If $X \rightarrow Y$ and $Y \rightarrow Z$ then $X \rightarrow Z$

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1 like 12 votes

-- Aashish (1.8k points)

3.5.3 Database Normalization: GATE CSE 1988 | Question: 12iiia top

<https://gateoverflow.in/94399>



- ✓ $x \rightarrow z$ (Given)

$\Rightarrow xx \rightarrow zx$ (Axiom of augmentation) $\rightarrow (I)$

Also $x \rightarrow y$ (Given)

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$\Rightarrow xz \rightarrow yz$ (Axiom of augmentation) $\rightarrow (II)$

Using (I) and (II) we get

$xx \rightarrow yz$ (Axiom of transitivity)

$\Rightarrow x \rightarrow yz$

1 like 9 votes

-- Satbir Singh (21k points)

3.5.4 Database Normalization: GATE CSE 1988 | Question: 12iib top

<https://gateoverflow.in/94618>



- ✓ $x \rightarrow y$ (Given)

$\Rightarrow xw \rightarrow yw$ (using axiom of augmentation $A \rightarrow B \Rightarrow AX \rightarrow BX$)

also $yw \rightarrow z$ (Given)

$\Rightarrow xw \rightarrow z$ (using Axiom of transitivity ($A \rightarrow B$ and $B \rightarrow C$) $\Rightarrow A \rightarrow C$)

1 like 5 votes

-- Satbir Singh (21k points)

3.5.5 Database Normalization: GATE CSE 1988 | Question: 12iic top

<https://gateoverflow.in/94619>



- ✓ $\because z \subset y$, Trivially $y \rightarrow z$. Now by transitivity, $x \rightarrow y, y \rightarrow z \Rightarrow x \rightarrow z$

1 like 6 votes

-- Arkaprava Paul (1.9k points)

3.5.6 Database Normalization: GATE CSE 1990 | Question: 2-iv top

<https://gateoverflow.in/83977>



- ✓ Secondary index \Rightarrow B-tree

Non-procedural query language \Rightarrow Domain calculus

Closure of a set of attributes \Rightarrow Function dependency

Natural join \Rightarrow Relational algebraic operations

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(a)	Secondary index	(q)	B-tree
(b)	Non-procedural query language	(r)	Domain calculus
(c)	Closure of a set of attributes	(p)	Function dependency
(d)	Natural join	(s)	Relational algebraic operations

-- Pankaj Kumar (7.8k points)

3.5.7 Database Normalization: GATE CSE 1990 | Question: 3-ii top ↗

<https://gateoverflow.in/84054>



A . Transitive functional dependency. Therefore it is not in 3NF

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B. 3NF because right side is prime attribute

C. Not in 3NF because let us suppose ABC is a candidate key (you can assume any candidate key with any no of attribute) . now consider AB \rightarrow non-prime attribute which shows it is not in 3NF

D. involving only prime attribute so the **Right** side should definitely contain only prime attribute. therefore it is in 3NF

so B, D is the answer

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Edited on 24th Nov 2020 by Gurdeep saini

10 votes

-- Gurdeep (6.8k points)

3.5.8 Database Normalization: GATE CSE 1994 | Question: 3.6 top ↗

<https://gateoverflow.in/2492>



✓ False

BCNF decomposition can always be lossless, but it may not be always possible to get a dependency preserving BCNF decomposition.

38 votes

-- Sourav Roy (2.9k points)

3.5.9 Database Normalization: GATE CSE 1995 | Question: 26 top ↗

<https://gateoverflow.in/2665>



✓ The Candidate Keys are AB and BC .

None of the given functional dependencies are partial. So, the scheme qualifies for 2NF.

There is no transitive dependency. So, the scheme qualifies for 3NF.

All determinants are not Candidate Keys. So, the scheme do not qualify for BCNF.

37 votes

-- Rajarshi Sarkar (27.9k points)

3.5.10 Database Normalization: GATE CSE 1997 | Question: 6.9 top ↗

<https://gateoverflow.in/2265>



✓ Candidate Key is ab .

Since all a,b,c,d are atomic so the relation is in 1 NF.

Checking the FDs :

$a \rightarrow c$ (Prime derives Non-Prime.)

$b \rightarrow d$ (Prime derives Non-Prime.)

Since, there are partial dependencies it is not in 2NF.

gateover

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a} Answer 1NF but not 2NF

1 36 votes

-- Sourav Roy (2.9k points)

3.5.11 Database Normalization: GATE CSE 1998 | Question: 1.34 top

→ <https://gateoverflow.in/1671>



✓ 3NF,

because we can always have a 3NF decomposition which is dependency preserving and lossless (not possible for any higher forms).

1 50 votes

-- Digvijay (44.9k points)

3.5.12 Database Normalization: GATE CSE 1998 | Question: 26 top

→ <https://gateoverflow.in/1741>



✓ Since Book_id is the key we have,

- Book_id → Subject_Category_of_book
- Book_id → Name_of_Author
- Book_id → Nationality_of_Author

If we assume no other FD is there (this is not specified in the question), the relation is in BCNF as the LHS of every FD is primary key which is also a super key.

a. 2NF

b. New set of FDs are

- Book_id → Subject_Category_of_book
- Book_id → Name_of_Author
- Book_id → Nationality_of_Author
- Book_id → Book_title
- {Name_of_Author, Book_title} → Nationality_of_Author
- {Name_of_Author, Book_title} → Author_address
- {Name_of_Author, Book_title} → Book_id

One thing to notice here is only the primary key is being changed from Book_id to {Book_title, Name_of_Author}, but Book_id is still a key as based on convention Book_id always determines Book_title. Again if we assume no other FD, the relation is in BCNF as LHS of every FD is a super key. But it is logical to assume the FD

Name_of_Author → Author_address

(won't be valid if two authors have same address and should have been explicit in the question) and this FD is a partial FD on the candidate key {Name_of_Author, Book_title} as Name_of_Author is a part of the key and Author_address is not a key attribute. So, this violates 2NF and relation is now just in 1NF. (Debatable if we can assume FDs)

1 49 votes

-- Arjun Suresh (332k points)

3.5.13 Database Normalization: GATE CSE 1999 | Question: 1.24 top

→ <https://gateoverflow.in/1477>



✓ Answer: B

EC is the key for R. Both E and C are not coming on the right hand side of any functional dependency. So, both of them must be present in any key. Now, with EC and the given FDs, we can derive all other attributes making EC a key.

1 26 votes

-- Rajarshi Sarkar (27.9k points)

3.5.14 Database Normalization: GATE CSE 1999 | Question: 2.7, UGCNET-June2014-III: 25 top

→ <https://gateoverflow.in/1485>



✓ $R_1 \cap R_2 \neq \emptyset$. This makes the decomposition lossless join, as all the attributes are keys, $R_1 \cap R_2$ will be a key of the decomposed relations (lossless condition says the common attribute must be a key in at least one of the decomposed relation). Now, even the original relation R is in 3NF (even BCNF) as all the attributes are prime attributes (in fact each attribute is a candidate key). Hence, any decomposition will also be in 3NF (even BCNF). Option D.

PS: Decomposition in 3NF means decomposed relations are in 3NF. But when we consider any decomposed relation, we must also include any FD which are being implied by the original relational schema. For example, in a decomposed relation STU, there will be a FD $U \rightarrow S$ as well.

85 votes

-- Arjun Suresh (332k points)

3.5.15 Database Normalization: GATE CSE 2000 | Question: 2.24 top

https://gateoverflow.in/671



- ✓ (b) is answer.

If $A \rightarrow B$ then for each same value of A , B value should be same. If all the A values are distinct the FD hold irrespective of the B values.

Since all Y values are distinct FDs with Y, YX and YZ on LHS hold. So, option B is correct.

In option A, $Z \rightarrow Y$ is violated as for same Z value we have different Y values.

Similarly in C, $X \rightarrow Z$ is violated and in D, $XZ \rightarrow Y$ is violated.

37 votes

-- Aravind (2.8k points)

3.5.16 Database Normalization: GATE CSE 2001 | Question: 2.23 top

https://gateoverflow.in/741



- ✓ taking up option A first :

We have, $R(A, B, C, D)$ and the Functional Dependency set = $\{A \rightarrow B, B \rightarrow CD\}$.

Now we will try to decompose it such that the decomposition is a Lossless Join, Dependency Preserving and new relations thus formed are in BCNF.

We decomposed it to $R_1(A, B)$ and $R_2(B, C, D)$. This decomposition satisfies all three properties we mentioned prior.

taking up option B :

we have, $R(A, B, C, D)$ and the Functional Dependency set = $\{A \rightarrow B, B \rightarrow C, C \rightarrow D\}$.

we decomposed it as $R_1(A, B)$, $R_2(B, C)$ and $R_3(C, D)$. This decomposition too satisfies all properties as decomposition in option A.

taking up option D :

we have, $R(A, B, C, D)$ and the Functional Dependency set = $\{A \rightarrow BCD\}$.

This set of FDs is equivalent to set = $\{A \rightarrow B, A \rightarrow C, A \rightarrow D\}$ on applying decomposition rule which is derived from Armstrong's Axioms.

we decomposed it as $R_1(A, B)$, $R_2(A, C)$ and $R_3(A, D)$. This decomposition also satisfies all properties as required.

taking up option C :

we have, $R(A, B, C, D)$ and the Functional Dependency set = $\{AB \rightarrow C, C \rightarrow AD\}$.

we decompose it as $R_1(A, B, C)$ and $R_2(C, D)$. This preserves all dependencies and the join is lossless too, but the relation R_1 is not in BCNF. In R_1 we keep ABC together otherwise preserving $\{AB \rightarrow C\}$ will fail, but doing so also causes $\{C \rightarrow A\}$ to appear in R_1 . $\{C \rightarrow A\}$ violates the condition for R_1 to be in BCNF as C is not a superkey. Condition that all relations formed after decomposition should be in BCNF is not satisfied here.

We need to identify the INCORRECT, Hence mark option C.

References



134 votes

-- Amar Vashishth (25.2k points)

(C) is the answer. Because of $AB \rightarrow C$ and $C \rightarrow A$, we cannot have A, B and C together in any BCNF relation- in relation ABC, C is not a super key and $C \rightarrow A$ exists violating BCNF condition. So, we cannot preserve $AB \rightarrow C$ dependency in any decomposition of ABCD.

For (A) we can have AB, BCD, A and B the respective keys

For (B) we can have AB, BC, CD, A, B and C the respective keys

For (D) we can have ABCD, A is key

37 votes

-- Arjun Suresh (332k points)

3.5.17 Database Normalization: GATE CSE 2002 | Question: 1.19 top

https://gateoverflow.in/824



- ✓ Answer is A.

If a relation schema is in **BCNF** then all redundancy based on functional dependency has been removed, although other types of redundancy may still exist. A relational schema R is in Boyce–Codd normal form if and only if for every one of its dependencies $X \rightarrow Y$, at least one of the following conditions hold:

- $X \rightarrow Y$ is a trivial functional dependency ($Y \subseteq X$)
- X is a super key for schema R
- http://en.wikipedia.org/wiki/Boyce%20%93Codd_normal_form

References



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-- Priya_das (603 points)

3.5.18 Database Normalization: GATE CSE 2002 | Question: 16 top

<https://gateoverflow.in/869>



A. Yes as $R_1 \cap R_2 = M$ and $M \rightarrow O$

B. NO

c From the Dependencies obtained from R_1 and R_2 , we CANNOT infer $NO \rightarrow P$

Mistake That CAN be made: Here we CANNOT apply Pseudo Transitivity Rule using $M \rightarrow O$ & $MN \rightarrow P$ to obtain $NO \rightarrow P$ because the rule says :if $M \rightarrow O$ and $NO \rightarrow P$ then $NM \rightarrow P$ or $MN \rightarrow P$, But here we have $M \rightarrow O$ and $MN \rightarrow P$... SO we CANNOT apply the rule here to obtain $NO \rightarrow P$ from it.

C. BCNF

R_1 keys : P, L, MN hence BCNF

R_2 key : M hence BCNF

1 like 54 votes

-- Danish (3.4k points)

3.5.19 Database Normalization: GATE CSE 2002 | Question: 2.24 top

<https://gateoverflow.in/854>



- A. False. BCNF may or may not satisfy Dependency preservation, 3NF always does. But we can't make any guaranteed decision, regarding BCNF if it satisfies Dependency preservation
- B. False. Both are lossless.
- C. True. Using this we can always decide between BCNF & 3NF.
- D. False. Every BCNF relation is also 3NF trivially.

Answer -> C (& Only C).

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1 like 58 votes

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-- Akash Kanase (36k points)

A. dependency preservation.

in 3NF Dependency always preserved but in BCNF it may or may not be preserved.

For a particular set of FDs it may not differentiate BCNF and 3NF.

B. Lossless join always possible in both BCNF as well as 3NF.

D. 3NF definition also unable to differentiate BCNF & 3NF bcoz every BCNF is trivially 3NF.

C. every 3NF which is not BCNF fails BCNF Definition so it may used to differentiate which is BCNF & which is 3NF ..

1 like 25 votes

-- Digvijay (44.9k points)

3.5.20 Database Normalization: GATE CSE 2002 | Question: 2.25 top

<https://gateoverflow.in/855>



✓ Answer is C.

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Generally Normalization is done on the schema itself.

From the relational instance given, we may strike out FD s that do not hold.

e.g. B does not functionally determine C (This is true).

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But, we cannot say that A functionally determines B for the entire relation itself. This is because that, $A \rightarrow B$ holds for this instance, but in future there might be some tuples added to the instance that may violate $A \rightarrow B$.

So, overall on the relation we cannot conclude that $A \rightarrow B$, from the relational instance which is just a subset of an entire relation.

Upvote 70 votes

-- Sourav Roy (2.9k points)

3.5.21 Database Normalization: GATE CSE 2003 | Question: 85 top 5

https://gateoverflow.in/368



- ✓ There are three FDs that are valid from the above set of FDs for the given relation :

1. Date_of_Birth \rightarrow Age
2. Name \rightarrow Roll_number
3. Roll_number \rightarrow Name

Candidate keys for the above are : (Date_of_Birth, Name) and (Date_of_Birth, Roll_number)

Clearly there is partial dependency here ($Date_of_Birth \rightarrow Age$) and Age is not a prime attribute. So, it is in 1NF only.

Option (D).

Upvote 58 votes

-- Danish (3.4k points)

3.5.22 Database Normalization: GATE CSE 2004 | Question: 50 top 5

https://gateoverflow.in/1046



- ✓ Here candidate keys are,

- name, courseNo
- rollNo, courseNo

That makes name, rollNo, and courseNo prime attributes (part of some candidate key)

Functional dependencies 3 and 4 are not partial FDs.

If a relation schema is not in 2NF, then for some FD $x \rightarrow y$, x should be a **proper subset** of some candidate key and y should be a non-prime attribute.

FDs 3 and 4 are not violating 2NF, because the RHS are prime attributes.

For a relation to be in 3NF, for every FD, $x \rightarrow y$, x should be a super key or y is a prime attribute. For FDs 3 and 4, LHS are not super keys, but RHS are prime attributes. So, they are not violating 3NF.

For a relation to be in BCNF, for every FD, $x \rightarrow y$, x should be super key. This is clearly violated for FDs 3 and 4 and so the relation scheme is not in BCNF and hence not in 4NF also.

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Correct option: B.

Upvote 36 votes

-- rameshbabu (2.6k points)

3.5.23 Database Normalization: GATE CSE 2005 | Question: 29, UGCNET-June2015-III: 9 top 5

https://gateoverflow.in/1365



- ✓ Option C is the only FALSE statement.

We can always have a lossless decomposition into BCNF but not always we can have a lossless and dependency preserving decomposition. But this is always possible in the case of 3NF.

Option A is true as the requirement of BCNF required a relation schema to be in 3NF. Actually 3NF allows transitive dependency for prime attributes whereas BCNF does not.

Option D is true as shown below.

Assume the two attributes to be A and B .

Now, we can have three cases:

1. Either A or B is the candidate key but not both. i.e., $A \rightarrow B$ or $B \rightarrow A$. No other FD is possible and LHS of all FDs are superkeys and so BCNF requirement is satisfied.
2. Both A and B are candidate keys. i.e., $A \rightarrow B$ and $B \rightarrow A$. Like in above case BCNF requirement is satisfied.
3. Neither $A \rightarrow B$ nor $B \rightarrow A$ and so AB is the key. So, no other FD is possible and this case also satisfies BCNF requirement.

Thus any relation with 2 attributes is guaranteed to be in BCNF.

Ref: <https://gatecse.in/demystifying-database-normalization/>

References



0 votes

-- Arjun Suresh (332k points)

3.5.24 Database Normalization: GATE CSE 2005 | Question: 78

<https://gateoverflow.in/1401>



- ✓ (d) AEH, BEH, DEH

using the given functional dependencies and looking at the dependent attributes, E and H are not dependent on any. So, they must be part of any candidate key. So, only option is D. If we see the FD's, adding A, B or D to EH do form candidate keys.

34 votes

-- Aravind (2.8k points)

3.5.25 Database Normalization: GATE CSE 2006 | Question: 70

<https://gateoverflow.in/1848>



- ✓ $\{AF\}^* = \{AFDE\}$.

Hence, option C is wrong.

33 votes

-- Sankaranarayanan P.N (8.5k points)

3.5.26 Database Normalization: GATE CSE 2007 | Question: 62, UGCNET-June2014-II: 47

<https://gateoverflow.in/1260>



- ✓ Any relation with two attributes is in BCNF \Rightarrow This is true. It is trivial

A relation in which every key has only one attribute is in 2NF \Rightarrow This is true. As it is not possible to have Partial Functional Dependency !

A prime attribute can be transitively dependent on a key in a 3NF relation \Rightarrow This is true. As For 3NF to be violated we need something like Key \Rightarrow Non Key, Non Key \Rightarrow Non key. 3NF definition says that for functional dependency $x \rightarrow y$, either x should be key or y should be prime attribute. Then we can have something like Key \Rightarrow Non Key, Non key \Rightarrow Prime Attribute, resulting in Transitive FD on Prime Attribute, still in 3NF.

LHS must be always key, so No Transitive dependency is allowed.

Answer is D.

68 votes

-- Akash Kanase (36k points)

3.5.27 Database Normalization: GATE CSE 2008 | Question: 69

<https://gateoverflow.in/492>



- ✓ Answer: C

It is given that {Author, Title} is the key for both schemas.

The given dependencies are :

- {Title, Author} \rightarrow Catalog_no

- $\{Catalog_no\} \rightarrow \{\text{Title, Author, Publisher, Year}\}$
- $\{\text{Publisher, Title, Year}\} \rightarrow \{\text{Price}\}$

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First, let's take schema $Collection(\text{Title, Author, Catalog_no})$:

- $\{\text{Title, Author}\} \rightarrow Catalog_no$

$\{\text{Title, Author}\}$ is a candidate key and hence super key also and by definition of BCNF this is in BCNF.

Now, let's see $Book(\text{Title, Author, Catalog_no, Publisher, Year, Price})$:

- $\{\text{Title, Author}\}^+ \rightarrow \{\text{Title, Author, Catalog_no, Publisher, Year, Price}\}$
- $\{\text{Catalog_no}\}^+ \rightarrow \{\text{Title, Author, Publisher, Year, Price, Catalog_no}\}$

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So candidate keys are : $Catalog_no, \{\text{Title, Author}\}$

But in the given set of dependencies we have $\{\text{Publisher, Title, Year}\} \rightarrow \text{Price}$, which has a Transitive Dependency. **So, Book is not in 3NF but is in 2NF.**

45 votes

-- worst_engineer (2.8k points)

3.5.28 Database Normalization: GATE CSE 2009 | Question: 56 top

https://gateoverflow.in/43474



- ✓ The non-trivial FDs are

1. $(sname, city) \rightarrow street$
2. $sid \rightarrow street$
3. $(sname, city) \rightarrow sid$
4. $sid \rightarrow sname$
5. $sid \rightarrow city$

For all these, LHS is a super key and hence BCNF condition is satisfied. But we have some more dependencies here:

"each supplier and each street within a city has unique name"

This basically means each supplier in a city has unique name making $(sname, city)$ determine sid and hence making it a candidate key. Each street within a city also has a unique name and so $(street, city)$ is also a candidate key. Even then with all 3 candidate keys (for Suppliers schema), for any FD, the LHS is a super key here, and hence the relation schema (for other two relations it is straight forward) is in BCNF.

<http://db.grussell.org/section009.html>

Correct Answer: A

References



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62 votes

-- Arjun Suresh (332k points)

3.5.29 Database Normalization: GATE CSE 2012 | Question: 2 top

https://gateoverflow.in/34



- ✓ (C) Every relation in BCNF is also in 3NF. Straight from definition of BCNF.

31 votes

-- Arjun Suresh (332k points)

3.5.30 Database Normalization: GATE CSE 2013 | Question: 54 top

https://gateoverflow.in/1558



- ✓ Here, we can see that D is not part of any $FD's$, hence D must be part of the candidate key.

Now $D^+ = \{D\}$.

Hence, we have to add A, B, C, E, F, G, H to D and check which of them are Candidate keys of size 2.

We can proceed as:

$$AD+=\{A,B,C,D,E,F,G,H\}$$

Similarly we see $BD+$, $ED+$ and $FD+$ also gives us all the attributes. Hence, **AD, BD, ED, FD** are definitely the candidate keys.

But $CD+$, $GD+$ and $HD+$ doesn't give all the attributes hence, **CD, GD** and **HD** are not candidate keys.

Now we need to check the candidate keys of size 3. Since **AD, BD, ED, FD** are all candidate keys hence we can't find candidate keys by adding elements to them as they will give us superkeys as they are already minimal. Hence, we have to proceed with **CD, GD** and **HD**.

Also, we can't add any of **A, B, E, F** to **CD, GD, HD** as they will again give us superset of **AD, BD, ED, FD**.

Hence, we can only add among **C, G, H** to **CD, GD, HD**.

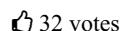
Adding **C** to **GD** and **HD** we get **GCD, HCD**. Taking closure and we will see they are not candidate keys.

Adding **H** to **GD** we get **GHD** which is also not a candidate key.(no more options with 3 attributes possible)

Now we need to check for candidate keys with 4 attributes. Since, only remaining options are **CGH** and we have to add **D** only possible key of size 4 is **CGHD** whose closure also doesn't give us all of the attributes in the relation (All possible options covered)

Hence, no of candidate keys are 4 : **AD, BD, ED, FD**.

Correct Answer: **B**



32 votes

-- Indranil Maji (537 points)



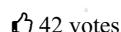
- ✓ Here, candidate keys are **AD, BD, ED** and **FD**.

Partial dependency exists $A \rightarrow BC$, $B \rightarrow CFH$ and $F \rightarrow EG$ etc. In the following **FDs**.

For example partial dependency $A \rightarrow C$ exists in $A \rightarrow BC$ and $B \rightarrow C$ and $B \rightarrow H$ in $B \rightarrow CFH$. etc.

So, given relation is in **1NF**, but not in **2NF**.

Correct Answer: **A**



42 votes

-- Manoj Kumar (26.7k points)



3.5.32 Database Normalization: GATE CSE 2014 Set 1 | Question: 21

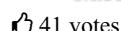
<https://gateoverflow.in/1788>

- ✓ Since E, F, H cannot be derived from anything else E, F, H should be there in key.

Using Find $\{EFH\}^+$, it contains all the attributes of the relation.

Hence, it is key.

Correct Answer: **B**



41 votes

-- Sankaranarayanan P.N (8.5k points)



3.5.33 Database Normalization: GATE CSE 2014 Set 1 | Question: 30

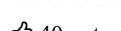
<https://gateoverflow.in/1797>



- ✓ (A) S1 is TRUE and S2 is FALSE.

A relation with 2 attributes is always in BCNF

The two sets of functional dependencies are not the same. We can not derive $AB \rightarrow E$ from the 1st set



40 votes

-- Aravind (2.8k points)



3.5.34 Database Normalization: GATE CSE 2015 Set 3 | Question: 20

<https://gateoverflow.in/8420>



- ✓ Option C is correct because $\{P, S\} \rightarrow \{S\}$

for trivial FD, if $X \rightarrow Y$ then Y must be a subset of X and for non trivial FD $X \cap Y = \emptyset$. and here $\{S\}$ is subset of $\{P, S\}$.

PS: Trivial means something which is always there. An attribute set always determines any of the component attributes and this is always true irrespective of the relation instance. Hence, this FD becomes trivial.

Like 54 votes

-- Anoop Sonkar (4.1k points)

3.5.35 Database Normalization: GATE CSE 2016 Set 1 | Question: 21 [top](#)

<https://gateoverflow.in/39637>



- ✓ Any superset of a key is also a superkey from definition of a superkey.
So, answer is B.

Tip: a superkey can be defined as a set of attributes of a [relation schema](#) upon which all attributes of the schema are [functionally dependent](#)

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References



Like 39 votes

-- Abhilash Panicker (7.6k points)

3.5.36 Database Normalization: GATE CSE 2016 Set 1 | Question: 23 [top](#)

<https://gateoverflow.in/39646>



- ✓ The actual design is in $1NF$ coz there are partial dependencies in the given FD set so the original DB design is in $1NF$ but not $2NF$.

Now, the new design is removing all the partial dependencies so its in $2NF$

So, the weakest form that the new schema satisfies that the old one couldn't is $2NF$ answer is B.

Like 48 votes

-- Bharani Viswas (611 points)

3.5.37 Database Normalization: GATE CSE 2017 Set 1 | Question: 16 [top](#)

<https://gateoverflow.in/118296>



- ✓ In option B and option D there is a dependency $W \rightarrow X$ which is not implied by the question and hence they are definitely wrong.

Now in option C) $Y \rightarrow X$ can be removed as it can be implied as $Y \rightarrow V$ and $V \rightarrow X$.

Hence, option (A) is correct.

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Like 52 votes

-- sriv_shubham (2.8k points)

3.5.38 Database Normalization: GATE CSE 2018 | Question: 42 [top](#)

<https://gateoverflow.in/204116>



- ✓ Answer is (B).

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rollno, courseid \rightarrow email

(rollno, courseid is a super key, so it comes under 3NF as well as BCNF).

email \rightarrow rollno

Here, email is not a key though but rollno comes under prime-attribute. Hence it's in 3NF but not BCNF.

Like 25 votes

-- Baljit kaur (1k points)



- ✓ Y is in BCNF because binary attribute.
 Z is not in BCNF because $S \rightarrow Q$ is in Z and S is not Super key.

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Dependency Preserving:

$QR \rightarrow S$ in Z

$R \rightarrow P$ is in Y

$S \rightarrow Q$ is in Z

So it is dependency preserving.

Lossless:

$Y \cap Z = R$ which is key of Y .

Lossless it is.

Only 2nd is correct.

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So Option C is the answer

128 votes

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-- Digvijay (44.9k points)



- ✓ In 3NF where functional dependency is of type $X \rightarrow Y$

X can be the super key or Y can be the prime attribute

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Whereas in BCNF where functional dependency is of type $X \rightarrow Y$

X should be super key (BCNF is more strict compared to 3NF)

- Option (C) says it has a partial dependency (not even 2NF).
- Option (D) multiple values in a cell. i.e not atomic (not even 1NF).
- Option (B) says X is not a super key and Y is not a prime attribute. Therefore not 3NF.

Ans (A): Says X is not a super key but Y is a prime attribute. Satisfies one of the conditions of the 3NF formal definition. As X is not a Super Key it is not in BCNF.

15 votes

-- Srinivas_Reddy_Kotla (775 points)



- ✓ Decomposition removes redundancy from the database. It is lossless if it's possible to reconstruct the table from the given set of decomposition tables using natural join.

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Decomposition of a relation R into R_1, R_2 is a lossless-join decomposition if at least one of the following functional dependencies are in F^+ :

1. $((R_1 \cap R_2) \rightarrow (R_1 - R_2))$ is in F^+ or
2. $((R_1 \cap R_2) \rightarrow (R_2 - R_1))$ is in F^+

- Decomposition is lossless iff $R_1 \bowtie R_2 = R$

$D_1 : R = [r_1(PQST), r_2(PTX), r_3(QY), r_4(YZW)]$

$\Rightarrow r_1 \cap r_2 = (PT)^+ = PTYXZW$ which is superkey, we can combine them.

So new table is $x_1 = (PQSTX)$

In the same way; $r_3 \cap r_4 = Y^+ = YZW$

which is SK, and so we can merge them.

Thus $x_2 = (QYZW)$

Now $x_1 \cap x_2 = Q^+ = QYZW$ which is SK.

So we can get original table $(PQSTXYZW)$

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So given decomposition D_1 is lossless join decomposition.

Similarly we can check for D_2

$$D_2 : R = [r_1(PQS), r_2(TX), r_3(QY), r_4(YZW)]$$

$\Rightarrow r_3 \cap r_4 = Y^+ = YZW$, is Sk we can merge them.

So new table will be $x_1 = (QYZW)$

Similarly $x_1 \cap r_1 = Q^+ = QYZW$ is also Sk, we can combine them. new table will be $x_2 = (PQSYZW)$

Now $x_2 \cap r_2$ is not superkey. no common attribute is present between them. We can try any other order of combining the relations and none of them will satisfy the lossless decomposition condition. Hence it is lossy decomposition.

\therefore decomposition D_2 is lossy decomposition.

Option A is correct.

Ref: [lossless-join-and-dependency-preserving-decomposition](#)

References



3 votes

-- Hira (14.1k points)

3.5.42 Database Normalization: GATE CSE 2021 Set 2 | Question: 40

<https://gateoverflow.in/357500>



- ✓ Option A: $(PS)^+ = P, Q, R, S, T$ so $PS \rightarrow T$ holds.

Option B: $(R)^+ = R$ so $R \rightarrow T$ doesn't hold.

Option C: $(P)^+ = P, Q, R$ so $P \rightarrow R$ holds.

Option D: $(PS)^+ = P, Q, R, S, T$ so $PS \rightarrow Q$ holds

3 votes

-- zxy123 (2.8k points)

3.5.43 Database Normalization: GATE IT 2004 | Question: 75

<https://gateoverflow.in/3719>



- ✓ It is in $2nf$ - for $2NF$ all non prime attribute should be fully functionally dependent on key. Here key is empcode and contains only one attribute hence no partial dependency. But there is transitive dependency in this (pincode \rightarrow city, state). So it is not in $3NF$.

answer: B

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51 votes

-- Sankaranarayanan P.N (8.5k points)

3.5.44 Database Normalization: GATE IT 2005 | Question: 22

<https://gateoverflow.in/3767>



- ✓ Answer is A 1NF

Key is $\{F_1, F_2\}$

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$F_1 \rightarrow F_3, F_2 \rightarrow F_4$ are partial dependencies (a proper subset of candidate key determining a non-key attribute) thus violating 2 NF requirement.

35 votes

-- K Rajashekhar (997 points)

3.5.45 Database Normalization: GATE IT 2005 | Question: 70

<https://gateoverflow.in/3833>



- ✓ Answer is (B).

Apply membership test for all the given Functional Dependencies.

1. $CD \rightarrow AC$
 $CD^+ = CDEAB$

2. $BD \rightarrow CD$
 $BD^+ = BD$

i.e. BD cannot derive CD and hence is not implied.
 Similarly do for rest two.

39 votes

-- Gate Keeda (15.9k points)

3.5.46 Database Normalization: GATE IT 2006 | Question: 60 [top](#)



- ✓ As we can see attributes X and Y do not appear in the RHS of any FD and so they need to be part of any super/candidate key. So, candidate keys are: VXY, WXY, ZXY as these three **can determine any other** attribute where as a **proper subset** of any of them cannot determine all other attributes.

VXZ is not a super key as Y is not there whereas $VWXY$ and $VWXYZ$ are super keys but since their proper subsets are also super keys they are not candidate keys.

Answer is **B**.

27 votes

-- Pooja Palod (24.1k points)

3.5.47 Database Normalization: GATE IT 2008 | Question: 61 [top](#)



- ✓ Option A.

$(A, B) (B, C)$ – common attribute is B and due to $B \rightarrow C$, B is a key for (B, C) and hence ABC can be losslessly decomposed into (A, B) and (B, C) .

$(A, B, C)(B, D)$, common attribute is B and $B \rightarrow D$ is a FD (via $B \rightarrow C, C \rightarrow D$), and hence, B is a key for (B, D) . So, decomposition of (A, B, C, D) into $(A, B, C)(B, D)$ is lossless.

Thus the given decomposition is lossless.

The given decomposition is also dependency preserving as the dependencies $A \rightarrow B$ is present in (A, B) , $B \rightarrow C$ is present in (B, C) , $D \rightarrow B$ is present in (B, D) and $C \rightarrow D$ is indirectly present via $C \rightarrow B$ in (B, C) and $B \rightarrow D$ in (B, D) .

<http://www.sztaki.hu/~fodroczi/dbs/dep-pres-own.pdf>

References



112 votes

-- Arjun Suresh (332k points)

3.5.48 Database Normalization: GATE IT 2008 | Question: 62 [top](#)



- ✓ Answer: D

Here AB is the candidate key and $B \rightarrow G$ is a partial dependency. So, R is not in $2NF$.

41 votes

-- Rajarshi Sarkar (27.9k points)

3.5.49 Database Normalization: GATE2001-1.23, UGCNET-June2012-III: 18 [top](#)

<https://gateoverflow.in/716>



- ✓ Answer is C.

Here, no common attribute in $R1$ and $R2$, therefore lossy join will be there.

and both the dependencies are preserved in composed relations so, dependency preserving.

30 votes

-- jayendra (6.7k points)

A decomposition $\{R_1, R_2\}$ is a lossless-join decomposition if $R_1 \cap R_2 \rightarrow R_1$ (**R_1 should be key**) or $R_1 \cap R_2 \rightarrow R_2$ (**R_2 should be key**) but $(A,B) \cap (C,D) = \emptyset$ so lossy join

FD:1 $A \rightarrow B$

FD:2 $C \rightarrow D$

$R_1(A,B)$ have all attributes of FD1 and $R_2(C,D)$ have all attributes of FD2 so ,dependency preserved decompostion

Reference : - question no. 8.1 Korth <http://codex.cs.yale.edu/avi/db-book/db6/practice-exer-dir/8s.pdf>

References classroom.gateoverflow.in

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12 votes

-- Rishi yadav (9k points)

3.6

Er Diagram (10) [top](#)

3.6.1 Er Diagram: GATE CSE 2005 | Question: 75 [top](#)

<https://gateoverflow.in/1398>



Let E_1 and E_2 be two entities in an E/R diagram with simple-valued attributes. R_1 and R_2 are two relationships between E_1 and E_2 , where R_1 is one-to-many and R_2 is many-to-many. R_1 and R_2 do not have any attributes of their own. What is the minimum number of tables required to represent this situation in the relational model?

- A. 2 tests.gatecse.in
- B. 3 goclasses.in
- C. 4 tests.gatecse.in
- D. 5 tests.gatecse.in

gate2005-cse databases er-diagram normal

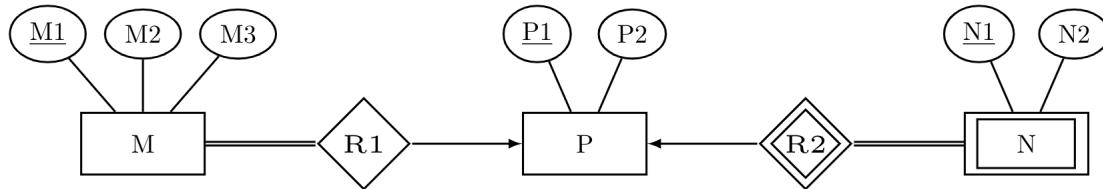
Answer [¶](#)

3.6.2 Er Diagram: GATE CSE 2008 | Question: 82 [top](#)

<https://gateoverflow.in/390>



Consider the following ER diagram



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The minimum number of tables needed to represent $M, N, P, R1, R2$ is

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- B. 3 tests.gatecse.in
- C. 4 goclasses.in
- D. 5 tests.gatecse.in

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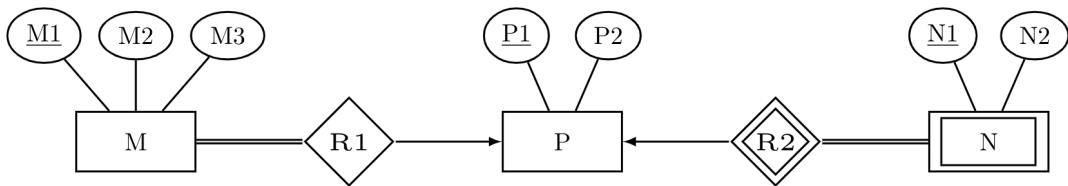
Answer [¶](#)

3.6.3 Er Diagram: GATE CSE 2008 | Question: 83 [top](#)

<https://gateoverflow.in/87025>



Consider the following ER diagram



The minimum number of tables needed to represent $M, N, P, R1, R2$ is

Which of the following is a correct attribute set for one of the tables for the minimum number of tables needed to represent $M, N, P, R1, R2$?

- A. $M1, M2, M3, P1$
- B. $M1, P1, N1, N2$
- C. $M1, P1, N1$
- D. $M1, P1$

[gate2008-cse](#) [databases](#) [er-diagram](#) [normal](#)

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[Answer](#)

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3.6.4 Er Diagram: GATE CSE 2012 | Question: 14 [top](#)

<https://gateoverflow.in/46>



Given the basic ER and relational models, which of the following is **INCORRECT**?

- A. An attribute of an entity can have more than one value
- B. An attribute of an entity can be composite
- C. In a row of a relational table, an attribute can have more than one value
- D. In a row of a relational table, an attribute can have exactly one value or a NULL value

[gate2012-cse](#) [databases](#) [normal](#) [er-diagram](#)

[Answer](#)

[tests.gatecse.in](#)

3.6.5 Er Diagram: GATE CSE 2015 Set 1 | Question: 41 [top](#)

<https://gateoverflow.in/8309>



Consider an Entity-Relationship (ER) model in which entity sets E_1 and E_2 are connected by an $m : n$ relationship R_{12} . E_1 and E_3 are connected by a $1 : n$ (1 on the side of E_1 and n on the side of E_3) relationship R_{13} .

E_1 has two-singled attributes a_{11} and a_{12} of which a_{11} is the key attribute. E_2 has two singled-valued attributes a_{21} and a_{22} of which a_{21} is the key attribute. E_3 has two single-valued attributes a_{31} and a_{32} of which a_{31} is the key attribute. The relationships do not have any attributes.

If a relational model is derived from the above ER model, then the minimum number of relations that would be generated if all relation are in 3NF is _____.

[gate2015-cse-set1](#) [databases](#) [er-diagram](#) [normal](#) [numerical-answers](#)

[Answer](#)

[tests.gatecse.in](#)

3.6.6 Er Diagram: GATE CSE 2017 Set 2 | Question: 17 [top](#)

<https://gateoverflow.in/118157>



An ER model of a database consists of entity types A and B . These are connected by a relationship R which does not have its own attribute. Under which one of the following conditions, can the relational table for R be merged with that of A ?

- A. Relationship R is one-to-many and the participation of A in R is total
- B. Relationship R is one-to-many and the participation of A in R is partial
- C. Relationship R is many-to-one and the participation of A in R is total
- D. Relationship R is many-to-one and the participation of A in R is partial

[gate2017-cse-set2](#) [databases](#) [er-diagram](#) [normal](#)

[Answer](#)



In an Entity-Relationship (ER) model, suppose R is a many-to-one relationship from entity set E_1 to entity set E_2 . Assume that E_1 and E_2 participate totally in R and that the cardinality of E_1 is greater than the cardinality of E_2 .

Which one of the following is true about R ?

- A. Every entity in E_1 is associated with exactly one entity in E_2
- B. Some entity in E_1 is associated with more than one entity in E_2
- C. Every entity in E_2 is associated with exactly one entity in E_1
- D. Every entity in E_2 is associated with at most one entity in E_1

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[gate2018-cse](#) [databases](#) [er-diagram](#) [normal](#)

Answer



Which one of the following is used to represent the supporting many-one relationships of a weak entity set in an entity-relationship diagram?

- A. Diamonds with double/bold border
- B. Rectangles with double/bold border
- C. Ovals with double/bold border
- D. Ovals that contain underlined identifiers

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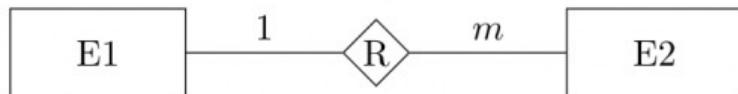
[gate2020-cse](#) [databases](#) [er-diagram](#)

Answer



Consider the following entity relationship diagram (ERD), where two entities E_1 and E_2 have a relation R of cardinality 1:m.

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The attributes of E_1 are A_{11} , A_{12} and A_{13} where A_{11} is the key attribute. The attributes of E_2 are A_{21} , A_{22} and A_{23} where A_{21} is the key attribute and A_{23} is a multi-valued attribute. Relation R does not have any attribute. A relational database containing minimum number of tables with each table satisfying the requirements of the third normal form (3NF) is designed from the above ERD. The number of tables in the database is

- A. 2
- B. 3
- C. 5
- D. 4

[gate2004-it](#) [databases](#) [er-diagram](#) [normal](#)

Answer



Consider the entities 'hotel room', and 'person' with a many to many relationship 'lodging' as shown below:

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If we wish to store information about the rent payment to be made by person (s) occupying different hotel rooms, then this information should appear as an attribute of

- A. Person
- B. Hotel Room
- C. Lodging
- D. None of these

[gate2005-it](#) [databases](#) [er-diagram](#) [easy](#)

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Answer 

Answers: Er Diagram

3.6.1 Er Diagram: GATE CSE 2005 | Question: 75 top

<https://gateoverflow.in/1398>



- ✓ We need a separate table for many-to-many relation.
one-to-many relation doesn't need a separate table and can be handled using a foreign key.
So, answer is **B** - 3 tables.

Reference: [MIT notes](#).

References



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 42 votes

-- Arjun Suresh (332k points)

3.6.2 Er Diagram: GATE CSE 2008 | Question: 82 top

<https://gateoverflow.in/890>



- ✓ First strong entity types are made to tables. So, we get two tables **M** and **P**.

I assume **R1** is $1 : 1$ or $1 : n$ as that would minimize the number of tables as asked in question.

Now participation of **M** in **R1** is total (indicated by double arrow) meaning every entity of **M** participate in **R1**. Since **R1** is not having an attribute, we can simple add the primary key of **P** to the table **M** and add a foreign key reference to **M**. This handles **R1** and we don't need an extra table. So, **M** becomes **M1, M2, M3, P1**.

Here is a [weak entity](#) weakly related to **P**. So, we form a new table **N**, and includes the primary key of **P(P1)** as foreign key reference. Now **(P1, N1)** becomes the primary key of **N**.

Thus we get 3 tables.

M : **M1, M2, M3, P1** - **M1** primary key, **P1** references **P**

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P : **P1, P2** - **P1** primary key

N : **P1, N1, N2** - **(P1, N1)** primary key, **P1** references **P**.

So, answers is **B**.

References



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 88 votes

-- Arjun Suresh (332k points)

3.6.3 Er Diagram: GATE CSE 2008 | Question: 83 top

<https://gateoverflow.in/87025>



- ✓ First strong entity types are made to tables. So, we get two tables **M** and **P**.

I assume **R1** is $1 : 1$ or $1 : n$ as that would minimize the number of tables as asked in question.

Now participation of **M** in **R1** is total (indicated by double arrow) meaning every entity of **M** participate in **R1**. Since **R1** is not having an attribute, we can simple add the primary key of **P** to the table **M** and add a foreign key reference to **M**. This handles **R1** and we don't need an extra table. So, **M** becomes **{M1, M2, M3, P1}**.

N here is a [weak entity](#) weakly related to P . So, we form a new table N , and includes the primary key of $P(P1)$ as foreign key reference. Now $(P1, N1)$ becomes the primary key of N .

Thus we get 3 tables.

$M: M1, M2, M3, P1 - M1$ primary key, $P1$ references P

$P: P1, P2 - P1$ primary key

$N: P1, N1, N2 - (P1, N1)$ primary key, $P1$ references P .

So, answers is A .

References



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thumb up 28 votes

-- Arjun Suresh (332k points)

3.6.4 Er Diagram: GATE CSE 2012 | Question: 14 top ↗

↗ <https://gateoverflow.in/46>



- ✓ (C) is incorrect as a relational table requires that, in a row, an attribute can have exactly one value or NULL value.

thumb up 39 votes

-- Arjun Suresh (332k points)

3.6.5 Er Diagram: GATE CSE 2015 Set 1 | Question: 41 top ↗

↗ <https://gateoverflow.in/8309>



- ✓ Answer is 4. The relations are as shown:

$\langle a_{11}, a_{12} \rangle$ for E_1
 $\langle a_{21}, a_{22} \rangle$ for E_2

$\langle a_{31}, a_{32}, a_{11} \rangle$ for E_3 and $E_1 - E_3$ relationship

$\langle a_{11}, a_{21} \rangle$ for $m : n$ relationship $E_1 - E_2$

We cannot combine any relation here as it will give rise to partial functional dependency and thus violate 3NF.

Reference: [MIT notes](#)

References



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thumb up 73 votes

-- Arjun Suresh (332k points)

3.6.6 Er Diagram: GATE CSE 2017 Set 2 | Question: 17 top ↗

↗ <https://gateoverflow.in/118157>



- ✓ The relation table for R should always be merged with the entity that has total participation and relationship should be many to one.

Answer is C.

thumb up 36 votes

-- Arnabi Bej (5.8k points)

3.6.7 Er Diagram: GATE CSE 2018 | Question: 11 top ↗

↗ <https://gateoverflow.in/204085>



- ✓ Since it is a **many to one relationship** from **E1 to E2**, therefore:

1. No entity in E_1 can be related to more than one entity in E_2 . (hence B is incorrect)
2. An entity in E_2 can be related to more than one entity in E_1 .(hence C and D are incorrect).

Option (A) is correct: Every entity in E1 is associated with exactly one entity in E2.

37 votes

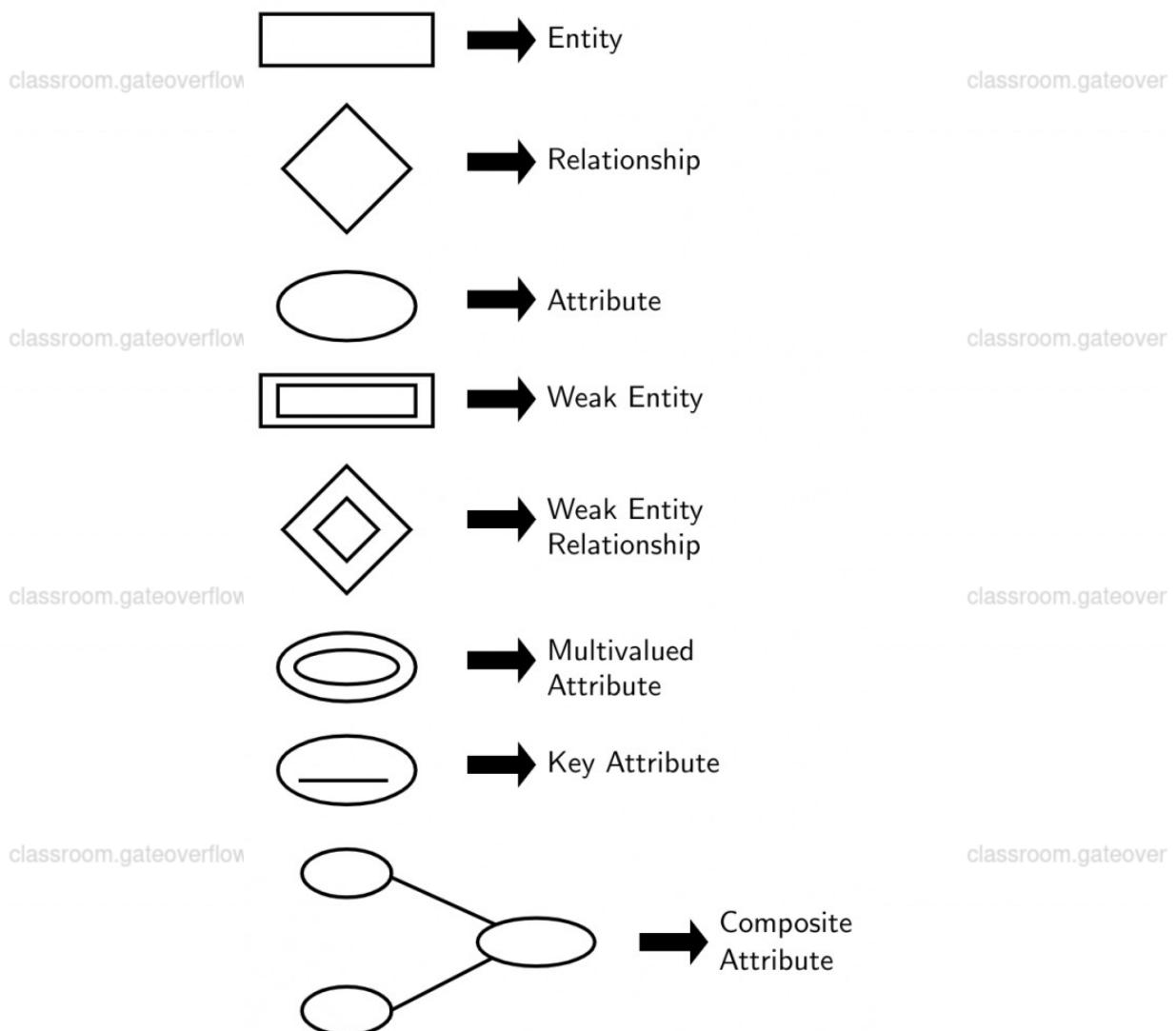
-- Aakanchha (471 points)

3.6.8 Er Diagram: GATE CSE 2020 | Question: 14 [top](#)

<https://gateoverflow.in/33321>



- ✓ Answer : A



Weak entity set is represented by Rectangles with double/bold border.

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-- Prashant Singh (47.2k points)

13 votes

3.6.9 Er Diagram: GATE IT 2004 | Question: 73 [top](#)

<https://gateoverflow.in/3717>



- ✓ We need just two tables for 1NF.

T1: {A11, A12, A13}

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T2: {A21, A22, A23, A11}

A23 being multi-valued, A21, A23 becomes the key for T2 as we need to repeat multiple values corresponding to the multi-valued attribute to make it 1NF. But, this causes partial FD $A21 \rightarrow A22$ and makes the table not in 2NF. In order to make the table in 2NF, we have to create a separate table for multi-valued attribute. Then we get

T1 : {A11, A12, A13} – key is A11

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T3 : {A21, A23} – key is {A21, A23}

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Here, all determinants of all FDs are keys and hence the relation is in BCNF and so 3NF also. So, we need minimum 3 tables.

Correct Answer: *B*

98 votes

-- Arjun Suresh (332k points)

3.6.10 Er Diagram: GATE IT 2005 | Question: 21 [top](#)

<https://gateoverflow.in/3766>



- ✓ Since it is many to many, rent cannot be an attribute of room or person entities alone. If depending on number of persons sharing a room the rent for each person for the room will be different. Otherwise rent can be attribute of room. hence i go for attribute of Lodging.

Correct Answer: *C*

47 votes

-- Sankaranarayanan P.N (8.5k points)

3.7

Indexing (11) [top](#)

3.7.1 Indexing: GATE CSE 1989 | Question: 4-xiv [top](#)

<https://gateoverflow.in/8828>



For secondary key processing which of the following file organizations is preferred? Give a one line justification:

- A. Indexed sequential file organization.
- B. Two-way linked list.
- C. Inverted file organization.
- D. Sequential file organization.

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gate1989 normal databases indexing descriptive

Answer

3.7.2 Indexing: GATE CSE 1990 | Question: 10b [top](#)

<https://gateoverflow.in/85691>



One giga bytes of data are to be organized as an indexed-sequential file with a uniform blocking factor 8. Assuming a block size of 1 Kilo bytes and a block referencing pointer size of 32 bits, find out the number of levels of indexing that would be required and the size of the index at each level. Determine also the size of the master index. The referencing capability (fanout ratio) per block of index storage may be considered to be 32.

gate1990 databases indexing descriptive

Answer

3.7.3 Indexing: GATE CSE 1993 | Question: 14 [top](#)

<https://gateoverflow.in/2311>



An ISAM (indexed sequential) file consists of records of size 64 bytes each, including key field of size 14 bytes. An address of a disk block takes 2 bytes. If the disk block size is 512 bytes and there are 16K records, compute the size of the data and index areas in terms of number blocks. How many levels of tree do you have for the index?

gate1993 databases indexing normal descriptive

Answer

3.7.4 Indexing: GATE CSE 1998 | Question: 1.35 [top](#)

<https://gateoverflow.in/1672>



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There are five records in a database.

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Name	Age	Occupation	Category
Rama	27	CON	A
Abdul	22	ENG	A
Jennifer	28	DOC	B
Maya	32	SER	D
Dev	24	MUS	C

There is an index file associated with this and it contains the values 1, 3, 2, 5 and 4. Which one of the fields is the index built from?

- A. Age
- B. Name
- C. Occupation
- D. Category

gate1998 databases indexing normal

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Answer ↗

3.7.5 Indexing: GATE CSE 2008 | Question: 16, ISRO2016-60 top ↗

https://gateoverflow.in/414



A clustering index is defined on the fields which are of type

- A. non-key and ordering
- B. non-key and non-ordering
- C. key and ordering
- D. key and non-ordering

gate2008-cse easy databases indexing isro2016

goclasses.in

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Answer ↗

3.7.6 Indexing: GATE CSE 2008 | Question: 70 top ↗

https://gateoverflow.in/259



Consider a file of 16384 records. Each record is 32 bytes long and its key field is of size 6 bytes. The file is ordered on a non-key field, and the file organization is unspanned. The file is stored in a file system with block size 1024 bytes, and the size of a block pointer is 10 bytes. If the secondary index is built on the key field of the file, and a multi-level index scheme is used to store the secondary index, the number of first-level and second-level blocks in the multi-level index are respectively

- A. 8 and 0
- B. 128 and 6
- C. 256 and 4
- D. 512 and 5

gate2008-cse databases indexing normal

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Answer ↗

3.7.7 Indexing: GATE CSE 2011 | Question: 39 top ↗

https://gateoverflow.in/2141



Consider a relational table r with sufficient number of records, having attributes A_1, A_2, \dots, A_n and let $1 \leq p \leq n$. Two queries $Q1$ and $Q2$ are given below.

- $Q1 : \pi_{A_1, \dots, A_p} (\sigma_{A_p=c} (r))$ where c is a constant
- $Q2 : \pi_{A_1, \dots, A_p} (\sigma_{c_1 \leq A_p \leq c_2} (r))$ where c_1 and c_2 are constants.

The database can be configured to do ordered indexing on A_p or hashing on A_p . Which of the following statements is TRUE?

- A. Ordered indexing will always outperform hashing for both queries
- B. Hashing will always outperform ordered indexing for both queries
- C. Hashing will outperform ordered indexing on $Q1$, but not on $Q2$
- D. Hashing will outperform ordered indexing on $Q2$, but not on $Q1$

tests.gatecse.in databases indexing normal

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Answer ↗

3.7.8 Indexing: GATE CSE 2013 | Question: 15 top ↗

https://gateoverflow.in/1437



An index is clustered, if

- A. it is on a set of fields that form a candidate key
- B. it is on a set of fields that include the primary key
- C. the data records of the file are organized in the same order as the data entries of the index

D. the data records of the file are organized not in the same order as the data entries of the index

gate2013-cse databases indexing normal

Answer 

3.7.9 Indexing: GATE CSE 2015 Set 1 | Question: 24 top ↗

↗ <https://gateoverflow.in/8222>



A file is organized so that the ordering of the data records is the same as or close to the ordering of data entries in some index. Than that index is called

- A. Dense
- B. Sparse
- C. Clustered
- D. Unclustered

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gate2015-cse-set1 databases indexing easy

Answer 

3.7.10 Indexing: GATE CSE 2020 | Question: 54 top ↗

↗ <https://gateoverflow.in/333177>



Consider a database implemented using B+ tree for file indexing and installed on a disk drive with block size of 4 KB. The size of search key is 12 bytes and the size of tree/disk pointer is 8 bytes. Assume that the database has one million records. Also assume that no node of the B+ tree and no records are present initially in main memory. Consider that each record fits into one disk block. The minimum number of disk accesses required to retrieve any record in the database is _____

gate2020-cse numerical-answers databases b-tree indexing

Answer 

3.7.11 Indexing: GATE CSE 2021 Set 2 | Question: 21 top ↗

↗ <https://gateoverflow.in/357519>



A data file consisting of 1,50,000 student-records is stored on a hard disk with block size of 4096 bytes. The data file is sorted on the primary key RollNo. The size of a record pointer for this disk is 7 bytes. Each student-record has a candidate key attribute called ANum of size 12 bytes. Suppose an index file with records consisting of two fields, ANum value and the record pointer to the corresponding student record, is built and stored on the same disk. Assume that the records of data file and index file are not split across disk blocks. The number of blocks in the index file is _____

gate2021-cse-set2 numerical-answers databases indexing

Answer 

Answers: Indexing

3.7.1 Indexing: GATE CSE 1989 | Question: 4-xiv top ↗

↗ <https://gateoverflow.in/88228>



Inverted File organization

Because of the following reasons

An index for each secondary key.

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- An index entry for each distinct value of the secondary key.

It exhibits better inquiry performance

 4 votes

-- Neeraj7375 (1.1k points)

3.7.2 Indexing: GATE CSE 1990 | Question: 10b top ↗

↗ <https://gateoverflow.in/85691>



- ✓ First we can understand the terms given in the question:

- Uniform blocking factor = 8

This is the no. of records which can be held in a data block.

This information is required for DENSE index which is mandatory when the index is unclustered - data records not ordered by the search key (there is an index entry for each record) as compared to fully sparse (which has an index entry for each data block). Since in the question we do not have any information about "record pointer size" we can assume that the index is sparse. (Solution considering dense index is given at end)

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- Block size = 1 KB

This is the size of data block (file block containing records) as well as index block (file block containing index entries). Since file size is given as 1 giga bytes, we get no. of data blocks = $\frac{1 \text{ GB}}{1 \text{ KB}} = 1 \text{ M} = 2^{20}$

- Block referencing pointer size = 32 bits = 4 B

This is the pointer size required to point to a block.

- The referencing capability (fanout ratio) per block of index storage may be considered to be 32.

This means that an index block can refer to 32 blocks (either data or index blocks). i.e., even though we have 1024 bytes in a block, and each block pointer size is 4 bytes, it can refer to only 32 blocks. This might be due to large search key size which must be present for each index entry.

Now, coming to the solution:

No. of entries in first level index (which indexes to the data blocks) (in case of page tables in virtual memory, this will be the total no. of entries in last level page table) = no. of data blocks (assuming sparse index) = 2^{20}

No. of index blocks in level 1 = $\frac{2^{20}}{32} = 2^{15}$ as each index block can refer to 32 blocks (given fanout) which means size of level 1 index = $2^{15} \times 1 \text{ KB} = 32 \text{ MB}$

Since the fanout is 32, no. of index blocks in second level = $\frac{2^{15}}{32} = 2^{10}$.

Size of second level index = $2^{10} \times 1 \text{ KB} = 1 \text{ MB}$

No. of index blocks in third level = $\frac{2^{10}}{32} = 32$.

Size of third level index = $32 \times 1 \text{ KB} = 32 \text{ KB}$

No. of index blocks in fourth level = $\frac{32}{32} = 1$ and it occupies 1 KB. Since only 1 index block is there we do not need further level of indexing.

Searching starts in the last level (this will be level 1 page table in case of virtual memory in OS).

Master Index -- not sure exactly what this means but I assume this is the complete index whose size will be $32 \text{ MB} + 1 \text{ MB} + 32 \text{ KB} + 1 \text{ KB} = 33.033 \text{ MB}$

Now assuming dense index.

Block pointer size = 32 bits. Since, we have 8 records in a block, we need at least 3 more extra bits for a record pointer. So, we need to assume 5 bytes for a record pointer. As fanout is given in the question it is not changing when the record pointer size changes. If fanout was not given, we could have calculated it as $\frac{\text{block size}}{\text{search key size} + \text{record pointer size}}$

Here, we need an index entry for each record. So, we need = $\frac{1 \text{ GB}}{1 \text{ KB}} \times 8 = 8 \text{ M} = 2^{23}$ entries in first level index.

No. of index blocks in first level = $\frac{2^{23}}{32} = 2^{18}$

Size of first level index = $2^{18} \times 1 \text{ KB} = 256 \text{ MB}$

No. of index blocks in second level = $\frac{2^{18}}{32} = 2^{17}$

Size of second level index = $2^{17} \times 1 \text{ KB} = 8 \text{ MB}$

No. of index blocks in third level = $\frac{2^{17}}{32} = 2^{16}$

Size of third level index = $2^{16} \times 1 \text{ KB} = 256 \text{ KB}$

No. of index blocks in fourth level = $\frac{2^{16}}{32} = 2^{15}$

Size of fourth level index = $2^{15} \times 1 \text{ KB} = 8 \text{ KB}$

No. of index blocks in fifth level = $\frac{8}{32} = 1$

Size of fifth level index = $1 \times 1 \text{ KB} = 1 \text{ KB}$

Master Index size = $256 \text{ MB} + 8 \text{ MB} + 256 \text{ KB} + 8 \text{ KB} + 1 \text{ KB} = 264.265 \text{ MB}$

34 votes

-- Arjun Suresh (332k points)



- ✓ Answer: 3

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Size of each index entry = $14 + 2 = 16 \text{ B}$

$$\text{Blocking factor of record file} = \frac{\text{Block size}}{\text{Record size}} = 512 \text{ B}/64 \text{ B} = 8$$

$$\text{Blocking factor of index file} = \frac{\text{Block size}}{\text{Index entry size}} = 512 \text{ B}/16 \text{ B} = 32$$

$$\text{No. of Blocks needed for data file} = \frac{\text{No. of Records}}{\text{Blocking factor of record file}} = 16 \text{ K}/8 = 2 \text{ K}$$

No. of first level index entries = No. of Data Blocks needed for data file = 2 K

$$\text{No. of first level index blocks} = \lceil \frac{\text{No. of first level index entries}}{\text{Blocking factor of index file}} \rceil = \lceil \frac{2K}{32} \rceil = 64$$

No. of second level index entries = No. of first level index blocks = 64

$$\text{No. of second level index blocks} = \lceil \frac{\text{No. of second level index entries}}{\text{Blocking factor of index file}} \rceil = \lceil \frac{64}{32} \rceil = 2$$

No. of third level index entries = No. of second level index blocks = 2

$$\text{No. of third level index blocks} = \lceil \frac{\text{No. of third level index entries}}{\text{Blocking factor of index file}} \rceil = \lceil \frac{2}{32} \rceil = 1$$

👍 56 votes

-- Rajarshi Sarkar (27.9k points)



- ✓ [classroom.gateoverflow.in](#)
- Indexing will be on Occupation field because Occupation field lexicographically sorted will give the sequence 1, 3, 2, 5, 4.

Correct Answer: C

👍 71 votes

-- Digvijay (44.9k points)



- ✓ There are several types of ordered indexes. A **primary index** is specified on the *ordering key field* of an **ordered file** of records. Recall from **Section 17.7** that an ordering key field is used to *physically order* the file records on disk, and every record has a *unique value* for that field. If the ordering field is not a key field- that is, if numerous records in the file can have the same value for the ordering field— another type of index, called a **clustering index**, can be used. The data file is called a **clustered file** in this latter case. Notice that a file can have at most one physical ordering field, so it can have at most one primary index or one clustering index, *but not both*.

Reference -> Database Systems book BY Navathe, 6th Edition, **18.1 Types of Single- Level Ordered Indexes** Page **no. 632**.

Answer should be A.

👍 33 votes

-- Akash Kanase (36k points)



- ✓ Content of an index will be <key, block pointer> and so will have size $6 + 10 = 16$.

In the first level, there will be an entry for each record of the file. So, total size of first-level index

$$= 16384 * 16$$

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No. of blocks in the first-level = Size of first-level index / block size

$$= 16384 * 16 / 1024$$

$$= 16 * 16 = 256$$

In the second-level there will be an entry for each block in the first level. So, total number of entries = 256 and total size of

second-level index

$$\begin{aligned} &= \text{No. of entries} * \text{size of an entry} \\ &= 256 * 16 \end{aligned}$$

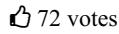
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$$\begin{aligned} \text{No. of blocks in second-level index} &= \text{Size of second-level index / block size} \\ &= 256 * 16 / 1024 \end{aligned}$$

$$= 4$$

Correct Answer: C



72 votes

-- gatecse (63.3k points)



3.7.7 Indexing: GATE CSE 2011 | Question: 39 top ↗

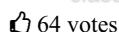
↗ <https://gateoverflow.in/2141>

- ✓ (C) Hashing works well on the 'equal' queries, while ordered indexing works well better on range queries too. For ex consider B+ Tree, once you have searched a key in B+ tree , you can find range of values via the block pointers pointing to another block of values on the leaf node level.

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64 votes

-- Prateeksha Keshari (1.7k points)



3.7.8 Indexing: GATE CSE 2013 | Question: 15 top ↗

↗ <https://gateoverflow.in/1437>

- ✓ Answer is C).

Index can be created using any column or combination of column which need not be unique. So, A, B are not the answers.

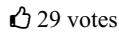
Indexed column is used to sort rows of table.Whole data record of file is sorted using index so, C is correct option. (Simple video explains this).



Video:



Video:



29 votes

-- prashant singh (337 points)



3.7.9 Indexing: GATE CSE 2015 Set 1 | Question: 24 top ↗

↗ <https://gateoverflow.in/8222>

- ✓ Clustered- this is the definition of clustered indexing and for the same reason a table can have only one clustered index.

<http://www.ece.rutgers.edu/~yyzhang/spring03/notes/7-B+tree.ppt>

Correct Answer: C

References



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37 votes

-- Arjun Suresh (332k points)



3.7.10 Indexing: GATE CSE 2020 | Question: 54 top ↗

↗ <https://gateoverflow.in/333177>

Given,

1. Search Key: 12 bytes
2. Tree Pointer: 8 bytes
3. Block Size: 4096 bytes
4. Number of database records: 10^6

Since it's a B^+ tree, an internal node only has search key values and tree pointers. Let p be the order of an internal node. Hence,

$$p(8) + (p-1)(12) \leq 4096$$

which gives $p \leq 205.4$.

Therefore $p = 205$

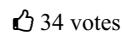
Now,

Level	Nodes	Keys	Pointers
1	1	204	205
2	205	204×205	205^2
3	205^2	204×205^2	205^3

Level 3 alone has approximately 8.5×10^6 entries. So we can be sure that a 3-level B^+ tree is sufficient to index 10^6 records.

So to access any record (in the worst case), we need 3 block access to search for the record in the index along with 1 more access to actually access the record.

Hence, 4 accesses are required.



34 votes

-- Debasish Das (1.5k points)



ANS = 698 .

Index is being built on attribute "ANum" which is Candidate Key, but Given that file is Sorted on Primary Key "Roll No".

This indicates that The Index must a **Secondary Index**, (data records not being physically ordered as per the index making a dense record necessary) so "THERE SHOULD EXIST AN INDEX RECORD FOR **EVERY RECORD** of Original 'Student Table'".

=> Also this Line: "Assume that Records of data file and index file are not split across disc blocks".

This indicates **UNSPANNED STRATEGY**.

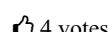
With This Knowledge, let's see the Data given.

→ Record Size in Index = $12 + 7 = 19$ B ('ANum' key size + Record pointer Size), and Block Size = 4096 B

→ So number of Index records in 1 Block = $\lfloor \frac{4096}{19} \rfloor = 215$ records in 1 block (Remember again, unspanned strategy).

→ So number of blocks in the Index file = $\frac{\text{Total Number of records}}{\text{Records per block}} = \left\lceil \frac{1,50,000}{215} \right\rceil = 698$.

(Recall that this is Secondary Index)



4 votes

-- Amcodes (745 points)



3.8.1 Joins: GATE CSE 2004 | Question: 14 top

<https://gateoverflow.in/1011>

Consider the following relation schema pertaining to a students database:

- Students (rollno, name, address)
- Enroll (rollno, courseno, coursename)

where the primary keys are shown underlined. The number of tuples in the student and Enroll tables are 120 and 8 respectively. What are the maximum and minimum number of tuples that can be present in (Student * Enroll), where '*' denotes natural join?

- A. 8, 8
- B. 120, 8

- C. 960,8
D. 960,120

gate2004-cse databases easy joins natural-join

Answer ↗

3.8.2 Joins: GATE CSE 2012 | Question: 50 top ↗

↗ <https://gateoverflow.in/2180>



Consider the following relations A , B and C :

A		
ID	Name	Age
12	Arun	60
15	Shreya	24
99	Rohit	11

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B		
ID	Name	Age
15	Shreya	24
25	Hari	40
98	Rohit	20
99	Rohit	11

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C		
ID	Phone	Area
10	2200	02
99	2100	01

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How many tuples does the result of the following relational algebra expression contain? Assume that the schema of $A \cup B$ is the same as that of A .

$$(A \cup B) \bowtie_{A.Id > 40 \vee C.Id < 15} C$$

- A. 7
B. 4
C. 5
D. 9

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gate2012-cse databases joins normal

Answer ↗

3.8.3 Joins: GATE CSE 2014 Set 2 | Question: 30 top ↗

↗ <https://gateoverflow.in/1989>



Consider a join (relation algebra) between relations $r(R)$ and $s(S)$ using the nested loop method. There are 3 buffers each of size equal to disk block size, out of which one buffer is reserved for intermediate results. Assuming $\text{size}(r(R)) < \text{size}(s(S))$, the join will have fewer number of disk block accesses if

- A. relation $r(R)$ is in the outer loop.
B. relation $s(S)$ is in the outer loop.
C. join selection factor between $r(R)$ and $s(S)$ is more than 0.5.
D. join selection factor between $r(R)$ and $s(S)$ is less than 0.5.

gate2014-cse-set2 databases normal joins

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Answer ↗

3.8.4 Joins: GATE IT 2005 | Question: 82a top ↗

↗ <https://gateoverflow.in/3847>



A database table T_1 has 2000 records and occupies 80 disk blocks. Another table T_2 has 400 records and occupies 20 disk blocks. These two tables have to be joined as per a specified join condition that needs to be evaluated for every pair of records from these two tables. The memory buffer space available can hold exactly one block of records for T_1 and one block of records for T_2 simultaneously at any point in time. No index is available on either table.

If Nested-loop join algorithm is employed to perform the join, with the most appropriate choice of table to be used in outer loop, the number of block accesses required for reading the data are

- A. 800000
B. 40080
C. 32020
D. 100

gate2005-it databases normal joins

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Answer ↗



A database table T_1 has 2000 records and occupies 80 disk blocks. Another table T_2 has 400 records and occupies 20 disk blocks. These two tables have to be joined as per a specified join condition that needs to be evaluated for every pair of records from these two tables. The memory buffer space available can hold exactly one block of records for T_1 and one block of records for T_2 simultaneously at any point in time. No index is available on either table.

If, instead of Nested-loop join, Block nested-loop join is used, again with the most appropriate choice of table in the outer loop, the reduction in number of block accesses required for reading the data will be

- A. 0
- B. 30400
- C. 38400
- D. 798400

[gate2005-it](#) [databases](#) [normal](#) [joins](#)

Answer



Consider the relations $r_1(P, Q, R)$ and $r_2(R, S, T)$ with primary keys P and R respectively. The relation r_1 contains 2000 tuples and r_2 contains 2500 tuples. The maximum size of the join $r_1 \bowtie r_2$ is :

- A. 2000
- B. 2500
- C. 4500
- D. 5000

[gate2006-it](#) [databases](#) [joins](#) [natural-join](#) [normal](#)

Answer



Consider the following relation schemas :

- b-Schema = (b-name, b-city, assets)
- a-Schema = (a-num, b-name, bal)
- d-Schema = (c-name, a-number)

Let branch, account and depositor be respectively instances of the above schemas. Assume that account and depositor relations are much bigger than the branch relation.

Consider the following query:

$\Pi_{c\text{-name}} (\sigma_{b\text{-city} = "Agra"} \wedge \text{bal} < 0) \text{ branch} \bowtie (\text{account} \bowtie \text{depositor})$

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Which one of the following queries is the most efficient version of the above query ?

- A. $\Pi_{c\text{-name}} (\sigma_{\text{bal} < 0} (\sigma_{b\text{-city} = "Agra"} \text{ branch} \bowtie \text{account}) \bowtie \text{depositor})$
- B. $\Pi_{c\text{-name}} (\sigma_{b\text{-city} = "Agra"} \text{ branch} \bowtie (\sigma_{\text{bal} < 0} \text{ account} \bowtie \text{depositor}))$
- C. $\Pi_{c\text{-name}} ((\sigma_{b\text{-city} = "Agra"} \text{ branch} \bowtie \sigma_{b\text{-city} = "Agra"} \wedge \text{bal} < 0 \text{ account}) \bowtie \text{depositor})$
- D. $\Pi_{c\text{-name}} (\sigma_{b\text{-city} = "Agra"} \text{ branch} \bowtie (\sigma_{b\text{-city} = "Agra"} \wedge \text{bal} < 0 \text{ account} \bowtie \text{depositor}))$

[gate2007-it](#) [databases](#) [joins](#) [relational-algebra](#) [normal](#)

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Answer

Answers: Joins



- ✓ Rollno in students is key, ans students table has 120 tuples, In Enroll table rollno is FK referencing to Students table. In natural join it'll return the records where the rollno value of enroll matches with the rollno of students so, in both conditions min and max records will be resulted (8, 8). hence A is the answer.

Hint: table which has non-key, no of records of that will be resulted.

47 votes

-- Manu Thakur (34k points)

3.8.2 Joins: GATE CSE 2012 | Question: 50 top

<https://gateoverflow.in/2180>



- Given relations A, B and C :

A		
ID	Name	Age
12	Arun	60
15	Shreya	24
99	Rohit	11

B		
ID	Name	Age
15	Shreya	24
25	Hari	40
98	Rohit	20
99	Rohit	11

C		
ID	Phone	Area
10	2200	02
99	2100	01

This is an example of theta join and we know: $R \bowtie_{\theta} S = \sigma_{\theta}(R \times S)$

$$\therefore (A \cup B) \bowtie_{A.Id > 40 \vee C.Id < 15} C = (A.Id > 40 ((A \cup B) \times C)) \cup (C.Id < 15 ((A \cup B) \times C))$$

To make the query more efficient we can perform the select operation before the cross product.

$$\therefore (A \cup B) \bowtie_{A.Id > 40 \vee C.Id < 15} C = (A.Id > 40 (A \cup B) \times C) \cup ((A \cup B) \times C.Id < 15 C)$$

Now calculate $A \cup B$:

ID	Name	Age
12	Arun	60
15	Shreya	24
25	Hari	40
98	Rohit	20
99	Rohit	11

Please note that union is a set operation and duplicates will not be included by default.

First perform cross-product $(A.Id > 40 (A \cup B) \times C)$, i.e., Multiply each row of $A.Id > 40 (A \cup B)$ with each row of C :

ID	Name	Age	C.ID	Phone	Area
98	Rohit	20	10	2200	02
98	Rohit	20	99	2100	01
99	Rohit	11	10	2200	02
99	Rohit	11	99	2100	01

Now perform cross-product $((A \cup B) \times C.Id < 15 C)$, i.e., Multiply each row of $(A \cup B)$ with each row of $C.Id < 15 C$:

ID	Name	Age	C.ID	Phone	Area
12	Arun	60	10	2200	02
15	Shreya	24	10	2200	02
25	Hari	40	10	2200	02

Now take the union: $(A.Id > 40 (A \cup B) \times C) \cup ((A \cup B) \times C.Id < 15 C)$

We will get:

ID	Name	Age	C.ID	Phone	Area
12	Arun	60	10	2200	02
15	Shreya	24	10	2200	02
25	Hari	40	10	2200	02
98	Rohit	20	10	2200	02
98	Rohit	20	99	2100	01
99	Rohit	11	10	2200	02
99	Rohit	11	99	2100	01

which has 7 Tuples, hence answer is A.

1 like 8 votes

-- Sourabh Gupta (4k points)

50. For C.ID = 10, all tuples from $A \cup B$ satisfies the join condition, hence 5 tuples (union of A and B has only 5 tuples are 2 of them are repeating for Shreya and Rohit) will be returned. Now, for C.ID = 99, A.ID = 99 and A.ID = 98 (for A.ID = 98, we need to assume A \cup B, has the same schema s A as told in the question) satisfies the condition A.ID > 40, and hence two tuples are returned. So, number of tuples = 5 + 2 = 7.

The output will be:

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Id	Name	Age	Id	Phone	Area
12	Arun	60	10	2200	02
15	Shreya	24	10	2200	02
99	Rohit	11	10	2200	02
25	Hari	40	10	2200	02
98	Rohit	20	10	2200	02
99	Rohit	11	99	2100	01
98	Rohit	20	99	2100	01

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Correct Answer: A

1 like 51 votes

-- Arjun Suresh (332k points)

3.8.3 Joins: GATE CSE 2014 Set 2 | Question: 30 [top](#)

→ <https://gateoverflow.in/1989>



- ✓ In joining B and B using nested loop method, with A in outer loop two factors are involved.

- No. of blocks containing all rows in A should be fetched
- No. of Rows A times no of Blocks containing all Rows of B

(in worst case all rows of B are matched with all rows of A).

In above ques, $|R| < |S|$

(i) will be less when number of rows in outer table is less since less no of rows will take less no. of blocks

(ii) if we keep R in outer loop, no. of rows in R are less and no. of blocks in S are more

If we keep S in outer loop, no of rows in S are more and no. of blocks in R are less.

In (ii) block accesses will be multiplication and will come same in both cases.

So, (i) will determine no of block accesses

So, answer is A.

1 like 20 votes

-- Anurag Semwal (6.7k points)



3.8.4 Joins: GATE IT 2005 | Question: 82a [top](#)

→ <https://gateoverflow.in/3847>

- ✓ We just have to think which table would be in the outer loop. To minimize block accesses, we have to put that table outside having fewer records because for each outer record, one block access inside will be required.

Therefore, putting 2nd table outside,

- for every 400 records
 - 80 block accesses in the first table
 - = 32000
- 20 block accesses of the outer table.

So, the answer comes out to be $32000 + 20 = 32020$

Correct Answer: C.

84 votes

-- Vishesh Bajpai (383 points)

Reference: http://en.wikipedia.org/wiki/Nested_loop_join

As per this reference this algorithm will involve $nr * bs + br$ block transfers

T_1 can be either R or T_2

- If R is T_1 then total number of block accesses is $2000 \times 20 + 80 = 40080$
- If R is T_2 then total number of block accesses is $400 \times 80 + 20 = 32020$

So, better is the second case (32020) Hence, I go for option C.

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References



42 votes

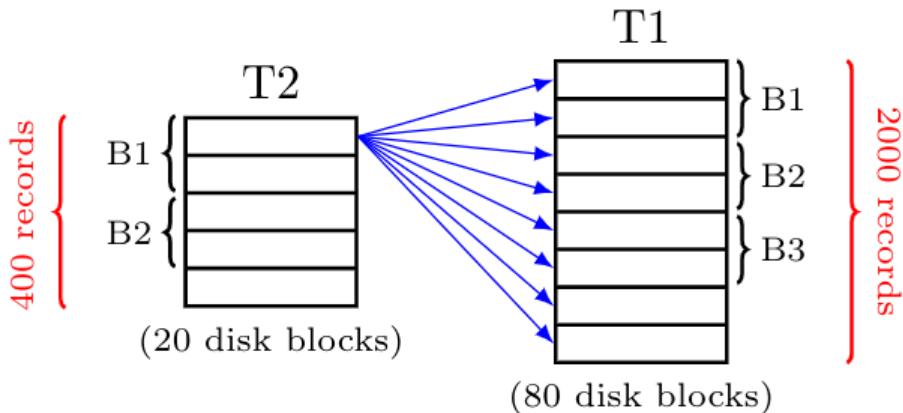
-- Sankaranarayanan P.N (8.5k points)

3.8.5 Joins: GATE IT 2005 | Question: 82b top

<https://gateoverflow.in/3848>



- ✓ In Nested loop join for each tuple in first table we scan through all the tuples in second table.



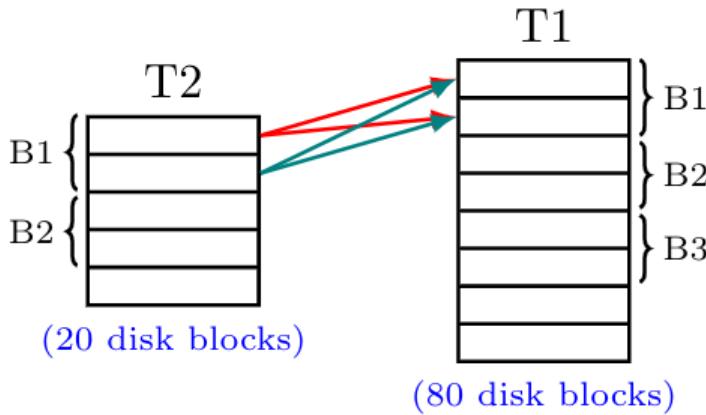
Here we will take table T_2 as the outer table in nested loop join algorithm. The number of block accesses then will be $20 + (400 \times 80) = 32020$

In block nested loop join we keep 1 block of T_1 in memory and 1 block of T_2 in memory and do join on tuples.

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For every block in T1 we need to load all blocks of T2. So number of block accesses is $80 \times 20 + 20 = 1620$

So, the difference is $32020 - 1620 = 30400$

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(B) 30400

65 votes

-- Omesh Pandita (1.9k points)

3.8.6 Joins: GATE IT 2006 | Question: 14 top

→ <https://gateoverflow.in/3553>



- ✓ The common attribute is R and it is the primary key in the second relation. So R value should be distinct (primary key implies unique) for 2500 rows. Hence when we do join, maximum possible number of tuples is 2000.

Correct option is **A**.

36 votes

-- Sankaranarayanan P.N (8.5k points)

3.8.7 Joins: GATE IT 2007 | Question: 68 top

→ <https://gateoverflow.in/3513>



- ✓ It should be **A**. As in **B** we are doing a join between two massive table whereas in **A** we are doing join between relatively smaller table and larger one and the output that this inner table gives (which is smaller in comparison to joins that we are doing in **B**) is used for join with depositer table with the selection condition.

Options **C** and **D** are invalid as there is no b-city column in a-Schema.

Lets see in detail. Let there be 100 different branches. Say about 10% of accounts are below 0. Also, let there be 10,000 accounts in a branch amounting to 1,000,000 total accounts. A customer can have multiple accounts, so let there be on average 2 accounts per customer. So, this amounts to 2,000,000 total entries in depositor table. Lets assume these assumptions are true for all the branches. So, now lets evaluate options **A** and **B**.

1. All the accounts in Agra branch, filter by positive balance, and then depositor details of them. So,

- Get branch name from branch table after processing 100 records
- Filter 10,000 accounts after processing 1,000,000 accounts belonging to Agra
- Filter 1000 accounts after processing 10,000 accounts for positive balance
- Get 500 depositor details after processing 2,000,000 entries for the given 1000 accounts (assuming 1 customer having 2 accounts). So, totally this amounts to 2,000,000,000 record processing.
- So totally ≈ 2 billion records needs processing.

2. All the positive balance accounts are found first, and then those in Agra are found.

- Filter 100,000 accounts after processing 1,000,000 accounts having positive balance
- Find the depositor details of these accounts. So, 100,000*2,000,000 records need processing and this is a much larger value than for query **A**. Even if we reduce the percentage of positive balance (10 we assumed) the record processing of query **A** will also get reduced by same rate. So, overall query **A** is much better than query **B**.

59 votes

-- Shaun Patel (6.1k points)

3.9

Multivalued Dependency 4nf (1) top



Consider the following implications relating to functional and multivalued dependencies given below, which may or may not be correct.

- i. if $A \rightarrow\!\!\rightarrow B$ and $A \rightarrow\!\!\rightarrow C$ then $A \rightarrow BC$
- ii. if $A \rightarrow B$ and $A \rightarrow C$ then $A \rightarrow\!\!\rightarrow BC$
- iii. if $A \rightarrow\!\!\rightarrow BC$ and $A \rightarrow B$ then $A \rightarrow C$
- iv. if $A \rightarrow BC$ and $A \rightarrow\!\!\rightarrow B$ then $A \rightarrow\!\!\rightarrow C$

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Exactly how many of the above implications are valid?

- A. 0
- B. 1
- C. 2
- D. 3

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Answer

Answers: Multivalued Dependency 4nf



- ✓ a. If $A \rightarrow\!\!\rightarrow B$ and $A \rightarrow\!\!\rightarrow C$ then $A \rightarrow BC$. So FALSE
- b. If $A \rightarrow B$ and $A \rightarrow C$ then $A \rightarrow BC$. So $A \rightarrow\!\!\rightarrow BC$ TRUE..
- c. If $A \rightarrow\!\!\rightarrow BC$ and $A \rightarrow B$ here B is Subset of AB and (A intersection BC) is phi so $A \rightarrow B$ but not $A \rightarrow C$ so FALSE (**Coalescence rule**)
- d. If $A \rightarrow BC$ then $A \rightarrow C$ so $A \rightarrow\!\!\rightarrow C$ TRUE
if $A \rightarrow B$ then $A \rightarrow\!\!\rightarrow B$ holds but reverse not true.

Correct Answer: C

34 votes

-- Digvijay (44.9k points)



Let r be a relation instance with schema $R = (A, B, C, D)$. We define $r_1 = \pi_{A,B,C}(R)$ and $r_2 = \pi_{A,D}(r)$. Let $s = r_1 * r_2$ where $*$ denotes natural join. Given that the decomposition of r into r_1 and r_2 is lossy, which one of the following is TRUE?

- A. $s \subset r$
- B. $r \cup s = r$
- C. $r \subset s$
- D. $r * s = s$

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Answer



The following functional dependencies hold for relations $R(A, B, C)$ and $S(B, D, E)$.

- $B \rightarrow A$
- $A \rightarrow C$

The relation R contains 200 tuples and the relation S contains 100 tuples. What is the maximum number of tuples possible in the natural join $R \bowtie S$?

- A. 100
- B. 200
- C. 300
- D. 2000

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Answer

3.10.3 Natural Join: GATE CSE 2015 Set 2 | Question: 32 [top](#)<https://gateoverflow.in/8151>

Consider two relations $R_1(A, B)$ with the tuples $(1, 5), (3, 7)$ and $R_2(A, C) = (1, 7), (4, 9)$. Assume that $R(A, B, C)$ is the full natural outer join of R_1 and R_2 . Consider the following tuples of the form (A, B, C) :

$a = (1, 5, null), b = (1, null, 7), c = (3, null, 9), d = (4, 7, null), e = (1, 5, 7), f = (3, 7, null), g = (4, null, 9)$.

Which one of the following statements is correct?

- A. R contains a, b, e, f, g but not c, d .
- B. R contains all a, b, c, d, e, f, g .
- C. R contains e, f, g but not a, b .
- D. R contains e but not f, g .

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Answer

Answers: Natural Join

3.10.1 Natural Join: GATE CSE 2005 | Question: 30 [top](#)<https://gateoverflow.in/1366>

- ✓ Answer is C $r \subset s$.

r			
A	B	C	D
1	2	3	3
1	5	3	4

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r1		
A	B	C
1	2	3
1	5	3

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r2	
A	D
1	3
1	4

s = r1 * r2			
A	B	C	D
1	2	3	3
1	2	3	4
1	5	3	4
1	5	3	4

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All the rows of r are in s (marked bold). So, $r \subset s$.

And one more result $r * s = r$.

👉 56 votes

-- Vikrant Singh (11.2k points)

3.10.2 Natural Join: GATE CSE 2010 | Question: 43 [top](#)<https://gateoverflow.in/2344>

- ✓ (A) 100.

Natural join will combine tuples with same value of the common rows(if there are two common rows then both values must be equal to get into the resultant set). So by this definition we can get at the max only 100 common values.

👉 37 votes

-- Aravind (2.8k points)

3.10.3 Natural Join: GATE CSE 2015 Set 2 | Question: 32 [top](#)<https://gateoverflow.in/8151>

$R_1(A, B)$:	
A	B
1	5
3	7

$R_2(A, C)$:	
A	C
1	7
4	9

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Now , if we do full natural outer join:

A	B	C
1	5	7
3	7	NULL
4	NULL	9

So, option (C) is correct.

1 37 votes

-- worst_engineer (2.8k points)

3.11

Referential Integrity (4) [top](#)

3.11.1 Referential Integrity: GATE CSE 1997 | Question: 6.10, ISRO2016-54 [top](#)

Let $R(a, b, c)$ and $S(d, e, f)$ be two relations in which d is the foreign key of S that refers to the primary key of R . Consider the following four operations R and S

- I. Insert into R
- II. Insert into S
- III. Delete from R
- IV. Delete from S

Which of the following can cause violation of the referential integrity constraint above?

- A. Both I and IV
- B. Both II and III
- C. All of these
- D. None of these

[gate1997](#) [databases](#) [referential-integrity](#) [easy](#) [isro2016](#)

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Answer 

3.11.2 Referential Integrity: GATE CSE 2005 | Question: 76 [top](#)

[https://gateoverflow.in/1399](#)



The following table has two attributes A and C where A is the primary key and C is the foreign key referencing A with on-delete cascade.

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A	C
2	4
3	4
4	3
5	2
7	2
9	5
6	4

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The set of all tuples that must be additionally deleted to preserve referential integrity when the tuple $(2, 4)$ is deleted is:

- A. $(3, 4)$ and $(6, 4)$
- B. $(5, 2)$ and $(7, 2)$
- C. $(5, 2), (7, 2)$ and $(9, 5)$
- D. $(3, 4), (4, 3)$ and $(6, 4)$

[gate2005-cse](#) [databases](#) [referential-integrity](#) [normal](#)

Answer 



Consider the following tables T_1 and T_2 .

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T_1		T_2	
P	Q	R	S
2	2	2	2
3	8	8	3
7	3	3	2
5	8	9	7
6	9	5	7
8	5	7	2
9	8		

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In table T_1 P is the primary key and Q is the foreign key referencing R in table T_2 with on-delete cascade and on-update cascade. In table T_2 , R is the primary key and S is the foreign key referencing P in table T_1 with on-delete set NULL and on-update cascade. In order to delete record $\langle 3, 8 \rangle$ from the table T_1 , the number of additional records that need to be deleted from table T_1 is

Answer



Consider the following statements S_1 and S_2 about the relational data model:

- S_1 : A relation scheme can have at most one foreign key.
- S_2 : A foreign key in a relation scheme R cannot be used to refer to tuples of R .

Which one of the following choices is correct?

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- A. Both S_1 and S_2 are true
 B. S_1 is true and S_2 is false
 C. S_1 is false and S_2 is true
 D. Both S_1 and S_2 are false

Answer

Answers: Referential Integrity



R		
a (PK)	b	c
1		
2		

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S		
d (FK referring to PK of R)	e	f
gateoverflow.2		
1		

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- Insert into R cannot cause any violation.
- Insert into S can cause violation if any value is inserted into d of S , which value is not in a of R .
- Delete from S cannot cause any violation.
- Delete from R can cause violation if any tuple is deleted, and as a result a value in 'a' gets deleted which is referenced to by 'd' in S .

Correct Answer: B

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42 votes

-- Sourav Roy (2.9k points)



✓ (C)

Since deleting (2, 4), since 2 is a primary key, you have to delete its foreign key occurrence i.e (5, 2) and (7, 2). Since we are deleting 5, and 7 we have deleted its foreign key occurrence i.e (9, 5).

There is no foreign key occurrence for 9.

43 votes

-- Aravind (2.8k points)

3.11.3 Referential Integrity: GATE CSE 2017 Set 2 | Question: 19 [top](#)

<https://gateoverflow.in/118236>



- ✓ As Q refers to R so, deleting 8 from Q won't be an issue, however S refers P. But as the relationship given is on delete set NULL, 3 will be deleted from T1 and the entry in T2 having 3 in column S will be set to NULL. So, no more deletions. Answer is 0.

74 votes

-- Prateek Kumar (1.1k points)

3.11.4 Referential Integrity: GATE CSE 2021 Set 2 | Question: 6 [top](#)

<https://gateoverflow.in/357534>



- ✓ Both S_1 and S_2 are FALSE.

In a relation scheme multiple foreign attributes can be present referring to primary keys of other relation schemes. A typical example is an EXAM_RESULTS(sid,eid,marks) scheme where sid and eid are foreign keys referring to the primary keys in STUDENT and EXAM schemes respectively.

S_2 is FALSE because a foreign key can refer to the same scheme (self-referencing foreign key). A typical example is an EMPLOYEE(eid, mid, ...) scheme where mid is the Manager ID referring to the primary key eid of the same scheme.

3 votes

-- gatecse (63.3k points)

3.12

Relational Algebra (26) [top](#)

3.12.1 Relational Algebra: GATE CSE 1992 | Question: 13b [top](#)

<https://gateoverflow.in/43581>



Suppose we have a database consisting of the following three relations:

FREQUENTS	(CUSTOMER, HOTEL)
SERVES	(HOTEL, SNACKS)
LIKES	(CUSTOMER, SNACKS)

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The first indicates the hotels each customer visits, the second tells which snacks each hotel serves and last indicates which snacks are liked by each customer. Express the following query in relational algebra:

Print the hotels the serve the snack that customer Rama likes.

gate1992 databases relational-algebra normal descriptive

Answer

3.12.2 Relational Algebra: GATE CSE 1994 | Question: 13 [top](#)

<https://gateoverflow.in/2509>



Consider the following relational schema:

- COURSES (cno, cname)
- STUDENTS (rollno, sname, age, year)
- REGISTERED_FOR (cno, rollno)

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The underlined attributes indicate the primary keys for the relations. The 'year' attribute for the STUDENTS relation indicates the year in which the student is currently studying (First year, Second year etc.).

- Write a relational algebra query to print the roll number of students who have registered for cno 322.
- Write a SQL query to print the age and year of the youngest student in each year.

gate1994 databases relational-algebra sql normal descriptive

Answer 

3.12.3 Relational Algebra: GATE CSE 1994 | Question: 3.8 top

<https://gateoverflow.in/2494>



Give a relational algebra expression using only the minimum number of operators from $(\cup, -)$ which is equivalent to $R \cap S$.

gate1994 databases relational-algebra normal descriptive

Answer 

3.12.4 Relational Algebra: GATE CSE 1995 | Question: 27 top

<https://gateoverflow.in/2666>



Consider the relation scheme.

AUTHOR	(ANAME, INSTITUTION, ACITY, AGE)
PUBLISHER	(PNAME, PCITY)
BOOK	(TITLE, ANAME, PNAME)

Express the following queries using (one or more of) SELECT, PROJECT, JOIN and DIVIDE operations.

- Get the names of all publishers.
- Get values of all attributes of all authors who have published a book for the publisher with PNAME='TECHNICAL PUBLISHERS'.
- Get the names of all authors who have published a book for any publisher located in Madras

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Answer 

3.12.5 Relational Algebra: GATE CSE 1996 | Question: 27 top

<https://gateoverflow.in/2779>



A library relational database system uses the following schema

- USERS (User#, User Name, Home Town)
- BOOKS (Book#, Book Title, Author Name)
- ISSUED (Book#, User#, Date)

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Explain in one English sentence, what each of the following relational algebra queries is designed to determine

- $\sigma_{User\#=6}(\pi_{User\#}, Book\ Title ((USERS \bowtie ISSUED) \bowtie BOOKS))$
- $\pi_{Author\ Name}(BOOKS \bowtie \sigma_{Home\ Town=Delhi}(USERS \bowtie ISSUED))$

gate1996 databases relational-algebra descriptive

Answer 

3.12.6 Relational Algebra: GATE CSE 1997 | Question: 76-a top

<https://gateoverflow.in/19838>



Consider the following relational database schema:

- EMP (eno name, age)
- PROJ (pno name)
- INVOLVED (eno, pno)

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EMP contains information about employees. PROJ about projects and involved about which employees involved in which projects. The underlined attributes are the primary keys for the respective relations.

What is the relational algebra expression containing one or more of $\{\sigma, \pi, \times, \rho, -\}$ which is equivalent to SQL query.

```
select eno from EMP | INVOLVED where EMP.eno=INVOLVED.eno and INVOLVED.pno=3
```

gate1997 databases sql relational-algebra descriptive

Answer 



Given two union compatible relations $R_1(A, B)$ and $R_2(C, D)$, what is the result of the operation $R_1 \bowtie_{A=C \wedge B=D} R_2$?

- A. $R_1 \cup R_2$
- B. $R_1 \times R_2$
- C. $R_1 - R_2$
- D. $R_1 \cap R_2$

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[gate1998](https://gate1998.gateoverflow.in) [normal](https://normal.gateoverflow.in) [relational-algebra](https://relational-algebra.gateoverflow.in)

Answer



Consider the following relational database schemes:

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- COURSES (Cno, Name)
- PRE_REQ(Cno, Pre_Cno)
- COMPLETED (Student_no, Cno)

COURSES gives the number and name of all the available courses.

PRE_REQ gives the information about which courses are pre-requisites for a given course.

COMPLETED indicates what courses have been completed by students

Express the following using relational algebra:

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List all the courses for which a student with Student_no 2310 has completed all the pre-requisites.

[gate1998](https://gate1998.gateoverflow.in) [databases](https://databases.gateoverflow.in) [relational-algebra](https://relational-algebra.gateoverflow.in) [normal](https://normal.gateoverflow.in) [descriptive](https://descriptive.gateoverflow.in)

Answer



Consider the join of a relation R with a relation S . If R has m tuples and S has n tuples then the maximum and minimum sizes of the join respectively are

- A. $m + n$ and 0
- B. mn and 0
- C. $m + n$ and $|m - n|$
- D. mn and $m + n$

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Answer



Given the relations

- employee (name, salary, dept-no), and
- department (dept-no, dept-name, address),

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Which of the following queries cannot be expressed using the basic relational algebra operations ($\sigma, \pi, \times, \bowtie, \cup, \cap, -$)?

- A. Department address of every employee
- B. Employees whose name is the same as their department name
- C. The sum of all employees' salaries
- D. All employees of a given department

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Answer



Suppose the adjacency relation of vertices in a graph is represented in a table $\text{Adj}(X, Y)$. Which of the following queries cannot be expressed by a relational algebra expression of constant length?

- A. List all vertices adjacent to a given vertex
- B. List all vertices which have self loops
- C. List all vertices which belong to cycles of less than three vertices
- D. List all vertices reachable from a given vertex

[gate2001-cse](#) [databases](#) [relational-algebra](#) [normal](#)

Answer



Let r and s be two relations over the relation schemes R and S respectively, and let A be an attribute in R . The relational algebra expression $\sigma_{A=a}(r \bowtie s)$ is always equal to

- A. $\sigma_{A=a}(r)$
- B. r
- C. $\sigma_{A=a}(r) \bowtie s$
- D. None of the above

[gate2001-cse](#) [databases](#) [relational-algebra](#)

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Answer



A university placement center maintains a relational database of companies that interview students on campus and make job offers to those successful in the interview. The schema of the database is given below:

COMPANY (<u>cname</u> , clocation)	STUDENT (<u>srollno</u> , sname, sdegree)
INTERVIEW (<u>cname</u> , <u>srollno</u> , <u>idate</u>)	OFFER (<u>cname</u> , <u>srollno</u> , <u>osalary</u>)

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The COMPANY relation gives the name and location of the company. The STUDENT relation gives the student's roll number, name and the degree program for which the student is registered in the university. The INTERVIEW relation gives the date on which a student is interviewed by a company. The OFFER relation gives the salary offered to a student who is successful in a company's interview. The key for each relation is indicated by the underlined attributes

- a. Write a **relational algebra** expressions (using only the operators $\bowtie, \sigma, \pi, \cup, -$) for the following queries.
 - i. List the *rollnumbers* and *names* of students who attended at least one interview but did not receive *any* job offer.
 - ii. List the *rollnumbers* and *names* of students who went for interviews and received job offers from *every* company with which they interviewed.
- b. Write an SQL query to list, for each degree program in which more than *five* students were offered jobs, the name of the degree and the average offered salary of students in this degree program.

[gate2002-cse](#) [databases](#) [normal](#) [descriptive](#) [relational-algebra](#) [sql](#)

Answer



Consider the following SQL query

Select distinct a_1, a_2, \dots, a_n

from r_1, r_2, \dots, r_m

where P

For an arbitrary predicate P , this query is equivalent to which of the following relational algebra expressions?

- A. $\Pi_{a_1, a_2, \dots, a_n} \sigma_p (r_1 \times r_2 \times \dots \times r_m)$

- B. $\Pi_{a_1, a_2, \dots, a_n} \sigma_p (r_1 \bowtie r_2 \bowtie \dots \bowtie r_m)$
- C. $\Pi_{a_1, a_2, \dots, a_n} \sigma_p (r_1 \cup r_2 \cup \dots \cup r_m)$
- D. $\Pi_{a_1, a_2, \dots, a_n} \sigma_p (r_1 \cap r_2 \cap \dots \cap r_m)$

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gate2003-cse databases relational-algebra normal

Answer 

3.12.15 Relational Algebra: GATE CSE 2004 | Question: 51 top ↺

<https://gateoverflow.in/1047>



Consider the relation Student (name, sex, marks), where the primary key is shown underlined, pertaining to students in a class that has at least one boy and one girl. What does the following relational algebra expression produce? (Note: ρ is the rename operator).

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$$\pi_{name}\{\sigma_{sex=female}(\text{Student})\} - \pi_{name}(\text{Student} \bowtie_{(sex=female \wedge x=male \wedge marks \leq m)} \rho_{n,x,m}(\text{Student}))$$

- A. names of girl students with the highest marks
 B. names of girl students with more marks than some boy student
 C. names of girl students with marks not less than some boy student
 D. names of girl students with more marks than all the boy students

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Answer 

3.12.16 Relational Algebra: GATE CSE 2007 | Question: 59 top ↺

<https://gateoverflow.in/2428>



Information about a collection of students is given by the relation studInfo(studId, name, sex). The relation enroll(studId, courseId) gives which student has enrolled for (or taken) what course(s). Assume that every course is taken by at least one male and at least one female student. What does the following relational algebra expression represent?

$$\pi_{courseId}((\pi_{studId}(\sigma_{sex='female'}(\text{studInfo})) \times \pi_{courseId}(\text{enroll})) - \text{enroll})$$

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- A. Courses in which all the female students are enrolled.
 B. Courses in which a proper subset of female students are enrolled.
 C. Courses in which only male students are enrolled.
 D. None of the above

gate2007-cse databases relational-algebra normal

Answer 

3.12.17 Relational Algebra: GATE CSE 2008 | Question: 68 top ↺

<https://gateoverflow.in/491>



Let R and S be two relations with the following schema

$$R(P, Q, R1, R2, R3)$$

$$S(P, Q, S1, S2)$$

where $\{P, Q\}$ is the key for both schemas. Which of the following queries are equivalent?

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- I. $\Pi_P(R \bowtie S)$
 II. $\Pi_P(R) \bowtie \Pi_P(S)$
 III. $\Pi_P(\Pi_{P,Q}(R) \cap \Pi_{P,Q}(S))$
 IV. $\Pi_P(\Pi_{P,Q}(R) - (\Pi_{P,Q}(R) - \Pi_{P,Q}(S)))$

- A. Only I and II
 B. Only I and III
 C. Only I, II and III
 D. Only I, III and IV

gate2008-cse databases relational-algebra normal

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Answer 

3.12.18 Relational Algebra: GATE CSE 2012 | Question: 43 [top](#)

▪ <https://gateoverflow.in/2151>



Suppose $R_1(\underline{A}, B)$ and $R_2(\underline{C}, D)$ are two relation schemas. Let r_1 and r_2 be the corresponding relation instances. B is a foreign key that refers to C in R_2 . If data in r_1 and r_2 satisfy referential integrity constraints, which of the following is **ALWAYS TRUE**?

- A. $\prod_B(r_1) - \prod_C(r_2) = \emptyset$
- B. $\prod_C(r_2) - \prod_B(r_1) = \emptyset$
- C. $\prod_B(r_1) = \prod_C(r_2)$
- D. $\prod_B(r_1) - \prod_C(r_2) \neq \emptyset$

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gate2012-cse databases relational-algebra normal

Answer 

3.12.19 Relational Algebra: GATE CSE 2014 Set 3 | Question: 21 [top](#)

▪ <https://gateoverflow.in/2055>



What is the optimized version of the relation algebra expression $\pi_{A1}(\pi_{A2}(\sigma_{F1}(\sigma_{F2}(r))))$, where $A1, A2$ are sets of attributes in r with $A1 \subset A2$ and $F1, F2$ are Boolean expressions based on the attributes in r ?

- A. $\pi_{A1}(\sigma_{(F1 \wedge F2)}(r))$
- B. $\pi_{A1}(\sigma_{(F1 \vee F2)}(r))$
- C. $\pi_{A2}(\sigma_{(F1 \wedge F2)}(r))$
- D. $\pi_{A2}(\sigma_{(F1 \vee F2)}(r))$

gate2014-cse-set3 databases relational-algebra easy

Answer 

3.12.20 Relational Algebra: GATE CSE 2014 Set 3 | Question: 30 [top](#)

▪ <https://gateoverflow.in/2064>



Consider the relational schema given below, where **eId** of the relation **dependent** is a foreign key referring to **empId** of the relation **employee**. Assume that every employee has at least one associated dependent in the **dependent** relation.

employee (**empId**, **empName**, **empAge**)

dependent (**depId**, **eId**, **depName**, **depAge**)

Consider the following relational algebra query:

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$\Pi_{empId} (employee) - \Pi_{empId} (employee \bowtie_{(empId=eID) \wedge (empAge \leq depAge)} dependent)$

The above query evaluates to the set of **empIds** of employees whose age is greater than that of

- A. some dependent.
- B. all dependents.
- C. some of his/her dependents.
- D. all of his/her dependents.

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gate2014-cse-set3 databases relational-algebra normal

Answer 

3.12.21 Relational Algebra: GATE CSE 2015 Set 1 | Question: 7 [top](#)

▪ <https://gateoverflow.in/8094>



SELECT operation in SQL is equivalent to

- A. The selection operation in relational algebra
- B. The selection operation in relational algebra, except that SELECT in SQL retains duplicates
- C. The projection operation in relational algebra
- D. The projection operation in relational algebra, except that SELECT in SQL retains duplicates

gate2015-cse-set1 databases sql relational-algebra easy

Answer 

3.12.22 Relational Algebra: GATE CSE 2017 Set 1 | Question: 46 [top](#)

<https://gateoverflow.in/118329>



Consider a database that has the relation schema CR(StudentName, CourseName). An instance of the schema CR is as given below.

StudentName	CourseName
SA	CA
SA	CB
SA	goclasses.in CC
SB	CB
SB	CC
SC	CA
SC	CB
SC	CC
SD	CA
SD	CB
SD	goclasses.in CC
SD	CD
SE	CD
SE	CA
SE	CB
SF	CA
SF	CB
SF	goclasses.in CC

The following query is made on the database.

- $T1 \leftarrow \pi_{CourseName} (\sigma_{StudentName=SA} (CR))$
- $T2 \leftarrow CR \div T1$

The number of rows in $T2$ is _____.

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gate2017-cse-set1 databases relational-algebra normal numerical-answers

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Answer 

3.12.23 Relational Algebra: GATE CSE 2018 | Question: 41 [top](#)

<https://gateoverflow.in/204115>



Consider the relations $r(A, B)$ and $s(B, C)$, where $s.B$ is a primary key and $r.B$ is a foreign key referencing $s.B$. Consider the query

$Q : r \bowtie (\sigma_{B < 5}(s))$

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Let LOJ denote the natural left outer-join operation. Assume that r and s contain no null values.

Which of the following is NOT equivalent to Q?

- $\sigma_{B < 5}(r \bowtie s)$
- $\sigma_{B < 5}(r LOJ s)$
- $r LOJ (\sigma_{B < 5}(s))$
- $\sigma_{B < 5}(r) LOJ s$

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gate2018-cse databases relational-algebra normal

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Answer 

3.12.24 Relational Algebra: GATE CSE 2019 | Question: 55 [top](#)

<https://gateoverflow.in/302793>



Consider the following relations $P(X, Y, Z), Q(X, Y, T)$ and $R(Y, V)$.

Table: P

X	Y	Z
X1	Y1	Z1
X1	Y1	Z2
X2	Y2	Z2
X2	Y4	Z4

Table: Qn

X	Y	T
X2	Y1	2
X1	Y2	5
X1	Y1	6
X3	Y3	1

Table: R

Y	V
Y1	V1
Y3	V2
Y2	V3
Y2	V2

How many tuples will be returned by the following relational algebra query?

$$\Pi_x(\sigma_{(P.Y=R.Y \wedge R.V=V2)} (P \times R)) - \Pi_x(\sigma_{(Q.Y=R.Y \wedge Q.T>2)} (Q \times R))$$

Answer: _____

gate2019-cse numerical-answers databases relational-algebra

Answer 

3.12.25 Relational Algebra: GATE CSE 2021 Set 1 | Question: 27 top ↺

<https://gateoverflow.in/357424>



The following relation records the age of 500 employees of a company, where *empNo* (indicating the employee number) is the key:

$$\underline{\text{empAge}}(\text{empNo}, \text{age})$$

Consider the following relational algebra expression:

$$\Pi_{\text{empNo}}(\text{empAge} \bowtie_{(\text{age} > \text{age1})} \rho_{\text{empNo1}, \text{age1}}(\text{empAge}))$$

What does the above expression generate?

- A. Employee numbers of only those employees whose age is the maximum
- B. Employee numbers of only those employees whose age is more than the age of exactly one other employee
- C. Employee numbers of all employees whose age is not the minimum
- D. Employee numbers of all employees whose age is the minimum

gate2021-cse-set1 databases relational-algebra

Answer 

3.12.26 Relational Algebra: GATE IT 2005 | Question: 68 top ↺

<https://gateoverflow.in/3831>



A table 'student' with schema (roll, name, hostel, marks), and another table 'hobby' with schema (roll, hobbyname) contains records as shown below:

Table: student

Roll	Name	Hostel	Marks
1798	Manoj Rathor	7	95
2154	Soumic Banerjee	5	68
2369	Gumma Reddy	7	86
2581	Pradeep pendse	6	92
2643	Suhas Kulkarni	5	78
2711	Nitin Kadam	8	72
2872	Kiran Vora	5	92
2926	Manoj Kunkalikar	5	94
2959	Hemant Karkhanis	7	88
3125	Rajesh Doshi	5	82

Table: hobby

Roll	Hobby Name
1798	chess
1798	music
2154	music
2369	swimming
2581	cricket
2643	chess
2643	hockey
2711	volleyball
2872	football
2926	cricket
2959	photography
3125	music
3125	chess

The following SQL query is executed on the above tables:

```
select hostel
from student natural join hobby
where marks >= 75 and roll between 2000 and 3000;
```

Relations S and H with the same schema as those of these two tables respectively contain the same information as tuples. A new relation S' is obtained by the following relational algebra operation:

$$\text{tests.gatecse.i } S' = \Pi_{\text{hostel}}((\sigma_{s.roll=H.roll}(\sigma_{\text{marks}>75 \text{ and } \text{roll}>2000 \text{ and } \text{roll}<3000}(S)) \times (H)))$$

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The difference between the number of rows output by the SQL statement and the number of tuples in S' is

- A. 6
- B. 4
- C. 2
- D. 0

gate2005-it databases sql relational-algebra normal

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[Answer](#)

Answers: Relational Algebra

3.12.1 Relational Algebra: GATE CSE 1992 | Question: 13b [top](#)

<https://gateoverflow.in/43581>



✓ OPTIMIZED ANSWER

$$\Pi_{\text{hotel}}((\sigma_{\text{customer}=\text{"Rama"}(\text{LIKES})}) \bowtie \text{SERVES})$$

35 votes

-- Shubham Pandey (5k points)

3.12.2 Relational Algebra: GATE CSE 1994 | Question: 13 [top](#)

<https://gateoverflow.in/2509>



- A. $\pi_{\text{rollno}}(\sigma_{\text{cno.} = 322}(\text{REGISTERED_FOR}))$
- B. SELECT year, min(age) FROM STUDENTS GROUP BY year

In the second question we have to find the year and youngest student from that year. So, we have to apply MIN aggregate function on each year (group by year).

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31 votes

-- SAKET NANDAN (4.2k points)

3.12.3 Relational Algebra: GATE CSE 1994 | Question: 3.8 [top](#)

<https://gateoverflow.in/2494>



✓ $R - (R - S)$

There is no need to use Union operator here.

Just because they say you can use operators from $(\cup, -)$ we don't need to use both of them.

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Also they are saying that **only the minimum number of operators from $(\cup, -)$** which is equivalent to $R \cap S$.

My expression is Minimal.

47 votes

-- Akash Kanase (36k points)

3.12.4 Relational Algebra: GATE CSE 1995 | Question: 27 [top](#)

<https://gateoverflow.in/2666>



- A. $\pi_{\text{pname}}(\text{publishers})$
- B. $\pi_{\text{authors.*}}(\sigma_{\text{book.pname}=\text{"TECHNICAL PUBLISHERS"}}(\text{book}) \bowtie \text{authors})$
- C. $\pi_{\text{book.aname}}(\sigma_{\text{publishers.pcit}=\text{"Madras"}}(\text{publishers}) \bowtie \text{book})$

24 votes

-- Sheshang M. Ajwalia (2.6k points)

3.12.5 Relational Algebra: GATE CSE 1996 | Question: 27<https://gateoverflow.in/2779>

- Select the (user# and) titles of the books issued to User# 6
- Select author names of the books issued to users whose home town is Delhi

41 votes

-- Arjun Suresh (332k points)

3.12.6 Relational Algebra: GATE CSE 1997 | Question: 76-a<https://gateoverflow.in/19838>

-
- $\pi_{eno}(\sigma_{EMP.eno=INVOLVED.eno \wedge INVOLVED.pno=3}(EMP \times INVOLVED))$

23 votes

-- Prashant Singh (47.2k points)

3.12.7 Relational Algebra: GATE CSE 1998 | Question: 1.33<https://gateoverflow.in/1670>

-
- This question is an example of **Theta Join**,

$$r \bowtie_\theta s = \sigma_\theta(r \times s)$$

The join here will be selecting only those tuples where $A = C$ and $B = D$, meaning it is the intersection. D option.

38 votes

-- Arjun Suresh (332k points)

3.12.8 Relational Algebra: GATE CSE 1998 | Question: 27<https://gateoverflow.in/1742>

-
- T_1 will have all the available course numbers

T_2 will have all the course numbers completed by student2310

T_3 will have the combination of all the courses and the courses completed by student2310

$PRE_REQ - T_3$ (set minus operation) will return us all the entries of PRE_REQ which are not there in T_3 ,

Suppose $\langle C_1, C_5 \rangle$ is a particular tuple of $(PRE_REQ - T_3)$,

Now what does it imply? \implies It implies that C_5 is one of the prerequisite course for C_1 which has not been completed by C_5 .

Proof: If student2310 would have completed C_5 then definitely $\langle C_1, C_5 \rangle$ should have been there in T_3 (remember T_3 is the combination of all the courses and the courses completed by student2310) and in that case $(PRE_REQ - T_3)$ can not have $\langle C_1, C_5 \rangle$ as a tuple.

So, for any such $\langle C_1, C_5 \rangle$ tuple, $(\langle C_1, \text{any course id} \rangle)$ of $PRE_REQ - T_3, C_1$ should not be printed as output (Since there is some prerequisite course for C_1 which student2310 has not completed).

Now, suppose we have not got any tuple as a result of $(PRE_REQ - T_3)$ where C_2 is there under cno attribute ($\langle C_2, \text{any course id} \rangle$), what does it imply? \implies It implies that student2310 has completed all the prerequisite courses C_2 .

Hence, in order to get the final result we need to project cno from $(PRE_REQ - T_3)$ and subtract it from T_1 .

- $T_1 \leftarrow \pi_{cno}(\text{COURSES})$
- $T_2 \leftarrow \rho_{T_1}(\text{std2310completedcourses})(\pi_{cno}(\sigma_{\text{student_no}=2310}(\text{COMPLETED})))$
- $T_3 \leftarrow T_1 \times T_2$
- $T_4 \leftarrow \rho_{T_4}(\text{cno, pre_cno})(PRE_REQ - T_3)$
- $\text{Result} \leftarrow T_1 - \pi_{cno}(T_4)$

21 votes

-- Sourav Basu (2.7k points)

3.12.9 Relational Algebra: GATE CSE 1999 | Question: 1.18, ISRO2016-53<https://gateoverflow.in/1471>

-
- Answer is **B**.

Case 1: if there is a common attribute between R and S , and every row of r matches with the each row of s - i.e., it means, the

join attribute has the same value in all the rows of both r and s ,
Case 2: If there is no common attribute between R and S .

0 There is a common attribute between R and S and nothing matches- the join attribute in r and s have no common value.

43 votes

-- Anurag Semwal (6.7k points)

3.12.10 Relational Algebra: GATE CSE 2000 | Question: 1.23, ISRO2016-57 top

→ <https://gateoverflow.in/647>



- ✓ Possible solutions, relational algebra:

(a) Join relation using attribute dpart_no.

- $\Pi_{\text{address}}(\text{emp} \bowtie \text{depart})$ OR
- $\Pi_{\text{address}}(\sigma_{\text{emp.dpart_no.}=\text{depart.depart_no.}}(\text{emp} \times \text{depart}))$

(b)

- $\Pi_{\text{name}}(\sigma_{\text{emp.depart_no.}=\text{depart.depart_no.} \wedge \text{emp.name}=\text{depart.depart_name}}(\text{emp} \times \text{depart}))$ OR
- $\Pi_{\text{name}}(\text{emp} \bowtie_{\text{emp.name}=\text{depart.depart_name}} \text{depart})$

(d) Let the given department number be x

- $\Pi_{\text{name}}(\sigma_{\text{emp.depart_no.}=\text{depart.depart_no.} \wedge \text{depart_no.}=x}(\text{emp} \times \text{depart}))$ OR
- $\Pi_{\text{name}}(\text{emp} \bowtie_{\text{depart_no.}=x} \text{depart})$

(c) We cannot generate relational algebra of aggregate functions using basic operations. We need extended operations here.

Option (c).

43 votes

-- Mithlesh Upadhyay (4.3k points)

3.12.11 Relational Algebra: GATE CSE 2001 | Question: 1.24 top

→ <https://gateoverflow.in/717>



- ✓ The answer is D.

- A. This is a simple select query.
- B. This is the simple query we need to check $X = Y$ in the where clause.
- C. Cycle < 3 . Means cycles of lengths 1 and 2. The cycle of length 1 is easy., the same as self-loop. The cycle of length 2 is also not too hard to compute. Though it'll be a bit more complex, will need to do like $(X, Y) \& (Y, X)$ both present and $X! = Y$. We can do this with a constant length (not depending on the number of tuples) RA query.
- D. This is the hardest part. Here we need to find closure of vertices. This will need a kind of loop. If the graph is like a skewed tree, our query must loop for $O(N)$ times. We can't do this with a constant length query here.

Answer: D.

51 votes

-- Akash Kanase (36k points)

3.12.12 Relational Algebra: GATE CSE 2001 | Question: 1.25 top

→ <https://gateoverflow.in/718>



- ✓ Answer is C.

C is just the better form of query, more execution friendly because requires less memory while joining. query, given in question takes more time and memory while joining.

34 votes

-- jayendra (6.7k points)

3.12.13 Relational Algebra: GATE CSE 2002 | Question: 15 top

→ <https://gateoverflow.in/868>



(I will write only useful attributes in relation which are required)

Ex: INTERVIEW

company name	student roll
A	1

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B	1
C	1
A	2
B	2
A	3

OFFER

company name	student roll
A	1
B	1
C	1
A	2

So the student with rolls 1,2,3 interviewed. Student 1 did sit for all companies, got the job in all companies A,B,C. Student 2 sat for A,B, got job in A only. Student 3 sat for A, did not get.

a) Part i) :

1
2
3

minus

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1
2

equals to

3

$\prod \text{scrollno} (\text{Interview}) - \prod \text{scrollno} (\text{Offer})$

You got the required student's roll numbers but to print their names, store that in **Temp** and join with Student table.
 $\prod \text{scrollno}, \text{sname} (\text{Temp} \bowtie \text{Student})$

a) Part ii) : Those who got interviewed (includes those who got jobs in all,some,none)
Now **interviewed - offer** = those who **did not** get jobs or got in **some**.

B	2
A	3

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Now again subtract whatever you got from all students of the interview again

1
2
3

minus

2
3

equals to

1

But note that it is not an intersection. You may think.... A-(A-B) so intersection.

But it is not... We are doing A-B on all tuples.

But the next subtraction is done on a particular attribute. (It became distinct since we focused on it only)

$\prod \text{scrollno} (\text{Interview}) - \prod \text{scrollno} (\text{Interview} - \text{Offer})$

You got the required student's roll numbers but to print their names, store that in **Temp** and join with Student table.

$\prod \text{scrollno}, \text{sname} (\text{Temp} \bowtie \text{Student})$

b) select s.sdegree, AVG(o.osalary) from Student s,Offer o where s.scrollno=o.scrollno having count(distinct s.scrollno)>5 group by

s.degree;

40 votes

-- Ahwan Mishra (10.2k points)

3.12.14 Relational Algebra: GATE CSE 2003 | Question: 30 top

<https://gateoverflow.in/920>



- ✓ select distinct in SQL is equivalent to project and by default relation 1, relation 2 in SQL corresponds to cross-product.
So, option A.

40 votes

-- Arjun Suresh (332k points)

3.12.15 Relational Algebra: GATE CSE 2004 | Question: 51 top

<https://gateoverflow.in/1047>



- ✓ OPTION : (D)

The given query states the following conditions:

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$$\begin{array}{l} \text{Sex} = F \wedge \\ x = M \wedge \\ \text{Marks} \leq m \end{array} \rightarrow (1)$$

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Let the relation be Student(Name, Sex, Marks)

	Name	Sex	Marks
	S1	F	30
	S2	F	10
	S3	M	20

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Student(Name, Sex, Marks) Relation is renamed as Student(n, x, m).

Taking the cross product of the relations

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No.	Name	Sex	Marks	n	x	m
1	S1	F	30	S1	F	30
2	S1	F	30	S2	F	10
3	S1	F	30	S3	M	20
4	S2	F	10	S1	F	30
5	S2	F	10	S2	F	10
6	S2	F	10	S3	M	20
7	S3	M	20	S1	F	30
8	S3	M	20	S2	M	10
9	S3	M	20	S3	M	30

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Selecting the tuple (row#6 from the above table), which satisfies the condition (1) and PROJECTING $\Pi_{name} \Rightarrow [S2]$

$$\Pi_{name}(\sigma_{sex=F}(\text{Student})) = \boxed{S1}$$
$$\quad \quad \quad \boxed{S2}$$

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Hence, the query:

$$\Pi_{name} [\sigma_{sex=F}(\text{student})] - \Pi_{name} \left[\begin{array}{l} \text{student} \Join \sigma_{x,x,m}(\text{student}) \\ sex = F \wedge \\ x = M \wedge \\ marks \leq m \end{array} \right]$$

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$$\boxed{S1} - \boxed{S2} = \boxed{S1}$$

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Let us take another relation data of Student(Name, Sex, Marks)

Name	Sex	Marks	
S1	M	100	> highest marks of M student
S2	F	50	> highest marks of F student
S3	M	40	
S4	F	30	

Taking the cross product

No.	Name	Sex	Marks	w.	n	x	m
1	S1	M	100	S1	M	100	
2	S1	M	100	S2	F	50	
3	S1	M	100	S3	M	40	
4	S1	M	100	S4	F	30	
5	S2	F	50	S1	M	100	
6	S2	F	50	S2	F	50	
7	S2	F	50	S3	F	40	
8	S2	F	50	S4	F	30	
9	S3	M	100	S1	M	100	
10	S3	M	100	S2	F	50	
11	S3	M	100	S3	M	40	
12	S3	M	100	S4	F	30	
13	S4	F	30	S1	M	100	
14	S4	F	30	S2	F	50	
15	S4	F	30	S3	M	40	
16	S4	F	30	S4	F	30	

Consider the row numbers 5, 13, 15 from the above table,

$\boxed{S2}$ $\boxed{S4} \implies$ Female students who scored less than equal to some Male students.

$$\Pi_{name}[\sigma_{sex=F}(\text{Student})] = \boxed{S2} - \boxed{S4}$$

Hence, the result of the query will be:

$$\boxed{S2} - \boxed{S2} = \{\}$$

From the above relational data of table Student(Name, Sex, Marks)

(D) is the correct option

- In short,
- $\{\geq \text{All boys}\} = |\text{universal}| - |< \text{some M}|$
 - $\{> \text{All boys}\} = |\text{universal}| - |\leq \text{some M}|$
 - $\{\geq \text{some boys}\} = |\text{universal}| - |< \text{all M}|$

126 votes

-- Akhil Nadh PC (16.5k points)

3.12.16 Relational Algebra: GATE CSE 2007 | Question: 59 [top](#)

<https://gateoverflow.in/2428>



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STUDENTINFO			ENROLL	
1	A	M	1	C1
2	A	F	2	C1
3	A	F	2	C2
			3	C2

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- $\pi_{courseId}(\sigma_{sex='female'}(studInfo)) \times \pi_{courseId}(\text{enroll})$

$$\begin{array}{ccc} & 2 & C1 \\ \implies & * & = \\ & 3 & C2 \end{array} \quad \begin{array}{ccc} & 2 & C1 \\ & 2 & C2 \\ & 3 & C1 \\ & 3 & C2 \end{array}$$

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- $(\pi_{studId}(\sigma_{sex='female'}(studInfo)) \times \pi_{courseId}(\text{enroll})) - \text{enroll}$

$$\implies 3 \ C1$$

- $\pi_{courseId}((\pi_{studId}(\sigma_{sex='female'}(studInfo)) \times \pi_{courseId}(\text{enroll})) - \text{enroll})$

$$\implies C1$$

$C1$ is a course id in which not all girl students enrolled.

i.e. a proper subset of girls' students appeared.

Hence (B) is the correct answer.

1 62 votes

-- Digvijay (44.9k points)

Ans is b,

First it does a cross join between female students id and all course ids, then subtract the entries which are already present in enroll table.

Remaining are the courseids which are NOT done by at least one female student

1 25 votes

-- Anurag Semwal (6.7k points)

3.12.17 Relational Algebra: GATE CSE 2008 | Question: 68 top

→ <https://gateoverflow.in/491>



✓ (d) i, iii, iv

iv) is the expansion for natural join represented with other operators.

Why ii is not equivalent? Consider the following instances of R and S

$R : \{(1, abc, p1, p2, p3), (2, xyz, p1, p2, p3)\}$

$S : \{(1, abc, q1, q2), (2, def, q1, q2)\}$

Now, consider the given queries:

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i. $R \bowtie S$ gives

$\{(1, abc, p1, p2, p3, q1, q2)\}$

Projecting P gives $\{(1)\}$

ii. $\pi_P(R) \bowtie \pi_P(S)$ gives

$\{(1, 2)\} \bowtie \{(1, 2)\}$

$= \{(1, 2)\}$

iii. $\Pi_P(\Pi_{P,Q}(R) \cap \Pi_{P,Q}(S))$ gives

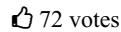
$$\{\langle "1", "abc" \rangle, \langle "2", "xyz" \rangle\} \cap \{\langle "1", "abc" \rangle, \langle "2", "def" \rangle\} = \{\langle "1", "abc" \rangle\}$$

Projecting P gives $\{\langle "1" \rangle\}$

iv. $\Pi_P(\Pi_{P,Q}(R) - (\Pi_{P,Q}(R) - \Pi_{P,Q}(S)))$ gives

$$\begin{aligned} & \{\langle "1", "abc" \rangle, \langle "2", "xyz" \rangle\} - (\{\langle "1", "abc" \rangle, \langle "2", "xyz" \rangle\} - \{\langle "1", "abc" \rangle, \langle "2", "def" \rangle\}) \\ &= \{\langle "1", "abc" \rangle, \langle "2", "xyz" \rangle\} - \{\langle "2", "xyz" \rangle\} = \{\langle "1", "abc" \rangle\} \end{aligned}$$

Projecting P gives $\{\langle "1" \rangle\}$



72 votes

-- Aravind (2.8k points)

3.12.18 Relational Algebra: GATE CSE 2012 | Question: 43 top

<https://gateoverflow.in/2151>



- ✓ Answer is A.

Referential integrity means, all the values in foreign key should be present in primary key.

$r2(c)$ is the super set of $r1(b)$

So, {subset - superset} is always empty set.



38 votes

-- Aravind (2.8k points)

3.12.19 Relational Algebra: GATE CSE 2014 Set 3 | Question: 21 top

<https://gateoverflow.in/2055>



- ✓ (A) $\pi_{A1}(\sigma_{F1 \wedge F2}(r))$

since A1 is subset of A2 will get only A1 attributes as it is in the outside, so we can remove project A2.

Two Selects with boolean expression can be combined into one select with And of two boolean expressions.



38 votes

-- Aravind (2.8k points)

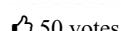
3.12.20 Relational Algebra: GATE CSE 2014 Set 3 | Question: 30 top

<https://gateoverflow.in/2064>



- ✓ (D) all of his/her dependents.

The inner query selects the employees whose age is less than or equal to at least one of his dependents. So, subtracting from the set of employees, gives employees whose age is greater than all of his dependents.



50 votes

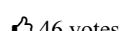
-- Arjun Suresh (332k points)

3.12.21 Relational Algebra: GATE CSE 2015 Set 1 | Question: 7 top

<https://gateoverflow.in/8094>



- ✓ Option D is correct because SELECT operation in SQL is equivalent to The projection operation in relational algebra, except that SELECT in SQL retains duplicates but projection gives only distinct.



46 votes

-- Anoop Sonkar (4.1k points)

3.12.22 Relational Algebra: GATE CSE 2017 Set 1 | Question: 46 top

<https://gateoverflow.in/118329>



- ✓ ANS) 4

T1 WILL GIVE :-	<table border="1"><tr><td>1. CA</td></tr><tr><td>2. CB</td></tr><tr><td>3. CC</td></tr></table>	1. CA	2. CB	3. CC
1. CA				
2. CB				
3. CC				

1. SA
2. SC
3. SD
4. SF

T2 = CR ÷ T1 = All the tuples in CR which are matched with every tuple in T1 :

//SB IS NOT MATCHED WITH CA, SE IS NOT MATCHED WITH CC
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144 votes

classroom.gateoverflow.in

-- jatin saini (4.2k points)

3.12.23 Relational Algebra: GATE CSE 2018 | Question: 41 [top](#)

<https://gateoverflow.in/204115>



- ✓ Option a, b, d will restrict all record with $B < 5$ but option C will include record with $b \geq 5$ also, so false.

C is answer.

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144 votes

-- Prashant Singh (47.2k points)

3.12.24 Relational Algebra: GATE CSE 2019 | Question: 55 [top](#)

<https://gateoverflow.in/302793>



- ✓ $R \cdot V = V_2$, there are two tuples which have Y parameter as Y_3 and Y_2 .

$P \cdot Y = R \cdot Y$, there are no coincide with Y_3 , and there is one tuple coincide with Y_2 which have X parameter as X_2 .

$$\Pi_X(\sigma_{(P.Y=R.Y \wedge R.V=V_2)}(P \times R)) = \{X_2\}$$

$Q \cdot T > 2$, there are two tuples which have Y parameter as Y_1 and Y_2 which have X parameter as X_1

(there is no need of checking R in this query part !)

$$\Pi_X(\sigma_{(Q.Y=R.Y \wedge Q.T>2)}(Q \times R)) = \{X_1\}$$

$$\Pi_X(\sigma_{(P.Y=R.Y \wedge R.V=V_2)}(P \times R)) - \Pi_X(\sigma_{(Q.Y=R.Y \wedge Q.T>2)}(Q \times R)) = \{X_2\} - \{X_1\} = \{X_2\}$$

Number of Tuples = 1

144 votes

-- Shaik Masthan (50.4k points)

3.12.25 Relational Algebra: GATE CSE 2021 Set 1 | Question: 27 [top](#)

<https://gateoverflow.in/357424>



- ✓ classroom.gateoverflow.in
Correct Answer: C

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Whenever a Database Problem intimidating like the above one(maybe it's just me) appears, it's often worth to Dissect the statements for Individual components and build up your arguments from there rather than attempting it head-on by some random example/argument only to get swayed by your hidden biases and choose the wrong answer.

Couple of Basic Ideas:

$\rho_{r1(x,y,...)}$ is the **rename operation** here, it's used to change the name of the $empAge$'s attributes $empNo, age$ to $empNo1, age1$ to resolve potential conflicts that can arise while referring the relations'(the table) attributes(column) when using relations that might share a common attribute name.

$\bowtie_{<cond>}$ is a combination of σ and \times where we take the Cross Product at First between the two relations and apply the tuple select condition supplied to \bowtie by using σ . So \bowtie equals $\sigma_{<cond>} (A \times B)$

$\Pi_{<attr>}$ is a Column Select Operation in naive words, it's supplied with attributes that needs to be selected.

A Relation contains only **unique tuples** unlike in conventional SQL Databases.

Now,

1. First the ρ operator renames the RHS relation to $empNo1, age1$.
2. We take the cross product of both the relations, each tuple in A (unmodified relation $empAge$) will be combined with every tuple in B (renamed relation $empAge$).
3. We filter the tuples according to the condition $age > age1$ which implies those tuples whose age values in A that are

greater than at least one of B are selected. Since A and B are the same here only those values which aren't the minimum are selected in A are selected($>$).

4.c We find out the set of unique $empNo$ by using Projection(Π)(Note: $empNo$ derived from LHS side of \bowtie the original $over$ relation A that we were talking about).

Since the $empNo$ is derived from relation A (LHS) whose age attribute is greater than the relation's minimum implies employees from A are selected whose age isn't the minimum hence, Option C is true.

Also, if $empNo1$ was chosen instead of $empNo$ then it would list all the employee numbers whose age isn't the maximum.

1 votes

-- Cringe is my middle name... (885 points)

3.12.26 Relational Algebra: GATE IT 2005 | Question: 68 [top](#)



✓ SQL query will return:

Roll	Hostel
2369	7
2581	6
2643	5
2643	5
	Duplicate Row is present in Hobby table
2872	5
2926	5
2959	7

Total 7 rows are selected.

In RA only distinct values of hostels are selected i.e. 5, 6, 7

SQL row count - RA row count = $7 - 3 = 4$

Answer is **B**.

66 votes

-- Vikrant Singh (11.2k points)

3.13

Relational Calculus (14) [top](#)

3.13.1 Relational Calculus: GATE CSE 1993 | Question: 23 [top](#)



The following relations are used to store data about students, courses, enrollment of students in courses and teachers of courses. Attributes for primary key in each relation are marked by '*'.

```
Students (rollno*, sname, saddr)
courses (cno*, cname)
enroll(rollno*, cno*, grade)
teach(tno*, tname, cao*)
```

(cno is course number cname is course name, tno is teacher number, tname is teacher name, sname is student name, etc.)

Write a SQL query for retrieving roll number and name of students who got A grade in at least one course taught by teacher names Ramesh for the above relational database.

gate1993 databases sql relational-calculus normal descriptive

Answer [♂](#)

3.13.2 Relational Calculus: GATE CSE 1993 | Question: 24 [top](#)



The following relations are used to store data about students, courses, enrollment of students in courses and teachers of courses. Attributes for primary key in each relation are marked by '*'.

- students(rollno*, sname, saddr)
- courses(cno*, cname)
- enroll(rollno*, cno*, grade)

- teach(tno*, tname, cao*)

(cno is course number, cname is course name, tno is teacher number, tname is teacher name, sname is student name, etc.)

For the relational database given above, the following functional dependencies hold:

- rollno → sname, saddr
- cno → cname
- tno → tname
- rollno, cno → grade

a. Is the database in 3rd normal form (3NF)?

b. If yes, prove that it is in 3NF. If not, normalize the relations so that they are in 3NF (without proving).

[gate1993](#) [databases](#) [sql](#) [relational-calculus](#) [normal](#) [descriptive](#)

Answer 

3.13.3 Relational Calculus: GATE CSE 1998 | Question: 2.19 [top](#)

Which of the following query transformations (i.e., replacing the l.h.s. expression by the r.h.s expression) is incorrect? R₁ and R₂ are relations, C₁ and C₂ are selection conditions and A₁ and A₂ are attributes of R₁.

- A. $\sigma_{C_1}(\sigma_{C_2}(R_1)) \rightarrow \sigma_{C_2}(\sigma_{C_1}(R_1))$
- B. $\sigma_{C_1}(\pi_{A_1}(R_1)) \rightarrow \pi_{A_1}(\sigma_{C_1}(R_1))$
- C. $\sigma_{C_1}(R_1 \cup R_2) \rightarrow \sigma_{C_1}(R_1) \cup \sigma_{C_1}(R_2)$
- D. $\pi_{A_1}(\sigma_{C_1}(R_1)) \rightarrow \sigma_{C_1}(\pi_{A_1}(R_1))$

[gate1998](#) [databases](#) [relational-calculus](#) [normal](#)

Answer 

3.13.4 Relational Calculus: GATE CSE 1999 | Question: 1.19 [top](#)

The relational algebra expression equivalent to the following tuple calculus expression:

{t | t ∈ r ∧ (t[A] = 10 ∧ t[B] = 20)} is

- A. $\sigma_{(A=10 \vee B=20)}(r)$
- B. $\sigma_{(A=10)}(r) \cup \sigma_{(B=20)}(r)$
- C. $\sigma_{(A=10)}(r) \cap \sigma_{(B=20)}(r)$
- D. $\sigma_{(A=10)}(r) - \sigma_{(B=20)}(r)$

[gate1999](#) [databases](#) [relational-calculus](#) [normal](#)

Answer 

3.13.5 Relational Calculus: GATE CSE 2001 | Question: 2.24 [top](#)

Which of the rational calculus expression is not safe?

- A. {t | ∃u ∈ R₁ (t[A] = u[A]) ∧ ¬∃s ∈ R₂ (t[A] = s[A])}
- B. {t | ∀u ∈ R₁ (u[A] = "x" ⇒ ∃s ∈ R₂ (t[A] = s[A] ∧ s[A] = u[A]))}
- C. {t | ¬(t ∈ R₁)}
- D. {t | ∃u ∈ R₁ (t[A] = u[A]) ∧ ∃s ∈ R₂ (t[A] = s[A])}

[gate2001-cse](#) [relational-calculus](#) [normal](#) [databases](#)

Answer 



With regards to the expressive power of the formal relational query languages, which of the following statements is true?

- A. Relational algebra is more powerful than relational calculus
- B. Relational algebra has the same power as relational calculus
- C. Relational algebra has the same power as safe relational calculus
- D. None of the above

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[goclasses.in](#)

[tests.gatecse.in](#)

[Answer](#)



Let $R_1 (\underline{A}, B, C)$ and $R_2 (\underline{D}, E)$ be two relation schema, where the primary keys are shown underlined, and let C be a foreign key in R_1 referring to R_2 . Suppose there is no violation of the above referential integrity constraint in the corresponding relation instances r_1 and r_2 . Which of the following relational algebra expressions would necessarily produce an empty relation?

- A. $\Pi_D(r_2) - \Pi_C(r_1)$
- B. $\Pi_C(r_1) - \Pi_D(r_2)$
- C. $\Pi_D(r_1 \bowtie_{C \neq D} r_2)$
- D. $\Pi_C(r_1 \bowtie_{C=D} r_2)$

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[Answer](#)



Consider the relation **employee**(name, sex, supervisorName) with *name* as the key, *supervisorName* gives the name of the supervisor of the employee under consideration. What does the following Tuple Relational Calculus query produce?

$$\{e. \text{name} \mid \text{employee}(e) \wedge (\forall x) [\neg \text{employee}(x) \vee x. \text{supervisorName} \neq e. \text{name} \vee x. \text{sex} = \text{"male"}]\}$$

- A. Names of employees with a male supervisor.
- B. Names of employees with no immediate male subordinates.
- C. Names of employees with no immediate female subordinates.
- D. Names of employees with a female supervisor.

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[Answer](#)



Which of the following tuple relational calculus expression(s) is/are equivalent to $\forall t \in r (P(t))$?

- I. $\neg \exists t \in r (P(t))$
- II. $\exists t \notin r (P(t))$
- III. $\neg \exists t \in r (\neg P(t))$
- IV. $\exists t \notin r (\neg P(t))$
 - A. I only
 - B. II only
 - C. III only
 - D. III and IV only

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[Answer](#)



Let R and S be relational schemes such that $R = \{a, b, c\}$ and $S = \{c\}$. Now consider the following queries on the database:

1. $\pi_{R-S}(r) - \pi_{R-S}(\pi_{R-S}(r) \times s - \pi_{R-S,S}(r))$
2. $\{t \mid t \in \pi_{R-S}(r) \wedge \forall u \in s (\exists v \in r (u = v[S] \wedge t = v[R - S]))\}$
3. $\{t \mid t \in \pi_{R-S}(r) \wedge \forall v \in r (\exists u \in s (u = v[S] \wedge t = v[R - S]))\}$

4. `Select R.a,R.b
From R,S
Where R.c = S.c`

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Which of the above queries are equivalent?

- A. 1 and 2
- B. 1 and 3
- C. 2 and 4
- D. 3 and 4

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[Answer](#)



Consider the following relational schema.

- Students(rollno: integer, sname: string)
- Courses(courseno: integer, cname: string)
- Registration(rollno: integer, courseno: integer, percent: real)

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Which of the following queries are equivalent to this query in English?

"Find the distinct names of all students who score more than 90% in the course numbered 107"

- I. `SELECT DISTINCT S.sname FROM Students as S, Registration as R WHERE R.rollno=S.rollno AND R.courseno=107 AND R.percent >90`
- II. $\prod_{sname}(\sigma_{courseno=107 \wedge percent>90}(Registration \bowtie Students)).in$
- III. $\{T \mid \exists S \in Students, \exists R \in Registration (S.rollno = R.rollno \wedge R.courseno = 107 \wedge R.percent > 90 \wedge T.sname = S.sname)\}$
- IV. $\{\langle S_N \rangle \mid \exists S_R \exists R_P (\langle S_R, S_N \rangle \in Students \wedge \langle S_R, 107, R_P \rangle \in Registration \wedge R_P > 90)\}$

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- A. I, II, III and IV
- B. I, II and III only
- C. I, II and IV only
- D. II, III and IV only

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[Answer](#)



Which of the following relational query languages have the same expressive power?

- I. Relational algebra
- II. Tuple relational calculus restricted to safe expressions
- III. Domain relational calculus restricted to safe expressions
- A. II and III only
- B. I and II only
- C. I and III only
- D. I, II and III

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gate2006-it databases relational-algebra relational-calculus easy

[Answer](#)

3.13.13 Relational Calculus: GATE IT 2007 | Question: 65 top

▪ <https://gateoverflow.in/3510>



Consider a selection of the form $\sigma_{A \leq 100}(r)$, where r is a relation with 1000 tuples. Assume that the attribute values for A among the tuples are uniformly distributed in the interval $[0, 500]$. Which one of the following options is the best estimate of the number of tuples returned by the given selection query ?

- A. 50 tests.gatecse.in
- B. 100 goclasses.in
- C. 150 tests.gatecse.in
- D. 200 tests.gatecse.in

[gate2007-it](https://gate2007-it.gateoverflow.in) [databases](#) [relational-calculus](#) [probability](#) [normal](#)

Answer

3.13.14 Relational Calculus: GATE IT 2008 | Question: 75 top

▪ <https://gateoverflow.in/3389>



Consider the following relational schema:

- Student(school-id, sch-roll-no, sname, saddress)
- School(school-id, sch-name, sch-address, sch-phone)
- Enrolment(school-id, sch-roll-no, erollno, examname)
- ExamResult(erollno, examname, marks)

Consider the following tuple relational calculus query.

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$\{t \mid \exists E \in \text{Enrolment} \quad t = E.\text{school-id} \wedge \{x \mid x \in \text{Enrolment} \wedge x.\text{school-id} = t \wedge (\exists B \in \text{ExamResult} \quad B.\text{erollno} = x.\text{erollno})$

If a student needs to score more than 35 marks to pass an exam, what does the query return?

- A. The empty set
- B. schools with more than 35% of its students enrolled in some exam or the other
- C. schools with a pass percentage above 35% over all exams taken together
- D. schools with a pass percentage above 35% over each exam

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[gate2008-it](https://gate2008-it.gateoverflow.in) [databases](#) [relational-calculus](#) [normal](#)

Answer

Answers: Relational Calculus

3.13.1 Relational Calculus: GATE CSE 1993 | Question: 23 top

▪ <https://gateoverflow.in/2320>



```
classroom.gateoverflow.in
select student.rollno, student.sname
From student natural join enroll on student.rollno=enroll.rollno
Where enroll.grade='A' AND enroll.cno in (select cno from teach where tname='Ramesh')
```

16 votes

-- Aravind (2.8k points)

3.13.2 Relational Calculus: GATE CSE 1993 | Question: 24 top

▪ <https://gateoverflow.in/203351>



✓ classroom.gateoverflow.in

gateoverflow.in

classroom.gateoverflow.in

- ✓ In table teach we have Primary Key (which is automatically a candidate key as well) as (tno, coa). We have the functional dependency tno \rightarrow tname which is a partial functional dependency (a proper subset of candidate key determining a non-key attribute) which violates 2NF requirement and hence 3NF too. So the relational database is not in 3NF.

To make it in 3NF we have to break teach table into (tno*, coa*) and (tno*, tname).

9 votes

-- Tarun kushwaha (1.7k points)

3.13.3 Relational Calculus: GATE CSE 1998 | Question: 2.19 top

▪ <https://gateoverflow.in/1692>



- ✓ D) if the selection condition is on attribute A_2 , then we cannot replace it by RHS as there will not be any attribute A_2 due to projection of A_1 only.

44 votes

-- Shaun Patel (6.1k points)

3.13.4 Relational Calculus: GATE CSE 1999 | Question: 1.19 top ↗

→ <https://gateoverflow.in/1472>



- ✓ Answer: (C)

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Tuple t should have two attributes A and B such that $t.A = 10$ and $t.B = 20$.

So, (Tuples having $A = 10$) \cap (Tuples having $B = 20$) = (Tuples having $A = 10$ and $B = 20$).

26 votes

-- Rajarshi Sarkar (27.9k points)

3.13.5 Relational Calculus: GATE CSE 2001 | Question: 2.24 top ↗

→ <https://gateoverflow.in/742>



- ✓ Answer: C.

It returns tuples not belonging to R1 (which is infinitely many). So, it is not safe.

Reference: http://nptel.ac.in/courses/IIT-MADRAS/Intro_to_Database_Systems_Design/pdf/3.1_Tuple_Relational_Calculus.pdf

References



gateoverflow.in

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37 votes

-- Rajarshi Sarkar (27.9k points)

3.13.6 Relational Calculus: GATE CSE 2002 | Question: 1.20 top ↗

→ <https://gateoverflow.in/825>



- ✓ Answer: C

Relational algebra has the same power as safe relational calculus as:

- A query can be formulated in safe Relational Calculus if and only if it can be formulated in Relational Algebra.

30 votes

-- Rajarshi Sarkar (27.9k points)

3.13.7 Relational Calculus: GATE CSE 2004 | Question: 13 top ↗

→ <https://gateoverflow.in/1010>



- ✓ Answer is (B).

C in $R1$ is a foreign key referring to the primary key D in $R2$. So, every element of C must come from some D element.

25 votes

-- Vicky Bajoria (4.1k points)

3.13.8 Relational Calculus: GATE CSE 2007 | Question: 60 top ↗

→ <https://gateoverflow.in/1258>



- ✓ OR (\vee) is commutative and associative, therefore i can rewrite given query as:

$\{e.name \mid employee(e) \wedge (\forall x) [\neg employee(x) \vee x.sex = "male" \vee x.supervisorName \neq e.name]\}$

$\{e.name \mid employee(e) \wedge (\forall x) [-(employee(x) \wedge x.sex \neq "male") \vee x.supervisorName \neq e.name]\}$

$\{e.name \mid employee(e) \wedge (\forall x) [(employee(x) \wedge x.sex \neq "male") \Rightarrow x.supervisorName \neq e.name]\}$

$\{e.name \mid employee(e) \wedge (\forall x) [(employee(x) \wedge x.sex = "female") \Rightarrow x.supervisorName \neq e.name]\}$

It is clear now they are saying something about female employees, This query does not say anything about male employees.

Therefore Option A and B are out of consideration.

This query retrieves those $e.name$ who satisfies this condition:

$$\forall x[(\text{employee}(x) \wedge x.sex = "female") \Rightarrow x.supervisorName \neq e.name]$$

Means retrieves those $e.name$, who is not a supervisor of any female employees.
i.e it retrieves name of employees with no female subordinate.
(here "immediate" is obvious, as we are checking first level supervisor.)

Hence, option C.

185 votes

-- Sachin Mittal (15.8k points)

3.13.9 Relational Calculus: GATE CSE 2008 | Question: 15 top

<https://gateoverflow.in/413>



✓ Only III is correct.

The given statement means for all tuples from r , P is true. III means there does not exist a tuple in r where P is not true. Both are equivalent.

IV is not correct as it is saying that there exist a tuple, not in r for which P is not true, which is not what the given expression means.

43 votes

-- Arjun Suresh (332k points)

3.13.10 Relational Calculus: GATE CSE 2009 | Question: 45 top

<https://gateoverflow.in/1331>



✓

$$\begin{aligned} 1. \quad & \pi_{R-S}(r) - \pi_{R-S}(\pi_{R-S}(r) \times s - \pi_{R-S,S}(r)) \\ &= \pi_{a,b}(r) - \pi_{a,b}(\pi_{a,b}(r) \times s - \pi_R(r)) \\ &\equiv (r/s) \end{aligned}$$

2. Expanding logically the statement means to select $t(a, b)$ from r such that for all tuples u in s , there is a tuple v in r , such that $u = v[S]$ and $t = v[R - S]$. This is just equivalent to (r/s)
3. Expanding logically the statement means that select $t(a, b)$ from r such that for all tuples v in r , there is a tuple u in s , such that $u = v[S]$ and $t = v[R - S]$. This is equivalent to saying to select (a, b) values from r , where the c value is in some tuple of s .
4. This selects (a, b) from all tuples from r which has an equivalent c value in s .

So, 1 and 2 are equivalent.

r		
a	b	c
Arj	TY	12
Arj	TY	14
Cell	TR	13
Tom	TW	12
Ben	TE	14

s	
c	
12	
14	

1. will give $\langle Arj, TY \rangle$.

2. will give $\langle Arj, TY \rangle$.

3. will not return any tuple as the c value 13, is not in s .

4. will give $\langle Arj, TY \rangle, \langle Arj, TY \rangle, \langle Tom, TW \rangle, \langle Ben, TE \rangle$.

<http://pages.cs.wisc.edu/~dbbook/openAccess/firstEdition/slides/pdfs/slides/mod311.pdf>

Correct Answer: A

References



61 votes

-- Arjun Suresh (332k points)

3.13.11 Relational Calculus: GATE CSE 2013 | Question: 35 top

<https://gateoverflow.in/1546>



- ✓ Answer: A

Four queries given in SQL, RA, TRC and DRC in four statements respectively retrieve the required information.

36 votes

-- Rajarshi Sarkar (27.9k points)

3.13.12 Relational Calculus: GATE IT 2006 | Question: 15 top

<https://gateoverflow.in/3554>



- ✓ Answer: D

All are equivalent in expressive power.

21 votes

-- Rajarshi Sarkar (27.9k points)

3.13.13 Relational Calculus: GATE IT 2007 | Question: 65 top

<https://gateoverflow.in/3510>



- ✓ $\sigma_{A \leq 100}(r)$
 r has 1000 tuples

Values for A among the tuples are uniformly distributed in the interval [0, 500]. This can be split to 5 mutually exclusive (non-overlapping) and exhaustive (no other intervals) intervals of same width of 100 ([0 – 100], [101 – 200], [201 – 300], [301 – 400], [401 – 500], 0 makes the first interval larger - this must be a typo in question) and we can assume all of them have same number of values due to Uniform distribution. So, number of tuples with A value in first interval should be

$$\frac{\text{Total no. of tuples}}{5} = 1000/5 = 200$$

Correct Answer: D

35 votes

-- Abhinav Rana (723 points)

3.13.14 Relational Calculus: GATE IT 2008 | Question: 75 top

<https://gateoverflow.in/3389>



- ✓ $t \mid \exists E \in \text{Enrolment } t = E.\text{school-id}$

Returns school-ids from Enrolment table SUCH THAT

- $\mid\{x \mid x \in \text{Enrolment} \wedge x.\text{school-id} = t \wedge (\exists B \in \text{ExamResult } B.\text{erollno} = x.\text{erollno} \wedge B.\text{examname} = x.\text{examname}) \wedge \dots)$
- the number of student enrolments from the school for exams with marks > 35 divides
 - $\mid\{x \mid x \in \text{Enrolment} \wedge x.\text{school-id} = t\}$
 - total number of student enrolments from the school
 - $*100 > 35$
 - percentage of student enrolments with mark > 35 is > 35

Since to pass an exam > 35 mark is needed, this means selecting the school-ids where the pass percentage of students across all the exams taken together is > 35.

Correct Answer: C.

11 votes

-- gatecse (63.3k points)

3.14

Safe Query (1) top

3.14.1 Safe Query: GATE CSE 2017 Set 1 | Question: 41 top

<https://gateoverflow.in/118324>



Consider a database that has the relation schemas EMP(EmpId, EmpName, DeptId), and DEPT(DeptName, DeptId). Note that the DeptId can be permitted to be NULL in the relation EMP. Consider the following queries on the database expressed in tuple relational calculus.

- I. $\{t \mid \exists u \in \text{EMP}(t[\text{EmpName}] = u[\text{EmpName}] \wedge \forall v \in \text{DEPT}(t[\text{DeptId}] \neq v[\text{DeptId}]))\}$
- II. $\{t \mid \exists u \in \text{EMP}(t[\text{EmpName}] = u[\text{EmpName}] \wedge \exists v \in \text{DEPT}(t[\text{DeptId}] \neq v[\text{DeptId}]))\}$

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III. $\{t \mid \exists u \in \text{EMP}(t[\text{EmpName}] = u[\text{EmpName}] \wedge \exists v \in \text{DEPT}(t[\text{DeptId}] = v[\text{DeptId}]))\}$

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Which of the above queries are safe?

- A. I and II only
- B. I and III only
- C. II and III only
- D. I, II and III

gate2017-cse-set1 databases relational-calculus safe-query normal

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Answer 

Answers: Safe Query

3.14.1 Safe Query: GATE CSE 2017 Set 1 | Question: 41 [top](#)

<https://gateoverflow.in/11834>



✓ Answer is (D)

before \wedge operation all three expressions are the same,

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i.e. return true if for each tuple t we have finite no of tuple u in employee table for which they have same employee_name.

(I) but in 2nd part, for each tuple v in department there may exist infinite no of tuple t for which they may not be equal.

i.e. true for finite no of tuples \wedge true for infinite no of tuples, over all true for finite tuple.

(ii) there may exist infinite no of tuple for which at least one tuple v belongs to department table for which they may not be equal.

i.e. true for finite no of tuples \wedge true for infinite no of tuples, over all true for finite tuple.

(iii) this one actually true for finite no of tuples, as there may exist only finite tuple which may be equal to at least one tuple v in department. bcz department table contain finite no of tuple all tuple t which are same may not be more than all tuple v in department table in case of equality operation.

i.e. true for finite \wedge true for finite tuple, over all true for finite tuple.

so all TRC query will return finite tuple which implies all are safe.

reference:<http://www.cs.sfu.ca/CourseCentral/354/zaiane/material/notes/Chapter3/node14.html>

<http://people.cs.pitt.edu/~chang/156/10calculus.html> gateoverflow.in

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http://www.cs.princeton.edu/courses/archive/fall13/cos597D/notes/relational_calc.pdf

References



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 47 votes

-- 2018 (5.5k points)

3.15

Sql (51) [top](#)

3.15.1 Sql: GATE CSE 1988 | Question: 12iii [top](#)

<https://gateoverflow.in/94625>



Describe the relational algebraic expression giving the relation returned by the following SQL query.

```
Select      SNAME
from       S
Where      SNOin
          (select    SNO
           from     SP
           where    PNOin
                   (select    PNO
                    from     P
                    Where   COLOUR='BLUE'))
```

gate1988 normal descriptive databases sql

Answer ↗

3.15.2 Sql: GATE CSE 1988 | Question: 12iv top ↗

↗ <https://gateoverflow.in/94626>



```
Select      SNAME
from       S
Where      SNOin
           (select      SNO
            from s.gatecse.in
            where      PNOin
           (select      PNO
            from      P
            Where      COLOUR='BLUE'))
```

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What relations are being used in the above SQL query? Given at least two attributes of each of these relations.

gate1988 normal descriptive databases sql

Answer ↗

3.15.3 Sql: GATE CSE 1990 | Question: 10-a top ↗

↗ <https://gateoverflow.in/85686>



Consider the following relational database:

- employees (eno, ename, address, basic-salary)
- projects (pno, pname, nos-of-staffs-allotted)
- working (pno, eno, pjob)

The queries regarding data in the above database are formulated below in SQL. Describe in ENGLISH sentences the two queries that have been posted:

i.

```
SELECT ename
FROM employees
WHERE eno IN
      (SELECT eno
       FROM working
       GROUP BY eno
       HAVING COUNT(*) =
              (SELECT COUNT(*)
               FROM projects))
```

ii.

```
SELECT pname
FROM projects
WHERE pno IN
      (SELECT pno
       FROM projects
       MINUS
       SELECT DISTINCT pno
       FROM working);
```

gate1990 descriptive databases sql

Answer ↗

3.15.4 Sql: GATE CSE 1991 | Question: 12,b top ↗

↗ <https://gateoverflow.in/42998>



Suppose a database consist of the following relations:

```
SUPPLIER (SCODE, SNAME, CITY).
PART (PCODE, PNAME, PDESC, CITY).
PROJECTS (PRCODE, PRNAME, PRCITY).
SPPR (SCODE, PCODE, PRCODE, QTY).
```

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Write algebraic solution to the following :

- Get SCODE values for suppliers who supply to both projects PR1 and PR2.
- Get PRCODE values for projects supplied by at least one supplier not in the same city.

sql gate1991 normal databases descriptive

Answer ↗



Suppose a database consist of the following relations:

```
SUPPLIER (SCODE, SNAME, CITY) .
PART (PCODE, PNAME, PDESC, CITY) .
PROJECTS (PRCODE, PRNAME, PRCITY) .
SPPR (SCODE, PCODE, PRCODE, QTY) .
```

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Write SQL programs corresponting to the following queries:

- Print PCODE values for parts supplied to any project in DEHLI by a supplier in DELHI.
- Print all triples <CITY, PCODE, CITY> such that a supplier in first city supplies the specified part to a project in the second city, but do not print the triples in which the two CITY values are same.

[gate1991](#) [databases](#) [sql](#) [normal](#) [descriptive](#)

Answer



Consider the following relational database schema:

- EMP (eno name, age)
- PROJ (pno name)
- INVOLVED (eno, pno)

EMP contains information about employees. PROJ about projects and involved about which employees involved in which projects. The underlined attributes are the primary keys for the respective relations.

State in English (in not more than 15 words)

What the following relational algebra expressions are designed to determine

- $\Pi_{eno}(\text{INVOLVED}) - \Pi_{eno}((\Pi_{eno}(\text{INVOLVED}) \times \Pi_{pno}(\text{PROJ})) - \text{INVOLVED})$
- $\Pi_{age}(\text{EMP}) - \Pi_{age}(\sigma_{E.\text{age} < E'.\text{age}}((\rho E(\text{EMP}) \times \text{EMP}))$

(Note: $\rho E(\text{EMP})$ conceptually makes a copy of EMP and names it E (ρ is called the rename operator))

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[gate1997](#) [databases](#) [sql](#) [descriptive](#) [normal](#)

Answer



Suppose we have a database consisting of the following three relations:

- FREQUENTS (student, parlor) giving the parlors each student visits.
- SERVES (parlor, ice-cream) indicating what kind of ice-creams each parlor serves.
- LIKES (student, ice-cream) indicating what ice-creams each student likes.

(Assume that each student likes at least one ice-cream and frequents at least one parlor)

Express the following in SQL:

Print the students that frequent at least one parlor that serves some ice-cream that they like.

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[gate1998](#) [databases](#) [sql](#) [descriptive](#)

Answer



Which of the following is/are correct?

- An SQL query automatically eliminates duplicates
- An SQL query will not work if there are no indexes on the relations
- SQL permits attribute names to be repeated in the same relation
- None of the above

gate1999 databases sql easy

Answer ↗

3.15.9 Sql: GATE CSE 1999 | Question: 22-a top ↵

↗ <https://gateoverflow.in/1521>



Consider the set of relations

- EMP (Employee-no, Dept-no, Employee-name, Salary)
- DEPT (Dept-no, Dept-name, Location)

Write an SQL query to:

- Find all employees names who work in departments located at 'Calcutta' and whose salary is greater than Rs.50,000.
- Calculate, for each department number, the number of employees with a salary greater than Rs. 1,00,000.

gate1999 databases sql easy descriptive

Answer ↗

3.15.10 Sql: GATE CSE 1999 | Question: 22-b top ↵

↗ <https://gateoverflow.in/203572>



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Consider the set of relations

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- EMP (Employee-no, Dept-no, Employee-name, Salary)
- DEPT (Dept-no, Dept-name, Location)

Write an SQL query to:

Calculate, for each department number, the number of employees with a salary greater than Rs. 1,00,000

gate1999 databases sql descriptive easy

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Answer ↗

3.15.11 Sql: GATE CSE 2000 | Question: 2.25 top ↵

↗ <https://gateoverflow.in/672>



Given relations r(w, x) and s(y, z) the result of

select distinct w, x
from r, s

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is guaranteed to be same as r, provided.

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- r has no duplicates and s is non-empty
- r and s have no duplicates
- s has no duplicates and r is non-empty
- r and s have the same number of tuples

gate2000-cse databases sql

Answer ↗

3.15.12 Sql: GATE CSE 2000 | Question: 2.26 top ↵

↗ <https://gateoverflow.in/673>



In SQL, relations can contain null values, and comparisons with null values are treated as unknown. Suppose all comparisons with a null value are treated as false. Which of the following pairs is not equivalent?

- $x = 5 \quad not(not(x = 5))$
- $x = 5 \quad x > 4 \text{ and } x < 6$, where x is an integer
- $x \neq 5 \quad not(x = 5)$
- none of the above

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gate2000-cse databases sql normal

Answer ↗

3.15.13 Sql: GATE CSE 2000 | Question: 22 [top ↵](#)

↗ <https://gateoverflow.in/693>



Consider a bank database with only one relation
transaction (transno, acctno, date, amount)
The amount attribute value is positive for deposits and negative for withdrawals.

- Define an SQL view TP containing the information
(acctno,T1.date,T2.amount)
for every pair of transaction T1,T2 and such that T1 and T2 are transaction on the same account and the date of T2 is \leq the date of T1.
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- Using only the above view TP, write a query to find for each account the minimum balance it ever reached (not including the 0 balance when the account is created). Assume there is at most one transaction per day on each account and each account has at least one transaction since it was created. To simplify your query, break it up into 2 steps by defining an intermediate view V.

gate2000-cse databases sql normal descriptive

Answer ↗

3.15.14 Sql: GATE CSE 2001 | Question: 2.25 [top ↵](#)

↗ <https://gateoverflow.in/743>



Consider a relation geq which represents "greater than or equal to", that is, $(x, y) \in \text{geq}$ only if $y \geq x$.

```
create table geq
(
    ib integer not null,
    ub integer not null,
    primary key ib,
    foreign key (ub) references geq on delete cascade
);
```

Which of the following is possible if tuple (x,y) is deleted?

- A. A tuple (z,w) with $z > y$ is deleted
- B. A tuple (z,w) with $z > x$ is deleted
- C. A tuple (z,w) with $w < x$ is deleted
- D. The deletion of (x,y) is prohibited

gate2001-cse databases sql normal

Answer ↗

3.15.15 Sql: GATE CSE 2001 | Question: 21-a [top ↵](#)

↗ <https://gateoverflow.in/762>



Consider a relation examinee (regno, name, score), where regno is the primary key to score is a real number.

Write a relational algebra using $(\Pi, \sigma, \rho, \times)$ to find the list of names which appear more than once in examinee.

gate2001-cse databases sql normal descriptive

Answer ↗

3.15.16 Sql: GATE CSE 2001 | Question: 21-b [top ↵](#)

↗ <https://gateoverflow.in/203574>



Consider a relation examinee (regno, name, score), where regno is the primary key to score is a real number.

Write an SQL query to list the *regno* of examinees who have a score greater than the average score.

gate2001-cse databases sql normal descriptive

Answer ↗

3.15.17 Sql: GATE CSE 2001 | Question: 21-c [top ↵](#)

↗ <https://gateoverflow.in/203573>



Consider a relation examinee (regno, name, score), where regno is the primary key to score is a real number.

Suppose the relation appears (regno, centr_code) specifies the center where an examinee appears. Write an SQL query to list the centr_code having an examinee of score greater than 80.

gate2001-cse databases sql normal descriptive

Answer ↗

3.15.18 Sql: GATE CSE 2003 | Question: 86 top ↗

https://gateoverflow.in/969



Consider the set of relations shown below and the SQL query that follows.

Students: (Roll_number, Name, Date_of_birth)

Courses: (Course_number, Course_name, Instructor)

Grades: (Roll_number, Course_number, Grade)

```
Select distinct Name
from Students, Courses, Grades
where Students.Roll_number=Grades.Roll_number
and Courses.Instructor = 'Korth'
and Courses.Course_number = Grades.Course_number
and Grades.Grade = 'A'
```

Which of the following sets is computed by the above query?

- A. Names of students who have got an A grade in all courses taught by Korth
- B. Names of students who have got an A grade in all courses
- C. Names of students who have got an A grade in at least one of the courses taught by Korth
- D. None of the above

gate2003-cse databases sql easy

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Answer ↗

3.15.19 Sql: GATE CSE 2004 | Question: 53 top ↗

https://gateoverflow.in/1049



The employee information in a company is stored in the relation

- Employee (name, sex, salary, deptName)

Consider the following SQL query

```
Select deptName
From Employee
Where sex = 'M'
Group by deptName
Having avg(salary) >
       (select avg (salary) from Employee)
```

It returns the names of the department in which

- A. the average salary is more than the average salary in the company
- B. the average salary of male employees is more than the average salary of all male employees in the company
- C. the average salary of male employees is more than the average salary of employees in same the department
- D. the average salary of male employees is more than the average salary in the company

gate2004-cse databases sql normal

Answer ↗

3.15.20 Sql: GATE CSE 2005 | Question: 77, ISRO2016-55 top ↗

https://gateoverflow.in/1400



The relation **book** (**title,price**) contains the titles and prices of different books. Assuming that no two books have the same price, what does the following SQL query list?

```
select title
from book as B
where (select count(*) from book as T
```

where T.price>B.price) < 5

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- A. Titles of the four most expensive books
- B. Title of the fifth most inexpensive book
- C. Title of the fifth most expensive book
- D. Titles of the five most expensive books

gate2005-cse databases sql easy isro2016

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Answer ↗

3.15.21 Sql: GATE CSE 2006 | Question: 67 top ↵

▪ <https://gateoverflow.in/1845>



Consider the relation account (customer, balance) where the customer is a primary key and there are no null values. We would like to rank customers according to decreasing balance. The customer with the largest balance gets rank 1. Ties are not broke but ranks are skipped: if exactly two customers have the largest balance they each get rank 1 and rank 2 is not assigned.

Query1: tests.gatecse.in

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```
select A.customer, count(B.customer)
from account A, account B
where A.balance <=B.balance
group by A.customer
```

Query2:

```
select A.customer, 1+count(B.customer)
from account A, account B
where A.balance < B.balance
group by A.customer
```

Consider these statements about Query1 and Query2.

1. Query1 will produce the same row set as Query2 for some but not all databases.
2. Both Query1 and Query 2 are a correct implementation of the specification
3. Query1 is a correct implementation of the specification but Query2 is not
4. Neither Query1 nor Query2 is a correct implementation of the specification
5. Assigning rank with a pure relational query takes less time than scanning in decreasing balance order assigning ranks using ODBC.

Which two of the above statements are correct?

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- A. 2 and 5
- B. 1 and 3
- C. 1 and 4
- D. 3 and 5

gate2006-cse databases sql normal

Answer ↗

3.15.22 Sql: GATE CSE 2006 | Question: 68 top ↵

▪ <https://gateoverflow.in/1846>



Consider the relation enrolled (student, course) in which (student, course) is the primary key, and the relation paid (student, amount) where student is the primary key. Assume no null values and no foreign keys or integrity constraints.

Given the following four queries:

Query1:

```
select student from enrolled where student in (select student from paid)
```

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Query2:

```
select student from paid where student in (select student from enrolled)
```

Query3:

```
select E.student from enrolled E, paid P where E.student = P.student
```

Query4:

```
select student from paid where exists
(select * from enrolled where enrolled.student = paid.student)
```

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Which one of the following statements is correct?

- A. All queries return identical row sets for any database
- B. Query2 and Query4 return identical row sets for all databases but there exist databases for which Query1 and Query2 return different row sets
- C. There exist databases for which Query3 returns strictly fewer rows than Query2
- D. There exist databases for which Query4 will encounter an integrity violation at runtime

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gate2006-cse databases sql normal

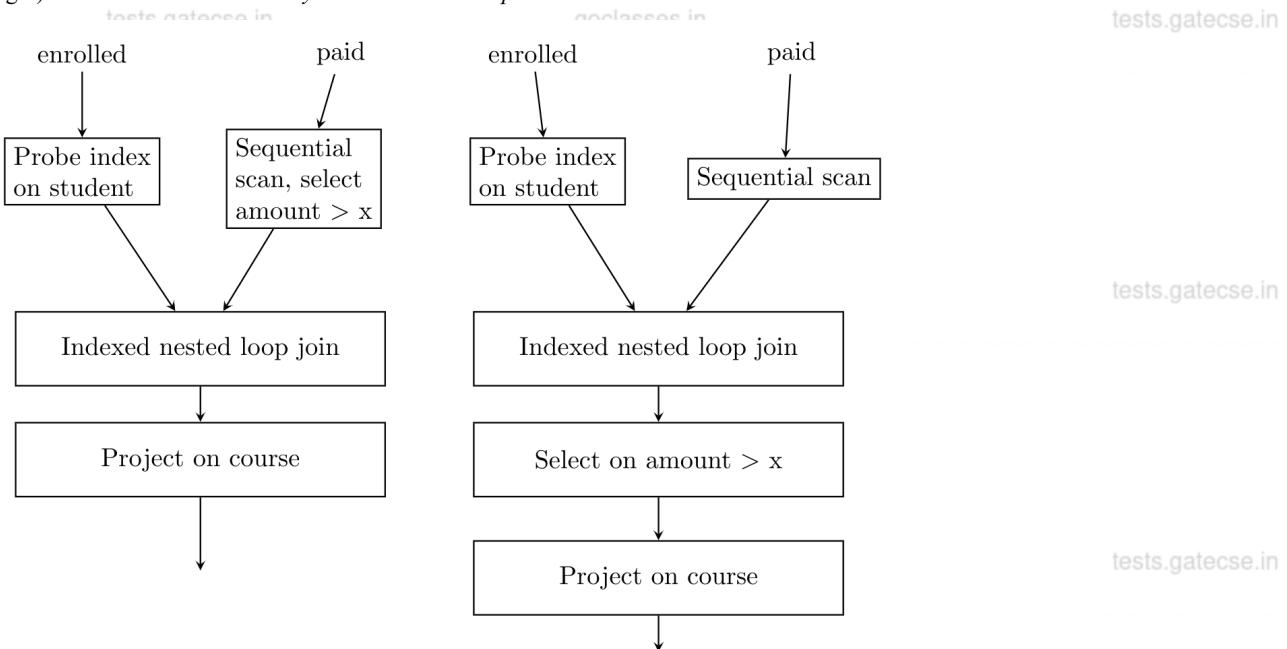
Answer ↗

3.15.23 Sql: GATE CSE 2006 | Question: 69 [top ↺](#)

→ <https://gateoverflow.in/1847>



Consider the relation enrolled (student, course) in which (student, course) is the primary key, and the relation paid (student, amount) where student is the primary key. Assume no null values and no foreign keys or integrity constraints. Assume that amounts 6000, 7000, 8000, 9000 and 10000 were each paid by 20% of the students. Consider these query plans (Plan 1 on left, Plan 2 on right) to “list all courses taken by students who have paid more than x ”



A disk seek takes 4ms, disk data transfer bandwidth is 300 MB/s and checking a tuple to see if amount is greater than x takes 10 μ s. Which of the following statements is correct?

- A. Plan 1 and Plan 2 will not output identical row sets for all databases
- B. A course may be listed more than once in the output of Plan 1 for some databases
- C. For $x = 5000$, Plan 1 executes faster than Plan 2 for all databases
- D. For $x = 9000$, Plan 1 executes slower than Plan 2 for all databases

gate2006-cse databases sql normal

Answer ↗

3.15.24 Sql: GATE CSE 2007 | Question: 61 [top ↺](#)

→ <https://gateoverflow.in/1259>



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Consider the table **employee**(empId, name, department, salary) and the two queries Q_1 , Q_2 below. Assuming that department 5 has more than one employee, and we want to find the employees who get higher salary than anyone in the department 5, which one of the statements is TRUE for any arbitrary employee table?

$Q_1:$

```

Select e.empId
From employee e
Where not exists
(Select * From employee s Where s.department = "5" and s.salary >= e.salary)

```

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Select e.empId
 From employee e
 Q_2 : Where e.salary > Any
 (Select distinct salary From employee s Where s.department = "5")

- A. Q_1 is the correct query
- B. Q_2 is the correct query
- C. Both Q_1 and Q_2 produce the same answer
- D. Neither Q_1 nor Q_2 is the correct query

gate2007-cse databases sql normal verbal-aptitude

Answer 

3.15.25 Sql: GATE CSE 2009 | Question: 55 top ↻

<https://gateoverflow.in/1339>



Consider the following relational schema:

Suppliers(sid:integer, sname:string, city:string, street:string)

Parts(pid:integer, pname:string, color:string)

Catalog(sid:integer, pid:integer, cost:real)

Consider the following relational query on the above database:

```
SELECT S.sname
FROM   Suppliers S
WHERE S.sid NOT IN (SELECT C.sid
                     FROM Catalog C
                     WHERE C.pid NOT IN (SELECT P.pid
                                         FROM Parts P
                                         WHERE P.color<>'blue'))
```

Assume that relations corresponding to the above schema are not empty. Which one of the following is the correct interpretation of the above query?

- A. Find the names of all suppliers who have supplied a non-blue part.
- B. Find the names of all suppliers who have not supplied a non-blue part.
- C. Find the names of all suppliers who have supplied only non-blue part.
- D. Find the names of all suppliers who have not supplied only blue parts.

gate2009-cse databases sql normal

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Answer 

3.15.26 Sql: GATE CSE 2010 | Question: 19 top ↻

<https://gateoverflow.in/2194>



A relational schema for a train reservation database is given below.

- passenger(pid, pname, age)
- reservation(pid, class, tid)

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Passenger		
pid	pname	Age
0	Sachine	65
1	Rahul	66
2	Sourav	67
3	Anil	69

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Reservation		
pid	class	tid
0	AC	8200
1	AC	8201
2	SC	8201
5	AC	8203
1	SC	8204
3	AC	8202

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What **pids** are returned by the following SQL query for the above instance of the tables?

```
SELECT pid
FROM Reservation
WHERE class='AC' AND
EXISTS (SELECT *
        FROM Passenger
        WHERE age>65 AND
        Passenger.pid=Reservation.pid)
```

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- A. 1, 0
- B. 1, 2
- C. 1, 3
- D. 1, 5

gate2010-cse databases sql normal

Answer 

3.15.27 Sql: GATE CSE 2011 | Question: 32 top ↗

<https://gateoverflow.in/2134>



Consider a database table T containing two columns X and Y each of type integer. After the creation of the table, one record ($X=1, Y=1$) is inserted in the table.

Let MX and MY denote the respective maximum values of X and Y among all records in the table at any point in time. Using MX and MY, new records are inserted in the table 128 times with X and Y values being $MX+1, 2*MY+1$ respectively. It may be noted that each time after the insertion, values of MX and MY change.

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What will be the output of the following SQL query after the steps mentioned above are carried out?

```
SELECT Y FROM T WHERE X=7;
```

- A. 127
- B. 255
- C. 129
- D. 257

gate2011-cse databases sql normal

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Answer 

3.15.28 Sql: GATE CSE 2011 | Question: 46 top ↗

<https://gateoverflow.in/2148>



Database table by name Loan_Records is given below.

Borrower	Bank_Manager	Loan_Amount
Ramesh	Sunderajan	10000.00
Suresh	Ramgopal	5000.00
Mahesh	Sunderajan	7000.00

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What is the output of the following SQL query?

```
SELECT count(*)
FROM (
    SELECT Borrower, Bank_Manager FROM Loan_Records) AS S
    NATURAL JOIN
    (SELECT Bank_Manager, Loan_Amount FROM Loan_Records) AS T
);
```

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- A. 3
- B. 9
- C. 5
- D. 6

gate2011-cse databases sql normal

Answer 

3.15.29 Sql: GATE CSE 2012 | Question: 15 top ↗

<https://gateoverflow.in/47>



Which of the following statements are **TRUE** about an SQL query?

P : An SQL query can contain a HAVING clause even if it does not have a GROUP BY clause

- Q : An SQL query can contain a HAVING clause only if it has a GROUP BY clause
 R : All attributes used in the GROUP BY clause must appear in the SELECT clause
 S : Not all attributes used in the GROUP BY clause need to appear in the SELECT clause

- A. P and R
 B. P and S
 C. Q and R
 D. Q and S

gate2012-cse databases easy sql ambiguous

Answer ↗

3.15.30 Sql: GATE CSE 2012 | Question: 51 top ↗

↗ <https://gateoverflow.in/43313>



Consider the following relations A, B and C :

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A		
Id	Name	Age
12	Arun	60
15	Shreya	24
99	Rohit	11

B		
Id	Name	Age
15	Shreya	24
25	Hari	40
98	Rohit	20
99	Rohit	11

C		
Id	Phone	Area
10	2200	02
99	2100	01

How many tuples does the result of the following SQL query contain?

```
SELECT A.Id
FROM A
WHERE A.Age > ALL (SELECT B.Age
                     FROM B
                     WHERE B.Name = 'Arun')
```

- A. 4
 B. 3
 C. 0
 D. 1

gate2012-cse databases sql normal

Answer ↗

3.15.31 Sql: GATE CSE 2014 Set 1 | Question: 22 top ↗

↗ <https://gateoverflow.in/1789>



Given the following statements:

- S1:** A foreign key declaration can always be replaced by an equivalent check assertion in SQL.
S2: Given the table $R(a, b, c)$ where a and b together form the primary key, the following is a valid table definition.

```
CREATE TABLE S (
  a INTEGER,
  d INTEGER,
  e INTEGER,
  PRIMARY KEY (d),
  FOREIGN KEY (a) REFERENCES R)
```

Which one of the following statements is CORRECT?

- A. S1 is TRUE and S2 is FALSE
 B. Both S1 and S2 are TRUE
 C. S1 is FALSE and S2 is TRUE
 D. Both S1 and S2 are FALSE

gate2014-cse-set1 databases normal sql

Answer ↗

3.15.32 Sql: GATE CSE 2014 Set 1 | Question: 54 top ↗

↗ <https://gateoverflow.in/1934>



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Given the following schema:

employees(emp-id, first-name, last-name, hire-date, dept-id, salary)

departments(dept-id, dept-name, manager-id, location-id)

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You want to display the last names and hire dates of all latest hires in their respective departments in the location ID 1700. You issue the following query:

```
SQL>SELECT last-name, hire-date
  FROM employees
 WHERE (dept-id, hire-date) IN
 (SELECT dept-id, MAX(hire-date)
  FROM employees JOIN departments USING(dept-id)
 WHERE location-id =1700
 GROUP BY dept-id);
```

What is the outcome?

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- A. It executes but does not give the correct result
- B. It executes and gives the correct result.
- C. It generates an error because of pairwise comparison.
- D. It generates an error because of the GROUP BY clause cannot be used with table joins in a sub-query.

gate2014-cse-set1 databases sql normal

Answer ↗

3.15.33 Sql: GATE CSE 2014 Set 2 | Question: 54 top

↗ <https://gateoverflow.in/2021>



SQL allows duplicate tuples in relations, and correspondingly defines the multiplicity of tuples in the result of joins. Which one of the following queries always gives the same answer as the nested query shown below:

```
select * from R where a in (select S.a from S)
```

- A. select R.* from R, S where R.a=S.a
- B. select distinct R.* from R,S where R.a=S.a
- C. select R.* from R,(select distinct a from S) as S1 where R.a=S1.a
- D. select R.* from R,S where R.a=S.a and is unique R

gate2014-cse-set2 databases sql normal

Answer ↗

3.15.34 Sql: GATE CSE 2014 Set 3 | Question: 54 top

↗ <https://gateoverflow.in/2089>



Consider the following relational schema:

employee (empId, empName, empDept)

customer (custId, custName, salesRepId, rating)

salesRepId is a foreign key referring to **empId** of the employee relation. Assume that each employee makes a sale to at least one customer. What does the following query return?

```
SELECT empName FROM employee E
WHERE NOT EXISTS (SELECT custId
                   FROM customer C
                   WHERE C.salesRepId = E.empId
                   AND C.rating <> 'GOOD');
```

- A. Names of all the employees with at least one of their customers having a 'GOOD' rating.
- B. Names of all the employees with at most one of their customers having a 'GOOD' rating.
- C. Names of all the employees with none of their customers having a 'GOOD' rating.
- D. Names of all the employees with all their customers having a 'GOOD' rating.

gate2014-cse-set3 databases sql easy

Answer ↗

3.15.35 Sql: GATE CSE 2015 Set 1 | Question: 27 top

↗ <https://gateoverflow.in/8225>



Consider the following relation:

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Student	
Roll_No	Student_Name
1	Raj
2	Rohit
3	Raj

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Performance		
Roll_No	Course	Marks
1	Math	80
1	English	70
2	Math	75
3	English	80
2	Physics	65
3	Math	80

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Consider the following SQL query.

```
SELECT S.Student_Name, Sum(P.Marks)
FROM Student S, Performance P
WHERE S.Roll_No= P.Roll_No
GROUP BY S.Student_Name
```

The numbers of rows that will be returned by the SQL query is _____.

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Answer

3.15.36 Sql: GATE CSE 2015 Set 3 | Question: 3

→ <https://gateoverflow.in/8396>



Consider the following relation

Cinema(*theater, address, capacity*)

Which of the following options will be needed at the end of the SQL query

```
SELECT P1.address
FROM Cinema P1
```

such that it always finds the addresses of theaters with maximum capacity?

- A. WHERE P1.capacity >= All (select P2.capacity from Cinema P2)
- B. WHERE P1.capacity >= Any (select P2.capacity from Cinema P2)
- C. WHERE P1.capacity > All (select max(P2.capacity) from Cinema P2)
- D. WHERE P1.capacity > Any (select max(P2.capacity) from Cinema P2)

gate2015-cse-set3 databases sql normal

Answer

3.15.37 Sql: GATE CSE 2016 Set 2 | Question: 52

→ <https://gateoverflow.in/39604>



Consider the following database table named water_schemes:

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Water_schemes		
scheme_no	district_name	capacity
1	Ajmer	20
1	Bikaner	10
2	Bikaner	10
3	Bikaner	20
1	Churu	10
2	Churu	20
1	Dungargarh	10

The number of tuples returned by the following SQL query is _____.

```
with total (name, capacity) as
  select district_name, sum (capacity)
    from water_schemes
   group by district_name
with total_avg(capacity) as
  select avg (capacity)
```

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```

from total
select name
from total, total_avg
where total.capacity >= total_avg.capacity

```

gate2016-cse-set2 databases sql normal numerical-answers

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Answer ↗

3.15.38 Sql: GATE CSE 2017 Set 1 | Question: 23 top ↗

↗ <https://gateoverflow.in/118303>



Consider a database that has the relation schema EMP (EmpId, EmpName, and DeptName). An instance of the schema EMP and a SQL query on it are given below:

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EMP		
EmpId	EmpName	DeptName
1	XYA	AA
2	XYB	AA
3	XYC	AA
4	XYD	AA
5	XYE	AB
6	XYF	AB
7	XYG	AB
8	XYH	AC
9	XYI	AC
10	XYJ	AC
11	XYK	AD
12	XYL	AD
13	XYM	AE

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```

SELECT AVG(EC.Num)
FROM EC
WHERE (DeptName, Num) IN
    (SELECT DeptName, COUNT(EmpId) AS
     EC(DeptName, Num)
    FROM EMP
    GROUP BY DeptName)

```

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tests.gatecse.in

The output of executing the SQL query is _____.

gate2017-cse-set1 databases sql numerical-answers

Answer ↗

3.15.39 Sql: GATE CSE 2017 Set 2 | Question: 46 top ↗

↗ <https://gateoverflow.in/118391>



Consider the following database table named top_scorer .

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top_scorer		
player	country	goals
Klose	Germany	16
Ronaldo	Brazil	15
G Muller	Germany	14
Fontaine	France	13
Pele	Brazil	12
Klinsmann	Germany	11
Kocsis	Hungary	11
Batistuta	Argentina	10
Cubillas	Peru	10
Lato	Poland	10
Lineker	England	10
T Muller	Germany	10
Rahn	Germany	10

Consider the following SQL query:

```
SELECT ta.player FROM top_scorer AS ta
WHERE ta.goals > ALL (SELECT tb.goals
                      FROM top_scorer AS tb
                      WHERE tb.country = 'Spain')
AND ta.goals > ANY (SELECT tc.goals
                      FROM top_scorer AS tc
                      WHERE tc.country='Germany')
```

The number of tuples returned by the above SQL query is _____

gate2017-cse-set2 databases sql numerical-answers

Answer ↗

3.15.40 Sql: GATE CSE 2018 | Question: 12 top ↗

↗ <https://gateoverflow.in/204086>



Consider the following two tables and four queries in SQL.

Book (isbn, bname), Stock(isbn, copies)

Query 1:

```
SELECT B.isbn, S.copies FROM Book B INNER JOIN Stock S ON B.isbn=S.isbn;
```

Query 2: [tests.gatecse.in](#)

[goclasses.in](#)

[tests.gatecse.in](#)

```
SELECT B.isbn, S.copies FROM Book B LEFT OUTER JOIN Stock S ON B.isbn=S.isbn;
```

Query 3:

```
SELECT B.isbn, S.copies FROM Book B RIGHT OUTER JOIN Stock S ON B.isbn=S.isbn
```

Query 4:

```
SELECT B.isbn, S.copies FROM Book B FULL OUTER JOIN Stock S ON B.isbn=S.isbn
```

Which one of the queries above is certain to have an output that is a superset of the outputs of the other three queries?

- A. Query 1
- B. Query 2
- C. Query 3
- D. Query 4

gate2018-cse databases sql easy

Answer ↗

3.15.41 Sql: GATE CSE 2019 | Question: 51 top ↗

↗ <https://gateoverflow.in/302797>



A relational database contains two tables Student and Performance as shown below:

Table: student

Roll_no	Student_name
1	Amit
2	Priya
3	Vinit
4	Rohan
5	Smita

Table: Performance

Roll_no	Subject_code	Marks
1	A	86
1	B	95
1	C	90
2	A	89
2	C	92
3	C	80

The primary key of the Student table is Roll_no. For the performance table, the columns Roll_no. and Subject_code together form the primary key. Consider the SQL query given below:

```
SELECT S.Student_name, sum(P.Marks)
FROM Student S, Performance P
WHERE P.Marks >84
GROUP BY S.Student_name;
```

The number of rows returned by the above SQL query is _____

gate2019-cse numerical-answers databases sql

Answer 

3.15.42 Sql: GATE CSE 2020 | Question: 13 top ↗

<https://gateoverflow.in/333218>



Consider a relational database containing the following schemas.

Catalogue

sno	pno	cost
S1	P1	150
S1	P2	50
S1	P3	100
S2	P4	200
S2	P5	250
S3	P1	250
S3	P2	150
S3	P5	300
S3	P4	250

Suppliers

sno	sname	location
S1	M/s Royal furniture	Delhi
S2	M/s Balaji furniture	Bangalore
S3	M/s Premium furniture	Chennai

Parts

pno	pname	part_spec
P1	Table	Wood
P2	Chair	Wood
P3	Table	Steel
P4	Almirah	Steel
P5	Almirah	Wood

The primary key of each table is indicated by underlining the constituent fields.

```
SELECT s.sno, s.sname
FROM Suppliers s, Catalogue c
WHERE s.sno=c.sno AND
      cost > (SELECT AVG (cost)
                FROM Catalogue
               WHERE pno = 'P4'
              GROUP BY pno) ;
```

The number of rows returned by the above SQL query is

- A. 4
- B. 5
- C. 0
- D. 2

gate2020-cse numerical-answers databases sql

Answer 

3.15.43 Sql: GATE CSE 2021 Set 1 | Question: 23 top ↗

<https://gateoverflow.in/357428>



A relation $r(A, B)$ in a relational database has 1200 tuples. The attribute A has integer values ranging from 6 to 20, and the attribute B has integer values ranging from 1 to 20. Assume that the attributes A and B are independently distributed.

The estimated number of tuples in the output of $\sigma_{(A>10) \vee (B=18)}(r)$ is _____.

gate2021-cse-set1 numerical-answers databases sql

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Answer ↗

3.15.44 Sql: GATE CSE 2021 Set 2 | Question: 31 top ↵

↗ <https://gateoverflow.in/357509>



The relation scheme given below is used to store information about the employees of a company, where `emplId` is the key and `deptId` indicates the department to which the employee is assigned. Each employee is assigned to exactly one department.

`emp(emplId, name, gender, salary, deptId)`

Consider the following SQL query:

```
select deptId, count(*)
from emp
where gender = "female" and salary > (select avg(salary) from emp)
group by deptId;
```

The above query gives, for each department in the company, the number of female employees whose salary is greater than the average salary of

- A. employees in the department
- B. employees in the company
- C. female employees in the department
- D. female employees in the company

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gate2021-cse-set2 databases sql easy

Answer ↗

3.15.45 Sql: GATE IT 2004 | Question: 74 top ↵

↗ <https://gateoverflow.in/3718>



A relational database contains two tables `student` and `department` in which `student` table has columns `roll_no`, `name` and `dept_id` and `department` table has columns `dept_id` and `dept_name`. The following insert statements were executed successfully to populate the empty tables:

```
Insert into department values (1, 'Mathematics')
Insert into department values (2, 'Physics')
Insert into student values (1, 'Navin', 1)
Insert into student values (2, 'Mukesh', 2)
Insert into student values (3, 'Gita', 1)
```

How many rows and columns will be retrieved by the following SQL statement?

```
Select * from student, department
```

- A. 0 row and 4 columns
- B. 3 rows and 4 columns
- C. 3 rows and 5 columns
- D. 6 rows and 5 columns

gate2004-it databases sql normal

Answer ↗

3.15.46 Sql: GATE IT 2004 | Question: 76 top ↵

↗ <https://gateoverflow.in/3720>



A table `T1` in a relational database has the following rows and columns:

Roll no.	Marks
1	10
2	20
3	30
4	NULL

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The following sequence of SQL statements was successfully executed on table `T1`.

```
Update T1 set marks = marks + 5
Select avg(marks) from T1
```

What is the output of the select statement?

- A. 18.75
 B. 20
 C. 25
 D. Null

gate2004-it databases sql normal

goclasses.in

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Answer ↗

3.15.47 Sql: GATE IT 2004 | Question: 78 top ↵

► <https://gateoverflow.in/3722>



Consider two tables in a relational database with columns and rows as follows:

Table: Student

Roll_no	Name	Dept_id
1	ABC	1
2	DEF	1
3	GHI	2
4	JKL	3

Table: Department

Dept_id	Dept_name
1	A
2	B
3	C

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Roll_no is the primary key of the Student table, Dept_id is the primary key of the Department table and Student.Dept_id is a foreign key from Department.Dept_id

What will happen if we try to execute the following two SQL statements?

- i. update Student set Dept_id = Null where Roll_on = 1
- ii. update Department set Dept_id = Null where Dept_id = 1

- A. Both i and ii will fail
- B. i will fail but ii will succeed
- C. i will succeed but ii will fail
- D. Both i and ii will succeed

gate2004-it databases sql normal

Answer ↗

3.15.48 Sql: GATE IT 2005 | Question: 69 top ↵

► <https://gateoverflow.in/3832>



In an inventory management system implemented at a trading corporation, there are several tables designed to hold all the information. Amongst these, the following two tables hold information on which items are supplied by which suppliers, and which warehouse keeps which items along with the stock-level of these items.

Supply = (supplierid, itemcode)
 Inventory = (itemcode, warehouse, stocklevel)

For a specific information required by the management, following SQL query has been written

```
Select distinct STMP.supplierid
From Supply as STMP
Where not unique (Select ITMP.supplierid
From Inventory, Supply as ITMP
Where STMP.supplierid = ITMP.supplierid
And ITMP.itemcode = Inventory.itemcode
And Inventory.warehouse = 'Nagpur');
```

For the warehouse at Nagpur, this query will find all suppliers who

- A. do not supply any item
- B. supply exactly one item
- C. supply one or more items
- D. supply two or more items

gate2005-it databases sql normal

Answer ↗

3.15.49 Sql: GATE IT 2006 | Question: 84 top ↵

► <https://gateoverflow.in/3640>



Consider a database with three relation instances shown below. The primary keys for the Drivers and Cars relation are did and

cid respectively and the records are stored in ascending order of these primary keys as given in the tables. No indexing is available in the database.

D: Drivers relation

did	dname	rating	age
22	Karthikeyan	7	25
29	Salman	1	33
31	Boris	8	55
32	Amoldt	8	25
58	Schumacher	10	35
64	Sachin	7	35
71	Senna	10	16
74	Sachin	9	35
85	Rahul	3	25
95	Ralph	3	53

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R: Reserves relation

did	Cid	day
22	101	10 / 10 / 06
22	102	10 / 10 / 06
22	103	08 / 10 / 06
22	104	07 / 10 / 06
31	102	10 / 11 / 16
31	103	06 / 11 / 16
31	104	12 / 11 / 16
64	101	05 / 09 / 06
64	102	08 / 09 / 06
74	103	08 / 09 / 06

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C: Cars relation

Cid	Cname	colour
101	Renault	blue
102	Renault	red
103	Ferrari	green
104	Jaguar	red

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What is the output of the following SQL query?

```
select D.dname
from Drivers D
where D.did in (
    select R.did
    from Cars C, Reserves R
    where R.cid = C.cid and C.colour = 'red'
    intersect
    select R.did
    from Cars C, Reserves R
    where R.cid = C.cid and C.colour = 'green'
)
```

- A. Karthikeyan, Boris
- B. Sachin, Salman
- C. Karthikeyan, Boris, Sachin
- D. Schumacher, Senna

gate2006-it databases sql normal

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Answer ↗

3.15.50 Sql: GATE IT 2006 | Question: 85 top ↗

↗ <https://gateoverflow.in/3641>



Consider a database with three relation instances shown below. The primary keys for the Drivers and Cars relation are *did* and *cid* respectively and the records are stored in ascending order of these primary keys as given in the tables. No indexing is available in the database.

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D: Drivers relation				R: Reserves relation		
did	dname	rating	age	did	Cid	day
22	Karthikeyan	7	25	22	101	10 – 10 – 06
29	Salman	1	33	22	102	10 – 10 – 06
31	Boris	8	55	22	103	08 – 10 – 06
32	Amoldt	8	25	22	104	07 – 10 – 06
58	Schumacher	10	35	31	102	10 – 11 – 16
64	Sachin	7	35	31	103	06 – 11 – 16
71	Senna	10	16	31	104	12 – 11 – 16
74	Sachin	9	35	64	101	05 – 09 – 06
85	Rahul	3	25	64	102	08 – 09 – 06
95	Ralph	3	53	74	103	08 – 09 – 06

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C: Cars relation

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Cid	Cname	colour
101	Renault	blue
102	Renault	red
103	Ferrari	green
104	Jaguar	red

```

select D.dname
from Drivers D
where D.did in
      select R.did
      from Cars C, Reserves R
      where R.cid = C.cid and C.colour = 'red'
      intersect
      select R.did
      from Cars C, Reserves R
      where R.cid = C.cid and C.colour = 'green'
    )
  
```

Let n be the number of comparisons performed when the above SQL query is optimally executed. If linear search is used to locate a tuple in a relation using primary key, then n lies in the range:

- A. 36 – 40
- B. 44 – 48
- C. 60 – 64
- D. 100 – 104

gate2006-it databases sql normal

Answer ↗

3.15.51 Sql: GATE IT 2008 | Question: 74 top ↗

↗ <https://gateoverflow.in/3388>



Consider the following relational schema:

- Student(school-id, sch-roll-no, sname, saddress)
- School(school-id, sch-name, sch-address, sch-phone)
- Enrolment(school-id, sch-roll-no, erollno, examname)
- ExamResult(erollno, examname, marks)

What does the following SQL query output?

```

SELECT sch-name, COUNT (*)
FROM School C, Enrolment E, ExamResult R
WHERE E.school-id = C.school-id
  
```

```

AND
E.examname = R.examname AND E.erollno = R.erollno
AND
R.marks = 100 AND S.school-id IN (SELECT school-id
                                    FROM student
                                    GROUP BY school-id
                                    HAVING COUNT (*) > 200)
GROUP BY school-id

```

- A. for each school with more than 200 students appearing in exams, the name of the school and the number of 100s scored by its students
- B. for each school with more than 200 students in it, the name of the school and the number of 100s scored by its students
- C. for each school with more than 200 students in it, the name of the school and the number of its students scoring 100 in at least one exam
- D. nothing; the query has a syntax error

gate2008-it databases sql normal

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tests.gatecse.in

Answer ↗

Answers: Sql

3.15.1 Sql: GATE CSE 1988 | Question: 12iii top ↗

→ <https://gateoverflow.in/94625>



`select PNO from P Where COLOUR='BLUE';`

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This can be written as: $\pi_{pno}(\sigma_{colour='Blue'}(P))$

Store this in T1.

$\therefore T1 \leftarrow \pi_{pno}(\sigma_{colour='Blue'}(P))$

Then

```

select SNO from SP
where PNO in (select PNO from P
               Where COLOUR='BLUE')

```

$T2 \leftarrow \pi_{sno}(\sigma_{pno=T1}(SP))$

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Similary

```

Select SNAME from S
Where SNO in (select SNO from SP
               where PNO in (select PNO from P
                             Where COLOUR='BLUE'))

```

$Result \leftarrow \pi_{sname}(\sigma_{sno=T2}(S))$

👍 4 votes

-- Sourabh Gupta (4k points)

3.15.2 Sql: GATE CSE 1988 | Question: 12iv top ↗

→ <https://gateoverflow.in/94626>



✓ There are 3 relations here:

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- S(SNAME, SNO)
- SP(SNO, PNO)
- P(PNO, COLOUR)

👍 9 votes

-- Akash Dinkar (27.9k points)

3.15.3 Sql: GATE CSE 1990 | Question: 10-a top ↗

→ <https://gateoverflow.in/85686>



```

1.SELECT ename
FROM employees
WHERE eno IN
      (SELECT eno
       FROM working
       GROUP BY eno
       HAVING COUNT (*) =
              (SELECT COUNT (*)
               FROM projects));

```

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This will return : Employee name who is working for all projects.

(ii)
SELECT pname
FROM projects
WHERE pno IN
(SELECT pno
FROM projects
MINUS
SELECT DISTINCT pno
FROM working);

This will return : Project name for which no employee is working.

33 votes

-- Prashant Singh (47.2k points)

3.15.4 Sql: GATE CSE 1991 | Question: 12,b [top](#)

<https://gateoverflow.in/42998>



SCODE values for suppliers who supply to both projects PR1 and PR2 -

$\Pi_{scode,prcode}(SPPR) \div \Pi_{prcode}(\sigma_{prname=pr1 \vee prname=pr2}(PROJECTS))$

PRCODE values for projects supplied by at least one supplier not in the same city -

$\Pi_{prcode}(\sigma_{city <> prcity}((SUPPLIER * SPPR) * PROJECTS))$

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* is natural join.

8 votes

-- Ashish verma (7.2k points)

3.15.5 Sql: GATE CSE 1991 | Question: 12-a [top](#)

<https://gateoverflow.in/539>



- i. Print PCODE values for parts supplied to any project in DELHI by a supplier in DELHI

Select SP.PCODE
From SPPR SP, Projects PR, Supplier SU
Where SP.PRcode = PR.PRcode
and SU.Scode = SP.Scode
and PR.PRcity = "DELHI"
and SU.city = "DELHI";

- ii. Print all triples <CITY, PCODE, CITY>

Select SU.city, SP.Pcode, PR.PRcity
from Supplier SU, Projects PR, SPPR SP
Where SU.Scode = SP.Scode
And PR.PRcode = SP.PRcode
And SU.city <> PR.PRcity;

22 votes

-- Manu Thakur (34k points)

3.15.6 Sql: GATE CSE 1997 | Question: 76-b [top](#)

<https://gateoverflow.in/203570>



- i. $\Pi_{eno}(INVOLVED) - \Pi_{eno}((\Pi_{eno}(INVOLVED) \times \Pi_{pno}(PROJ) - INVOLVED))$

classroom.gateoverflow.in $\rightarrow (A)$

$\circ \Pi_{eno}(INVOLVED) - \text{All employees involved in projects} \rightarrow (A)$

$\circ \Pi_{eno}((\Pi_{eno}(INVOLVED) \times \Pi_{pno}(PROJ) - INVOLVED)) - \text{gives all employee who are not involved in at least one project.} \rightarrow (B)$

$\circ A - B = \text{employee No. of employees involved on the all project. (Division Operator)}$

- ii. $\Pi_{age}(EMP) - \Pi_{age}(\sigma_{Eage < EMP.age} (\rho E(EMP) \times EMP))$

classroom.gateoverflow.in $\rightarrow (C)$

$\circ \Pi_{age}(EMP) - \text{Age of all employees} \rightarrow (C)$

$\circ \Pi_{age}(\sigma_{Eage < EMP.age} (\rho E(EMP) \times EMP)) - \text{Employees who have age less than at least one other employee}$

$\rightarrow (D)$

$\circ C - D = \text{Maximum of all ages of employees.}$

14 votes

-- Prashant Singh (47.2k points)



```
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SELECT DISTINCT A.student FROM
FREQUENTS A, SERVES B, LIKES C
WHERE
    A.parlor=B.parlor
    AND
    B.ice-cream=C.ice-cream
    AND
    A.student=C.student;
```

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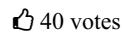
classroom.gateover

OR

```
classroom.gateoverflow.in
SELECT DISTINCT A.student FROM FREQUENTS A
WHERE
    parlor IN
        (SELECT parlor FROM SERVES B
        WHERE B.ice-cream IN
            (SELECT ice-cream
            FROM LIKES C
            WHERE C.student = A.student));
```

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40 votes

-- Arjun Suresh (332k points)

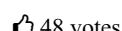


(D)

SQL wont remove duplicates like relational algebra projection, we have to remove it explicitly by distinct.

If there are no indexes on the relation SQL will either chose one/more on its own or simply work without any index. No index would just slow the query but it will surely work.

SQL does not permit 2 attributes to have same name in a relation.



48 votes

-- Aravind (2.8k points)



(a)

```
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select Employee-name
from EMP, DEPT
where Salary>50000 and EMP.Dept-no=DEPT.Dept-no and Location="Calcutta"
```

gateoverflow.in

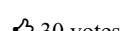
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(b)

```
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select Dept-no, count(*)
from EMP where salary > 100000
group by Dept-no
```

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30 votes

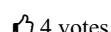
-- Aravind (2.8k points)



```
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SELECT Dept-no, count(Employee-no) as total_employees
FROM EMP
WHERE Salary > 100000
GROUP BY Dept-no
```

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4 votes

-- balraj_allam (95 points)



This question is about SQL, in SQL Relations are **MULTISET**, not SET. So, R or S can have duplicated.

Answer: A.

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A. If R has duplicates, in that case, due to distinct keyword those duplicates will be eliminated in final result. So, R can not have duplicates. If S is empty $R \times S$ becomes empty, so S must be non empty. This is true.

B. Here, assume that S is empty. (No duplicates.) Then R X S will be empty. SO this is false.

C. Same argument as B.

D. Assume that R has duplicates. Then Distinct keyword will remove duplicates. So, result of query $\{R\} = R$, so This is false.

73 votes

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-- Akash Kanase (36k points)

3.15.12 Sql: GATE CSE 2000 | Question: 2.26 [top](#)

<https://gateoverflow.in/673>



✓ classroom.gateoverflow.in
Answer is option C.

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Value at hand	Option A	Option B	Option C
6	✗ ✗	✗ ✗	✓ ✓
5	✓ ✓	✓ ✓	✗ ✗
NULL	✗ ✗	✗ ✗	✗ ✓

68 votes

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-- Amar Vashishth (25.2k points)

3.15.13 Sql: GATE CSE 2000 | Question: 22 [top](#)

<https://gateoverflow.in/693>



a.

```
Create view TP(T1.acctno, T1.date, T2.amount)
as (Select T1.acctno, T1.date, T2.amount
    from Transaction T1, Transaction T2
    where T1.acctno=T2.acctno
    and T2.date <= T1.date);
```

b.

i.

```
Create view V(acctno, date, balance)
as (select acctno, date, sum(amount)
    from TP
    group by acctno, date);
```

ii.

```
select acctno, min(balance)
from V
group by acctno;
```

7 votes

-- Sourabh Gupta (4k points)

3.15.14 Sql: GATE CSE 2001 | Question: 2.25 [top](#)

<https://gateoverflow.in/743>



✓ classroom.gateoverflow.in
Answer: C

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The table can be depicted as:

ib(PK)	ub(FK)
z	w = u
u	v = x
x	y

If (x, y) is deleted then from the above table:

- $v \leq y$ (as $v = x$)
- $u < v \leq y, u! = v$ (as $v = x$ and ib is the Primary Key)
- $w < v \leq y$ (as $w = u$)
- $z < w < v \leq y, z! = w$ (as $w = u$ and ib is the Primary Key)

As, it can be seen that $w < v$ or $w < x$ (as $v = x$) so C is the answer.

34 votes

-- Rajarshi Sarkar (27.9k points)

3.15.15 Sql: GATE CSE 2001 | Question: 21-a [top](#)

<https://gateoverflow.in/762>



- ✓ $\pi_{\text{exm1.name}}(\sigma_{(\text{exm1.regno} \neq \text{examinee.regno}) \wedge (\text{emp1.name} = \text{emp2.name})})(\rho_{\text{exm1}}(\text{examinee}) \times \text{examinee})$

16 votes

-- Tauhin Gangwar (6.7k points)

3.15.16 Sql: GATE CSE 2001 | Question: 21-b [top](#)

<https://gateoverflow.in/203574>



- ✓ There are many ways to write a query, all of which will perform the same task. One way is:

```
SELECT regno
FROM examinee
WHERE score > (SELECT AVG(score)
                 FROM examinee )
```

Here, the inner query is returning the average of the scores. And outer query selects those *regno* that have a score greater than this average.

11 votes

-- Rishabh Gupta (12.5k points)

3.15.17 Sql: GATE CSE 2001 | Question: 21-c [top](#)

<https://gateoverflow.in/203573>



```
SELECT DISTINCT centr_code
FROM appears
WHERE regno IN (SELECT regno
                  FROM examinee
                  WHERE score > 80)
```

11 votes

-- Arjun Suresh (332k points)

3.15.18 Sql: GATE CSE 2003 | Question: 86 [top](#)

<https://gateoverflow.in/969>



- ✓ C. Names of the students who have got an A grade in at least one of the courses taught by Korth.

31 votes

-- Arjun Suresh (332k points)

3.15.19 Sql: GATE CSE 2004 | Question: 53 [top](#)

<https://gateoverflow.in/1049>



- ✓ D is the answer.

The inner query is over all department and over both male and female employees while the outer query is only for male employees.

28 votes

-- Arjun Suresh (332k points)

3.15.20 Sql: GATE CSE 2005 | Question: 77, ISRO2016-55 [top](#)

<https://gateoverflow.in/1400>



- ✓ Answer: D

The outer query selects all titles from book table. For every selected book, the subquery returns count of those books which are more expensive than the selected book. The where clause of outer query will be true for 5 most expensive book. For example count(*) will be 0 for the most expensive book and count(*) will be 1 for second most expensive book.

78 votes

-- Rajarshi Sarkar (27.9k points)

3.15.21 Sql: GATE CSE 2006 | Question: 67 [top](#)

<https://gateoverflow.in/1845>



- ✓ Both Query1 and Query2 are not correct implementations because: Assume that we have a table with n customers having the same balance. In that case Query1 will give rank n to each customer. But according to the question the rank assigned should be 1. And Query2 will return an empty result set (as it will never return rank 1). So statement 4 is correct. For the same reason Query1 is wrong though it is true if we assume the relation set is empty. Statements 2 and 3 are false as 4 is TRUE. Statement 5 is false as a single scan should be faster than a join query. So, the best option should be C, though 1 is not technically correct.

A correct query to achieve the task would be:

```
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select A.customer, (
    select l+count(*)
    from account B
    where A.balance < B.balance
) from account A
```

-- Rajarshi Sarkar (27.9k points)

72 votes

3.15.22 Sql: GATE CSE 2006 | Question: 68 top

► <https://gateoverflow.in/1846>



- ✓ Query1 and Query3 : output will be the same
and Query2 and Query4 : output will be same

I have run these queries on the online compiler, this what i get

```
BEGIN TRANSACTION;
-- /* Create a table called NAMES */
-- CREATE TABLE E(Id integer);
-- CREATE TABLE P(Id integer);
-- 
-- /* Create few records in this table */
-- INSERT INTO E VALUES(1);
-- INSERT INTO E VALUES(1);
-- INSERT INTO E VALUES(3);
-- INSERT INTO E VALUES(3);
-- 
-- INSERT INTO P VALUES(1);
-- INSERT INTO P VALUES(2);
-- INSERT INTO P VALUES(3);
-- INSERT INTO P VALUES(4);
-- 
-- COMMIT;

/* Display all the records from the table */
-- SELECT * FROM E;
-- select "----";
-- SELECT * FROM P;
-- select "----";
select "Query 1:";
select E.id from E
where E.id in (select P.id from P);

select "Query 2:";
select id from P
where id in (select id from E);

select "Query 3:";

select E.id from E e, P p
where e.id = p.id;

select "Query 4:";
select id from P
where exists (select * from E where E.id = P.id);

/* output */
Query 1:
1
1
3
3
Query 2:
1
3
Query 3:
1
1
3
3
Query 4:
1
3
```

So, answer should be B.

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-- Vikrant Singh (11.2k points)

40 votes

3.15.23 Sql: GATE CSE 2006 | Question: 69 top

► <https://gateoverflow.in/1847>



Answer should be (C)

In all cases plan 1 is faster than plan 2 cause in plan 1 we are reducing the load by doing select amount > x and then the loop

But, in case of plan 2 its in the nested loop so it need to check every time and will take more time to execute .

27 votes

-- Pranay Datta (7.8k points)



✓ Answer: A

Create a table like this:

```
create table employee(empId int(50), name varchar(50), department int(50), salary int(50));
insert into employee values (1, 'a', 4, 90);
insert into employee values (2, 'b', 5, 30);
insert into employee values (3, 'c', 5, 50);
insert into employee values (4, 'd', 5, 80);
insert into employee values (8, 'f', 7, 10);
```

Q₁ returns 1 for the above table. See here: <http://sqlfiddle.com/#!9/9acce/1>

Q₂ returns empId of those employees who get salary more than the minimum salary offered in department 5. It returns 1,3,4 for the above table. See here: <http://sqlfiddle.com/#!9/9acce/2>

According the question the answer should be 1 for the above table.

PS: The question implies that the required employee must not be from department 5.

References



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👍 40 votes

-- Rajarshi Sarkar (27.9k points)



✓

```
SELECT P.pid FROM Parts P WHERE P.color<>'blue'
```

Select all non blue parts

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```
SELECT C.sid FROM Catalog C WHERE C.pid NOT IN
```

Selects all suppliers who have supplied a blue part

```
SELECT S.sname
FROM Suppliers S
WHERE S.sid NOT IN
```

Selects suppliers who have not supplied any blue parts.

So, **none** of the options matches.

Option C is wrong as it does not select suppliers who have not supplied any parts which the given query does.

Option A is wrong because it even selects those suppliers who have supplied blue and non-blue parts and also does not include those suppliers who have not supplied any parts.

👍 78 votes

-- Arjun Suresh (332k points)



✓ (C) 1, 3

The inner query gives passenger_id with age above 65 i.e., 1, 2, 3
The outer query chooses the class as AC, which are 1 and 3

👍 32 votes

-- Aravind (2.8k points)



✓ $X = 1, Y = 1$

$X = 2, Y = 2 \times 1 + 1 = 3$

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$X = 3, Y = 2 \times 3 + 1 = 7$

$X = 4, Y = 2 \times 7 + 1 = 15$

$X = 5, Y = 2 \times 15 + 1 = 31$

$X = 6, Y = 2 \times 31 + 1 = 63$

$X = 7, Y = 2 \times 63 + 1 = 127$

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Correct Answer: A

41 votes

-- Arjun Suresh (332k points)



3.15.28 Sql: GATE CSE 2011 | Question: 46 [top](#)

<https://gateoverflow.in/2148>

✓ The answer is (C).

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When we perform the natural join on S and T then result will be like this

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Borrower	Bank_Manager	Loan_Amount
Ramesh	Sunderajan	10000.00
Ramesh	Sunderajan	7000.00
Suresh	Ramgopala	5000.00
Mahesh	Sunderajan	10000.00
Mahesh	Sunderajan	7000.00

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After that count (*) will count total tuples present in this table so here it is 5.

41 votes

-- neha pawar (3.3k points)



3.15.29 Sql: GATE CSE 2012 | Question: 15 [top](#)

<https://gateoverflow.in/47>

✓ GATE 2012 Answer key is (C) Q and R are true.

But correct answer should be B.

- When group by is not present, having is applied to the whole table

"A grouped table is a set of groups derived during the evaluation of a <group by clause> or a <having clause>. A group is a multiset of rows in which all values of the grouping column or columns are equal if a <group by clause> is specified, or the group is the entire table if no <group by clause> is specified. A grouped table may be considered as a collection of tables. Set functions may operate on the individual tables within the grouped table."

This shows that P is indeed correct.

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Also see "having clause section"

<http://www.contrib.andrew.cmu.edu/~shadow/sql/sql1992.txt>

<http://searchsqlserver.techtarget.com/answer/ISO-ANSI-SQL-and-the-GROUP-BY-clause>

The above link says that all columns used in group by must be present in select clause as per SQL-92 standard but later standards doesn't enforce it. I tried this on MySQL and it works. It is allowed in MSSQL also- see below link.

From Microsoft (obviously applicable only to MS-SQL)

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<http://msdn.microsoft.com/en-us/library/ms177673.aspx>



Expressions in the GROUP BY clause can contain columns of the tables, derived tables or views in the FROM clause. The columns are not required to appear in the SELECT clause <select> list. Each table or view column in any nonaggregate expression in the <select> list must be included in the GROUP BY list:

So, as per standard it is not allowed, but in most current DBMS it is allowed. And there is no reason why this shouldn't be allowed. So, ideally 'S' is more correct than 'R' or both are debatable and marks should have been given to all.

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1 like 56 votes

-- Arjun Suresh (332k points)

3.15.30 Sql: GATE CSE 2012 | Question: 51 [top](#)

<https://gateoverflow.in/43313>



- ✓ <cond> ALL evaluates to TRUE if inner query returns no tuples. So, Number of tuples returned will be number of tuples in A = 3.

Reference: <http://dcx.sap.com/1200/en/dbusage/all-test-quantified-subquery.html>

Correct Answer: *B*

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References



1 like 48 votes

-- Arjun Suresh (332k points)

3.15.31 Sql: GATE CSE 2014 Set 1 | Question: 22 [top](#)

<https://gateoverflow.in/1789>



- ✓ (D)Both are false

S1: Foreign key constraint means a lot of constraints it has to be a primary key(which intrun has few constraints)

Alternate reason: Using a check condition we can have the same effect as Foreign key while adding elements to the child table. But when we delete an element from the parent table the referential integrity constraint is no longer valid. So, a check constraint cannot replace a foreign key.

So, we cannot replace it with a single check.

S2: if a and b forms a primary key in R, a alone cannot form a foreign key. i.e. R(a,b,c) and S(a,d,e) a of S references to a of R but a of R is not candidate key but a prime attribute since a,b combine a key.

Foreign key definition: it should be a candidate key in some other table(in our case it is only a prime attribute).

1 like 92 votes

-- Aravind (2.8k points)

3.15.32 Sql: GATE CSE 2014 Set 1 | Question: 54 [top](#)

<https://gateoverflow.in/1934>



```
SELECT dept-id, MAX(hire-date)
FROM employees JOIN departments USING(dept-id)
WHERE location-id =1700
GROUP BY dept-id
```

This inner query will give the max hire date of each department whose location_id =1700

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and outer query will give the last name and hire-date of all those employees who joined on max hire date.
answer should come to (B) no errors.

And we can use group by and where together, who said we can not :(

Example: create table departments(dept_id number, dept_name varchar2(25), location_id number);
Query: select d1.dept_name,max(d1.location_id)

from departments d1, departments d2
where d1.dept_name = d2.dept_name
and d1.dept_name='AA'
group by d1.dept_name;
will give output.

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40 votes

-- Manu Thakur (34k points)

3.15.33 Sql: GATE CSE 2014 Set 2 | Question: 54 top



✓ C)

Consider the following instances of R and S

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R		
A	B	C
1	2	3
1	2	3
7	8	9
7	8	9

S		
A	X	Z
1	2	3
3	5	7
7	6	5
7	6	5

Now output of given query

```
select * from R where a in (select S.a from S)
```

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R		
A	B	C
1	2	3
1	2	3
7	8	9
7	8	9

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For Option,

A) since multiplicity of tuples is disturbed

```
select R.* from R, S where R.a=S.a
```

∴ Output will be

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R		
A	B	C
1	2	3
1	2	3
7	8	9
7	8	9
7	8	9
7	8	9

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B)

```
select distinct R.* from R,S where R.a=S.a
```

∴ only Distinct R will be chosen in the end so, output will be

R		
A	B	C
1	2	3

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C) ANSWER

```
select R.* from R,(select distinct a from S) as S1 where R.a=S1.a
```

Multiplicity of tuples is maintained. ∴ Multiplicity of duplicate tuples will be distributed when there is a match between $R.a$ and $S.a$ and for that match $S.a$'s value is repeated.

So, Output will be

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A	B	C
1	2	3
1	2	3
7	8	9
7	8	9

76 votes

-- Kalpish Singhal (1.6k points)

3.15.34 Sql: GATE CSE 2014 Set 3 | Question: 54 top<https://gateoverflow.in/2089>

SELECT empNAME
 FROM employee E
 WHERE NOT EXISTS
 if any customer is there
 who gave bad rating then
 do not choose this EMPLOYEE
 if something exist in this then

For an employee
 (SELECT custId
 FROM CUSTOMER C
 WHERE C.saleRepId = E.empId
 AND C.rating <> 'GOOD')
 all customer who did not give good rating

So, an employee whose *ALL* customers gives him GOOD rating is chosen;

All such employees are chosen.

Answer = option D

50 votes

-- Amar Vashishth (25.2k points)

3.15.35 Sql: GATE CSE 2015 Set 1 | Question: 27 top<https://gateoverflow.in/8225>

For answering there is no need to execute the query, we can directly answer this as 2
 How?

Group by Student_Names

It means all name that are same should be kept in one row.

There are 3 names. But in that there is a duplicate with Raj being repeated \implies Raj produces one row and Rohit produces one row \implies Total 2 rows.

For better understanding, I'll just analyze the whole query

1st statement which is executed from the query is From Clause : **From Student S, Performance P**

\implies cross product of those two tables will be

S.RollNo	S.Student_name	P.Roll_no	P.Course	P.marks
1	Raj	1	Maths	80
1	Raj	1	English	70
1	Raj	2	Maths	75
1	Raj	3	English	80
1	Raj	2	Physics	65
1	Raj	3	Maths	80
2	Rohit	1	Maths	80
2	Rohit	1	English	70
2	Rohit	2	Maths	75
2	Rohit	3	English	80
2	Rohit	2	Physics	65
2	Rohit	3	Maths	80
3	Raj	1	Maths	80
3	Raj	1	English	70
3	Raj	2	Maths	75
3	Raj	1	English	80
3	Raj	2	Physics	65
3	Raj	3	Maths	80

2nd statement which is executed from the query is Where Clause : **Where S.Roll_no = P.Roll_no**

⇒ delete those rows which does not satisfy the WHERE condition. Then the result will be

S.RollNo	S.Student_name	P.Roll_no	P.Course	P.marks
1	Raj	1	Maths	80
1	Raj	1	English	70
2	Rohit	2	Maths	75
2	Rohit	2	Physics	65
3	Raj	3	English	80
1	Raj	3	Maths	80

3rd statement which is executed from the query is Group by Clause : **Group by S.Student_Name**

⇒ Merge those rows which are having same name, then result will be

S.RollNo	S.Student_name	P.Roll_no	P.Course	P.marks
{1, 1, 3, 3}	Raj	{1, 1, 3, 3}	{Maths, English}	{80, 70, 80, 80}
2	Rohit	2	{Maths, Physics}	{75, 65}

Note that, this can't be used as final result as it violates 1NF (multiple values in each tuple for S.Roll_no, P.Roll_no, P.Course and P.marks)

4th statement which is executed from the query is Select Clause : **Select S.Student_Name, SUM(P.marks)**

⇒ Delete un-necessary columns and calculate the aggregate functions, then result will be

S.Student_name	P.marks
Raj	310
Rohit	140

70 votes

-- naresh1845 (1.1k points)

3.15.36 Sql: GATE CSE 2015 Set 3 | Question: 3 [top](#)

→ <https://gateoverflow.in/8396>



✓ A is the answer

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B - Returns the addresses of all theaters.

C - Returns null set. max() returns a single value and there won't be any value > max.

D - Returns null set. Same reason as C. All and ANY works the same here as max returns a single value.

63 votes

-- Arjun Suresh (332k points)

3.15.37 Sql: GATE CSE 2016 Set 2 | Question: 52 top

<https://gateoverflow.in/39604>



- ✓ 1st query will return the following:

Table Name : Total (**name, capacity**)

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name	capacity
Ajmer	20
Bikaner	40
Churu	30
Dungargarh	10

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2nd Query will return, **Total_avg (capacity)** [25]

Since sum of capacity = $100/4 = 25$

3rd query will be final and it's tuples will be considered as output, where name of district and its total capacity should be more than or equal to 25

name
Bikaner
Churu

Hence, **2 tuples** returned.

75 votes

-- Shashank Chavan (2.4k points)



3.15.38 Sql: GATE CSE 2017 Set 1 | Question: 23 top

<https://gateoverflow.in/118303>

- ✓ The inner query will return

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DeptName	Num
AA	4
AB	3
AC	3
AD	2
AE	1

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Now AVG(EC.Num) will find the average of Num values in the above-returned query, which is $(4 + 3 + 3 + 2 + 1) \div 5 = 2.6$

So according to me, the answer should be 2.6.

43 votes

-- sriv_shubham (2.8k points)



3.15.39 Sql: GATE CSE 2017 Set 2 | Question: 46 top

<https://gateoverflow.in/118391>

- ✓ ALL (EMPTY SET) always returns TRUE. So first where condition is always satisfied.

Second where condition will return all those rows who have more goals than ANY German player. Since, minimum goals by a German is 10, all the rows which are greater than 10 Goals will be returned.

I.e. first 7 rows in the table.

Hence, answer: 7.

48 votes

-- tvkkk (1.1k points)

3.15.40 Sql: GATE CSE 2018 | Question: 12 [top](#)

<https://gateoverflow.in/204086>



- ✓ Answer is D.

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Since the full-outer join is nothing but a combination of inner-join and the remaining tuples of both the tables that couldn't satisfy the common attributes' equality condition, and merging them with "null" values.

20 votes

-- Baljit kaur (1k points)

3.15.41 Sql: GATE CSE 2019 | Question: 51 [top](#)

<https://gateoverflow.in/302797>



- ✓ Group by Student_name \Rightarrow number of distinct values of Student_name

in the instance of the relation all rows have distinct name then it should results 5 tuples !

27 votes

-- Shaik Masthan (50.4k points)

3.15.42 Sql: GATE CSE 2020 | Question: 13 [top](#)

<https://gateoverflow.in/333218>



- ✓ The given query is a nested subquery but not co-related subquery (inner query is independent of the outer and so can be executed independently)

```
SELECT AVG (cost) FROM Catalogue WHERE pno= 'P4' GROUP BY pno
```

sno	pno	cost
S1	P1	150
S1	P2	50
S1	P3	100
S2	P4	200
S2	P5	250
S3	P1	250
S3	P2	150
S3	P5	300
S3	P4	250

First, we will select the tuples with pno = 'P4' and then group by pno (so just one group) and then find the average cost.

sno	pno	cost
S2	P4	200
S3	P4	250

So average cost = $\frac{200+250}{2} = 225$

\therefore the inner query will return 225

Now the given SQL query would become

```
SELECT s.sno,s.sname FROM Supplier s , Catalogue c WHERE s.sno=c.sno AND cost> 225
```

So here we need to do cross product of supplier table *s* and Catalogue table *c* and from the cross product we will select those rows where *s.sno* = *c.sno* AND cost > 225

Since it is given that cost > 225 so we do not need to consider rows from the Catalogue table having cost ≤ 225 while doing cross product. Hence from the Catalogue table only the row numbers 5, 6, 8, 9 need to be taken while doing the cross product.

After doing cross product we'll get,

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s.sno	s.name	s.location	c.sno	c.pno	c.cost
S1	M/s Royal furniture	Delhi	S2	P5	250
S1	M/s Royal furniture	Delhi	S3	P1	250
S1	M/s Royal furniture	Delhi	S3	P5	300
S1	M/s Royal furniture	Delhi	S3	P4	250
S2	M/s Balaji furniture	Bangalore	S2	P5	250
S2	M/s Balaji furniture	Bangalore	S3	P1	250
S2	M/s Balaji furniture	Bangalore	S3	P5	300
S2	M/s Balaji furniture	Bangalore	S3	P4	250
S3	M/s Premium furniture	Chennai	S2	P5	250
S3	M/s Premium furniture	Chennai	S3	P1	250
S3	M/s Premium furniture	Chennai	S3	P5	300
S3	M/s Premium furniture	Chennai	S3	P4	250

Now after doing cross product only 4 tuples will be selected from the table due to the condition $s.sno = c.sno$

s.sno	s.name	s.location	c.sno	c.pno	c.cost
S2	M/s Balaji furniture	Bangalore	S2	P5	250
S3	M/s Premium furniture	Chennai	S3	P1	250
S3	M/s Premium furniture	Chennai	S3	P5	300
S3	M/s Premium furniture	Chennai	S3	P4	250

\therefore Option A. 4 is the correct answer

17 votes

-- Satbir Singh (21k points)

3.15.43 Sql: GATE CSE 2021 Set 1 | Question: 23

<https://gateoverflow.in/357428>



- $P(A > 10) = \frac{10}{15} = \frac{2}{3}$
- $P(B = 18) = \frac{1}{20}$
- $P(A > 10 \wedge B = 18) = \frac{2}{3} \times \frac{1}{20} = \frac{1}{30}$

$$\begin{aligned} P(A > 10 \vee B = 18) &= P(A > 10) + P(B = 18) - P(A > 10 \wedge B = 18) \\ &= \frac{2}{3} + \frac{1}{20} - \frac{1}{30} = \frac{40+3-2}{60} = \frac{41}{60} \end{aligned}$$

$$\text{Estimated number of tuples} = \frac{41}{60} \times 1200 = 820$$

The above answer is TRUE for SQL SELECT but not for Relational Algebra as by theory relational algebra operates on a set which means all the elements must be distinct. Since we have 15 distinct possible values for A and 20 distinct possible values for B , in strict relational algebra we'll get

$$\text{Estimated number of tuples} = \frac{41}{60} \times (15 \times 20) = 205.$$

Official Answer: 205 OR 820.

9 votes

-- zxy123 (2.8k points)

3.15.44 Sql: GATE CSE 2021 Set 2 | Question: 31

<https://gateoverflow.in/357509>



- It's a nested query but not Co-related query.

Evaluate the innermost query first.

```
select avg(salary)
from emp
```

It is given that `emp` represent employees of a company.

So, Option B is the correct answer.

2 votes

-- Shaik Masthan (50.4k points)



- ✓ classroom.gateoverflow.in Since, there is no specific joining condition specified, it will retrieve Cartesian product of the table

Number of rows = product of number of rows in each relation = $3 \times 2 = 6$

Number of columns = sum of number of columns = $3 + 2 = 5$

Answer: D.

52 votes

-- Sankaranarayanan P.N (8.5k points)



- ✓ Update on null gives null. Now, avg function ignores null values. So, here avg will be $(15 + 25 + 35)/3 = 25$.

<http://msdn.microsoft.com/en-us/library/ms177677.aspx>

Correct Answer: C

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44 votes

-- Arjun Suresh (332k points)



- ✓ Answer is C

Here in (i) when we update in STUDENT table Dept_id = NULL it is fine as a foreign key can be NULL.

But in (ii) if we set in DEPARTMENT table dept id = NULL it is not possible as PRIMARY KEY cannot be NULL.

Instead of update to NULL, if we try DELETE, then also it is not allowed as we have foreign key reference to it from STUDENT table with Dept_id = 1. DELETE ON CASCADE clause is a way to avoid this issue which will delete all referenced entries from the child table too but unless told we cannot assume this as this cause is not universally applicable.

40 votes

-- neha pawar (3.3k points)



- ✓ Answer is D) supply two or more items

The whole query returns the distinct list of suppliers who supply two or more items.

32 votes

-- Bran Stark (339 points)



- ✓ For color = "Red", did = {22, 22, 31, 31, 64}

For color = "Green", did = {22, 31, 74}

Intersection of Red and Green will give did = {22, 31} which is Karthikeyan and Boris

Answer: A

34 votes

-- Vikrant Singh (11.2k points)



```

    select D.dname
    from Drivers D
    where D.did in (
        select R.did
        from Cars C, Reserves R
        where R.cid = C.cid and C.colour = 'red'
        intersect
        select R.did
        from Cars C, Reserves R
        where R.cid = C.cid and C.colour = 'green'
    )

```

```
select R.did from Cars C, Reserves R where R.cid = C.cid and C.colour = 'red'
```

So, first, get 2 red cars by scanning 4 tuples of the cars relation. Now, for each of the two 'red' cars, we scan all the 10 tuples of the 'Reserves' relation and thus we get $2 \times 10 + 4 = 24$ comparisons. But this is not optimal. We can check in the reverse order for each tuple of the 'Reserves' relation because 'cid' is a primary key (hence unique) of 'Cars' relation.

Supposing our earlier selection is $\langle 102, 104 \rangle$ then this requires $3 + 7 \times 2 = 17$ comparisons. due to if $(R.cid == 102 || R.cid == 104)$

If the order was $\langle 104, 102 \rangle$, then $2 + 8 \times 2 = 18$ comparisons. due to if $(R.cid == 104 || R.cid == 102)$

Thus, totally 21 to 22 comparisons and gives $\langle 22, 31, 64 \rangle$ as did.

Similarly for the 'green' car we get $4 + 10 = 14$ comparisons. due to if $(R.cid == 103)$ and gives $\langle 22, 31, 74 \rangle$ as did.

Intersect requires $1 + 2 + 3 = 6$ comparisons in the best case and $3 + 2 + 3 = 8$ in the worst case and this gives $\langle 22, 31 \rangle$.

Finally, we have to locate the did 22 and did 31 from the driver table and did is the primary key. As told in the question, we use linear search and for 22, we hit on the first try, and for 31 we hit on the third try. So, $1 + 3 = 4$ comparisons.

Thus total no. of comparisons = $(21 \text{ to } 22) + 14 + (6 \text{ to } 8) + 4 = 45 \text{ to } 48$.

Correct Answer: B.

63 votes

-- Arjun Suresh (332k points)



D:

If Select clause consist aggregate and non - aggregate columns. All non aggregate columns in the Select clause must appear in Group By clause. But in this query Group by clause consists school-id instead of school-name

<http://weblogs.sqlteam.com/jeffs/archive/2007/07/20/but-why-must-that-column-be-contained-in-an-aggregate.aspx>

References



63 votes

-- erravi90 (131 points)



In a database system, unique timestamps are assigned to each transaction using Lamport's logical clock. Let $TS(T_1)$ and $TS(T_2)$ be the timestamps of transactions T_1 and T_2 respectively. Besides, T_1 holds a lock on the resource R, and T_2 has requested a conflicting lock on the same resource R. The following algorithm is used to prevent deadlocks in the database system assuming that a killed transaction is restarted with the same timestamp.

if $TS(T_2) < TS(T_1)$ then

T_1 is killed

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else T_2 waits.

Assume any transaction that is not killed terminates eventually. Which of the following is TRUE about the database system that uses the above algorithm to prevent deadlocks?

- A. The database system is both deadlock-free and starvation-free.
- B. The database system is deadlock-free, but not starvation-free.
- C. The database system is starvation-free, but not deadlock-free.
- D. The database system is neither deadlock-free nor starvation-free.

gate2017-cse-set1 databases timestamp-ordering deadlock normal

Answer 

Answers: Timestamp Ordering

3.16.1 Timestamp Ordering: GATE CSE 2017 Set 1 | Question: 42 [top](#)

<https://gateoverflow.in/118325>



In a database system, **unique** timestamps are assigned to each transaction using Lamport's logical clock

Since Unique Timestamps are assigned, so there is no question of two transaction having same timestamp.

Moreover, there is nothing mentioned about the size of the counter by which it can be determined that whether there will be case of timestamp wrap around or not.

So, there will be no timestamp wrap around.

In Lamport's logical clock Timestamps are assigned in increasing order of enumeration.

So, $T_i < T_j$ if Transaction T_i came into system before T_j .

The above scheme given is nothing but "**Wound-Wait**" Scheme in which younger transaction is killed by older transaction that came into system before this younger transaction came.[1][2]

So, this is a part of Basic Time-Stamp Ordering in Concurrency Control.

And Basic Time Stamp ordering protocol is deadlock free and **not starvation free, in general.**

Here in this question according to given condition, the database system is both deadlock free and starvation free as well , as it is Wound wait scheme and in case of wound wait it **avoid starvation**, because in Wound Wait scheme **we restart a transaction that has been aborted, with it's same original Timestamp** . If it restart with a new Timestamp then there is a possibility of Starvation (as larger TimeStamp transaction is aborted here and new Transaction which is coming next have always greater TimeStamp than previous one). But that is Not the case here.

Reference:

[1] <http://www.cs.colostate.edu/~cs551/CourseNotes/Deadlock/WaitWoundDie.html>

[2] <http://stackoverflow.com/questions/32794142/what-is-the-difference-between-wait-die-and-wound-wait>

Hence, answer is (A).

PS: The **Wound-wait scheme means :**

- The **newer transactions** are **killed** when an **older transaction** make a **request** for a **lock** being **held** by the **newer transactions** .
- Here the algorithm says $TS(T2) < TS(T1)$ means $T2$ is **older** transaction (as TS of $T2$ is less than TS of $T1$..means $T2$ come first then $T1$ come and TS is assign in increasing order), so **newer one is $T1$** and also question says $T1$ holds a lock on the resource R, and $T2$ has requested a conflicting lock on the same resource R.
- So $T1$ is killed as per Wound-wait scheme .

Reference :

<http://www.mathcs.emory.edu/~cheung/Courses/554/Syllabus/8-recv+serial/deadlock-compare.html>

timestamps are assigned to each transaction using Lamport's logical clock.

This line means timestamps are assigned in increasing order .

We can divide the answer into 3 parts:

Part 1: Is it Wound wait scheme?

Yes, given algorithm:

If $TS(T2) < TS(T1)$, then

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T1 is killed

else, T2 waits.

comes under wound wait scheme..as here old transaction is always survive and older transaction wounds newer transaction when both want to apply lock on same resource ..

Part 2 : Wound Wait avoid Starvation

Yes, How?

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as newer one is die and restart with same timestamp and older one is survive always so after execute older transaction that newer one can definitely execute and new transactions which are coming can die and restart again (previous newer became older that time).

Part 3 : Does Starvation freedom implies Deadlock freedom?

Yes, here no starvation means also No deadlock possibility.

In one line - wound wait -> no starvation -> no deadlock -> option A.

EDIT

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Another way to think about Deadlock and starvation

Deadlock is prevented because we are **violating NO-Premption** Condition for the deadlock to happen.

How starvation free? Here Bounded waiting for transactions is ensured.HOW?

Consider "n" transactions T_1, T_2, \dots, T_n having their timestamps order as $TS(T_1) < TS(T_2) < \dots < TS(T_n)$ (Timestamps are unique)

Consider for $k, 1 < k \leq n$ a transaction T_k , this transaction T_k can be atmost preempted by Transaction sets T_1, T_2, \dots, T_{k-1} and it is also given "**Any transaction that is not killed eventually terminates**". Means Eventually a time would come when, all transactions T_j having $TS(T_j) < TS(T_k)$ will terminate and T_k would get chance without preemption. And this J would lie in range $1 \leq j \leq k-1$. **Bounded waiting ensured.**

References



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111 votes

-- Ayush Upadhyaya (28.4k points)

3.17

Transaction And Concurrency (28) top

3.17.1 Transaction And Concurrency: GATE CSE 1999 | Question: 2.6 top

https://gateoverflow.in/1484



For the schedule given below, which of the following is correct:

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