Ejercicio 1

Caja negra:

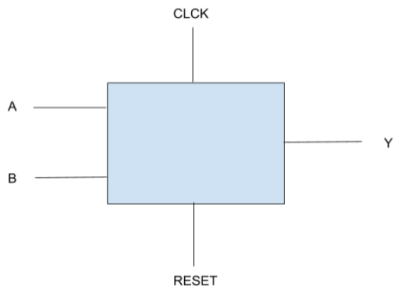


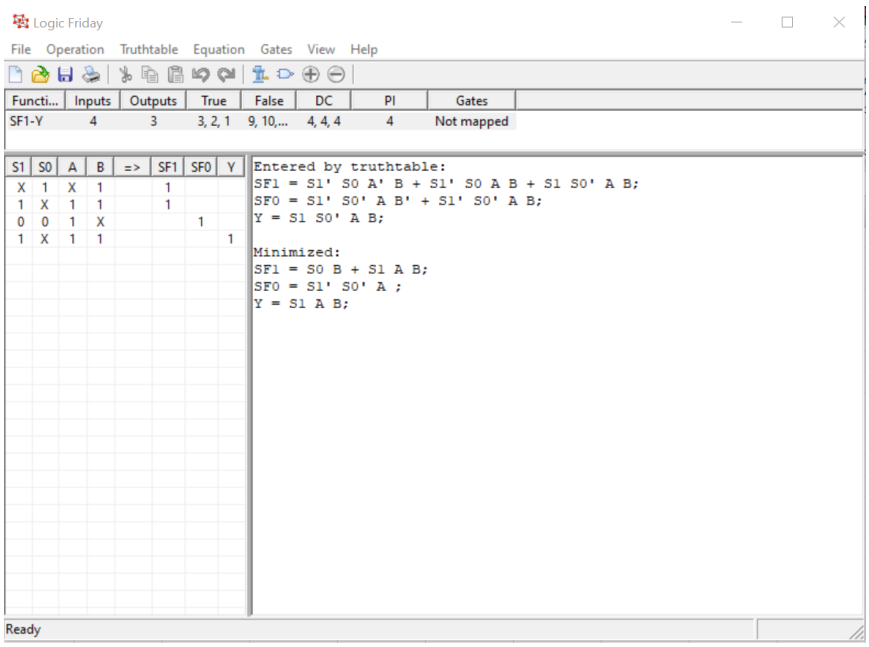
Tabla de transiciones de estado sin codificar:

Estado inicial	A	B	Estado futuro	Y
S0	0	X	S0	0
S0	1	X	S1	0
S1	X	0	S0	0
S1	X	1	S2	0
S2	0	0	S0	0
S2	1	1	S2	1

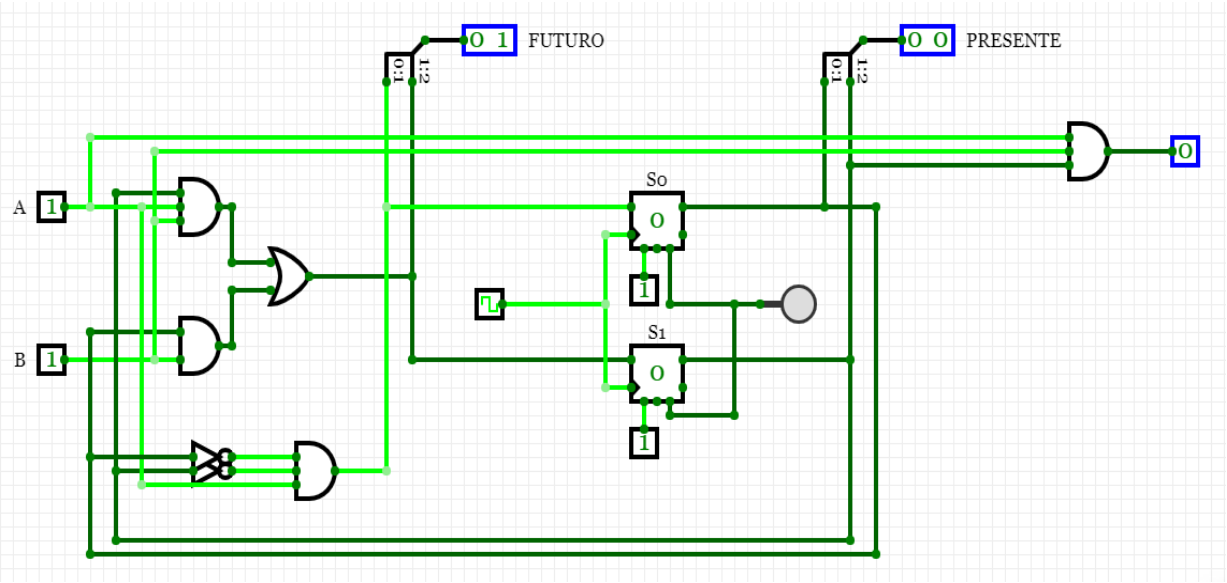
Tabla de transiciones de estado codificada:

Estado inicial	A	B	Estado futuro	Y
0 0	0	X	0 0	0
0 0	1	X	0 1	0
0 1	X	0	0 0	0
0 1	X	1	1 0	0
1 0	0	0	0 0	0
1 0	1	1	1 0	1

Tabla y ecuaciones booleanas reducidas:

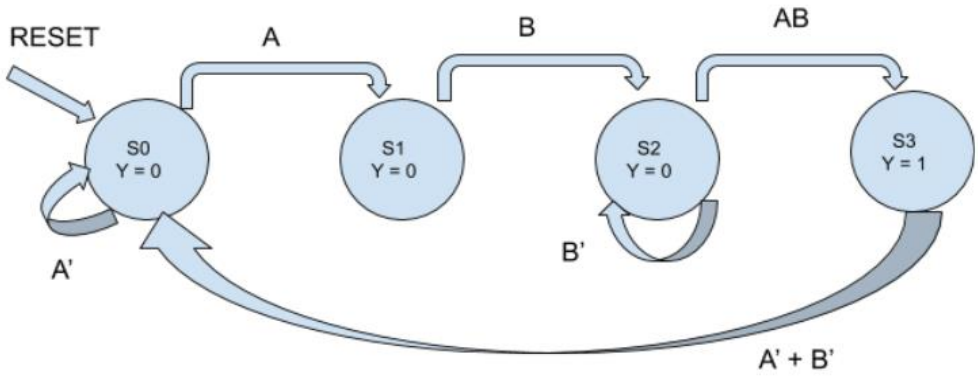


Implementación en circuit verse:



Ejercicio 2

FSM de Moore del diagrama de ejercicio 1:



Ejercicio 3

Caja negra:

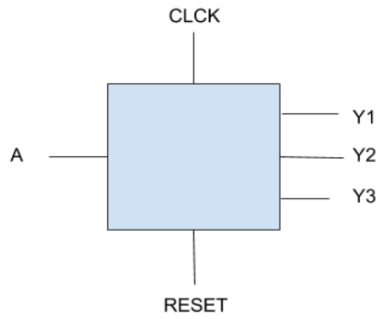


Tabla de transiciones de estado sin codificar:

Estado inicial	A	Estado futuro	Y1	Y2	Y3
S0	0	S7	0	0	0
S0	1	S1	0	0	0
S1	0	S0	0	0	1
S1	1	S2	0	0	1
S2	0	s1	0	1	1
S2	1	S3	0	1	1
S3	0	S2	0	1	0
S3	1	S4	0	1	0
S4	0	S3	1	1	0
S4	1	S5	1	1	0
S5	0	S4	1	1	1
S5	1	S6	1	1	1
S6	0	S5	1	0	1
S6	1	S7	1	0	1
S7	0	S6	1	0	0
S7	1	S0	1	0	0

Tabla de transiciones de estado codificada:

Estado inicial	A	Estado futuro	Y1	Y2	Y3
0 0 0	0	1 1 1	0	0	0
0 0 0	1	0 0 1	0	0	0
0 0 1	0	0 0 0	0	0	1
0 0 1	1	0 1 0	0	0	1
0 1 0	0	0 0 1	0	1	1
0 1 0	1	0 1 1	0	1	1
0 1 1	0	0 1 0	0	1	0
0 1 1	1	1 0 0	0	1	0
1 0 0	0	0 1 1	1	1	0
1 0 0	1	1 0 1	1	1	0
1 0 1	0	1 0 0	1	1	1
1 0 1	1	1 1 0	1	1	1
1 1 0	0	1 0 1	1	0	1
1 1 0	1	1 1 1	1	0	1
1 1 1	0	1 1 0	1	0	0
1 1 1	1	0 0 0	1	0	0

Diagrama de transiciones de estado:

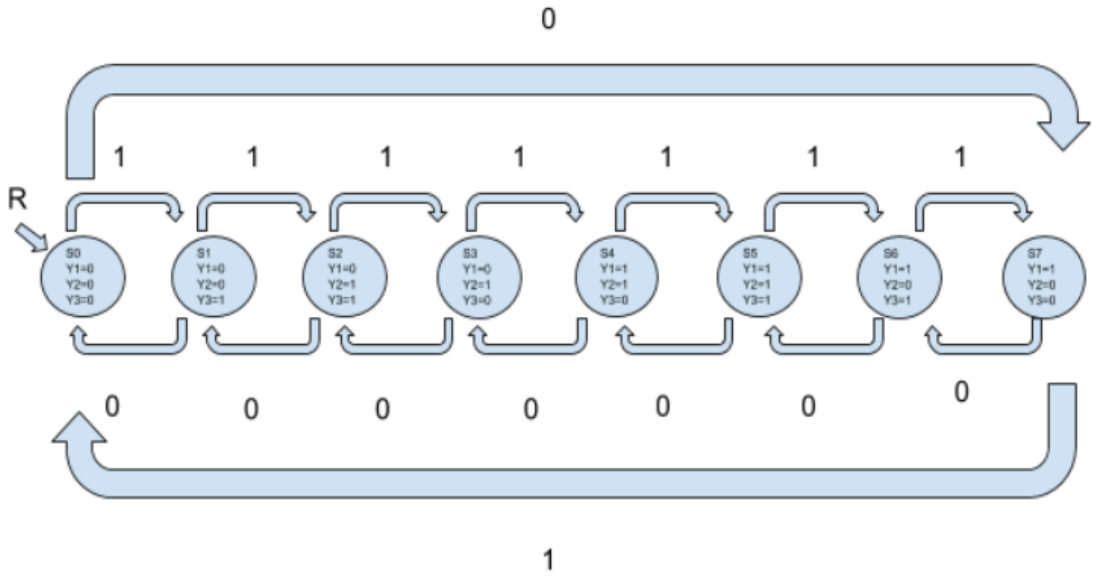
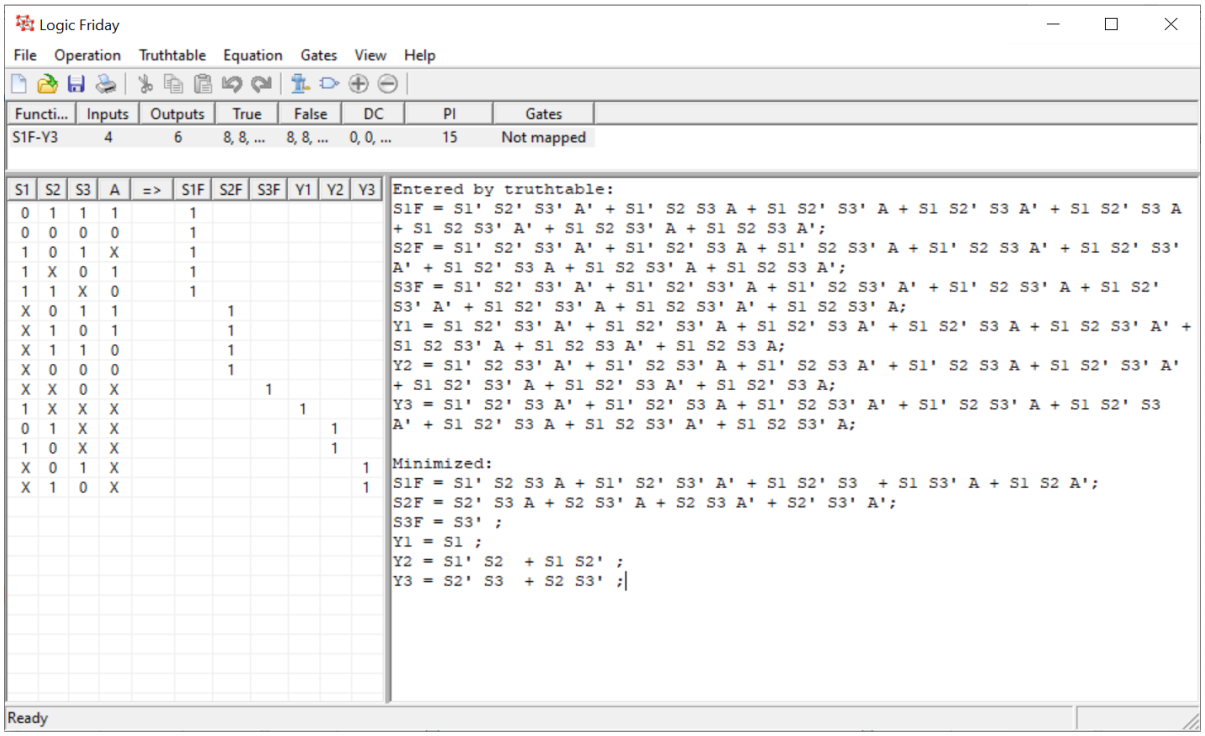
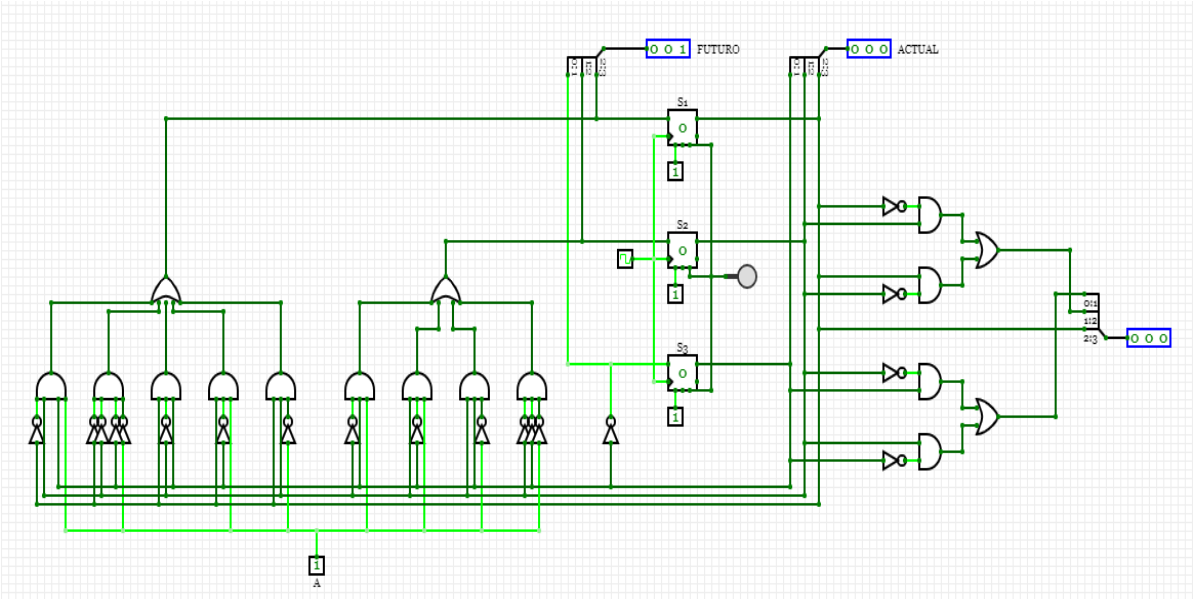


Tabla y ecuaciones booleanas reducidas:



Implementación en circuit verse:



Ejercicio 6

Diagrama de timming - Ejercicio 1

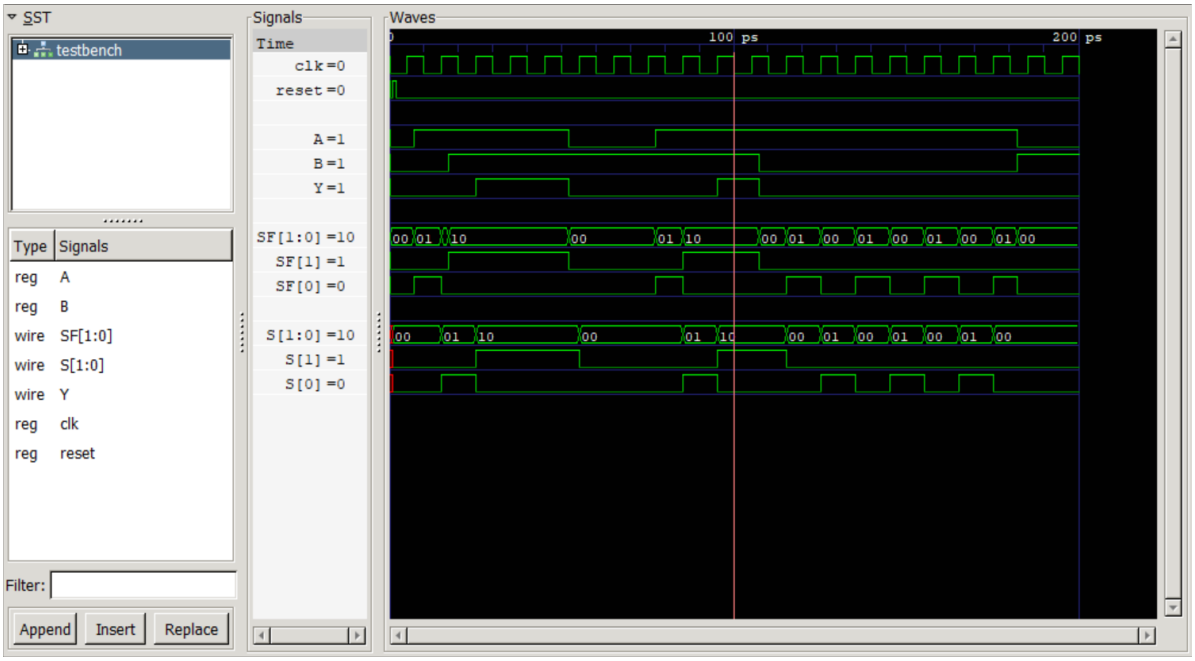


Diagrama de timming - Ejercicio 3