

Ejercicio 1

Caja negra:

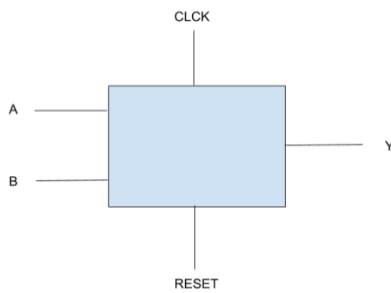


Tabla de transiciones de estado sin codificar:

Estado inicial	A	B	Estado futuro	Y
S0	0	X	S0	0
S0	1	X	S1	0
S1	X	0	S0	0
S1	X	1	S2	0
S2	0	0	S0	0
S2	1	1	S2	1

Tabla de transiciones de estado codificada:

Estado inicial	A	B	Estado futuro	Y
00	0	X	00	0
00	1	X	01	0
01	X	0	00	0
01	X	1	10	0
10	0	0	00	0
10	1	1	10	1

Tabla y ecuaciones booleanas reducidas:

Logic Friday

File Operation Truthtable Equation Gates View Help

Funci... Inputs Outputs True False DC PI Gates

SF1-Y 4 3 3, 2, 1 9, 10, ... 4, 4, 4 4 Not mapped

S1	S0	A	B	=>	SF1	SF0	Y
X	1	X	1		1		
1	X	1	1		1		
0	0	1	X			1	
1	X	1	1				1

Entered by truthtable:

$$SF1 = S1' S0 A' B + S1' S0 A B + S1 S0' A B;$$

$$SF0 = S1' S0' A B' + S1' S0' A B;$$

$$Y = S1 S0' A B;$$

Minimized:

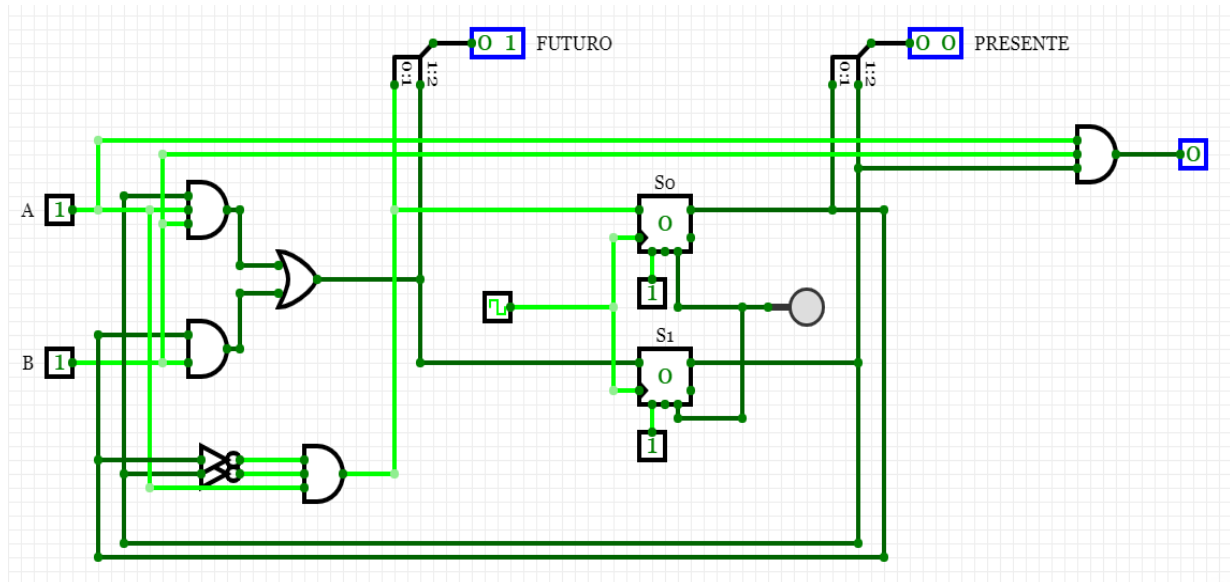
$$SF1 = S0 B + S1 A B;$$

$$SF0 = S1' S0' A ;$$

$$Y = S1 A B;$$

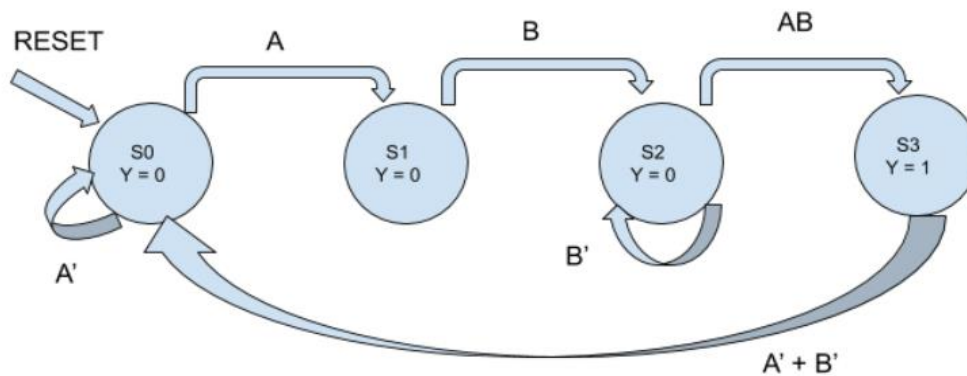
Ready

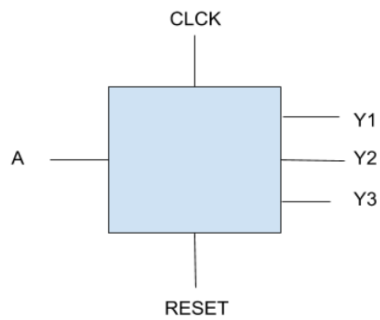
Implementación en circuit verse:



Ejercicio 2

FSM de Moore del diagrama de ejercicio 1:



Ejercicio 3**Caja negra:****Tabla de transiciones de estado sin codificar:**

Estado inicial	A	Estado futuro	Y1	Y2	Y3
S0	0	S7	0	0	0
S0	1	S1	0	0	0
S1	0	S0	0	0	1
S1	1	S2	0	0	1
S2	0	s1	0	1	1
S2	1	S3	0	1	1
S3	0	S2	0	1	0
S3	1	S4	0	1	0
S4	0	S3	1	1	0
S4	1	S5	1	1	0
S5	0	S4	1	1	1
S5	1	S6	1	1	1
S6	0	S5	1	0	1
S6	1	S7	1	0	1
S7	0	S6	1	0	0
S7	1	S0	1	0	0

Tabla de transiciones de estado codificada:

Estado inicial	A	Estado futuro	Y1	Y2	Y3
0 0 0	0	1 1 1	0	0	0
0 0 0	1	0 0 1	0	0	0
0 0 1	0	0 0 0	0	0	1
0 0 1	1	0 1 0	0	0	1
0 1 0	0	0 0 1	0	1	1
0 1 0	1	0 1 1	0	1	1
0 1 1	0	0 1 0	0	1	0
0 1 1	1	1 0 0	0	1	0
1 0 0	0	0 1 1	1	1	0
1 0 0	1	1 0 1	1	1	0
1 0 1	0	1 0 0	1	1	1
1 0 1	1	1 1 0	1	1	1
1 1 0	0	1 0 1	1	0	1
1 1 0	1	1 1 1	1	0	1
1 1 1	0	1 1 0	1	0	0
1 1 1	1	0 0 0	1	0	0

Diagrama de transiciones de estado:

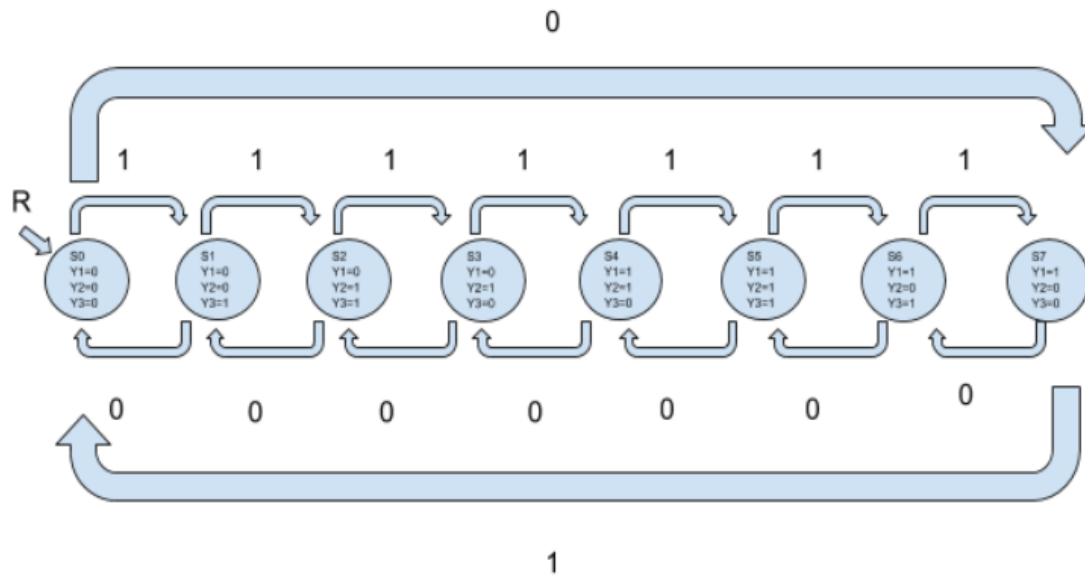


Tabla y ecuaciones booleanas reducidas:

Logic Friday

File Operation Truthtable Equation Gates View Help

Funci... Inputs Outputs True False DC PI Gates

S1F-Y3 4 6 8, 8, ... 8, 8, ... 0, 0, ... 15 Not mapped

S1	S2	S3	A	=>	S1F	S2F	S3F	Y1	Y2	Y3
0	1	1	1		1					
0	0	0	0							
1	0	1	X		1					
1	X	0	1		1					
1	1	X	0		1					
X	0	1	1			1				
X	1	0	1			1				
X	1	1	0			1				
X	0	0	0			1				
X	X	0	X				1			
1	X	X	X					1		
0	1	X	X						1	
1	0	X	X							1
X	0	1	X							1
X	1	0	X							1

Entered by truthtable:

$$S1F = S1' S2' S3' A' + S1' S2 S3 A + S1 S2' S3' A + S1 S2' S3 A' + S1 S2' S3 A + S1 S2 S3' A' + S1 S2 S3 A' + S1 S2 S3 A';$$

$$S2F = S1' S2' S3' A' + S1' S2' S3 A + S1' S2 S3' A + S1' S2 S3 A' + S1 S2' S3' A' + S1 S2' S3 A + S1 S2 S3' A' + S1 S2 S3 A';$$

$$S3F = S1' S2' S3' A' + S1' S2' S3 A + S1' S2 S3' A + S1' S2 S3 A' + S1 S2' S3' A' + S1 S2' S3 A + S1 S2 S3' A' + S1 S2 S3 A';$$

$$Y1 = S1 S2' S3' A' + S1 S2' S3 A + S1 S2' S3 A' + S1 S2' S3 A' + S1 S2' S3 A + S1 S2' S3 A' + S1 S2' S3 A' + S1 S2' S3 A';$$

$$Y2 = S1' S2 S3' A' + S1' S2 S3 A + S1' S2 S3' A + S1' S2 S3 A' + S1' S2 S3 A + S1' S2 S3' A' + S1' S2 S3 A' + S1' S2 S3 A';$$

$$Y3 = S1' S2' S3 A' + S1' S2' S3 A + S1' S2 S3' A' + S1' S2 S3 A' + S1' S2 S3 A + S1' S2 S3' A' + S1' S2 S3 A' + S1' S2 S3 A';$$

Minimized:

$$S1F = S1' S2 S3 A + S1' S2' S3' A' + S1 S2' S3 + S1 S3' A + S1 S2 A';$$

$$S2F = S2' S3 A + S2 S3' A + S2 S3 A' + S2' S3' A';$$

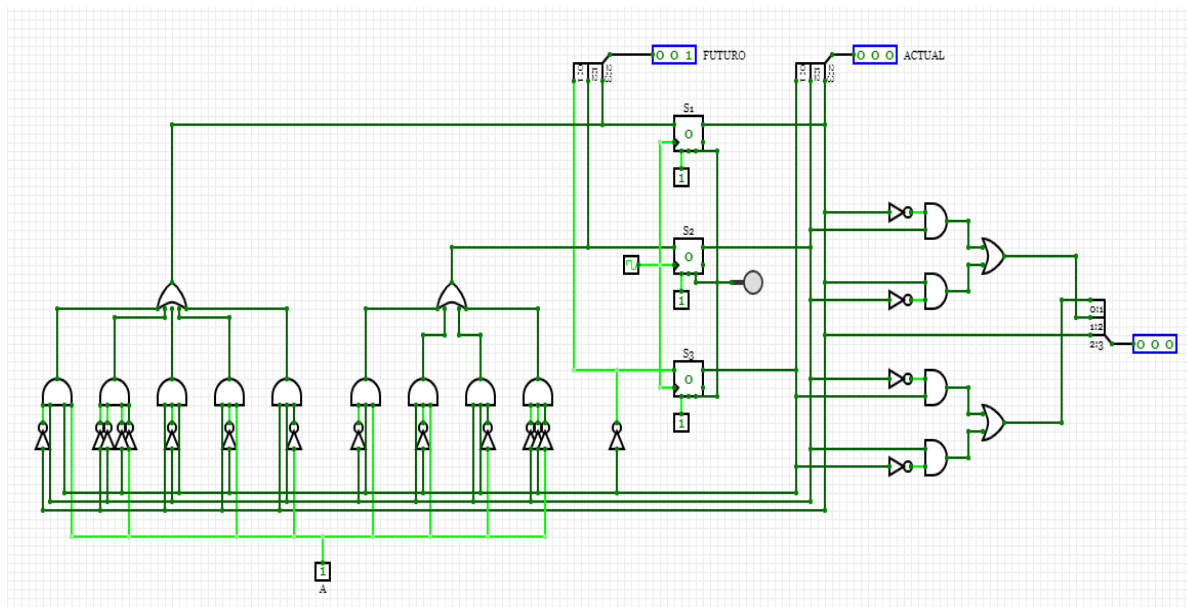
$$S3F = S3';$$

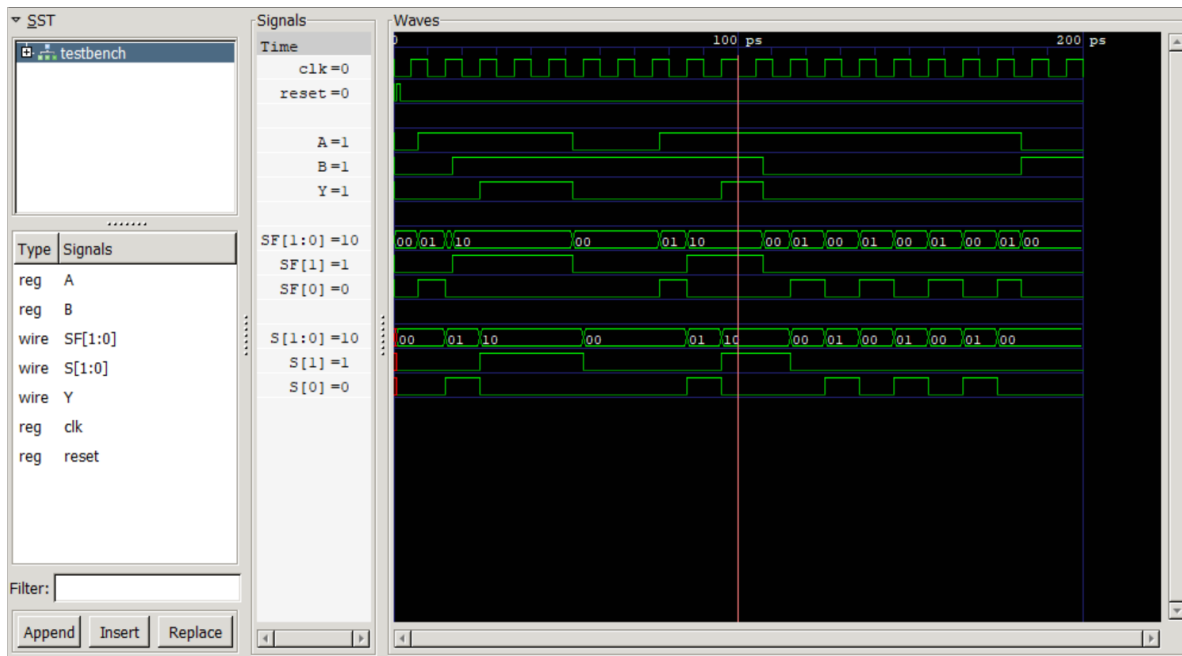
$$Y1 = S1;$$

$$Y2 = S1' S2 + S1 S2';$$

$$Y3 = S2' S3 + S2 S3';$$

Implementación en circuit versee:



Ejercicio 6**Diagrama de timming - Ejercicio 1****Diagrama de timming - Ejercicio 3**