4 × Input / Output

CLB 8 × LUT4 + FF

EG  $4 \times 32$  bit, 2r1w

MAC  $8 \text{ bit} \cdot 8 \text{ bit} + 20 \text{ bit}$ 

BRAM 32 × 256 bit, 1rw1r

ADC 12 bit SAR-ADC

DAC 8 bit R-DAC

TERM Termination

**NULL** No tile

NULL	TERM	TERM	TERM	TERM	TERM								
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	SRAM
10	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB		CLB	CLB	CLB	
10	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	SRAM
10	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB		CLB	CLB	CLB	
10	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	SRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB		CLB	CLB	CLB	
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	SRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	M M	CLB	CLB	CLB	SR
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	ပ္	CLB	CLB	CLB	SRAM
10	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MA	CLB	CLB	CLB	SR
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	SRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	M	CLB	CLB	CLB	SR
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	SRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB		CLB	CLB	CLB	
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	МАС	CLB	CLB	CLB	SRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	M	CLB	CLB	CLB	SR
NULL	TERM	TERM	TERM	TERM	ADC	ADC	DAC	DAC	TERM	TERM	TERM	TERM	TERM