

IO	4 × Input / Output
CLB	8 × LUT4 + FF
REG	4 × 32 bit, 2r1w
MAC	8 bit · 8 bit + 20 bit
BRAM	32 × 256 bit, 1rw1r
ADC	12 bit SAR-ADC
DAC	8 bit R-DAC
TERM	Termination
NULL	No tile

NULL	TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM	TERM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	BRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	BRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	BRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	BRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	BRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	BRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	BRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	SRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	BRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	BRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	BRAM
IO	CLB	CLB	CLB	REG	CLB	CLB	CLB	CLB	MAC	CLB	CLB	CLB	BRAM
NULL	TERM	TERM	TERM	TERM	ADC	ADC	DAC	DAC	TERM	TERM	TERM	TERM	TERM