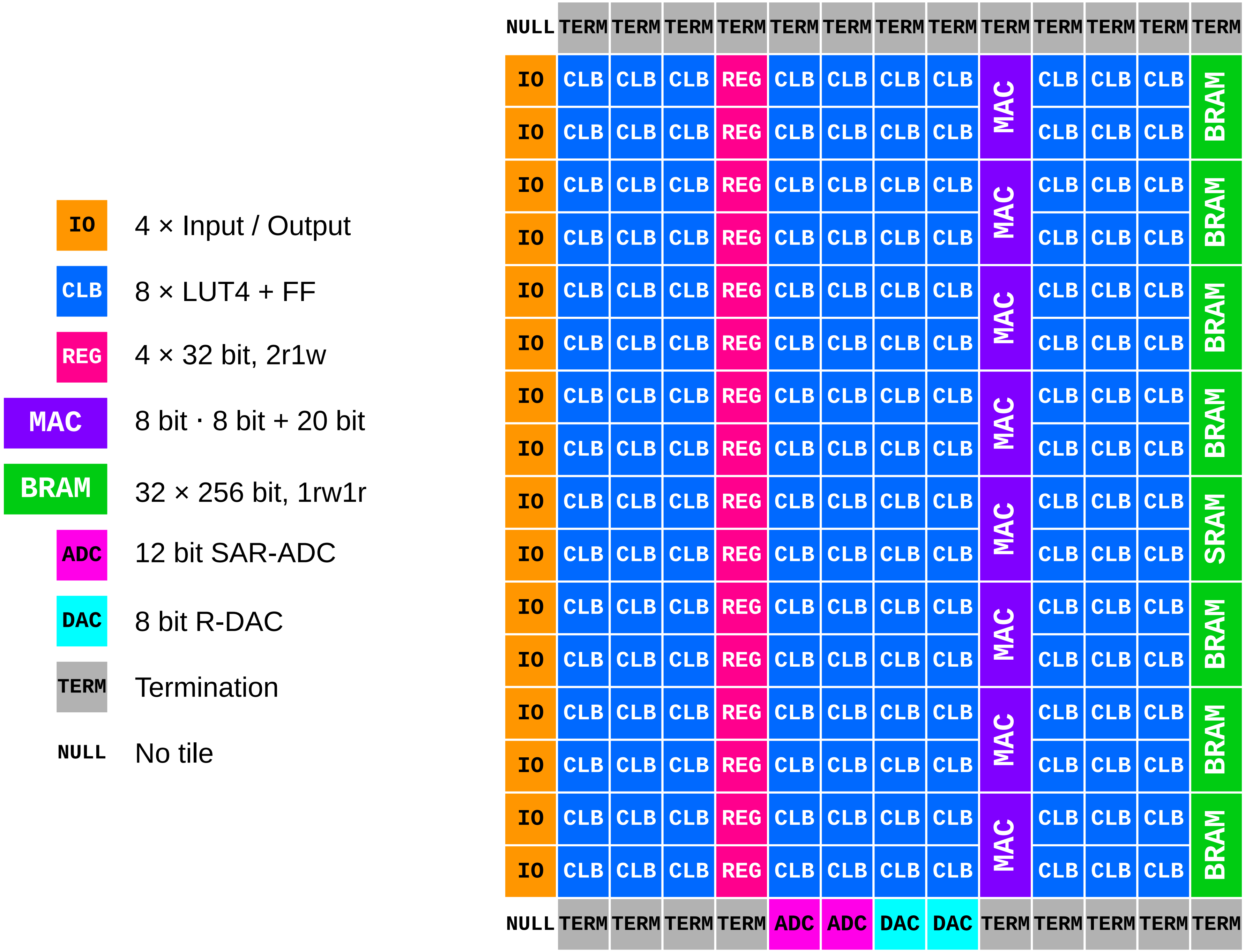
IO 4 × Input / Output
CLB 8 × LUT4 + FF
REG 4 × 32 bit, 2r1w
MAC 8 bit · 8 bit + 20 bit
BRAM 32 × 256 bit, 1rw1r
ADC 12 bit SAR-ADC
DAC 8 bit R-DAC
TERM Termination
NULL No tile
NULL
TERM
IO
CLB
REG
MAC
BRAM
SRAM
ADC
DAC