Evaluation of GaN as a Radiation Detection Material

THESIS

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By

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Abstract

The semiconductor material Gallium Nitride (GaN) has been widely applied in the fields of optoelectronic and high power devices, e.g., light emission diodes (LEDs) and high electron mobility transistors (HEMTs). Due to its remarkable properties, especially the wide band gap (3.39 eV), large dislocation density (N: 109 eV and Ga: 45 eV) and high thermal stability (Melting point: 2500 ^{0}C), GaN is now attracting considerable attention in application for nuclear radiation detections. Up until now, several promising results have been obtained for alpha particle detection based on Schottky diode structure fabricated on thin-film epitaxial semi-insulating or undoped GaN. Some research has also been carried out for gamma and neutron detections by employing special material such as Gadolinium doped GaN and structures such as coplanar structure. However, the development of GaN radiation detector is still plagued by the material and fabrication problems; thus, a systematic study for the influence of different type GaN materials and detector structures on the performance of the device is of great significance.

In this research, two types of structures, sandwich and mesa, are employed to fabricate Schottky diode detector based on three kinds of GaN materials: Compensated freestanding semi-insulating (SI) GaN, undoped (UD) freestanding GaN and Gadolinium

doped super-lattice (SL) GaN. Current-Voltage (I-V) characteristic is used to evaluate the quality of these devices. The major findings in this research are: for SI material, Ohmic contact can be successfully produced by silicon implantation (dose: 1×10^{16} cm^{-3}) and high temperature activation (temperature: 1150 ^{0}C) processes. Schottky contact can be formed on GaN substrate purchased from Ammono Company; it cannot be formed on GaN purchased from Kyma due to surface decomposition. As a radiation detection material, SI GaN suffers low charge collection efficiency (CCE) due to the deep level trapping centers introduced by the compensated iron impurities. However, if the thickness of the wafer can be controlled within a limit value *(i.e.,* smaller than the alpha particle projection range, for instance), there is still a possibility for partial collection of the radiation signals. For UD GaN, Si implantation is also needed to form good Ohmic contact. For making Schottky contact, surface degradation effect is a major concern that can be eliminated by following a chemical physical polishing process after high temperature activation. When used for radiation detection, UD GaN needs high bias voltage to obtain a large depletion depth, which at the same time results in a high leakage current. Thus, only high quality GaN grown by MOCVD with carrier concentration on the orders of or less than 10^{16} cm^{-3} can be used for radiation detection. For Gd doped super-lattice thin-film GaN grown on a foreign substrate, relatively good Schottky diode can be obtained by decreasing the size of the contact, due to which, however, both the energy deposition rate and signal counting rate are largely decreased. Thus, both the thickness of the material and the size of the device should be carefully controlled in this case. Based on the theoretical analysis of the I-V characteristic, a Surface Parallel Resistance Model (SPRM) is proposed that could successfully explain the origination of

the leakage current for these devices. Finally, a new detector structure is proposed by taking into account all these considerations. This research provides some good insights into the making of radiation detectors based on GaN.

The SL GaN was grown by Professor Roberto Myers in the Department of Material Science and Engineering, the Ohio State University (OSU). Most fabrication processes, such as photolithography, etching, metal deposition, rapid temperature annealing, wire bonding, etc. were performed in the Nanotech West Lab (NTW), OSU; the Asher process was done in Dreese Lab, Department of Computer Science and Engineering. The characterization processes were completed in NTW Lab and Nuclear Analysis and Radiation Sensor Laboratory (NARS), Department of Mechanical and Aerospace Engineering, OSU.

Dedication

Dedication to my parents

Acknowledgments

This research project would not have been possible without the support of many people. First and foremost, I would like to express my utmost gratitude to my advisor, Dr. Lei (Raymond) Cao for his invaluable support, guidance and encouragement; he is also the person who has won most of my respect while studying in the US. I am also thankful to Dr. Xiaodong Sun for dedicating his valuable time to be my committee member. Special thanks go to my senior Zeng Zhang for his assistance working in NTW Lab; I am also thankful to Tim Garcia for sharing his broad knowledge with me. Finally, I also want to say thank you to all my classmates for their in time help in my daily life.

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Publications

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Fields of Study

Major Field: Nuclear Engineering

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1. Introduction

Recently, the semiconductor material GaN has been intensely studied for potential use as a radiation detection material. However, the development has been plagued by material and fabrication problems, such as thin wafer thickness, large defect density and unreliable metal contacts [1]. In this research, several detector configurations based on Schottky diode structure are fabricated on different types of GaN materials, and their performance is primarily evaluated by current-voltage characteristic. The purpose is to find the most promising material available and detector structure for GaN to make a radiation detector.

Compound semiconductors like GaN, SiC and GaAs have several advantages over the traditional elemental materials Si and Ge, such as, wide band-gap, high critical field, large displacement energy and high carrier mobility, which make them more suitable for application to the field of radiation detections. During the past several decades, many studies have been carried out for these wide band-gap semiconductor materials. Among this list of materials, the growth technology for GaAs has been fully developed, but GaN and SiC are still immature [2]. For GaAs, the intrinsic EL2 defect has prevent it from further development [3]; SiC and GaN have very similar properties,

but GaN's electron mobility and critical field is higher than SiC indicates it would be the best choice for radiation detections [4].

Until now, several promising results have been reported for GaN-based radiation detectors. Based on Schottky diode structure, alpha particle detectors were first successfully fabricated by J. Vaitkus on a 2 μm semi-insulating GaN, and a charge collection efficiency of 100% has been found [5, 6]. These detectors were also studied by J. Grant for its applications in harsh radiation environments [7, 8]. Several years later, L. Min fabricated an alpha detector on a 3 μm undoped GaN grow by MOCVD with a carrier concentration of 4×10^{16} cm^{-3} [9]. Thin-film undoped GaN grown by different technologies were further evaluated by A.Y. Polyakow for their application for alpha particle detection [10]. Undoped GaN has also shown a spectroscopic response to UV light by employing coplanar structure with a pitch of several to hundred micrometers [11]. Besides the Schottky diode structure, GaN-based PIN structure has also been developed for both alpha particle and x-ray detection [12].

In addition, other novel structures such as super-lattice [13], nanowire p-n junction [14] and quantum dot detectors [15] have also been tested for possible photo detections. Neutron detection has been tried by adding gadolinium neutron convertors but no promising result has been obtained [16]. Recently, the most exciting result has been the realizing of alpha particle detector based on freestanding undoped GaN, in which a thick (~30 μm) low carrier concentration layer (10^{13}-10^{14} cm^{-3}) GaN was successfully grown by HVPE used to form the depletion region [17]. However, the research field of GaN as a radiation detection material is still far from fully developed, and the

performance of these detectors still need to be improved. The difficulty of the development mainly lies in the immature GaN growth technology. For the several available techniques, MBE and MOCVD can grow a high quality GaN, but the grown thickness (maximum ~12 μm for MOCVD) is less than the range of alpha particle [17]; HVPE allows for the growth of several millimeters GaN substrate, but the background donor concentration is usually higher than 10^{16} cm^{-3}, which value results in a high leakage current when the device is made [18]. Compensating the donor with acceptor materials such as Fe will again introduce deep level trapping centers [19, 20]. Thus, finding the most promising material for radiation detection based on the available growth techniques is urgent for any future progress of this area.

In this research, the quality of Schottky diode fabricated on different kinds of GaN materials are evaluated by current-voltage characteristics, and the influence of the fabrication process and detector structure are also investigated. The analysis of the leakage current generates a theoretical model named surface parallel resistance model, which can be used to estimate the effect of the leakage current on the performance of the devices. Based on these analyses, the most promising material we have found remains the semi-insulating thin film GaN grown on a foreign substrate, which guarantees both a low leakage current and a wide depletion depth. However, one note that needs to be made is that when the growth techniques are improved, thick freestanding undoped GaN with lower carrier concentration ($<10^{16}$ cm^{-3}) should become the most promising material for making radiation detectors.

2. Concept and Theory

2.1 Operating Principle of Semiconductor Detectors

Figure 1 presents a schematic diagram of a semiconductor detector, in which the semiconducting material is sandwiched between two metal electrodes. When a bias voltage is applied to the electrodes, the thickness of the depletion region inside the semiconductor will be increased. At this moment, if an incident charged particle enters the depletion region, electron-hole pairs (e-h) will be generated and drift toward the electrodes to form a signal. The strength of the signal, i.e., the number of e-h pairs generated, is proportional to the energy deposited by the charged particle in the depletion region [21].

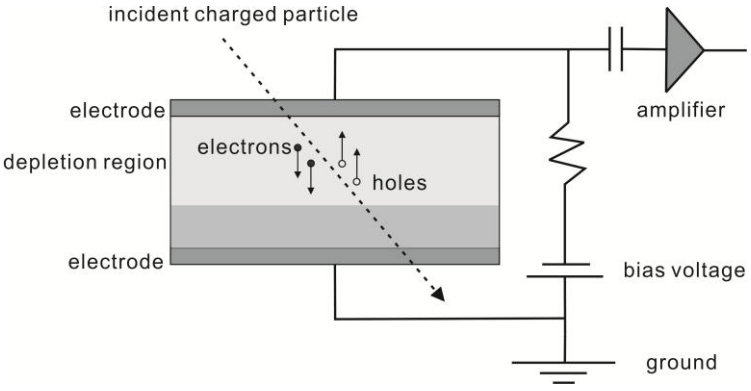


Figure 1. Operation principle of semiconductor detector

2.2 Requirements of The Semiconductor Materials

For a desired performance of semiconductor detectors, the properties of the semiconductor material play the most important role. The following requirements need to be met in order to fabricate a high quality detector [1]:

1, large band gap to ensure low leakage current, and the band gap should be larger than 0.14eV to prevent the generation of thermal carriers at room temperature;

2, the resistivity should be greater than 10^8 Ohm-cm to allow large bias voltage and thus to obtain a fast carrier drift velocity;

3, small e-h pair creation energy to maintain a high signal-to-noise ratio;

4, low dielectric constant to reduce white series noise [22];

5, high purity, homogeneous and single-crystal material to ensure high charge collection efficiency (CCE);

6, high mobility-lifetime product for charge carries to again ensure high CCE and also a good energy resolution. Specifically, for electrons and holes, this value should be better than 10^{-2} and 10^{-3} cm^2V^{-1}, respectively;

An additional two features are preferred when working in high temperature and hash radiation environments:

7, high threshold displacement energy to operate in harsh radiation environments or even in corrosive atmospheres;

8, high thermal conductivity to work at elevated temperatures.

2.3 Device Structure

In addition to the semiconductor material, the electrical properties of the depletion region also largely affect the performance of the detector. Both ***Schottky diode and p-n junction*** structures can be used to form the depletion region. In our research, Schottky diode is selected in which the depletion region is formed directly under the Schottky metal contact, thus offering simplicity in device fabrication. Other differences between the two structures include: a), in a Schotky diode, the current is carried by majority carriers instead of minority carriers in a p-n junction, which makes it suitable for high-frequency applications; b), Schottky diode has a lower turn-on voltage, which makes it attractive for clamping and clipping applications; c), Schottky diode has a higher leakage current when reverse biased, and thus special structures must be employed such as the guard ring structure to be discussed later for small signal detection. Figure 2 compares the current-voltage characteristics for the two devices [23].

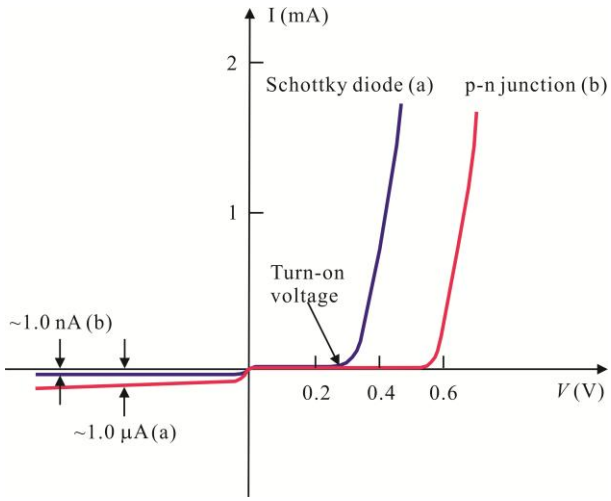


Figure 2. Current-voltage characteristics of a p-n junction and a Schottky diode

2.4 Schottky Contact

The quality of the Schottky diode is determined by Schottky contact. Schottky contact is formed in a metal-semiconductor (MS) junction where the work function of the metal is higher than the semiconductor. Schottky contact can be depicted by three parameters, as shown in Figure 3: ***depletion region, Schottky barrier height and built-in potential***. The depletion region is also named the "space charge region" or "active region", in which the e-h pairs are generated upon receiving radiations. Schottky barrier height is the potential barrier seen by electrons moving from the metal into the semiconductor, and built-in potential is the barrier seen by electrons moving from the conduction band of the semiconductor into the metal [24]. Schottky barrier height does not change under a bias voltage, and thus electrons cannot move from the metal to the semiconductor and a Schottky contact is formed. However, the width of the depletion region will change according to the bias voltage which property is used to form Ohmic contact, as will be discussed later.

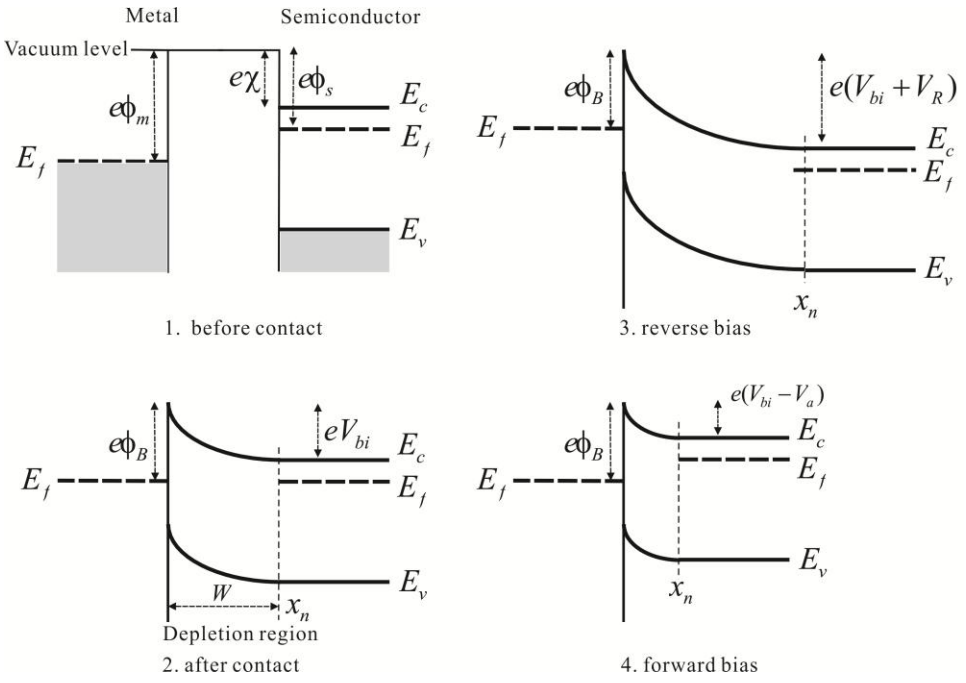


Figure 3. Formation of Schottky contact

2.5 Current Flow Mechanisms

Ideally, no electrons can pass through the Schottky barrier when the contact is reverse biased, as discussed in the preceding section. However, under forward bias, electrons can transport from the semiconductor to the meal via three mechanisms: ***thermionic emission (TE), thermionic field emission (TFE) and field emission (FE)***. When the semiconductor is lightly doped (carrier concentration $\mathbf{N_D \leq 10^{17} cm^{-3}}$), because of the wide depletion region, electrons can only pass through the built-in barrier from the top of the barrier since the forward bias has lowered the barrier height. This is the case of TE shown in Figure 4(a). For intermediately doped semiconductors ($\mathbf{10^{17}<N_D<10^{18}\ cm^{-3}}$), the depletion region becomes thinner, but not sufficiently so to allow direct tunneling effect. Electrons will first gain a certain amount of energy from the bias voltage and then

tunneling through the barrier at the height where it is sufficiently thin. This is TFE as shown in Figure 4(b). In heavily doped semiconductors ($\mathbf{N_D \geq 10^{18}\ cm^{-3}}$), the depletion region is thin enough for the electrons at the bottom of the conduction band to be able to tunnel through the barrier directly. This case is FE, as shown in Figure 4(c). Thus, a heavily doped layer can be utilized to form an Ohmic contact in which current can pass through either direction [25].

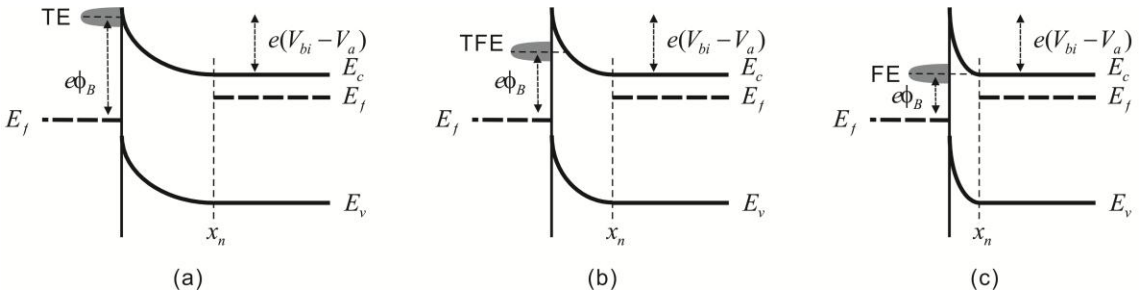


Figure 4. Current flow mechanisms for a forward biased Schottky contact: (a) thermionic emission, (b) thermionic field emission and field emission

2.6 Ohmic Contact

Ohmic contact requires the resistance of the contact to be negligible compared with the voltage drop across the device, and the current-voltage relationship follows the linear Ohmic law: $R = V/I$ [26]. For most applicable devices, a resistance lower than 10^{-5} $\Omega \cdot cm^2$ is desired [27]. Generally it is difficult to form Ohmic contacts to wide band gap semiconductors because only a few metals can satisfy the work function requirements. However, by doping a high carrier concentration layer on the surface of the semiconductor, carriers can tune through the thin barrier and in this way an Ohmic contact can be formed. Additionally, the selection of metal contact scheme is also

important to the optimization of an Ohmic contact, Ti/Al/Ni/Au Ohmic contact followed by rapid thermal annealing (RTA) at 850^0C for 30 s has been broadly used for GaN [28]. Table 1 summarized the Ti/Al based Ohmic contacts fabricated on n-type GaN [29].

Material	Annealing temperature (^{0}C)	Resistance
Ti/Al	900	8×10^{-6} Ohm-cm^2
Ti/Al	850	1.6×10^{-4} Ohm-cm^2
Ti/Al/Au	750	6×10^{-6} Ohm-cm^2
Ti/Al/Pt/Au	850	12×10^{-6} Ohm-cm^2
Ti/Al/Ni/Au	850	0.5 Ohm-mm
Ti/Al/Ni/Au	830	1.5 Ohm-mm

Table 1. Ti/Al based Ohmic contacts on n-GaN

2.7 Leakage Current and Guard Ring Structure

During operations, leakage current will degrade the performance of the detector by introducing electronic noise. Two kinds of leakage exist in semiconductor detectors, as shown in Figure 5(a): ***Bulk leakage and surface leakage current***. Bulk leakage current exists because of the finite conductivity of the semiconductor material; surface leakage current is generated due to the current path formed by the surface defect. At the level of 10^{-9} A, the surface leakage may be more significant than bulk leakage [21], and must thus be controlled to obtain a sufficient signal-to-noise ratio. Guard ring structure is introduced to minimize the surface leakage, as shown in Figure 5(b): by connecting both the Schottky contact and guard ring to the same reverse bias supply, there will be no potential drop between them and thus no surface leakage. Instead, the leakage current will be formed between the guard ring and Ohmic contact that will not affect the signal circuit loop [30].

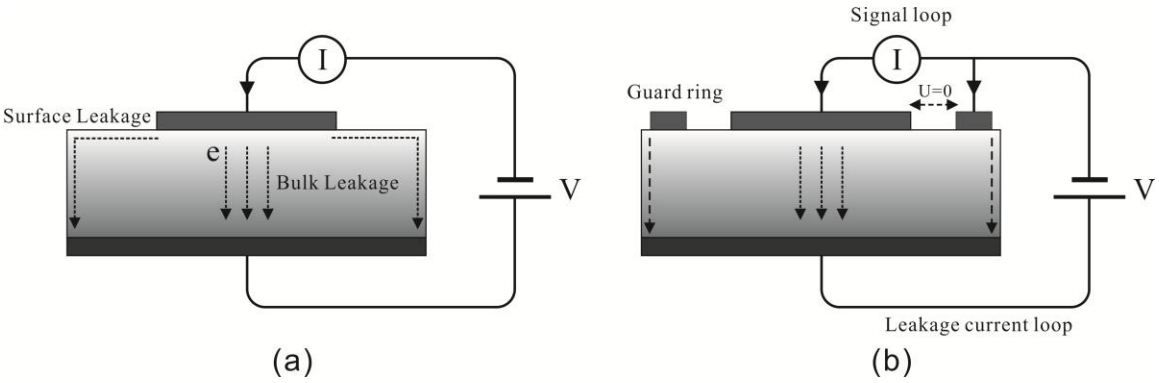


Figure 5. Leakage current (a) and guard ring structure (b)

2.8 Break Down

Under normal reverse bias, a reverse saturation current passes through the Schottky diode due to the few thermally generated minority carriers. If the voltage is high enough, then these carriers may pick up enough energy to create e-h pairs within the semiconductor material. And if the generated e-h pairs have enough kinetic energy, an avalanche multiplication process occurs, which results in a large dark current and the device is said to have broken down (see Figure 6) [31].

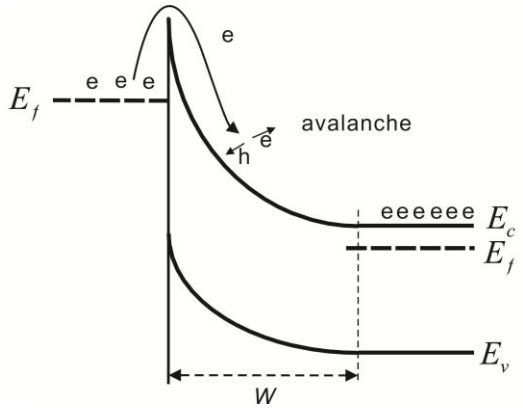


Figure 6. Break down of Schottky contact

2.9 Super-lattice Structure

Most semiconductor materials have very small neutron absorption cross sections, and thus neutron convertors are added into the detector for the purpose of making it neutron sensitive. There are three ways to add the convertors shown in Figure 7: ***coating, doping and super-lattice growing.*** Coating a convertor layer on top of the detector is one of the most widely employed methods, but the device may have a small CCE because half of the charge particles will escape from the top side of the device. Doping, either by diffusion or ion implantation, generates a significant amount of defects in the active region, which will degrade the performance of the detector. Super-lattice (SL) growing means the convertor and the semiconductor material are grown layer by layer to form the active region. This structure overcomes the drawbacks that existed in the former two methods. However, it needs advanced growing techniques and precise control conditions [32].

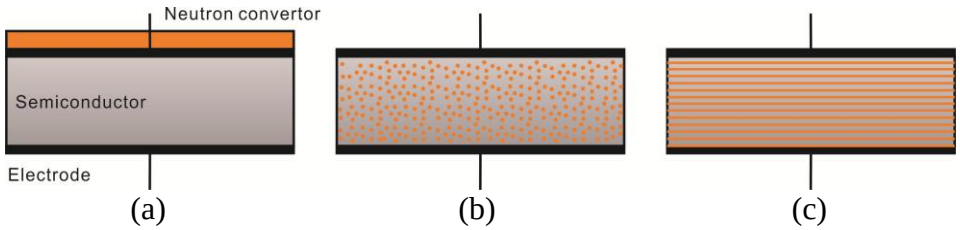


Figure 7. Adding of neutron convertors: (a) Thin-film coated device, (b) Doped device, (c) Super-lattice growing device

The super-lattice Gd:GaN material is intentionally used for semiconductor spintronics study by Prof. Myers' group. In this work, super-lattice structure is realized by growing sequences of several monolayers GdN and 10 nm GaN. Gadolinium is chosen

because it has the largest thermal neutron absorption cross section among all the stable isotopes, i.e., 254,000 barns. Gd neutron capture can result in a number of gamma-rays and moderate-energy electrons at energies of 79 and 182 keV, which can be used for e-h pairs generation [33]. Compared to undoped GaN wafer, the Gd doped GaN will increase the wafer's free electron concentration [16], which will then degrade the performance of the detector.

3. Properties of GaN

3.1 Wide Band Gap

For semiconductor detectors, room temperature operations can only be achieved for band gaps above 1.4 eV. Thus, the wide band gap (WBG) semiconductors are defined as having a band gap higher than 1.4 eV. WBG semiconductor can largely reduce the generated thermal electrons, which make it applicable for high temperature applications. Figure 8 compares the band gap for different semiconductors [34]. GaN is a wide band gap semiconductor because it has direct band gap in the ultraviolet (UV) region with an energy of E_g = 3.42 eV [1]. AlN has the widest band-gap (6.2 eV) but with very low electron and hole motilities; SiC has almost the same electric properties as GaN but has a lower critical field than GaN.

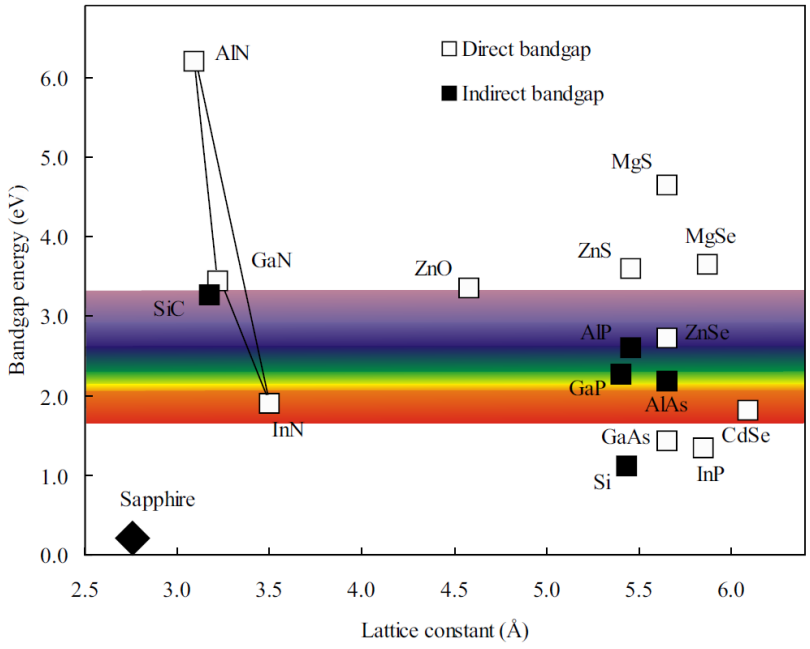


Figure 8. Band gap energy for various semiconductors [34]

3.2 Structure of GaN

GaN belongs to Group III–V compounds, which combine an anion (N) and a cation (Ga). In GaN, each atom has a fully filled valence band; however, the bonding is not entirely covalent because the shift of valence charge from N atom to Ga atom induces a weak ionic bonding. The stable bulk GaN often exhibits a wurtzite (WZ) structure and can be cut in various orientations or "planes". WZ structure belongs to C_{6v} space group, which has a stacking sequence of close-packed (111) planes of ABAB…. Three planes exist in GaN crystal, as shown in Figure 9: ***c-plane is a polar plane; m-plane and a-plane are nonpolar planes***. Nonpolar GaN technology can overcome some of the fundamental limitations of conventional c-plane GaN. Nonpolar GaN offers the potential

for increased electrical efficiency, reduced electrical resistance, elimination of color shifting with varying operating current, and reduced device sizes [35].

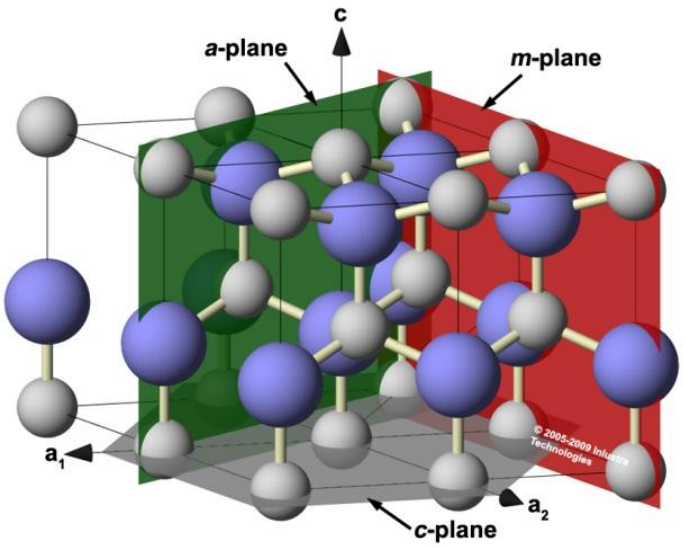


Figure 9. WZ structure of GaN and its planes [35]

3.3 Growth of GaN

GaN wafers can be grown by several nonmolten techniques, e.g., ***molecular-beam epitaxy (MBE), Metalorganic Chemical Vapor Deposition (MOCVD), and halide vapor-phase epitaxy (HVPE).*** Each of these methods is suited for a particular application. Epitaxy implies the arrangement of atoms on an ordered substrate, and thus a foreign substrate usually participates in the growing process. For growth rate and purity, HVPE can give the highest growth rate, but the carrier concentration is usually high (~10^{19} cm^{-3}); MOCVD can produce the purist wafer, but with a slow growth rate; the growth rate of MBE is between the two in which the beam fluxes and the growth condition can be precisely controlled [36].

Typically, semiconductors are manufactured on native substrates that have identical crystalline structure. Due to the lack of GaN substrates, however, GaN thin-film is usually grown on a nonnative substrate such as silicon, sapphire (Al_2O_3), and aluminum nitride (AlN), which produces a large number of threading dislocations and other defects caused by the lattice mismatch between GaN and the nonnative substrate. In order to minimize the lattice mismatch and thus prevent the degradation of detector stability and performance, a thin GaN buffer layer is usually grown between the epitaxial layer and the foreign substrate, as shown in Figure 10.

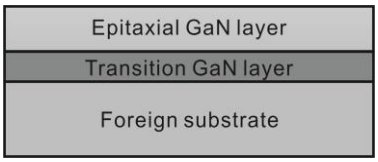


Figure 10. Growth of GaN on a foreign substrate

3.4 Types of GaN

Different growth methods produce different types of GaN, which can be cataloged into ***unintentionally doped (UD), semi-insulating (SI) and highly doped (HD) GaN***. Typically, the UD GaN has a background carrier concentration of 10^{16} electrons/cm^3 [37], caused either by oxygen impurities [38] or nitrogen vacancies [39]. This value is a little higher for device application because of the bulk leakage current under a large bias voltage. To mitigate the relatively high-intrinsic concentration of free carriers in UD GaN, a number of impurities, especially iron, are selected to compensate the shallow donors, and a semi-insulating GaN is thus obtained [19]. Both as-grown and ion implantation can

be used to dope Fe atoms and high temperature annealing is needed for donor activation. However, the introduction of these impurities forms deep level trapping centers that will largely decease the charge collection efficiency of the detector [20]. Contrary to SI GaN, highly doped GaN uses silicon to increase the carrier concentration in order to form Ohmic contact. Si is chosen because, firstly, it forms a relatively shallow donor level, and thus allows for almost complete donor activation at room temperature [37]; secondly, the solubility of Si in GaN is high, in the order of 10^{20} cm^{-3} [40]; thirdly, there is almost no dopant redistribution after high temperature activation [41]. The properties of these three types of GaN are summarized in Table 2.

Property	UD GaN	SI GaN	HD GaN
Carrier concentration (electrons/cm^3)	~10^{16}	10^{13}-10^{15}	≥10^{18}
Defect	Low	Low-High	High

Table 2. Comparison of different types GaN

3.5 Defects in GaN

During the growth of GaN, several kinds of defects invariably arise inside or on top of the wafer, including: ***particles, scratches, point defects, micropipes, dislocations, pits, etc***. Among these defects, foreign particles that stick on the surface, such as organic residuals, can be cleaned by organic solutions in ultrasonic bath. Scratches can be avoided by careful fabrication process. Neither of the two defects will largely degrade the performance of the device. Point defects like O impurities, N vacancies, Si dopant and Fe dopants will alter the electrical properties of the device by changing its carrier concentration. Dislocations, including misfit and threading dislocations, are generated by

lattice mismatch and will form trapping or recombination centers. The dislocation density must be controlled under 10^{-6} cm^2 in favor of radiation detections. These defects are inherently embedded in the GaN wafer, which significantly affects the device behavior, and especially the dislocations, which may cause the early breakdown of the device whose area contains such a defect [2]. Micropipes penetrate the whole wafer that forms current paths whose locations must be examined by optical microscopy. Pits can be directly seen by naked eyes which also penetrate the whole wafer. These two defects have a detrimental effect on the formation of a Schottky contact, and should thus be avoided in any case.

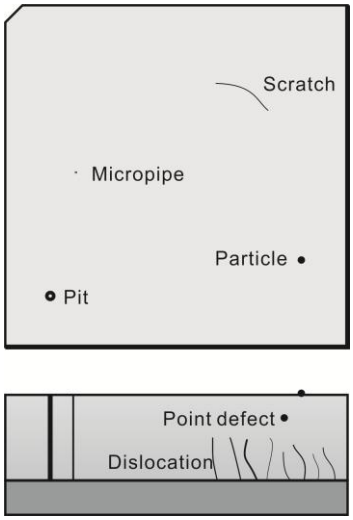


Figure 11. Defects in GaN

3.6 Comparison of GaN With Other Semiconductors

Table 3 summarizes the material properties of several narrow band-gap and wide-band semiconductors [1, 42, 43], from which we can see that GaN and SiC have very

similar properties, such as wide band gap, high melting point and high critical field. Note that most of these values are given in an ideal condition. In reality, some parameters suffering degradation, for instance, the electron and hole motilities, are largely affected by the defects in the material.

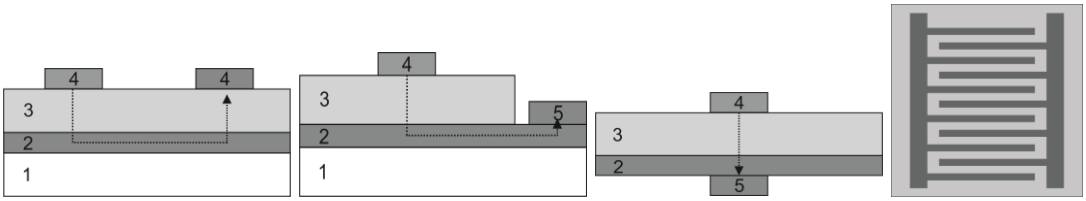
Materials Property	GaN	4H-SiC	AsGa	Si	Ge
Crystal structure	Wurtzite	Wurtzite	Zinc Blend	Diamond	Diamond
Lattice constant (Å)	3.19	3.08	5.65	5.43	5.65
Density (g/cm^3)	6.15	3.21	5.32	2.33	5.33
Average atomic number	19	10	31.5	14	32
Band gap (eV)	3.4	3.26	1.43	1.12	0.67
e-h pair creation energy (eV)	8.9	8.4	4.35	3.62	2.96
Electron mobility ($cm^2V^{-1}s$)	2000	900	9200	1450	3900
Hole mobility ($cm^2V^{-1}s$)	30	115	320	1900	1800
Melting point (^0C)	2500	2827	1240	1412	958
Dielectric constant	5.35	9.7	12.9	11.7	16.2
Critical field (10^6 V/cm)	3.5	3	0.4	0.3	0.1
Electron saturation velocity (10^6 cm/s)	25	22	400	10	1900
Thermal conductivity (W/cm ^0C)	1.3	5	0.55	1.5	0.58
Coefficient of thermal expansion (10^{-6}/C)	3.17	3.7	5.73	2.6	5.9

Table 3. Comparison of wide band-gap and narrow band-gap semiconductors

3.7 Possible Detector Structures

Based on the investigation of several semiconductor detectors fabricated on GaN [5], SiC [44], AsGa [45], and diamond [46], four kinds of structures are proposed for GaN Schottky diode detector in this study, as listed in Figure 12. For the double-Schottky contact structure, the electric field is perpendicular to the wafer surface and connects each Schottky contact with the buried high carrier concentration layer GaN [47]. For the mesa structure, etching process is employed to reach the buried layer in order to form Ohmic

contact. Sandwich structure can be fabricated on freestanding GaN wafer, which has two advantages: low dislocation density and simple fabrication process. During fabrications, the Schottky contact is grown on Ga-side, while the backside Ohmic contact should be produced on N-side [48]. In coplanar structure, both contacts are deposited on the front side and the pitch ranges from several to hundreds of micrometers. For both the sandwich and coplanar structures, two contacts can be Ohmic (photoconductive operation), Schottky (photovoltaic operation), and Schottky-Ohmic [49]. In this study, the mesa structure and the sandwich structure are applied.



(a) (b) (c) (d)

Figure 12. Possible detector structures based on Schottky diode: (a) Double-Schottky; (b) Mesa; (c) Sandwich; (d) coplanar; 1-Substrate, 2-high carrier concentration GaN, 3-Low carrier concentration GaN, 4-Schottky contact, 5-Ohmic contact

4. Device Fabrication

4.1 Wafer Dicing

Dicing occurs when the wafer that is purchased or grown is not of the desired size or shape. Based on the required accuracy, the wafer can either be sent to a company for accurate dicing or roughly cut by a simple diamond scribing pen. One company we keep contact with is Kadco Ceramics, LLC. The scribing pen, shown in Figure 13, can be purchased from Home Hardware Solutions. When using the diamond scriber to do dicing for GaN, the slicing directions should run parallel to the crystal orientations that are indicated by the wafer. Usually, one direction is easier than the other.

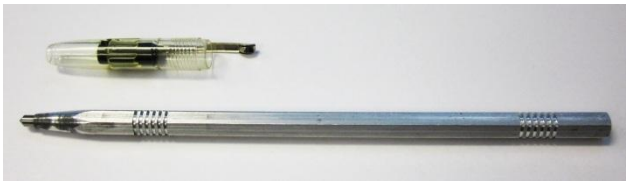


Figure 13. Diamond scribing tool

4.2 Silicon Implantation

4.2.1 Diffusion and Ion Implantation

Thermal diffusion and ion implantation are the two methods commonly used to introduce impurities into semiconductors in order to control their electric properties such as carrier concentration and resistivity. In the thermal diffusion process, a shallow high concentration dopant layer is first deposited on top of the wafer, and then a long high temperature process (900-1200 ℃) is employed to drive the dopant into the wafer. In the ion implantation process, dopant ions are first formed in an ion source and then accelerated by an accelerator to inject into the wafer. In typical applications, the dopant ions are accelerated through a potential of 10 to100 kV [50]. Figure 14 illustrates the dopant profile for the two methods, which can be approximated by Error function or Gaussian distribution. The advantages and disadvantages of the two methods are compared in Table 4 [51].

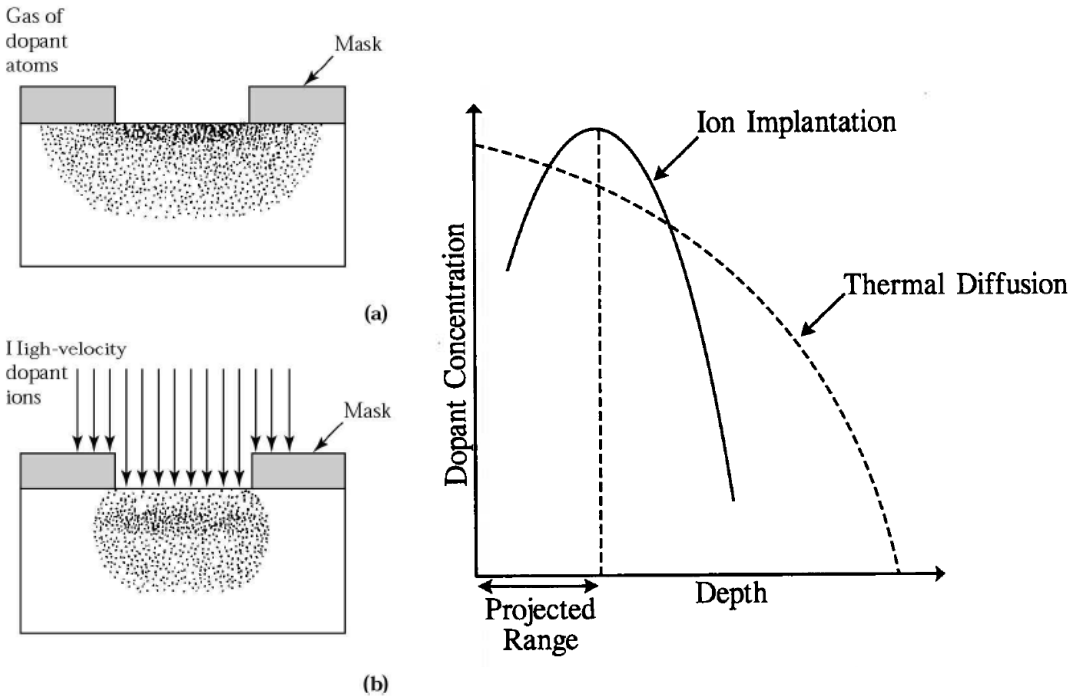


Figure 14. Doping profile of (a) thermal diffusion and (b) ion implantation [50]

Thermal diffusion	Ion implantation
Unable to achieve high dopant concentrations	Wide range of dopant dose (1 0^{11}-10^{17} atoms/cm^2)
High temperature process, needs hard mask	Low temperature process, photoresist mask
Isotropic dopant profile, large lateral dopant spread	Anisotropic dopant profile, little lateral dopant spread
Cannot independently control the dopant concentration and junction depth	Can independently control of the dopant concentration and junction depth
Long time process	Doping process is very fast
Low defect formation	Large defect formation
Most of the dopant is electrically active	Most of the dopant is electrically inactive, needs high temperature activation
No channeling effect	Channeling effect should be avoided

Table 4. Comparison of ion implantation and diffusion

4.2.2 Si Implantation and Activation

In this research, ion implantation is used to dope Si into the back side of the free standing semi-insulating GaN in order to form Ohmic contact. Si dopant is used due to its shallow donor property, high solubility (~10^{20} cm^{-3}), and minimum dopant redistribution after high temperature annealing. The doping process is carried out by Leonard Kroko, Inc. and the doping conditions are listed in Table 5.

Dopant	Si
Energy	50 keV
Dose	1×10^{16} /cm^2
Temperature	Room temperature
Doping side	Back side with scratches at the corner
Angle of incidence	7 degree to the normal of the surface

Table 5. Si implantation conditions

Figure 15 shows the simulation result of Si dopant profile in GaN, from which we calculated the project range to be about 40 nm, with a peak dopant concentration of 2×10^{21} cm^{-3} when the dose employed is 10^{16} cm^{-2}.

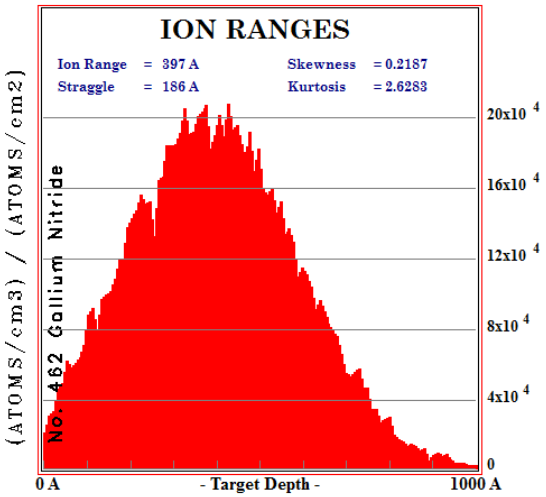


Figure 15. SRIM simulation of 50 keV Si dopant profile in GaN

The implanted Si dopants are not electrically activated immediately after the implantation, and a high temperature annealing process is thus employed to drive these dopants into the lattice site. The activation rates at different temperatures found by Y. Irokawa [52] are shown in Figure 16. From this we can see that a rate of 25 % can be achieved at an annealing temperature of 1150 ^{0}C for 1 minute.

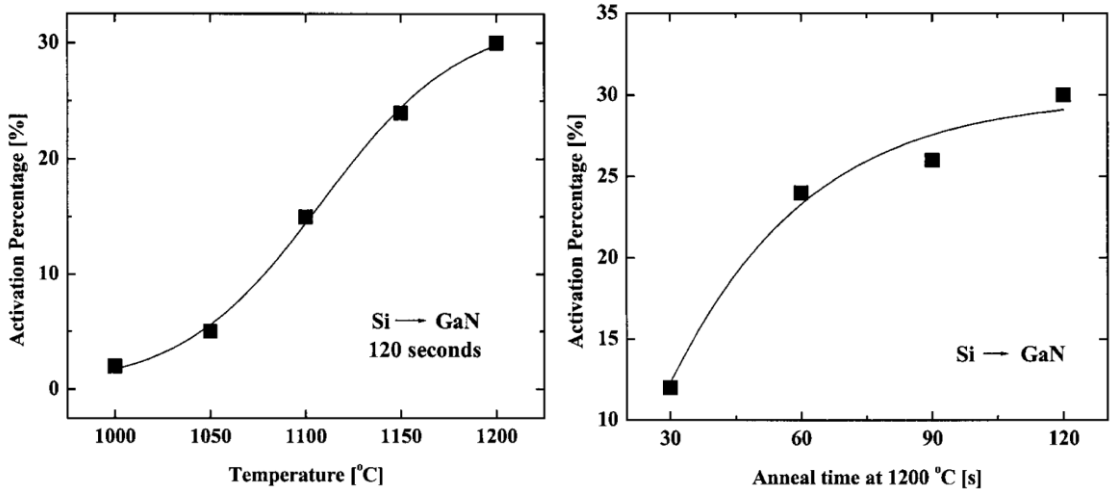
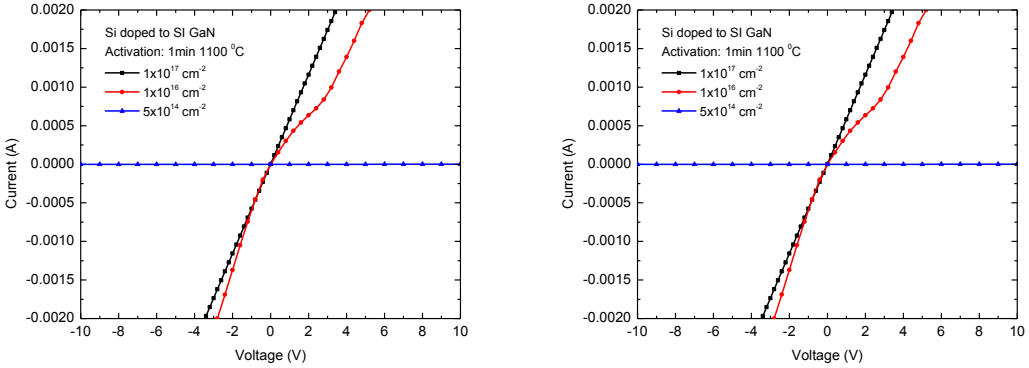


Figure 16. Si activation percentage in GaN as a function of (a) annealing temperature or (b) anneal time at 1200 °C [52]

4.2.3 Ohmic Contact Formed by Si Implantation

In order to form a good Ohimc contact for our semi-insulating GaN, three doses are used for the purpose of finding an optimum value: 5×10^{14}, 1×10^{16} and 1×10^{17} cm^{-2}. The current-voltage characteristics of two metal contacts (2 mm diameter with 2 mm distance) on the activated sample are shown in Figure 17. From Figure 17(a) we can see that doses of 10^{16} and 10^{17} cm^{-3} give nearly the same results. The reason that the activation rate satuatued at around 10^{16} cm^{-3} is probably because the maximum solubility of Si in GaN is reached. Figure 17(b) shows that, ***first, higher annealing temperature gives higher activation rate; second, increased activation time does not increase activation rate***. These results are consistent with the conclusions from Y. Irokawa. Based on these findings, we modified our ion implantation and activation recipe to be: 50 keV 1×10^{16} cm^{-2} Si ions implanted to GaN followed by a 30 second 1150 ^{0}C high temperature annealing. Note that the highest temperature for the rapid thermal annealing tool is 1200 ^{0}C.



(a) (b)

Figure 17. Si activation of Semi-insulating GaN: (a) different doses; (b) different temperatures

4.3 Photolithography

4.3.1 Basic Theory

Generally speaking, lithography is a process used to transfer a pattern from a mask onto the surface of a semiconductor via a radiation sensitive polymer. For photolithography, ultra-violet (UV) light is used as the radiation source, photomask is used to define the transferred pattern, and photoresist acts as the UV sensitive polymer. The steps involved in the photolithographic process are [53]: ***wafer cleaning, photoresist coating, soft-baking, mask alignment and exposure, development and hard baking,*** which will be discussed briefly in the following sections. The tool we used for photolithography is EV Group 620 Advanced Contact Aligner located in OSU NTW Lab.

4.3.2 Wafer Cleaning

Before coating with photoresist, the water should first be chemically cleaned to remove the foreign particles that adhere onto the surface. The steps involved to clean the GaN wafer are:

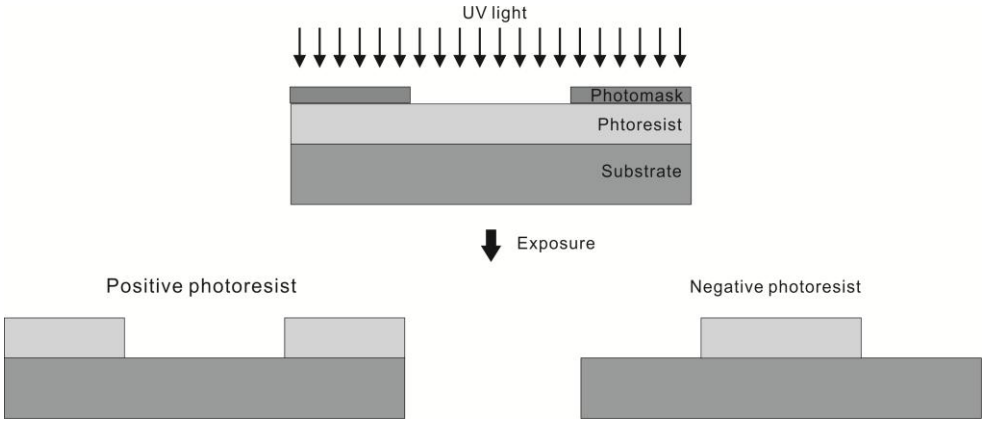
1) Ultrasonic bath in Acetone for 2 min;
2) Ultrasonic bath in IPA (Isopropanol) for 2 min;
3) Rinse with HF: DI (Deionized Water) dip (1:10) for 30 second;
4) Rinse in DI water for 1 min;
5) Dry the wafer by blow N_2 gas.

The purpose of steps 1 and 2 is to remove the organic residuals; step 3 is to remove the oxide layer of GaN; step 4 is to clean the acid residual; nitrogen gas is used in

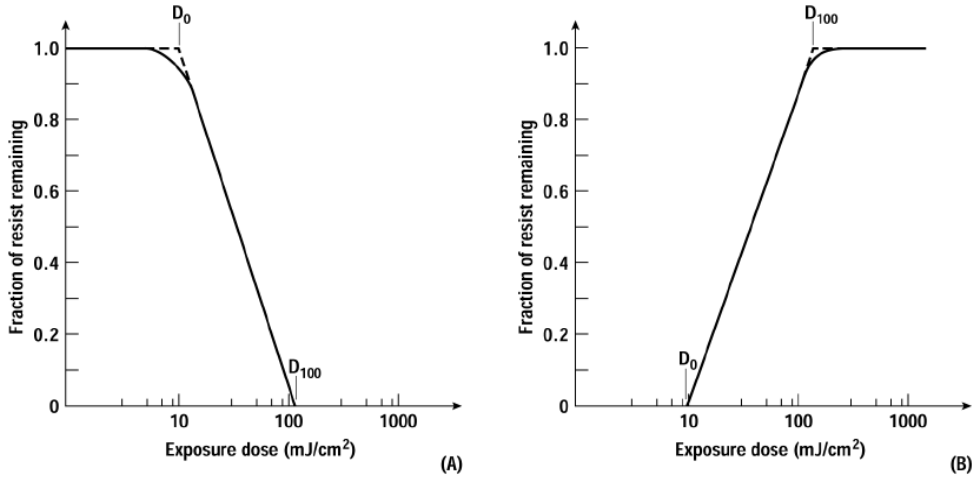
step 5 because of its inertia property. HCl:DI (1:10) dip can also be used to remove oxide layer. Here HF:DI dip is used because it is directly provided by the lab. Note that if the oxide layer is not removed, a phenomenon named zero shift will be observed when measuring the I-V characteristic, i.e., an electric current continues even when the applied voltage is zero. Also note that if the concentration of the acid is too high, then Ohmic and Schottky contacts may be stripped off, especially in the case of Ohmic contact on Si implanted side.

4.3.3 Photoresist

Positive photoresist is used throughout this research since it can achieve better resolution than negative photoresist, which suffers from a swelling problem. In positive photoresist, the region exposed to UV light will be dissolved in the developer. Three components exist in the resist: ***a base material (resin), a photoactive compound (PAC), and a solvent***. The solvent controls the mechanical properties like the viscosity that keep the resist in a liquid state. The PAC changes the dissolution rate on receiving UV light. Figure 18(a) shows the outcome of both the positive and negative photoresists after exposure and development. Figure 18(b) shows the contrast curve for the two resists, which are referred to calculate the exposure time [53].



(a)



(b)

Figure 18. Positive and negative photoresist: (a) profile after exposure and development; (b) contrast curve for (a) positive resist and (b) negative resist [53]

After dropping the liquid photoresist onto the wafer with a pipette, a spin coater (COT03-Cost Effective Equipment 100CB Spin Coater) is used to distribute the resist uniformly on top of the wafer (see Figure 19). For a photoresist with certain viscosity, different spin speed results in different final resist thickness. Two types of photoresists are employed in our experiment: LOR5A and Shipely 1813, the final thickness of which are 200 nm and 1.4 μm respectively, resulting from the spin coat cycle shown below. The

purpose of using two kinds of photoresist is to facilitate the metal strip-off process, as will be discussed later.

1) Spin Coat program for LOR5A (program 9);
2) 2 s spread at 300RPM, ramp at 500 rpm (verify before coating);
3) 3 s spread at 500 rpm, ramp at 500 rpm;
4) 45 s spin at 3000 rpm, ramp at 10,000 rpm;
5) Spin coat program for S1813 (Program 4);
6) 4s spread at 300 rpm, ramp at 100 rpm (verify before coating);
7) 60 s spread at 3000 rpm, ramp at 5000 rpm.

Figure 19. Coating wafer with photoresist

4.3.4 Soft-Baking

Immediately after resist coating, a soft baking process (also named prebake) is involved to evaporate the coating solvent and thus densify the resist. The efficiency of soft backing is temperature related: for positive resist, over soft-baking will degrade the photosensitivity of the resist and thus the development rate by destroying a portion of the PAC; under soft-backing will increase the development rate by preventing light from reaching the PAC during the exposure process.

In this research,, a faster and more controllable hot plate (Super Nuova "purple" hotplate) is used to bake the wafer. After coating with LOR5A, a 5-minute hot bake at temperature of 180 ^{0}C is employed (note that the actual setting of 190 ^{0}C will give the desired surface temperature). After coating with S1813, 1 minute hot bake at 115 ^{0}C is employed inside the COT03 hotplate oven.

4.3.5 Photomask

After soft baking, the wafer is ready for exposure, during which photomask is used to define the feature that is designed to show on the wafer. Generally, the photomask is made of 4 inch rectangular quartz coated with chrome. Quartz has low thermo-expansion coefficient and transparency in the shorter wavelengths, and chrome can stop the penetration of light and thus define the unexposed area [54].

In this research, L-Edit software is used to design the photomask, which is a layout tool that represents the masks that are used to fabricate an integrated circuit. In L-Edit, the basic concepts are layers and cells. Different layers are represented by different colors, and each layer contains many kinds of patterns named cells. Figure 20 shows the designed photomask. In reality, other kinds of masks can also be used to define the patterns, such as aluminum mask and printed transparency because of their cheapness. However, their resolution is worse and cannot be used to define small features in the order of micrometer.

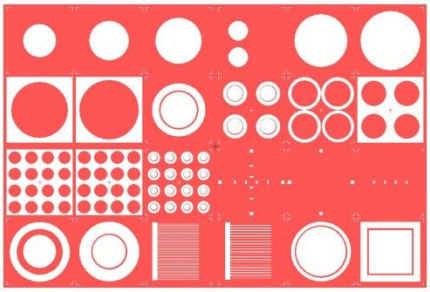


Figure 20. Photomask designed by L-Edit 7.12 student version

4.3.6 Alignment

Alignment is the most important step during the whole photolithography process, which is why the tool is more commonly called the "Aligner". The purpose of this process is to align the features on the mask and the wafer, so that the patterns can be transferred to the exact location. In reality, some markers are intentionally designed on the photomask to facilitate this process, like crosses with a dimension of several micrometers, as shown below: the dark region is the maker on the wafer, which is created in the former metal deposition step, and the light region is the marker on the mask, which is an open window in chrome through which the marker on the wafer can be seen. In reality, the two markers can be the same size in order to reduce the complexity of the photomask.

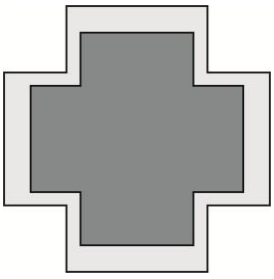


Figure 21. Markers on photomask

During the experiment, the alignment process is accomplished by a micrometer that can be used to adjust x and y positions and rotation of the photomask. Note that during the adjustment, photomask and wafer should be separated by a gap ranging from 70 to 200 nm, for the purpose of avoiding mask damage and keeping them both focused under the microscope.

4.3.7 Exposure

Once the mask and wafer have been aligned, the wafer is ready to be exposed to UV light. There are three exposure schemes shown in Figure 22: ***contact, proximity, and projection***. In the contact (also named hard contact) exposure method, the resist-coated wafer and the photomask are physically brought into contact with each other. This method offers a very high resolution but suffers mask damage. Proximity exposure reduces mask damage by keeping the mask a certain distance above the wafer, but at the same time sacrifices the resolution. The projection method uses a set of optical devices to project the image of the mask onto the wafer, and thus the size of the pattern on the mask and the actual feature on the wafer can be different. This method can avoid mask damage and maintain a high resolution, and is thus broadly used in the industry world [53].

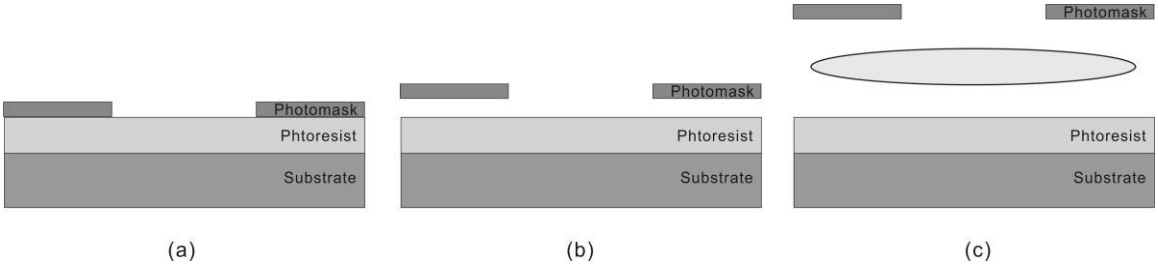


Figure 22. Exposure method: (a) contact; (b) proximity; (c) projection

In this research, the hard contact method is used provided by the EV 620 Aligner (ALN02) located in OSU NTW lab. The UV light is i-line (365 nm) with intensity of 15 mW/cm^2, and the exposure time is 2.4 seconds.

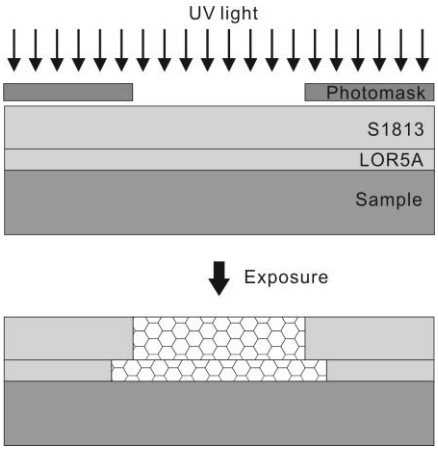
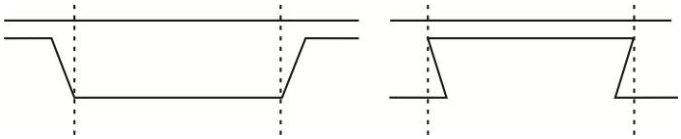


Figure 23. Exposure process

4.3.8 Development

Once exposed, the photoresist will then be developed in order to proceed in the following steps such as metal deposition or ion implantation. Development is also one of the most critical steps in the photolithographic process, which determines to a large extent the shape of the photoresist profile. Figure 24 shows the dissolution-rate image of both the positive and negative photoresist. Note that, because a finite dissolution rate exists in the unexposed area, the resist will lose its thickness while being developed, and thus at the same time develop an overcut sidewise profile [54].



(a) (b)

Figure 24.Absorptive positive (a) and negative (b) resists images

In our experiment, MF-319 is used as the developer. The developing time is about 2 minutes but should be flexible in different experiments because the rate is affected by all the former resist processing steps. In order to ensure that the exposed region has been fully developed, an inspection process should be involved by using the Nikon IC-66 Optical Microscope (INS05) or any other powerful microscope. Redevelop may be needed until the developed region is absent of photoresist. Note that the yellow filter in INS05 can avoid exposing photoresist by its light during inspection. Because the bilayer photoresist scheme is used in our case, and LOR5A is more sensitive than S1813 under UV light, a sidewise profile can be constructed after development, as shown in Figure 25.

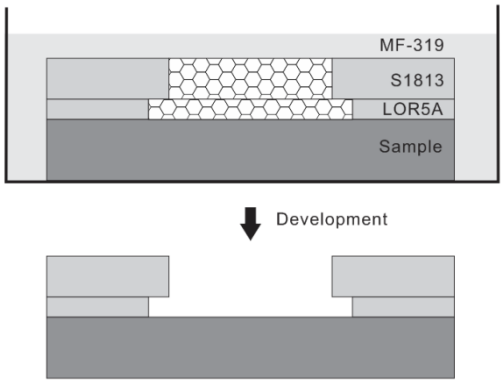


Figure 25. Development of photoersist

4.3.9 Hard-Baking

Hard-baking is also named post-baking, which is the final step in the photolithographic process. The purpose of this step is to improve the adhesion of the resist to the wafer and to harden it. The baking temperature should be carefully controlled because higher temperatures will cause desensitization or even reflow of the photoresist. In our experiment, if the following step is metal deposition, then hard-baking process is not needed; if the next step is dry etching, then 5 minutes hard-baking at 115 ^{0}C is employed to harden the resist.

4.4 Asher

After development, a few nanometers photoresist (approximately) remains on top of the developed region. The thin layer of resist can lower the barrier height when Schottky contact is formed, and it must thus be removed before metal deposition.

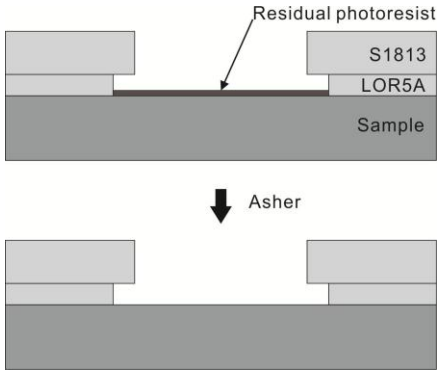


Figure 26. Asher process to clean the residual photoresist

In our experiment, Barrel Reactors are used to remove the photoresist by applying oxygen plasma. Oxygen plasma is chosen because it has a large efficiency and no chemical waste problems. The parameters of the reactor are set at:

Temperature: Room temperature
RF Power: 150 watts
O_2 Flow: 700 sccm
Pressure: 4500 mTorr
Time: 15 second

Note that an inspection process using microscope is also needed to make sure the total removal of the resist.

4.5 Etching

4.5.1 Dry Etching vs. Wet Etching

Etching is used to reach a certain depth of the wafer. Etching methods can generally be divided into two groups: ***wet etching*** (also known as chemical etching) and ***dry etching*** (also known as physical etching). In wet etching, the wafer is immersed in a solution that reacts with the exposed film to form soluble byproducts. It is a purely chemical process that can be highly selective and thus does not damage the substrate. However, it has serious drawbacks, including lack of anisotropy, poor process control, excessive particle contamination, and the production of large volumes of chemical waste. Thus, wet etching can only be used for noncritical tasks for large features [55]. Dry etching is synonymous with plasma assistant etching, which denotes several techniques that use plasma to remove the material from the wafer either by physical sputtering,

radical chemical reactions, or both. It overcomes most the former drawbacks but with a low etching rate. Figure 27 compares the layer profiles generated by wet and dry etching.

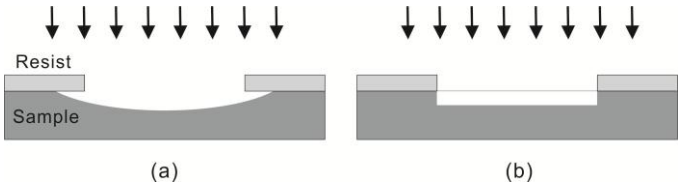


Figure 27. Comparison of wet etching and dry etching

4.5.2 ICP-RIE System

In this research, Plasma Therm 770 SLR ICP-RIE (ETC04) system is chosen to do dry etching for our GaN wafer diagramed in Figure 28. The operation mechanism of the reactive ion etching (RIE) system involves both ion bombardment and chemical reaction: a radio frequency (RF) voltage is applied between the cathode where holding the sample and the upper anode. The inlet gas will be ionized by the RF power and form a plasma. At the same time, due to the vast difference in mobility between ions and electrons – that is, electrons can drift to the electrode but ions still remain in their former location – a static direct current (DC) potential develops between the electrode and the plasma, and ions can thus be accelerated to bombard the wafer on top of the electrode. In RIC system, high RF power generates high DC bias and thus high ion energy [42].

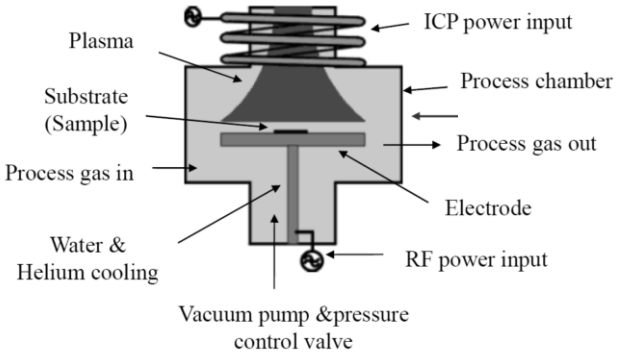


Figure 28. ICP-RIE system [42]

In order to increase the plasma density and thus increase the etching rate, an inductively coupled plasma (ICP) system is added to the RIE system. In this setup, plasmas are formed in a dielectric vessel encircled by an inductive coil into which anther RF power is applied. When a time-varying electric current is passed through the coil, it creates a high time-varying magnetic field in the chamber, which leads to gas breakdown and the formation of a plasma. The neutrality of the ICP plasma allows a large RF power to be applied, creating a much denser plasma. The ions in the dense plasma can be accelerated to the sample by the RIE RF source. In ICP-RIE system, ion energy and plasma density are decoupled, and uniform density and energy distributions are transferred to the sample while keeping the ion energy low, and thus implantation will not occur. The relatively high etching rate of ICP-RIE system is particular useful for GaN.

4.5.3 Etching of GaN

The etching process generates a mesa structure as shown in Figure 29. The etching recipe for GaN is: 20 ccm Cl2, 5 sccm Ar, 40 W RIE, No ICP, Pressure 5 mTorr,

and Helium backside cooling. Before the mesa etching step, there is a BCl_3 blast step. The use of BCl_3 is to remove any oxide on GaN. Usually, the etching rate of GaN using this recipe is 70 nm/min (with the same rate for S1813 photoresist), but different among different types of samples, and even diverse on the same sample at different locations. Take the super-lattice GaN as an example: in order to reach the buffer layer, which is about 600 nm deep, three rounds of etching process are employed, as listed in Table 6.

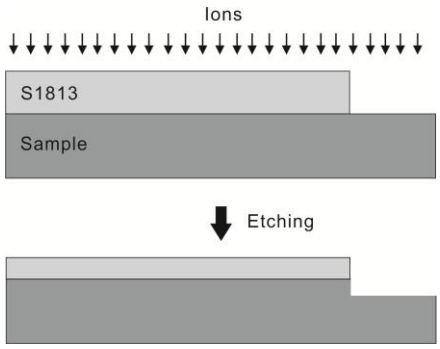


Figure 29. Etching of GaN

Etching	Etching time (min)	Etching depth measured at different locations (nm)	Etching rate (nm/min)
Round 1	6	130	22.5
		140	
Round 2	20	313	15.4
		302	
Round 3	15	200	14.5
		235	

Table 6. Etching of super-lattice GaN

The height can be measured by Sloan Dektak3 Profilometer (PRF01), and the generated height map is shown in Figure 30.

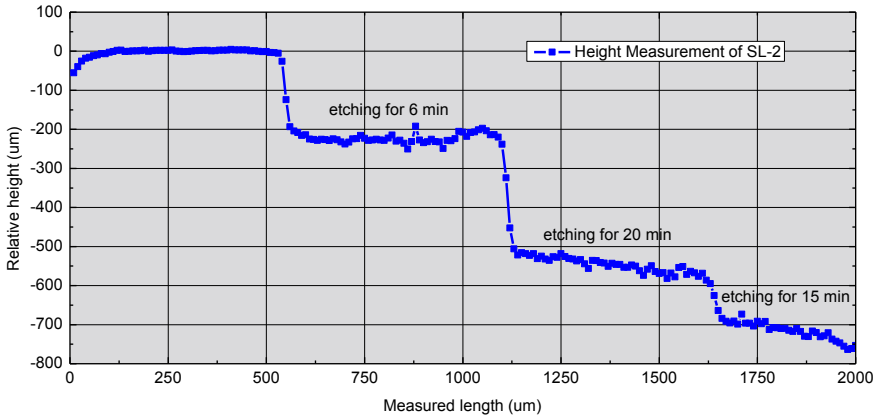


Figure 30. Height measurement after dry etching

Etching has also been performed on other samples, and their etching rates are summarized in Table 7. From this we can see that the etching rate was largely decreased by adding impurities.

GaN Sample	Etching rate
Undoped GaN	70 nm/min
Ammono semi-insulating GaN doped with 50 keV 1×10^{14} cm^{-2} Si	27 nm/min
Ammono semi-insulating GaN doped with 50 keV 1×10^{16} cm^{-2} Si	18 nm/min
Super-lattice GaN with period of 10 nm GaN/2.4 ML GdN	17 nm/min

Table 7. Etching rate for different types of GaN

4.6 Metal Deposition

4.6.1 Methods of Metal Deposition

Metal deposition is used to make Ohmic and Schoottky contact on GaN. Three kinds of deposition methods are available, namely: ***Filament Evaporation, Sputtering, and E-Beam Evaporation***. In the filament evaporation method, metal pellets are placed on the filament made of tungsten, graphite, etc. Under vacuum conditions, when the

filament is heated to the melting point of the metal, the metal will be vaporized and deposited on the sample. Deposition rates on the order of 1 nm/sec are standard in this method. In the sputtering method, gas plasma is first formed and then ions in it will be accelerated to bombard the source material. The gas must be inert in order not to react with the sample, and the energy must be low in order to avoid sputtering off the sample atoms. Sputtering method works well for materials with high melting points such as carbon, silicon and alloys. In the electron-beam evaporation method, thermal emission of electrons from a filament source (usually tungsten) are used to heat metals to their melting point. Because no foreign ion directly faces the sample during the evaporation process, this method can give the highest purity. Table 8 summarizes the pros and cons of different deposition methods [56].

Method	Pros	Cons
E-Beam Evaporation	• high temperature materials • good for liftoff • highest purity	• some CMOS processes sensitive to radiation • alloys difficult • poor step coverage
Filament Evaporation	• simple to implement • good for liftoff	• limited source material (no high temperature) • alloys difficult • poor step coverage
Sputter Deposition	• better step coverage • alloys • high temperature materials • less radiation damage	• possible grainy films • porous films • plasma damage/contamination

Table 8. Summary of Pros and Cons for different deposition methods [55]

4.6.2 E-Beam Evaporation System

The CHA Solution System E-Gun Evaporator (EVP03) shown in Figure 31 is selected in our experiment. During operations, the system is pumped to vacuum before metal deposition. During depositions, electrons generated by electron-gun (generally tungsten filament) are steered by 270^0 before reaching the metal source by magnetic field and raster. This is done to allow shielding of tungsten filament and thus prevent contamination. Because of the bombardment of the electrons, the metals in the crucible are heated to their melting point, and the metal vapors are then deposited on the sample surface. The thickness of the deposited metal is measured by a quartz crystal monitor in real time. The deposition rate ranges from 3 to 50 Å/s depending on the metal used. Note that when electrons strike on the metals, X-rays are produced and thus any sample sensitive to X-rays must be taken care of in this process [42].

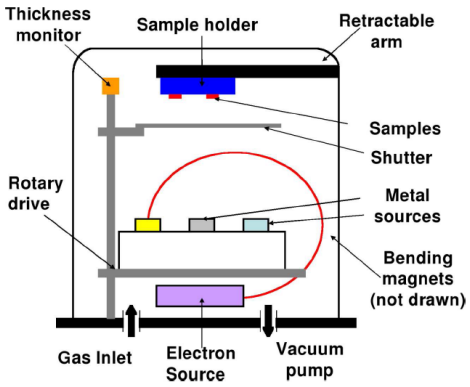


Figure 31. Schematic of an electron-beam evaporator [42]

4.6.3 Metal Deposition for GaN

Before metal deposition, the sample should be cleaned by using the wafer cleaning process. The setup parameters for Ohmic (Ti/Al/Ni/Au) and Schottky contact

(Ni/Au) deposition are listed in Table 9. Note that the metal used and parameters for Schottky contact are identical to the last two layers for Ohmic contact.

Parameters	**Ohmic contact**					**Schottky contact**	
	Layer 1	Layer 2	Layer 3	Layer 4		Layer 1	Layer 2
Material index	Ti	Al	Ni	Au		Ni	Au
Rate (Å/s)	0.5	0.5	0.5	0.5		0.5	0.5
Final thickness (kÅ)	0.1	2.0	0.2	3.0		0.2	3.0
Thickness limit (kÅ)	0.000	0.000	0.000	0.000		0.000	0.000
Time limit (MM:SS)	00:00	00:00	00:00	00:00		00:00	00:00
Rate watch time	00:00	00:00	00:00	00:00		00:00	00:00
Rate watch accuracy (%)	5	5	5	5		5	5
Crucible	2	1	3	4		3	4
Rate ramp 1							
New rate (Å/s)	0	2.5	1.0	2.5		1.0	2.5
Start ramp (kÅ)	0	0.05	0.05	0.05		0.05	0.05
Ramp time (MM:SS)	0	1:00	0:30	1:00		0:30	1:00
Rate ramp 2							
New rate (Å/s)	0	5.0	0	5.0		0	5.0
Start ramp (kÅ)	0	0.3	0	0.3		0	0.3
Ramp time (MM:SS)	0	1:00	0:00	1:00		0:00	1:00

Table 9. Parameter setup for metal deposition

In the ramp step, for example rate ramp 1 for Al, the parameters employed means that when the metal thickness reaches 0.05 kÅ, the deposition rate will ramp from 0.5 Å/s to 2.5 Å/s in 1 minute. This is clearly seen by the following plot of data in Table 9. Note that this program still needs a modification, i.e., at the end of metal deposition, another ramping rate should be added to decrease the deposition rate slowly to zero, and this can protect the equipment from a sudden change of operation conditions. Figure 32 illustrates the metal deposition process.

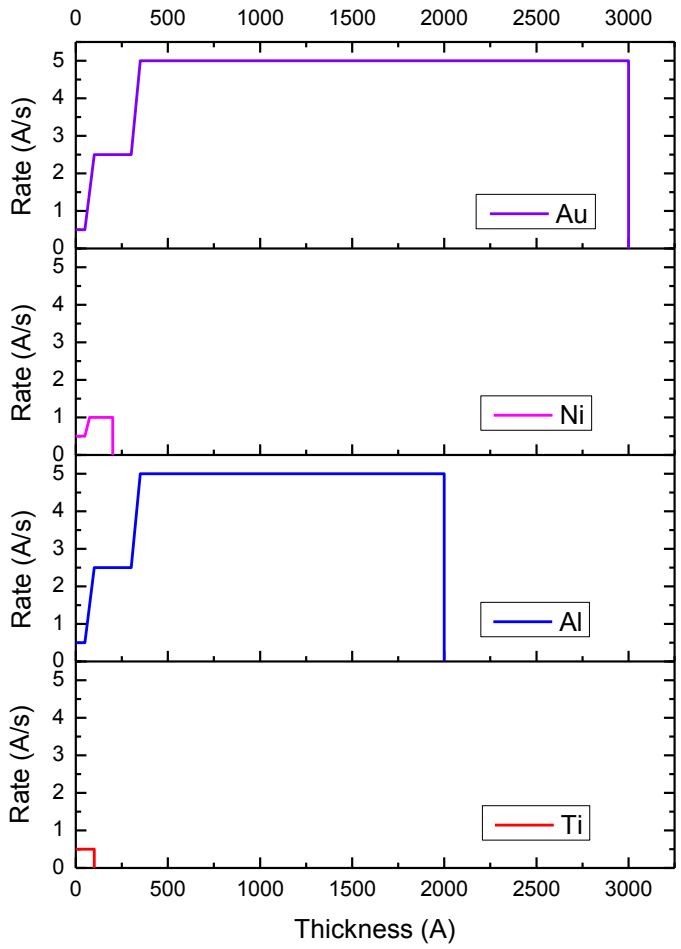


Figure 32. Deposition pattern for Ohmic and Schottky contact

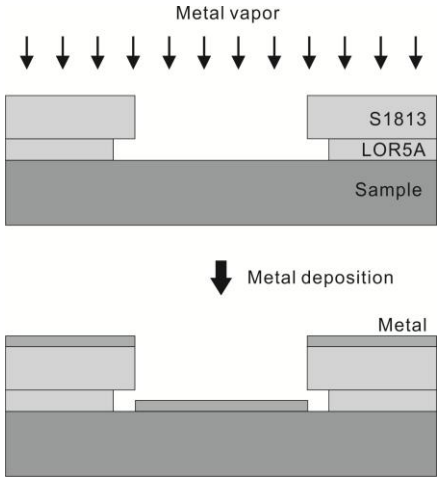


Figure 33. Metal deposition process

4.7 Lift Off

Lift off process is used to remove the undesired metal area following metal deposition. As discussed before, a bilayer resist scheme is used in order to generate a lift off friendly profile, as shown in Figure 34. The steps involved in this process are:

1) Put sample in NMP (n-methyl-2- pyrrolidinone) solution heated by hotplate at 100 ^{0}C for 5 minutes;

2) Ultrasonic bath the whole bottle for 20 to 30 seconds;

3) Ultrasonic bath the sample in IPA for 1 minute.

Note that, during the first step, an NMP squirt bottle can be used to strip off the metal.

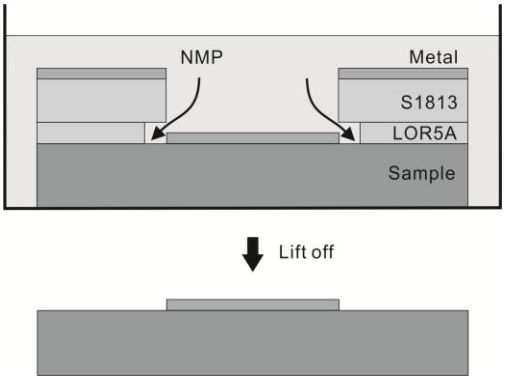


Figure 34. Metal lift off from bilayer photoresist

4.8 Rapid Thermal Annealing

4.8.1 Types of Rapid Thermal Processes

Rapid thermal processes are divided into three classes according to the type of heat that is carried out: ***adiabatic, thermal flux, and isothermal***. In adiabatic systems, a broad beam of fast light pulse is used to heat the front side of the wafer. While this method allows the shortest annealing time, it has several drawbacks, including poorly controlled temperature, poorly controlled annealing time and large vertical temperature gradient. Thermal flux systems employ an intense spot source, such as an electron beam to scan across the wafer, in which the defects caused by the lateral thermal non-uniformity are too large for IC fabrication. Isothermal systems use a broad beam of radiation generated by tungsten-halogen lamps to heat the wafer for many seconds. The wafer rests on quart pins because of its chemical stability and low thermal conductivity [55].

4.8.2 Rapid Thermal Annealing System

Unlike furnace anneals that usually take a long time, Rapid Thermal Annealing (RTA) refers to a semiconductor manufacturing process that heats wafers to high temperatures (up to 1200 ^{0}C) for a very short time (less than 1 minute). The purpose of RTA include: activate dopants, change film-to-film interfaces, densify deposited films, change states of grown films, repair damage from ion implantation, move dopants from one film to another, etc. The tool we used is AG Associates Model 410 Rapid Thermal Annealer (RTA01). This tool has two different models for monitoring the temperature: for temperature below 850 ^{0}C, thermocouple (TC) is used; for temperature above 850 ^{0}C, optical pyrometer (PR) is used. Note that the reading is inaccurate below 650 ^{0}C for PR.

4.8.3 RTA of GaN

In our experiment, the purpose of RTA is to densify the Ohmic contact, i.e., enhance its adhesion to the GaN surface, dopant activation. For densify the contact, the annealing recipe is listed in Table 10. Since the up limit of the temperature is 850 ^{0}C, thermocouple is used to monitor the temperature. For Si activation, the annealing recipe is listed in Table 11, and since the highest temperature employed is 1150 ^{0}C, pyrometer is used to monitor the temperature.

Step	Type	Time (second)	Temperature (^{0}C)
1	Delay	20	
2	Ramp	50	300
3	Steady state	10	300
4	Ramp	50	860
5	Steady state	2	860
6	Delay	300	

Table 10. RTA recipe for densify Ohmic contact

Step	Type	Time (second)	Temperature (^{0}C)
1	Delay	20	
2	Ramp	20	700
3	Steady state	10	700
4	Ramp	50	1100
5	Steady state	2	1100
6	Ramp	20	1150
7	Steady state	30	1150
8	Delay	600	

Table 11. RTA recipe for Si activation

Note that during the activation process, the sample should be put on top of another disposed sample, because if the Si side (usually back N-side) faces the pyrometer, which is made of Si wafer, the sample may stick on to the wafer; on the other hand, if the front Ga-side faces the wafer, Si atoms may diffuse into the sample to generate defects in

Ohmic behavior when the metal is deposited. Also note that the intimacy contact method (i.e., putting the two samples face to face) was not found to be useful for protecting the sample from surface decomposition. The surface decomposition may not be severe enough to destroy the formation of Schottky contact, like Ammono SI GaN; but for Kyma SI GaN, Schottky contact cannot be formed after Si activation process.

4.9 Wire Bonding

After the formation of Ohmic and Schottky contacts, wire bonding process is usually employed to connect these contacts to a sample holder and thus to outside circuit for further device characterization (see Figure 35). This process is done by Kulicke and Soffe 3123 Wire Bonder (BND03). The wires used in this tool are either 1.0 mil (one thousandth of an inch) gold or 1.0 mil aluminum. The success of wire bonding is mainly the combination of four parameters: ***force, ultrasonic power, temperature and time***. Note that the smoothness and cleanliness of the metal surface will also affect the quality of the bonding. Oxidation of the metal surface will cause the failure of wire bonding.

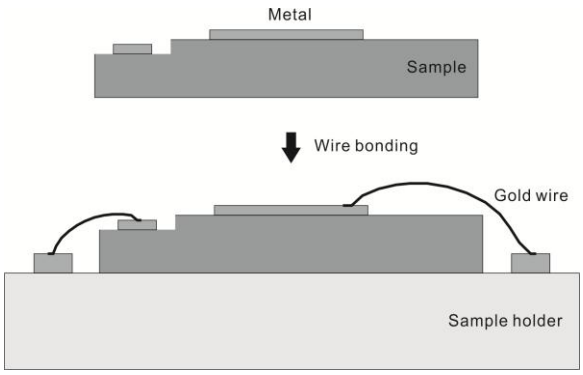


Figure 35. Wire bonding process

Gold wire is used in this research. The bonding is very successful on the Au surface on both the sample and sample holder, but has very bad quality for the Au surface deposited on the etched surface, this is because the smoothness of the sample surface has been degraded during the etching process. Au wire bonding to other metal surfaces such as Ni has not yet been successful, further adjustments of the four parameters are still needed. The setup of the parameters to perform wire bonding is listed in Table 12.

Parameters	Loop	Search	Force	Time	Power
First bonding	3.0	50	3.0	5.2	3.10
Second bonding		50	3.0	4.8	3.30

Table 12. Parameters setup for wire bonding

5. Device Characterization

5.1 Resistivity

5.1.1 Contact Resistance and Sheet Resistance

The quality of Ohmic contact is essential to the performance of semiconductor devices and is characterized by contact resistance. For wide band-gap semiconductor devices, Ohmic contact is formed between the metal and the doped layer, and thus the total resistance shown in Figure 36 between two Ohmic contacts is the sum of metal resistance, contact resistance and sheet resistance [1]:

$$R_t = 2R_m + 2R_c + R_s \quad (1)$$

In which the doping layer is characterized by sheet resistance *Rs* (Ω/sq); the interface layer is characterized by contact resistivity $\rho_c = R_c A_c$ (Ohm-cm^2), where *Rc* is the specific contact resistance (Ohm-cm), and *Ac* is the contact area.

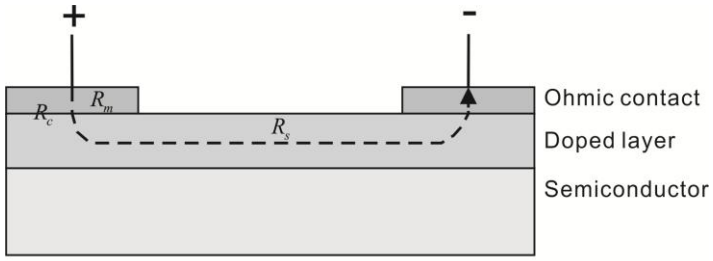


Figure 36. Typical resistance of semiconductor devices

In reality, only the semiconductor directly under the contact is heavily doped, and thus the contact resistance consists of the metal-semiconductor contact resistance and the n+n junction resistance shown in Figure 37 [1]:

$$R_c = R_{ms} + R_{n^+n} \quad (2)$$

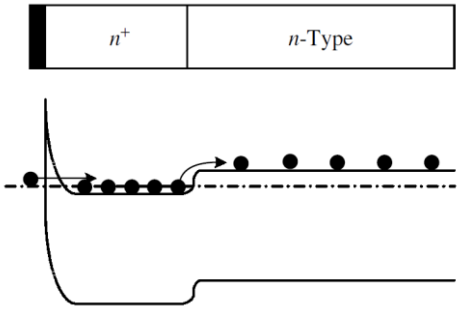


Figure 37. Metal-semiconductor contact resistance [57]

Theoretically, the contact resistance can be derived from thermionic-emission model given by

$$R_c = \frac{k}{qA^*T}\exp\left(\frac{q\phi_B}{kT}\right) \quad (3)$$

Where k is Boltzmann constant: k=1.381x10^{-23} J/K, q the electron charge: q=1.602x10^{-19} C, T the temperature in Kelvin: T=300 K, V the bias voltage, R^* the Effective Richardson Constant: R^*=24A=0.0202 cm^{-2}K^{-2} calculated by using effective electron mass $m_e^* = 0.2m_e$ [2, 3], A the detector area (cm^2), and ϕ_B the Schottky barrier height in volts.

5.1.2 Circular Transmission Line Method

In order to measure the sheet resistance of the doping layer and the contact resistivity of the Ohmic contact, two methods have been developed [4]: ***Rectangular transmission line method (RTML) and Circular transmission line method (CTLM)***. Compared with RTML, CTLM can restrict the current flow vertical to the contact edge and thus avoid the current crowding problem, and the sample can also be much larger than the deposited patterns. Therefore, only CTLM is discussed, the patterns of which are shown in Figure 38. The suggested parameters of these patterns are listed in Table 13.

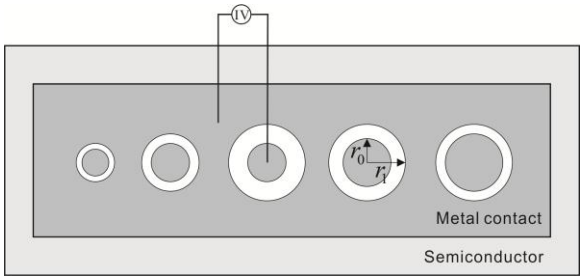


Figure 38. CTLM for resistivity measurement

The total resistance, sheet resistance, dot radius and inner radius of the circular patterns are related by the equation

$$R_t = \frac{R_s}{2\pi}\left[\ln\left(\frac{r_1}{r_0}\right) + L_T\left(\frac{1}{r_0} + \frac{1}{r_1}\right)\right] \quad (4)$$

In which, L_T is transfer length demoted by

$$L_T = \sqrt{\frac{\rho_c}{R_s}} \quad (5)$$

In order to characterize the Ohmic contact, first, the total resistance between the outer metal and the inner dots are measured, in which four-point probe method (refer to next section) is usually used to avoid inaccuracies; then, a least-squares fit of the data to equation (4) is performed, in which step the transmission length L_T and the sheet resistance R_s are extracted; finally, the contact resistivity ρ_c can be calculated by equation (5).

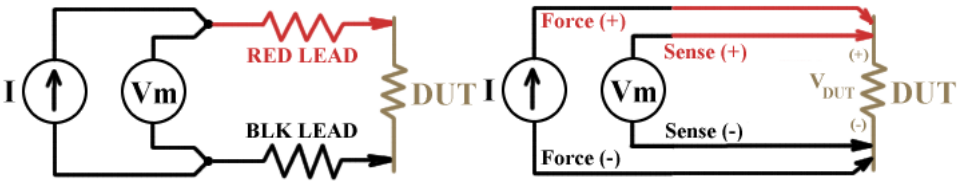
Parameters	Pattern 1	Pattern 2	Pattern 3	Pattern 4	Pattern 5
Dot radius (μm)	25	50	50	100	150
Inner radius (μm)	50	100	150	200	200

Table 13. Suggested parameters for CLTM

5.1.3 Four-point Probe Measurement

2-wire resistance measurement uses two leads to connect the device under test (DUT) (see Figure 39(a)). During the measurement, first the ohmmeter forces a current through the wire, and then the voltage developed is measured. Finally, the resistance is

calculated by dividing the voltage by current. From the setup we can see that the resistance measured actually also includes the resistance of the two leads.



(a) (b)

Figure 39. Setup of 2-wire measurement (a) and 4-wire measurement (b) [61]

4-wire measurements (also known as 4-Wire "Kelvin" Testing) overcome this problem by introducing four connections shown in Figure 39(b): two come from the current source (sometimes called the "force" leads), and two come from the voltmeter (usually called the "sense" leads). During the measurement, a current is generated by the force leads and the voltage is measured by the sense leads. Since the sense leads have a very large resistance, nearly no current passes through them and there is thus no voltage drop in them; the measured voltage drop all results from the DUT [5]. The 4-wire measurement can be performed by Keithley 2400 SourceMeter connected to the probe station.

5.2 Current-Voltage Characteristic

5.2.1 I-V Curve of a Schottky Diode

Current-Voltage (I-V) measurement is used to characterize the quality of the Schottky diode, especially the leakage current of the Schottky contact when the device is

reverse biased. Figure 40 illustrates a typical I-V curve for a Schottky diode. When the device is forward biased, three parameters used to depict the diode are:

1) Forward bias turn-on voltage V_{on}. Starts from which the device is said to be turned on and the value is usually defined when the current density reaches to 100 A/cm^2 [6];

2) Forward on-resistance R_{on}. The ratio of the voltage to the corresponding current, characterizes the linear region of the I-V curve, which is mainly the resistance of the semiconductor layer;

3) Self-heat effect current density J_h. At which the I-V curve begins to depart from linear because the density is so high that self-heating effect starts to degrade the diode transport properties. This effect usually starts to occur at a current density of 1000 A/cm^2 [6].

Under reverse bias, two important parameters are:

1) Saturation current I_0. The reverse saturation current, also named dark current, that consists of thermionic emission (diffusion), generation–recombination in the depletion region (GR) and thermionic-field emission (tunneling) current [7], which is one component of the leakage current. Theoretically, it will not change until the device suffers breakdown.

2) Breakdown voltage V_B. Breakdown happens when the reverse bias is so high that the minority carries gain enough energy to produce ionizations and finally result

in an avalanche multiplication process as discussed earlier. In reality, it can be defined when the reverse current density reaches 10 A/cm^2 [8].

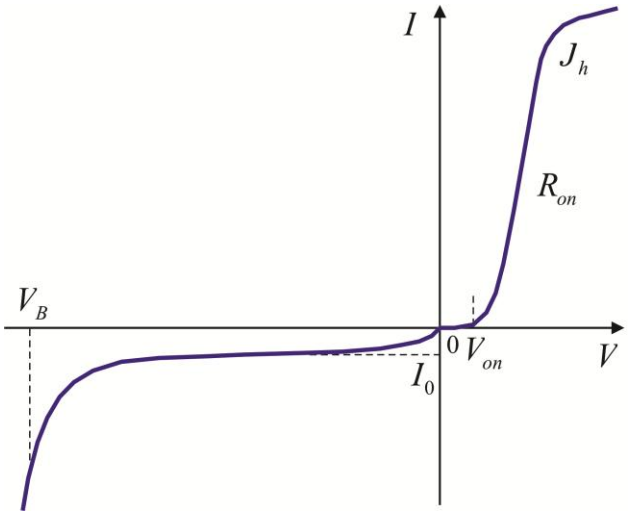


Figure 40. Typical current-voltage characteristic of a Schottky diode

The I-V characteristic of a Schottky diode can be calculated by thermionic emission mechanism [9]

$$I = I_0\left(e^{qV/nkT} - 1\right) (6)$$

In which, the reverse saturation current is given by

$$I_0 = AR^*T^2 e^{-q(\phi_B - \Delta\phi)/kT} (7)$$

And the image-force lowering of the Schottky barrier height

$$\Delta\phi = \sqrt{qE/4\pi\varepsilon_0} (8)$$

Where *n* is idea factor, which will be larger than unity when surface defects are present on the semiconductor surface, ε_0 the vacuum permittivity: ε_0 =8.85x10^{-14} F/cm; *E* the self-induced electric field that will be discussed later. For the sake of simplicity, the image-force lowering of the barrier height can be ignored, and thus, by measuring the I-V curve, the idea factor and reverse saturation current can be calculated from equation (6) and (7).

5.2.2 Schottky Barrier Height

Schottky barrier height (SBH) is the barrier seen by electrons in the metal trying to move into the semiconductor, and is ideally given by

$$\phi_B = \phi_m - \chi_s \quad (9)$$

Where ϕ_m is the metal work function given by 5.24 eV for nickel, and 4.10 eV for titanium. χ_s is the semiconductor electron affinity, which value is 4.1 eV for GaN at 300 K. Note that during calculations, their unit used is V instead of eV because the electron charge has been pulled out of the equations.

In reality, for Schottky diodes, surface states play a dominant role in determining the barrier height, which makes it essentially independent from both the work function of the metal and the electron affinity of the semiconductor. Surface states exist because of the disruption of crystal lattice at the interface and also other surface defects. The former is unavoidable; the latter should be minimized by keeping the surface as clean as possible during fabrication process [9].

5.2.3 Induced Electric Field

The induced electric field (IEF) is created inside the depletion region by the separation of positive and negative carriers. For a uniformly doped semiconductor, the IEF is given by

$$E = -\frac{qN_d}{\varepsilon_s}(W - x) \quad (10)$$

And the highest electric field for metal-semiconductor contact at their interface is thus

$$\left|E_{\max}\right| = \frac{qN_dW}{\varepsilon_s} \quad (11)$$

In which, N_d is the carrier concentration (or doping concentration if the two are equal) in unit of per cubic centimeters; ε_s is the semiconductor dielectric constant given by $\varepsilon_s = K_s\varepsilon_0$, where K_s is the relative permittivity, for GaN, K_s = 8.9; *x* is the depth into the semiconductor start form the contact interface; and *W* is the width of the space charge region in centimeters.

5.2.4 Depletion Depth

The depletion depth is calculated to be [10]

$$W = \sqrt{2\varepsilon_s(V_{bi} - V)/qN_d} \quad (12)$$

In which V_{bi} is the built-in potential barrier (V) seen by electrons in the semiconductor trying to move into the metal given by

$$V_{bi} = \phi_B - \phi_n \quad (13)$$

Note that another definition for built-in potential barrier is $V_{bi} = \phi_m - \phi_s$, which gives a larger result, since definition (13) gives $V_{bi} = \phi_B - \phi_n = \phi_m - \chi_s - \phi_n$. ϕ_n is the electrostatic potential of the n-type neutral region with respect to the Fermi level

$$\phi_n = \frac{kT}{q} \ln\left(\frac{N_c}{N_d}\right) \quad (14)$$

Where N_c is state effective density of the conduction band (cm^{-3}), for wurtzite structure GaN, $N_c = 4.3\times10^{14}\ T^{3/2}\ cm^{-3}$ [11].

5.2.5 Breakdown Voltage

The breakdown voltage of a Schottky diode is given by

$$V_B = \frac{\varepsilon_s E_c^2}{2qN_d} \quad (15)$$

In which E_c is the critical field for GaN, which value is $3.5\text{x}10^6$ V/cm in an ideal case [11].

5.3 Capacity-Voltage Characteristic

5.3.1 Principle of C-V Measurement

The purpose for Capacity-Voltage (C-V) measurement is to determine the carrier concentration of the semiconductor at different depth. Note that carrier concentration is not identical to doping concentration for two main reasons: first, they are only identical for uniform doping; second, when a portion of the dopant is not activated, the carrier concentration is less than the doping concentration [9]. C-V measurement can only be performed when both Schottky and Ohmic contact are present, because it relies on the fact that the width of the space charge region depends on the applied voltage. The principle for C-V measurement technique is shown in Figure 41 [1], in which the semiconductor is n-type with doping concentration N_d, the metal contact on the left is Schottky, and the right is Ohmic. During the measurement, a DC bias voltage is applied to the Schottky contact. This voltage produces a space charge region of width W. Then, if a small amplitude AC voltage v is superimposed on the DC voltage V, the capacity can be determined by

$$C = -\frac{dQ_s}{dV} \quad (16)$$

Where dQ_s is the charge increase of the semiconductor within a thin layer of dW.

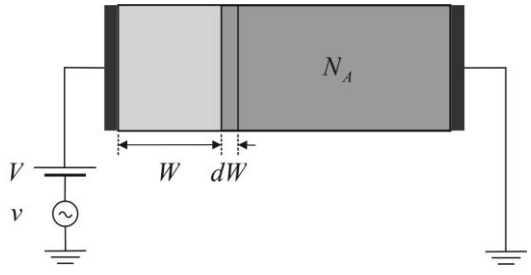


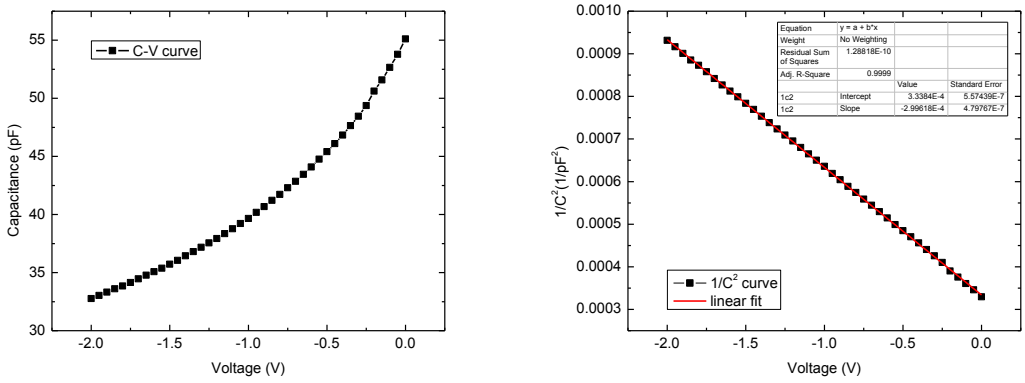
Figure 41. Mechanism of C-V measurement

5.3.2 Schottky Barrier Height

The measured capacitance at different reverse bias voltages can be recast in the form of $1/C^2$ versus V written as

$$\frac{1}{C^2} = \frac{2}{qK_s\varepsilon_0 N_d A^2}\left(V + \phi_{bi}\right) \quad (17)$$

All the notations can be found in the former sections. As an example, the C-V plot is shown in Figure 42(a) and the generated $1/C^2$ over V plot is shown in Figure 42 (b). By fitting this plot to linear, the built-in potential can be extracted, and then the Schottky barrier height can be calculated by Equation (13). This is another way to find the SBH besides the Current-Voltage method.



(a) **(b)**

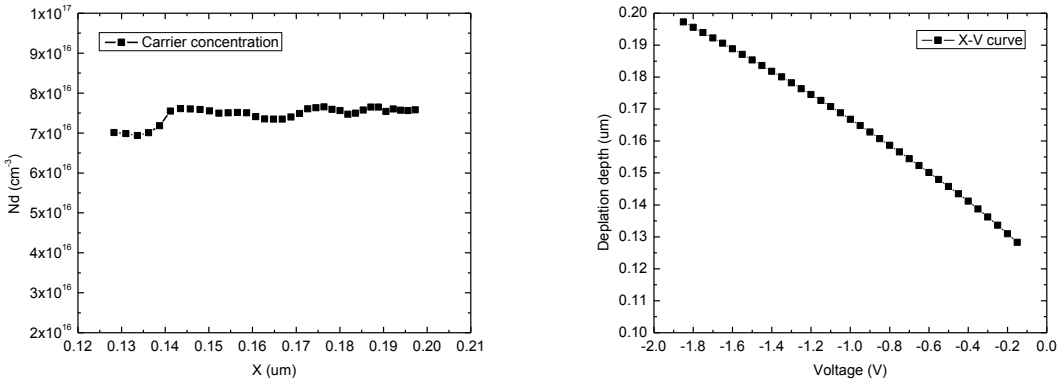
Figure 42. (a) C-V plot and (b) 1/C2-V plot (data provided by Prof. Ringel's group, Zeng Zhang, Electrical & Computer Engineering, The Ohio State University)

5.3.3 Carrier Concentration

From differential equation (17), the formula to calculate the doping concentration is found to be [1]

$$N_d = \frac{2}{qK_s\varepsilon_0 A^2\left[d\left(1/C^2\right)/dV\right]} \quad (18)$$

Usually, the calculation process is embedded in the C-V measurement program controlled by LabVIEW, and the generated plot from the former data is shown in Figure 43(a). From this we can see that the depletion depth already reaches 130 nm when the reverse bias voltage is zero. Note the C-V measurement also provides the voltage information, from which we can directly find the depletion depth at a certain voltage, see Figure 43(b).



(b) **(b)**

Figure 43. The doping concentration plot (a) and the depletion depth at different reverse bias voltages (b) (data provided by Prof. Ringel's group, Zeng Zhang, Electrical & Computer Engineering, The Ohio State University)

5.4 Alpha Spectroscopy

5.4.1 System Setup

The setup for the alpha spectroscopy system is shown in Figure 44, in which a probe station is used for small device (in the order of tens or hundreds of micrometers) measurement under the monitor of a microscope. During measurement, the ground, shielding, light, length of the BNC cable between the preamplifier and the device, voltage, and the setup parameters all play an important role in obtaining a spectrum with a high signal-to-noise ratio.

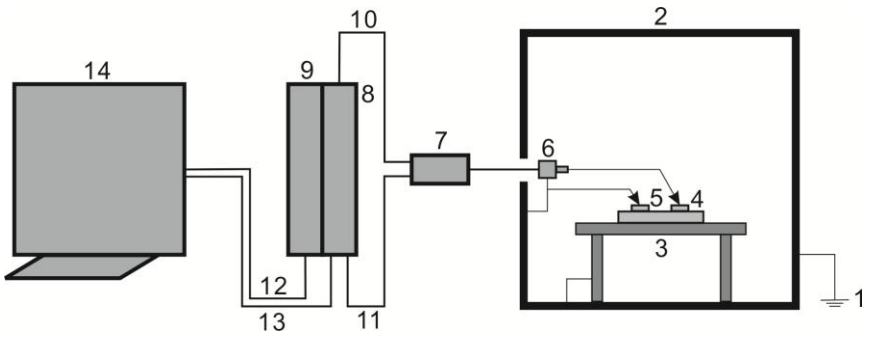


Figure 44. Alpha spectroscopy system: 1, Earth ground; 2, Shielding; 3, Probe station; 4, Ohmic contact; 5, Schottky Contact; 6, BNC cable; 7, Preamplifier; 8, CAEN N6724 Digitizer; 9, CAEN Power Supply; 10, Power supply to Preamplifier; 11, High voltage supply to detector; 12, Remote control of power supply; 13, Digitizer connect to computer; 14, Computer

5.4.2 Shielding

The shielding of electromagnetic (EM) waves in the open air is necessary for an electronic circuit, especially when an amplifying process is involved. For our alpha spectroscopy system, two types of shielding methods are employed: ***Metal box shielding and BNC wire shielding.***

The amplitude of an electromagnetic wave propagating through a conductor decays exponentially on a characteristic length scale named skin depth [12]

$$E(x,t) = E_0 e^{-x/d} \cos(\omega t - x/d) \quad (19)$$

In which E is the electric field strength of the EM, x the propagating depth to the conductor, ω the angular frequency of the EM given by $\omega = 2\pi f$, and d the skin depth that is given by

$$d = \sqrt{\frac{\rho}{\pi f \mu}} \quad (20)$$

Where ρ and μ are the resistivity and the absolute magnetic permeability of the conductor respectively. Based on this formula, the skin depth for different metals can be calculated, and the results of which are shown in Figure 45, from which we can see that steel is a very good material for shielding EM waves.

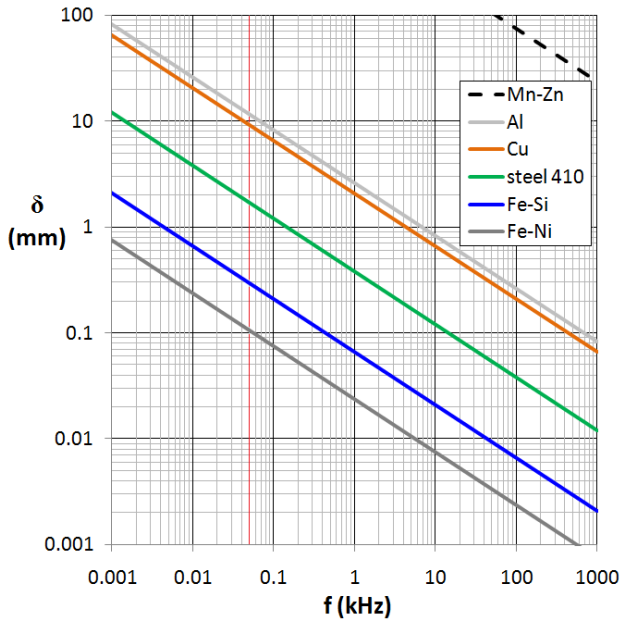


Figure 45. Skin depth for different metals [12]

5.4.3 Ground

Besides shielding, the proper ground of the device also plays an important role for the alpha spectroscopy experiment. In our setup, the ground is fulfilled by connecting the shielding, the guard of the probe station, and the ground wire of the BNC cable to the metal sheet stick on the wall (earth ground). The effect of the ground can be clearly seen by sets of experiments keeping all the other parameters the same but with different ground methods (Figure 46): without any ground, ground the cable, and ground both the cable and the shielding box. From which we can see that the ground of both cable and shielding is necessary to significantly reduce the noise.

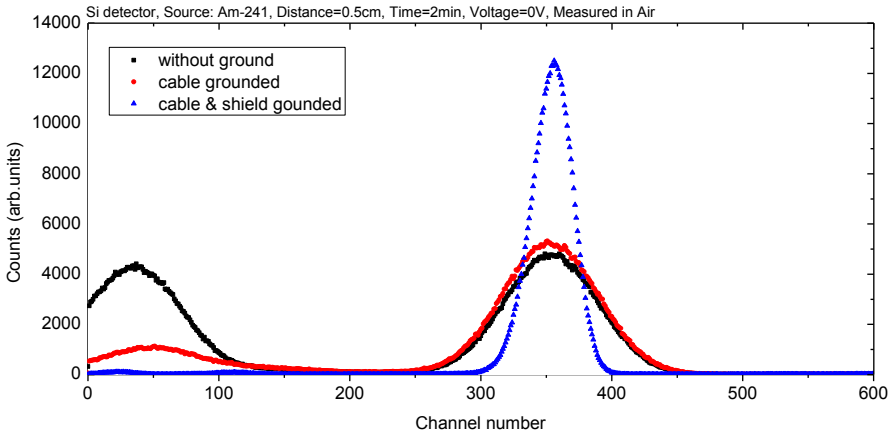


Figure 46. Effect of ground to alpha spectroscopy experiment

5.4.4 System Characterization

In order to test the validity of this setup, a measurement is performed using a Co-57 source emitting Gamma-rays with energy of 122 keV and a commercial Si detector.

Figure 47 shows the measured spectrum for Co-57, from which we can see that the peak of 122 keV can be clearly seen, which indicates that the setup of the system works well.

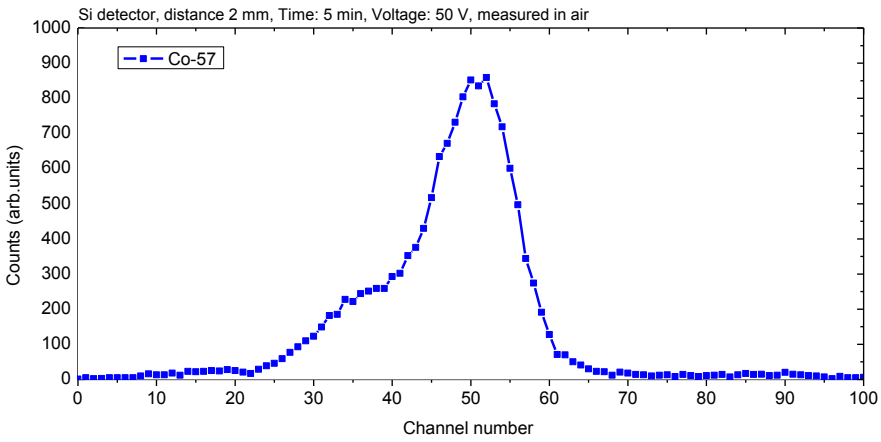


Figure 47. Co-57 gamma-ray spectrum

However, for the mesa structure disscussed later, there are some limitations when doing the alpha spectroscopy: First, the voltage should be less than 10 V in order to maintain a small leakage current. Second, based on the voltage supplied, only a low energy of about 100 keV can be deposited in the depletion region. Third, the distance between the source and detector is larger because the probe station is empoyed in the measurement in which two probes have to be put between them. Fourth, in order to maintain a low leakage curent, the active area of the detector is very small, in this case only about 0.09 mm^2 (Schottky contact area) instead of 300 mm^2 for the Si detecor. Thus, during the measurement, special care must be taken, especially regarding the optimization of the parameters for the control software. The parameters for this experiment are shown in Figure 48.

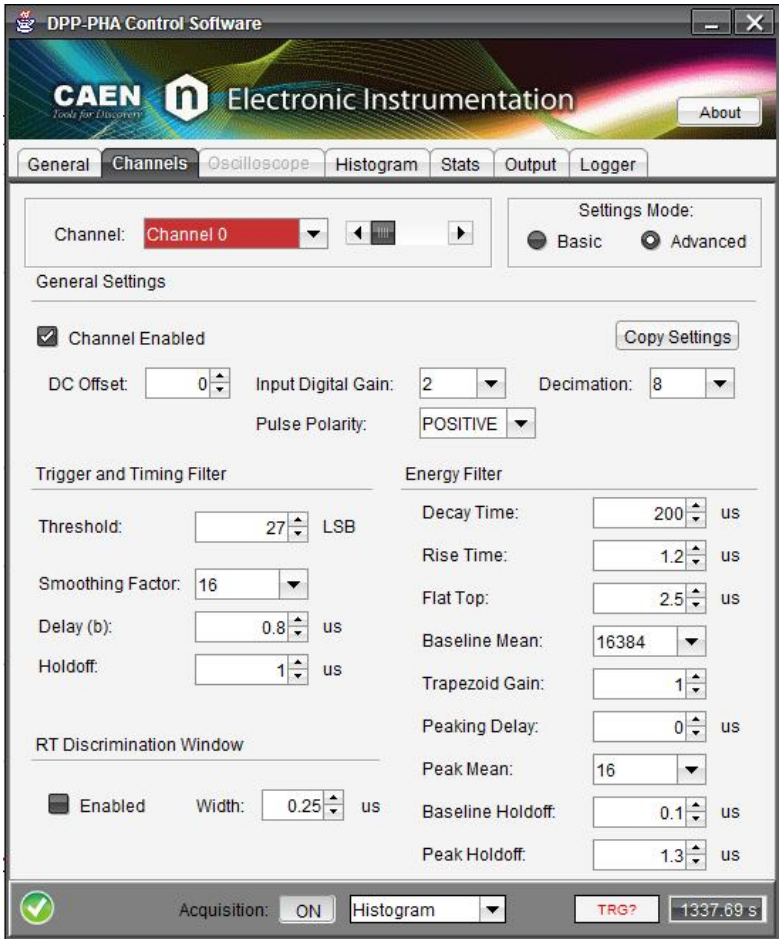


Figure 48. Parameters set up for Co-57 spectroscopy measurement

5.5 Charge Collection Efficiency

5.5.1 Definition of CCE

The charge collection efficiency (CCE) of a detector is defined as the measured charge divided by the generated charge [13, 14]

$$CCE = \frac{Q_{meas}}{Q_{gen}} \quad (21)$$

When a charged particle enters the active region of the detector, its energy will be deposited in the detector and mainly cause two effects: one fraction of the energy is used for electronic stopping process to liberate e-h pairs, and one portion is used for nuclear stopping process to cause vibration of lattice atoms (also known as phonons). If all the generated electrons and holes are collected by the outer circuit, the CCE is said to be 100 %; otherwise, if some of them are trapped or recombined during transport process in the detector, then the CCE is less than 100 %.

5.5.2 CCE of the Detector

In view of the CCE measurement, detectors can be categorized into thick and thin detectors, which indicate whether or not the active region is thick enough to fully stop the incident charged particles. The CCE of a thick detector can be determined by comparing its alpha spectrum with the result of a silicon barrier detector, which is assumed to have a CCE of 100 % [14]. Figure 49 for instance illustrates this [13]: two alpha spectrums are generated by a Si detector and a test detector, respectively, after energy calibration if the channel number of 4100 corresponds to the energy of 4600 keV, and the channel number of 1500 corresponding to the energy of 1683 KeV, then the CCE of the tested detector is approximately 1683/4600=37 %.

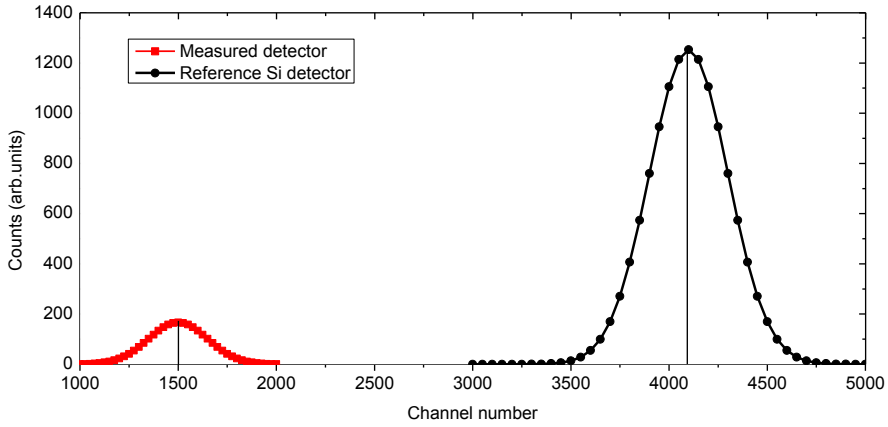


Figure 49. CCE calculation demonstration (data used is generated by Gaussian distribution)

For thin detectors, the thickness of the active region is smaller than the project range of the charged particle. Thus, only a portion of its energy is deposited in the detector. In this case, the CCE can be estimated by comparing the experimental result with the simulation result generated from SRIM code.

5.6 Neutron Irradiation and High Temperature Performance

Neutron irradiation experiment is used to evaluate the potential use of GaN detector in a harsh radiation environment. Several studies have been conducted for the neutron irradiation effect on GaN material and device performance. According to these results, both fast and thermal neutrons contribute to the lattice damage. The former is due to direct knock-on atoms, and the latter is due to recoil processes during the neutron activation of Ga and N atoms [15]. After neutron irradiation, the undoped material becomes more semi-insulating. In addition, a dominant deep level trapping center was introduced by neutron damage with an activation energy of 0.75 eV [16]. After the neutron irradiation, light-dose damage (~10^{11} cm^{-3}) can be recovered by self-annealing

process [17], high-dose damage (10^{17}-10^{18} cm^{-3}) can only be recovered at high temperature over 1000 ^{0}C because of the formation of defect clusters [18]. Our primary experiment shows that the device will lose both of its Schottky and Ohmic behavior when the dose is ~10^{16} cm^{-2};

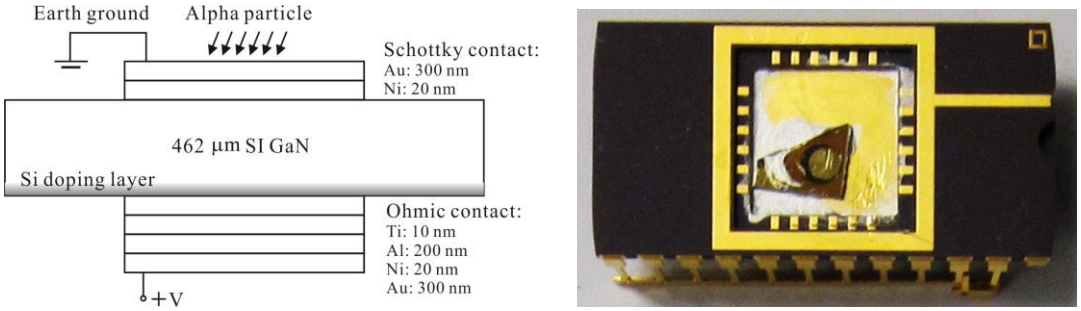
Very little research has been conducted into the high temperature performance of GaN detectors. Based on our experiment, Schottky contact fabricated on SI GaN is more stable at elevated temperatures, and Schottky contact realized on UD GaN suffers a degradation after rapid thermal annealing.

6. GaN Schottky Diodes and Their Performance

6.1 Sandwich Schottky Diode Based on Ammono SI GaN

6.1.1 Schottky Diode Structure

In our research, the sandwich structure Schottky diodes were fabricated on freestanding GaN, either semi-insulating or undoped. First, the SI GaN wafer purchased from Ammono Company, Poland was studied. The 462 μm bulk SI GaN with front-side (Ga-face) optically polished and back-side (N-face) roughly polished has a resistivity in the range of 10^{9}-10^{12} Ohm-cm, which is achieved by compensating the unintentional, background oxygen donor with some kind of material. (Unfortunately, the applied isotopes are not disclosed.) The resulting carrier concentration ranges from 10^{11} to 10^{13} cm^{-3}. Figure 50(a) shows the schematic, cross-sectional diagram of the GaN Schottky diode device, and Figure 50(b) is the photography of the fabricated device wire bonded to a sample holder. The fabrication processes and their setup parameters can be found in the former discussions.



(a) (b)

Figure 50. (a) The schematic, cross-sectional diagram of the GaN Schottky diode and (b) the fabricated device

After device fabrication, I-V measurement and Alpha spectroscopy experiment are performed. Figure 51 shows the I-V curve, measured by a Keithley 2400 SourceMeter that is connected to a four-probe station, from which we can see that the device exhibits a typical Schottky diode behavior. However, the leakage current under large reverse bias voltage is still high, which may be due to the surface decomposition during high temperature annealing process. The linear behavior, when the device is forward biased, indicates a high resistance, which originates from the thick semi-insulating bulk matter.

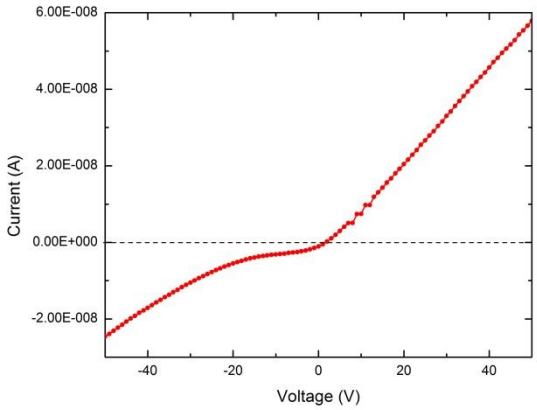


Figure 51. I-V curve for Schottky diode based on Ammono freestanding SI GaN

The Alpha spectroscopy experiment was also performed using Am-241 source, which produces alpha particles at energies of 5.486 MeV, 5.443 MeV and 5.388 MeV as well as 60 keV gamma rays [19]. The reverse bias has been aplied up to –200 V, but no signal has been extracted. Based on theoretical calculations, the device can be fully depleted at a voltage of -26 V by assuming a carrier concentration of 10^{13} cm^{-}3, and thus all the alpha particles have been fully stopped in the depleted region. We conclude that the liberated electron-hole pairs are trapped or recombined inside the material, which results in a very low Charge Collection Efficiency (CCE). From the literature review, Fe used for compensating GaN will form deep level trapping centers [20, 21], which might be the main reason for the carrier lost during transportation. Thus, for SI GaN, the thickness of the wafer should not be larger than the range of the Alpha particle (~15 μm).

6.1.2 Cathodoluminescence Results of Ammono SI GaN

In order to obtain some quantitative information for the traping centers in SI GaN, Cathodoluminescence (CL) experiment was performed by Prof. Brillson's group in the Department of Electronic and Computer Sience Engineering, OSU. Two abnormal phenomena were observed. The first is that the 3.4 eV wide band-gap was totally missing in the CL spectrum shown in the Figure 52. This indicates that the material is no longer a semiconductor because no band-gap is ever present. The reason for this is most likely due to the fact that the material has been over-doped with certain kinds of compensators, whose energy levels fill out the band gap between the conduction band and the valence band. Thus, whenever e-h pairs are liberated by the charged particles, they will be

immediately trapped by these energy levels instead of jumping to the conduction band of the semiconductor.

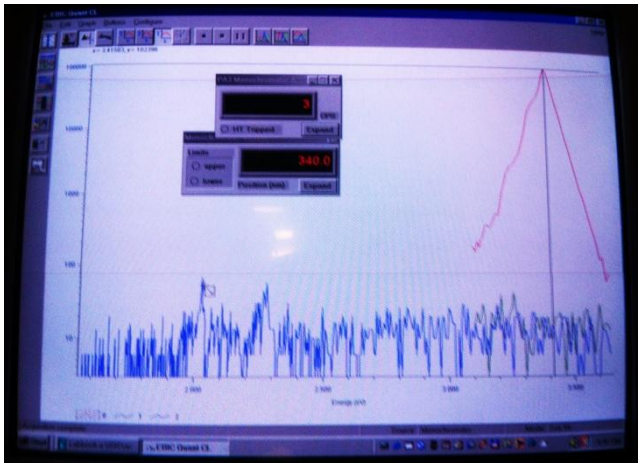


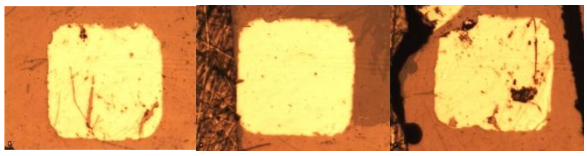
Figure 52. CL spectrum of a reference GaN (red line) and the Ammono SI GaN (blue line)

For the CL experiment, energetic electrons (1-5 keV) are used to promote electrons from the valence band to the conduction band. When an electron and hole are recombined, a photo is emitted from which energy levels present in the semiconductor can be found. Another strange phenomenon observed it that the electrons used for CL experiment were not scattered away after inject into the wafer. This usually happens for insulators such as oxide materials, but not for semiconductors such as GaN. This result again indicates that the material has lost its semiconductor properties and become an insulating material.

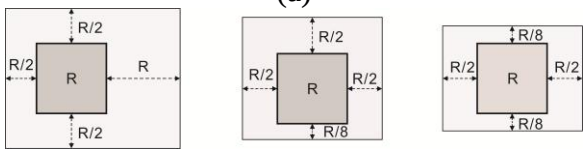
6.1.3 Leakage Current Analysis for Sandwich Structure Devices

In order to find the originations of the leakage current and their relative weights for the sandwich structure devices, three devices were fabricated on Ammono free-standing SI GaN with both sides Schottky contact. They all have a rectangular shape

with the same size of 1 mm by 1 mm. The photography of these devices and their I-V curves are shown in Figure 53(a) and Figure 54(a), respectively. For leakage current analysis, we propsed a **Surface Paralell Resistance Model** (SPRM): the leakage current composed of both surface leakage and bulk leakage, with the bulk leakage characterized by bulk resistance which is proportional to the thickness of the wafer; the surface leakage is characterized by surface reistance, which is proportional to the distance between the edge of the metal contact and the edge of the wafer. Based on the geometry of the devices, the resistances calculated are shown in Figure 53(b), and the generated I-V curves are shown in Figure 54(b), in which the reference resistance R is chosen to be 4×10^8 Ohm. From this we can see that the measured and calculated I-V curves are consistent with each other, and the model is thus verified and the leakage current is mainly due to the surface leakage in this case.



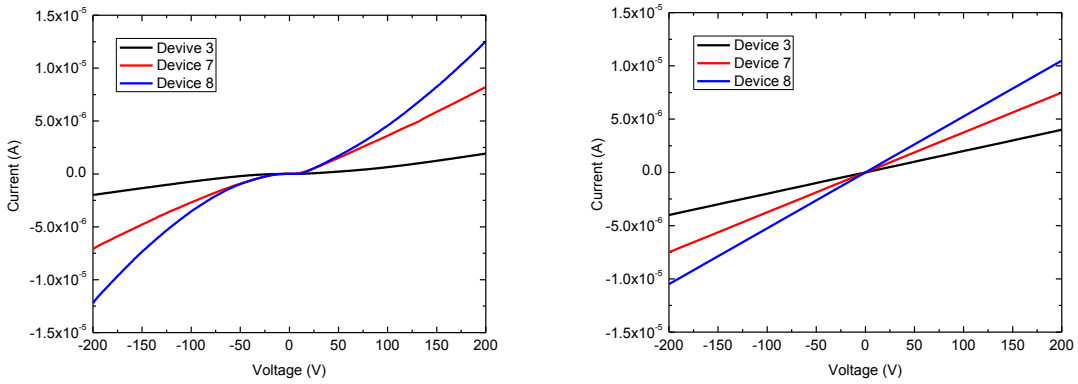
(a)



$R_3=R/8$ $R_7=R/15$ $R_8=R/21$

(b)

Figure 53. Resistance model of surface leakage current analysis for device 3, 7 and 8



(a) (b)

Figure 54. Measured I-V curve (a) and calculated I-V curve (b)

6.2 Sandwich Schottky Diode Based on Kyma SI GaN

6.2.1 DRCLS Results of Kyma SI GaN

Before making a device on the Fe compensated SI GaN purchased from Kyma, deep level transient spectroscopy (DRCLS) experiment was performed by Prof. Brillson's group in the Department of Electronic and Computer Sience Engineering to estimate the possible defects present in this material, and the results are shown in Figure 55. Besides the band-gap peak at 3.47 eV, the spectrum also shows two common peaks of yellow luminescence (YL: 2.18 eV) and blue luminescence (BL: 2.93 eV), and a new peak at 1.71 eV. This 1.71 eV peak is the conduction band to deepen the level defect transition. Compared with undoped samples, the peak of the YL band for the SI material shows a redshift, which may result from the V_{Ga} related complexes due to the Fe-doping.

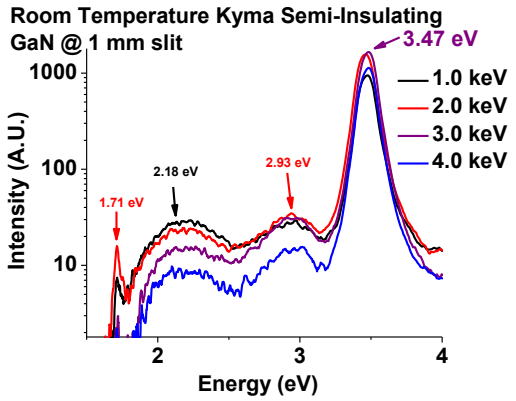
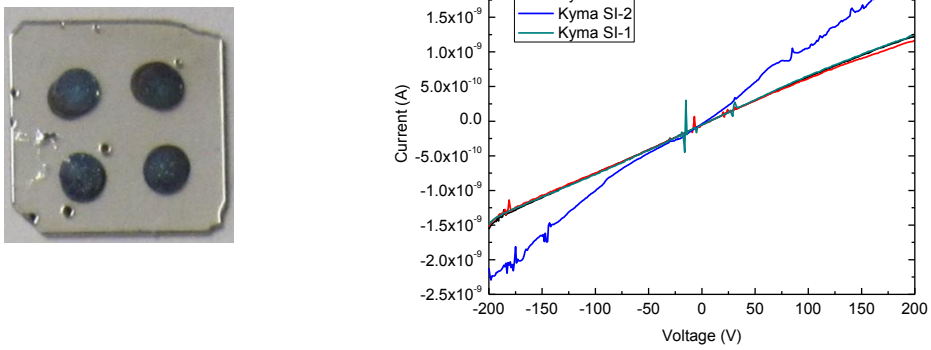


Figure 55. DRCLS spectral for Kyma SI GaN sample

6.2.2 Double Schottky Contact Structure Devices

Since double Schottky contact structure detectors have been successfully realized on SiC and AsGa semiconductors, we also employed this structure on the Kyma freestanding SI GaN. Figure 56(a) illustrates the device in which one side is Ti/Al/Ni/Au metal stack with 1 minute annealing at a temperature of 850 C, and one side is Ni/Au metal stack. The I-V curce for the four devices are shown in Figure 56(b). From this we can see that these devices have not broken down at a large bias of -200 V; in addition, we find the Schottky contact can withstand a high temperature up to 850 ^{0}C. Alpha spectroscopy was perfomed, but it was still impossible to obtain a spectrum, which is again due to the trapping centers formed by the Fe dopant.



(a) (b)

Figure 56. Double Schottky contact structure devices fabricated on Kyma freestanding SI GaN (a) and its I-V curve (b)

6.3 Sandwich Schottky Diode Based on Kyma UD GaN

For the freestanding undoped GaN, the influence of the deep level trapping centers caused by Fe dopant can be eliminated. However, for this kind of material, we facing a difficulty in making a good Schottky diode. First, an Ohmic contact (Ti/Al/Ni/Au) with a diameter of 7.5 mm was formed by high temperature annealing at a temperature of 850 ^{0}C for 1 minute, which method has been successfully employed by Zhou [3], and then a Schottky contact (Ni/Au) with the same size is deposited. The measured I-V curve is shown in Figure 57(b), from which we can see that the Ohmic contact is formed but can be further improved by Si implantation, and a large leakage current existed for the Schottky contact, which results from the large contact area and the possible detects under the contact. By employing Si implantation and activation processes, good Ohmic contact can be formed, which result is shown in Figure 57 (c) by measuring two Ohmic contacts deposited on the same side. However, because of the severe surface

decomposition or bulk defect propagation during the high temperature annealing process (1150 ^{0}C for 1 min), Schottky contact can no longer be formed (see Figure 57(d)) by measuring a 300 µm by 300 µm Schottky diode.

Based on these results, we conclude that in order to fabricate a good Schottky diode on UD GaN, the diameter of the Schottky contact should be controlled to minimize the leakage current, and a chemical mechanical polishing (CMP) process should be employed after Si activation. It is important to note that meeting these requirements will not guarantee an alpha response detector, because some other types of trapping defects may still be present in the material, and the thickness may thus also have to be decreased.

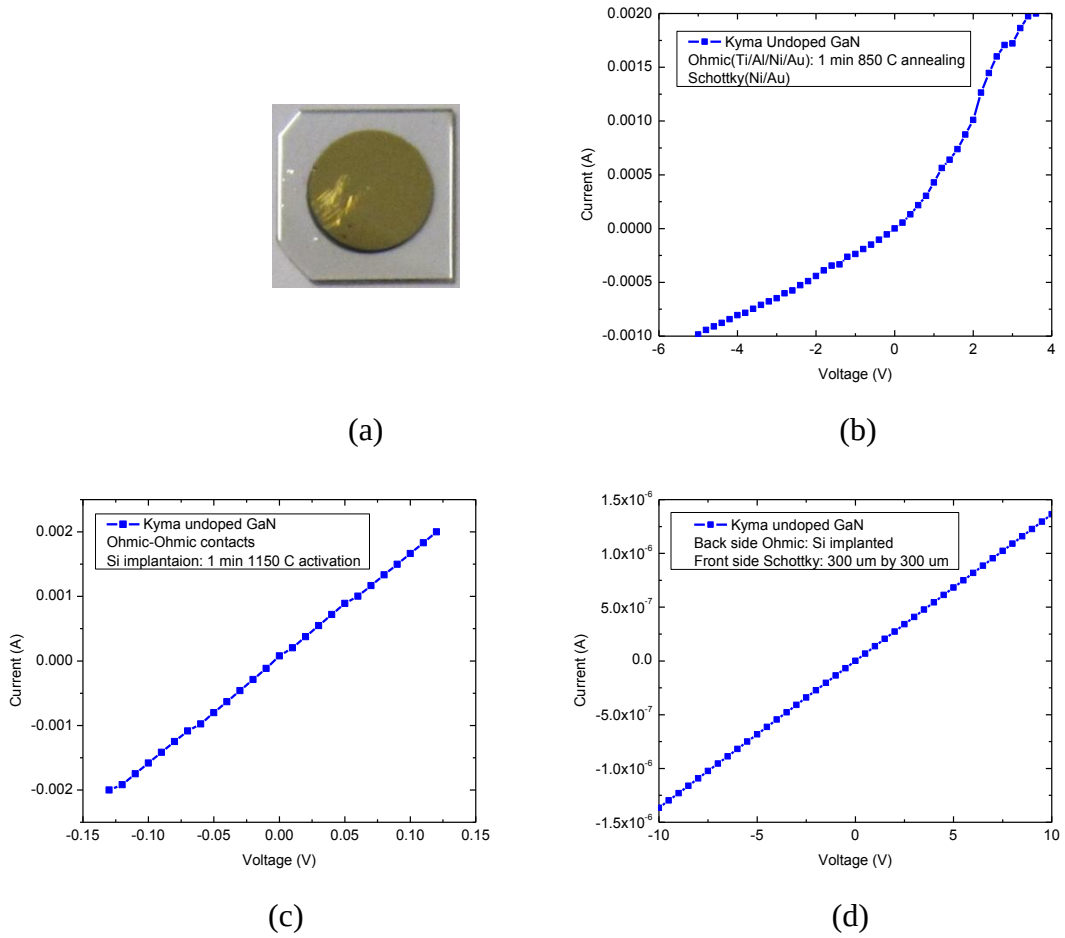


Figure 57. Schottky diode based on Kyma UD GaN and its I-V curves

6.4 Mesa Structure Based on Super-lattice GdN/GaN

6.4.1 Material Growth

Two super-lattice (SL) GdN doped GaN wafers were grown by Myers' group in the Department of Material Science and Engineering, OSU, one composed of 50 periods of alternating 10 nm UD GaN and 1 Monolayer (ML) GdN (SL-1), and the other composed of 50 periods of alternating 10 nm UD GaN and 2.4ML GdN (SL-2). During the growth, a difference was observed between the two wafers in terms of their micro structures: for SL-1, GdN is uniformly distributed inside GaN, but for SL-2, the doped GdN forms islands that embed into GaN and that separate from each other (see Figure 58). Figure 59(a) shows the Atomic force microscopy (AFM) result of the surface for SL-2 wafer, from which a root mean square (RMS) of 0.8 nm was calculated. This value indicates a relatively smooth surface, but this still needs to be improved for device fabrication (the best value should be less than 0.5 nm). Figure 59(b) shows the X-ray diffraction (XRD) analysis for the SL-2 wafer, which indicates that a final period thickness of 13 nm is achieved, and thus the total thickness is found to be 650 nm for this SL layer using this method [22].

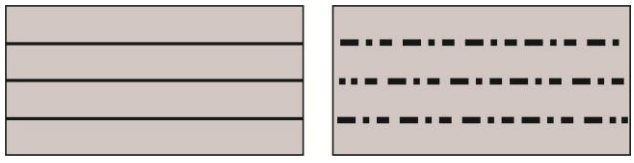
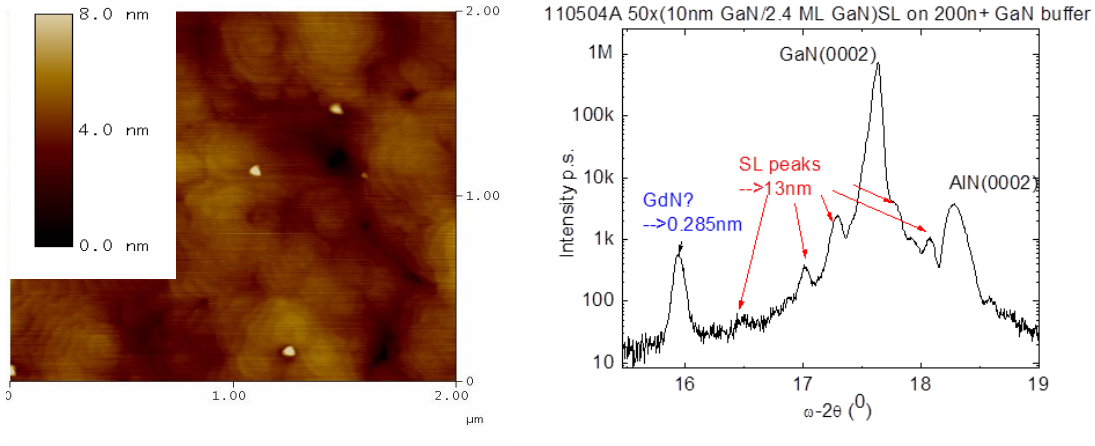


Figure 58. Representation of GdN distribution in GaN



(a) (b)

Figure 59(a). AFM of SL-2; (b) XRD of SL-2

On the one hand, Gd dopant will increase the carrier concentration of the GaN wafer; on the other hand, since the scale of the layers are so small, quantum mechanical effects may exist, but what form this will take and to what extent remains unclear. One possibility is that the several MLs of doped GdN may form sequences of potential barriers that degrade the transportation of the generated carriers in GaN.

6.4.2 Device Structures

The schematic cross-sectional and top view diagram, together with the photographs of the two devices made on SL-1 and SL-2, are shown in Figure 60. Sapphire (Al_2O_3) is used as the substrate for growing GaN because of the availability for large high quality crystals and its stability at high temperatures. AlN template is used to minimize the lattice mismatch between GaN and sapphire, thus increasing the quality of the epitaxial GaN layer. The high carrier concentration buffer layer GaN is used to form Ohmic contact and also to act as a transition layer to future decrease the lattice mismatch. The dopant GdN is used for neutron detection as discussed early.

For SL-1, the guard ring structure is employed, but some areas are destroyed; the Ohmic contact is not realized by metal deposition but formed by directly touching the buried surface with a metal probe. Because the buffer layer has a high carrier concentration, a relatively good Ohmic contact can still be formed by this method. For SL-2, all the individual Schottky contacts are fabricated far from the Ohmic contact, which prevents us from obtaining a reliable C-V experiment due to the parasitic capacitance generated from the buried buffer layer. Rectangular Schottky contacts with four dimensions were deposited in order to find the optimal size: 200 μm by 200 μm, 300 μm by 300 μm, 250 μm by 500 μm, and 500 μm by 500 μm. The 200 μm versions cannot be used because they are located near the edge of the wafer where lots of surface defects exist.

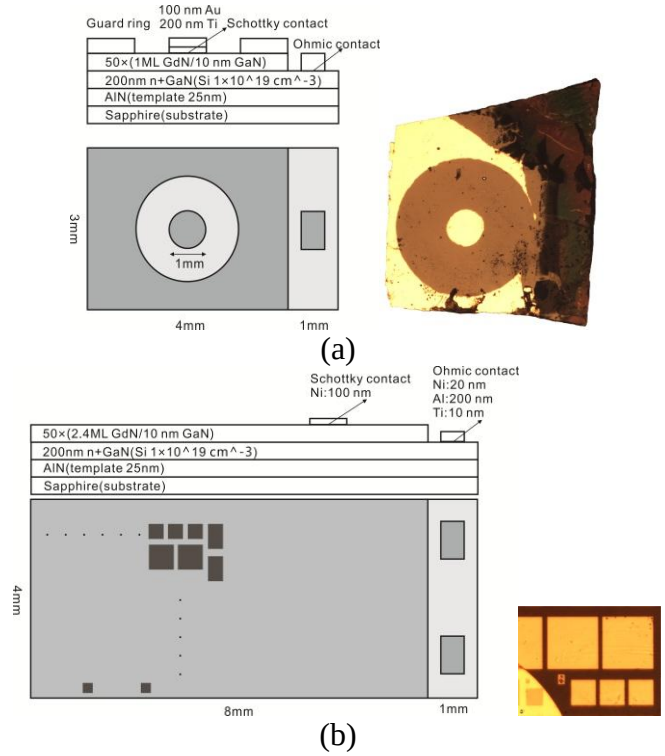


Figure 60. The schematic cross-sectional and top-view diagram of the GaN Schottky diode for SL-1 (a) and SL-2 (b)

6.4.3 I-V Characteristic of the SL-1 Schottky Diode

The I-V curve measured for SL-1 Schottky diode before and after neutron irradiation is shown in Figure 61. This shows that, before neutron irradiation, the Schottky contact can withstand a high reverse bias, but the leakage current is also high (the leakage current should be less than 10^{-9} A for device application). This is due to both the bulk leakage and surface leakage discussed early. The Ohmic contact is not ideal because the current has not reached the default limit of 2 mA, even if the voltage goes up to 20 V (ideally, several V should be enough to reach this default value), due to the physical contact method used. After neutron irradiation with a total flux of about 10^{16} cm^{-2}, both the Ohmic and Schottky contacts were destroyed and the device became a resistor with very high resistance. This result is consistent with former observations by J. Grant, who states that the extremely low leakage currents exhibited by heavily irradiated detectors could be as a result of the generation of deep acceptor levels within the band gap [23].

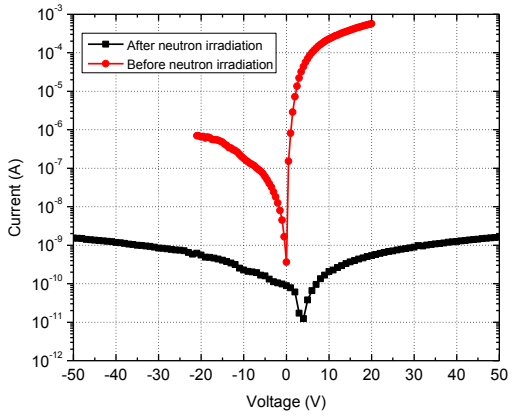
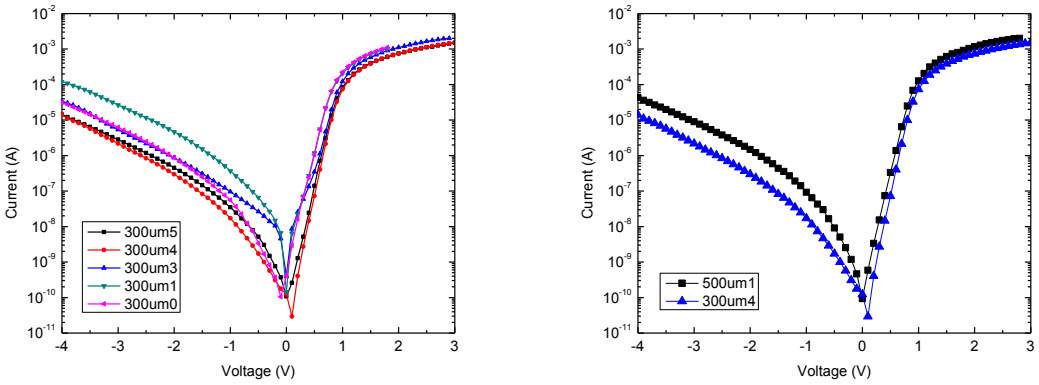


Figure 61. I-V curve of SL-1 before and after neutron irradiation

6.4.4 I-V Characteristic of the SL-2 Schottky Diode

The I-V curves measured for the SL-2 Schottky diodes are shown in Figure 62. Figure 62(a) shows the I-V curves measured from several 300 μm by 300 μm size Schottky diodes, from which we can see that: a) the wafer has non-uniform quality across the surface since the leakage currents are different for different diodes; b) the leakage current is still high, which is mainly due to the surface leakage that will be discussed later; c) very good Ohmic contact is formed, which means the etching has reached the buried GaN layer. Figure 62(b) compares the best I-V curves for the 300 μm and 500 μm size Schottky diodes, from which we can see that leakage current increases with contact size, this is result from the bulk leakage that will be discussed later



(a) (b)

Figure 62. (a) I-V curve of SL-2, 300 μm Schottky diode; (b) I-V curve of two size Schottky diode

6.4.5 Leakage Current Analysis for the Mesa Structure Device

In order to find the origination of the leakage current for the mesa structure devices realized on super-lattice wafer, we applied these diodes with high reverse bias

voltage until they were close to breakdown. We find that the breakdown voltage is not proportional to the contact size; instead, all the devices break down at almost the same voltage, which can be seen by extrapolation of the reverse I-V curves shown in Figure 63. This indicates that the leakage current is mainly due to the bulk leakage, which can again be explained by the surface resistance model: since the distance of these diodes are far from the edge of the wafer, the resistance caused by the surface will be very high, and thus the leakage current through the bulk will be dominated [24].

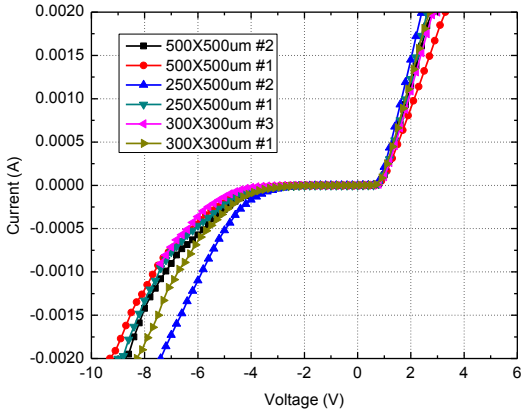


Figure 63. Large reverse biased I-V curve of different size Schottky diode

6.5 Proposed Detector Structure

Based on the former analyses, we proposed a new Schottky diode structure that can be realized on a wafer purchased from Kyma Company, as shown in Figure 64:

1) The 2 μm semi-insulating GaN grown directly on a high carrier concentration n+ GaN substrate to minimize the lattice mismatch between the two layers, and thus to reduce the dislocation density of the epitaxial layer;

2) Semi-insulating GaN is chosen to minimize the leakage current and obtain a large depletion region under small bias voltage;

3) The thickness of 2 μm is chosen to increase the depletion depth and thus to deposit more energy from the charged particle, but to prevent it from becoming too thick to cause severe e-h pair trapping problem;

4) The shape of the Schottky contact should be circular to minimize the current crowding effect in order to increase the breakdown voltage, and the size should be larger than 0.5 mm to ensure enough counting rate during alpha spectroscopy measurement;

5) Guard ring structure is employed to decrease the leakage current;

6) Ohmic contact should not be far from the Schottky contact to eliminate the influence of parasitic capacitance caused by the substrate layer.

7) On top of both the Schottky and Ohmic contacts, a layer of gold is used to facilitate wire bonding process, and the thickness of the gold layer should be larger than 200 nm to ensure the bonding quality;

8) During the fabrication process, high temperatures should be avoided to prevent the introduction of surface defects, and if surface quality was degraded (RMS

larger than 0.5 nm), a chemical mechanical polishing process should be adopted, which can be carried out by Kyma company.

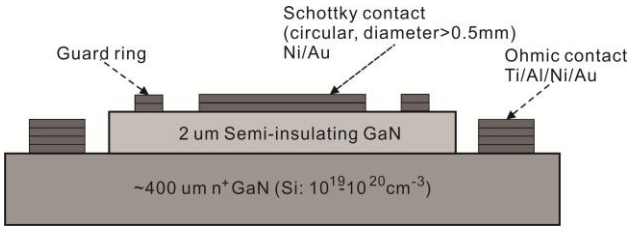


Figure 64. Proposed Schottky diode structure

7. Conclusion

In this study, fabrication processes such as photolithography, etching, ion implantation, metal deposition, wire bonding, etc. are investigated with respect to the performance of the radiation detector fabricated on the semiconductor material GaN. We found that the etching rate of GaN decreases with increasing impurities, and an optimum Si implantation dose and activation temperature is established for the semi-insulating materials to from Ohmic contact. The characterization processes such as resistivity, current-voltage, capacitance-voltage, charge collection efficiency and neutron irradiation etc., which are used to evaluate the quality of the device, are discussed. In order to find the origination of the leakage currents and their relative weight, a Surface Parallel Resistance Model, which has been successfully applied to the fabricated devices, is proposed. Based on these analyses, we find that the most promising type of GaN material with which to make a radiation detector is still the thin-film epitaxial semi-insulating GaN by comparing the available growth techniques. A new detector structure based on this kind of material is thus proposed, which takes into account all the factors that will affect the performance of the detector.

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Appendix A: Wafer Cleaning Process

1) Ultrasonic bath in Acetone for 2 min;
2) Ultrasonic bath in IPA (Isopropanol) for 2 min;
3) Rinse with HF: DI (Deionized Water) dip (1:10) for 30 second;
4) Rinse in DI water for 1 min;
5) Dry the wafer by blow N_2 gas.

Note: the process is provided by Prof. Ringel's group, Zeng Zhang, Electrical & Computer Engineering, The Ohio State University

Appendix B: Photolithography Process

Step	Operation	Date/Initials	Notes
1	Dehydration Bake		Hotplate 5.0 min 180º C (note that setting one of the Super Nuova "purple" hotplates to 190º C will give the desired surface temperature).
2	Spin Coat LOR5A		COT03 Program 9, final spin speed 3,000RPM Pipette using brown neoprene bottle labeled LOR 2A in secondary containment tray. Cover at least two-thirds of the substrate with LOR, ensure that all dispense holes are covered with tape, and then start the program.
3	Bake		Hotplate 5.0 min 180º C (see step 1)
4	Spin Coat 1813		COT03 Program 4, final spin speed 3,000 RPM Pipette using brown neoprene bottle labeled Shipley 1813 in secondary containment tray. Cover at least two-thirds of the substrate with resist, ensure that all dispense holes are covered with tape, and then start the program.
5	Bake		COT03 hotplate, Program 4, 1.0 min, 115º C
6	Expose		ALN01 or ALN02 Hard Contact, 2.4 secs, 15 mW / cm^2 i-line
7	Develop		HOD07 2.0 min, MF-319 in glass dish, DI water rinse, N2 dry.
8	Inspect		INS05 or any microscope Use yellow filter to avoid exposing resist if any redevelop is under consideration Inspect for pattern quality. Ensure exposed areas of the substrate are absent of photoresist. Redevelop if desired.

Note: recipe provided by Prof. Ringel's group, Zeng Zhang, Electrical & Computer Engineering, The Ohio State University

Appendix C: Etching Process

1. **Turn on the RIE & ICP power.**
2. **Chamber Preparation.**

Program mode: Load batch file "ganprep.bch" after loading sapphire. Ready. Run. **When Mesa Etch step takes place, tune the RIE power knobs if necessary.**

*Manual mode:

1. Vent load-lock, load sapphire carrier wafer, pump load-lock, wafer handling, Ion gauge on.
2. BCl_3 Blast: 32 sccm Cl_2; 8 sccm BCl_3; 5 sccmAr; Pressure 5mTorr; 65W RIE; 300W ICP; He backside cooling on.
    a. Flow gas for 2:30 before turning on ICP and RIE
    b. **1 min** with ICP and RIE on
    c. Feature plate should be 10^oC, walls should be 20^o
    d. Cleans surface, knocks off native oxide
3. Mesa Etch: 20 sccm Cl_2; 5 sccmAr; 40W RIE; NO ICP; pressure 5mTorr; He backside cooling
    a. Flow gas for 1 minute before turning on RIE power
    b. **9 mins** with RIE power engaged.
4. Purge: N_2 gas; pressure 10 mTorr
    a. 1 minute
    b. Keeps any 'bad' gas from getting into the Ion gauge
5. Ion gauge off, wafer handling, vent load-lock.

3. **Actual Etch. (40W RIE~ 127V)**

Program mode: **Set the etch time in the program first!** Load batch file "ganringe.bch" after loading sapphire & sample. Ready. Run.

*Manual mode:

1. Vent load-lock, load sapphire & sample, pump load-lock, wafer handling, Ion gauge on.
2. BCl_3 Blast: 32 sccm Cl_2; 8 sccm BCl_3; 5 sccmAr; Pressure 5mTorr; 65W RIE; 300W ICP; He backside cooling on.
    a. Flow gas for 2:30 before turning on ICP and RIE
    b. **12 sec** with ICP and RIE on
    c. Feature plate should be 10^oC, walls should be 20^o
    d. Cleans surface, knocks off native oxide
3. Mesa Etch: 20 sccm Cl_2; 5 sccmAr; 40W RIE; NO ICP; pressure 5mTorr; He backside cooling
    a. Flow gas for 1 minute before turning on RIE power
    b. **? mins** with RIE power engaged.
4. Purge: N_2 gas; pressure 10 mTorr
    a. 1 minute
    b. Keeps any 'bad' gas from getting into the Ion gauge
5. Ion gauge off, wafer handling, vent load-lock.

4. **Ar clean**

Program mode: Load batch file “arclean.bch” with sapphire in load lock. Ready. Run.

5. Turn off the RIE & ICP power. Pump the load lock.

Note: recipe provided byZeng Zhang, Electrical & Computer Engineering, The Ohio State University

Appendix D: Metal Deposition Setup

Parameters	**Ohmic contact**					**Schottky contact**	
	Layer 1	Layer 2	Layer 3	Layer 4		Layer 1	Layer 2
Material index	Ti	Al	Ni	Au		Ni	Au
Rate (Å/s)	0.5	0.5	0.5	0.5		0.5	0.5
Final thickness (kÅ)	0.1	2.0	0.2	3.0		0.2	3.0
Thickness limit (kÅ)	0.000	0.000	0.000	0.000		0.000	0.000
Time limit (MM:SS)	00:00	00:00	00:00	00:00		00:00	00:00
Rate watch time	00:00	00:00	00:00	00:00		00:00	00:00
Rate watch accuracy (%)	5	5	5	5		5	5
Crucible	2	1	3	4		3	4
Rate ramp 1							
New rate (Å/s)	0	2.5	1.0	2.5		1.0	2.5
Start ramp (kÅ)	0	0.05	0.05	0.05		0.05	0.05
Ramp time (MM:SS)	0	1:00	0:30	1:00		0:30	1:00
Rate ramp 2							
New rate (Å/s)	0	5.0	0	5.0		0	5.0
Start ramp (kÅ)	0	0.3	0	0.3		0	0.3
Ramp time (MM:SS)	0	1:00	0:00	1:00		0:00	1:00

Appendix E: High Temperature Annealing Setup for Densify Ohmic Contact

Step	Type	Time (second)	Temperature (^{0}C)
1	Delay	20	
2	Ramp	50	300
3	Steady state	10	300
4	Ramp	50	860
5	Steady state	2	860
6	Delay	300	

Appendix F: High Temperature Annealing Setup for Si Activation

Step	Type	Time (second)	Temperature (^{0}C)
1	Delay	20	
2	Ramp	20	700
3	Steady state	10	700
4	Ramp	50	1100
5	Steady state	2	1100
6	Ramp	20	1150
7	Steady state	30	1150
8	Delay	600	

Appendix G: Wire Bonding Setup for Au

Parameters	Loop	Search	Force	Time	Power
First bonding	3.0	50	3.0	5.2	3.10
Second bonding		50	3.0	4.8	3.30

Appendix H: Si Implantation

Dopant	Si
Energy	50 keV
Dose	$1x10^{16}$ /cm^2
Temperature	Room temperature
Doping side	Back side with scratches at the corner
Angle of incidence	7 degree to the normal of the surface