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Review

A review on the GaN-on-Si power electronic devices

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ABSTRACT

The past decades have witnessed a tremendous development of GaN-based power electronic devices grown on Si substrate. This article provides a concise introduction, review, and outlook of the research developments of GaN-on-Si power device technology. The comprehensive review has discussed the crucial issues in the state-of-the-art device technology based on both GaN materials epitaxy including stress control and point defects study, and device fabrication including normally off solutions like Cascode, trench MIS-gate, and p-GaN gate. Device reliability and other common fabrication issues in GaN high electron mobility transistors (HEMTs) are also discussed. Lastly, we give an outlook on the GaN-on-Si power devices from two aspects, namely high frequency, and high power GaN ICs, and GaN vertical power devices.

1. Introduction

Power electronic devices are adopted to convert electrical energy from one form into another, which is the core of power electronic technology [1]. The development of power electronics technology has gone through a century of history, and the overall technical level has been continuously improved. This improvement has occurred along with the continuous evolution of device performance. It is not only reflected in the boost of energy conversion efficiency, but also in the increase of systems' power density. Generally, the power density is doubled in an average of every 4 years to meet the ever-increasing requirement (the so-called Moore's law of power electronics is shown in Fig. 1). In the 1960s, the solid-state power electronic era based on Si materials began, and many novel structures such as Silicon controlled rectifier (SCR), bipolar junction transistor (BJT), insulated gate bipolar transistors (IGBTs), and super-junction metal oxide semiconductor field effect transistors (MOSFETs) were invented to enhance the power density and efficiency. However, the conventional Si-based devices are running into their physical limits, resulting in the saturation trend of power density. Fortunately, the emerging wide bandgap semiconductors (GaN, SiC, etc.) are regarded as the promising materials to maintain the increasing trend.

Gallium nitride (GaN) is a good candidate for the next-generation power device, which can significantly outperform the traditional Si-based power devices due to its higher breakdown strength, faster switching speed, and higher thermal conductivity. In 1993, A. Khan et al. demonstrated the first GaN transistor based on the AlGaN/GaN heterojunction inspired by the development of the GaAs heterostructure field-effect transistors (HFETs) [2]. The polarization effect in the heterojunction induces a two-dimensional electron gas (2DEG) in the heterostructure with a high density of about 10^{13} cm^{-2}, which is one order of magnitude higher than that of the counterpart (GaAs). In addition, the 2DEG also presents a mobility of higher than 2000 $cm^2/(V•s)$. The feasibility of GaN power device was confirmed by the HFETs grown on sapphire substrate with a breakdown voltage up to 1 kV by N.Q. Zhang et al. in 2000 [3]. In 2010, the commercial enhancement-mode GaN-on-Si device was firstly released by International Rectifier (IR) and Efficient Power Conversion (EPC) corporations, followed by many other companies, such as GaN system, Transform, Navitas, Panasonic, etc [4].

Generally, GaN power devices can be classified into two categories: *lateral* and *vertical* structures. In the conventional Si power devices, vertical structure is the mainstream. Compared with the lateral one, the ver-

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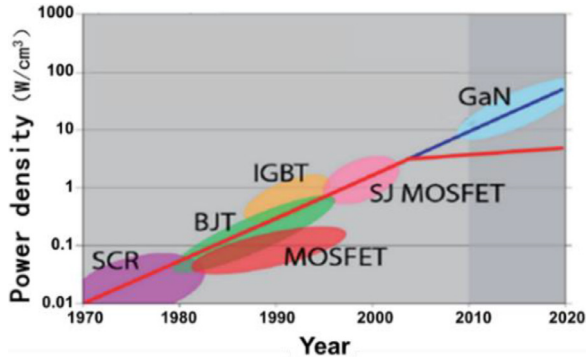

Fig. 1. The increasing trend of power density for electronic system.

tical structure can deliver a higher power density without increasing the footprints [5]. Owing to the lack of large size and low-cost free-standing high-quality GaN substrates, GaN vertical structure is still limited to academic research. In contrast, the low-cost AlGaN/GaN HFET grown on Si with a lateral structure becomes the commercial route in the industry because of its cost advantage of compatibility with the Si CMOS process flow with a feasibility for high density integration [6]. Furthermore, GaN-on-Si power devices can be fabricated on a larger wafer diameter (200 mm and above) thus lowering the fabrication cost. Thanks for the 2DEG channel, AlGaN/GaN HFET can realize a high Baliga Figure of Merit (FOM) value due to the small on-resistance and small gate charge ($R_{on} \times Q_g$), which is beneficial to enhancing the switching frequency up to Mega Hertz level. The lateral devices are suited for the low-medium voltage range (several voltages to around 1.2 kV) to replace the existing Si power devices and expand market, which includes a large portion of the power supply for photovoltaic inverter, data center, light detection and ranging (LIDAR) and so on. Though limited by the long-term reliability, GaN-on-Si devices open up the application market of consumer electronics and Quick Charger firstly in 2021.

2. Key issues in materials epitaxy and device fabrication

Since the past decade, Si has become the mainstream choice of substrate for GaN-based power high-electron-mobility transistors (HEMTs) due to its large size and low cost. The challenges of lattice and thermal mismatch have been overcome by advanced metal-organic chemical vapor deposition (MOCVD) systems with several epitaxial solutions. The high-quality, crack-free thick Ga(Al)N layer can be achieved on Si substrates as large as 8 inches. Together with the progress of GaN-based device fabrication technologies, lateral and vertical electronic devices are widely reported with increased performance year by year.

However, due to the limitation of GaN epitaxy and device fabrication, defects (dislocations, point defects, etc.) still widely exist in the GaN based materials and processing layers, and dramatically affect device performance especially when they are under high electric fields. Thus, key issues such as GaN materials epitaxy, enhancement-mode operation, device reliabilities, etc. draw much attention and call for urgent solutions.

2.1. GaN materials

2.1.1. GaN epitaxial growth on Si substrate

High quality GaN-based electronic materials grown on Si substrates are essential for high performance power devices. However, due to the large lattice mismatch (~17%) and thermal expansion coefficient mismatch (~54%) between GaN and Si, it is challenging to grow low-dislocation-density and crack-free GaN epilayers. In order to address these issues, various approaches for crystalline quality improvement and stress control have been reported for nearly twenty years, such as AlN/GaN superlattice [7], low-temperature (LT) AlN interlayer, and AlGaN buffer layer.

The AlN/GaN superlattice technology can effectively control the stress and improve the crystal quality, by inserting an AlN/GaN superlattice buffer layer with a certain thickness grown between the AlN nucleation layer and the GaN epitaxial film. As shown in Fig. 2a, the thickness ratio of AlN to GaN in the superlattice determines the equivalent Al component. Thus, the large lattice mismatch between GaN and AlN can be effectively alleviated. Meanwhile, the period of the superlattice can control the strain of GaN film. The vertically propagating dislocations may be terminated at the superlattice interfaces, thus improving the crystal quality. Using this technique, Egawa et al. [7] reported growth of AlGaN/GaN high electron mobility transistors (HEMTs) with high breakdown field (2.3 MV/cm) on 200 mm Si substrates.

Amano et al. [11] demonstrated crack-free GaN films on sapphire obtained by LT-AlN interlayer technique for the first time (Fig. 2b). The LT-AlN interlayer can also promote most dislocations bending and annihilation. This technique was previously used for improvement of crystal quality of GaN and AlN on sapphire. Then, Krost et al. [12] applied this technique to the growth of GaN on Si substrate and successfully obtained crack-free GaN films on Si.

Another alternative technique for GaN growth on Si is introduction of compositionally graded AlGaN buffers. For this technique, three step-graded AlGaN (with Al composition of about 75%, 50% and 25%) or multiple step-graded AlGaN buffers with a thickness up to 1 μm are generally used (Fig. 2c). The main purpose of this technique is to slow down the relaxation rate of the compressive strain by decreasing the lattice mismatch between the two adjacent layers. There is thus a larger compressive strain accumulated in the GaN layer during the growth. Recently, Cheng et al. developed a large lattice-mismatch induced stress control technology with a low-Al-content single AlGaN layer to grow high-quality GaN layers on Si [10], as shown in Fig. 2d.

While those approaches have made the rapid progress, as shown in Fig. 3 [8,13–22], the crystal quality and residual stress in GaN-based epitaxial layers on Si still cannot be comparable to the GaN films on SiC substrates. Thus, it limits the performance of electronic devices, especially the reliability. So, further efforts and significant innovation in material epitaxy, device design and device physics are still required.

2.1.2. Point defects in GaN materials

In addition to dislocations, point defects including intrinsic defects and impurities play an essential role in GaN. In particular, with the decrease of dislocation density and thus the improvement of GaN quality, point defects, especially impurities, have more significant influence on material properties and device reliability. This is based on the fact that, on one hand, impurities are inevitably introduced during the growth of GaN. On the other hand, they have to be intentionally doped to improve material and device properties.

Generally, Si, O, C, H, and Mg are the most common and important impurities in GaN. Si incorporated on the Ga sites (Si_{Ga}) and O on the N sites (O_N) would act as shallow donors and become one of the main sources of background carriers in GaN, Si thus becomes the dopant of n-type GaN. By contrast, Mg on the Ga sites (Mg_{Ga}) could give rise to shallow acceptors, hence p-type GaN can be realized by Mg doping. The successful preparation of p-type GaN plays an important role in the realization of E-mode HEMTs with p-GaN gate. In addition, C impurities were also highly valued. In GaN based power electronic devices on Si substrate, C is usually intentionally introduced to realize semi-insulating GaN buffer layer and thus achieve better withstand voltage characteristics. C on the N sites (C_N) act as deep acceptors (0.9–1.1 eV above the valence band) and could thus compensate the background carriers in GaN. C doped semi-insulating GaN buffer technique turns to be the mainstream method to develop GaN based electronic devices. H also act as an unavoidable and important impurity in GaN. H incorporated into interstitial sites (H_i) tend to exist in two charge states: H^+ and H^-, whereas the H^0 state is unstable due to the large negative-U

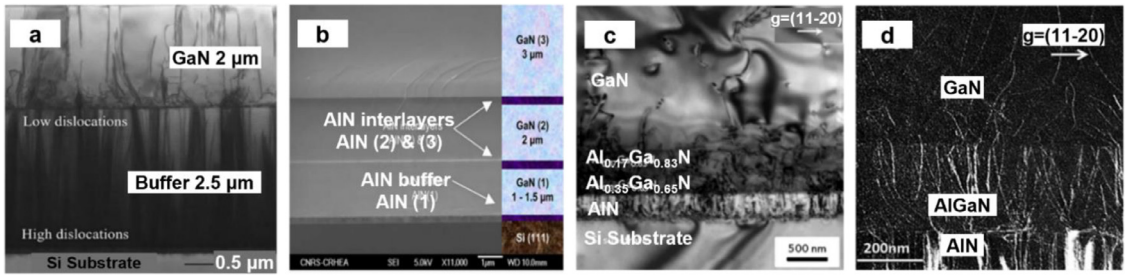

Fig. 2. Various buffer structures for GaN growth on Silicon. (a) AlN/GaN superlattice [7], (b) low-temperature AlN interlayer [8], (c) step-graded AlGaN [9] and (d) low-Al-content single AlGaN buffer layer [10].

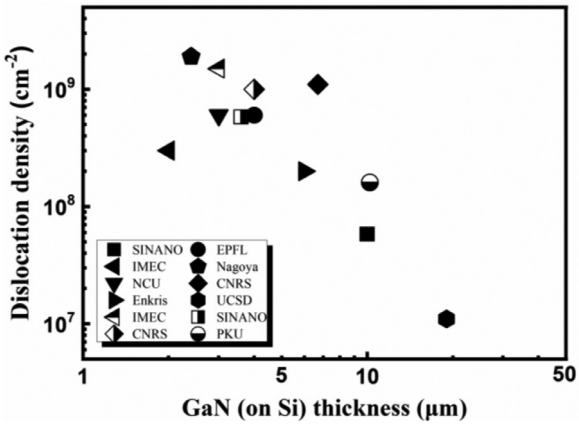

Fig. 3. The crystal quality versus thickness of GaN films on Silicon.

(-2.4 eV) effect. H is ubiquitous and has small atomic radius and very active chemical properties, it is thus easy to react with a wide variety of lattice imperfections, leading to significant effects on the optoelectronic materials properties and devices performance.

To understand the effect of impurities on the properties of materials and devices, it is necessary to study their doping behaviors. The impurity doping mechanism and regulation are extremely complex, especially for the impurities with various atomic sites and complexes. Taking C impurity as an example: C doping is usually used to prepare semi-insulating GaN, which is a core component for power electronic devices. However, the mechanism that C makes GaN semi-insulating is still a subject of debate. As a group IV element, C is amphoteric in GaN, i.e., it may occupy either Ga site to form C_{Ga} or N site to form C_N, and they can also coexist with each other, individually or forming complexes with other defects. The formation energy is related to Fermi level and growth environment, and the relevant the calculation results from Lyons et al. are shown in Fig. 4a, b. Wright et al. [25] proposed the self-compensation model through interplay between C_N and C_{Ga} states. However, Lyons et al. [23] suggested that carbon on the N site, by itself, could make GaN semi-insulating by pinning the Fermi level in the vicinity of its deep acceptor level. The controversy of C lattice site occupation confused the optical properties in GaN. Whether the isolated C_N or C_N-O_N complex that contributes to the longstanding problem about the origins of the GaN yellow luminescence (YL), has still been a subject of controversy even very recently. Wu et al. [24] investigated the atomic structure and LVMs of C impurity by vibrational spectroscopy and provided unambiguous evidence of the substitutional C atoms occupying the N site with a "−1" charge state in GaN. The schematic energy level diagrams and fundamental dipole transitions in a C_N^- center with C_{3v} symmetry is shown in Fig. 4c.

Although C doping can effectively improve the voltage with-stand properties of power devices, researchers show that the deep level introduced by C impurity can also cause the on-resistance degradation. Therefore, apart from the atomic structure, deep understanding of the localized state properties of C in GaN is also required. Referring to the localized state properties, Iwinska et al. [26] obtained the p-type conduction in C doped GaN grown by HVPE by temperature dependent hall measurement, and the hole activation energy was 1.02 eV. They propose that the energy level of C_N (0/-) was about E_V + 1.02 eV, by the reason that the hole was caused by the ionization of C_N deep acceptor. Subsequently, Narita et al. [27] obtained an E_V + 0.88 eV acceptor level signal in Mg doped p-type GaN by using DLTS, and they considered that the DLTS signal was related to C_N(0/-) level.

In addition to the C related isolated defect, the behavior of complexes has also been investigated theoretically and experimentally. Matsubara et al. [28] calculated various complexes of C in GaN. They proposed that C could form complexes with intrinsic defects and impurities such as C_N-V_{Ga}, C_{Ga}-V_N, C_N-Si_{Ga}, C_N-O_N, and C_N-H_i.

At present, due to the difficulty in point defects characterization, the research of C related point defects in the world is mostly focused on theoretical calculation, while the experimental research is still in a very preliminary stage. Consequently, the correlation between impurity defects and device performance such as the dynamic properties is still unclear. Therefore, point defect characterization methods and techniques innovation is urgently needed, and it is often necessary to combine experiments with first principles calculation when investigating the behaviors of point defects.

2.2. Enhancement-mode operation

The AlGaN/GaN heterostructure induced 2DEG is continuous in the GaN channel when the gate is biased at 0 V, which is usually called as normally-on (or depletion-mode, D-mode) operation. However, normally-off (or enhancement-mode, E-mode) properties are keenly required for the power electronic devices due to their safe operation and simplified gate driving in the power electronic systems. Approaches like Cascode of Si + GaN HEMT, F-ion implantation gated HEMT, trench gated MIS-FET/MIS-HFET and p-GaN gated HEMT are developed in past decades to reach this goal. In this part, Si + GaN HEMT Cascode technology, Trench gated HEMT, and p-GaN gated HEMT will be discussed.

2.2.1. Normally off operation using D-mode HEMT

Cascode structure is composed of D-mode GaN HEMT and E-mode Si MOSFET in series, and the switch of the whole device is controlled by controlling Si MOSFET, the high voltage is borne by the D-mode GaN device. The representative companies of Cascode structure are Transphorm, Nexperia, etc. However, Cascode structure still have some challenges need to be solved, such as capacitance mismatch, parasitic parameters, etc. First, the capacitance mismatch issue caused by different chips (Fig. 5a). The interelectrode capacitance will be charged during the switching of the device. The schematic diagram of the charging path and the equivalent schematic diagram of the red part are also illustrated.

The equivalent circuit is a circuit in parallel with the source-drain capacitance of the Si MOSFET, the gate-drain capacitance of the Si MOS-

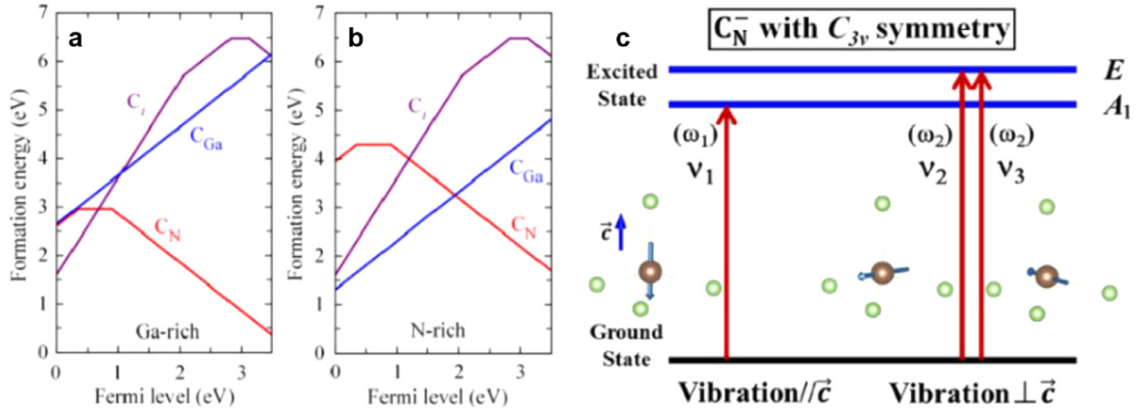

Fig. 4. Behaviors of Carbon atoms in GaN-based materials. Formation energy versus Fermi level for substitutional C_{Ga}, C_N, and interstitial C_i configurations in GaN under (a) Ga-rich conditions, (b) N-rich conditions [23]. (c) The schematic energy level diagrams, and fundamental dipole transitions in a C_N center with C_{3v} symmetry. The calculated vibrational directions of C atom are also depicted [24].

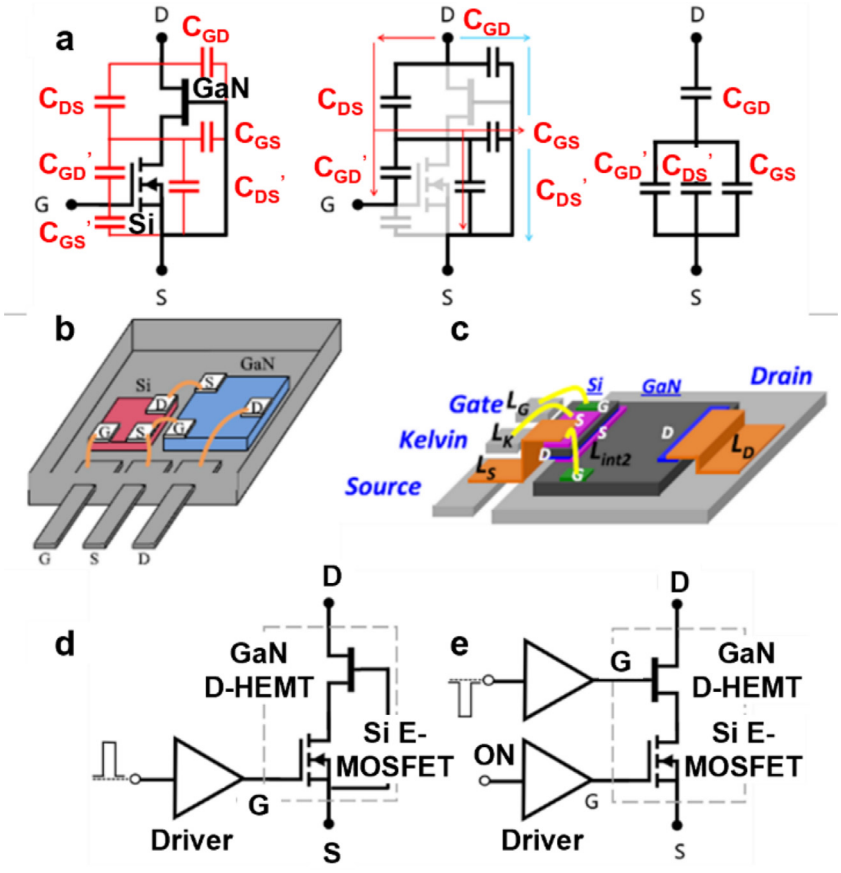

Fig. 5. Normally off operation using D-mode HEMTs. (a) The interelectrode capacitance of Cascode, charging path of interelectrode capacitor during device turn off, and equivalent circuit diagram of red charging path, respectively; the schematic diagram of (b) the parallel packaging structure [29], and (c) the COC package [30]. (d) equivalent circuit of Cascode structure, and (e) negative voltage direct drive mode.

FET, the gate-drain capacitance of the GaN device and in series with the source-drain capacitance of the GaN device. According to the voltage sharing principle of the capacitor series, when the capacitance of the three parallel capacitors is smaller, its voltage is larger, at the time the voltage across them, the drain voltage of Si MOSFET may be higher than its breakdown voltage during the shutdown process, and lead to device degradation or even damage, this phenomenon we called capacitive mismatch. Therefore, in the process of device design, Si devices are required to match the capacitance of GaN devices. Specific requirements are to make the capacitance of three shunt capacitors large enough to make the drain- source voltage of Si devices smaller than avalanche voltage after the charging of the device's interelectrode capacitance completed. The common capacitance matching method is to parallel a capacitor between the drain-sources of the Si device to improve the capacitance of the shunt. However, selecting an appropriate capacitance value is a difficult problem in capacitance matching. A too small capacitance value cannot meet the matching requirements, while a too large capacitance value will affect the switching performance of the device. Additionally, the capacitive mismatch will lead to extra power loss in the soft switching process of Cascode devices [31].

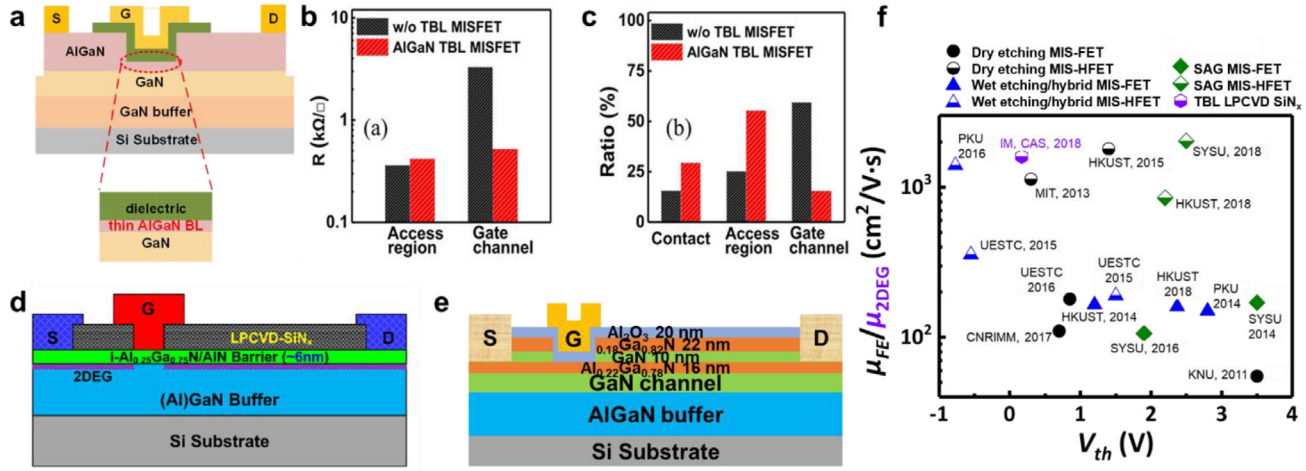

Fig. 6. Technologies and developments of MIS-HFETs. (a) Schematic cross-section of MIS-HFET, (b) sheet resistance in gate and access regions, (c) resistance distribution for w/o TBL MISFET and AlGaN TBL MISFET [32], and schematic cross-section of (d) MIS-HFET by TBL + LPCVD SiN_x [33], (e) MIS-HFET with recessed gate by MOCVD thermal etching method, (f) Benchmark of μ_{FE} and V_{th} for the recessed-gate GaN transistors.

The second issue is that the parasitic parameters caused by the Cascode structure becoming larger [29]. Fig. 5b shows the schematic diagram of the parallel packaging structure. Parasitic inductance is induced when the chips are connected with other chips, which will bring unnecessary oscillation at high switching frequency. A COC (chip-on-chip) packaging [30] is presented as an optimization of the parasitic inductance caused by the parallel packaging structure (Fig. 5c). The parasitic inductance between the source of GaN device and the drain of Si MOSFET can be minimized by the COC packaging.

In order to solve the problems in Cascode structure, the negative voltage direct drive mode was proposed by separating the drive form of Si MOSFET and GaN HEMT (Fig. 5e). Compared with Cascode structure, this direct driving mode has no reverse recovery loss caused by the body diode, neither the capacitance mismatch issue. Due to the chip directly controls GaN FET by negative voltage drive, it can well reflect the advantages of GaN devices in switching speed. Therefore, it has been adopted by many companies, e.g., TI, VisIC, etc.

2.2.2. *Insulated gate structure: MIS-FET and MIS-HFET*

GaN-based insulated gate field-effect transistors (FETs) with an insulating gate dielectric provide many desirable properties, such as suppressed gate leakage and large gate voltage swing. These devices are generally in the form of fully recessed-gate GaN metal-insulator-semiconductor FETs (MIS-FETs) or the partially recessed-gate metal-insulator-semiconductor HFETs (MIS-HFETs).

Conventional MIS-FETs can achieve E-mode operation by cut off 2DEG under the gate by completely removing the AlGaN barrier layer under the gate, so that the device is turned off under zero gate voltage. When the positive gate voltage increases to greater than the V_{th}, an electron accumulation layer will be formed at the gate interface as the conductive channel of the device, and device is turned on. These devices have an advantage of large threshold voltage (V_{th}), while suffer from the deterioration of the channel mobility (μ_{FE}) scattered by rough surface of recessed area and electrically active defects of MIS structure. And the unsatisfactory channel mobility will increase on-resistance (R_{on}) of the devices and power consumption of the system.

In order to improve μ_{FE} and reduce the R_{on}, MIS-HFET is proposed, with the insulating dielectric on a residual thin AlGaN barrier layer (TBL) of several nanometers (Fig. 6a). The residual TBL could keep the channel 2DEG away from the MIS interface, resulting in a higher μ_{FE} and leading to a lower R_{on} [32], while at the expense of threshold voltage. In Ref. [32], sheet resistance and resistance distribution for MISFET and MIS-HFET are compared. MIS-HFET has a lower resistance of gate channel because of the higher μ_{FE} (Fig. 6b, c). Obviously, both structures have their own advantages and disadvantages, and can be selected according to actual applications. Having high V_{th} and high μ_{FE} at the same time is preferred. In addition, the reliability of threshold voltage caused by MIS interface charges and trap states is still the biggest challenge that hinders the commercialization of insulated gate FETs, which will be discussed in Section 2.3.2.

To date, many technologies have been proposed to develop insulated gate FETs, such as dry etching, wet etching, selective area growth, thin barrier layer (TBL) + LPCVD SiN_x, and MOCVD thermal etching methods.

Dry etching technology is the earliest proposed method for the insulated-gate E-mode GaN transistors, it uses inductively coupled plasma (ICP), reactive ion etching (RIE) or ion beam etching (IBE) equipment for direct etching. To suppress or eliminate negative impaction of lattice damage defects during in dry etching, large numbers of research have been carried out to optimize and improve this technology. A tetramethylammonium hydroxide (TMAH) treatment was developed to achieve a MIS-FET with V_{th} = 3.5 V, but the μ_{FE} as low as 55 $cm^2/V{\cdot}s$ [34]. To further improve μ_{FE}, Huang et al. [35] partially removed the AlGaN barrier by a high temperature ICP etching process, and fabricated a MIS-HFET with V_{th} = 1.6 V, ΔV_{th} = 50 mV. As discussed in literatures, dry etching has the advantages of simple process, low cost, high etching efficiency, and excellent anisotropic, the etching results can be improved by reducing power, post-chemical treatment, and self-terminating technology. However, inevitably lattice damage and interface contamination still cause the carrier mobility in gate region much lower than that in the access region and bring serious problems of the gate reliability. The uniformity of etching depth also cannot be precisely controlled. So wet etching and other methods are presented and expected to solve these problems.

Wet etching is another technique to remove materials in selected areas through a chemical reaction between the solution and the GaN materials, which presents an obvious advantage of no lattice damage. Because of its high corrosion resistance, gallium nitride is mostly removed through a wet treatment including oxidization subsequent with acid corrosion. Using the digital wet etching method, Wang's group obtained a MIS-FET with μ_{FE} = 150 $cm^2/V{\cdot}s$, V_{th} = 2.8 V, ΔV_{th} = 170 mV [36]. Lin et al. [37] successfully realized the self-terminated by inserting a thin AlN/GaN bilayer, and promoted the μ_{FE} to 1400 $cm^2/V{\cdot}s$. Although wet etching can alleviate lattice damage, the μ_{FE} still relatively low, and the anisotropy of oxidative corrosion can magnify dislocation defects [38], which degrade device characteristics, such as drift of the device threshold voltage, current collapse. Furthermore, wet etching lacks efficiency and uniformity. Therefore, new methods need to be developed.

Using the principle that single crystals is difficult to nucleate on an amorphous mask (usually SiO_2), the selective area growth method as follows: prepare a mask in the gate area of the GaN template, regrowth epitaxial materials in the unmasked area, and then remove the mask, finally a recessed gate structure is obtained. Based on the SAG technique, an E-mode GaN recessed gate MIS-FET was fabricated by Zheng et al. [39], presenting V_{th} = 1.9 V, ΔV_{th} = 50 mV. Subsequently, Liu's [32] group published a partially recessed-gate Al_2O_3/AlGaN /GaN MIS-HFET using SAG technique with both high V_{th} (~2.5 V) and μ_{FE} (~2033 $cm^2/V{\cdot}s$). The SAG method avoids etch damage, Ga-O bonds, and improves the gate mobility, while the contamination introduced by the mask is inevitable, and efficiency is low.

Technique of TBL + LPCVD SiN_x is based on the interface charge modulation to overcome the controllability issue in recessed gate. TBL AlGaN/GaN heterostructure is used to ensure natural normally off gate channel and high electron mobility. As the SiO_2 or SiN_x passivation grown by low-pressure chemical vapor deposition (LPCVD) exists high density of positive charge on the surface of heterojunction [40], the 2DEG in access region can be effectively recovered to reduce R_{on}. If passivation was deposited before gate formation, fluorine-based plasmas can be adopted to via the passivation in gate region and the AlGaN TBL serves as a good etch-stopping layer. As shown in Fig. 6d, Huang et al confirmed that the SiN_x passivation layer grown by LPCVD can significantly increase 2DEG density and mobility (1601 $cm^2/V{\cdot}s$) [33], and demonstrated E-mode Al_2O_3/AlGaN/GaN MIS-HFETs with high-uniformity and low-hysteresis. This new method has the advantages of high etching-depth uniformity and batch-to-batch repeatability, and it could also avoid lattice damage and improve mobility. While the V_{th} of devices is relatively low, and the device reliability need further works to enhance it.

MOCVD thermal etching method takes advantage of the distinction of thermal decomposition selectivity between materials (such as GaN and AlGaN) caused by different bond energy. Using a composite barrier heterostructure, Su et al. tried this method for the preparation of E-mode GaN HFETs (Fig. 6e). Although no device results about MIS-HFETs have been reported by this novel technique, it still has the advantages of excellent uniformity and low interface state density demonstrated by the CV results [41]. This provides a promising path for E-mode insulated gate devices with excellent reliability and stability.

However, challenges still exist in MIS HFETs to reach reliable performance, and more efforts are required in order to succeed in commercial applications. To improve the threshold voltage, channel mobility, and the reliability of the device, several preparation methods, each of them have their own strengths and weaknesses, have been developed for realizing MIS-FET and MIS-HFET.

Usually, FETs with both high μ_{FE} and high V_{th} are welcome thus some comparisons of μ_{FE} versus V_{th} are given in Fig. 6f for MIS-FET and MIS-HFET fabricated by these methods. More importantly, the defects introduced during the process can cause device reliability issue, which is a major obstacle to the commercialization. In short, the insulated gate device technology has made significant progress in research and will continue to strive for further improvements.

2.2.3. p-type gate structure

A p-GaN gate solution is another way for HEMT to realize the normally off operation. The p-type GaN can lift up the surface potential of the AlGaN barrier layer, resulting in a depletion of the 2DEG in the gate region even at zero gate bias. The threshold voltage (V_{th}) is usually in the range of +1 ~ 2 V at a criterion of I_{DS} = 10 μA/mm [46]. Due to the robust operation, p-GaN E-HEMTs are stepping into the commercial market, particularly in the consumer electronics. However, there are still some challenges should be overcome in the fabrication of p-GaN gated HEMT with higher performance.

Obtaining an ideal Mg acceptor doping profile is of great significance for the p-GaN gate to reach high controllability. While it is almost impossible because that the "memory effect" of Mg turning-on and impurity out-diffusion will result in a graded doping curve (Fig. 7a). The low Mg doping concentration in the p-GaN approaching to AlGaN will lead to a low V_{th}, and the high Mg acceptor concentration in the GaN channel will cause an increase of the R_{on}. Therefore, the growth conditions of p-GaN layer should be accurately controlled in order to achieve a well balance.

In conventional p-GaN E-HEMT, the whole epitaxial structure is grown layer by layer for once. Thus, the AlGaN barrier thickness is uniform in the whole wafer, typically 10–20 nm with Al component of 15–28%. A main conflict lies between the improving of V_{th} and the lowering of R_{on}. Improving of Mg doping level can effectively enhance the V_{th}, while R_{on} may be increased due to Mg out diffusion presented in Fig. 7a [42]. Moreover, increasing Al component and barrier thickness of the AlGaN layer indeed significantly reduce the R_{on} due to an increase of the 2DEG density, but the V_{th} will be hard to improve into a large enough range. To moderate this contradiction, a p-GaN regrowth technique has been proposed with thick barrier in non-gate region and thin barrier in gate region. As the remained AlGaN barrier thickness is crucial for the V_{th}, conventional dry etching methods for partial gate recessing usually results in a wide distribution of the DC characteristics. Through a newly developed approach of fully gate recessing and AlGaN barrier regrowth technique, V_{th} uniformity has been intensively improved from 229 to 63 mV [43], as shown in Fig. 7b. For the gate regrowth technique, achieving a high-quality interface is another key challenge because problems of surface damage and contamination will be brought by the gate recessing process, and defects can be easily generated at the start of (AlGaN/) p-GaN regrowth (Fig. 7c) [44]. If the interface states were not well treated, the gate performance will deteriorate with enlarged hysteresis, high gate leakage, etc. Therefore, thermal cleaning or decomposition prior to the Ga(Al)N regrowth in MOCVD has been utilized to effectively solve these problems [41,47]. The OFF-state leakage in p-GaN E-HEMTs with thermal cleaning has been demonstrated to be reduced about 3 orders of magnitudes (Fig. 7d).

Another crucial process in the device fabrication is recovery of the 2DEG in the non-gate region. Usually, the p-GaN layer in the non-gate region is removed by some dry etching methods, thus, to recover the 2DEG. Due to a thin AlGaN barrier and depletion effect of p-GaN, the dry etch process should stop at the AlGaN surface precisely because both over-etching and under-etching will result in a low 2DEG density then a high R_{on}. Adding some oxygen or fluorine in the conventional chlorine-based atmosphere, the dry etching process can present a high selectivity ratio for GaN over AlGaN due to formation of (Al, Ga)O_x or (Al, Ga)F_x compounds on the AlGaN surface, which cannot be easily etched away due to owning of high bond energy [48]. To avoid the etching process, the p-GaN can be passivated by some ion treatment techniques, e.g., H plasma, for that the Mg acceptor can be deactivated when forming Mg-H complexes [49]. The 2DEG recovery in the non-gate region has a strong influence on the total on-resistance, which is usually around 15 Ω•mm for the 650 V devices and particularly depends on the 2DEG sheet resistance, ohmic contact resistance and the resistance of the interlayer metals.

Moreover, the gate contact types, either Ohmic or Schottky, in the p-GaN E-HEMTs are widely studied because of its heavy impacts on the gate performance. Theoretically, when the gate is at a positive bias, the total voltage uniformly drops on the two layers of p-GaN and AlGaN for the gate with Ohmic contact, thus the resistance of the p-GaN need to be high, for instance, increasing the p-GaN thickness, to reduce the gate current. If the gate contact is Schottky type, the most voltage will drop on the reverse junction formed by metal/p- GaN thus a low gate current can be achieved. With this consideration, metals with low work function (TiN, Ti, Al, etc.) are employed for the Schottky gate contact, and the Mg doping concentration need to be relatively low in the p-GaN surface layer. In this Schottky case, the p-GaN thickness is commonly set in the range of 70 ~ 100 nm to effectively control the 2DEG underneath. During the formation of gate contact, p-GaN surface damage and

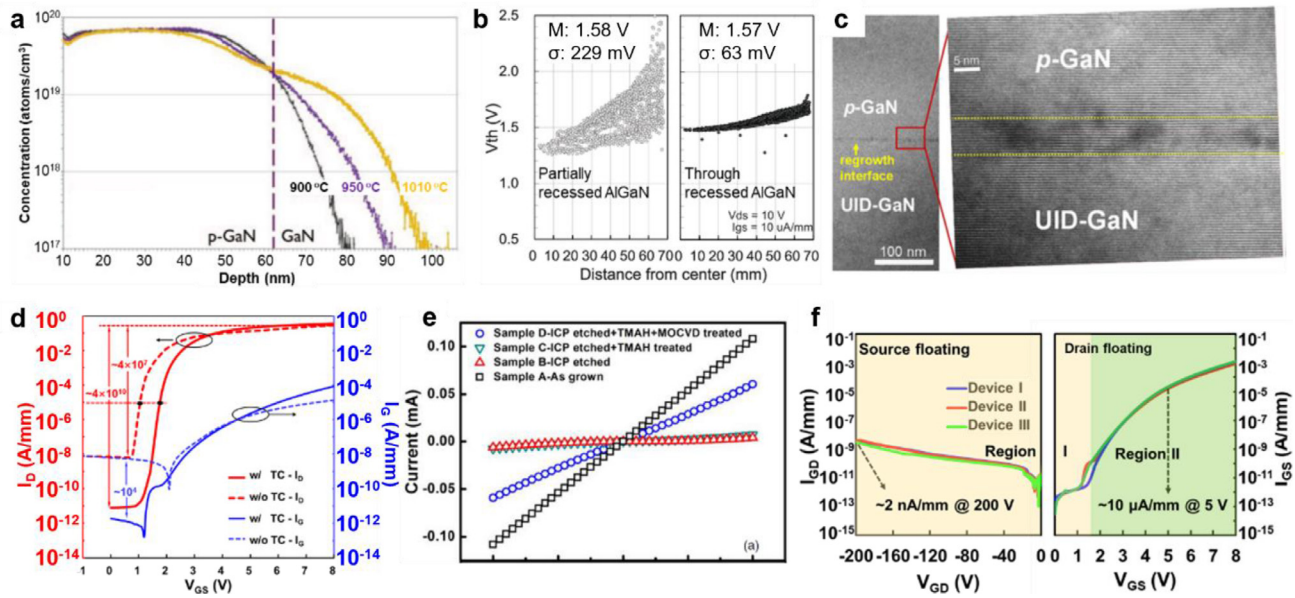

Fig. 7. Challenges in fabrication of p-GaN gated E-mode HEMT and its developments. (a) Mg doping files at various growth temperatures [42], (b) statistics of V_{th} in p-GaN E-HEMT with AlGaN barrier partially or fully recessed prior to gate regrowth [43], (c) image of the regrowth interface between p-GaN and UID-GaN [44], (d) transfer characteristics of the p-GaN E-HEMTs w/ and w/o thermal cleaning before gate regrowth, e) Ohmic contact fabrication for p-GaN with surface damage [45], and (f) gate leakage uniformity for the E-HEMTs with regrown p-GaN gate [46].

contamination should be carefully treated to improve the gate reliability and uniformity [45,46], as shown in Fig. 7e, f.

2.3. Device reliability

Till now, the reliability is still the key constraint for the HEMTs to step into the high-level applications and mass market. Due to an imperfect (Al)GaN crystal and unexpected defects introduced during the fabrication processes, the HEMTs are likely failed in the switching operation, which might turn to disasters for the whole systems. Therefore, the device reliability must be studied in-depth and evaluated to fulfill some standards to keep safe. In application circuit, GaN-based HEMTs are required with high breakdown voltage, low on-state resistance, fast switching frequency, etc. The issues of device reliability often come from two aspects: the 2DEG conduction and the gate controllability. In this section, the device reliability will be reviewed from dynamic R_{on}, gate reliability (especially the V_{th} instability) and other common issues to understand the physic basis behind the real devices.

2.3.1. Dynamic R_{on}

Unlike traditional Si power devices, unstable on-resistance (R_{ON}) issues commonly occur in GaN power devices. Specifically, after dynamic switching stress, the dynamic R_{ON} will be larger than the static value, which leads to inaccurate power consumption assessments. This section focuses on the dynamic R_{on} from the aspects of physical mechanisms, characterization techniques, and its current status in GaN HEMTs.

As we known, GaN devices can provide enhanced energy efficiency and higher power density in power electronics applications with low power loss and high switching frequency. Although GaN devices in power electronic converters have advantages, the newly developed devices still have some problems such as the dynamic R_{ON} phenomenon. The dynamic R_{ON} is the on-resistance measured immediately after switching the HEMT from high stress OFF-state to ON-state. Since the dynamic R_{ON} value is larger than the static R_{ON}, the conduction loss will be higher than expected, thereby reducing the efficiency of the converters. As for the lateral GaN-on-Si power devices, dynamic R_{ON} degradation, originating from buffer trapping, surface trapping and gate instability (Fig. 8a), has been regarded as a main challenge [50].

When the device is subjected to high voltage stress on the off-state drain, the positive bias between drain and gate causes the injection of electrons in the gate region, and the injected electrons are captured by the surface defects of the AlGaN barrier layer in the gate-drain access region. The positive voltage between drain and substrate will also cause electrons to be injected from the substrate and trapped by defects in the GaN buffer layer [53]. On one hand, the accumulation of the above-mentioned negative charges leads to a decrease in the 2DEG density. On the other hand, during the hard-switching transient state, the hot electron effect causes some electrons in the channel to be trapped by nearby defects, which will also cause the reduction of 2DEG density. Another cause of the degradation of dynamic R_{on} is the gate instability. For a p-GaN gated HEMT, electron trapping will occur in the gate region when the gate is overdriven. Because the gate overdrive voltage will decrease under the preset on-state gate bias, a positive threshold voltage (V_{TH}) shift may also lead to the increase of dynamic R_{ON}.

According to recent reports, the high-voltage off-state stress, in addition to on-state gate stress, could also bring about a positive V_{TH} shift in p-GaN HEMT with a Schottky gate contact.

Due to the switching speed of GaN devices, the measurement speed of the dynamic R_{ON} measurement circuit is a key issue. A semiconductor analyzer is an approach to measure dynamic on-resistance, but the switching delay of the instrument will be relatively large, so this test method is not recommended. Meanwhile, due to shorter delay, higher sampling rate and lower cost, double pulse tester (DPT) is widely used to assess the dynamic performance of power devices, including dynamic R_{ON} performance. As shown in Fig. 8b, the DPT with a clamping circuit is commonly used for quantitative evaluation of dynamic R_{ON} under various switching conditions, including off-state time, off-state voltage, temperature, frequency, duty cycle, on-state current, and on-state gate voltage. The clamping circuit clamps the off-state drain-source high voltage near the on-state voltage drop to ensure the on-state voltage measurement accuracy requirements. It is worth noting that the clamping circuit needs a fast enough response to accurately measure the low on-state voltage after switching from the high off-state voltage. The red insert in Fig. 8b is an example of fast clamping circuit [51], which contains only passive components, and can measure the dynamic R_{ON} value in a short time after the device switching transient.

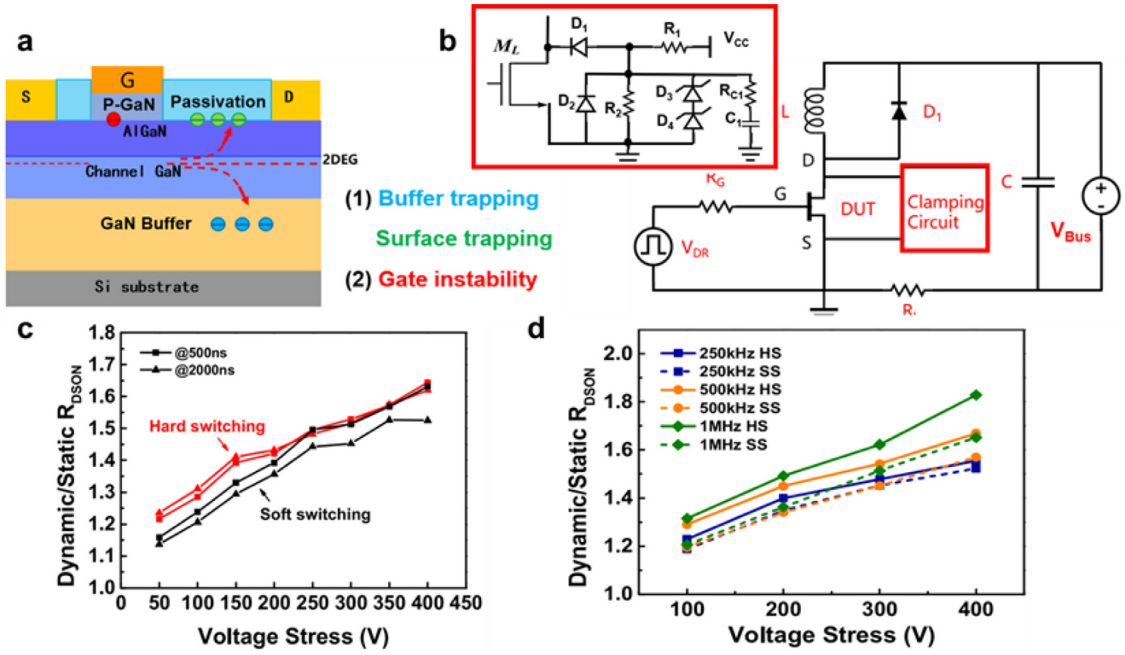

Fig. 8. Issue of dynamic Ron in GaN-based HEMTs. (a) Schematic cross section of p-GaN HEMT and mechanisms of trapping-induced dynamic R_{ON} [50], (b) Double Pulse Tester (DPT) with a clamping circuit (red insert) [51], (c) Dynamic/static R_{ON} with different voltage stresses under hard- and soft-switching modes, and (d) Dynamic/static R_{ON} with different voltage stresses under different switching frequency modes [52].

The dynamic R_{ON} degradation is related to the switching mode of the GaN devices. When under different switching modes, the increase of the R_{ON} is different [52]. Fig 8c shows the R_{ON} increment of a commercial GaN devices under the hard-switching mode is larger than that under the soft-switching mode. When voltage stress is 400 V, R_{ON} is 1.55 to 1.6 times the static resistance. On the other hand, the higher the switching frequency of the device, the greater the increase in R_{ON}. Since GaN devices are widely applied in high frequency switching scenarios, the increase in R_{ON} will lead to additional circuit loss. In addition to V_{DS} and switching frequency, there are many other factors that affect the R_{ON} of GaN devices, such as junction temperature, turn-off voltage, load current, and duty cycle. Therefore, it is necessary to perform characterization analysis and further optimization on GaN devices.

As for optimization methods, buffer stack optimization is a common optimization method, but it is difficult to achieve low dynamic R_{ON} while maintaining high breakdown voltage. Chevtchenko et al. [59] found that there is a tradeoff between the breakdown voltage and dynamic R_{ON}. Würflfl et al. [60] proposed a compromise solution in which AlGaN buffer layers in conjunction with C-doped GaN buffer underneath simultaneously show high breakdown properties and good switching properties. Compared to bulk C-doped buffer layers, the concentration of slowly responding deep traps is much less in device regions adjacent to the channel, resulting in suppression of dynamic R_{ON}.

2.3.2. *Gate reliability*

Gate degradation affects the performance of GaN-based HEMTs temporarily or permanently. The gate performance is measured at the pulse conditions to study the recoverable degradation, while the permanent deterioration can be usually obtained from the DC characteristics. Gate leakage current (I_G), breakdown time (t_B), V_{th} instability, etc., are often measured to evaluate the gate reliability, which is also deeply affected by the gate module concept. When the gate is stressed at a relatively high gate bias, the I_G will vary with the stress time and finally increase abruptly to a large value or even present a final destruction, as illustrated in Fig. 9a. The statistics of t_B often obey to the Weibull distribution (Fig. 9b), which vary with the stress voltages [54]. Through the voltage-dependent distributions, the operation voltage (V_O) can be deduced by exponential or power laws for the gates holding a 10-years lifetime. With exponential fitting, the V_O at a failure rate of 63% is in the range of 7 to 8 V for the p-GaN E-HEMTs (Fig. 9c) [54,61] and approximately16.5 V for the MIS HEMTs with a gate dielectric of LPCVD SiN_x (Fig. 9d) [56].

The mechanism of gate breakdown is widely investigated, and some possibilities have been proposed. In p-GaN E-HEMTs with Schottky gate contact, an equivalent circuit of two back-to-back junctions in series, Schottky junction (J_S) formed by metal/p-GaN structure and P-i-N junction (J_P) by p-GaN/AlGaN/GaN structure shown in Fig. 9e, has been utilized to understand the components of I_G [62]. The gate current components are presented in Fig. 9f. At a positive gate voltage, the J_S is reversely biased and almost dominates the I_G. Defects may generate at the high electric field and the acceptors of Mg will be compensated, which finally results in a failure of J_S thus a high I_G can be detected due to most voltage will then drop on the forward J_P [54]. Another explanation is that the generated defects will form leakage paths through the p-GaN, leading to the abruptly increased I_G. Moreover, the deterioration of AlGaN barrier in J_P is also believed to be one of the possibilities of the gate breakdown. Especially in the Ohmic case, current is allowed to flow through the J_P thus thermal runaway is reasonable for the gate failure [63]. In MIS HEMTs, the gate breakdown is usually attributed to the interface states between the gate dielectric and AlGaN barrier. On another side, the quality of the gate dielectric itself should also be questioned whether it is strong enough to form a low I_G under a high electric field. For instance, the gate breakdown performance of the HEMTs with gate dielectrics of LPCVD SiN_x strongly depend on the SiN_x stoichiometry. Therefore, a bilayer gate dielectric scheme consisting of a Si-rich SiNx interlayer and a high-resistivity SiNx leakage-current-blocking layer has been proposed and not only can suppress the trapping effect but also maintain a low leakage current and large gate swing [58].

The V_{th} instability has a critical impact on the device operation and runs another hot topic in GaN-based HEMTs. Usually, a negative V_{th} shift will present when net positive charges are stored in the gate stack, and a positive V_{th} shift results from the stored net negative charges. The Negative V_{th} shifts can induce a fake ON-operation thus lead to safety risk. On the other hand, positive V_{th} shifts can negatively impact the ON-resistance and the switching time. Therefore, keeping a stable V_{th}

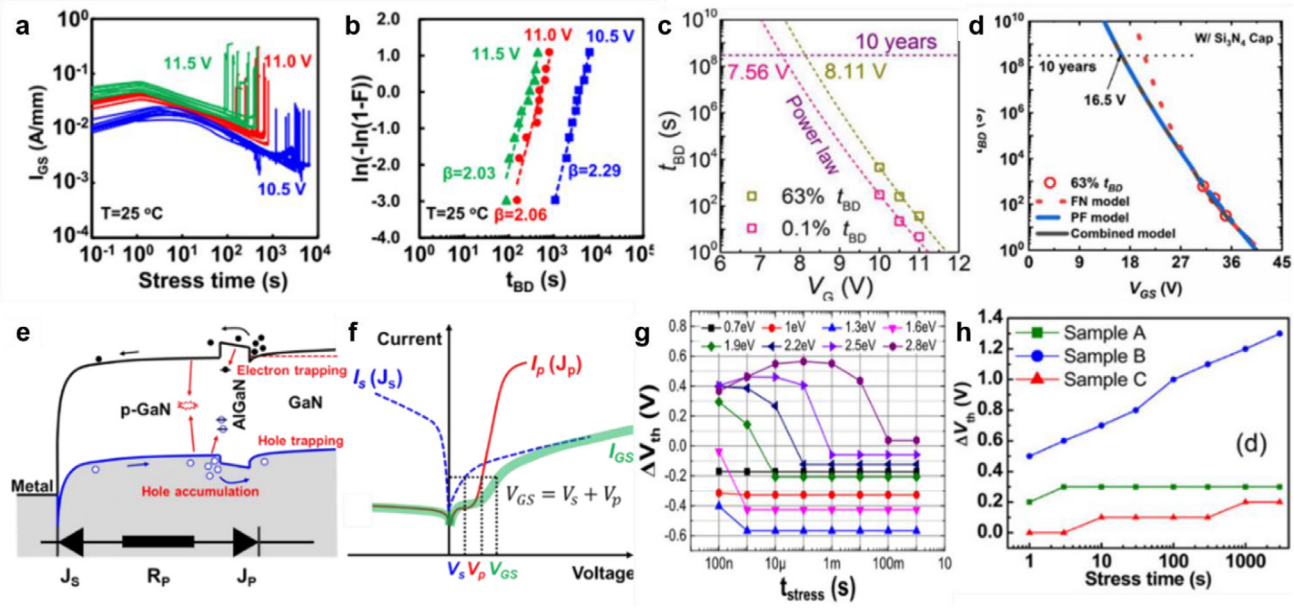

Fig. 9. Issue of gate reliability in GaN-based HEMTs. (a) I_{GS} ~ t curves, (b)Weibull distribution of t_B [54], (c) Lifetime prediction for p-GaN E-HEMTs [55], d, Lifetime prediction for MIS-HFETs [56], (e) Carrier behaviors in p-GaN gate under positive bias, (f) Gate current components [54], (g) V_{th} shifts with stress pulse time in p-GaN E-HEMTs [57], and (h) V_{th} shifts with stress pulse time in MIS-HFETs [58].

no matter in the long-term operation or in the fast switching is urgently desirable for the device application.

In the p-GaN gated E-HEMTs, most V_{th} instabilities after long-term operation are related to defects generation and/or reactivation in the p-GaN, AlGaN layer and/or at the interfaces of the gate stack. For instance, defects generated in the depletion region of the J_S, close to the metal interface with high electric field strength (*E*), will compensate the Mg acceptors as negative charges store in this region [54]. Finally, a positive V_{th} shift can be observed. The dynamic V_{th} instability in p-GaN gated E-HEMTs, which is usually investigated by means of double pulse measurement, strongly depends on the gate energy band structure. The J_S and J_P obviously affect the carriers transport behaviors through the gate (Fig. 9e). The balance between hole tunneling current through the Schottky barrier and the thermionic current across the AlGaN barrier results in a variation of the total charge stored in the p-GaN, thus, in a V_{th} shift [57], as illustrated in Fig. 9g. It is worthy to point out that the V_{th} shift can be negative and/or positive for p-GaN E-HEMTs because the charge storage in J_S and J_P will vary with the voltage, pulse time, Schottky barrier height, etc.

The MIS HEMTs usually present a positive long-term V_{th} shifts due to electron trapping in the gate dielectric and/or at the interface with assistance of a relatively high electric field. To suppress the trapping effect, some interlayers, such as in-situ SiN_x, oxides, and Si-rich SiN_x, are introduced and significant improvement has been observed. As shown in Fig. 9h), ΔV_{th} after stressing for 10^4 s has reduced from 1.2 V for the device with high-resistivity SiN_x to 0.3 V for that with Si-rich SiN_x inserted between the AlGaN and high-resistivity SiN_x [58]. The positive V_{th} shift in MIS HEMTs is also observed in high-base down-sweep pulse-mode measurement. A +0.84 V hysteresis is obtained as the base voltage rises from 3 to 15 V. It suggests that the dynamic V_{th} instability is also challengeable for the MIS HEMTs.

2.3.3. Other reliability issues in GaN HEMT

Recently, due to fast development of GaN-based HEMT, its reliability studies are more interested in the device robustness and industrial devices. Issues like dynamic breakdown voltage (BV), surge energy robustness, and short-circuit robustness are widely studied in current years.

Dynamic BV, which is a hot topic in GaN HEMT, has been found to be influenced by the bulk traps, showing higher value than the static BV and an increasing tendency with the reduced pulse width [64,65]. A developed method based on the unclamped inductive switching (UIS) tests reveals that the dynamic BV can provide GaN HEMTs additional overvoltage and surge energy margin in power applications. However, the recently commercialized GaN HEMTs still have no or very little avalanche capability, due to the lack of p-n junctions between source and drain that can extract the holes during impact ionization.

Another emerging issue is the short-circuit capabilities [68], which prevent the GaN HEMT applications into high-level markets, e.g., electric vehicle powertrains. In most applications, E-mode HEMTs can suffer from extreme operating conditions that result in a short-circuit fault, which needs properly designed protection circuit. Thus, to be the first, a careful measurement and a full analysis of the short-circuit behavior are desirable.

2.4. Common issues in fabrication of GaN-based lateral devices

In the fabrication of GaN-based lateral power devices, some other common issues draw much attention to improve the device performance. As the on-state losses and off-state withstand voltages are critically important for the power devices, the lowering of Ohmic contact resistance and suppression of peak electric field strength are two momentous aspects, which will be discussed in this section.

2.4.1. Ohmic contact

In order to minimize the specific R_{on} and, hence, the power losses of the system, the resistance of Ohmic contacts, which provide the link from the device to the external circuitry and vice-versa, must be negligible with respect to that of the device drift layer. In the GaN based HEMTs, the source-drain Ohmic contacts are formed on the AlGaN/GaN heterostructure. The most straightforward approach is that transfer the metal schemes already used for n-type GaN to the AlGaN/GaN system. Particularly, some important factors should be considered. For instance, AlGaN is a material with wider bandgap than GaN, and it is usually an undoped layer, thus the formation of Ohmic contact on the AlGaN/GaN heterostructure may be more difficult than that on the n-type GaN.

The most metal stack used in the AlGaN/GaN based HEMTs is Ti/Al/*x*/Au (*x* = Ni, Ti, Mo, Pt, ……), which is annealed at the temperature usually higher than 800 °C to form Ohmic contact with low

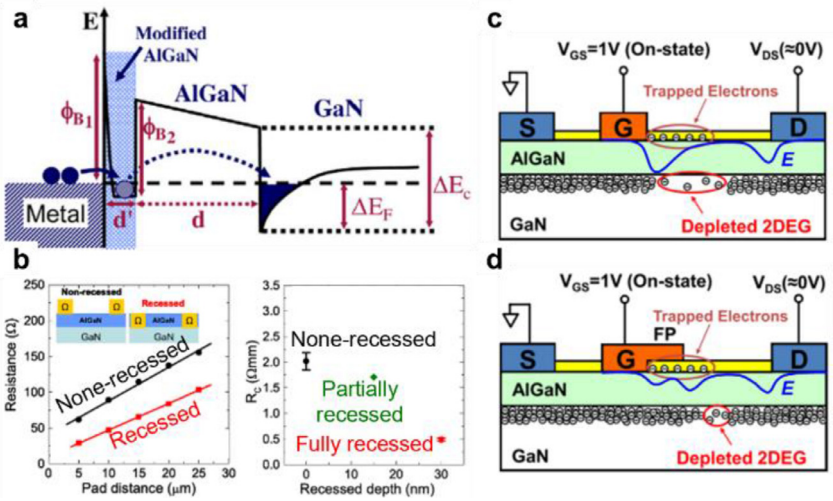

Fig. 10. Common issues in fabrication of GaN-based HEMTs. (a) Schematic band diagram to describe the mechanism of current transport in Ohmic contacts to AlGaN/GaN heterostructures [66], (b) Resistance of the Ohmic contact for AlGaN/GaN heterostructure with AlGaN barrier non-, partially-, and fully- recessed [66]. And 2DEG and Electric field distributions for HEMT (c) w/o field plate, and (d) w/ field plate [67].

resistivity in the range of 10^{-5} ~to 10^{-6} Ω·cm^2 [66]. Moreover, as indicated in Fig. 10a, the Al component and thickness of the AlGaN barrier are also strongly affect the contact resistivity (ρ_c). It is worthy to point out that forming the Ohmic contact at a high annealing temperature might bring some compatibility issues in the fabrication of GaN-based HEMTs, especially the E-mode types.

Therefore, Ohmic contacts formed at low annealing temperature, typically, 500 to 600 ˚C, are widely studied together with the topic of C-MOS compatible processes [71]. Au-free metal stacks like Ti/Al/Ti/TiN are commonly deposited on the recessed source and drain region with a few nanometers AlGaN barrier residual or even fully etched. In this approach, contact resistivity keenly depends on the AlGaN barrier thickness, Ti/Al ratio, etc. And the contact resistance can be reduced to approximately 0.5 Ω·mm if the AlGaN barrier is fully recessed (Fig. 10b). In most cases, Ti is believed to enhance the formation of TiN islands thus increase the generation of N-vacancies acting as donor states below the contact.

2.4.2. *Suppression of peak E*

In power devices at OFF-state, the electric fields at the edge corners are strong thus leakage current will increase with some assistant effects, i.e., tunneling effect, which will finally cause a breakdown phenomenon. On another side, the defects will be easily charged or discharged in the devices at the high electric field, resulting in a switching lag if they were hardly recovered into the initial states. Therefore, suppression of the peak electric field is of great importance to improve the device performance.

For electronic devices, the peak electric field commonly lies in the semiconductor at the metal edge, thus, some edge termination techniques, e.g., field plate termination, have been proposed to effectively improve the device BV. And the situation for transistors goes complicated due to much more sophisticated device structure. In GaN HEMTs shown in Fig. 10c, the electric field (blue line) usually peaks at the gate edge in drain side, which serves as a vortex for the electric field streamlines, and also probably at the drain edge especially in GaN buffer with high density of acceptor-like defects. The peak electric fields at the gate edge also can drive the electrons to the AlGaN surface thus forming a "virtual gate" effect during the fast switching, and finally lead to a deterioration of the dynamic R_{on}.

Naturally, field plates (FPs) have been designed and utilized to moderate the peak *E* in GaN HEMTs. Without any FP, the breakdown field distribution along the 2DEG is confined over a small distance from the gate edge. Inclusion of a FP (Fig. 10d) can reduce and spread the field along the 2DEG thus a moderation of the device failure. Particularly, gate FP and/or source FPs are adopted in many works. In comparison, gate FP is more potential to reduce the peak E and the dynamic R_{on} [67], however, it will bring a relatively high parasitic gate capacitance thus lowering the switching frequency and intensifying switching oscillations. Therefore, source FPs are more common in the most cases, even multiple FPs can be found in some works [72].

3. Outlook

GaN transistors can provide substantial performance improvement in either continuous conduction mode or discontinuous conduction mode at high frequencies. In 600/650 V application, GaN + Si Cascode can offer a 3.3 kW output power with peak efficiencies of > 99%, > 98.5%, and > 98% at frequencies of 100, 200, and 300 kHz, respectively [73]. And the E-mode GaN HEMTs are confirmed to be able to serve a maximum output power of 400 W and a very high power density of 30 W/in^3 with a high frequency of 1 MHz and a conversion efficiency of 96.4% [74]. These evidences strongly prove that superior performance can be achieved with GaN-based power devices. However, it should be stressed that various challenges still exist in the GaN based lateral devices for high-frequency and high-power applications. They still suffer from surface-related current dispersion, poor heat dissipation, high defect densities, and inability to support avalanche breakdown. Moreover, their reliability and stability issues are key constraints for GaN based power devices to step into high-end applications and mass markets.

In this section, new technologies and devices will be introduced for next generation of GaN power devices with superior performance. High switching frequency, high output power density, and high reliability are the strategic research directions which will greatly fulfill the future requirements of power devices.

3.1. *High frequency application*

The parasitic inductances from the interconnection bonding wires and PCB (printed circuit board) traces often create a bottleneck in exploiting the full potential of GaN power devices switching at high-frequencies, since they could induce voltage spikes/oscillations that may lead to various reliability issues [75]. Monolithic integration of GaN integrated circuit (IC) is expected to help unlock the full potential of GaN power electronics, especially in promoting the high-frequency power switching applications. Intensive research efforts have been dedicated

to GaN smart power integration. In 2004, S. G. Fytel et al. reported an AlGaN/GaN MOSFET integrated circuit power converter based on the depletion mode device platform [76]. However, as the threshold voltage is negative, additional negative-voltage-source is indispensible to drive the device, which further complicates the integration. The E-mode GaN HEMT can greatly simplify the design and process complexity of GaN IC and has gradually become the mainstream platform to realize GaN n-channel metal oxide semiconductor (NMOS) integration.

3.1.1. NMOS integration

As discussed in Section 2.2, there are several device technologies for realizing the E-mode GaN HEMT and monolithic integration of GaN ICs, including flurine ion implanted gate, recessed gate and p-GaN gate technology.

The F ion plantation technology for E-mode HEMT was firstly proposed in 2005. Based on this technique, the enhancement/depletion mode (E/D-mode) GaN inverter has been successfully fabricated [77] with an output logic swing of 1.25 V, a logic-low noise margin of 0.21 V and a logic-high noise margin of 0.51 V. The as-fabricated ring oscillator shows a minimum delay of 130 ps/stage at VDD = 3.5 V, and a minimum power-delay product of 0.113 pJ/stage at V_{DD} = 1 V. After that, GaN smart power chip technology, including some key analog functional blocks such as voltage reference generators and comparators, has been demonstrated. The voltage of the reference generators showed an average drift of less than 70 ppm/°C, which could be used as a reference voltage in various biasing and sensing circuits. The positive limiting level of the temperature-compensated comparator was less than 450 ppm/°C drift compared with 1350 ppm/°C in the conventional comparator. The comparator delivered a voltage gain of as high as 132 V and a unity-gain bandwidth of 270 MHz and it is also capable of operating at 250 °C with temperature-compensated bias. Gate recess method has also been commonly adopted in laboratories. Y. Kong et al. reported a monolithic integration of E/D-mode AlGaN/GaN MIS-HEMTs based on gate recess for mixed signal applications in 2014 [81]. The incorporation of gate dielectric provides the inverter with a large logic voltage swing of 3.71 V at a supply voltage V_{DD} of 5 V. The 51-stage ring oscillator implemented with 106 transistors shows an oscillation frequency of 427.6 MHz at V_{DD} = 5 V, corresponding to a stage delay of 23 ps. In addition, GaN-based NAND and NOR logic gates shows very good performance. Ruize Sun et al. [82] reported an Au-free GaN power integration platform and a complete integration scheme from devices to functional sub-circuits and application-oriented GaN converter ICs. The all-GaN converter ICs with monolithically integrated high-side gate driver, pulse width modulation (PWM) feedback controller and over-current protection circuits are proposed. It can realize a stable output of 10 V with constant output ripples below 4% from 15-30 V input line voltage. Stable output with constant ripples can be maintained according to the designed feedback control when the input and load conditions are abruptly changed. When subjected to an over-current incident, the converter IC can be protected according to the desired over-current threshold values within one duty cycle period.

F ion plantation and gate recess works are either based on Schottky-gate HEMTs or metal-insulated-semiconductor (MIS) gate HEMTs, and neither of them have been adopted in commercial GaN power devices yet due to their small gate swing in Schottky-gate HEMTs and their gate-dielectric reliability concerns. The p-GaN gate technology has been proved to decrease the gate leakage and increase the gate voltage swing, and it is already commercially available for its excellent characteristics and stability. Academia and industry have reported intensive research progress on GaN power IC. In 2017, Hong Kong University of Science and Technology and Taiwan Semiconductor Manufacturing demonstrated a monolithic integration of E/D-mode HEMTs on a commercial E-mode GaN power device technology platform [83]. A direct-coupled FET logic (DCFL) inverter is demonstrated with a large input voltage swing and a wide noise margin. A 101-stage ring oscillator has been demonstrated with a propagation delay of approximately 0.1 ns/stage at room temperature and approximately 0.25 ns/stage at 250 °C. Fraunhofer Institute for Applied Solid State Physics reported a 600 V p-GaN Gate Power IC platform [84], in which they presented a 600 V GaN Power IC, combining a large-area power transistor with an intrinsic freewheeling diode, a gate driver, and a temperature and current sensor on-chip. The IC enables unipolar +5 V or bipolar ±5 V. Finally, 390 V/10 A switching transitions and efficiencies up to 98.9% at 350 V, 900 W DC-DC conversions are realized based on this platform. Commercialization of GaN power IC took place relatively early and fast. In 2017, Taiwan Semiconductor Manufacturing showed a smart GaN platform with 2-level integration of peripheral low voltage active and passive devices. They demonstrated four function blocks of the 1st level integration, including control blocks, clock, pre-gate driver and Electronic Static Discharge (ESD) protection. The 2nd level integration has a high-low side integration on a 100 V technology platform and the system efficiency of DC-DC buck converter using such scheme is enhanced with low on-sate resistance and good stability. The same year, Navitas Semiconductor demonstrated an AllGaN™ power IC of 650 V E-mode GaN transistor, driver and logic by monolithic integration [85]. The extremely low gate charge enables a driver loss of < 35 mW at 1 MHz. The device can handle up to 200 V/ns dV/dt and enables resistor programmable slew rate control down to 10 V/ns.

3.1.2. GaN power logic integrated circuits (ICs) development trends

The GaN ICs possesses the advantages of low parasitic parameters, high power density, high operating frequency and so on. If the Complementary Metal- Oxide- Semiconductor Transistor (CMOS) logic ICs can be achieved on GaN HEMT platform, the total performance will be significantly improved. However, conventional GaN HEMTs are mainly N-channel devices. The key obstacle to realize the GaN-based CMOS logic ICs is the performance improvement of GaN P-channel devices. In 2016, R. Chu et al., demonstrated the first GaN CMOS technology, in which an E-mode NMOS with a channel mobility of 300 $cm^2/V{\cdot}s$ was achieved by recessing the AlGaN barrier, and the PMOS with a channel mobility of 20 cm^2/Vs was attained through removing the p-GaN cap layer in the AlGaN/GaN/p-GaN structure [86]. Later, N. Chowhury, et al., fabricated p-channel transistor using the same epitaxial structure as the p-GaN gated n-channel devices [87]. In 2021, Z. Zhang et al., reported the monolithic integration of E-mode n-channel and p-channel GaN field-effect transistors and the fabrication of GaN-based complementary logic ICs [70] (Fig. 11c). The inverters exhibit a rail-to-rail operation, a suppressed static power dissipation, a high thermal stability, and large noise margins. However, the hole mobility is still at a very limited level of approximately 10 $cm^2/V{\cdot}s$, which has a huge mismatch with the electron mobility. Therefore, the improvement of hole mobility is one of the directions to propel the development and innovation of GaN-based monolithic ICs in the future.

Another new trend of GaN-based HEMTs research is the all-GaN power ICs, which require various modules including half-bridge, diode, capacitor, driver, dead-time control, level shifter, PWM, diagnostic and protection, etc. Efforts have been dedicated to integrating single or multiple modules. However, the most challenging issue for the all-GaN ICs on standard Si substrate is the cross-talk and back-gating effect due to the lack of effective isolation. These two problems can be solved by growing GaN on silicon-on-insulator (SOI) substrates technology combined with trench isolation method, by which the HEMTs and their respective Si(111) device layers are fully isolated [88].

3.2. High-power application

Due to the availability of bulk GaN substrates, vertical GaN power devices have been demonstrated with promising performance, such as high current, high voltage, low defect density, good thermal management, small chip area, and avalanche breakdown. A typical vertical GaN power device is composed of a channel/contact layer, a drift layer, a buffer layer, and edge termination. In recent years, the development

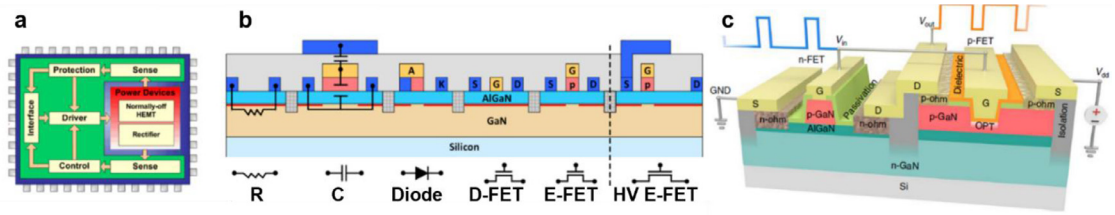

Fig. 11. GaN based monolithically integrated circuit. (a) Schematic of the development for GaN power IC, (b) 650-V GaN power IC platform based on *p*-GaN gate HEMT technology [69], and (c) the perspective view of a GaN-based complementary logic IC based on a commercial p-GaN gate power HEMT platform [70].

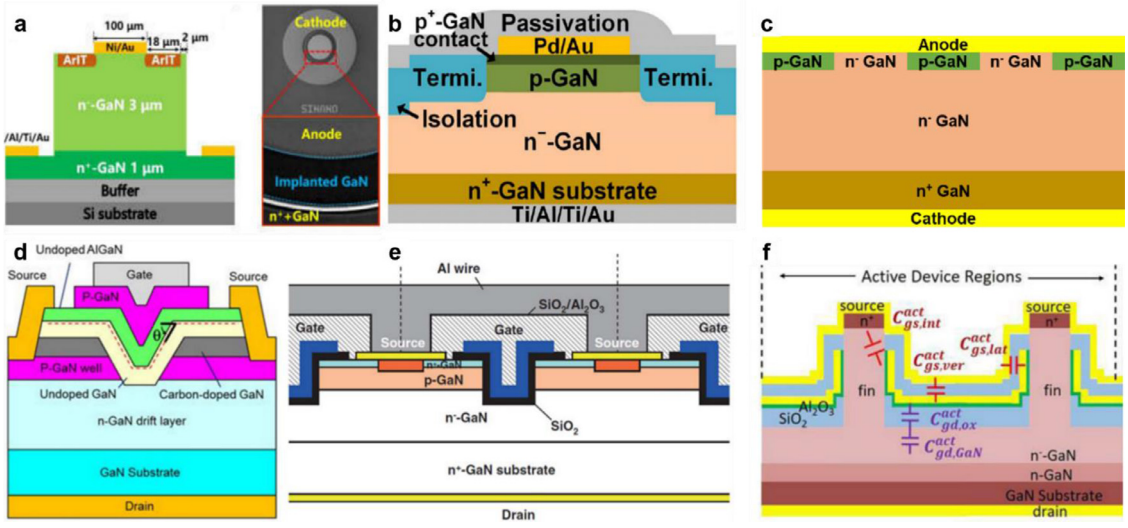

Fig. 12. GaN based vertical power devices. (a) quasi-vertical SBD [78], (b) PIN diode, (c) JBS, (d) CAVET [79], (e) MOSFET [79], and (f) FinFET [80].

of advanced vertical GaN power rectifiers (Fig. 12), including Schottky barrier diodes (SBD), junction barrier Schottky (JBS) rectifiers, P-N diodes, etc., and vertical GaN power transistors, such as current aperture vertical electron transistors (CAVETs), junction field-effect transistors (JFETs), metal-oxide-semiconductor field-effect transistors (MOSFETs), and fin field-effect transistors (FinFETs), has demonstrated the potentials of GaN vertical device for the next generation power applications [79,89,90].

High performance vertical GaN rectifiers have been achieved through optimization of materials epitaxy and device fabrication. Thick drift layer is pursued to reach high breakdown voltages. The stress in GaN materials is well controlled, and the dislocation density is reduced to a relatively low range. Therefore, the thickness of the drift layer in vertical power devices, e.g., SBD, is typically over 10 μm. Another key material challenge is the control of carrier concentration. With a good control of carbon and silicon doping through precise regulation of the epitaxial growth condition, the carrier concentration can be tuned in the low level of approximately 10^{15}/cm^3 [91], which is beneficial for device operation, thus the devices can finally realize high BV and low R_{on}. For device fabrication, many works have focused on the development of effective edge termination techniques, which can mitigate the electric field crowding effects at the device edges, thus enhancing the breakdown voltages [91]. The key edge termination techniques developed in recent years can be summarized as mesa termination, field plates, and ion implantation. The beveled mesa with a lightly doped layer can effectively suppress the electric field crowding, especially in the PIN diodes. And in most cases, the beveled mesa has avoided a very sharp edge where the electric field concentrates, and it is often used together with field plates, which can extend the depletion region along the device surface when reversely biased. Therefore, avalanche breakdown has been observed in the devices with field plates and beveled mesas. Ion implantation is another edge termination technique which is still under development for GaN power devices. The breakdown mechanisms are complex and widely studied. Forming a junction termination extension, a highly resistive region, and a partially compensated edge termination are the main approaches for the ion implantation terminations. With excellent material epitaxy and device fabrication, avalanche breakdown, the indicative of nondestructive repeatable breakdown capability, can be well observed in recent works on the GaN based vertical devices. To further improve the device performance, several advanced GaN power rectifiers were developed to overcome the limitations of basic GaN SBDs and PIN diodes. GaN JBS, merged p-n/Schottky (MPS) rectifiers, and trench metal-insulator-semiconductor barrier Schottky (TMBS) rectifiers have been demonstrated with great performance.

GaN based vertical transistors have also been developed due to their higher current density, and absence of the degradation issue of dynamic R_{on} when compared to the lateral HEMTs. To reach normally off operation, solutions of CAVETs, trench MOSFETs, FinFETs, etc. have been proposed and demonstrated with high threshold voltages and low on-resistance. With a 13-μm-thick GaN drift layer grown on GaN substrate, the vertical trench CAVETs had a breakdown voltage of 1.7 kV, an ON-resistance of 1.0 mΩ•cm^2, and a threshold voltage of 2.5 V [92]. In 2018, the first vertical GaN FinFET was realized by Y. Zhang et al.[80], the BV and specific R_{on} have been demonstrated as 1.2 kV and 1 mΩ•cm^2, respectively [93]. Other vertical devices e.g., JFETs, are also proved to reach superior performance, indicating that GaN based vertical transistors indeed have their own advantages in power applications. It is worthy to point out that all these GaN based vertical devices are still under development, and each technique still has its own issues to solve. For example, the device structures of CAVETs are quite complicated and require significant efforts in epitaxial regrowth.

Most of the reported GaN vertical devices are fabricated on high-quality freestanding GaN substrates, which are still limited by its small size and high cost. Thus, they are currently unsuitable for mass produc-

tion. Thanks to the tremendous progress of the epitaxial growth technology, >10-μm-thick crack-free high-quality GaN can be obtained on Si substrates, giving a great hope for reducing the cost of GaN vertical power devices. The first GaN-on-Si vertical power diodes were demonstrated in 2014, by utilizing the quasi-vertical structure [94]. With an only 1 to 1.5 μm-thick drift region, these diodes exhibited a BV of 200 to 300 V with a R_{on} of 6 to 10 mΩ·cm^2. In 2018, 820 V GaN-on-Si quasi-vertical p-i-n Diodes were achieved by R. A. Khadar et al. [95]. Later in 2019, they successfully fabricated fully vertical GaN-on-Si power MOSFETs with a $R_{on,sp}$ of 5 mΩ·cm^2, and a BV of 520 V [96]. In 2021, X. Guo et al., demonstrated a high BV of 602 V for quasi-vertical GaN-on-Si SBD [78]. With the accelerated research and development pace, it is expected that further progress of GaN-on-Si lateral and vertical power devices will be attained in the foreseeable future.

Declaration of Competing Interest

The authors declare they have no conflicts of interest in this work.

Acknowledgments

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