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## GaN-based power devices: Physics, reliability, and perspectives FREE

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Matteo Meneghini ; Carlo De Santi ; Idriss Abid; Matteo Buffolo ; Marcello Cioni; Riyaz Abdul Khadar ; Luca Nela ; Nicolò Zagni ; Alessandro Chini ; Farid Medjdoub ; Gaudenzio Meneghesso ; Giovanni Verzellesi ; Enrico Zanoni; Elison Matioli 



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## ABSTRACT

Over the last decade, gallium nitride (GaN) has emerged as an excellent material for the fabrication of power devices. Among the semiconductors for which power devices are already available in the market, GaN has the widest energy gap, the largest critical field, and the highest saturation velocity, thus representing an excellent material for the fabrication of high-speed/high-voltage components. The presence of spontaneous and piezoelectric polarization allows us to create a two-dimensional electron gas, with high mobility and large channel density, in the absence of any doping, thanks to the use of AlGaN/GaN heterostructures. This contributes to minimize resistive losses; at the same time, for GaN transistors, switching losses are very low, thanks to the small parasitic capacitances and switching charges. Device scaling and monolithic integration enable a high-frequency operation, with consequent advantages in terms of miniaturization. For high power/high-voltage operation, vertical device architectures are being proposed and investigated, and three-dimensional structures—fin-shaped, trench-structured, nanowire-based—are demonstrating great potential. Contrary to Si, GaN is a relatively young material: trapping and degradation processes must be understood and described in detail, with the aim of optimizing device stability and reliability. This Tutorial describes the physics, technology, and reliability of GaN-based power devices: in the first part of the article, starting from a discussion of the main properties of the material, the characteristics of lateral and vertical GaN transistors are discussed in detail to provide guidance in this complex and interesting field. The second part of the paper focuses on trapping and reliability aspects: the physical origin of traps in GaN and the main degradation mechanisms are discussed in detail. The wide set of referenced papers and the insight into the most relevant aspects gives the reader a comprehensive overview on the present and next-generation GaN electronics.

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## Contents

1 Table of Contents		6 Lateral GaN transistors: technology and operation	13
2 Introduction	2	6.1 Lateral GaN device architectures	14
3 Gallium nitride: properties and physical parameters	4	6.2 Approaches for normally-off operation	16
4 Polarization charges in GaN	7	6.2.1 Cascode configuration	16
5 Band diagrams and charge density in AlGaN/GaN heterostructures	8	6.2.2 Recessed gate MISHEMT	17
		6.2.3 The fluorine-treated HEMT	17
		6.2.4 P-GaN Gate	18

6.2.5 Tri-gate	19	9.5.5 Other ionizing species	75
6.2.6 Commercial perspective	20	10 Conclusions	75
6.3 Breakdown mechanisms	20	11 Acknowledgments	76
6.4 Ways to improve the breakdown voltage	21	12 Reference	76
6.4.1 Field plate structures	21		
6.4.2 Buffer optimization: Super-lattice buffer	22		
6.4.3 Local substrate removal	23		
6.5 Future perspectives	23		
6.5.1 AlGaN channel HEMTs	25		
6.5.2 Multi-channel devices	26		
6.5.3 Super Junctions	27		
6.5.4 N-polar GaN HEMTs	28		
7 Vertical GaN device structures	29		
7.1 Why Vertical GaN?	29		
7.2 Choice of substrate:	30		
7.3 Vertical device architectures:	30		
7.3.1 Development of vertical devices on sapphire and bulk	30		
GaN	30		
7.4 Open Challenges:	45		
8 Charge-trapping processes in GaN transistors	46		
8.1 Traps and deep levels in GaN	47		
8.2 Trapping mechanisms	47		
8.3 Surface traps in the gate-drain access region	47		
8.4 Barrier traps	49		
8.5 Buffer traps	49		
8.6 Gate-dielectric traps	49		
8.7 Trapping effects	51		
8.7.1 RF current collapse	51		
8.7.2 Dynamic $R_{ON}$ increase	51		
8.7.3 Threshold-voltage instabilities in isolated-gate	52		
and p-GaN transistors	52		
8.7.4 “Kink” effect	53		
8.8 Traps characterization techniques	53		
8.8.1 Pulsed IV	54		
8.8.2 DLTS/DLOS	55		
8.8.3 Current transients	56		
8.8.4 On-the-fly characterization	56		
8.8.5 Interface trap characterization by means of C-V	57		
and G-V measurements	57		
8.8.6 Photoluminescence (PL)	58		
9 Degradation processes in GaN devices	60		
9.1 ON-state	61		
9.1.1 Extrinsic degradation: the role of dielectrics	61		
9.1.2 Degradation of p-GaN gate stacks	62		
9.1.3 Vertical devices	64		
9.1.4 RF stress	65		
9.2 OFF-state	66		
9.2.1 Extrinsic degradation: the role of dielectrics	66		
9.2.2 Degradation of GaN stacks	67		
9.3 SEMI-ON-state	71		
9.4 Electrostatic discharges and electrical overstress	73		
9.5 Radiation hardness	74		
9.5.1 Proton irradiation	75		
9.5.2 Neutron irradiation	75		
9.5.3 Electron irradiation	75		
9.5.4 Gamma ray irradiation	75		

## I. INTRODUCTION

Over the past decade, gallium nitride (GaN) has emerged as an excellent material for the fabrication of power semiconductor devices. Thanks to the unique properties of GaN, diodes and transistors based on this material have excellent performance, compared to their Si counterparts,<sup>1</sup> and are expected to find wide applications in the next-generation power converters. Owing to the flexibility and the energy efficiency of GaN-based power converters, interest toward this technology is rapidly growing: the aim of this Tutorial is to review the most relevant physical properties, the operating principles, the fabrication parameters, and the stability/reliability issues of GaN-based power transistors. For introductory purposes, we start summarizing the physical reasons why GaN transistors achieve a much better performance than the corresponding Si devices to help the reader understanding the unique advantages of this technology.

The properties of GaN devices allow for the fabrication of high-efficiency (near or above 99%),<sup>2–6</sup> kW-range power converters. Such converters can have switching frequencies above 1 MHz,<sup>7,8</sup> and—through proper design, integration and/or hybrid GaN/CMOS manufacturing—frequencies as high as 40–75 MHz can be reached.<sup>9,10</sup> High-frequency operation permits us to substantially reduce the size and weight of inductors and capacitors, thus resulting in a compact converter design. Further innovation will come from the design of monolithically integrated all-GaN integrated circuits (ICs): specific platforms, such as GaN on silicon-on-insulator (SOI) can be used for the fabrication of fully integrated power converters, containing smart control, pulse width modulation (PWM) circuitry, dead time control, and half bridge.<sup>11,12</sup> Such solutions, which can be tailored for switching in the 1–10 MHz range, can reach very short turn ON/OFF times, which are considerably smaller than in discrete gate drivers.<sup>12</sup> The availability of fast, small, efficient, and lightweight power converters can be particularly beneficial in the fields of portable/consumer electronics, automotive, and avionics.

GaN is a wide-bandgap (WBG) semiconductor and has an energy gap of 3.4 eV.<sup>13</sup> This allows GaN devices to be operated at extremely high temperatures, thus substantially increasing the maximum power density that can be dissipated on a device, or permitting the use of light and small heat sinks. Over the last few decades, several reports on the high temperature and stable operation of GaN high-electron mobility transistors (HEMTs) have been published. Temperatures above 400–500 °C<sup>14–16</sup> have been reached and, for selected InAlN/GaN devices, up to 900 °C.<sup>16</sup> Operation at high temperature is a first, substantial, advantage of GaN devices, compared to Si-based metal–oxide–semiconductor field-effect transistors (MOSFETs), that are typically rated for maximum operating temperature of 125–150 °C.

A second advantage of GaN arises from its high breakdown field (3.3 MV/cm<sup>13</sup>), which is 11 times higher than that of Si (0.3 MV/cm). The direct consequence of such a high critical field is

that for withstanding a given voltage, a layer of GaN can be 11 times thinner than its Si counterpart, with consequent beneficial impact on resistivity. As a consequence, the use of GaN switches can substantially reduce the resistive losses in switching mode power supplies (SMPSS).

A third aspect to be considered is the high mobility of the channel; as will be discussed in Secs. III–V, GaN transistors are typically heterostructure devices. A high mobility (up to  $2000 \text{ cm}^2/\text{Vs}$ <sup>13</sup>) channel can be obtained through the formation of a two-dimensional electron gas (2DEG) at the heterointerface between the AlGaN barrier and the GaN channel layer. Such high mobility, along with the large saturation velocity ( $2.5 \times 10^7 \text{ cm/s}$ ), further contributes to reduce the resistivity of the devices. FETs based on AlGaN/GaN heterostructures are usually referred to as high-electron mobility transistors (HEMTs), or heterojunction field-effect transistors (HFETs).

At present, GaN devices are commercially available, and several products have been proposed, in three main voltage ranges: (a) low/mid-voltage ( $V_{DS,\max} < 200 \text{ V}$ ) devices find applications in dc–dc power converters, motor drives, wireless power transfer, LiDAR and pulsed power applications, solar micro-inverters, class D audio amplifiers, robotics, and synchronous rectification. Such devices can have ON-resistances below  $2 \text{ m}\Omega$  (for drain currents up to  $90 \text{ A}$ ),<sup>17</sup> or up to  $100\text{--}200 \text{ m}\Omega$  (for operating currents in the range  $0.5\text{--}5 \text{ A}$ ), depending on the final application.<sup>18,19</sup> (b) High voltage ( $V_{DS,\max}$  up to  $650 \text{ V}$ ) finds applications in telecommunication servers, industrial converters, photovoltaic inverters, servo motor control,<sup>20</sup> lighting applications,<sup>21</sup> power adapters, converters for consumer electronics,<sup>21</sup> class D amplifiers,<sup>22</sup> and datacenter SMPS.<sup>23,24</sup> (c) Devices with ultrahigh voltage ( $V_{DS,\max}$  above  $1 \text{ kV}$ ). At present, no kV-range transistor based on GaN is commercially available. Commercial transistors with highest voltage rating have a maximum voltage of  $900 \text{ V}$  (see, for example, Ref. 25) and are expected to find application in data communication systems, industrial application, motor control, and photovoltaic inverters. As will be discussed in the article, several research papers demonstrated the feasibility of GaN transistors with breakdown voltages (BVs) above  $1 \text{ kV}$ <sup>26–28</sup> and proposed possible fabrication processes to

target this voltage range. kV-range GaN transistors will compete with SiC-based devices in the industrial, automotive, and photovoltaic application environments.

As will be described in detail in the paper, current GaN devices have typically a lateral layout. Several key aspects related to device design, fabrication, and performance must be discussed in detail to understand how the performance of the transistors can be optimized through careful device design: this will be done extensively in Secs. III–VI of this paper. For introductory purposes, we remind here that in a HEMT, current flows between drain and source through a two-dimensional electron gas (2DEG), which is formed at the heterointerface between an AlGaN barrier and a GaN layer. Figure 1(a) reports the schematic structure of a GaN-based HEMT, showing the main layers that constitute the structure. Power GaN devices are typically grown on a Si substrate to minimize cost and maximize yield. Growing GaN on a Si substrate is particularly complicated, due to (a) the large mismatch of the in-plane thermal expansion coefficient ( $2.6 \times 10^{-6} \text{ K}^{-1}$  for Si and  $5.59 \times 10^{-6} \text{ K}^{-1}$  for GaN<sup>29</sup>), that may lead to cracking of the GaN layer during the cooling-phase after the epitaxial growth; (b) the large lattice mismatch [around 16% for Si (111)]<sup>30,31</sup> that may result in the propagation of dislocations through the GaN epitaxial layers, with consequent defect generation. A careful optimization of the buffer is needed in order to limit the propagation of such defects toward the 2DEG region; Fig. 1(b) reports a cross-sectional SEM image of the epitaxial layers of a GaN-based transistor. As can be noticed, the use of a step-graded buffer in combination with an AlN nucleation layer is used to release the strain and prevent the formation/propagation of dislocations.

The lateral structure described in Fig. 1 may have some limitations, when extremely high breakdown voltages and/or power densities are targeted. First, in a lateral transistor, the breakdown voltage scales with the gate–drain (G–D) spacing. Thus, devices with a high breakdown voltage can be fabricated but will be more resistive and will use a wider semiconductor area, thus resulting in a higher device cost. Second, the density of electrons in the 2DEG can be strongly influenced by surface charges: for this reason, the performance of the final devices is strongly dependent on the process and

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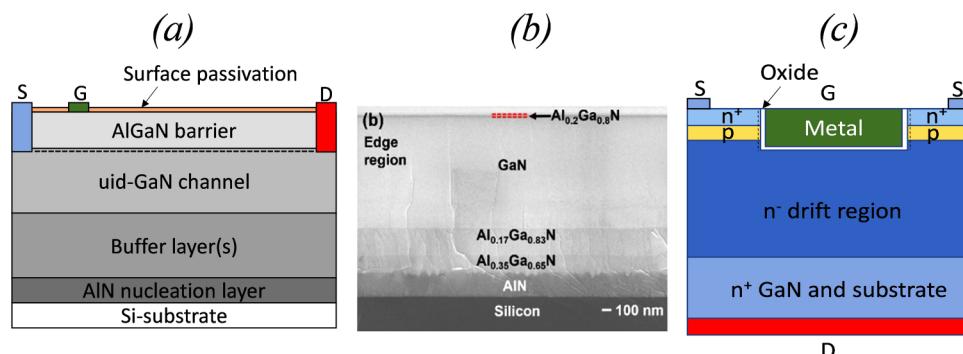


FIG. 1. (a) Schematic representation of the structure of a lateral GaN high-electron mobility transistor (HEMT). The main layers constituting the structure are shown, as well as the three contacts of source (S), gate (G), and drain (D). (b) Cross-sectional SEM images of the epi-structure of GaN HEMT on Si. Reproduced with permission from Cai *et al.*, Materials 11(10), 1968 (2018). Copyright 2018 by the authors of the cited paper, licensed under a Creative Common Attribution CC BY 4.0 License.<sup>32</sup> (c) Schematic representation of a vertical GaN trench MOSFET.

backend. To solve the limitation of GaN lateral devices, vertical device structures are currently being explored and investigated, in line with what has been done with Si and SiC components. In a vertical device [see a schematic structure in Fig. 1(c)], current flows through the bulk of the material, thus allowing high current and power densities. The density of electrons in the channel is modulated through a metal–oxide–semiconductor (MOS) stack, and a p-type body is usually employed to shift the threshold voltage toward more positive values. The breakdown voltage of a vertical GaN transistor depends on the thickness of the lightly doped drift region and not on the size and area of the device as in a lateral transistor. Vertical GaN devices represent the latest development in GaN technology, and the reader will find interest in the related concepts and applications, described in this paper.

As for every technology, there are some physical processes that may limit the performance and the reliability of GaN devices. The ON-resistance of a GaN transistors (and thus the density of electrons in the 2DEG) strongly depends on the intrinsic (spontaneous and piezoelectric) polarization charges of GaN, as well as on the presence of charges trapped at surface states (e.g., in the passivation layer or at the interface between the passivation layer and the AlGaN barrier) or in buffer states. For this reason, it is of fundamental importance to know and manage the surface- and buffer-related trapping phenomena that may limit the dynamic performance of GaN transistors, leading to a recoverable increase in ON-resistance (dynamic  $R_{ON}$  problem). Trapping in the epitaxial layers and/or at the gate stack may result in positive- or negative-bias threshold instability (PBTI or NBTI), and the related processes must be investigated and understood to be able to fabricate fast and reliable devices.

Finally, GaN-based transistors are operated at field, temperature, and frequency levels, which are unimaginable for conventional Si devices. Electric fields can be in excess of 3 MV/cm, and channel temperatures can be above 300 °C during operation, if lightweight heat dissipators are used. Such conditions may favor sudden or time-dependent breakdown phenomena, leading to the failure of the devices. Furthermore, operation at high frequencies may exacerbate the degradation processes related to hard-switching events. For this reason, it is of utmost importance to understand the degradation processes of GaN power devices and to identify ways and strategies for improving the robustness of the components.

This Tutorial presents a detailed overview on the physics, performance, and reliability of GaN-based power devices. In Secs. II–IV, the properties and physical parameters of GaN are discussed to help the reader understand the unique advantages offered by GaN compared to other semiconductors. The main figures of merit (FOMs) for high speed (Johnson FOM) and high power (Baliga FOM) devices are also introduced. Finally, the properties of AlGaN/GaN heterostructures and the related band diagrams are described in detail, and first-order formulas for the calculation of sheet electron charge and threshold voltage are introduced. In Sec. V, the properties, structure, and characteristics of lateral GaN devices are discussed. Specific details are given to the various approaches for normally off operations, to the main device parameters, and to the optimization of the buffer. A perspective on AlN-based devices and on possible strategies to increase the breakdown voltage is given, also by discussing devices with local substrate removal (LSR). Section VI deals with GaN vertical devices.

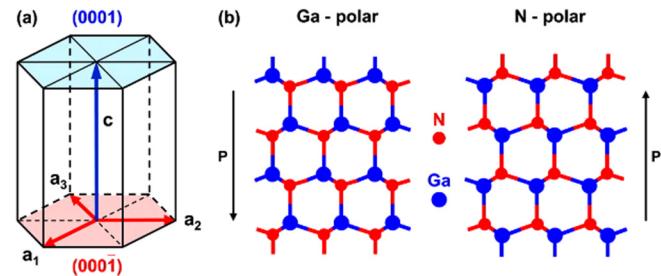
First, the advantages of vertical GaN transistors are described. Attention is then given to the choice of the substrate (GaN-on-GaN vs GaN-on-Si) for vertical device manufacturing. Then, the various vertical device architectures are discussed and compared, in terms of performance and structural parameters. In Sec. VII, the stability of GaN devices is analyzed in detail. Specific focus is given to the role of surface traps, barrier traps, and buffer traps in modifying the main device parameters to present a clear overview of the topic. A complete overview of the dominant defects and deep levels in GaN is given in Sec. VII A to provide an exhaustive view of the problem. Finally, Sec. VIII describes the most relevant degradation processes that can limit the lifetime of GaN-based transistors. Specific attention will be given toward the degradation mechanisms induced by exposure to OFF-state stress, SEMI-ON-state regime, and ON-state degradation (with focus on gate reliability for p-GaN and insulated-gate devices).

Through a pedagogical approach, this paper helps the reader to understand the advantages of GaN technology and get familiar with the main performance, design, and reliability aspects.

## II. GALLIUM NITRIDE: PROPERTIES AND PHYSICAL PARAMETERS

GaN, along with its InGaN and AlGaN alloys, represents an excellent material for both optoelectronics and electronics. In the early GaN era, the research efforts on GaN have been driven by the need of fabricating high-efficiency short-wavelength (blue/violet) LEDs. GaN has a direct bandgap of 3.4 eV, thus being ideal for manufacturing ultraviolet optoelectronic devices. In addition, the energy gap of III-N alloys can be tuned between the 0.7 eV of InN and the 6.2 eV of AlN, thus, in principle, allowing fabrication of LEDs with ultraviolet (UVA, UVB, UVC), visible, and infrared emission.

Contrary to other semiconductors, like InP or GaAs, III-N semiconductors typically have a wurtzite crystal, with its characteristic hexagonal shape (see Fig. 2). It can be easily understood that this lattice arrangement does not have an inversion plane perpendicular to the c axis (0001) and, for this reason, the surfaces have either atoms from group III (In, Ga, Al) or nitrogen atoms.<sup>33</sup> The nature of the surfaces has a fundamental importance, since it



**FIG. 2.** (a) Hexagonal unit cell and (b) atomic structure of Ga- and N-polar GaN. The arrows represent the direction of the spontaneous polarization dipole,  $P$ , in the GaN crystal. Reproduced with permission from Keller *et al.*, Semicond. Sci. Technol. **29**(11), 113001 (2014). Copyright 2014, IOP Publishing. All rights reserved.<sup>34</sup>

## REFERENCIA 36 TABLA

**TABLE I.** Main material parameters for GaN, as compared with other semiconductors. Reported parameters are energy gap ( $E_G$ ), relative dielectric permittivity ( $\epsilon_r$ ), electron mobility ( $\mu$ ), critical electric field ( $E_{crit}$ ), electron saturation velocity ( $v_s$ ), and thermal conductivity ( $\kappa_{th}$ ). Data are taken from Fay et al.<sup>36</sup>

Material	Si	GaAs	4H-SiC	GaN	b-Ga <sub>2</sub> O <sub>3</sub>	Diamond	AlN
$E_G$ (eV)	1.12	1.42	3.23	3.4	4.9	5.5	6.2
$\epsilon_r$	11.7	12.9	9.66	8.9	10	5.7	8.5
$\mu$ (cm <sup>2</sup> /V s)	1440	9400	950	1400	250	4500	450
$E_{crit}$ (MV/cm)	0.3	0.4	2.5	3.3	8 <sup>a</sup>	10 <sup>a</sup>	15 <sup>a</sup>
$v_s$ ( $\times 10^7$ cm/s)	1	0.9	2	2.4	1.1	2.3	1.4
$\kappa_{th}$ (W/cm K)	1.3	0.55	3.7	2.5	0.1–0.3	23	2.85

<sup>a</sup>Estimated: The critical electric field of GaN is taken from Ref. 13. Note that for GaN mobility values up to 2000 cm<sup>2</sup>/Vs are reported, see, for instance, Ref. 13.

determines the polarity of the polarization charges, as will be discussed in the following.

Table I reports the main parameters of GaN, as compared with other semiconductor materials, including Si, GaAs, SiC, AlN, diamond, and Ga<sub>2</sub>O<sub>3</sub>. The materials are ordered with increasing energy gap  $E_G$ , from left to right. Excluding the three semiconductors for which commercial devices are not available (gallium oxide, diamond, and aluminum nitride), GaN is the semiconductor with the largest energy gap, the largest critical field, and the highest saturation velocity. As a consequence, it is an ideal candidate for the fabrication of power semiconductor devices, capable of operating at high temperature and voltage levels.

Figure 3(a) reports the relation between breakdown field and energy gap for the semiconductor materials in Table I. As can be noticed, breakdown field has a power-law dependence on the energy gap, in the form  $E_{crit} \propto E_G^{2.3}$ . This dependence is consistent with previous reports in the literature<sup>35</sup> and demonstrates the great advantage of using wide-bandgap semiconductors for fabricating electron devices with high breakdown voltage.

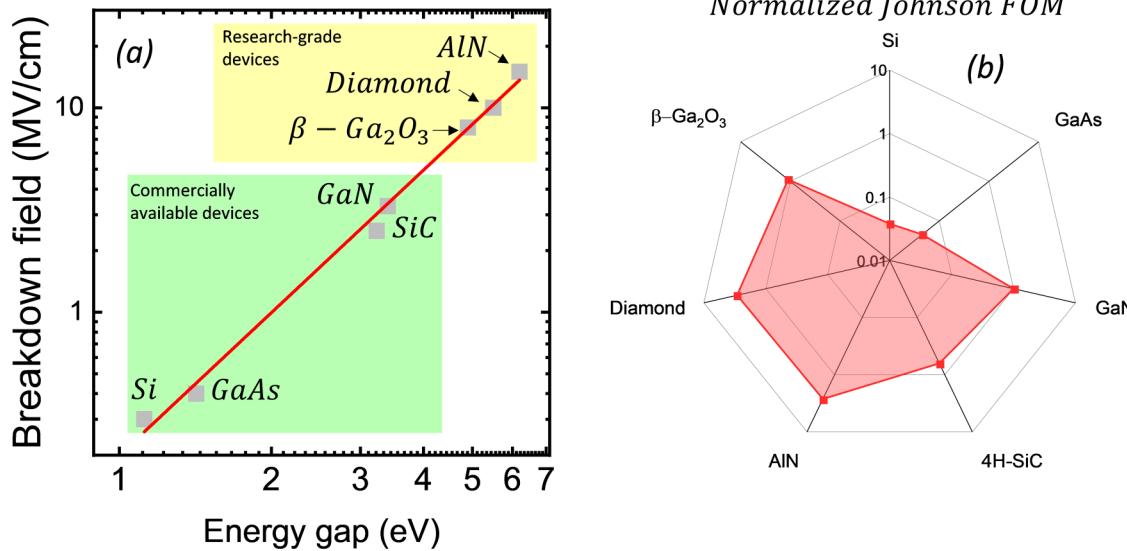
Since a single parameter does not fully describe the properties of a material, semiconductors are typically compared by using figures of merit: the most commonly used are the Johnson FOM, for high-speed devices, and the Baliga FOM, for high power devices. With regard to the first, it is defined as the product of the maximum voltage and the maximum transit frequency, for a given value of the drain-source spacing (see details in Ref. 36), i.e., as

$$\text{Johnson FOM} = f_T V_{DS,\max} = \frac{E_{crit} v_s}{2\pi}. \quad (1)$$

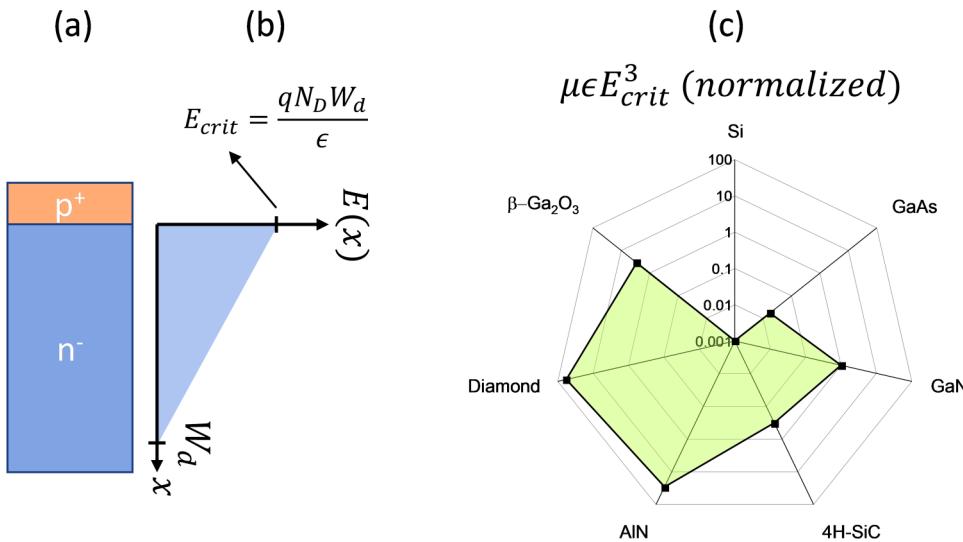
The Johnson figure of merit indicates that, in general, devices with high breakdown voltage are typically slower than devices with lower voltage rating.

Figure 3(b) reports the values of the Johnson figure of merit for the semiconductors listed in Table I; all values are normalized to that of GaN to allow for an easy comparison. As can be noticed, the Johnson FOM of GaN is slightly higher than that of SiC (0.556), comparable to β-Ga<sub>2</sub>O<sub>3</sub> (0.978), and is much larger than that of Si (0.0379) and GaAs (0.0455). AlN and diamond are better than GaN, but their Johnson FOMs are between 2.5 and 3, thus having the same order of magnitude of GaN. While there is a substantial advantage by moving from Si/GaAs to GaN, the

19 January 2025 21:33:19



**FIG. 3.** (a) Dependence of breakdown field on energy gap for the semiconductor materials in Table I. (b) Johnson figure of merit for the same set of semiconductors. All values are normalized to GaN to allow an easy comparison. Data are taken from Table I.



**FIG. 4.** (a) Schematic representation of a unilateral abrupt p+/n<sup>-</sup> junction; (b) approximated electric field profile for the junction in (a); and (c) Baliga figure of merit (calculated as  $\mu\epsilon E_{crit}^3$ ) for the same set of semiconductors in Table I. All values are normalized to GaN to allow an easy comparison. Data are taken from Table I.

19 January 2025 21:33:19

improvement obtained by changing to AlN and diamond is only incremental, in terms of the Johnson FOM.<sup>36</sup>

While the Johnson FOM allows us to compare semiconductor materials for the fabrication of high-speed devices, the Baliga FOM has been introduced to compare semiconductors for application in power electronics. Considering a unilateral and abrupt (e.g., p<sup>+</sup>/n<sup>-</sup>) junction, as depicted in Fig. 4(a), the electric field profile at the n-side has a triangular shape [Fig. 4(b)], and—at the critical electric field E<sub>crit</sub>—the space charge region has a width equal to

$$W_d = \epsilon_{r,GaN} \epsilon_0 E_{crit} / q N_D, \quad (2)$$

where N<sub>D</sub> is the donor density at the n-side of the diode and  $\epsilon_{r,GaN} \epsilon_0$  is the product between the relative permittivity of GaN and the permittivity of vacuum. The breakdown voltage is, therefore,

$$V_{br} = \frac{1}{2} E_{crit} W_d = \frac{1}{2} \frac{E_{crit}^2 \epsilon_{r,GaN} \epsilon_0}{q N_D}. \quad (3)$$

The resistance R<sub>ON</sub> of the n-type semiconductor region is proportional to  $W_d/\mu N_d$ , so we can calculate<sup>37</sup>

$$R_{ON} \propto \frac{W_d}{\mu N_D} \propto \frac{W_d^2}{\mu \epsilon_{r,GaN} \epsilon_0 E_{crit}} \propto \frac{4 V_{br}^2}{\mu \epsilon_{r,GaN} \epsilon_0 E_{crit}^3}. \quad (4)$$

The denominator of the last term is linked to the Baliga FOM<sup>38,39</sup> (that was initially defined as  $\mu\epsilon E_G^3$ ) and identifies the material parameters that help minimizing the conduction losses in power transistors. This FOM is defined based on the assumption that power losses only originate from the ON-resistance of the FET. For this reason, it applies at relatively moderate frequencies, where conduction losses are dominant.<sup>38</sup> For higher frequency devices, one would have to consider also the contribution of switching losses. Figure 4(c) reports the Baliga figure of merit (calculated as

$\mu\epsilon E_{crit}^3$ ) for the same set of semiconductors in Table I. All values are normalized to GaN: the plot indicates that the Baliga FOM of GaN is substantially larger than those of Si and GaAs, higher than SiC, similar to the one of gallium oxide. Diamond and AlN (ultra-wide-bandgap semiconductors) have a much higher Baliga FOM and can be considered interesting alternatives to further push the limits.

The dependence of the bandgap of GaN on temperature follows the Varshni relation

$$E_G(T) = E_{G,0} - \frac{\alpha T^2}{T + \beta}. \quad (5)$$

For GaN, AlN, and InN the related parameters are summarized in Table II. As can be noticed, by using alloys of GaN, AlN, and InN, it is possible to vary the bandgap of the alloy in a wide range, from 0.7 to 6.2 eV. In most cases, GaN transistors are based on AlGaN/GaN heterostructures, and AlN and AlGaN layers are used as nucleation and buffer layers, respectively. InAlN devices have also been investigated: lattice matched InAlN/GaN HEMTs allow an efficient down-scaling of the transistor dimensions, thus allowing to reach high cutoff frequencies.<sup>40</sup>

For ternary alloys, such as AlGaN and InGaN, the bandgap deviates from the Vegard's rule and follows the empirical

**TABLE II.** Bandgap and Varshni parameters for GaN, AlN, and InN. For GaN, results data are taken from Ref. 43, for AlN from Ref. 44, and for InN from Ref. 45.

	E <sub>G,0</sub> (eV)	$\alpha$ (meV/K)	$\beta$ (K)
GaN	3.507	0.909	830
AlN	6.23	1.799	1462
InN	0.69	0.414	454

expression

$$E_G(A_xB_{1-x}N) = xE_G(AN) + (1-x)E_G(BN) - x(1-x)b, \quad (6)$$

where  $E_G(AN)$  and  $E_G(BN)$  are the bandgaps of the two materials (AN and BN),  $x$  is the molar fraction of A, and  $b$  is a bowing parameter. For AlGaN, the material of interest for  $\text{Al}_x\text{Ga}_{(1-x)}\text{N}/\text{GaN}$  HEMTs, the relation has been determined as<sup>41,42</sup>

$$E_G(\text{AlGaN})(x) = [6.0x + 3.42(1-x) - 1.0x(1-x)] \text{ eV}. \quad (7)$$

Other band structure parameters of interest for GaN are the effective density of states in the conduction and valence bands ( $N_C = 2.24 \cdot 10^{18} \text{ cm}^{-3}$  and  $N_V = 4.56 \cdot 10^{19} \text{ cm}^{-3}$  at room temperature, RT), and the effective masses of electrons and holes ( $m_e = 0.20$  and  $m_h = 1.49$ ).<sup>36</sup>

### III. POLARIZATION CHARGES IN GaN

Controlled doping of wide-bandgap semiconductors is not always straightforward: typically, mobile carriers in FET are induced through impurity doping, i.e., by introducing foreign atoms in a semiconductor lattice. The energy distance between the dopant level and the related band ( $E_C - E_D$  for a donor level at energy  $E_D$ , or  $E_A - E_V$  for an acceptor level at energy  $E_A$ ) represents the dopant binding (or ionization) energy. The best dopants are relatively shallow, with binding energies in the range 0.01–0.05 eV. For GaN, only shallow donors are available (Si,  $E_C - E_D = 0.015$  eV), while the conventional acceptor is magnesium that creates a level 0.16 eV above the valence band energy. As a consequence, it is relatively easy to achieve high-electron concentrations, whereas for reaching high hole densities, dopant levels in excess of  $10^{19} \text{ cm}^{-3}$  are required. It is worth noticing that even high-quality GaN has a residual n-type (unintentional) conductivity, resulting in carrier densities in the range  $10^{15}\text{--}10^{17} \text{ cm}^{-3}$ , depending on material properties. Such residual conductivity has been ascribed to native defects of the semiconductor (e.g., point defects, vacancies, antisites) and impurities (like carbon, oxygen, and hydrogen).<sup>42</sup> The suppression of such defect-induced free carriers is very important for the fabrication of a highly insulating GaN layer to be used in devices with extremely high blocking voltages.

Contrary to conventional semiconductors, GaN has a unique advantage that helps obtain high carrier densities even in the absence of intrinsic doping: GaN, in fact, is a polar material and exhibits strong polarization effects.

As already mentioned, the wurtzite crystal of III-N semiconductors, which are typically grown epitaxially along the (0001) orientation, leads to the existence of polarization fields that are both spontaneous and piezoelectric. With zero external field, the total polarization  $P$  is equal to the sum of the spontaneous polarization  $P_{sp}$  and of the piezoelectric (or strain-induced) polarization  $P_{pz}$ . Bernardini *et al.*<sup>46</sup> investigated the polarization in GaN layers along the (0001) axis. Nitrogen has a higher electronegativity, compared to gallium. As a consequence, Ga and N atoms have anionic (+) and cationic (−) characteristics, generating a spontaneous polarization  $P_{sp}$  along the (0001) axis.<sup>37</sup> Wurtzite is the crystal arrangement with highest symmetry compatible with the

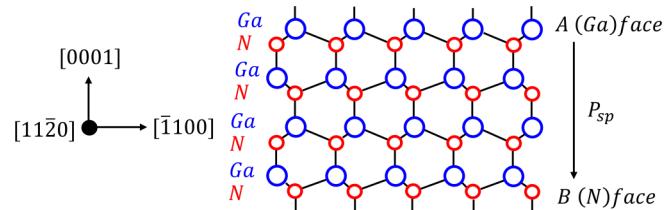


FIG. 5. Crystal structure of GaN, showing the sign and direction of the spontaneous polarization. Based on Yu *et al.*, J. Vac. Sci. Technol. B 17(4), 1742 (1999).<sup>52</sup>

presence of spontaneous polarization.<sup>46–48</sup> The arrangement of the cation and anion sublattices can lead to a relative movement from the ideal wurtzite position, favoring spontaneous polarization.<sup>49</sup> The orientation of spontaneous polarization is defined assuming that the positive direction goes from the metal (Ga) to the nearest nitrogen atom, along the c axis.<sup>50</sup> Figure 5 depicts the crystal structure of GaN and the sign and direction of the spontaneous polarization.

The values of the spontaneous polarization in GaN, InN, and AlN are reported in Table III for binary semiconductors. In the case of interfaces between binary and ternary semiconductors, the following expressions can be used (see also Ref. 51 and references therein):

$$\begin{aligned} P_{sp, \text{Al}_x\text{Ga}_{1-x}\text{N} / \text{GaN}}(x) &= (-0.052x - 0.029) [\text{C m}^{-2}], \\ P_{sp, \text{In}_x\text{Ga}_{1-x}\text{N} / \text{GaN}}(x) &= (-0.003x - 0.029) [\text{C m}^{-2}], \\ P_{sp, \text{In}_x\text{Al}_{1-x}\text{N} / \text{GaN}}(x) &= (0.049x - 0.081) [\text{C m}^{-2}]. \end{aligned} \quad (8)$$

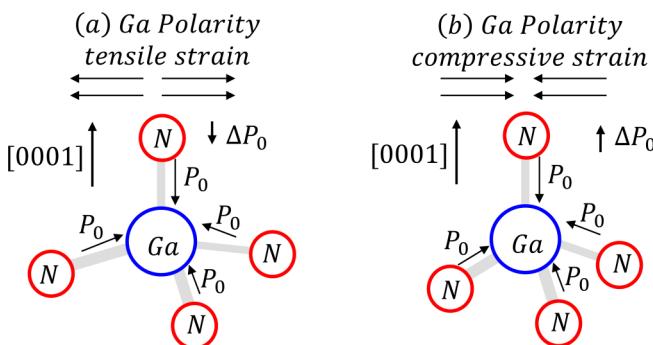
The strain in the crystal, and the displacement of the anion sublattice with respect to the cation sublattice, can lead to a piezoelectric polarization of the III-N semiconductors. A (simplified) representation of the polarization is given in Fig. 6, which reports a ball and stick diagram of the bond (tetrahedral) between gallium and nitrogen. In this figure, the Ga-polar configuration is represented. The electron cloud is closer to the nitrogen atoms, and this generates the polarization vectors. If the tetrahedron is ideal, the in-plane and vertical polarization components cancel each other.<sup>54</sup> When an in-plane tensile strain is applied [as shown in Fig. 6(a)], the polarization generated by the triple bonds decreases, and this generates a net polarization along the (0001) direction. On the contrary, when an in-plane compressive strain is applied [as shown in Fig. 6(b)], the polarization generated by the triple bonds increases, and this generates a net polarization along the (0001) direction.

To calculate the piezoelectric polarization, one needs to refer to the piezoelectric constants of the materials under analysis. Details on

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TABLE III. Values of spontaneous polarization of III-N semiconductors (binary). Values in the first row are from Ref. 46, and values in second row are from Ref. 53.

Material	GaN ( $\text{C m}^{-2}$ )	InN ( $\text{C m}^{-2}$ )	AlN ( $\text{C m}^{-2}$ )
$P_{sp}$	-0.029	-0.032	-0.081
$P_{sp}$	-0.034	-0.042	-0.090



**FIG. 6.** Schematic ball-and-stick configuration of a GaN tetrahedron with in-plane (a) tensile and (b) compressive strain, showing a net polarization. A full description including also the case of N-polar material can be found in Ref. 54.

the main parameters were given in Refs. 46, 50, and 55, and a comprehensive summary was presented in Ref. 51; here, in Table IV, we report the values of piezoelectric constants  $e_{ij}$  and lattice parameters  $a_0$  and  $c_0$  for GaN, InN, and AlN.

As discussed in Ref. 50, the lattice structure of wurtzite semiconductors is defined by the length of the hexagonal edge  $a_0$ , the height of the prism  $c_0$ , and a parameter  $u$  that defines the length of the bond parallel to the c axis ([0001]) in units of  $c_0$ . To calculate the piezoelectric polarization  $P_{pz}$  along the c axis, the key relation is

$$P_{pz} = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y). \quad (9)$$

Here,  $\epsilon_z = (c - c_0)/c_0$  represents the strain along the c axis, while the in-plane strain  $\epsilon_x = \epsilon_y = (a - a_0)/a_0$  is assumed to be isotropic.  $a$  and  $c$  are the lattice constants of the strained layers, and differ from  $a_0$  and  $c_0$ .

By considering that the lattice constants in a hexagonal AlGaN system are related according to

$$\frac{c - c_0}{c_0} = -2\left(\frac{C_{13}}{C_{33}}\right)(a - a_0)/a_0, \quad (10)$$

where  $C_{13}$  and  $C_{33}$  are elastic constants, the value of piezoelectric polarization along the c axis can be calculated as

**TABLE IV.** Values of piezoelectric constants  $e_{ij}$  and lattice parameters  $a_0$  and  $c_0$  for GaN, InN, and AlN.

Material	GaN	InN	AlN
$e_{31}$ ( $\text{C m}^{-2}$ )	-0.49 <sup>46</sup>	-0.57 <sup>46</sup>	-0.6, <sup>46</sup> -0.58 <sup>56</sup>
$e_{33}$ ( $\text{C m}^{-2}$ )	0.73 <sup>46</sup>	0.97 <sup>46</sup>	1.46, <sup>46</sup> 1.55 <sup>56</sup>
$a_0$ ( $\text{\AA}$ )	3.189	3.54	3.112
$c_0$ ( $\text{\AA}$ ) <sup>50</sup>	5.185	5.705	4.982

$$P_{pz} = 2(a - a_0)/a_0 \left( e_{31} - \frac{e_{33}C_{13}}{C_{33}} \right). \quad (11)$$

For an  $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$  stack, the material system of interest for GaN-based transistors, the values of the elastic constants can be calculated from the following formulas (see Refs. 51 and 56 for details):

$$\begin{aligned} C_{13}(x) &= (5x + 103) \text{ [GPa]}, \\ C_{33}(x) &= (-32x + 405) \text{ [GPa]}, \end{aligned} \quad (12)$$

and the variation of the lattice constant with the molar fraction is

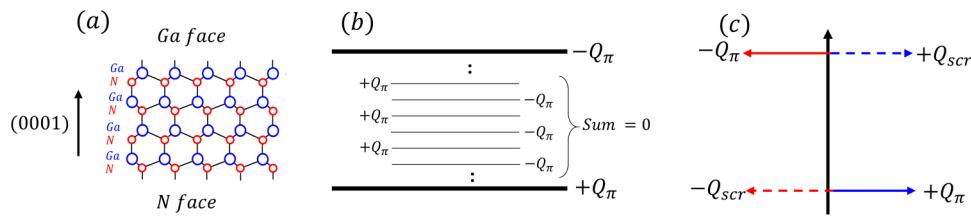
$$a(x) = (-0.077x + 3.189) \cdot 10^{-10} \text{ m}. \quad (13)$$

In a GaN layer, polarization charges are present on each unit cell. As schematically depicted in Fig. 7, the internal polarization charges cancel each other. Only the  $Q_\pi$  and  $-Q_\pi$  at the N- and Ga-faces remain and form a charge dipole [Fig. 7(c)]. Based on the numbers given in Table III, the spontaneous polarization charge in GaN has values in the range of  $1.8 - 2.1 \cdot 10^{13} \text{ e}^-/\text{cm}^2$ . In the absence of other charges, the polarization charge would lead to the presence of a dipole, resulting in a fairly high electric field, in the range of MV/cm. Such a dipole is screened through the formation of a screening dipole ( $Q_{scr}$ ). In the absence of the screening dipole, a non-physical situation would form. As discussed in Ref. 49, a first hypothesis would be that the screening dipole originates from ions from the atmosphere ( $\text{H}^+$ ,  $\text{OH}^-$ ); however, the dipole is present also in material grown in atmosphere free of counterions, like during molecular beam epitaxy (MBE) growth.

A different interpretation can be given by considering the presence of donor states at the surface of the GaN layer,<sup>57,58</sup> as schematically represented in Fig. 8(a). In the absence of compensating charge, due to the presence of the polarization dipole  $\pm Q_\pi$ , an electric field is present in the GaN layer, and the band diagram shows a linear slope [Fig. 8(b)]. If the GaN layer is sufficiently thick, the donor states pin the Fermi level at the surface (at the donor level  $E_{DD}$ ), and the screening charge  $N_{DD}^+$  at the surface is formed. The presence of a surface level  $E_{DD}$  has been proved also experimentally.<sup>49</sup> Realistic GaN layers typically have an n-type conductivity, as mentioned above. The ionized (bulk) donors also contribute to the overall charge balance. For a thick GaN layer [see Fig. 8(d)], the bands are nearly flat (corresponding to a negligible field), apart from the surface region. The polarization charge  $-Q_\pi$  at the surface is compensated by the positive charge of the ionized surface defects  $N_{DD}^+$  and by the total density of charges in the depleted n-type GaN.<sup>49</sup>

#### IV. BAND DIAGRAMS AND CHARGE DENSITY IN AlGaN/GaN HETEROSTRUCTURES

The core of a GaN-based HEMT is the AlGaN/GaN heterostructure. Both the GaN and the AlGaN layers are typically left undoped to minimize electron scattering at impurities. Based on the considerations above, undoped GaN has a weak n-type conductivity, with electron densities that depend on the quality of the epitaxy, and that—even in the best case—are higher than  $10^{15} \text{ cm}^{-3}$ <sup>49</sup> (early GaN films were showing a high n-type conductivity, in the range of  $10^{17}-10^{18} \text{ cm}^{-3}$ ).<sup>59,60</sup>



**FIG. 7.** (a) Schematic representation of a GaN lattice with ball and stick representation of the bonds, and indication of the Ga- and N-faces, along the (0001) direction. (b) Model for polarization charge in a GaN layer. (c) Charge distribution at the Ga- and N-faces, showing the polarization and screening dipoles (based on Ref. 49).

Optimizing the background electron density in lateral and vertical HEMTs requires a tuning of the growth process and the control of the residual impurities (such as carbon, see for instance Ref. 61).

Figure 9 shows the charge distribution, the electric field profile, and a schematic band diagram for an AlGaN/GaN heterostructure used in HEMT technology. In the figure,  $t$  is the thickness of the AlGaN layer, while the 2DEG is supposed to be located at a position  $d$ , a few nanometers far from the heterojunction, on the GaN side.

At the surface of the AlGaN layer, the total charge is determined by the sum of the charge of the surface donors and of the polarization charge of the AlGaN layer,  $qN_{DD}^+ - Q_\pi(\text{AlGaN})$ . At the AlGaN/GaN heterojunction, the total charge is given by the difference between the polarization charges of AlGaN and GaN, i.e.,  $Q_\pi(\text{AlGaN}) - Q_\pi(\text{GaN})$ . For gallium polar material, this is a positive number, since AlGaN has a higher polarization, compared to GaN. In the triangular potential well formed near the heterojunction, on the GaN side, a two-dimensional electron gas is formed. For simplicity, we consider this sheet of charge to be located in  $x = d$  (position of the centroid of the electron distribution).

The value of  $d$  can be easily determined by solving the Schroedinger equation in the triangular potential well formed at the AlGaN/GaN interface, that is schematically represented in Fig. 10. The electric field  $\epsilon_{\text{GaN}}$  is supposed to originate only from the charge in the 2DEG ( $n_s$ ), and is thus equal to  $qn_s/(\epsilon_0 \epsilon_{\text{GaN}})$ . The solution of the Schroedinger equation is approximated by<sup>62–64</sup>

$$\begin{aligned} E_n &\approx \left( \frac{\hbar}{2m^*} \right)^{\frac{1}{3}} \left( \frac{3}{2} \pi q \epsilon_{\text{GaN}} \right)^{\frac{2}{3}} \left( n + \frac{3}{4} \right)^{\frac{2}{3}} \\ &= \left( \frac{\hbar}{2m^*} \right)^{\frac{1}{3}} \left( \frac{3}{2} \pi q \right)^{\frac{2}{3}} \left( n + \frac{3}{4} \right)^{\frac{2}{3}} \left( \frac{qn_s}{\epsilon_0 \epsilon_{\text{GaN}}} \right)^{\frac{2}{3}}. \end{aligned} \quad (14)$$

We now consider that the first subband  $E_0$  is dominant. The 2D density of states associated with a single quantized level is<sup>64</sup>

$$D_{\text{DOS}} = \frac{qm^*}{\pi \hbar^2}. \quad (15)$$

The electron concentration in the 2DEG can then be calculated starting from the 2D density of states and from the position of the Fermi level, by using the Fermi-Dirac distribution as follows:<sup>64</sup>

$$n_s = D_{\text{DOS}} \cdot \frac{kT}{q} \cdot \ln \left[ 1 + \exp \frac{q(E_F - E_0)}{kT} \right], \quad (16)$$

where  $k$  is the Boltzmann constant.

By simple calculations (see details in Ref. 49), one can calculate the position  $d$  of the 2DEG, with respect to the heterointerface. Here, the 2DEG is considered an ideal 2D sheet of electrons located at a distance  $d$  from the interface, on the GaN side. For an AlGaN/GaN heterostructure, a typical value of  $d$  is 2 nm.<sup>49</sup>

At the bottom of the GaN layer, at the interface with the substrate, a screening charge compensates the (positive) component  $Q_\pi(\text{GaN})$ . The reader should note that in more realistic structures, other layers [e.g., a C-doped layer, a step-graded or a superlattice (SL)-based buffer, and an AlN nucleation layer] are placed between the GaN channel layer and the substrate; these layers are not shown here for simplicity.

At the surface of the AlGaN layer (if the layer is thick enough), the potential  $q\phi_s$  is pinned at the surface donor level  $E_{DD}$ . The AlGaN layer is not doped, so—in the absence of external bias—its electric field depends only on the sheet charge densities as follows:

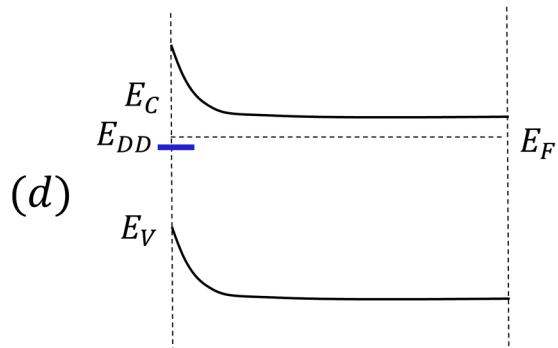
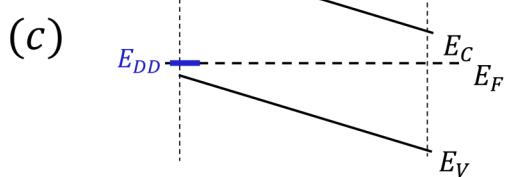
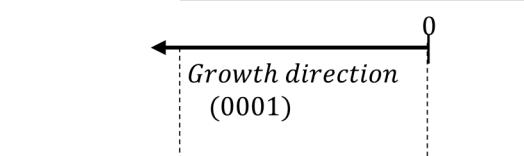
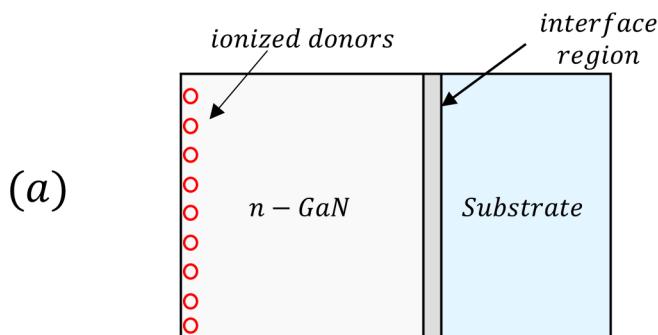
$$\epsilon_{\text{AlGaN}} = \frac{[qN_{DD}^+ - Q_\pi(\text{AlGaN})]}{\epsilon_0 \epsilon_{\text{AlGaN}}}. \quad (17)$$

With regard to the electric field in the GaN, we suppose that it originates only from the charge in the 2DEG and neglect (for this analysis) the effect of the n-type donor charge in the GaN. A more realistic solution can be obtained numerically, through technology computer-aided design (TCAD) tools. Under this assumption, the electric field in the GaN is

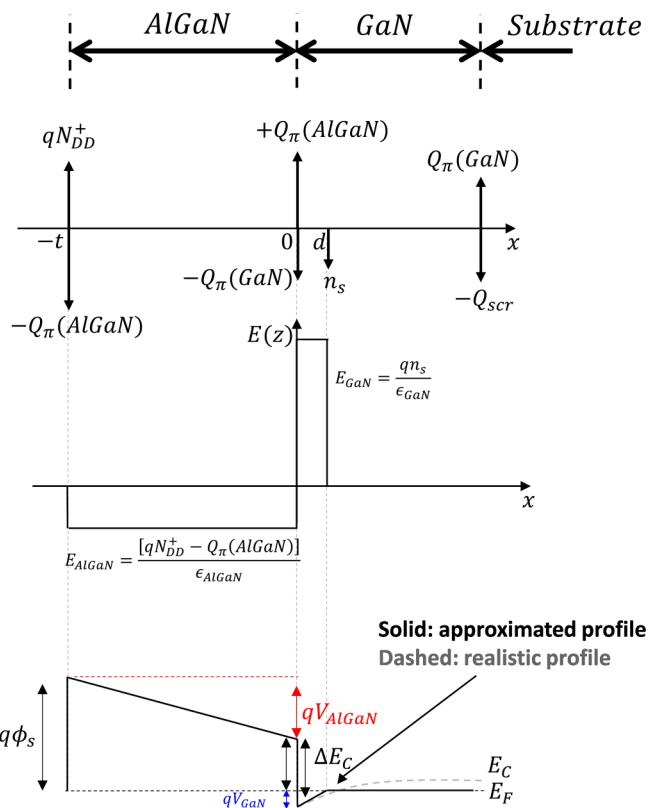
$$\epsilon_{\text{GaN}} = \frac{qn_s}{\epsilon_0 \epsilon_{\text{GaN}}}. \quad (18)$$

The total potential drop in the AlGaN is then

$$\begin{aligned} V_{\text{AlGaN}} &= -\epsilon_{\text{AlGaN}} t = -\frac{[qN_{DD}^+ - Q_\pi(\text{AlGaN})]}{\epsilon_0 \epsilon_{\text{AlGaN}}} t \\ &= \frac{[Q_\pi(\text{AlGaN}) - Q_\pi(\text{GaN}) - qn_s]}{\epsilon_0 \epsilon_{\text{AlGaN}}} t, \end{aligned} \quad (19)$$

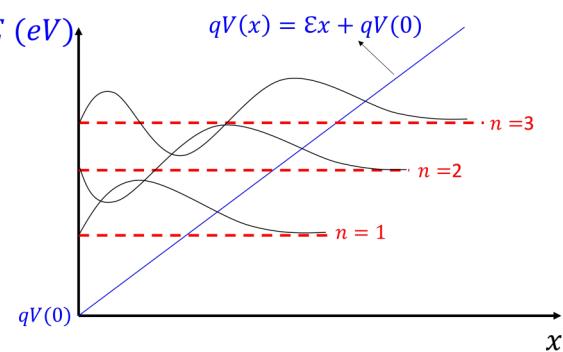


**FIG. 8.** (a) Schematic representation of a n-type GaN layer grown on a substrate. The (defective) interface region is shown. (b) Charge diagram showing the screening induced by surface donors. (c) Band diagram showing the surface donor level approaching the Fermi level at the surface of GaN, thus leading to the generation of the screening charge  $qN_{DD}^+$ . (d) Band diagram for a thick GaN (n-type), considering the presence of surface states and of donor charges. Based on *Semiconductor Device Physics and Design* (Springer Netherlands, Dordrecht, 2007).



**FIG. 9.** Charge distribution, electric field profile, and schematic band diagram of an AlGaN/GaN heterostructure.

19 January 2025 21:33:19



**FIG. 10.** Triangular potential well, similar to the one formed at the GaN side of an AlGaN/GaN interface. The energy varies linearly with field  $\epsilon$ , starting from the value  $qV(0)$  at the GaN side of an AlGaN/GaN interface. The energy levels and wavefunctions are schematically drawn (not to scale). Figure is based on Davies, *The Physics of Low-Dimensional Semiconductors* (Cambridge University Press, 1997).<sup>65</sup>

and, for GaN,

$$V_{\text{GaN}} = \epsilon_{\text{GaN}} d = \frac{q n_s}{\epsilon_0 \epsilon_{\text{GaN}}} d. \quad (20)$$

Considering the band diagram in Fig. 9, one can calculate

$$\phi_s - V_{\text{AlGaN}} - \frac{\Delta E_C}{q} + V_{\text{GaN}} = 0. \quad (21)$$

By combining the equations above, by considering  $\epsilon = \epsilon_0 \epsilon_{\text{GaN}} \sim \epsilon_0 \epsilon_{\text{AlGaN}}$ , the value of the sheet charge density  $n_s$  can be calculated as

$$n_s = \frac{[Q_\pi(\text{AlGaN}) - Q_\pi(\text{GaN})]t - \epsilon \left( \phi_s - \frac{\Delta E_C}{q} \right)}{q(t+d)}. \quad (22)$$

When a potential  $V_G$  is applied to the gate (through a suitable metal deposited on the AlGaN barrier), the charge in the 2DEG can be modulated: a more positive voltage will fill the channel, whereas moving to negative values of  $V_G$  will lead to the depletion of the 2DEG.

The dependence of  $n_s$  on  $V_G$  has the following form:

$$n_s(V_G) = \frac{[Q_\pi(\text{AlGaN}) - Q_\pi(\text{GaN})]t + \epsilon \left[ V_G - \left( \phi_b - \frac{\Delta E_C}{q} \right) \right]}{q(t+d)}, \quad (23)$$

where  $\phi_b$  is the barrier at the metal/AlGaN interface.

Figure 11(a) reports the value of the polarization charge  $Q_\pi(\text{AlGaN}) - Q_\pi(\text{GaN})$  at the  $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$  interface as a function of the molar fraction  $x$ . The values have been calculated based

on the parameters given in Ref. 56 as

$$Q_\pi(\text{AlGaN}) - Q_\pi(\text{GaN}) = Q_{\pi,pz}(\text{AlGaN}) + Q_{\pi,sp}(\text{AlGaN}) - Q_{\pi,sp}(\text{GaN}) \\ = \left| \frac{2(a(0) - a(x))}{a(x)} \left[ e_{31}(x) - e_{33}(x) \cdot \frac{C_{13}(x)}{C_{33}(x)} \right] + Q_{\pi,sp}(x) - +Q_{\pi,sp}(0) \right|, \quad (24)$$

where the spontaneous polarization charge in an  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  layer is defined as

$$Q_{\pi,sp}(x) = (-0.052x - 0.029) \left[ \frac{C}{m^2} \right]. \quad (25)$$

A typical range of interest for the mole fraction is between 0.2 and 0.4; such values are sufficiently high to give a reasonable polarization charge (which is necessary for generating electrons in the 2DEG), and enough conduction band discontinuity at the AlGaN/GaN heterointerface (which is necessary to ensure a good confinement of the 2DEG electrons). At the same time, the use of molar fractions higher than 0.4 may be critical, since the thermal and lattice mismatch between AlGaN and GaN may lead to high defect density and rough interfaces that may limit the overall device performance.

Figure 11(b) reports the sheet charge density ( $n_s$ ) of the 2DEG for three  $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$  interfaces as a function of the Al mole fraction and of the thickness of the AlGaN layer. For the calculation, a Schottky barrier equal to

$$q\phi_b = 1.3x + 0.84 \text{ eV} \quad (26)$$

was used, and the conduction band discontinuity at the  $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$  interface was calculated as

$$\Delta E_C = 0.7[E_G(x) - E_G(0)], \quad (27)$$

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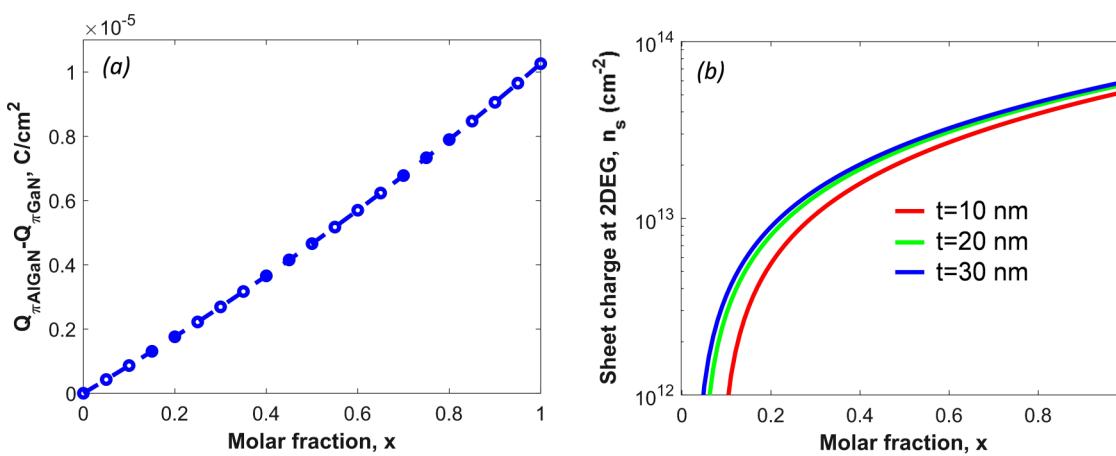


FIG. 11. (a) Polarization charge density at the AlGaN/GaN heterointerface  $[Q_\pi(\text{AlGaN}) - Q_\pi(\text{GaN})]$  calculated as described in Ref. 56. (b) Sheet charge density calculated for the 2DEG of an AlGaN/GaN heterojunction as a function of molar fraction  $x$  and thickness  $t$  of the AlGaN layer.

with

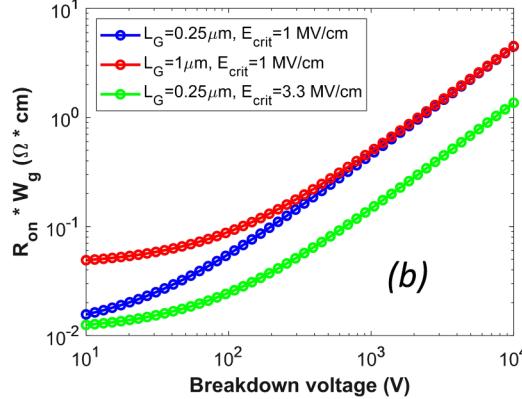
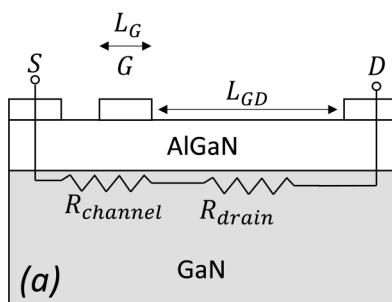
$$E_G(x) = x \cdot 6.13 \text{ eV} + (1 - x) \cdot 3.42 \text{ eV} - x(1 - x) \cdot 1 \text{ eV} \quad (28)$$

in agreement with Ref. 56.

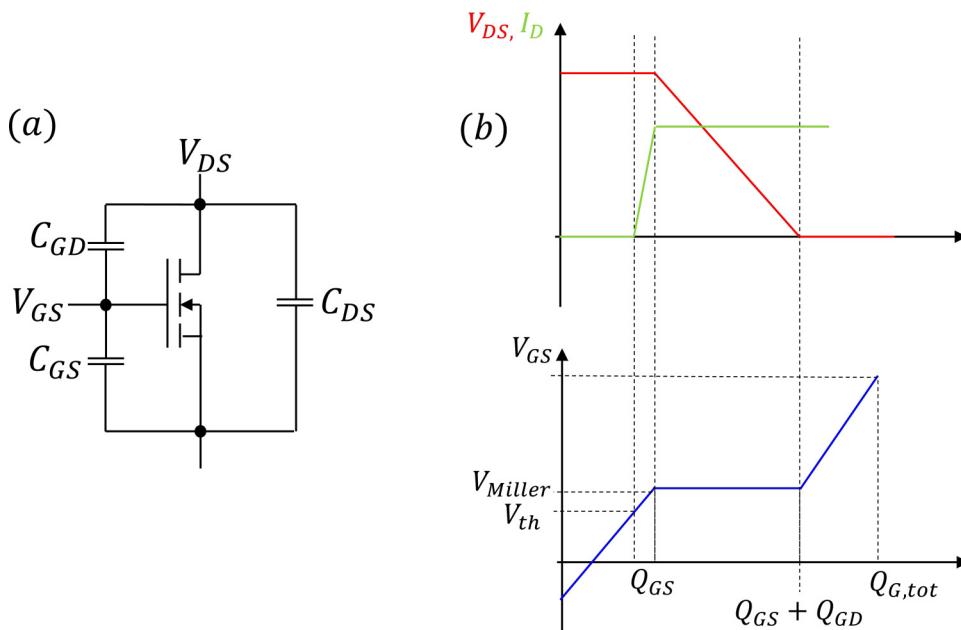
As can be noticed, when the mole fraction  $x$  is around 0.2–0.3, the sheet charge density is around  $10^{13} \text{ cm}^{-3}$ . With increasing thickness of the AlGaN layer, the density of electrons in the 2DEG increases, since the conduction band at the channel edge drops further below the Fermi level at the AlGaN/GaN interface (see also the band diagram in Fig. 9). As can be understood, AlGaN/GaN HEMTs are intrinsically normally ON. At zero gate bias, the channel is formed, with a high-electron density. A first possible approach to change the threshold voltage (by keeping the same Al content in the barrier) is to reduce the thickness of the AlGaN barrier. For sufficiently thin AlGaN barriers, the electron density falls to zero, and the 2DEG vanishes. This effect has also been observed experimentally, see for instance Ref. 57. This is just one of the possible approaches to achieve normally off operations in HEMTs; an excessive thinning of the barrier, along with the related etching process, may result in a significant increase in the leakage, and countermeasures are required to guarantee a good device performance.

In a GaN-based transistor, a gate metal is placed on an AlGaN/GaN heterostructure; the resulting schematic structure is shown in Fig. 12(a). For a power semiconductor device, the most critical parameters are the ON-resistance  $R_{on}$  (that needs to be as low as possible, to minimize the resistive losses in power converters) and the breakdown voltage  $V_{br}$  (that must be sufficiently high to ensure good reliability). In AlGaN/GaN HEMTs, these two parameters are strongly correlated: carriers are generated by polarization, and the breakdown voltage scales with the distance between the gate and drain ( $L_{GD}$ ).<sup>37</sup> In a first-order approximation, the ON-resistance of the device is the sum of the channel resistance ( $R_{channel}$ , originated from 2DEG under the gate) and of the drain-side access region ( $R_{drain}$ ), according to the following equation:<sup>37</sup>

$$R_{on} = R_{channel} + R_{drain} = \frac{L_G}{W_G} \cdot \frac{1}{qun_s} + \frac{L_{GD}}{W_G} \cdot \frac{1}{qun_s}. \quad (29)$$



**FIG. 12.** (a) Schematic representation of the structure of a GaN HEMT, showing the parasitic resistance of the channel ( $R_{channel}$ ) and of the gate-drain access region ( $R_{drain}$ ). (b) Dependence of the product  $R_{on} \cdot W_g$  on breakdown voltage, for devices with different gate lengths, and under the hypothesis that the breakdown field is 1 and 3.3 MV/cm.



**FIG. 13.** (a) Schematic circuit for understanding the dependence of gate charge on gate voltage during device turn-on. (b) Voltage, current, and gate charge characteristics for a generic field-effect transistor during a gate charge measurement.

ON-state (low-drain voltage, high current). At device turn-on, the gate-source voltage  $V_{GS}$  increases; when  $V_{GS}$  reaches the threshold voltage  $V_{th}$ , current starts flowing through the device. At the same time, the gate-source capacitance  $C_{GS}$  is charged, until the  $V_{Miller}$  voltage (and the corresponding plateau) is reached. At this point,  $C_{GS}$  is completely charged, and the drain current reaches the value fixed by the circuit. At the same time,  $V_{GS}$  becomes almost constant, and the drive current starts charging the Miller capacitance  $C_{GD}$ . This process goes on until the capacitance  $C_{GD}$  is fully charged. When both  $C_{GS}$  and  $C_{GD}$  are fully charged, the gate voltage starts increasing again. Through this experimental procedure, the charges  $Q_{GS}$  and  $Q_{GD}$  can be calculated. The gate charge  $Q_{GS} + Q_{GD}$  is the minimum charge required to turn on the transistor<sup>66</sup> and is thus representative of the switching losses.

A low value of  $Q_{GS} + Q_{GD}$  results in the device's ability to achieve high commutation speed ( $dV/dt$ ) and in a substantial reduction in switching losses.<sup>67</sup> A low gate charge also results in a reduced gate power for GaN devices, compared to Si components.<sup>68</sup> Since, as stated above, the dc losses depend on the  $R_{on}W_G$  product, and the ac losses are proportional to  $Q_G/W_G$ ,<sup>37</sup> the  $R_{on} \cdot Q_G$  product is an important parameter describing the switching efficiency of a given device. In a recent paper,<sup>1</sup> Chen *et al.* compared devices based on Si, SiC, and GaN in terms of figures of merit. They showed that, for devices with comparable ON-resistance, the  $R_{on} \cdot Q_G$  product can be around  $3800 \text{ m}\Omega \text{nC}$  for a Si superjunction MOSFET, in the range of  $1950\text{--}3480 \text{ m}\Omega \text{nC}$  for SiC-based FETs, and around  $290\text{--}300 \text{ m}\Omega \text{nC}$  for an E-mode GaN transistor. This result indicates that GaN E-mode HEMTs can contribute to a substantial reduction in switching losses, compared to conventional semiconductor transistors.

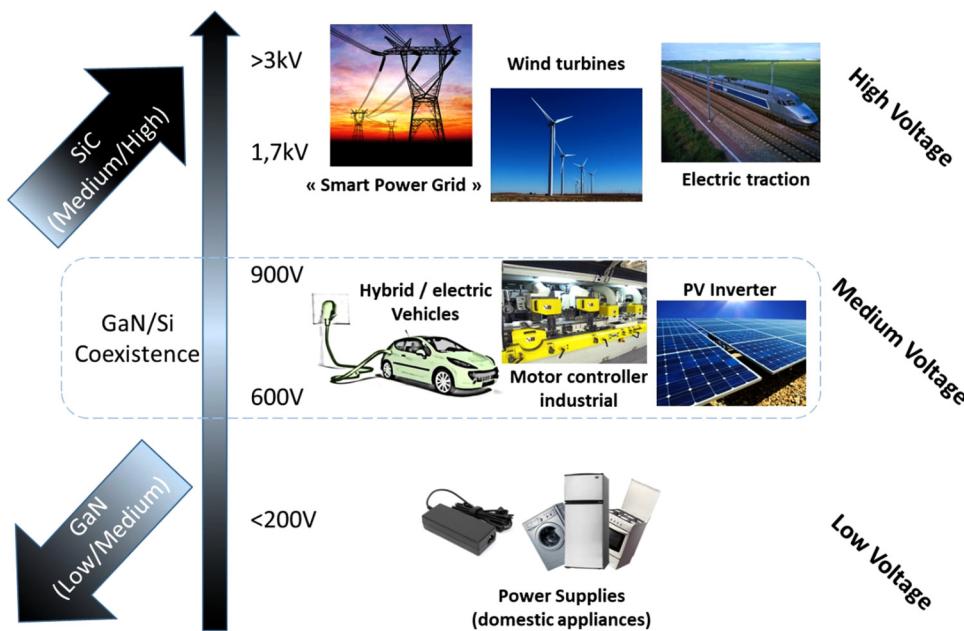
A further advantage of GaN-based transistors is the absence of reverse recovery charge. Si-based power transistors have an intrinsic body diode, whose presence results in a large reverse recovery

charge during commutation. For a Si superjunction (SJ) MOSFET, the product of ON-resistance ( $R_{DS,ON}$ ) and reverse recovery charge ( $Q_{rr}$ ) can be in excess of  $300 \text{ m}\Omega \mu\text{C}$ .<sup>1</sup> On the other hand, lateral GaN devices are based on the high-electron mobility transistor (HEMT) concept and do not have any body diode. HEMTs are majority carrier devices, and the lack of minority carriers leads to a near-zero  $Q_{rr}$  ( $R_{DS,ON} \times Q_{rr}$  down to  $2.2 \text{ m}\Omega \mu\text{C}$ ), with beneficial impact on the switching losses.

19 January 2025 21:33:19

## V. LATERAL GaN TRANSISTORS: TECHNOLOGY AND OPERATION

The rapid evolution of wide-bandgap semiconductors in the recent years has positioned lateral GaN transistors as key enablers in the power device market. The interest in power applications has undergone a remarkable shift due to the technological advantages of GaN HEMTs, which allow for simultaneous high voltage, high current, and low ON-state resistance, resulting in high power and high-efficiency operation. In addition, the wide bandwidth provides a robust and reliable technology capable of operating at high frequency and high temperature. This is why GaN-based lateral power electronic devices are emerging as switching components for next-generation high-efficiency power converters. Furthermore, the GaN-on-Si technology platform offers the best cost figures for commercialization of these products, although technologically very challenging. For instance, a complex GaN buffer for stress management and insulation purpose is required. This paves the way for a growing number of applications in various fields, including consumer electronics, transportation, and energy, as well as several industrial, automotive, and aerospace applications, such as rectifiers and high-voltage converters. As can be seen in Fig. 14, each application uses a specific voltage range. In terms of the device market, currently, the majority of GaN



**FIG. 14.** Examples of applications using different voltage ranges.

components are designed for 600/650 V applications and below (see Fig. 15). 900 V devices are also available.

## A. Lateral GaN device architectures

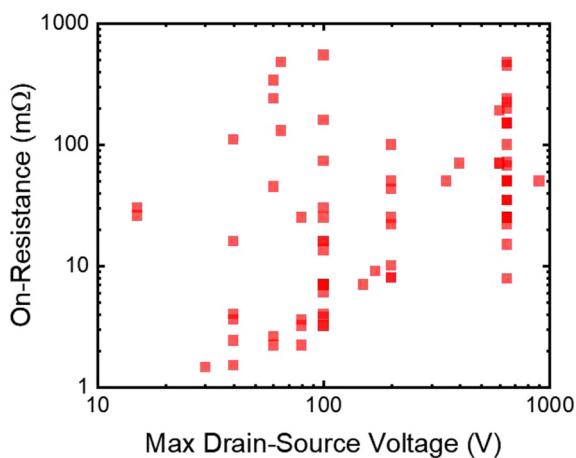
GaN-on-Si typical HEMT structures (Fig. 16) consist of several epilayers. These layers include materials with a wider bandgap and a lower bandgap, and an AlGaN/GaN heterostructure. At the interface between AlGaN and GaN, a two-dimensional electron gas (2DEG) is created with an electron channel accumulation without extrinsic doping. The 2DEG formation results from both

the spontaneous and piezoelectric effects.<sup>50,56,69</sup> The thickness and Al content of the AlGaN barrier layer defines the resulting polarization. It can be pointed out that a high-electron mobility above  $2000 \text{ cm}^2/\text{V s}$  can be combined with a high carrier density within the 2DEG, thus resulting in excellent electrical performance.

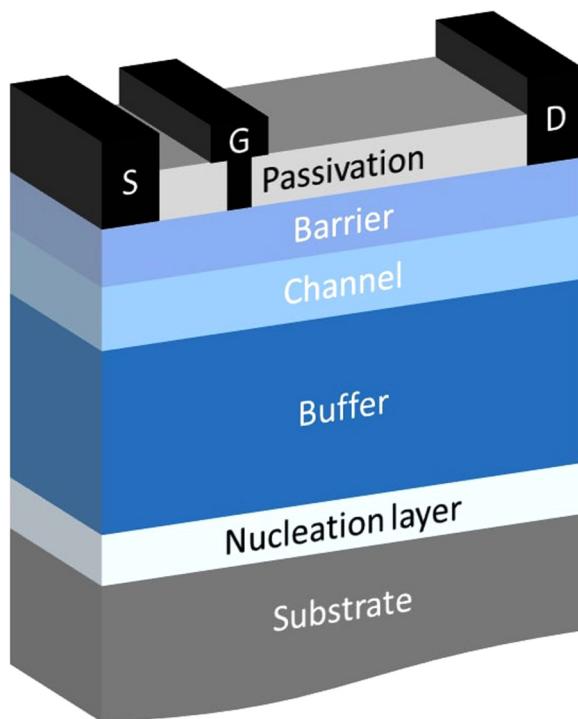
One of the main issues for GaN-based heteroepitaxy is the lattice mismatch and difference in thermal expansion coefficients with the substrate. This generally leads to a high dislocation density, which may be a source of leakage current under high electric field and subsequent device degradation. Residual stress may be created, inducing eventually cracks. The most common materials used as substrates are Si, sapphire, SiC, and, more recently, bulk GaN. In all cases, the epitaxial layers have rather high dislocation density ( $10^3$ – $10^{10}$  cm $^{-2}$ <sup>70,71</sup>). Some properties of the substrates typically used for GaN-based epitaxy are shown in Table V. For power applications, the Si substrate is preferred because of its low cost and availability in large diameter (up to 12 in.), despite a 17% lattice mismatch and a strong difference in thermal expansion coefficient between GaN and Si, which makes the growth challenging. Although sapphire substrates combine a high resistivity and low cost, the low thermal conductivity leads to a significant self-heating, which is not suitable for power applications. Finally, the high cost of SiC is prohibitive for large volume applications despite its outstanding properties.

Emerging GaN substrates, perfectly lattice matched, are of interest for vertical GaN architectures, see also Sec. VI.

In order to grow crack-free and high-quality GaN films by reducing the defect density, especially when using Si substrates, the tensile stress during the growth and cooling process needs to be limited. An AlN nucleation layer (NL) is typically used as an initiating layer for GaN growth. By using an AlN NL, the melt-back etching of Ga into Si can be avoided.<sup>72</sup> Moreover, the AlN NL provides a GaN layer with a compressive strain due to the 2.5% lattice



**FIG. 15.** Maximum drain–source voltage and on-resistance for a wide set of commercial GaN devices.

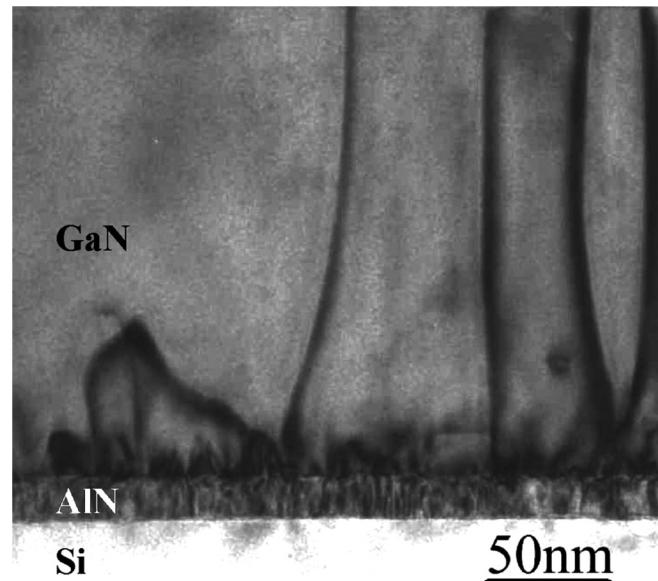


**FIG. 16.** Cross section of a typical AlGaN/GaN HEMT structure.

mismatch between AlN and GaN. This is necessary for compensating the tensile stress generated during the cooling process. Figure 17 shows a TEM image of the interface between the Si substrate and the AlN nucleation layer. Dislocations are reduced but still present across the buffer layers.

Whatever the choice of substrate, the buffer layers are critical. The high 2DEG sheet charge density in GaN-based HEMTs enables significant drain current densities. Inadequate carrier confinement within the channel leads to soft pinch-off characteristics and high subthreshold leakage. The presence of a high defect or impurity density in the buffer produces high leakage currents and poor device reliability. Consequently, on top of a high-quality AlN NL, proper buffer configuration and material quality is mandatory.

A well-known approach is the use of a step-graded AlGaN buffer, as shown in Fig. 18. Several micrometers thick  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  buffer layers with various Al contents enable us to further mitigate lattice and thermal-mismatch detrimental effects. The interest of



**FIG. 17.** TEM image of a cross section of an AlN/Si interface. Reproduced with permission from Liu *et al.*, Appl. Phys. Lett. **83**, 860–862 (2003). Copyright 2003 AIP Publishing LLC.<sup>74</sup>

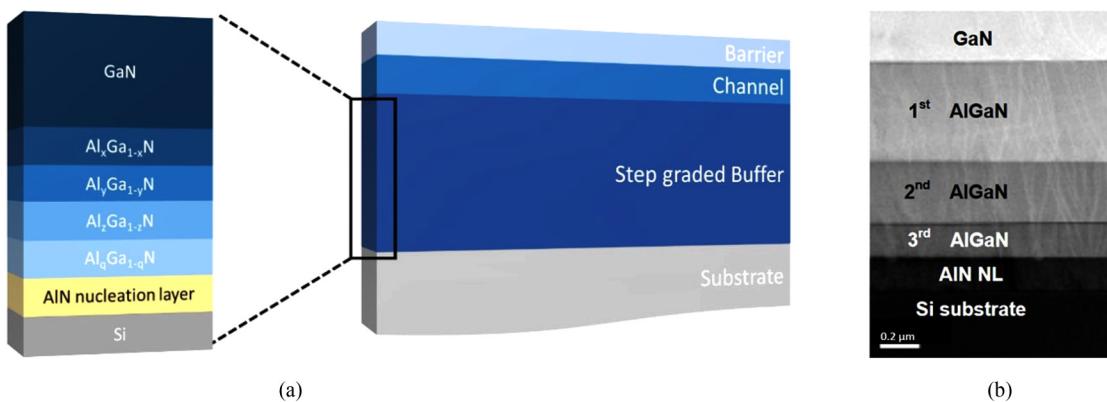
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this approach is also to improve the 2DEG electron confinement under high electric field, by limiting the carrier injection into the buffer layers, i.e., to the so-called punch-through effect. Another practical route to significantly increase the buffer layers' resistivity is the introduction of intentional compensating centers. Iron or carbon doping can be used to produce highly resistive buffers (carbon being the choice for GaN-on-Si GaN devices). Finally, superlattice (SL) buffers consisting in many periods of thin AlN/GaN pairs have been proved to be one of the most effective techniques both to control the stress and enhance the blocking voltage.<sup>75</sup> With thick SL buffers, high crystal quality and smooth surface of the top-GaN layer can be obtained resulting in superior performance as described further in this paper.

The epitaxial heterostructure is completed with a cap layer, which is generally composed of GaN or SiN to reduce the oxidation of the underlying AlGaN film. It is important to note that surface states<sup>57</sup> on top of the AlGaN constitute the origin of the 2DEG, as discussed in Sec. IV. However, surface defects may also be detrimental to the device performance. Under operating conditions, trapping at surface defects can create a virtual gate between gate and drain terminals, depleting unintentionally the 2DEG and thus

**TABLE V.** Properties of various substrates used for GaN epitaxy.<sup>73</sup>

	Structure	Lattice constants $a$ (nm)	Lattice constants $c$ (nm)	Thermal conductivity (W/cm K)	Lattice mismatch (%)
Sapphire	Hexagonal	0.476	1.2982	0.25	15
6H-SiC	Hexagonal	0.308 06	1.511 73	4.9	3.1
Si	Cubic	0.543 102		1.56	17



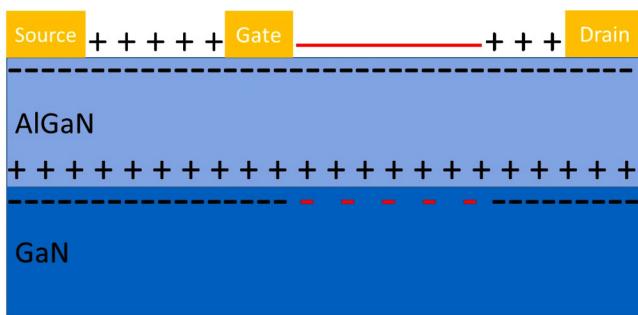
**FIG. 18.** Schematic cross section and TEM image of AlGaN layers with various Al content between the nucleation layer and the GaN layer. Reproduced with permission from Cho *et al.*, in *Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials* (2011). Copyright 2011, licensed under a Creative Commons Attribution 4.0 License CC BY.<sup>76</sup>

severely degrading the device performances and/or reliability. Negatively charged surface states may compensate the donor atoms, thus depleting the channel between the gate and the drain. A surface passivation layer, typically SiN, allows us to mitigate the 2DEG depletion as can be seen in Fig. 19.

Lateral heterostructure devices are inherently normally ON, i.e., they conduct current when no gate voltage is applied. This raises safety concerns because in case of a malfunctioning gate driver, the GaN transistor is not automatically switched off and an uncontrolled current flow can damage the entire system. Furthermore, normally ON transistors make circuit designs more complex because a negative-voltage supply is required. Thus, a substantial research effort was focused on creating normally off devices in recent years.

## B. Approaches for normally OFF operations

In a conventional AlGaN/GaN HEMT, the threshold voltage  $V_{TH}$  depends on several parameters related to the gate metal and the heterojunction properties, as can be seen from the following



**FIG. 19.** Schematic cross section showing surface state depletion effects within an AlGaN/GaN HEMT.

equation:<sup>77</sup>

$$V_{TH}(x) = \phi_B(x) - \Delta E_C(x) - \frac{\sigma(x)}{\epsilon_0 \epsilon_{AlGaN}(x)} t - \frac{q N_D}{2 \epsilon_0 \epsilon_{AlGaN}(x)} (t)^2. \quad (31)$$

$x$  represents the Al content in the barrier layer,  $\phi_B(x)$  is the Schottky barrier height between the gate metal and the AlGaN barrier layer,  $\Delta E_C(x)$  is the conduction band discontinuity at the AlGaN/GaN interface,  $\sigma(x)$  is the polarization charge at the AlGaN/GaN interface,  $\epsilon_0$  is the permittivity vacuum,  $\epsilon_{AlGaN}(x)$  is the permittivity of the AlGaN layer,  $t$  is the AlGaN thickness,  $q$  is the electric charge, and  $N_D$  is the doping.

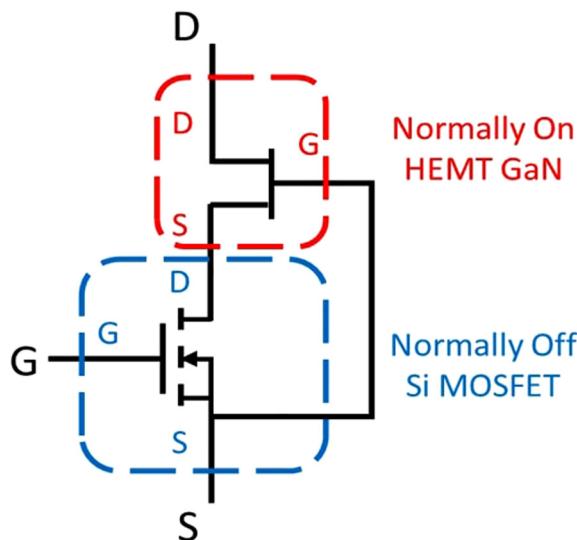
Thicker AlGaN barriers and higher polarization differences between AlGaN and GaN lead to more negative  $V_{TH}$  as they increase  $n_s$  at zero bias. From this equation, it is clear that several degrees of freedom exist to tune the  $V_{TH}$ , such as changing the Schottky barrier height or the 2DEG carrier density related to the AlGaN barrier layer, which is dependent on the Al content and its thickness.

Different topologies have been proposed in order to achieve normally off GaN HEMTs: a cascode configuration<sup>78–80</sup> combining a Si normally off MOSFET and a normally ON GaN HEMT, the use of a HEMT with fluorine implantation under the gate,<sup>81–83</sup> a gate recessed MIS-HEMT (metal-insulator-semiconductor) with partial<sup>84,85</sup> or complete<sup>86</sup> AlGaN barrier removal, and a p-GaN-gated<sup>26,87,88</sup> HEMT.

### 1. Cascode configuration

The cascode configuration uses a high-voltage normally ON GaN HEMT connected in series with a low-voltage Si MOSFET in the switching circuit, as can be seen in Fig. 20. The Si MOSFET controls the ON and OFF-state switching of the GaN HEMT. When a positive gate voltage above the threshold voltage is applied

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**FIG. 20.** A cascode circuit showing the normally ON HEMT in series connection of a normally off Si-MOSFET.

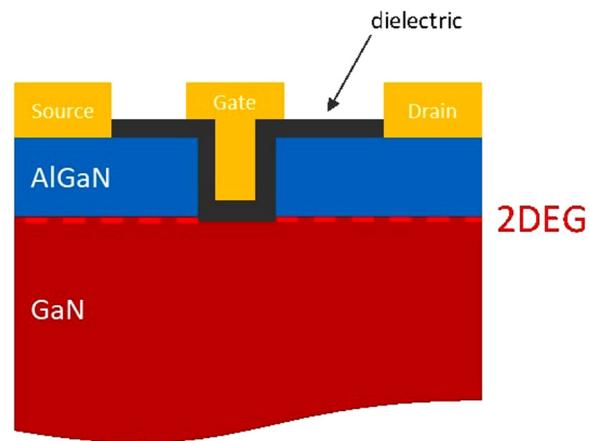
to the MOSFET, the GaN HEMT gate voltage is close to zero and the device is turned on. As the two devices are connected in series, when a voltage is applied to the drain of the HEMT, the current will also flow through the MOSFET. On the other hand, when no gate voltage is applied to the MOSFET to turn it off, no current can flow through the channel of the HEMT. In addition, any increase of the drain voltage will be handled by the HEMT, thus resulting in a high reliability.

Therefore, the cascode configuration enables us to take advantage of the positive threshold voltage of the MOSFET as well as the low ON-resistance of the 2DEG, together with the high breakdown field of the GaN HEMT in OFF-state conditions. However, it can be noticed that this approach limits the high-temperature operation by the presence of the Si device. In addition, the packaging complexity and size are increased and parasitic inductances are introduced, and this may have an impact on the switching performance of the circuit.

## 2. Recessed gate MIS-HEMT

Another approach consists of etching the AlGaN barrier layer under the gate area followed by a deposition of a gate dielectric insulating layer. The AlGaN barrier layer is fully etched by plasma in the gate region (Fig. 21). This allows for high threshold voltages, while the thick gate dielectric enables a large maximum forward gate bias ( $>+10$  V).

The choice of the dielectric is extremely important, as it will directly impact the channel mobility within the 2DEG<sup>89</sup> and the stability of the threshold voltage.<sup>90</sup> Also, the dielectric quality and surface roughness of the etched area are critical parameters, and the interface charge density needs to be well controlled. Several mechanisms, involving the surface states and related trapping, have

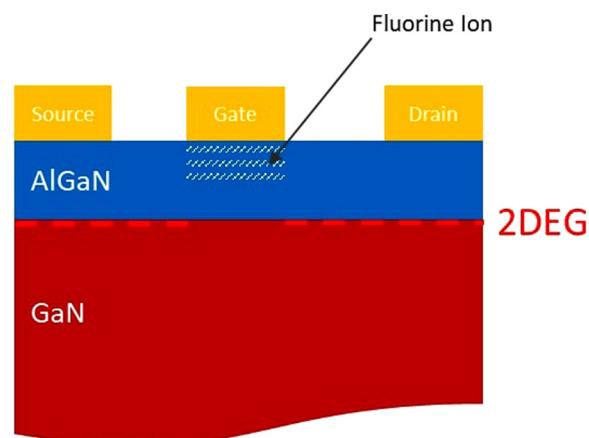


**FIG. 21.** Schematic cross section of a recessed gate GaN MIS-HEMT.

been proposed to explain the possible origin of the device degradation phenomena (see Secs. VII B and VII C).

## 3. The fluorine-treated HEMT

Fluorine ions implanted into the AlGaN layer self-aligned to the gate (see Fig. 22) can also create a normally off behavior.<sup>91,92</sup> The negative ions into the barrier change the surface potential, thus depleting the 2DEG. However, the  $V_{TH}$  stability after annealing at high temperature and/or under high electric field is a source of concern for this approach.<sup>93,94</sup> Moreover, previous studies have shown the relation between fluorine and current collapse,<sup>95,96</sup> which may be an issue for power switching applications.<sup>95,97</sup> Other reports focused on fluorine-treated MIS/MOS-HEMTs, see for instance Refs. 83 and 98.



**FIG. 22.** Schematic cross section of an F-doped GaN HEMT.

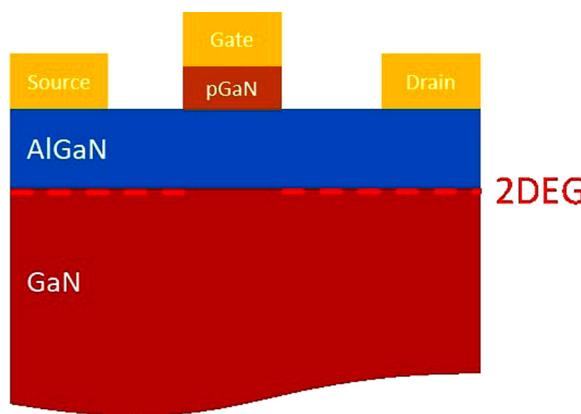


FIG. 23. Schematic cross section of a p-GaN gate GaN HEMT.

#### 4. P-GaN gate

An attractive method to achieve normally off GaN transistors is the use of a p-doped GaN layer<sup>99</sup> under the gate area (Fig. 23). The presence of the p-GaN layer lifts the band diagram to higher energies (Fig. 24), so that the 2DEG depletion occurs even in the absence of an applied external bias. In order to maximize the 2DEG depletion induced by the p-GaN cap layer, the Al mole fraction in the barrier and the thickness of the barrier must be carefully optimized. It has been demonstrated that to achieve a good depletion of the 2DEG, the Al content and thickness of the barrier should be kept relatively low.<sup>100</sup> Greco *et al.* determined the energy band diagram by Schrödinger–Poisson (Fig. 25) of two structures with an identical barrier thicknesses (25 nm) but different Al content (12% and 26%) by using a p-GaN layer thickness of 50 nm with an acceptor concentration of  $3 \times 10^{19} \text{ cm}^{-3}$ . Figure 25 clearly shows that despite the presence of the p-GaN layer, the high Al content structure still exhibits a normally ON behavior with the conduction band below the Fermi level at the AlGaN/GaN interface; on the contrary, the structure with reduced Al content can reach normally off operations. Similarly, the conduction band

diagram of p-GaN/AlGaN/GaN heterojunctions with two different barrier thicknesses (10 and 25 nm, with a fixed Al content of 26%) has been simulated. As can be noticed, the structure with a thickness of 25 nm reveals a normally ON behavior, whereas the thinner barrier results in normally off devices. Based on a series of tests, a summary graph can be produced showing the normally ON and normally off area with respect to the thickness and Al content of the AlGaN barrier layer (Fig. 26).

Also, a high Mg concentration in the p-GaN layer is required, which should be balanced with the deterioration of the crystal quality for too high Mg doping concentration. The p-GaN layer has shown a wide process window in terms of thickness and doping, which eases process control requirements. However, the low selectivity of the etching process between the p-GaN and the barrier layer needs to be carefully optimized in order to achieve a stable high threshold voltage.<sup>95</sup>

The presence of a p-GaN layer above the AlGaN barrier and the GaN channel creates a p-i-n diode. When the device is in the ON-state (i.e., with positive gate bias, PGB), this diode may gradually turn-on, resulting in an increase in gate current. The amount of current is strongly dependent on the properties of the metal/p-GaN interface. In general, most single-metal contacts to p-GaN have a Schottky-like nature: this is due to the wide bandgap of GaN (3.4 eV) and its large electron affinity (4.1 eV<sup>101,102</sup>). From these numbers, it appears evident that a ohmic contact on p-GaN would need a work function in excess of 7 eV, and this is not the case for common single-metal contacts based on Pt (work function = 5.65 eV<sup>103</sup>), Pd (work function = 5.12 eV<sup>103</sup>), and Ni (work function = 5.15 eV<sup>103</sup>). As a consequence, the metal/p-GaN contacts are not ohmic in strict sense; their conductivity depends on the properties of the materials formed at the metal/semiconductor interface during deposition and annealing.<sup>104</sup>

Depending on the choice of the metal, on the doping of p-GaN and on the process parameters, the metal/p-GaN contact can have a higher (referred to as ohmic) or lower (Schottky) leakage current. Ohmic contacts have been reported, see, for example, Refs. 88,104, and 105. Recent reports indicated that by using a titanium nitride (TiN) contact,<sup>106</sup> it is possible to significantly reduce the gate leakage for transistors. The use of a Schottky-like contact can significantly reduce the gate leakage;

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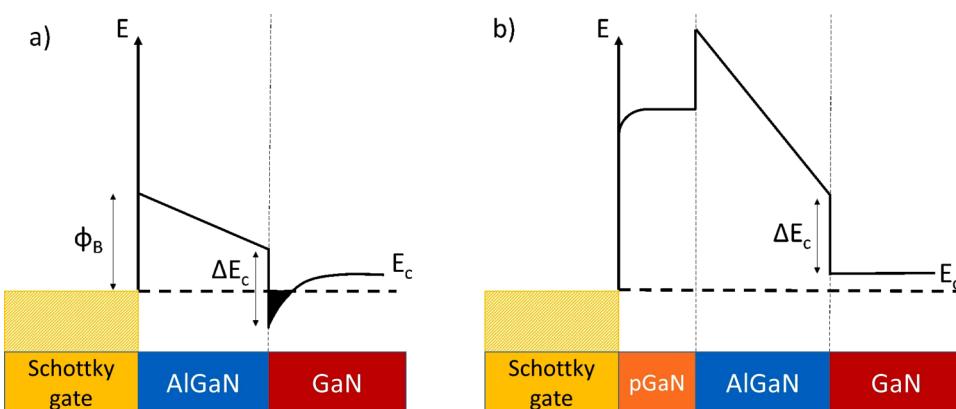
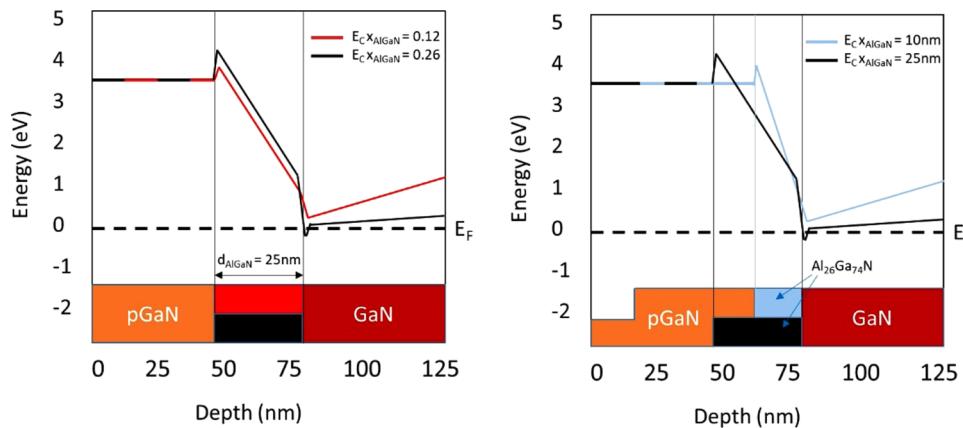


FIG. 24. Band diagram of an AlGaN/GaN heterostructure with (a) and without (b) p-GaN layer. Reproduced with permission from Greco *et al.*, Mater. Sci. Semicond. Process. 78, 96–106. Copyright 2018 Elsevier.<sup>95</sup>



**FIG. 25.** Simulated conduction band diagrams of a p-GaN/AlGaN/GaN heterostructure for two different Al contents (12% and 26%) into the AlGaN barrier layer (left) and two different AlGaN barrier thicknesses (right). Reproduced with permission from Greco *et al.*, Mater. Sci. Semicond. Process. **78**, 96–106. Copyright 2018 Elsevier.

however, degradation phenomena related to the depletion and high electric field across p-GaN must be avoided, as discussed in Sec. VII B. On the other hand, a forward-biased gate diode may require a specific driving strategy,<sup>107</sup> e.g., based on the use of a RC network. A ohmic contact can also favor hole injection and, in some cases,<sup>105</sup> promote conductivity modulation.

### 5. Tri-gate

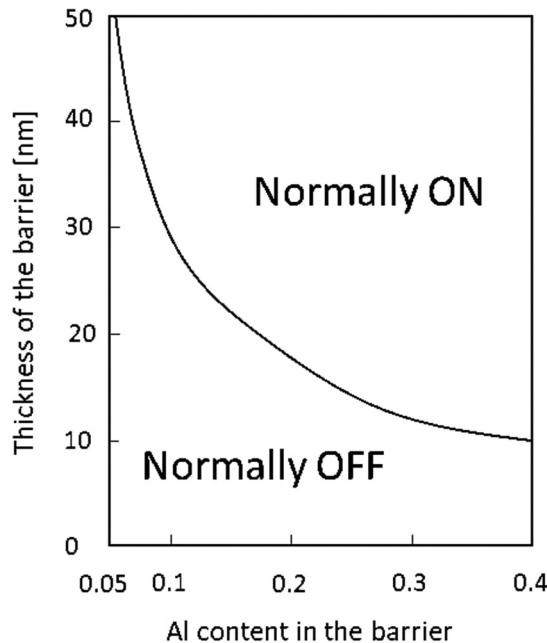
Compared to conventional planar AlGaN/GaN HEMTs, tri-gate transistors feature fins patterned in the gate region, which

are conformably covered by a 3D gate electrode [Figs. 27(a) and 27(b)]. While such architecture was first introduced for Si ultra-scale MOSFET in 2002<sup>108</sup> to address the short channel effects, it was soon adopted for power devices. The first tri-gate GaN demonstration appeared in 2008,<sup>109</sup> followed by several other works that showed the several benefits of such architecture, such as the improved current stability, the lower subthreshold slope, and the reduced OFF-state leakage.<sup>110–113</sup>

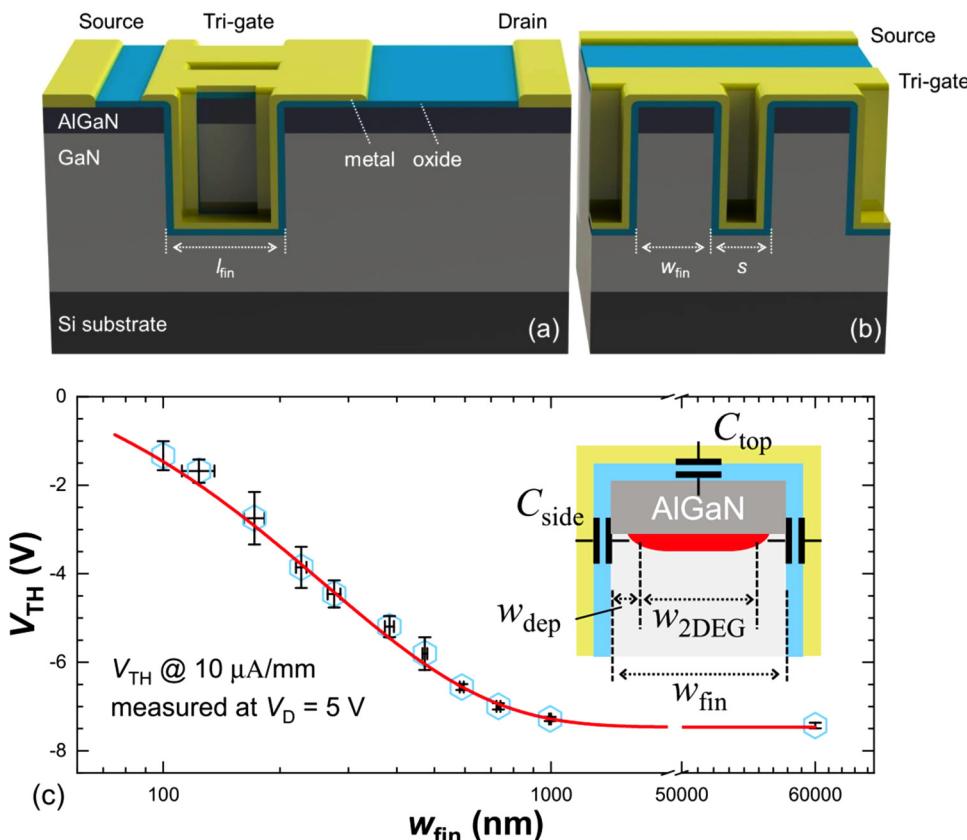
The most interesting feature of the tri-gate is, however, its ability to modulate the device threshold voltage ( $V_{TH}$ ) by simply tuning the fin width ( $w_{fin}$ ) [Fig. 27(c)]. Such an effect has been attributed to the partial AlGaN strain relaxation when patterned into fins and by the fin sidewalls depletion due the side gate electrode.<sup>115–117</sup>

The dependence of the device  $V_{TH}$  on the fin width can be used to achieve a normally off operation by simply designing the proper  $w_{fin}$  by lithography, without the need for any critical etching as for gate recess or p-GaN gates. However, early demonstrations based on this approach typically presented still negative  $V_{TH}$  (at 1  $\mu$ A/mm) and degraded ON-resistance due to the very small fin width required to achieve a normally off operation.<sup>110,118–120</sup> Recently, a tri-gate device with 20 nm-wide fins in combination with a large work function gate metal stack (Pt/Au) successfully showed a full normally off operation with a  $V_{TH}$  of 0.64 V (at 1  $\mu$ A/mm) and a competitive  $R_{ON}$  of 7.4  $\Omega$ ·mm.<sup>121</sup> To achieve such performance, however, very high-resolution lithographic processes are required both to define the fin width (which sets  $V_{TH}$ ) and to reduce the gap in-between fins (which degrades  $R_{ON}$ ). Since, at the moment, the lithographic resolution in power devices foundries is still in the order of several hundreds of nm, it is interesting to find solutions to increase the minimum required  $w_{fin}$ .

A promising approach consists of combining the tri-gate architecture with conventional methods to achieve a normally off operation such as recessed gate and p-GaN cap. This allows us to achieve large positive  $V_{TH}$  values while keeping the benefits of the tri-gate architecture and relaxing the lithographic requirements. The first demonstration of such an approach appeared in 2012<sup>122</sup> with the integration of the tri-gate architecture with AlGaN barrier recess, followed by a more recent work<sup>123</sup> in 2019 that showed promising  $V_{TH}$  of 1.4 V (at 1  $\mu$ A/mm) and  $R_{ON}$  of 7.3  $\Omega$ ·mm.



**FIG. 26.** Device operation modes as a function of the Al content and the thickness of the barrier. Reproduced with permission from Greco *et al.*, Mater. Sci. Semicond. Process. **78**, 96–106. Copyright 2018 Elsevier.



**FIG. 27.** Schematics of (a) the tri-gate MOSHEMTs and (b) its tri-gate region. (c) Dependence of  $V_{\text{TH}}$  on  $w_{\text{fin}}$ . Reproduced with permission from Ma, "Tri-gate technologies for high-performance power GaN devices," Thesis (EPFL) (2019). Copyright 2019 by the author of the cited Thesis.<sup>114</sup> The inset in (c) illustrates the effect of sidewall depletion in distributing the 2DEG across a fin. Reproduced with permission from Ma et al., in IEEE Trans. Electron Devices **66**(9), 4068–4074 (2019). Copyright 2019 IEEE.<sup>115</sup>

Moreover, the tri-gate architecture can also be integrated with the p-GaN cap approach, allowing us to further increase  $V_{\text{TH}}$  with respect to the planar case and relax the trade-off between  $V_{\text{TH}}$  and the heterostructure sheet resistance.<sup>124</sup> Finally, the tri-gate architecture can also be combined with promising p-type oxides, such as NiO, which can be conformably deposited around the fin and help us to further shift the device  $V_{\text{TH}}$  without the need of complex p-GaN regrowth.<sup>125</sup>

## 6. Commercial perspective

At the moment, commercial GaN normally OFF devices are based either on the cascode or the p-GaN technology. Cascode devices have demonstrated high reliability, obtaining several automotive certifications, and present large gate swing and robustness, which is highly appreciated by circuit designers used to work with Si devices. On the other hand, the introduction of the Si low-voltage device may lead to more complex and costly packaging. In parallel, normally OFF GaN devices with a p-GaN cap structure allow us to achieve a normally OFF operation with a good reliability and quite simple fabrication. However, the p-GaN technology may present some limitations in terms of gate swing. While fluorine implantation seems to have lost steam due to long-term and high-temperature reliability concerns, gate recess could leverage on the trade-off found for p-GaN devices and result in good

performance. Thanks to current and future research efforts, it is expected that the technology will improve and that the current issues regarding the GaN etched interface and the high-quality gate dielectric layer will be solved. Such research could strongly benefit also the tri-gate technology, which faces similar issues regarding the sidewalls interface quality and the gate dielectric. Moreover, the development of GaN logic [both direct-coupled FET logic (DCLF)<sup>126–129</sup> and CMOS<sup>130–132</sup>] will require the adoption of higher-resolution lithographic lines, which would allow for a reduction of the minimum fin width, making the tri-gate and its combination with gate recess a viable future technology.

## C. Breakdown mechanisms

Converters based on MOSFETs have the ability to survive a limited exposure to voltages above the device rating, according to the specified avalanche energy rating. However, lateral GaN HFETs do not have the potential for avalanche breakdown<sup>133</sup> because they do not rely on a p-n junction for blocking voltage and may experience catastrophic dielectric breakdown when exposed to sufficient overvoltage.<sup>134</sup> This breakdown is destructive and non-recoverable.

The main sources of leakage current and related breakdown voltage ( $V_{\text{BR}}$ ) for an AlGaN/GaN HEMT power transistor on an Si substrate are the following (see Fig. 28):

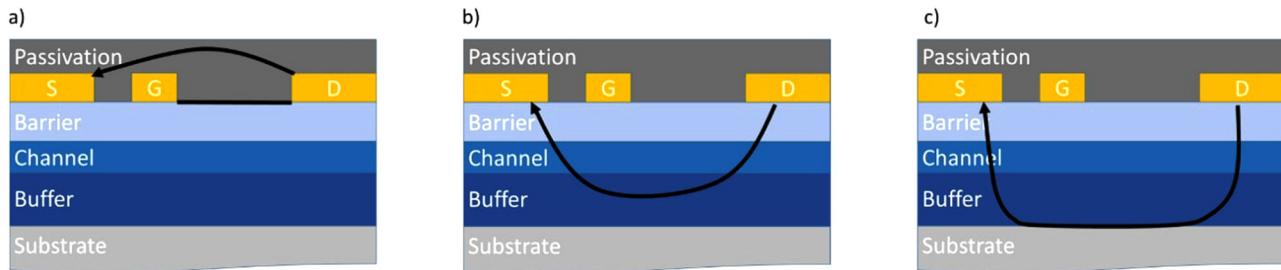


FIG. 28. Schematic representation of the main sources of leakage current for AlGaN/GaN transistors on Si.

- Punch-through effect reflecting a parasitic electron injection into the buffer.
- Leakage current through the passivation layer and/or due to a surface related conduction.
- Vertical breakdown, through the total buffer thickness, that can be due to a poor doping compensation of the buffer.

Different approaches have been developed in order to mitigate these leakage paths and associated premature breakdown while avoiding trapping effects.

- The use of a high-quality dielectric for surface passivation reduces leakage at the surface and at the interface with the barrier.<sup>135</sup>
- Proper doping compensation into the buffer layers, generally carbon or iron doping,<sup>136–138</sup> enables us to significantly enhance the buffer resistivity and consequently avoid carrier injection. Furthermore, back barrier<sup>139,140</sup> based on graded AlGaN or AlN material has been developed in order to reduce this phenomenon, increasing the blocking voltage. In both cases, the thickness of the GaN channel region must be carefully optimized with the aim of achieving a high-electron density in the 2DEG, a good electron confinement in the channel, and low trapping effects, especially in the case of doping compensation.<sup>141,142</sup>

It can be pointed out that the AlGaN/GaN transistor breakdown voltage scales linearly for small gate-drain distances

(typically below 15  $\mu\text{m}$ ), while larger gate-drain distances result in a saturation of  $V_{BR}$  due to the conduction into the substrate triggered by the vertical electric field. Extensive research is carried out to overcome the breakdown mechanisms and further push the limits of GaN-on-Si HEMTs.

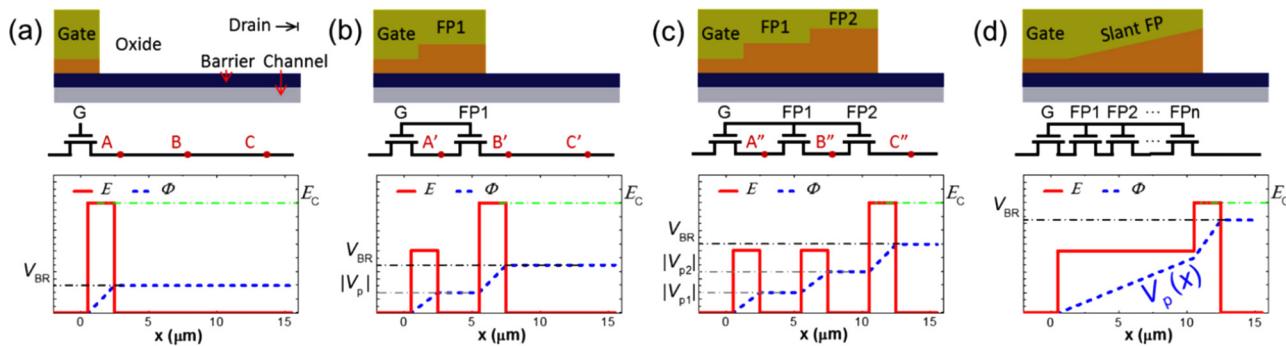
In addition, the crystal quality is an important factor. Considering the high material defect density in GaN/Si epilayers, recent studies<sup>143,144</sup> showed that the presence of defects may impact on the breakdown voltage.

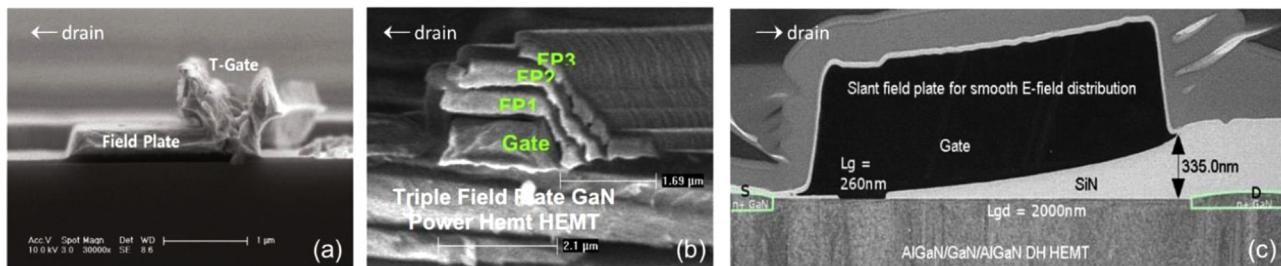
#### D. Ways to improve the breakdown voltage

##### 1. Field plate structures

AlGaN/GaN devices are based on a lateral design and a high-concentration two-dimensional electron gas. These features lead to an inhomogeneous electric field distribution in the OFF-state with a large peak at the gate electrode edge. If not treated properly, this results in the early breakdown of the device and in very limited voltage blocking capabilities.<sup>145–150</sup> To address the inhomogeneous electric field distribution, field plate (FP) structures are typically employed. As shown in Figs. 29(a)–29(d), the FP helps us to extend the depletion region from the gate to the drain electrode, alleviating the electric field peak at the gate edge. Various designs of field plates have been developed<sup>148,149,151</sup> (Figs. 29 and 30),

19 January 2025 21:33:19

FIG. 29. Schematics, equivalent circuits, and distributions of potential ( $\Phi$ ) and electric field ( $E$ ) in lateral GaN transistors in the OFF-state with (a) no FPs, (b) a single FP, (c) two FPs, and (d) a slant FP. Reproduced with permission from Ma and Matioli, IEEE Electron Device Lett. 38(9), 1305–1308 (2017). Copyright 2017 IEEE.



**FIG. 30.** Cross-sectional SEM images of (a) a single FP, (b) multiple FPs, and (c) a slant FP in GaN HEMTs. Image (a) reproduced with permission from Cho *et al.*, J. Kor. Phys. Soc. **67**(4), 682–686 (2015). Copyright 2015 Springer Nature.<sup>158</sup> Image (b) “[http://www.inrel-power.eu/sites/default/files/T05\\_Meneghesso-Reliability\\_PhD\\_Brixen\\_Jul\\_2017.pdf](http://www.inrel-power.eu/sites/default/files/T05_Meneghesso-Reliability_PhD_Brixen_Jul_2017.pdf)”.<sup>159</sup> Image (c) reproduced with permission from Wong *et al.*, IEEE Electron Device Lett. **38**(1), 95–98 (2017). Copyright 2017 IEEE.<sup>160</sup>

including the single FP, multiple FPs, and the slant field plate, which is the most effective but also very challenging to realize in a planar process. These structures are based on the precise control of the dielectric thickness, which sets the field plate threshold voltage and should be carefully designed. For high-voltage GaN devices (typically 650 V), several FP structures with increasing dielectric thickness are combined to smoothen the electric field profile.<sup>152</sup> Under this point of view, the tri-gate architecture provides an interesting solution for the design of the lower voltage section of the FPs since the fin width can be easily designed in a slanted shape by lithography to gradually increase its threshold voltage. This results in an optimal electric field distribution, which leads to significant breakdown voltage improvement.<sup>112,153</sup> Moreover, the ability to precisely tune the field plate threshold voltage is of great importance for AlGaN/GaN Schottky barrier diodes (SBDs) as it enables us to reduce the voltage drop on the Schottky contact and thus greatly improve the diode blocking performance.<sup>153–157</sup>

## 2. Buffer optimization: Superlattice buffer

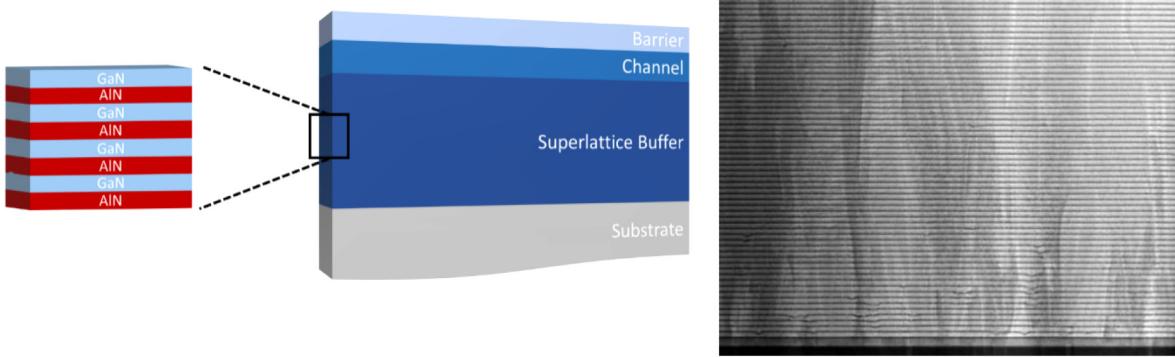
Unintentionally doped (UID) GaN buffer layers deliver insufficient resistivity for high-voltage operation due to the residual

n-type conductivity of GaN, which can induce parasitic leakage paths, thus increasing the OFF-state leakage current. As previously mentioned, high resistivity can be achieved by doping with deep acceptor impurities (such as C atoms) to compensate the background donors. However, this approach can generate severe current collapse, if the buffer is not carefully optimized.<sup>161–163</sup>

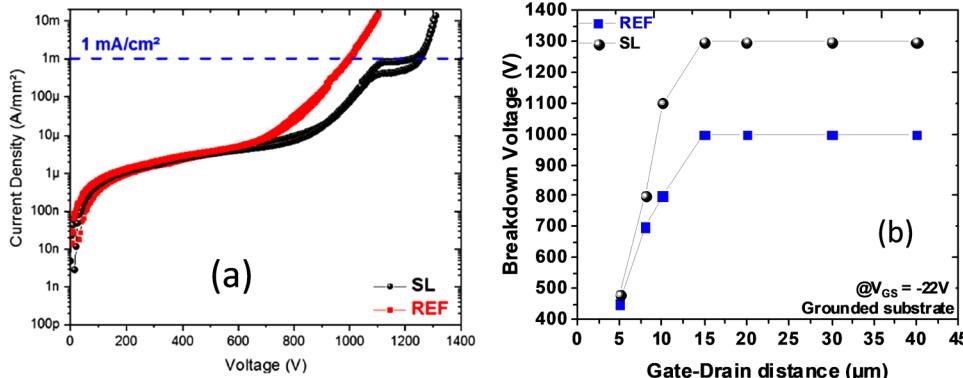
To further improve the carrier confinement while suppressing undesirable trapping effects, the doping compensation can be combined with the use of an AlGaN back barrier<sup>75</sup> or superlattices<sup>164,165</sup> consisting in AlN/GaN pairs (see Fig. 31). By alternating thin layers of high crystalline quality wide-bandgap semiconductors (e.g., AlGaN, AlN, or GaN), the accumulation of internal stress can be minimized, thus creating a highly insulating buffer with low buffer trapping effects.

Tajalli *et al.* showed that the insertion of superlattices (SL) into the buffer layers allows pushing the vertical breakdown voltage above 1200 V without generating additional trapping effects as compared to a more standard optimized step-graded AlGaN-based epi-structure using a similar total buffer thickness (see Fig. 32). Characterization of fabricated transistors by means of back-gating transient measurements reflects the much lower trapping effects and the advantages of the SL (Fig. 33).

19 January 2025 21:33:19



**FIG. 31.** Schematic cross section of a GaN HEMT using a superlattice-based buffer and TEM image of an AlN/GaN superlattice.



**FIG. 32.** (a) Vertical leakage curves and (b) breakdown voltage of a step-upgraded GaN carbon-doped buffer (REF) and a SL structure (black) at room temperature. Reproduced with permission from Tajalli *et al.*, Materials 13(19), 4271 (2020). Copyright 2020, licensed under CC BY 4.0.<sup>75</sup>

### 3. Local substrate removal

A limiting factor for the breakdown voltage of GaN-on-Si transistors is the poor critical electrical field strength of the Si substrate, together with a parasitic conduction at the buffer/substrate interface. In order to suppress the parasitic conduction phenomenon, local Si substrate removal (LSR)<sup>166</sup> has been shown to be very effective leading to significantly improved blocking voltage up to 3 kV.<sup>27,167</sup>

Dogmus *et al.* used the following device processing, which consists in ohmic contacts formed directly on top of the AlGaN barrier by rapid thermal annealing. After device isolation, a metal-insulator-semiconductor gate structure was employed by depositing an Ni/Au metal stack on top of the *in situ* SiN cap layer. Once the front-side processing was completed, the Si substrate is locally etched up to the AlN nucleation layer around the entire device (see Fig. 34). Devices with and without LSR have been fabricated on the same samples, eliminating any processing or epi variations during the device characterization. Electrical characterization showed a slight decrease of the maximum current density after LSR as can be

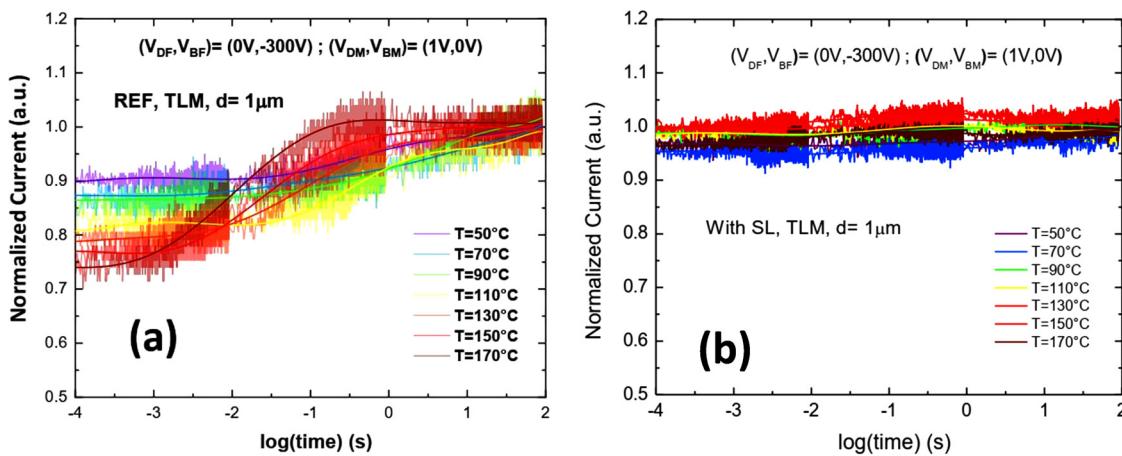
seen in Fig. 35 due to self-heating effects.<sup>35</sup> Further improvement of the heat dissipation would be required to avoid the decrease of the current density. On the other hand, a drastic enhancement of the blocking voltage is achieved by locally replacing the substrate with a wider bandgap material (Fig. 36).

Furthermore, the effects of Si removal were investigated by Raman thermometry,<sup>167,168</sup> which revealed a worsening of the thermal performance. A significant improvement of the thermal dissipation is obtained after the AlN and copper deposition.

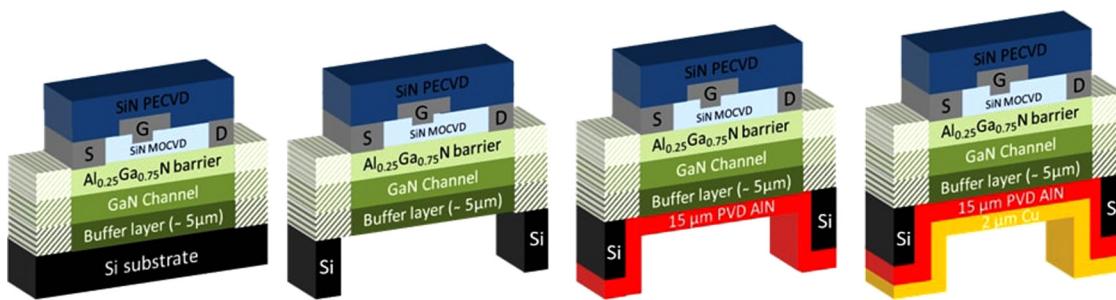
### E. Future perspectives

As the AlGaN/GaN power technology is reaching its maturity and increasing its market share, research on this topic is likely to follow two parallel paths. On the one hand, there will be growing interest on the aspects directly related to the realization of a successful commercial product such as trapping, reliability, stability, packaging, and circuit operation. On the other hand, researchers will continue to come up with novel device structures and designs to improve performance and take full advantage of the GaN

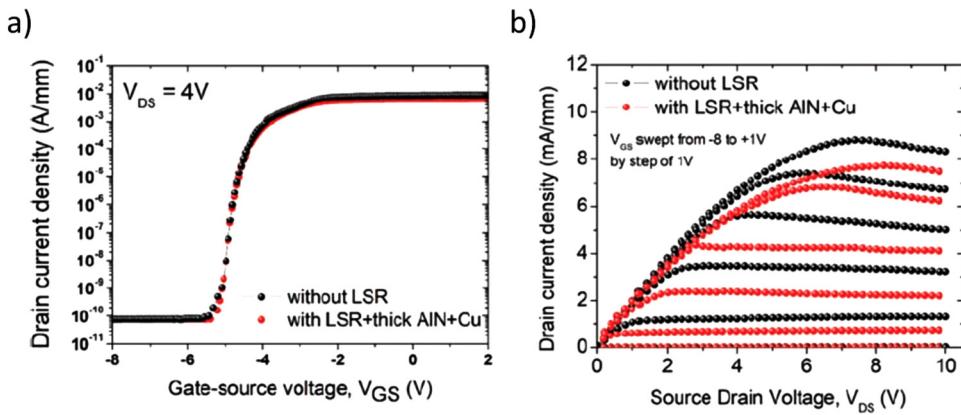
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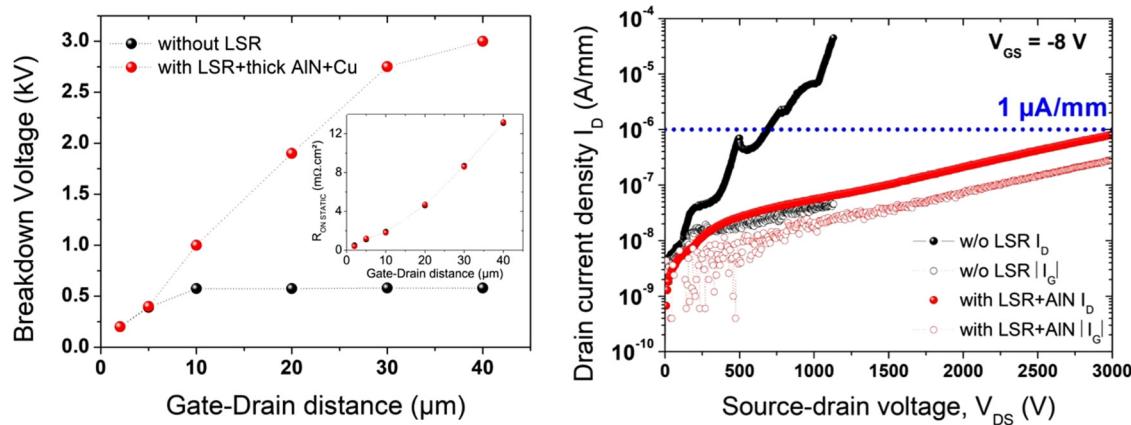
**FIG. 33.** Current transient behavior at multiple temperatures up to 170 °C using a 1 μm distance TLM on (a) a step-upgraded buffer and (b) a super-lattice buffer. Reproduced with permission from Tajalli *et al.*, Materials 13(19), 4271 (2020). Copyright 2020, licensed under CC BY 4.0.<sup>75</sup>



**FIG. 34.** Schematic cross section of AlGaN/GaN MISHEMT including the front-side process, the LSR technique, a thick PVD AlN, and metal backside deposition. Reproduced with permission from Dogmus *et al.*, Appl. Phys. Express 11(3), 034102 (2018). Copyright 2018, licensed under CC BY 4.0.<sup>27</sup>



**FIG. 35.** (a) Transfer and (b) output characteristics of GaN-based MISHEMTs with and without LSR/backside AlN and Cu. Reproduced with permission from Dogmus *et al.*, Appl. Phys. Express 11(3), 034102 (2018). Copyright 2018, licensed under CC BY 4.0.



**FIG. 36.** (Left) Evolution of  $L_{GD}$ -dependent device  $V_{BR}$  and specific on-resistance (inset) of AlGaN/GaN HEMTs with and without LSR by defining the blocking voltage at  $I_D = 1 \mu\text{A}/\text{mm}$  and (right) off-state leakage current characteristics of AlGaN/GaN MISHEMTs with and without LSR. Reproduced with permission from Dogmus *et al.*, Appl. Phys. Express 11(3), 034102 (2018). Copyright 2018, licensed under CC BY 4.0.<sup>27</sup>

19 January 2025 21:33:19

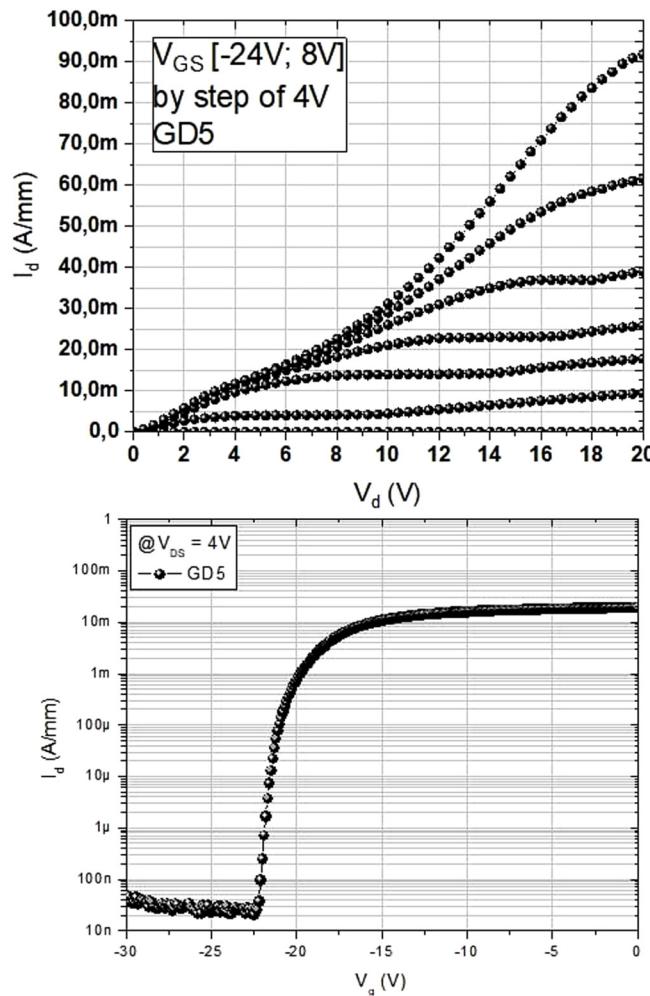
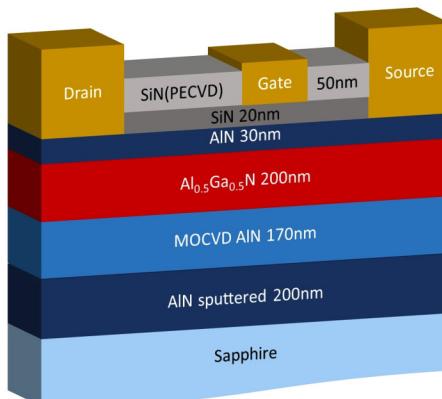
material properties for future generations of high-efficiency devices. Under this point of view, a few recent promising directions are presented below, which are rapidly growing and offer a significant advance in device performance.

### 1. AlGaN channel HEMTs

Ultra-wide-bandgap materials such as AlN (6.2 eV) and related Al-rich AlGaN channel could allow for further improvement, especially in terms of voltage and temperature operations. This is primarily due to their much higher critical electric field resulting from a wider bandgap (see Fig. 3). In addition, the use of an AlN back barrier would enable us to both increase the electron confinement in the transistor channel and enhance the thermal dissipation. It has already been demonstrated that for extremely high-temperature electronics, the properties of Al-rich transistors<sup>169–171</sup>

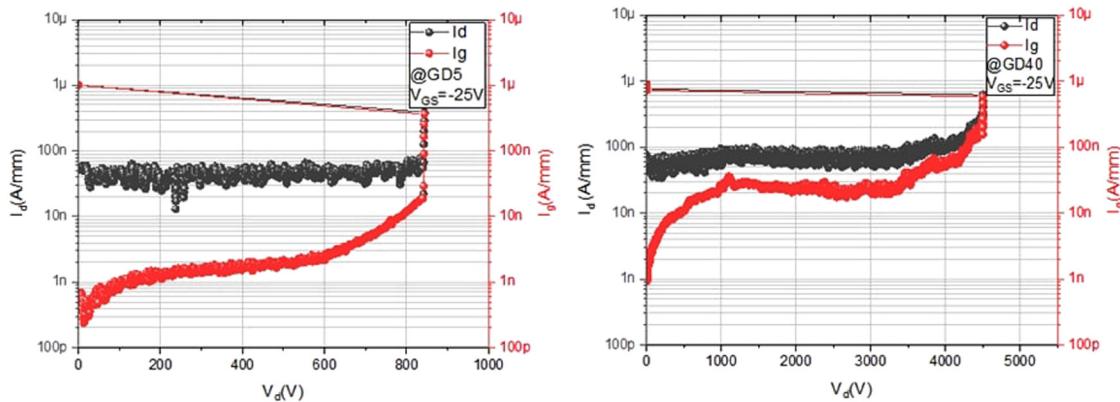
show favorable comparisons to conventional wide-bandgap materials. Despite the difficulty to achieve very high-voltage operations due to the material quality and the ability to implement high Al content above 50%, some recent attempts showed the premise of voltage enhancement with AlGaN channels together with superior thermal stability.

Abid *et al.* used an AlN barrier on top of an Al<sub>50</sub>Ga<sub>50</sub>N channel grown on an AlN/sapphire template (Fig. 37). The heterostructure provides a high carrier concentration close to  $1.9 \times 10^{13} \text{ cm}^{-2}$  with a rather limited electron mobility of  $145 \text{ cm}^2/\text{V s}$ . Low leakage current is obtained without the use of any field plates, confirming that tunneling mechanisms are not present in Al-rich transistors. In general, Al-rich transistors are less prone to gate leakage than AlGaN/GaN HEMTs. Despite the rather high defect density, a blocking voltage above of 4000 V with an OFF-state leakage current below  $0.1 \mu\text{A}/\text{mm}$  is achieved for AlGaN-based channel HEMTs (Fig. 38). It can be



19 January 2025 21:33:19

**FIG. 37.** Schematic cross section and typical transfer characteristic at  $V_{DS} = 4$  V of an Al-rich AlN/AlGaN/AlN HEMTs. Reproduced with permission from Abid *et al.*, 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD) (IEEE, 2020), pp. 310–312. Copyright 2020 IEEE.<sup>172</sup>



**FIG. 38.** Three-terminal breakdown voltage of AlN/AlGaN/AlN with  $L_{GD} = 5\text{ }\mu\text{m}$  (GD5) (left) and  $L_{GD} = 40\text{ }\mu\text{m}$  GD40 (right). Reproduced with permission from Abid *et al.*, 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD) (IEEE, 2020), pp. 310–312. Copyright 2020 IEEE.<sup>172</sup>

noticed that low gate-drain distance of  $5\text{ }\mu\text{m}$  yields a breakdown field of  $3.5\text{ MV/cm}$ , which is well beyond that of SiC and GaN devices. Furthermore, these transistors show a very stable behavior as a function of temperature, with no threshold voltage variation and low OFF-state leakage increase up to  $200\text{ }^{\circ}\text{C}$ .

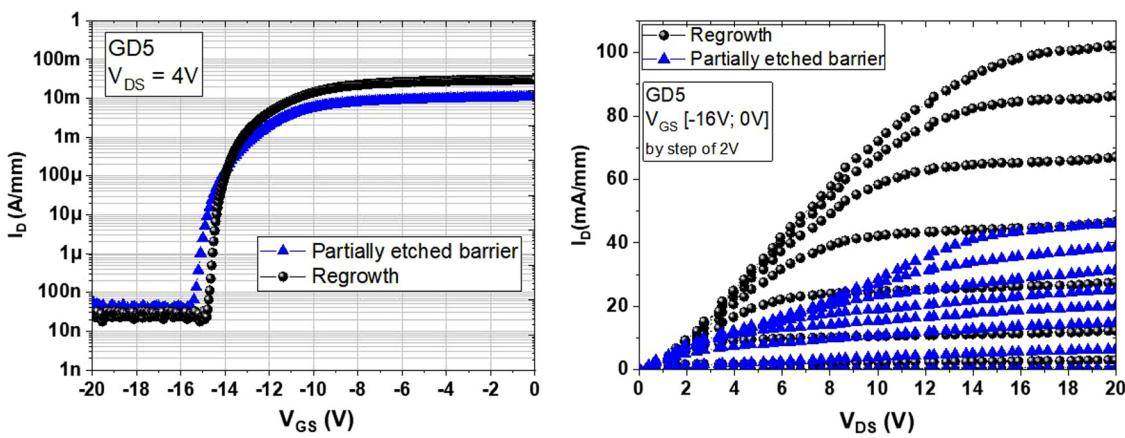
One of the major challenges limiting the research progress of Al-rich AlGaN transistors is the optimization of ohmic contacts. High resistance of the source and drain electrodes and the possible Schottky-like behavior lead to a reduced current density. Low resistance ohmic contacts are fundamental performance enablers in wide-bandgap HEMTs. Several approaches<sup>174–177</sup> are under development to mitigate this issue, namely, based on tuning the heterostructure and/or the subsequent annealing. For instance, regrown ohmic contacts using a  $\text{SiO}_2$  mask can be applied. The reduction of the contact resistances has been verified at the transistor level. Output characteristics of transistors with regrown non-alloyed

contacts showed a significant current density increase above  $100\text{ mA/mm}$  as compared to identical devices with partially etched barrier and annealed contacts (see Fig. 39). This is clearly resulting from the drastic drop of the contact resistances. In spite of these obstacles, preliminary results show that contact resistivity will improve over time and that advanced approaches such as the etch and regrowth processes will ensure successful achievement at even higher Al-composition.

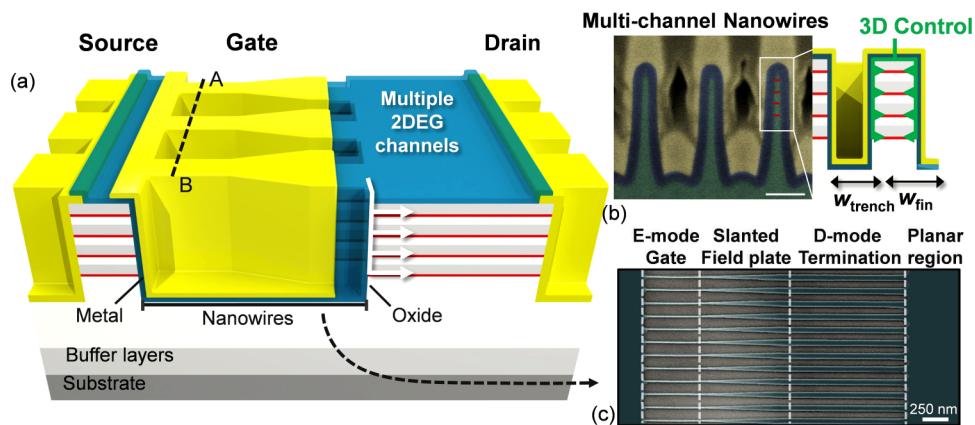
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## 2. Multi-channel devices

Despite the recent progress, the performance of AlGaN/GaN devices is still far from the theoretical limit predicted for the GaN materials.<sup>179</sup> A direct way to improve the device's performance is represented by increasing its carrier concentration, which directly leads to a reduced ON-resistance. Yet, achieving a large  $n_s$  leads to



**FIG. 39:** Transfer characteristics (left) and output characteristics (right) of AlN/AlGaN/AlN HEMTs using regrown ohmic contacts and partially etched barrier. Reproduced with permission from Abid *et al.*, Electronics **10**(6), 635 (2021). Copyright 2021, licensed under CC BY 4.0.<sup>173</sup>



**FIG. 40.** (a) Three-dimensional schematics of the multi-channel power device, featuring multiple parallel channels, controlled three-dimensionally by a tri-gate electrode. (b) FIB cross section and schematics of the multi-channel nanowires covered by the tri-gate structure along the AB line in (a). The scale bar is 100 nm. (c) Top SEM image of the tri-gate area that includes, starting from the source side, an e-mode region achieved by 15 nm-wide nanowires, and a slanted region terminated on 100 nm-wide d-mode nanowires for optimal electric field management. Reproduced with permission from Nat. Electronics, Nela *et al.*, Nat. Electron. 4(4), 284–290 (2021). Copyright 2021 Springer Nature.

19 January 2025 21:33:19

major challenges for the heterostructure and device design. First, a large  $n_s$  severely impacts the mobility ( $\mu$ ) due to the increased electron-to-electron scattering, limiting the reduction of the heterostructure  $R_{\text{sh}}$ . Second, a large  $n_s$  leads to a difficult control of the channel, which results in negative  $V_{\text{TH}}$  and degrades the device voltage blocking capability.

A promising approach to address these challenges is represented by the use of a multi-channel heterostructure, in which several barrier/channel layers are stacked to achieve multiple 2DEGs<sup>180–183</sup> [Fig. 40(a)]. This allows us to distribute a large  $n_s$  in several parallel channels, thus overcoming the trade-off between  $n_s$  and  $\mu$  and considerably increasing the heterostructure conductivity. However, the multi-channel heterostructure can be combined with a tri-gate architecture, which allows us to gain excellent control over all of the embedded channels and manage the large OFF-state electric field (Fig. 40).

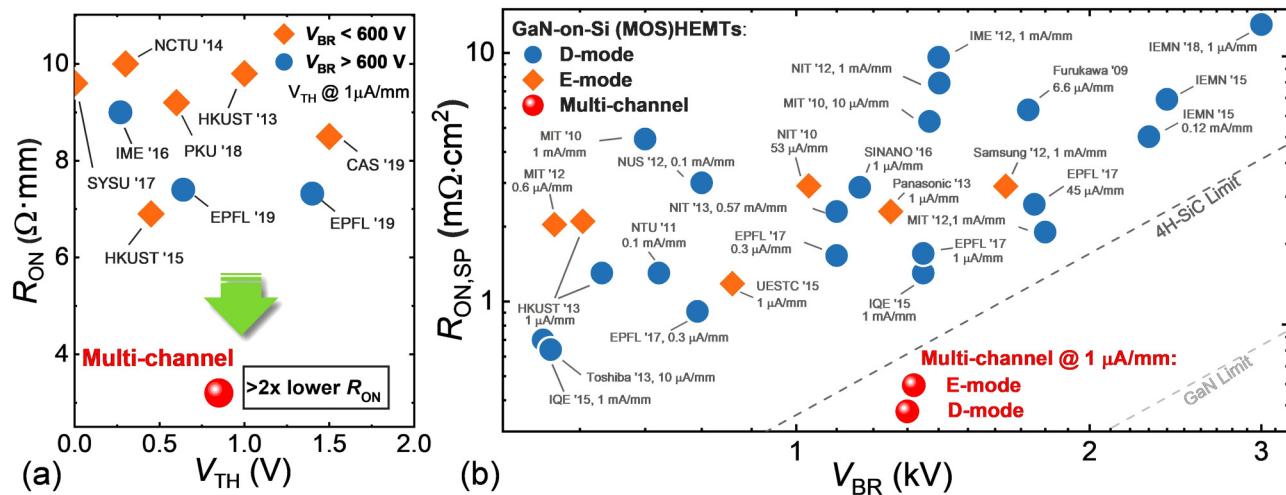
Since multi-channel devices have first been proposed for RF applications,<sup>184–187</sup> there has been a growing interest in their use in power electronics applications. However, power devices present very specific requirements such as normally OFF operations, large blocking voltage capabilities, and good stability during switching operation, which need to be separately addressed and solved. The first multi-channel power HEMT was reported in 2018,<sup>188</sup> followed by the demonstration of a high-voltage multi-channel SBD.<sup>189</sup> While these early works showed the concept of multi-channel power devices, their performance improvement was still quite limited due to the relatively high sheet resistance ( $\sim 240 \Omega/\text{sq}$ ) of the multi-channel heterostructure employed. More recent works,<sup>178,190,191</sup> however, showed the full potential of the multi-channel technology for power devices. By employing a highly conducting multi-channel heterostructure ( $R_{\text{sh}}$  of  $83 \Omega/\text{sq}$ ) in combination with a carefully designed slanted tri-gate structure, multi-channel power devices showing a normally OFF operation with a  $V_{\text{TH}}$  of  $0.85 \text{ V}$  (at  $1 \mu\text{A}/\text{mm}$ ), ON-resistance of  $3.2 \Omega \text{ mm}$ , and

breakdown voltage of  $1300 \text{ V}$  (at  $1 \mu\text{A}/\text{mm}$ ) were demonstrated.<sup>178</sup> Such a performance considerably surpasses the state-of-the-art conventional single-channel devices and opens new perspectives for GaN power devices (Fig. 41). Moreover, multi-channel devices passivated by low-pressure chemical vapor deposition (LPCVD)  $\text{Si}_3\text{N}_4$  presented reduced current collapse up to high-voltage stress and excellent  $V_{\text{TH}}$  stability both during switching and high-temperature operation, showing the potential of such technology.<sup>192</sup> Further research on this topic will likely concentrate on the optimization of the multi-channel heterostructure and on additional methods to achieve large positive  $V_{\text{TH}}$ .

### 3. Superjunctions

Superjunction (SJ) devices have revolutionized silicon power devices leading to unprecedented performance well beyond the one-dimensional material limit.<sup>194,195</sup> It is thus likely that eventually power devices based on other semiconductor material will embrace this technology too. In particular, the demonstration of SJs realized with wide-bandgap (WBG) semiconductors would result in a major further improvement for the performance of power devices.<sup>196–198</sup>

The realization of conventional vertical SJ (Fig. 42) in GaN is, however, not straightforward due to difficult technological challenges, among which the inefficient Mg-based p-doping of GaN is one of the most relevant. On the one side, the reduced Mg activation ratio results in relatively low doping concentrations, which, combined with the difficult control of the exact doping level, make charge-matching extremely challenging. On the other side, the absence of efficient implantation doping and high-quality p-GaN regrowth hinders the realization of the typical vertical SJ pillars. These challenges make the demonstration of vertical GaN SJ devices still out of reach and, until more efficient p-GaN doping is achieved, it is unlikely that this technology could progress significantly.



**FIG. 41.** (a)  $R_{ON}$  vs  $V_{TH}$  benchmark for the multi-channel device against state-of-the-art power devices.  $V_{TH}$  has been defined at  $1 \mu\text{A}/\text{mm}$ . (b)  $R_{ON,SP}$  vs  $V_{BR}$  benchmark for normally off and D-mode multi-channel devices with respect to state-of-the-art GaN-on-silicon (MOS)HEMTs. Reproduced with permission from Nat. Electronics, Nela et al., Nat. Electron. 4(4), 284–290 (2021). Copyright 2021 Springer Nature.

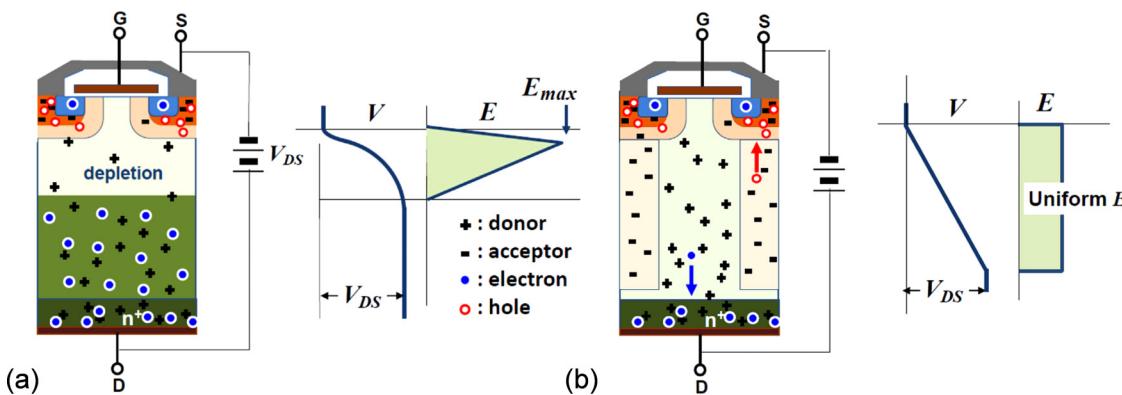
Yet, alternative solutions to realize SJ devices have been proposed in AlGaN/GaN lateral architectures. In these structures, it is possible to obtain two-dimensional electron and hole gas (2DEG and 2DHG) of equal concentration, thanks to the presence of matching polarization charges. Such devices are typically referred to as polarization superjunctions (PSJs) (Fig. 43) and can result in similar behavior to conventional, doping-based SJs, thus yielding much improved OFF-state performance. While these devices were first proposed in 2008,<sup>199–201</sup> technical challenges in achieving a good match between the 2DEG and 2DHG concentrations have decelerated the development of this technology. After some years, the research on this subject has regained a strong interest and several works have recently appeared on this topic,<sup>193,202–204</sup>

providing further insight into the device's working principle and showing its potential. Fast development of this field in the forthcoming years is thus expected, which could result in a new generation of GaN superjunction devices.

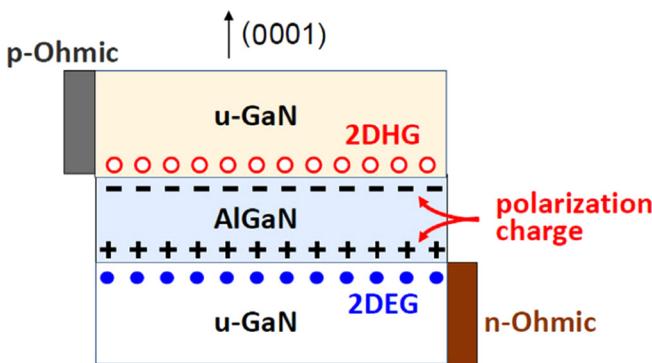
#### 4. N-polar GaN HEMTs

In most cases, III-nitride devices are manufactured along the Ga-polar (0001) orientation, as extensively discussed in Sec. II. Significant research efforts are under way to develop devices with inverted polarity: N-polar HEMTs (000-1) can have several advantages, compared to the Ga-polar counterparts, due to the fact that the 2DEG is induced above (instead of below) the AlGaN barrier

19 January 2025 21:33:19



**FIG. 42.** Schematic of the cross section of a conventional power MOSFET (a) and a super junction device (b) with the corresponding electric field distribution under OFF-state conditions. Reproduced with permission from Kawai et al., Phys. Status Solidi A 214(8), 1600834 (2017). Copyright 2017 Wiley-VCH Verlag GmbH & Co. KGaA.



**FIG. 43.** Schematic illustration of a PSJ structure. Reproduced with permission from Kawai *et al.*, Phys. Status Solidi A **214**(8), 1600834 (2017). Copyright 2017 Wiley-VCH Verlag GmbH & Co. KGaA.

layer,<sup>205,206</sup> with a stack including a GaN channel, an AlGaN barrier, and a GaN buffer.

As discussed in Ref. 205, the advantages of N-polar devices include (a) a strong back barrier (created by the AlGaN layer) that can minimize short channel effects;<sup>207</sup> (b) a low-resistivity ohmic contact, thanks to the fact that the 2DEG is contacted through the channel layer, having a narrower bandgap and lower surface barrier to electrons;<sup>208,209</sup> and (c) improved scalability, thanks to the fact that in N-polar devices the electron wavefunction spread reduces the gate–channel distance. This is contrary to Ga-polar transistors, where the wavefunction extension increases the effective gate–channel distance.<sup>210</sup>

Recent reports<sup>206,211</sup> demonstrated that N-polar devices (typically investigated for mm-wave operation) can be of interest also for power switching applications. Lateral<sup>206</sup> and vertical<sup>211</sup> device architectures have been evaluated, and breakdown voltages in excess of 2000 V were observed in HEMTs with a gate–drain distance of 28  $\mu\text{m}$ .

## VI. VERTICAL GaN DEVICE STRUCTURES

### A. Why vertical GaN?

The most common GaN-based power devices available presently are GaN HEMTs, which have been discussed in detail in Secs. II–V. GaN HEMTs rated for 650/900 V breakdown voltage (BV) and maximum output DC current ( $I_{\text{DS}}$ ) as high as 150 A are available commercially<sup>212–214</sup> for a broad spectrum of applications, such as on-board battery chargers, high-efficiency and high-density power converters, and solar panel inverters, among many others. However, the lateral topology of HEMTs presents some pertinent limitations related to reliability and breakdown voltage scaling, which hinder the usability of these devices for high-voltage applications requiring breakdown voltages above 700 V, for example, in electric and hybrid electric vehicles (EVs and HEVs), photovoltaic (PV) inverters, wind turbines, and traction systems for trains, to name a few.

Most of the limitations associated with GaN HEMTs arise from the lateral electron flow between the source and drain

terminals, very close to the device surface. The density of electrons in the channel is sensitive to the presence of surface traps that may degrade the electrical performance<sup>215–217</sup> of the transistors. This leads to issues like current collapse and dynamic degradation of the ON-resistance, which are more severe with increasing the BV rating of the device (see Secs. VII B and VIII). In addition, the lateral nature of the transport results in a very inhomogeneous distribution of the electric field in the device, peaking in specific regions (e.g., the edge of the gate, or of the field plate, on the drain side). This may enhance electron trapping at surface states and may lead to premature breakdown of the semiconductor and the dielectrics. This ultimately degrades the forward and reverse performance of the device<sup>217,218</sup> and limits its full voltage blocking potential. For traditional GaN HEMTs, the BV is dictated by the gate to drain spacing (provided this value is smaller than the drain-to-substrate BV), and thus larger breakdown voltages require larger device sizes, which also increases the device cost. Another major concern is that GaN HEMTs are, in general, normally ON devices: this is not desirable for power electronics applications from a safety perspective and for simplicity of the gate drivers, which are currently designed for normally OFF devices. As discussed in Sec. V B, several methods to achieve a normally OFF operation have been developed including cascode<sup>219–221</sup> configuration (based on GaN HEMT combined with a Si MOSFET), fluorine ion implantation<sup>81,91,97</sup> under the gate region, recessing the barrier layer<sup>84</sup> in the gate region, and by applying tri-gate structures<sup>111,112,121,122,190</sup> to the gate region, among others. However, in many cases and even for commercial devices, the threshold voltage ( $V_{\text{th}}$ ) that can be achieved is only around 1–2 V, which may not be ideal for fail-safe operations. Finally, GaN HEMTs do not present avalanche capability, which can prevent device failure under short term overvoltage conditions. Thus, for a GaN HEMT to qualify for a certain BV rating, the device has to be overdesigned to sustain a much higher BV, which increases the device size and cost.

Vertical GaN power devices are different from their lateral counterparts as the current flows vertically, i.e., parallel to the growth direction of the epitaxial GaN layers. The vast majority of the Si and SiC power devices available commercially are based on this design philosophy and are capable of delivering high ON-state currents (>7000 A) and high BVs (>8000 V).<sup>222</sup> For GaN, the vertical topology offers distinct advantages over lateral power HEMTs. The BV can be increased by increasing the thickness of the voltage blocking layer, generally formed by an unintentionally or low doped GaN layer (also referred to as the drift layer or i-GaN layer), independent of the size of the device. The  $R_{\text{ON}}$  in p-i-n diodes increases only slightly<sup>223</sup> with increasing the thickness of the drift layer as a result of extrinsic phenomena like conductivity modulation.<sup>224,225</sup> Vertical devices are also not affected by surface traps as in GaN HEMTs, and the electric field peaks well inside the GaN layers, away from the surface, thus improving the device breakdown voltage and reliability. In addition, vertical MOSFETs can provide high positive  $V_{\text{th}}$  of 5–15 V, which is well suited for higher power applications like in automobiles. Another major advantage is the existence of avalanche breakdown<sup>226–228</sup> for GaN vertical power devices. This greatly improves the reliability and eliminates the need to overdesign the device.

## B. Choice of substrate

The ideal solution for obtaining high-quality GaN epitaxial layers is by homoepitaxy, i.e., GaN layers grown on bulk GaN substrates. These substrates are mainly produced by hydride vapor-phase epitaxy (HVPE), although several other methods like Na-flux or ammonothermal growth are currently being investigated.<sup>229–234</sup> The major advantages of growing GaN by homoepitaxy are their low dislocation density of  $10^4$ – $10^6/\text{cm}^2$  and the inherently matched lattice and coefficient of thermal expansion (CTE) to the grown GaN layers. As a result, thick GaN layers suitable for achieving high-voltage ( $\sim 5000\text{ V}$ )<sup>235,236</sup> vertical power devices can be easily grown on these substrates. The downside is that these substrates are very expensive, at about  $50\$/\text{cm}^2$ , and mostly available in small 2-in. wafer diameters;<sup>237</sup> strategies for larger size substrates are currently under investigation.<sup>229,238</sup> This hinders the widespread commercialization of devices grown on bulk GaN. The bulk GaN market is also highly concentrated, as three companies based out of Japan hold about 85% stake in the bulk GaN market.<sup>239</sup> Currently, these expensive substrates are being used only for special applications, like laser diodes and high-brightness LEDs,<sup>239</sup> for which low dislocation densities are essential. Hence, in order to take advantage of the material benefits offered by GaN materials for power device applications, further improvements in wafer size and reduction in cost are highly desirable. However, over the past decade, improvements in wafer size have been relatively slow, which is a critical aspect for reducing the production cost per device. A strategy to tackle this issue would be by heteroepitaxy, i.e., GaN layers grown on foreign substrates like Si, SiC, and sapphire, which are cheaper than bulk GaN and are available up to 12-in. diameters.<sup>240,241</sup> However, these substrates are both lattice and CTE mismatched to GaN, as shown in Table VI. This results in a high defect density in the GaN crystalline structure as a result of the stress built up during growth. The growth of thick layers of GaN ( $>7\mu\text{m}$ ) on 6-in. Si substrates also results in significant wafer bowing and cracking.<sup>237,242,243</sup> Thus, further improvements in the dislocation density and investigation of stress-relaxation buffer layers for the growth of thick GaN layers on these substrates are essential.

The majority of the reported GaN vertical power devices are based on bulk GaN substrates as a result of their low dislocation density, which provide a fair representation of the superior material properties of GaN as compared to Si. Even though these bulk GaN substrates have a defect density higher than Si or SiC, these devices have been shown to pass reverse leakage tests, high temperature reverse bias (HTRB), high temperature operating life (HTOL), temperature humidity bias (THB), temperature cycling (TC), and inductive avalanche ruggedness stress tests,<sup>245</sup> which is of paramount importance from the point of view of commercialization of these devices in the future. This section aims to summarize the

research development on vertical GaN devices, providing an extensive review encompassing the fabrication and performance of various vertical devices reported until today. The development of vertical devices on sapphire and bulk GaN will be first presented followed by the recent development of GaN-on-Si vertical devices.

## C. Vertical device architectures

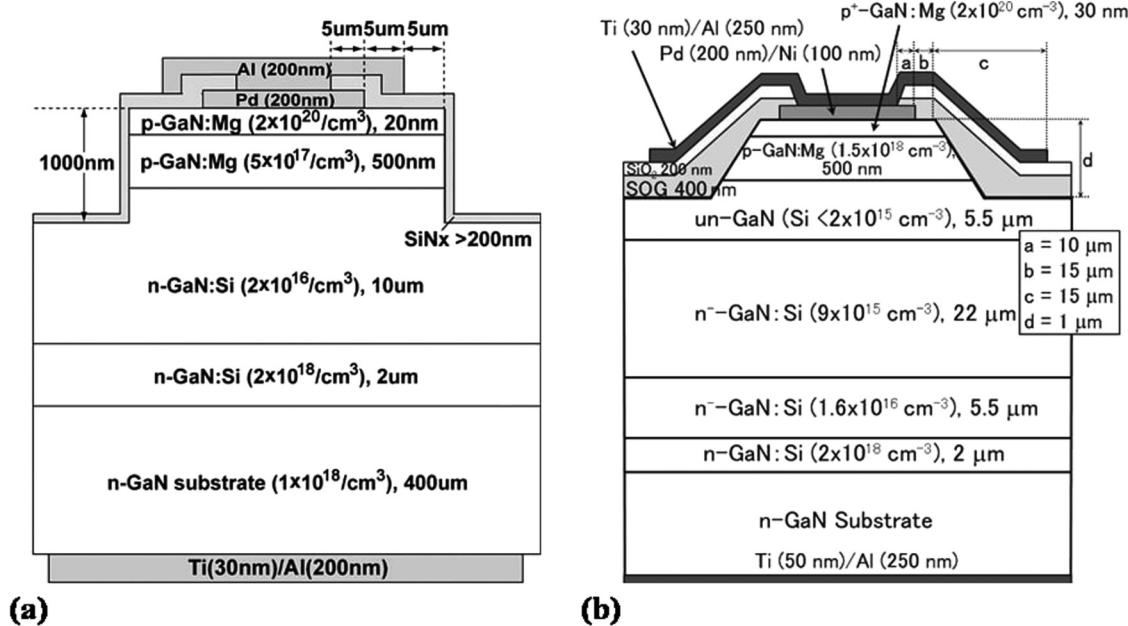
### 1. Development of vertical devices on sapphire and bulk GaN

*a. p-i-n diodes.* P-i-N junctions are ubiquitous structures that compose many electronic devices. In wide-bandgap semiconductors, however, the large turn-on voltage and high reverse recovery times of such diodes due to the large bandgap hinders their applications in efficient power electronics. Even though Schottky diodes are preferable in power applications, due to their low turn-on voltage and reverse recovery time during switching transients, p-n junctions are also an integral part of a number of modern vertical power devices, including IGBTs, junction barrier Schottky (JBS) diodes, merged p-i-n Schottky diodes, junction termination extensions (JTEs), etc., and thus merits a comprehensive study. Furthermore, the well-known and simple physics of p-n junctions is helpful in elucidating various material parameters, such as the critical electric field ( $E_c$ ), doping density, impact ionization coefficients, generation-recombination rates, mobility of electron and holes, temperature related effects, etc.<sup>246</sup> These properties are of utmost importance for designing and understanding of the power device.

The first report on GaN power p-i-n diodes on sapphire substrates date back to 2000<sup>248,249</sup> and the first GaN p-i-n diodes on bulk GaN substrates were reported in 2005.<sup>250</sup> However, high-voltage p-i-n diodes with  $\text{BV} > 1\text{ kV}$  were reported only in 2011.<sup>251</sup> Rapid developments in the growth and fabrication of p-i-n diodes ensued, mainly by start-ups like Avogy Inc. and researchers from institutions like Cornell University, Hosei University, Toyoda Gosei, etc.<sup>246,252–255</sup> The schematic of a p-i-n diode with  $\text{BV}$  of  $1100\text{ V}$ <sup>247</sup> as reported by Hosei University is shown in Fig. 44(a). A mesa termination with  $\text{SiO}_2$  passivation and a field plate structure were employed to improve the  $\text{BV}$  from  $\sim 450$  to  $1100\text{ V}$  along with a small  $R_{\text{ON},\text{sp}}$  (given by  $R_{\text{ON}} \times$  active area of the device) of  $0.4\text{ m}\Omega\text{ cm}^2$ , thus achieving an excellent Baliga's figure of merit  $(\text{BFOM} = \frac{\text{BV}^2}{R_{\text{ON},\text{sp}}}) > 3.0\text{ GW/cm}^2$ . Subsequently, a low-damage field plate process involving the use of a bilayer spin-on-glass (SOG)/sputtered  $\text{SiO}_2$  as the field plate dielectric along with a drift layer thickness of  $20\mu\text{m}$  was developed to achieve the first demonstration of GaN p-i-n diodes with very high  $\text{BV}$  of over  $3\text{ kV}$ .<sup>253</sup> The SOG protected the p-GaN anode contact area from damages related to the  $\text{SiO}_2$  sputtering process. A low  $R_{\text{ON},\text{sp}}$  of  $0.9\text{ m}\Omega\text{ cm}^2$  along

**TABLE VI.** Comparison of material properties of GaN grown on various substrates.<sup>244</sup>

Parameter	GaN-on-Si	GaN-on-SiC	GaN-on-sapphire	GaN-on-GaN
Defect density	$\sim 10^9/\text{cm}^2$	$\sim 5 \times 10^8/\text{cm}^2$	$\sim 10^9/\text{cm}^2$	$\sim 10^4$ – $10^6/\text{cm}^2$
Lattice mismatch (%)	17	3.5	16	0
CTE mismatch (%)	54	25	34	0



**FIG. 44.** (a) Schematic cross sections of the GaN p-n junction diodes with SiNx passivation and the FP structure. Reproduced with permission from Hatakeyama *et al.*, IEEE Electron Device Lett. **32**(12), 1674–1676 (2011). Copyright 2011 IEEE. (b) Schematic cross sections of the GaN p-n junction diodes with the triple drift layers and the FP structure. Reproduced with permission from Ohta *et al.*, IEEE Electron Device Lett., **36**(11), 1180–1182 (2015). Copyright 2015 IEEE.

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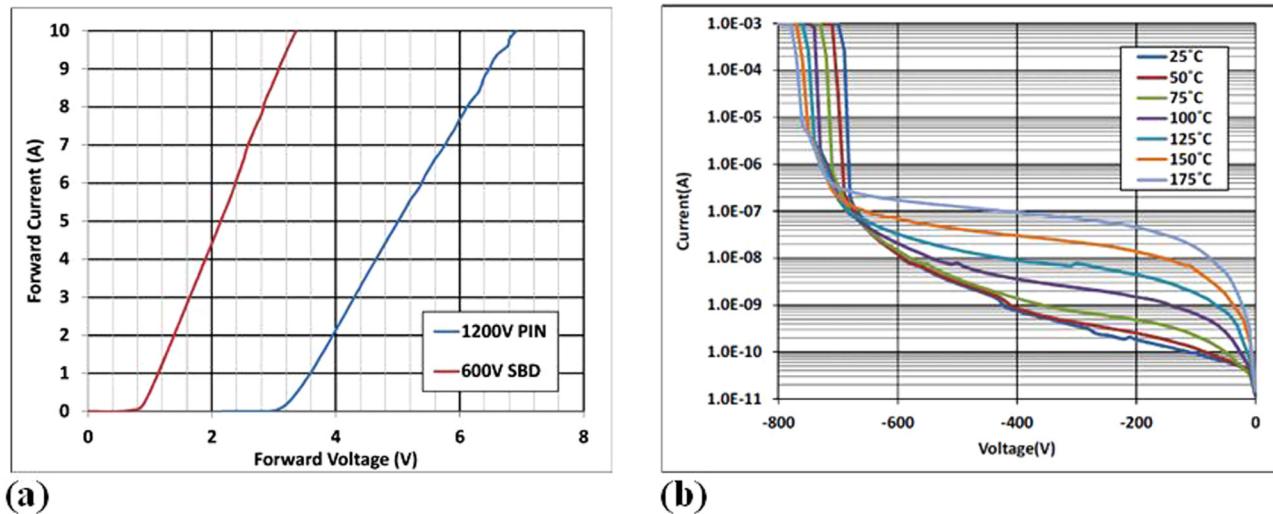
with this high BV resulted in record BFOM of  $10 \text{ GW/cm}^2$  in 2013. A p-i-n diode<sup>236</sup> with a triple drift layer to improve the distribution of the electric field was proposed in 2015 [Fig. 44(b)]. The drift layer forming the p-n junction was doped to low  $10^{15}/\text{cm}^3$  to create a near-flat electric field profile and thus reduce the electric field. Subsequent drift layers were moderately doped to reduce the  $R_{\text{ON},\text{sp}}$  to  $1.7 \text{ m}\Omega \text{ cm}^2$ , while still presenting a high BV of 4.7 kV. In 2018, a novel p-i-n diode with a guard-ring termination<sup>235</sup> was presented, which resulted in lower leakage current and an improvement in BV by 200 V to obtain a high blocking voltage of 5 kV.

Avogy Inc. first reported on the avalanche capability in p-i-n diodes with BV of 2.6 and 3.7 kV<sup>246,252</sup> (Fig. 45). The device structure is as shown in Fig. 46(a). An ion-implantation-based proprietary edge termination was employed for better redistribution of electric field peaks to realize breakdown voltages approaching 85% of that in theoretical parallel-plane junction breakdown and also to achieve avalanche capability. The role of substrate orientation on the reverse leakage current and reliability of the devices revealed that a slight miscut angle of several tenths of a degree is very beneficial. This results in the elimination of hillocks on the surface of the as-grown GaN layers and reveals a surface with a smooth morphology, which is essential for achieving reliable devices with low reverse leakage currents<sup>246</sup> [Fig. 46(b)]. These devices were qualified with HTRB, THB, HTOL, and TC tests, indicating that even with a defect density of  $10^4$ – $10^6/\text{cm}^2$ , GaN vertical devices could be adopted for fast commercialization.<sup>245</sup> Avogy p-i-n diodes also fared extremely well against Si fast diodes when used in power converter topologies, like the hard-switched boost circuit with little or

no ringing as well as no reverse recovery loss as compared to the Si fast diodes.<sup>257,258</sup> They also demonstrated large-area  $16 \text{ mm}^2$  p-i-n diodes with current capability of 400 A in a pulsed operation.<sup>259</sup> These diodes provided 100 A at 4.5 V forward bias in DC operation together with an excellent BV of 700 V.

Cornell University demonstrated the growth of high-quality GaN layers by metalorganic chemical vapor deposition (MOCVD) resulting in a Shockley–Read–Hall (SRH) lifetime of 12 ns. As a consequence, their p-i-n diodes exhibited ultra-low  $R_{\text{ON},\text{sp}}$  of  $0.12 \text{ m}\Omega \text{ cm}^2$  coupled with a high BV of 1.4 kV, thus resulting in a BFOM of  $16.5 \text{ GW/cm}^2$ .<sup>260</sup> GaN p-i-n diodes incorporating a bevel termination and a long field plate were also presented in 2015 with an improvement in BV by more than threefold to  $\sim 4 \text{ kV}$ ,<sup>261</sup> as compared to a p-i-n diode with no termination. In order to circumvent the issues faced during p-GaN growth by MOCVD, like the Mg memory effect and the hydrogen passivation of Mg dopants in p-GaN, high BV GaN p-i-n diodes with molecular beam epitaxy (MBE) grown p-GaN were also reported.<sup>262,263</sup> This study also provides an alternative strategy for p-GaN regrowth by MOCVD, which could result in impurity incorporation at the growth interface and issues arising from non-planar growth, like high leakage currents.<sup>254,255,264</sup>

Arizona State University reported on the beneficial effects of growing a thick buffer layer of about  $1 \mu\text{m}$  on the bulk GaN substrate prior to subsequent growth.<sup>266</sup> They also investigated in detail the regrowth of p-GaN layers on etched GaN surfaces.<sup>254,267</sup> Regrowth of p-GaN is an important topic, especially since ion implantation schemes for the realization of JTE (junction



**FIG. 45.** (a) Forward  $I$ - $V$  characteristics of SBDs and p-i-n diodes. Reproduced with permission from Disney *et al.*, 2013 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD) (IEEE, 2013), pp. 59–62. Copyright 2013 IEEE.<sup>256</sup> (b) Reverse  $I$ - $V$  characteristics of the p-i-n diodes as a function of temperature with BV demonstrating positive temperature coefficient indicative of avalanche breakdown. Reproduced with permission from Hirao *et al.*, “Low reverse recovery charge 30-V power MOSFETs for DC-DC converters,” 2013 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD) (IEEE, 2013), pp. 221–224. Copyright 2013 IEEE.

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termination extension) structures similar to Si and SiC carbide vertical power devices are very complicated in GaN and still not available. The study revealed that the regrowth process could result in a slight increase in the edge dislocations and a high concentration of Si and O impurity atoms at the growth interface [Fig. 47(a)]. In a subsequent work,<sup>267</sup> the reason for this high impurity atom concentration was shown to be from the defective etching process, and a low power etching coupled with UV-ozone/acid treatment of the etched surface prior to the p-GaN regrowth was presented as a remedy to this issue. A novel edge termination scheme was also introduced by passivating the p-GaN around the anode region by hydrogen plasma<sup>265</sup> to obtain significant gains in the BV [Fig. 47(b)].

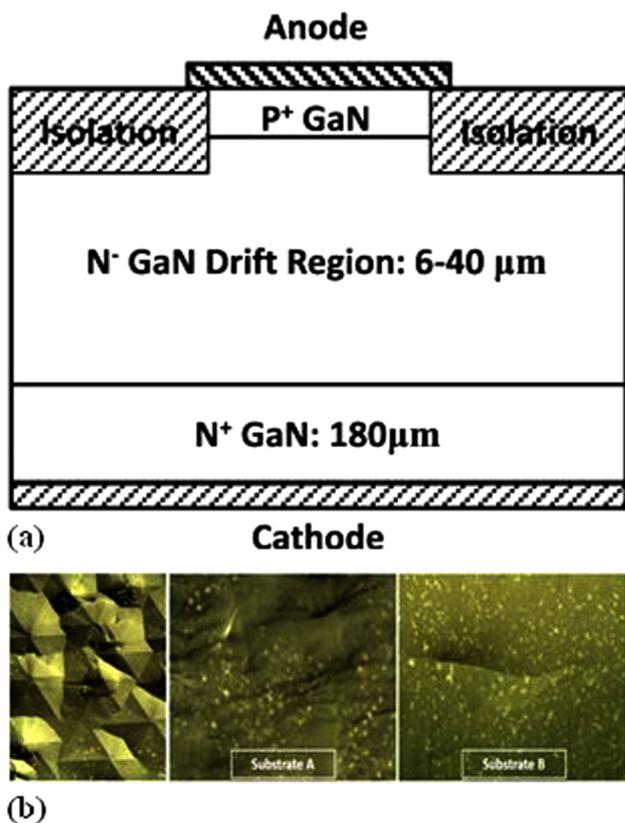
Besides these developments, several other groups demonstrated important advances in the growth, termination, and improvements to the ON-state electrical performance. University of Notre Dame and Sandia National Laboratory demonstrated the use of nitrogen implantation to form edge termination for p-i-n diodes<sup>268,270</sup> [Fig. 48(b)]. Devices with ultra-low  $R_{ON,sp}$  of  $0.15 \text{ m}\Omega \text{ cm}^2$  and BV of  $1.68 \text{ kV}$  corresponding to Baliga's figure of merit of  $18.8 \text{ GW/cm}^2$  were obtained. Another type of termination is a bevel edge termination, which was studied extensively for GaN p-i-n diodes by researchers from Kyoto University.<sup>228</sup> The study set forth important design instructions, particularly the angle of the bevel, the thickness, the doping of the GaN layers, etc.

Bulk GaN substrates are typically around  $350\text{--}400 \mu\text{m}$  thick and serve the purpose of providing a lattice and CTE matched template for epitaxial growth of GaN layers. However, after the growth of the low defective GaN layers, the bulk GaN substrate could be effectively removed and reused. This concept was demonstrated by introducing a thin i-InGaN layer between the bulk GaN substrate

and a p-i-n heterostructure<sup>268</sup> [Fig. 48(a)]. This i-InGaN layer can be photo-electrochemically etched resulting in an epitaxial lift-off from the bulk GaN substrate. The epitaxial layers can then be bonded to a high thermal conductivity material and processed further. The bulk GaN substrate can then be reused many times for growing new epitaxial layers by a similar process. The p-i-n diodes fabricated by using this method demonstrated an excellent  $R_{ON,sp}$  of  $0.2\text{--}0.5 \text{ m}\Omega \text{ cm}^2$  and a BV of  $1300 \text{ V}$  similar to a control device fabricated without epitaxial lift off, thus confirming no degradation in the performance as a result of this special fabrication process.

These results revealed the excellent progress made for GaN p-i-n diodes providing important insights into the material properties like critical electric field, reliability, avalanche capability, etc. Si and SiC devices normally employ junction termination extension structures formed by selective p/n-type doping by ion implantation to achieve reliable devices. Due to the difficulties involved in achieving selective doping in GaN, several other methods based on  $\text{N}_2/\text{H}_2$  plasma treatment, field plate deposition, and ion implantation schemes to form resistive regions around the anode were employed to obtain high BV devices.

*b. Schottky barrier diodes (SBDs).* Unlike p-i-n diodes, SBDs are unipolar devices, which find applications in power converters by virtue of their low turn-on voltage as well as absence of reverse recovery charge. Due to the absence of a p-type layer, and thus conductivity modulation, SBDs normally have a higher  $R_{ON}$  compared to p-i-n diodes.<sup>271</sup> The reverse leakage current is also higher as the reverse voltage is held by the depletion at the metal-semiconductor Schottky barrier. Vertical GaN SBDs on sapphire substrates were first reported in 2000 with a BV as high as  $550 \text{ V}$ .<sup>272,273</sup>



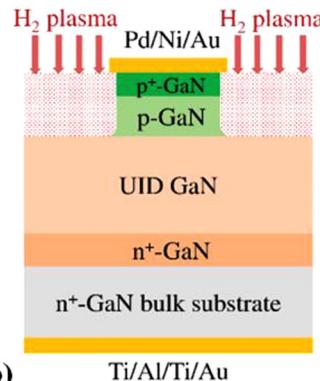
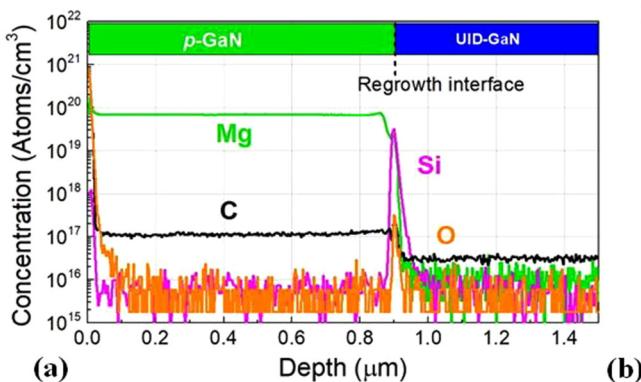
**FIG. 46.** (a) Schematic of a vertical GaN p-n diode with ion-implanted edge termination. Reproduced with permission from Kizilyalli *et al.*, IEEE Trans. Electron Devices **62**(2), 414–422 (2015). Copyright 2014 IEEE.<sup>246</sup> (b) Nomarski image of surface morphology observed on devices grown on GaN substrates. The image on the left demonstrates hillocks formed on the GaN surface in growth on low miscut angle substrates. Devices fabricated using substrate B will consistently have lower reverse leakage currents compared to those on substrate A. Reproduced with permission from Kizilyalli *et al.*, Microelectron. Reliab. **55**, 1654–1661 (2015). Copyright 2015 Elsevier.

In 2001, vertical GaN SBDs on bulk GaN substrate were demonstrated by incorporating a Mg<sup>+</sup>-ion-implanted p-guard rings at the edge of the Schottky contacts. The device presented a  $R_{ON,sp}$  of 3.01 mΩ cm<sup>2</sup> and a BV of 700 V. The first high-voltage SBDs on bulk GaN substrates, presenting BV > 1 kV, were only demonstrated in 2010 by Sumitomo Electric Industries.<sup>274</sup> The growth was optimized leading to an excellent electron mobility of 930 cm<sup>2</sup>/Vs in the undoped GaN layer resulting in an ultra-low  $R_{ON,sp}$  of 0.71 mΩ cm<sup>2</sup>. A field plate termination was employed to obtain an excellent BV of 1100 V using just a 5 μm-thick undoped GaN as the voltage blocking layer, leading to a BFOM of 1.7 GW/cm<sup>2</sup> [Fig. 49(a)]. Large-area SBDs with 1.1 × 1.1 mm<sup>2</sup> Schottky electrode area provided a forward current of 6 A at 1.46 V and a  $R_{ON,sp}$  of 0.84 mΩ cm<sup>2</sup> while still exhibiting a high BV of 600 V. This revealed the potential for scaling up these devices for commercial applications. The switching characteristics of these large-area

diodes were compared against Si fast recovery diodes (FRDs) and SiC SBDs, which revealed the smallest reverse recovery time, reverse recovery charge, and losses for GaN SBDs<sup>275</sup> [Fig. 49(b)]. Their study also confirmed stable forward and reverse aging characteristics for 1000 h. Further advances in the material quality of the bulk GaN substrates and optimizations in the MOCVD growth of GaN epitaxial layers led to the improvement in the electrical characteristics of SBDs, with forward currents of 50 A at 2.05 V while sustaining a high enough BV of 790 V, as reported by Toyoda Gosei.<sup>276</sup> The 3 × 3 mm<sup>2</sup> SBDs included a mesa termination with a field plate to improve the BV, while an excellent electron mobility of 1200 cm<sup>2</sup>/Vs for the undoped GaN layer provided a low differential ON-resistance of 25–29 mΩ.

From 2015 to 2020, significant progress was made in improving the quality of the epitaxial GaN layers and termination methods for SBDs. Cao *et al.* from HRL laboratories demonstrated an SBD with a graded AlGaN cap layer on top of the voltage blocking drift layer (i-GaN)<sup>277</sup> as shown in Fig. 50.

This reduced the reverse leakage current by three orders of magnitude while the polarization field in the graded AlGaN effectively shortened the depletion width leading to the formation of a tunneling current at relatively lower bias, thus providing a low turn-on voltage to 0.67 V. These AlGaN capped SBDs with a Schottky contact area of 0.8 × 0.8 mm<sup>2</sup> improved the BV by more than twofold, to 700 V, as compared to a control SBD with no AlGaN cap layer. The effect of C incorporation during the MOCVD growth was investigated on both the forward as well as the reverse characteristics of SBDs.<sup>278</sup> By varying the growth pressure and V/III ratio, different C concentrations from  $\leq 3 \times 10^{15}$  to  $3 \times 10^{19}/\text{cm}^3$  could be obtained. Their study revealed that lower C incorporation is better for both forward and reverse performance, resulting in SBDs with small turn-on voltage of 0.77 V and high BV of 800 V for a large Schottky contact area ( $0.8 \times 0.8 \text{ mm}^2$ ) devices. Professor Amano's group at Nagoya University also studied the effect of C impurity accumulation on the leakage current of GaN SBDs.<sup>279</sup> In their study, initial failure of SBDs at low voltages were ascribed to leakage current path through polygonal pits created by C impurity accumulation during the growth process. Their group also perfected the method of achieving low impurity levels in m-plane GaN, approaching c-plane values by using a quartz-free flow channel.<sup>280</sup> In 2019, they reported on the effect of drift layer thickness on BV, along with the demonstration of vertical GaN SBD with the highest reported BV of 2.4 kV for a drift layer thickness of 30 μm.<sup>281</sup> A reduction in the effective donor concentration with increasing the thickness of the drift layer was observed by secondary-ion mass spectrometry (SIMS) and is believed to have a positive effect on achieving such a high BV. In a recent publication, their group presented their results on SBDs with a drift layer compensated for the unintentional n-type doping by introducing Mg dopants during the growth.<sup>282</sup> The resulting SBDs provided more than 3×-higher BV as compared to a non-compensated SBD, but the ON-state current and  $R_{ON,sp}$  suffered as a result of the high resistivity of the drift layer. Arizona State University investigated ways to balance the interplay between  $R_{ON,sp}$  and BV with the introduction of double drift layers (DDL) for SBDs.<sup>283</sup> Basically, the SBDs consisted of an unintentionally doped (UID) drift layer on the top and a slightly doped drift layer



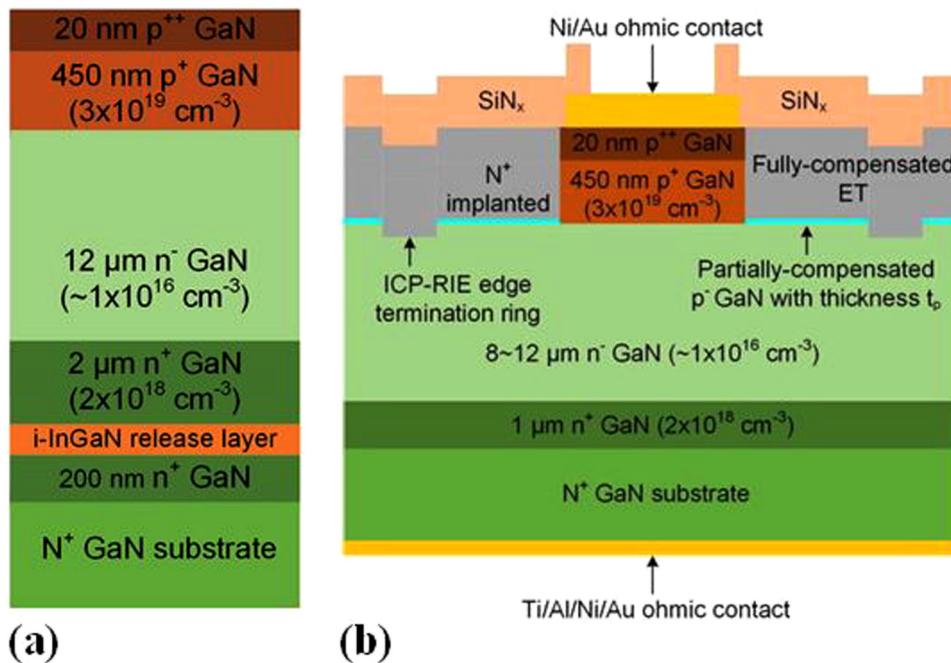
**FIG. 47.** (a) SIMS profile of the regrown p-n junction showing high levels of Si and O atoms at the regrowth interface. Reproduced with permission from Fu *et al.*, *Appl. Phys. Lett.* **113**, 233502 (2018). Copyright 2018 AIP Publishing LLC.<sup>254</sup> (b) Schematic cross section of GaN-on-GaN p-n diodes with hydrogen plasma based edge termination. Reproduced with permission from Fu *et al.*, *IEEE Electron Device Lett.* **39**(7), 1018–1021 (2018). Copyright 2018 IEEE.<sup>265</sup>

at the bottom. The UID drift layer at the top could suppress the peak electric field at the Schottky metal–UID interface and thus improve the BV.

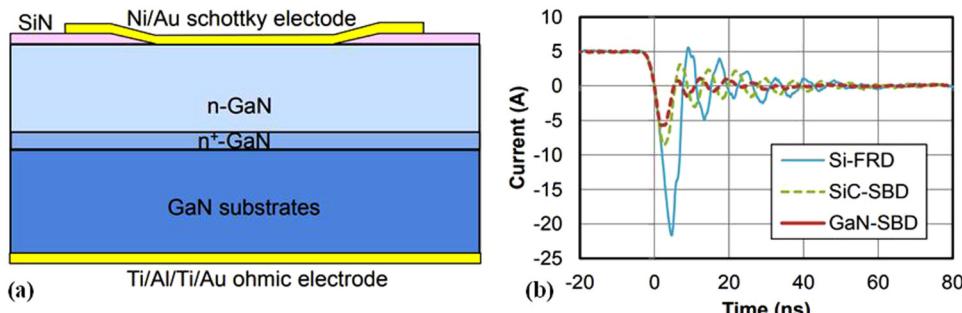
Several implantation-based termination methods were demonstrated in the recent years. Han *et al.* demonstrated a planar nitridation-based termination by subjecting the area around the Schottky contact to an N<sub>2</sub> plasma from a plasma-enhanced chemical vapor deposition (PECVD) system.<sup>284</sup> From ultraviolet photo-electron spectroscopy, it was inferred that the Fermi level at the GaN surface, which underwent the N<sub>2</sub> plasma treatment, went down by 0.68 eV possibly by the passivation of the Ga dangling bonds and, thus, an enlarged energy barrier height and/or effective barrier thickness is presented at the junction edge. This suppressed the thermionic field emission (TFE)/tunneling at this region, and the leakage current reduced as a result. The SBDs with this

termination scheme presented 4 orders of magnitude lower leakage current as compared to a control SBD with no termination and improved the BV from 335 to 995 V. These devices also provided excellent switching behavior with current collapse-free operation and zero reverse recovery characteristics.<sup>285</sup> Han *et al.* also demonstrated fluorine implanted edge termination schemes for GaN SBDs based on the principle that the implanted fluorine ions act as fixed negative ions in GaN<sup>286</sup> [Fig. 51(a)]. This results in spreading of the electric field and prevents the localized peaking at the Schottky contact edge, thus improving the BV as shown in Fig. 51(b). The implantation was done at energy levels of 30, 60, and 100 keV followed by post-implantation annealing at 450 °C in N<sub>2</sub> ambient for 10 min. The BV was boosted from 260 V for the unterminated SBD to 800 V. Further improvement in the BV to 1020 V was achieved by capping the drift layer with a thin 5 nm

19 January 2025 21:33:19



**FIG. 48.** (a) Schematic of the heterostructure used for the epitaxial lift-off devices clearly showing the i-InGaN release layer. Reproduced with permission from Wang *et al.*, *IEEE Electron Device Lett.* **39**(11), 1716–1719 (2018). Copyright 2018 IEEE.<sup>268</sup> (b) Schematic cross section of GaN-on-GaN p-n diodes with nitrogen implanted edge termination. Reproduced with permission from Wang *et al.*, *Appl. Phys. Lett.* **113**, 023502 (2018). Copyright 2018 AIP Publishing LLC.<sup>269</sup>



**FIG. 49.** (a) Schematic cross section of the vertical GaN SBD. (b) Reverse recovery characteristics of GaN SBD, SiC SBD, and Si FRD at  $I_F$  of 5 A, a reverse voltage of 380 V, and  $dI/dt = 3.4 \text{ kA}/\mu\text{s}$ . Reproduced with permission from Ueno *et al.*, 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD) (IEEE, 2014), pp. 309–312. Copyright 2014 IEEE.

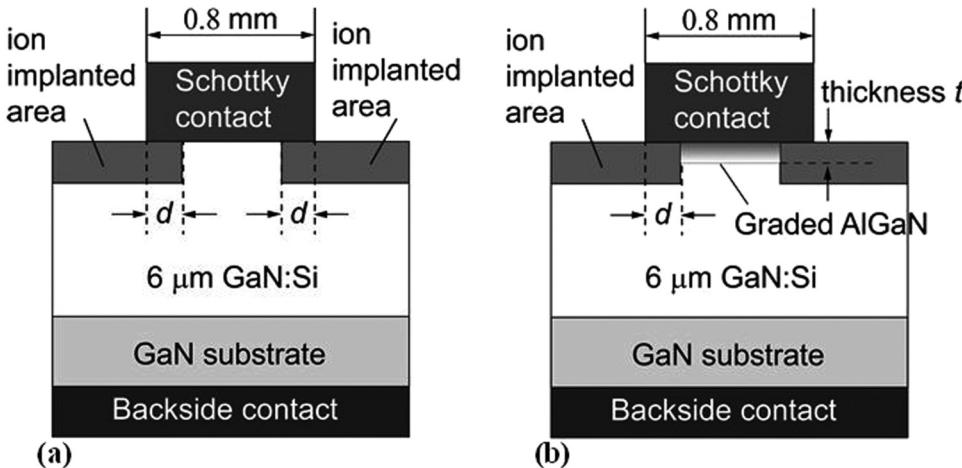
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layer of graded AlGaN, similar to that reported by Cao *et al.* Wang *et al.* demonstrated an identical edge termination scheme with boron implantation.<sup>287</sup> Similar to the fluorine implanted device described before, the boron implanted SBD provided 5 orders of magnitude improvement in the leakage current and improved the BV from 189 V for the unterminated SBD to 585 V.

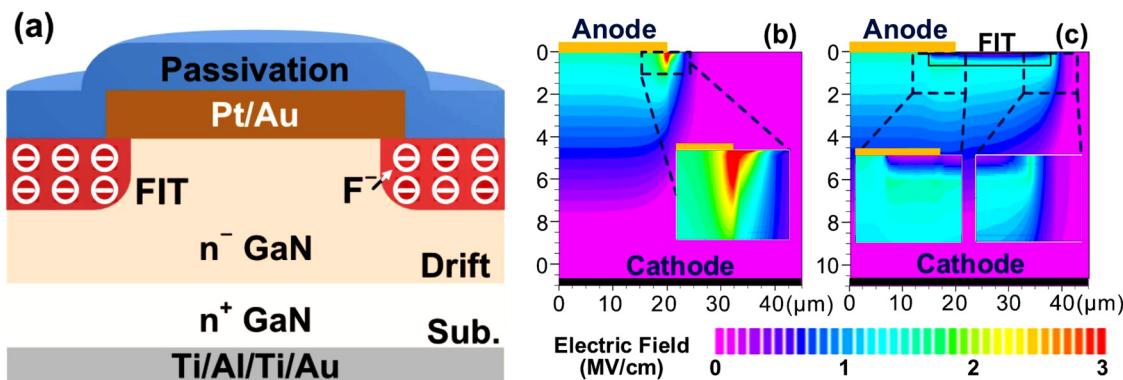
Junction barrier Schottky (JBS) diodes are another type of device that combines low turn-on voltage from the Schottky contacts and low leakage current provided by p-i-n diodes. This is achieved by having alternate undoped and p-type regions below the anode contact, which can be easily formed for Si and SiC by ion implantation methods. Since ion implantation of dopants to GaN is very difficult, other methods to achieve JBS structures were pursued. Cornell University created a trench JBS diode by selectively etching away portions of p-GaN layer form a p-i-n diode followed by Schottky contact formation,<sup>288</sup> as presented in Fig. 52(a). The reduced surface field (RESURF) effect at the Schottky surface as a result of the adjoining p-GaN layers were elaborately studied using TCAD [Fig. 52(b)]. Hayashida *et al.* from Mitsubishi Electric Corporation demonstrated a merged p-i-n Schottky diode<sup>290</sup> based on a trench JBS diode achieving a BV of 2 kV along with surge current capability. However, the leakage current was as high as  $10^{-3} \text{ A/cm}^2$  at  $\sim 750 \text{ V}$  and reached  $10 \text{ A/cm}^2$  at 2000 V, which needs to be further improved. Ion implantation methods have also

been tried to achieve JBS structures in GaN. First reported in 2016 by Koehler *et al.*,<sup>291</sup> the p-doped regions were formed by Mg ion implantation followed by symmetrical multi-cycle rapid thermal annealing (MRTA) for activation. The JBS action was confirmed from reverse bias measurements, which presented much improved leakage current and BV as compared to a normal SBD. Shortly after, Zhang *et al.* demonstrated vertical GaN JBS diodes<sup>289</sup> by (a) Mg implantation into n-GaN to form p-wells and (b) Si implantation into p-GaN to form n-wells (Fig. 53). The implantation and the activation scheme was similar to that used by Koehler *et al.*  $R_{ON,sp}$  values of 1.5–2.5 and 7–9  $\text{m}\Omega \text{ cm}^2$  were observed for the Mg implanted and Si implanted JBS diodes. Both sets of devices provided 100×-reduction in reverse leakage current at high reverse bias and presented a BV of 500–600 V.

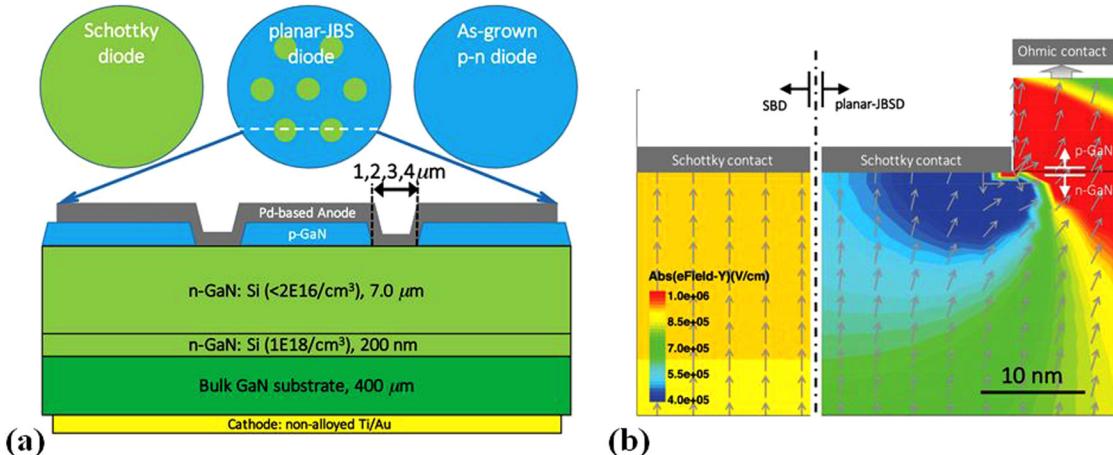
Trench metal barrier Schottky (TMBS) diodes first demonstrated in GaN by Zhang *et al.*<sup>292</sup> represents a device topology that can provide a better control of the reverse leakage current in an SBD. A TMBS diode consists of a trench metal-insulator-semiconductor (MIS) structure as shown in Fig. 54(a). The MIS structure does not contribute to the forward conduction phase, but in the reverse bias condition, the two adjacent MIS structures deplete the semiconductor region between them, thus reducing the leakage current and improving the BV. However, since the Schottky contact is formed only in a portion of the anode, the  $R_{ON,sp}$  is higher than



**FIG. 50.** (a) Schematic cross section of the control vertical GaN SBD and (b) the SBD with the graded AlGaN cap layer. Reproduced with permission from Cao *et al.*, Appl. Phys. Lett. **108**, 112101 (2016). Copyright 2016 AIP Publishing LLC.

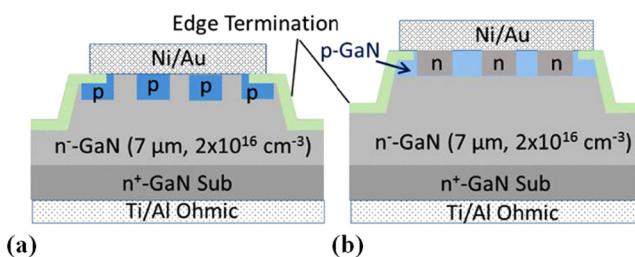


**FIG. 51.** (a) Schematic cross section of the control vertical GaN SBD with fluorine implanted termination and (b) and (c) show simulated electric field distribution in the unterminated-SBD and FIT-SBD at  $-600\text{ V}$ , respectively. Reproduced with permission from Han *et al.*, IEEE Electron Device Lett. **40**(7), 1040–1043 (2019). Copyright 2019 IEEE.<sup>286</sup>



19 January 2025 21:33:19

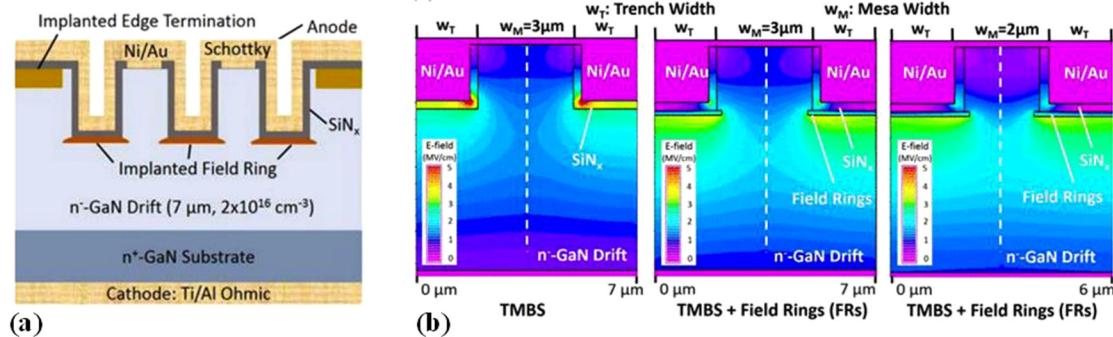
**FIG. 52.** (a) Schematic device top view and cross section of the fabricated trench JBS diode and (b) show simulated electric field distribution at  $-200\text{ V}$  clearly showing the reduction in electric field due to RESURF action from the adjacent p-GaN layer. Reproduced with permission from Li *et al.*, IEEE Trans. Electron Devices **64**(4), 1635–1641 (2017). Copyright 2017 IEEE.<sup>288</sup>



**FIG. 53.** Schematic cross section of a JBS diode by (a) Mg ion implantation in n-GaN and (b) Si ion implantation in p-GaN. Reproduced with permission from Zhang *et al.*, IEEE Electron Device Lett. **38**(8), 1097–1100 (2017). Copyright 2017 IEEE.

in a conventional SBD with Schottky contact in the entire anode area. The leakage current can be controlled by optimizing the trench depth and the TMBS pillar width [Fig. 54(b)]. But too deep a trench will also result in premature breakdown of the  $\text{SiN}_x$  dielectric layer due to electric field peaking at the trench bottom corner. To address this issue, argon-implanted field rings were employed to protect the base of the TMBS anode. The TMBS diode improved the leakage current by  $10^4$ -fold and improved the BV from 400 to 700 V.

Thus, high-performance vertical SBDs with low  $R_{\text{ON},\text{sp}}$  and high BV have been demonstrated in bulk GaN and sapphire substrates by improving the material quality of the GaN epitaxial layers as well as by employing various leakage current mitigation and edge termination schemes. Current collapse-free operation



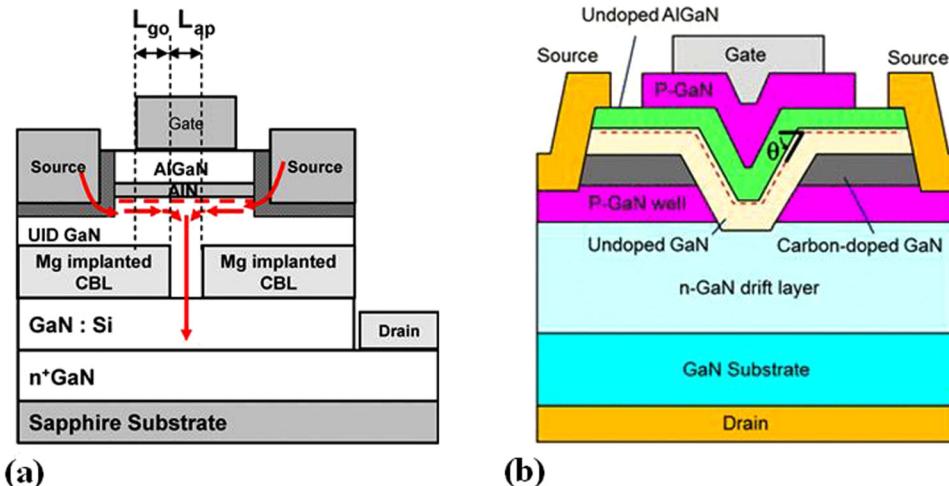
**FIG. 54.** (a) Schematic cross section of a TMBS diode and (b) TCAD simulation of electric field at a reverse bias of  $-1000\text{ V}$  displaying (i) how with the implementation of a field ring at the base of the trench, the electric field peak can be reduced and (ii) how the leakage current can be reduced by making the TMBS pillar narrow from 3 to  $2\mu\text{m}$ . Copyright 2016 IEEE. Reproduced with permission from Zhang *et al.*, 2016 *IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2016), pp. 10.2.1–10.2.4. Copyright 2016.

with zero reverse recovery characteristics could be achieved, thus making GaN SBDs an ideal candidate for low loss rectification purposes.

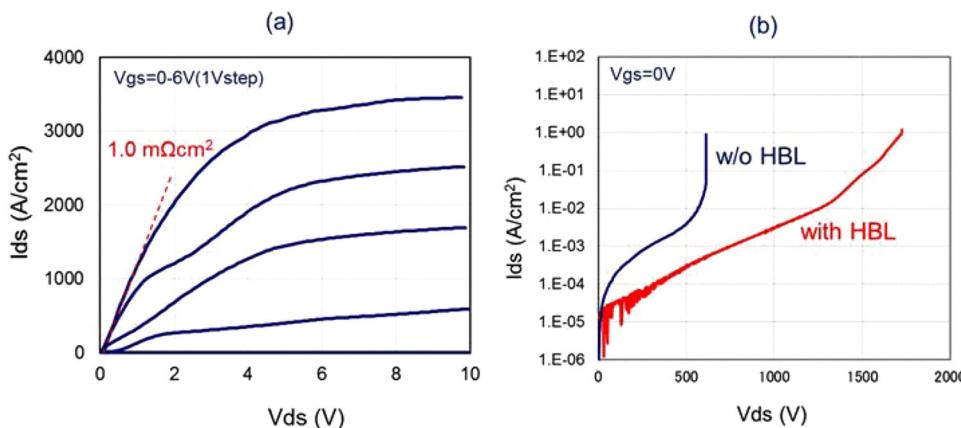
*c. GaN current aperture vertical electron transistors (CAVETs).* The first GaN-based CAVET structure for high-voltage applications were proposed by Ben-Yaacov *et al.*<sup>295</sup> The CAVET structure is similar to double-diffused MOS (DDMOS) structure and comprises of an AlGaN/GaN heterostructure at the top, current blocking layers (CBLs), and a n-type doped GaN layer at the bottom as shown in Fig. 55(a). The source terminals form ohmic contact to the 2DEG and the gate forms Schottky contact to AlGaN. The CBL implemented using Mg ion implantation restricts the flow of current to a small aperture region, which sits just below the gate. By applying a gate bias, the 2DEG below the gate can be switched ON/OFF, thus resulting in a transistor behavior. The main foreseen advantage is that under voltage blocking condition, the high-field region would sit under the gate in the bulk of the device, unlike a

lateral HEMT, and thus may support large BV as surface related breakdown was eliminated. However, CAVETs are in general normally ON devices, as they rely on an AlGaN/GaN channel, which is modulated by the gate. Chowdhury *et al.*<sup>293</sup> demonstrated the first E-mode CAVET with a threshold voltage of  $0.6\text{ V}$  achieved by  $\text{CF}_4$  treatment in the gate region prior to gate metallization. Since the AlGaN/GaN layers are regrown by MOCVD after the formation of CBL, the device threshold voltage varied considerably due to Mg diffusion to the regrown layers. Chowdhury *et al.*<sup>297</sup> demonstrated a GaN CAVET with MBE regrown AlGaN/GaN layers, which provided a low  $R_{\text{ON},\text{sp}}$  of  $2.2\text{ m}\Omega\text{ cm}^2$  and a BV of  $200\text{--}260\text{ V}$  at a  $V_{\text{GS}}$  of  $-15\text{ V}$ . The  $R_{\text{ON},\text{sp}}$  was reduced to  $0.4\text{ m}\Omega\text{ cm}^2$ <sup>298</sup> by using a buried conductive p-GaN layer as the CBL. Avogy developed on this idea and in 2014 demonstrated a modified version<sup>298</sup> of these CAVET structures with a p-GaN gate layer between the gate electrode and the AlGaN barrier for a normally OFF operation. Their device provided a forward current as high as  $2.3\text{ A}$  and a threshold voltage of  $0.5\text{ V}$ . A high BV of  $1.5\text{ kV}$  was observed at a  $V_{\text{GS}}$  of

19 January 2025 21:33:19



**FIG. 55.** (a) Schematic cross section of a GaN CAVET. Reproduced with permission from Chowdhury *et al.*, IEEE Electron Device Lett. **29**(6), 543–545 (2008). Copyright 2008 IEEE.<sup>293</sup> (b) Schematic cross section of an improved version the GaN CAVET with normally off behavior and  $1.7\text{ kV}$  BV. Reproduced with permission from Shibata *et al.*, 2016 *IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2016), pp. 10.1.1–10.1.4. Copyright 2016 IEEE.



**FIG. 56.** (a) DC output characteristics of the GaN transistor mentioned in Ref. 294. (b) OFF-state comparison with and without the carbon doped GaN layer (HBL). Reproduced with permission from Shibata *et al.*, 2016 IEEE International Electron Devices Meeting (IEDM) (IEEE, 2016), pp. 10.1.1–10.1.4. Copyright 2016 IEEE.

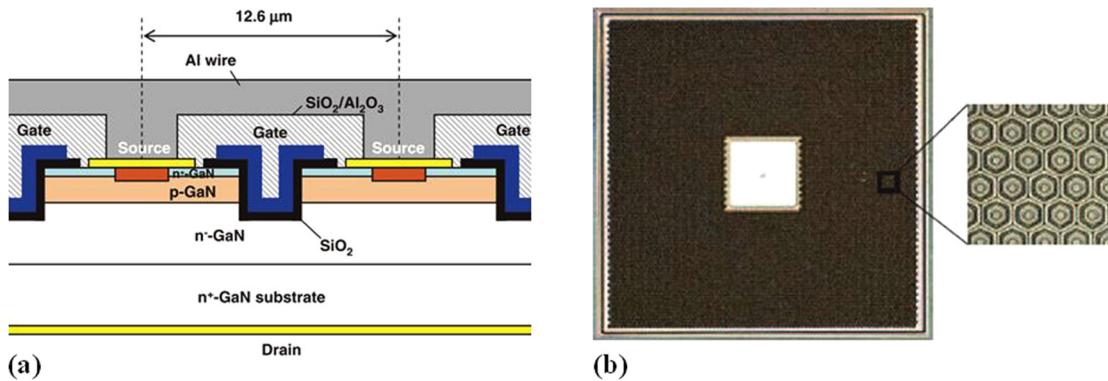
–5 V aided by implanted edge termination structures. Panasonic Corporation<sup>294</sup> demonstrated a similar device by placing a portion of the channel on the sidewall of an etched trench (forming the gate) and a p-GaN gate [Fig. 55(b)]. They were able to achieve a low  $R_{ON,sp}$  of  $1 \text{ m}\Omega\text{cm}^2$  and an excellent BV of  $1.7 \text{ kV}$  (Fig. 56). Ji *et al.*<sup>299</sup> demonstrated a GaN CAVET with a similar gate trench structure but without the p-GaN gate and achieved  $20 \text{ V}$  threshold voltage, and a BV of  $225 \text{ V}$ . A higher BV of  $880 \text{ V}$  was achieved by Ji *et al.*<sup>300</sup> in a subsequent report by improving the gate trench etching quality and by using a gate dielectric, which reduced the gate to drain leakage. However, as a result of using a MIS structure for the gate, the  $V_{GS}$  shifted to –21 from  $20 \text{ V}$  for the previous report.

Some aspects associated with the GaN CAVET need to be addressed to make this transistor viable for commercial use. The main issue stems from the regrowth process, which introduces high source to drain and gate to drain leakage currents in the majority of the reported devices. The ON-state performance is also very sensitive to the doping and dimension of the aperture region formed between the adjacent CBLs, which is difficult to control due to the relatively complicated fabrication process.

*d. Vertical trench gate MOSFETs.* GaN trench MOSFETs were first reported by ROHM Co. Ltd. in 2007.<sup>303</sup> These MOSFETs were fabricated on GaN layers grown by MOCVD on sapphire substrates. Two different gate dielectrics were investigated: electron-cyclotron-resonance (ECR) deposited  $\text{SiO}_2/\text{Si}_x\text{N}_y$  and PECVD  $\text{SiO}_2$ . A reduction in threshold voltage from  $25.5$  to  $5.1 \text{ V}$  was observed by using the ECR deposited dielectric pair. This work also reported a high channel mobility of  $133 \text{ cm}^2/\text{V s}$ . In 2008, the same group demonstrated the first fully vertical MOSFET<sup>304</sup> on bulk GaN substrates with similar performance figures as the previous report. Kodama *et al.* from Toyota Central R&D Labs<sup>305</sup> devised a method of achieving a smooth m-plane trench sidewall by dry etching followed by tetra methyl ammonium hydroxide (TMAH) wet etching. TMAH etches m-plane and c-plane of GaN at a much slower rate than the other facets. Hence, sufficient treatment of the dry etched trench sidewall in heated TMAH results in a smooth surface, which is predominantly m-plane. This is very beneficial for achieving smooth vertical sidewalls, which could

improve the channel mobility of the MOSFETs. Improvements in BV and  $R_{ON,sp}$  of GaN trench MOSFET were reported by the Toyoda Gosei Corporation in 2014<sup>306</sup> [Fig. 57(a)]. They demonstrated a GaN trench MOSFET with a field plate termination achieving a BV of over  $1.6 \text{ kV}$  and  $R_{ON,sp}$  of  $12.1 \text{ m}\Omega\text{cm}^2$ . In 2015,<sup>301</sup> they reported a similar device with  $R_{ON,sp}$  improved to  $1.8 \text{ m}\Omega\text{cm}^2$ , along with a high BV of  $1.2 \text{ kV}$ . This was achieved by tuning the doping and thickness of the p-GaN channel region and the i-GaN layer. The Mg doping of the p-GaN channel layer was reduced, which resulted in lower scattering of inversion channel electrons by the dopant atoms, and they also slightly increased the doping of the i-GaN layer. Large-area trench MOSFETs<sup>302</sup> with ON-state current over  $10 \text{ A}$  while still maintaining a high BV of over  $1.2 \text{ kV}$  was also reported by the same group in 2016, which indicates that dislocation densities from bulk GaN substrates do not necessarily become a bottleneck for obtaining both high BV and high ON-state current with large-area devices [Fig. 57(b)]. A hexagonal cell array was employed for achieving a high gate width per unit cell area, leading to an increase in a current density and, thus, a reduction in the  $R_{ON,sp}$ . Very recently,<sup>307</sup> their group also demonstrated a vertical trench MOSFET with a current distribution layer (CDL) below the p-GaN as shown in Fig. 58(a). The CDL consists of a thin slightly n-type doped ( $2 \times 10^{16}/\text{cm}^3$ ) layer, which can better distribute the current from the base of the gate trench. This resulted in  $1.17\times$  higher forward current density, and an absolute value of current of  $100 \text{ A}$  was achieved for large-area MOSFETs using the CDL [Fig. 58(b)]. HRL Laboratories developed a method to avoid plasma etch damage to the p-GaN body contact region by selective area regrowth of n-GaN on top of the p-GaN. They demonstrated a  $0.5 \text{ mm}^2$  large-area trench MOSFET with an  $R_{ON,sp}$  of  $8.5 \text{ m}\Omega\text{cm}^2$ , threshold voltage of  $4.8 \text{ V}$ , and a BV of  $600 \text{ V}$ . A detailed analysis of the dependence of main device parameters on gate dielectric thickness, body layer doping level, and cleaning process was presented recently in Ref. 308.

*e. In situ oxide GaN interlayer-based vertical trench MOSFET (OGFET).* In a traditional vertical trench gate MOSFET with an n-p-i-n heterostructure, the channel region is formed by the n-p-i sidewall of the trench gate structure; on the application of a positive



**FIG. 57.** (a) Schematic cross section of a GaN trench MOSFET. Reproduced with permission from Appl. Phys. Express 8(5), 054101 (2015). Copyright 2015 The Japan Society of Applied Physics. (b) Chip micrograph of a 1.8 mm<sup>2</sup> large area multi-cell trench MOSFET. Reproduced with permission from Oka *et al.*, 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD) (IEEE, 2016), pp. 459–462. Copyright 2016 IEEE.

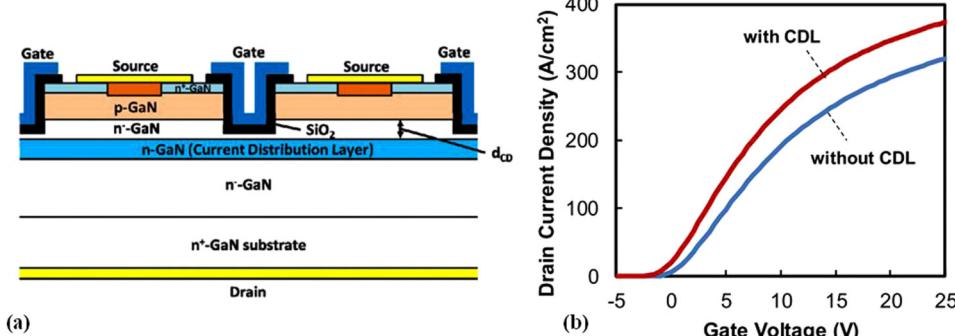
gate bias above the threshold voltage, an inversion sheet charge of electrons is formed in the p-GaN layer adjacent to the gate dielectric. Since the channel is formed by dry etching, the field effect mobility of the inversion channel electrons is degraded by the defects in the sidewall formed during the etching process. In order to alleviate this issue, Professor Mishra's group at UCSB devised a technique<sup>311</sup> whereby a thin undoped GaN layer is regrown in the gate trench region by MOCVD, followed by *in situ* Al<sub>2</sub>O<sub>3</sub> dielectric deposition as shown in Fig. 59(a). The initial reports on these devices presented 60% reduction in  $R_{ON,sp}$  as compared to traditional trench gate MOSFETs. A normally OFF operation with a threshold voltage of 2 V was also achieved along with a BV of 195 V. Subsequent devices<sup>309</sup> on bulk GaN substrates provided a higher BV of 990 V aided by a low-damage gate trench etching process. Ji *et al.* reported large-area (0.2 mm<sup>2</sup>) OGFETs with an output current close to 0.5 A and a BV of 320 V. Further optimizations on the growth, design, and fabrication of these devices resulted in OGFETs presenting a record channel mobility of 185 cm<sup>2</sup>/V s and a low  $R_{ON,sp}$  of 2.2 mΩ cm<sup>2</sup>.<sup>310</sup> The adoption of a novel double field plate design helped achieve a high BV of 1.4 kV for a single device and 0.9 kV for a large-area (0.2 mm<sup>2</sup>) device [Fig. 59(b)]. Variations of the OGFET have been reported by other groups as well. Li *et al.* reported<sup>312,313</sup> on a trench MOSFET similar

to the OGFET but with an MBE regrown channel rather than by MOCVD. The main aim was to improve on the issue of re-passivation of p-GaN during regrowth of the interlayer by MOCVD. They could achieve a record high BV of 600 V among GaN transistors with a MBE regrown channel along with reduced thermal budget.

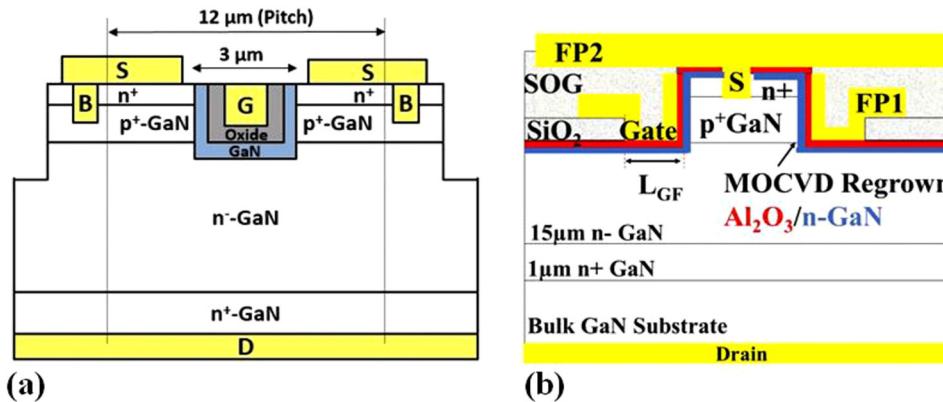
*f. GaN vertical fin power transistors.* In recent years, vertical fin power FETs<sup>315</sup> have been demonstrated, with sub-micrometer fins on bulk GaN substrates. The advantage over classical trench MOSFETs is that they do not require a p-GaN layer to provide a normally OFF operation and blocking under OFF-state. The gate region of these devices consists of dielectric/gate metal on the fin sidewalls, which deplete the charge carriers in the fin due to the work function difference between the gate metal and the GaN, providing a normally OFF operation (Fig. 60).<sup>316</sup>

However, the fin needs to be sufficiently narrow (<500 nm) to be completely depleted, which degrades the current capability of the device. The initial devices presented by Sun *et al.*<sup>315</sup> from MIT revealed a threshold of 1 V,  $R_{ON,sp}$  of 0.36 mΩ cm<sup>2</sup>, and a BV of 800 V with a fin width of 450 nm. The device works by accumulation of electrons rather than by inversion as in the case of trench gate MOSFETs and high-electron mobility of 150 cm<sup>2</sup>/V s was

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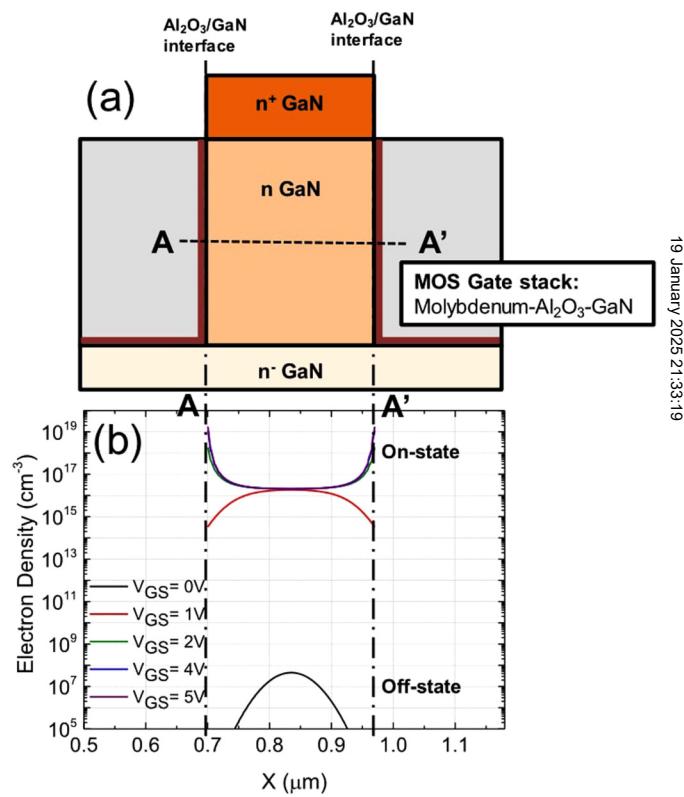
**FIG. 58.** (a) Schematic cross section of a GaN trench MOSFET with CDL. (b) Transfer characteristics measured at  $V_{DS}$  of 0.5 V for the MOSFET with and without the CDL. Reproduced with permission from Oka *et al.*, 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD) (IEEE, 2019), pp. 303–306. Copyright 2019 IEEE.



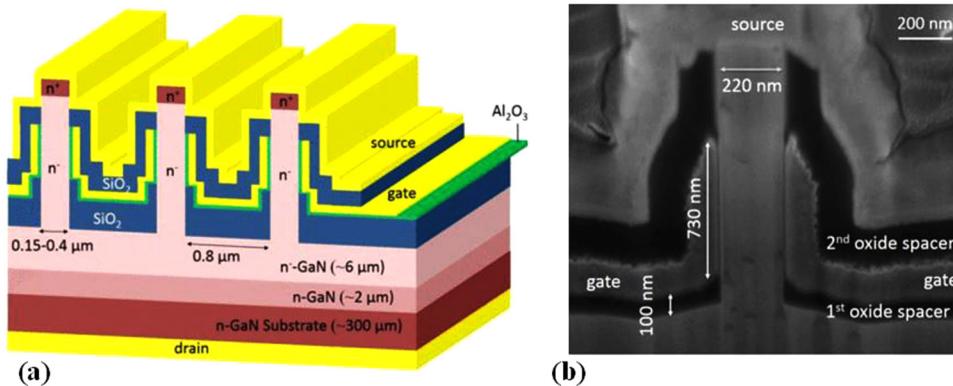
**FIG. 59.** (a) OG-FET cross-sectional schematic. Reproduced with permission from Gupta *et al.*, IEEE Electron Device Lett. **38**(3), 353–355 (2017). Copyright 2017 IEEE. (b) Schematic cross section of the GaN OG-FET with a double field-plate structure. Reproduced with permission from Ji *et al.*, 2017 IEEE International Electron Devices Meeting (IEDM) (IEEE, 2017), pp. 9.4.1–9.4.4. Copyright 2017 IEEE.

obtained in the accumulation layer. Zhang *et al.*<sup>314</sup> further optimized the fin width to obtain a higher BV of 1200 V and a lower  $R_{ON,sp}$  of  $0.2 \text{ m}\Omega \text{ cm}^2$ , normalized to the total device area [Fig. 61(b)] (Fig. 62). Large-area devices with a current capability of 10 A and a BV of 800 V were also demonstrated simultaneously. Switching characteristics<sup>317</sup> of these fin power FETs with a BV of 1200 V and output current capability of 5 A were compared against commercial 0.9–1.2 kV class Si and SiC power transistors, revealing the lowest input capacitance ( $C_{ISS}$ ), output capacitance ( $C_{OSS}$ ), gate charge ( $Q_G$ ), gate to drain charge ( $Q_{GD}$ ), and reverse recovery charge ( $Q_{rr}$ ). These devices exhibited high-frequency (~MHz) switching capabilities and superior switching figure of merits (FOMs) as compared to Si and SiC devices used for comparison. However, these devices break catastrophically, which is possibly due to the absence of p-GaN layers to modulate the electric field peaks. Also, the fabrication and control of the fin width could increase the fabrication complexity compared to other vertical devices. Since the threshold voltage is relatively low  $\sim 1$  V, a well-designed gate driver is required to ensure fail-safe operation. Recently, fin-FET and nanowire (NW)-based structures based on an npn vertical stack have been proposed to obtain a robust normally OFF operation;<sup>318,319</sup> the integration of a p-type layer in a 3D stack (either nanowire- or fin-based) was demonstrated to be a good strategy for achieving a robust normally OFF operation, also under gate-stress experiments<sup>320</sup> (Fig. 63).

*g. Recent development of vertical devices on GaN on Si.* As presented in Secs. II–VI, the ideal solution for obtaining high-quality GaN layers with defect density less than  $10^6/\text{cm}^2$  would be homoepitaxy, i.e., GaN grown on bulk GaN, as there would not be any lattice mismatch between substrate and epitaxial layer. However, even after the demonstration of high-performance diodes and transistors with excellent ON- and OFF-state characteristics, the commercialization of vertical GaN power devices have been hindered by the high cost and the small diameter of these bulk GaN substrates. Currently, these expensive substrates are being used only for specific applications in lasers and LEDs.<sup>239</sup> Hence, in order to take advantage of the material benefits that GaN offers for power device



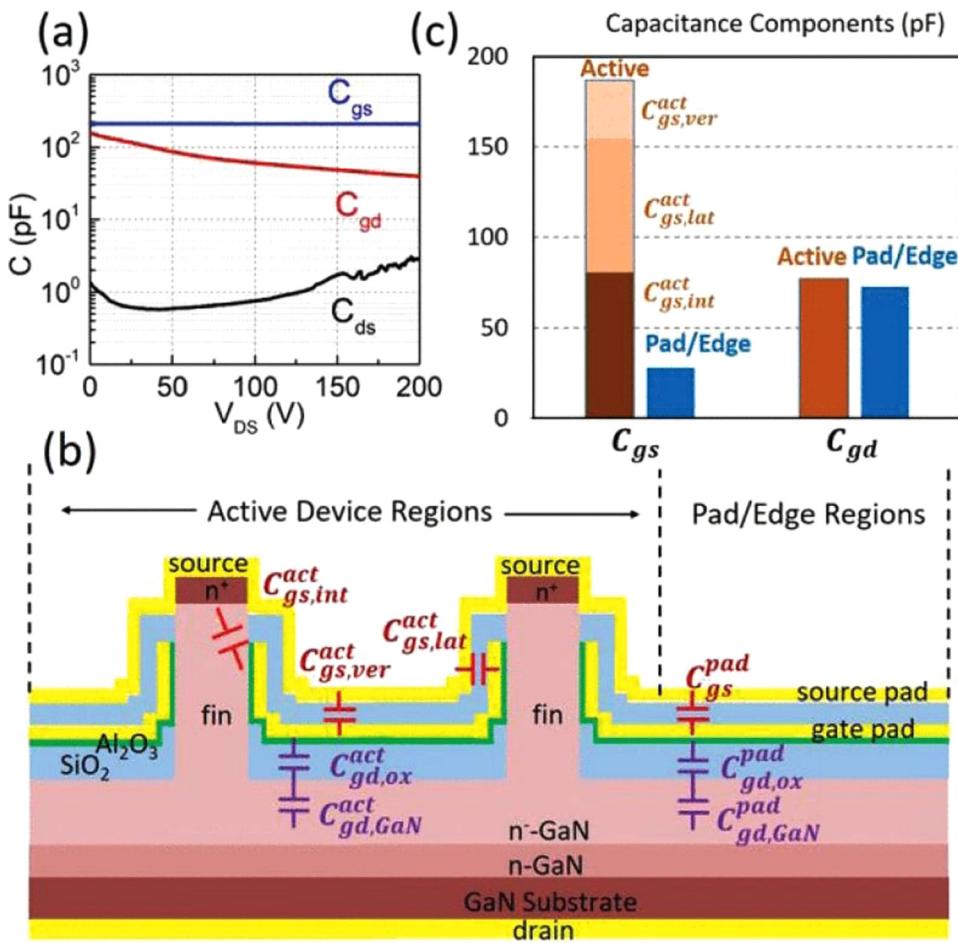
**FIG. 60.** (a) Structure of the GaN VFET. (b) Electron density simulation in the n-GaN channel (along the A–A' cut) under different gate biases: for  $V_{GS} = 0$  V, the device is in OFF condition; hence, the electron density in the channel is low and the maximum is located in the center of the n-GaN region far from the interfaces. At low gate voltage ( $V_{GS} = 1$  V), the e-density is still relatively low ( $\leq 10^{15} \text{ cm}^{-3}$ ). At high gate voltages ( $V_{GS} > 2$  V), the electron density peaks at the  $\text{Al}_2\text{O}_3/\text{GaN}$  interface. Copyright 2017 IEEE. Reproduced with permission from Ruzzarin *et al.*, IEEE Trans. Electron Devices **64**(8), 3126–3131 (2017). Copyright 2019 IEEE.



**FIG. 61.** (a) Schematic of a vertical fin power transistor. (b) Cross-sectional SEM image of the fin area with  $\sim 220$  nm channel width. Reproduced with permission from Zhang *et al.*, 2017 *IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2017), pp. 9.2.1–9.2.4. Copyright 2017 IEEE.

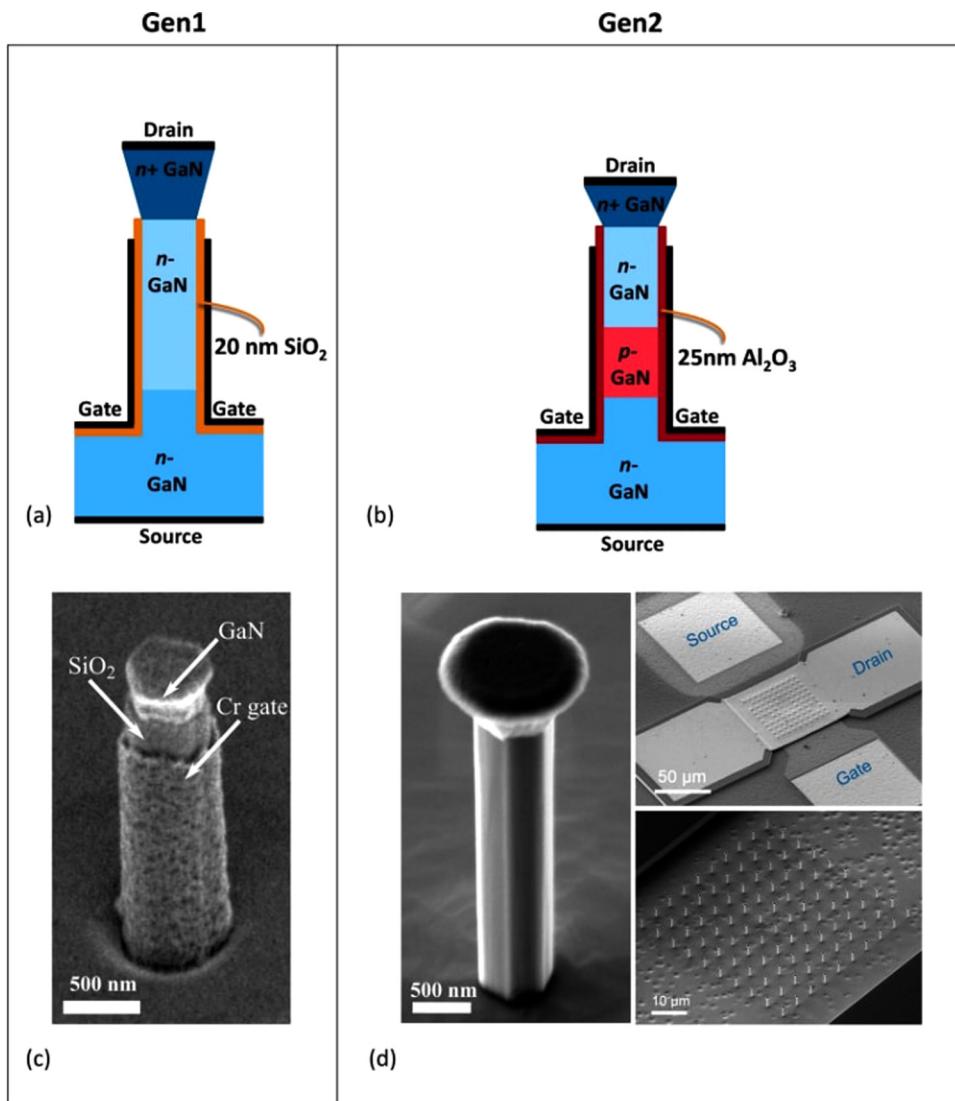
applications, further improvements in wafer size and reduction in cost are highly desirable. A strategy to tackle this issue is by adopting GaN grown on cheaper foreign substrates like Si and sapphire. GaN-on-Si growth has been widely researched and commercialized for the lateral GaN HEMT technology. A similar approach could

be embraced for vertical power devices as well. Furthermore, GaN-on-Si growth could give 10–100 times lower wafer + epitaxy cost<sup>237,322</sup> as compared to bulk GaN. Si substrates also provide better thermal and electrical conductivity as compared to sapphire, in addition to more mature fabrication processes for the backend



**FIG. 62.** (a) Measured device junction capacitances  $C_{ds}$ ,  $C_{gs}$ , and  $C_{gd}$ . (b) Schematic of the various  $C_{gs}$  and  $C_{gd}$  components of the FinFET. (c) Capacitance component break-out of the measured  $C_{gs}$  and  $C_{gd}$ . Reproduced with permission from Zhang *et al.*, IEEE Electron Device Lett. **40**(1), 75–78 (2019). Copyright 2019 IEEE.

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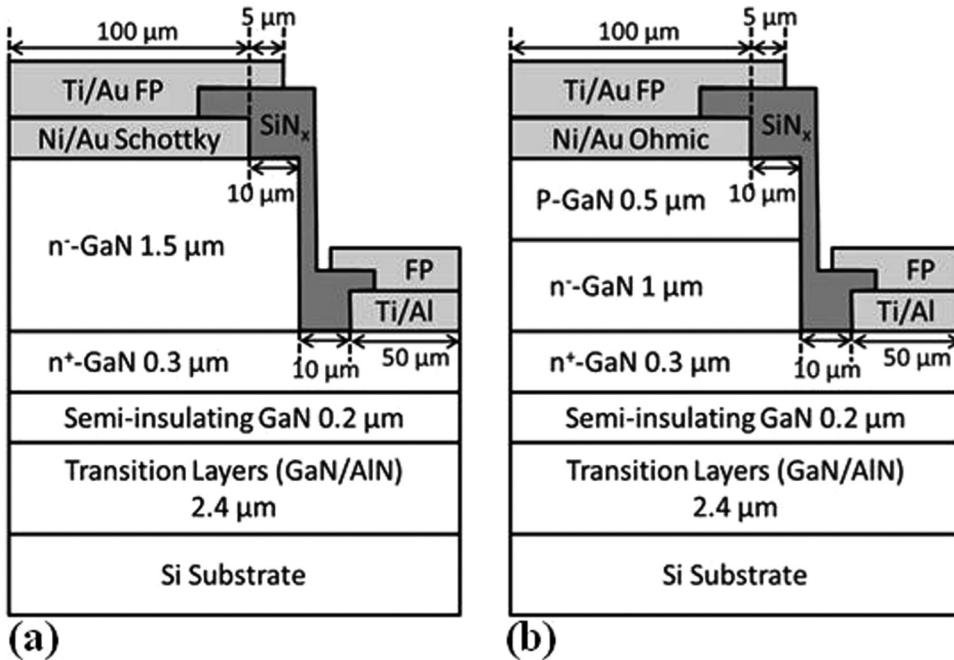
**FIG. 63.** Cross section of a nanowire device processed on a sapphire substrate. (a) The n-channel device (Gen1) consists of a  $2.5\text{ }\mu\text{m}$ -GaN buffer layer, a  $2\text{ }\mu\text{m}$ -GaN channel layer, a  $0.5\text{ }\mu\text{m}$ -GaN top layer, and a  $20\text{ nm}$ - $\text{SiO}_2$  gate dielectric. (b) The p-channel device (Gen2) comprises a  $2.5\text{ }\mu\text{m}$ -GaN buffer layer, a  $0.5\text{ }\mu\text{m}$  p-GaN channel layer,  $0.73\text{ }\mu\text{m}$ -GaN and  $0.5\text{ }\mu\text{m}$ -GaN as the top layer, and  $25\text{ nm}$ - $\text{Al}_2\text{O}_3$  as the gate dielectric. (c) SEM image of a nanowire of the n-channel device (Gen1). (d) SEM images of a nanowire of the p-channel device (Gen2) and bird's-eye view of vertically aligned n-p-n GaN nanowire (NW) arrays with top contacts. Reproduced with permission from Ruzzarin *et al.*, Appl. Phys. Lett. **117**, 203501 (2020). Copyright 2020 AIP Publishing LLC.

19 January 2025 21:33:19

processing. But the main advantage of GaN on Si is that Si substrates are commercially available up to 12-in. diameters, which could drastically reduce the overall cost per unit of the device. The adoption of Si substrates could also allow current CMOS compatible fabs to mass produce GaN-on-Si devices, thus saving the high cost normally required for setting up new technology fabs. Recently, a new class of engineered substrates with poly-AlN has been introduced.<sup>323–326</sup> The main advantage of these substrates is their coefficient of thermal expansion (CTE) matched to GaN and thus enabling the growth of thick, high-quality stress-free GaN with lower defect density as compared to GaN-on-Si substrates.<sup>30,102</sup> Thus, the future for GaN-on-Si vertical devices seems very promising.

GaN-on-Si p-i-n diodes have been demonstrated since 2014. Zhang *et al.* demonstrated the first GaN-on-Si p-i-n and Schottky

diodes<sup>321</sup> with a BV of 300 and 205 V, respectively (Fig. 64). Even with a high defect density of  $10^9/\text{cm}^2$ , a peak electric field of  $2.9\text{ MV/cm}$  could be achieved. The current leakage paths, leakage mechanisms, and methods to improve the leakage current were thoroughly researched and identified in a later work.<sup>322</sup> A device termination scheme based on ion implantation and anode field plate was found to reduce the leakage current by almost two orders of magnitude. For GaN layers grown on Si substrates, the traditional device structure is quasi-vertical, in which both top and bottom layers are accessed through the device top surface. This results in a non-uniform distribution of current from the anode and current crowding at the bottom GaN layer near the cathode terminal. In order to alleviate this issue, Zou *et al.* demonstrated a method of making a fully vertical p-i-n diode<sup>327</sup> by removing the Si substrate below the GaN layers, followed by transfer of GaN

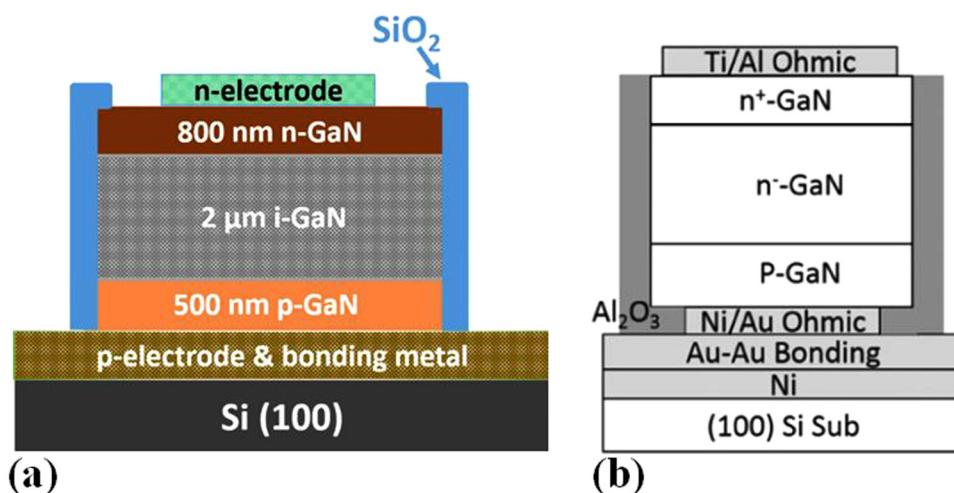


**FIG. 64.** Schematic structure of a GaN-on-Si: (a) Schottky diode and (b) p-i-n diode. Reproduced with permission from Zhang *et al.*, IEEE Electron Device Lett. 35(6), 618–620 (2014). Copyright 2014 IEEE.

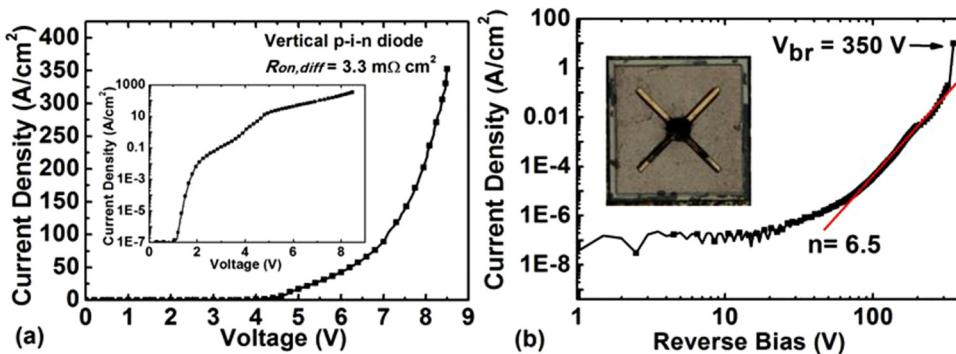
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epilayers to a carrier wafer as shown in Fig. 65(a). The finished p-i-n diode presented an  $R_{ON,sp}$  of  $3.3 \text{ m}\Omega \text{ cm}^2$  and a BV of 350 V [Fig. 66]. Excellent temperature stability up to  $175^\circ\text{C}$  was also observed during ON- and OFF-state measurements. Zhang *et al.* demonstrated a similar method of achieving fully vertical p-i-n diodes<sup>328</sup> but with a better  $R_{ON,sp}$  of  $1 \text{ m}\Omega \text{ cm}^2$  and BV of 500 V [Fig. 65(b)]. A low reverse recovery time of 50 ns comparable to bulk GaN diodes were extracted along with excellent thermal stability of the devices up till  $300^\circ\text{C}$ . Mase *et al.*<sup>329</sup> demonstrated a novel method of achieving a fully vertical GaN-on-Si p-i-n diode by using a conductive n-type Si substrate along with n-type buffer layers [Fig. 67(a)]. An interesting feature of their p-i-n

heterostructure was the use of a  $3.2 \mu\text{m}$  thick strained superlattice (SLS) of n-GaN/n-AlN. A sufficiently thick SLS layer ( $\sim 3 \mu\text{m}$ ) was necessary to control the edge dislocations to an appreciable value of  $\sim 2 \times 10^9/\text{cm}^2$ , which also dictated the lowest doping level possible for the GaN layers grown over the SLS layer. The devices presented an  $R_{ON,sp}$  of  $7.4 \text{ m}\Omega \text{ cm}^2$  and a BV of 288 V. A detailed analysis of current crowding effect in quasi-vertical structures were provided by Zhang *et al.*<sup>223</sup> According to this research, the thickness and the doping of the bottom n-GaN current collecting layer determines the  $R_{ON,sp}$ , and a thick highly doped bottom n-GaN is required to ensure lower levels of current crowding. High-voltage GaN-on-Si p-i-n diodes were demonstrated by Khadar *et al.*<sup>331</sup>



**FIG. 65.** Schematic structure of a completed GaN-on-Si fully-vertical p-i-n diode fabricated by substrate removal and bonding to a carrier wafer by (a) Zou *et al.*, Reproduced with permission from Zou *et al.*, IEEE Electron Device Lett. 37(5), 636–639 (2016). Copyright 2016 IEEE. (b) Similar structure fabricated by Zhang *et al.*, Reproduced with permission from Zhang *et al.*, IEEE Electron Device Lett. 38(2), 248–251 (2017). Copyright 2017 IEEE.



**FIG. 66.** (a) Forward and (b) reverse  $I$ - $V$  characteristics of vertical p-i-n diodes. The inset shows the anode region after destructive breakdown. Reproduced with permission from Zou *et al.*, IEEE Electron Device Lett. 37 (5), 636–639 (2016). Copyright 2016 IEEE.

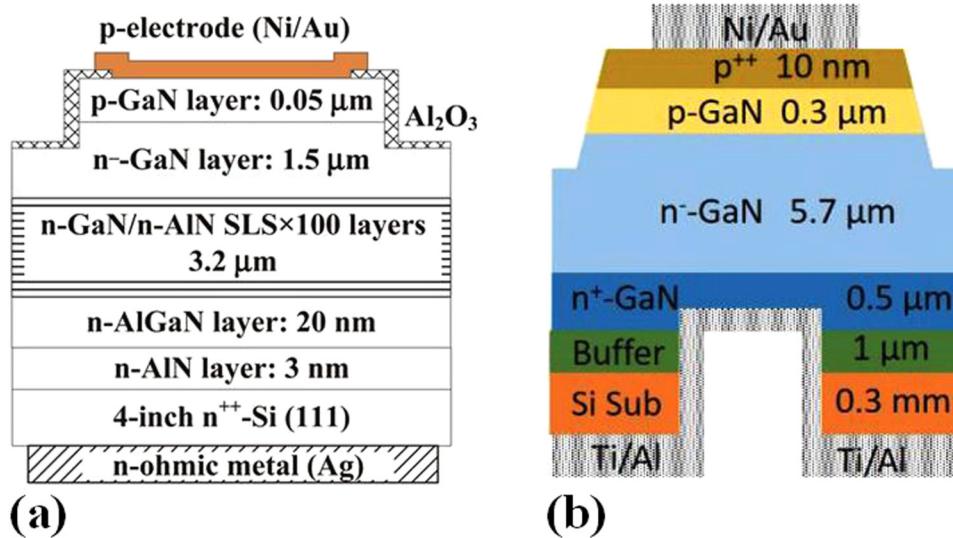
These diodes had a BV of 820 V with just a 4  $\mu\text{m}$  thick drift layer and an ultra-low  $R_{ON,sp}$  of 0.33  $\text{m}\Omega \text{ cm}^2$  resulting in a record value of 2  $\text{GW}/\text{cm}^2$  for the BFOM. The growth of these layers was optimized to obtain i-GaN layers with an excellent electron mobility of 720  $\text{cm}^2/\text{Vs}$  and a low defect density of  $2 \times 10^8/\text{cm}^3$  for GaN grown on Si. Shortly after, Zhang *et al.*<sup>330</sup> demonstrated a new method of achieving a fully vertical operation for GaN-on-Si p-i-n diodes by selective Si removal underneath the active area of the device followed by metallization [Fig. 67(b)]. An  $R_{ON,sp}$  of 0.35  $\text{m}\Omega \text{ cm}^2$  and a BV of 720 V were achieved.

GaN-on-Si vertical power MOSFETs have been also demonstrated, with the first demonstration being from Liu *et al.*<sup>332</sup> [Fig. 68(a)]. A normally OFF operation with a threshold voltage of 6.3 V, which is ideal for power converter applications, along with an ON/OFF ratio of over  $10^8$  was achieved. The device presented a low  $R_{ON,sp}$  of 6.8  $\text{m}\Omega \text{ cm}^2$  and a BV of 645 V, which is comparable to bulk GaN power MOSFETs. The first demonstration of fully vertical MOSFETs was subsequently devised by Khadar *et al.*<sup>333</sup> [Fig. 68(b)]. The method involved a robust fabrication process including selective substrate removal underneath the MOSFET

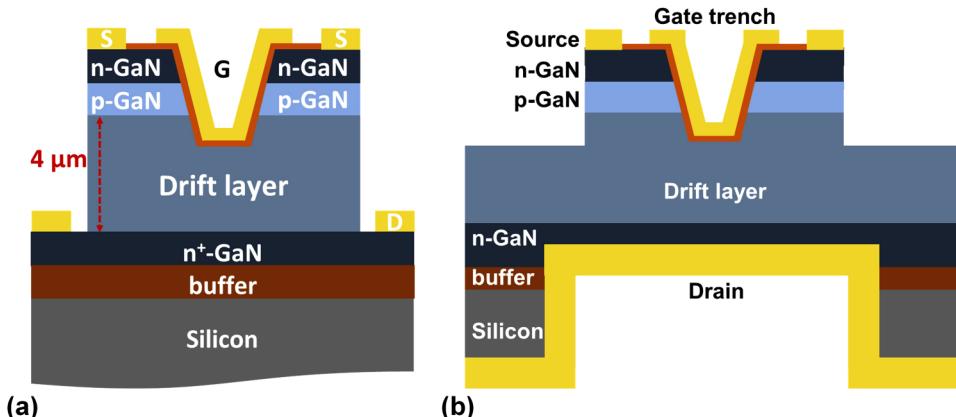
followed by ohmic contact deposition and copper electroplating to provide strength to the thin free standing epitaxial GaN layers. An  $R_{ON,sp}$  of 5  $\text{m}\Omega \text{ cm}^2$  and a BV of 520 V were obtained. These devices exhibited 2.8×-higher current density and 3×-lower  $R_{ON,sp}$  as compared to quasi-vertical control power MOSFETs, due to the absence of current crowding. Also, insights into the impact of hard mask selection for gate trench etching and gate trench alignment to either the m- or a-plane sidewall on the output current density were analyzed (Fig. 69). Devices having gate trench aligned along the m-plane provided 3×-higher output current as opposed to those with gate trench aligned along the a-plane. The use of a metal mask for gate trench etching provided a high inversion channel field-effect mobility of 41  $\text{cm}^2/\text{V s}$  for electrons.

GaN-on-Si technology offers a unique advantage for the possible integration of several different devices on the same chip to realize integrated circuits (IC), which have evident benefits like smaller IC foot print, greatly reduced parasitic capacitance and resistance arising from wire bonding of discrete devices leading to higher efficiency, lower cost, etc. To date, several different integration schemes on GaN-on-Si lateral technology have been

19 January 2025 13:33:19



**FIG. 67.** (a) Schematic cross section of the a fully vertical GaN p-i-n diode on an Si substrate grown by MOCVD. Reproduced with permission from Mase *et al.*, Appl. Phys. Express 9(11), 111005 (2016). Copyright 2015 The Japan Society of Applied Physics. (b) Fully vertical GaN-on-Si p-in diode by selective substrate removal. Reproduced with permission from Zhang *et al.*, IEEE Electron Device Lett. 39(5), 715–718 (2018). Copyright 2018 IEEE.



**FIG. 68.** (a) Schematic cross section of a quasi-vertical GaN power MOSFET on Si substrate. Based on Liu *et al.*, *IEEE Electron Device Lett.* **39**(1), 71–74 (2018). (b) Fully vertical GaN-on-Si power MOSFET by selective substrate removal. Based on Khadar *et al.*, *IEEE Electron Device Lett.* **40**(3), 443–446 (2019).

demonstrated with HEMTs.<sup>334–337</sup> Liu *et al.* demonstrated the first vertical monolithically integrated device<sup>338</sup> in 2018, where a free-wheeling Schottky barrier diode was integrated with the power MOSFET (Fig. 70) to overcome the lossy body diode by using a fast low turn-on voltage SBD. In several topologies of power converters, such as buck/boost converters, voltage-source inverters, and resonant converters, where an inductive load is controlled by switches, a freewheeling diode parallel to the power MOSFET is required to allow a reverse flow of current when the supply current to the load is suddenly interrupted. The integrated SBD was created by dry etching the top n- and p-GaN layers followed by TMAH treatment to smoothen the surface and then Schottky metallization. The integrated MOSFET/diode provided excellent forward and reverse characteristics. In particular, the freewheeling diode presented a low turn-on voltage of 0.76 V, a low  $R_{ON,sp}$  of

$1.6 \text{ m}\Omega \text{ cm}^2$ , an ideality factor of 1.5, and an excellent BV of 254 V achieved without any additional termination mechanisms.

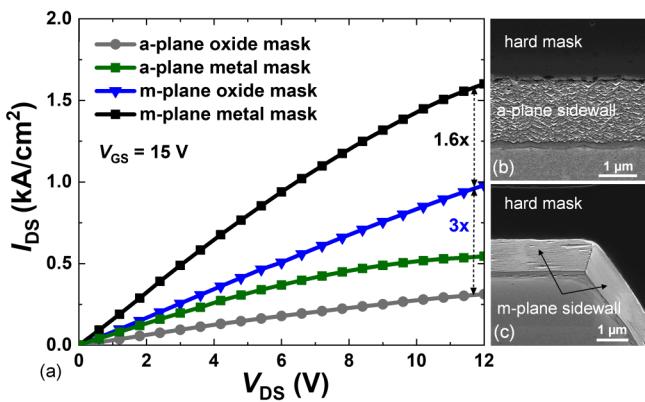
Recently, the optimization of GaN-on-Si semivertical devices has been the subject of pioneering projects in the field, working with Si substrates up to 200 mm in diameter. As an example, we mention recent papers aimed at optimizing the full GaN-on-Si structure, with focus on the Mg doping in the p-body layer,<sup>308</sup> the thickness of the gate insulator,<sup>339</sup> and the dielectric material used at the gate,<sup>340</sup> with the aim of minimizing ON-state resistance and charge trapping, and of obtaining high breakdown voltage.

19 January 2025 21:33:19

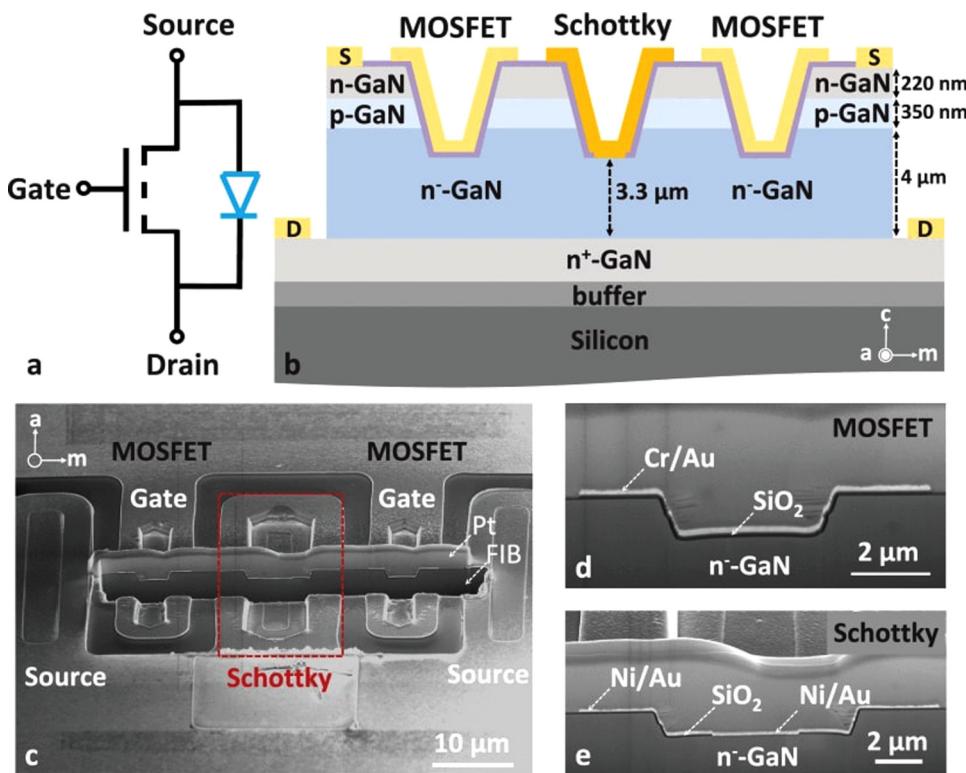
#### D. Open challenges

GaN-based vertical power devices could be used for realizing next-generation power efficient converters provided that pertinent issues related to material quality, device fabrication, and performance can be solved. Compared to Si and SiC, bulk GaN crystal growth process is highly challenging requiring high temperatures  $>2200^\circ\text{C}$  and nitrogen pressure  $>6 \text{ GPa}$  making it impossible to crystallize GaN from the melted compound.<sup>229</sup> Hence, lower pressure and temperature methods like hydride vapor-phase epitaxy (HVPE), sodium flux, and acidic/basic ammonothermal growth method have been utilized to realize bulk GaN substrates. Even so, the defect density in these substrates is around  $10^4\text{--}10^6/\text{cm}^2$ , the effect of which has to be closely scrutinized for use in commercial applications. In general, Si and SiC devices are qualified by the fully Joint Electron Device Engineering Council (JEDEC), which will also have to be done for GaN-based vertical power devices. For GaN HEMTs, it was realized that conventional JEDEC guidelines for Si-based devices are not sufficient and led to the creation of new JEDEC standards JC-70, JEP-180, and JEP-173 for GaN-based devices.<sup>341–343</sup> A similar situation may arise for vertical GaN, and guidelines used for Si, SiC, and lateral GaN may be adopted or refined, following an in-depth discussion by the involved community.

Conventional Si and SiC power devices rely on the selective doping capability by ion implantation or by diffusion to achieve junction termination structures (JTEs), which have been proven to be indispensable for achieving reliable devices with avalanche capability.<sup>344</sup> However, for GaN, doping by ion implantation is still a



**FIG. 69.** (a) Comparison of the  $I_{DS}$ - $V_{DS}$  of the fabricated vertical MOSFETs with gate trench aligned along m- and a-planes using metal and oxide hard masks. SEM images of the trench sidewall aligned along the (b) a-plane and (c) m-plane after TMAH wet treatment. Notice the much smoother m-plane sidewalls compared to the a-plane. Based on Khadar *et al.*, *IEEE Electron Device Lett.* **40**(3), 443–446 (2019).



**FIG. 70.** (a) Equivalent circuit and (b) schematic of integrated vertical MOSFET-Schottky barrier diode (SBD). (c) SEM image of integrated vertical MOSFET-SBD, (d) cross-sectional SEM image of the integrated vertical MOSFET, and (e) of the integrated vertical SBD. Reproduced with permission from Liu et al., IEEE Electron Device Lett. 39(7), 1034–1037 (2018). Copyright 2018 IEEE.

19 January 2025 21:33:19

highly complex process requiring specialized instruments capable of high-temperature<sup>345</sup> ( $>1200\text{ }^{\circ}\text{C}$ ) and high-pressure conditions<sup>346</sup> ( $>1\text{ GPa}$ ). Selective area growth is another option that has been investigated but with little success due to the presence of high concentration ( $>10^{18}/\text{cm}^3$ ) of Si atoms at the regrowth interface.<sup>254,347</sup> Several schemes, like Ar ion implantation and plasma-based treatments described in Secs. II–V, have been adopted for GaN-based vertical devices; however, their suitability for large scale production and long-term reliability is still unclear. There are also concerns related to the low activation efficiency (~1%) of p-GaN grown by MOCVD due to the high bond energy of the stable Mg–H complexes formed during the growth process.<sup>348–350</sup> Even high temperature annealing ( $\sim 750\text{--}850\text{ }^{\circ}\text{C}$ ) activates only a small fraction of the dopant atoms (Mg concentration  $>10^{19}/\text{cm}^3$ ), thus presenting a low hole concentration typically around  $10^{17}/\text{cm}^3$ <sup>351,352</sup> with low hole mobility due to scattering from the dopant atoms present in large concentrations. This is, in particular, not desirable for GaN trench power MOSFETs since the high concentration of dopant atoms in the p-GaN channel region scatters the electrons formed by inversion during normal ON-state operation, thereby degrading the channel mobility<sup>309,332,353</sup> and thus the output current. The low hole mobility of the p-GaN layers also affects the resistance of p-i-n diodes and results in ON-state losses.

Adoption of bulk GaN for commercialization is not only hindered by the high cost and the small size of these substrates but also by the huge initial investment needed for the setting up GaN specific fabs, which could shoot up the average selling price (ASP)

of discrete devices slowing down further the adoption of these devices. Hence, it is vital to make significant strides in the improvement of substrate size as well as the cost of these bulk GaN substrates.

GaN-on-Si could offer an alternative to lower the device costs, but significant progress has to be made on the GaN quality with low defect density and on the thickness of the GaN layers grown on Si substrates, in order to enable larger voltage devices. The advent of CTE matched substrates available in large wafer diameters<sup>354</sup> may further push the development of vertical GaN power devices.

## VII. CHARGE-TRAPPING PROCESSES IN GaN TRANSISTORS

The presence of deep-level traps<sup>355–357</sup> in GaN and its alloys and the effects of the associated charge capture/emission processes can rarely be neglected in GaN transistors under their typical operating conditions in power RF amplifiers and power switching converters. As will be detailed, figures of merit that are key to these applications and that can detrimentally be affected by trapping processes include output power ( $P_{\text{out}}$ ) and power-added efficiency (PAE) in RF amplifiers, switching, and conduction losses in power converters.

Spatial position (Fig. 73) of traps within the device (surface, barrier, buffer, and, if present, gate dielectric), trap parameters<sup>356,357</sup> (energy, capture cross sections, concentration, acceptor- or donor-like behavior), type of involved carriers (electrons or holes), and the associated charging/discharging path (contact

injection/removal, carrier generation, internal redistribution) can all play a role, and their signatures on transistor operation should be known by the technologist for a proper device optimization.

The detrimental consequences of charge-trapping processes include several, widely studied dynamical effects, including the current collapse,<sup>358–362</sup> the increase in the dynamic ON-state resistance (dynamic  $R_{ON}$ ,<sup>363–366</sup>) different forms of threshold voltage ( $V_T$ ) instabilities,<sup>367–373</sup> and the kink effect.<sup>374,375</sup> These phenomena are at the same time the incumbent burden of traps and the way the latter can be probed.

In addition, several trap measurement methods have been devised and extensively applied to GaN structures and transistors, in order to quantitatively characterize traps.

This section is organized as follows. First, the properties of the most common traps in GaN are reviewed to help the reader understand the complexity of the topic. Second, the most important trapping mechanisms affecting GaN transistors are elucidated by crossing the different trap locations with the corresponding possible charging/discharging paths. Then, the resulting trap effects and their relevance for applications are reviewed. Finally, methods that can be adopted for measuring trap parameters are reviewed.

## A. Traps and deep levels in GaN

The properties of GaN as a semiconductor material are determined by the specific periodicity of its crystalline structure. If this periodicity is lost, either due to incorporation of foreign atoms into the crystal or to a non-ideal arrangement of the host atoms during the growth of the material, a defect is locally generated. Defects are referred to as “impurity-related” in the former case, whereas they are defined as “native” in the latter. The presence of these defects locally perturbs the periodic potential of the lattice, therefore introducing allowed energy states within the forbidden bandgap of the material. These states, which can either act as carrier traps or recombination centers, can have a detrimental impact on both the performance and the reliability of GaN-based devices. It is therefore of primary importance to identify the properties and the physical origin that such states have in actual GaN devices. To this aim, a database of traps and deep levels related to the GaN material system has been created by collecting and comparing the data of almost 100 scientific publications (Table VII) (Figs. 71 and 72). The comparison of the 480+ records of traps experimentally detected in GaN by means of various techniques allowed us to correlate energy positioning, signature, and trapping behavior of the levels accredited to the defects most commonly found in GaN. In the following paragraphs, we report the outcome of the study of such defects based on energetic-positioning considerations.

### 1. Native defects

The positions of the trap levels associated with native defects in GaN are reported in Fig. 71. These levels are mainly related to nitrogen interstitial ( $N_i$ ), nitrogen antisites ( $N_{Ga}$ ), nitrogen vacancies ( $V_N$ ), gallium interstitials ( $Ga_i$ ), and gallium vacancies ( $V_{Ga}$ ), to clusters of the former or to unspecified extended defects (mostly dislocations).

**Nitrogen interstitials** have been reported to introduce trap states between  $E_C - 1.2$  eV and  $E_C - 0.76$  eV,<sup>376–383</sup> with average

preferential energy positioning at  $E_C - 1.02$  eV,  $E_C - 0.89$  eV, and  $E_C - 0.79$  eV. The former and the latter levels have also been tentatively associated with an extended defect in Ref. 381. Among nitrogen-related native defects, nitrogen interstitials exhibit the highest activation energy, allowing them to act both as traps or recombination centers.

**Nitrogen antisite** defects are assumed to form a mini-band of levels between  $E_C - 0.66$  eV and  $E_C - 0.5$  eV.<sup>377,381,384–394</sup> None of the aforementioned reports suggest a direct correlation between the levels associated with nitrogen antisite defects and extended defects.

**Nitrogen vacancies** represent the most commonly observed type of native defect in GaN, with more than 40 records in 25 different scientific publications.<sup>377,381,384–394</sup> The associated trap states are preferentially positioned in the  $E_C - 0.27$  eV to  $E_C - 0.089$  eV range, with most of the occurrences belonging to the mini-band at  $E_C - (0.24 \pm 0.003)$  eV identifying the typical level associated with nitrogen vacancies in GaN. The outliers of the aforementioned distribution are represented by the deeper  $E_C - 0.35$  eV,<sup>378</sup>  $E_C - 0.4$  eV,<sup>405</sup>  $E_C - 0.53$  eV,<sup>406</sup> and  $E_C - 0.613$  eV<sup>398</sup> levels, respectively, associated with  $V_N$  complexes, simple nitrogen vacancies, triply ionized nitrogen vacancies, and clusters of vacancies. Other  $V_{Ga}$ -related levels whose physical origin was found to be compatible with an extended defect are located at  $E_C - 0.19$  eV,<sup>387</sup> at  $E_C - 0.23$  eV,<sup>386,387</sup> and at  $E_C - 0.25$  eV.<sup>402</sup> The fact that trap levels with similar Arrhenius signatures, and therefore similar activation energy and cross section, have been associated both with extended and point defects suggests that even if the capture rate of the defect is influenced by the electrostatic repulsion due to the close proximity to other ionized traps or to extended crystal defects, gallium vacancies tend to maintain their characteristic emission properties.

**Gallium interstitials** are reported as the physical origin of traps detected in GaN by only a couple of papers. In Ref. 408, an  $E_C - 0.91$  eV level was associated with  $Ga_i$  complexes located along dislocations. In Ref. 382, a trap located at  $E_C - 0.8$  eV was tentatively ascribed to gallium interstitials located in an unspecified layer of an AlGaN/GaN HEMT.

**Gallium vacancies** are often associated with deep levels responding in the  $E_C - 2.42$  eV to  $E_C - 2.85$  eV range, with most occurrences roughly located at  $E_C - 2.6$  eV.<sup>379,382,383,385,401,403,409–414</sup> Some of these traps have been tentatively associated with oxygen-<sup>379,382</sup> or hydrogen-related<sup>401,411</sup> complexes formed with  $V_{Ga}$ . Also the  $E_C - 1.12$  eV, the  $E_C - 0.64$  eV, and the  $E_C - 0.6$  eV levels found in Ref. 390 have been referred to as  $V_{Ga}-O$ -related defects, whereas other deep levels detected outside the band of reference for this particular type of native defect have been associated to  $V_N-V_{Ga}$  complexes (at  $E_C - 0.24$  eV in Ref. 384) or to simple gallium vacancies (at  $E_C - 0.62$  eV in Ref. 402, at  $E_C - 1.64$  eV in Ref. 394, and at  $E_C - 3.19$  eV in Ref. 405).

**Trap states related to extended defects** have been found to cover a wide and non-continuous portion of the upper part of the GaN bandgap, ranging from  $E_C - 1.118$  eV to  $E_C - 0.24$  eV.<sup>378,381,385,388,390,396,403,407,415,416</sup> Interestingly, the upper group of levels, scattered from  $E_C - 0.27$  eV to  $E_C - 0.17$  eV, covers the same range of activation energies exhibited by  $V_N$ -related defects. Similarly, also a second mini-band of deep levels associated with extended defects, and scattered from

**TABLE VII.** Database of traps detected in GaN- and AlGaN-based devices.

Type of defect or impurity	Physical origin	Reported E <sub>a</sub> (eV)	Detected as	Reference
Native defects				
Nitrogen interstitial	N <sub>I</sub> -related	1–0.76 2.42	E <sub>C</sub> – E <sub>V</sub> +	376–380, 381 <sup>a,b</sup> and 382 383
Nitrogen antisite	N <sub>Ga</sub> -related	0.66–0.5 2.48	E <sub>C</sub> – E <sub>V</sub> +	377, 381, and 384–393 394
Nitrogen vacancy	V <sub>N</sub> -related	0.27–0.089  0.4 3.28 3.18 0.35 0.53 0.613 0.91 0.8	E <sub>C</sub> –  E <sub>C</sub> – E <sub>V</sub> + E <sub>C</sub> – E <sub>V</sub> +	378, 387 <sup>b</sup> , 392, and 395–397 <sup>b</sup> , 386 <sup>b</sup> , 398, and 399, 384 <sup>b</sup> , 400, and 401, 402 <sup>b</sup> , 381, 382, 393, 397, 398, 403–406 and 407 <sup>a</sup>  405 383 394 378 406 398 <sup>b</sup> 408 <sup>b</sup> 382 <sup>a</sup>
Gallium interstitial	Ga <sub>I</sub> complexes	2.85–2.47	E <sub>C</sub> –	401, 403, and 409–413 and 414 <sup>a</sup>
Gallium vacancy	V <sub>Ga</sub> or unspecified complexes (main band)	1.02, 0.83 and 0.89, 0.9, and 0.86  1.12, 0.64, and 0.6 0.62 1.8 0.25 0.24	E <sub>C</sub> –  E <sub>C</sub> – E <sub>V</sub> +	379, 382 <sup>a</sup> , 383, and 385  390 402 394 405 384 <sup>a</sup>
Extended defects	V <sub>Ga</sub> -O V <sub>Ga</sub> -related  V <sub>N</sub> –V <sub>Ga</sub> complexes Many	0.25 0.24 1.118–0.24	E <sub>C</sub> – E <sub>C</sub> – E <sub>C</sub> –	396 <sup>b</sup> , 390 <sup>a,b</sup> , 403 <sup>b</sup> , 388 <sup>b</sup> , 378 <sup>b</sup> , 415 <sup>b</sup> , 381 <sup>a,b</sup> , 416 <sup>b</sup> , 385 <sup>b</sup> , 407 <sup>b</sup>
Impurities-related defects				
Silicon	Si-related	0.59 0.4 0.37	E <sub>C</sub> – E <sub>C</sub> – E <sub>C</sub> –	417 396 396
Magnesium	Shallow acceptor level Mg–H complexes	0.16–0.24 0.08 0.62  0.355 and 0.597 0.44	E <sub>V</sub> + E <sub>V</sub> + E <sub>C</sub> –  E <sub>C</sub> – E <sub>C</sub> –	412 <sup>a</sup> , 418, 401, 414, and 394 419 <sup>a</sup> 412 395 and 420 404
Hydrogen	Mg–V <sub>N</sub> complexes H–V <sub>Ga</sub> complexes C- or H-related	2.62–2.47 0.578 and 0.49	E <sub>C</sub> – E <sub>C</sub> – E <sub>C</sub> –	401 and 411 421 <sup>a</sup> , 422 <sup>a</sup>
Oxygen	O–V <sub>Ga</sub> complexes or dislocations O <sub>N</sub>	1.118, 0.642, and 0.599 0.44 and 0.01	E <sub>C</sub> – E <sub>C</sub> –	390 <sup>b</sup> 423 and 405 <sup>a</sup>
Iron	Fe-related	0.397, 0.5, 0.57, 0.66, 0.68, and 0.72  2.5 0.34 3	E <sub>C</sub> – E <sub>V</sub> +	389, 409, 424, and 425 426 427 426
Carbon	(C <sub>N</sub> ) <sup>0</sup>  (C <sub>N</sub> ) <sup>-1</sup>	3.31–3.22  0.29 0.8–0.95	E <sub>C</sub> – E <sub>V</sub> +	412 <sup>a</sup> , 411, 401, 428, 403, 413, 429, 408 <sup>a</sup> , 430, 385, and 407 <sup>a</sup> 419 and 431 384, 419, and 430 <sup>a</sup> , 385, 431, and 432

19 January 2025 21:33:19

TABLE VII. (Continued.)

Type of defect or impurity	Physical origin	Reported $E_a$ (eV)	Detected as	Reference
$C_I$ C- or H-related		1.35–1.2	$E_C-$	401, 412, 403, and 407 <sup>a</sup>
		0.578, 0.49, and 0.14	$E_C-$	421 <sup>a</sup> and 422 <sup>a</sup>
	$C_{Ga}$	0.4	$E_C-$	384 <sup>a</sup>

<sup>a</sup>Tentative associations performed by the authors of the referenced work.

<sup>b</sup>Traps related to extended defects.

<sup>c</sup>Tentative grouping performed by the authors of this work. Activation energies and related references are reported in the same order.

$E_C - 0.641$  eV to  $E_C - 0.41$  eV, finds a correspondence with the typical range of response of  $N_{Ga}$ -related defects. These considerations suggest that both nitrogen vacancies and nitrogen antisite defects can be found in proximity of other defects, and therefore behave as interacting defects. Interestingly, no defects with activation energies corresponding to the  $V_{Ga}$  band were ascribed to extended defects, possibly suggesting that this type of native defect tends to predominantly behave as a non-interacting point defect or does not form in highly defective device regions.

## 2. Impurity-related defects

Imperfections of the lattice structure may also arise from the inclusion of atomic species that nominally do not belong to the GaN crystal. Such atoms, or atom complexes, are referred to as impurities. These impurities can either be intentionally introduced into the material, as in the case of dopants, be originated as the by-product of the chemical reactions occurring during crystal growth, or derive from unwanted contaminations. Si and Mg represent the main doping species for GaN. Similarly, Fe and C can be intentionally

introduced in order to compensate for the intrinsic n-type conductivity of GaN. Others may act as unwanted contaminants, like residual O and H atoms. A more detailed description of the deep levels introduced by these impurities is provided in the following paragraphs.

Aside from its shallow donor level, which has a typical activation energy ranging from  $E_C - 0.011$  eV to  $E_C - 0.028$  eV for moderately doped GaN layers,<sup>433–435</sup> only few scientific reports attribute to silicon deeper allowed energy levels, respectively located at  $E_C - 0.37$  eV,<sup>396</sup>  $E_C - 0.4$  eV,<sup>396</sup> and  $E_C - 0.59$  eV.<sup>417</sup>

**Magnesium** is employed in GaN devices in order to achieve p-type conductivity. Trap states detected near the valence band edge at  $E_C - 3.2$  eV,<sup>418</sup>  $E_C - 3.22$  eV,<sup>401,412</sup>  $E_C - 3.25$  eV,<sup>414</sup> and  $E_C - 3.28$  eV,<sup>394</sup> even if nominally assigned to other physical origins, can reasonably be ascribed to the shallow level of the dopant, which is known to be typically located from 0.15 to 0.2 eV above the valence band edge.<sup>436,437</sup> A shallower level at  $E_C - 3.36$  eV<sup>419</sup> was tentatively ascribed to Mg–H complexes, and a similar origin was assigned to the  $E_C - 0.62$  eV level in Ref. 412. Additional levels at  $E_C - 0.355$  eV<sup>395</sup> and at  $E_C - 0.597$  eV<sup>420</sup> were

19 January 2025 21:33:19

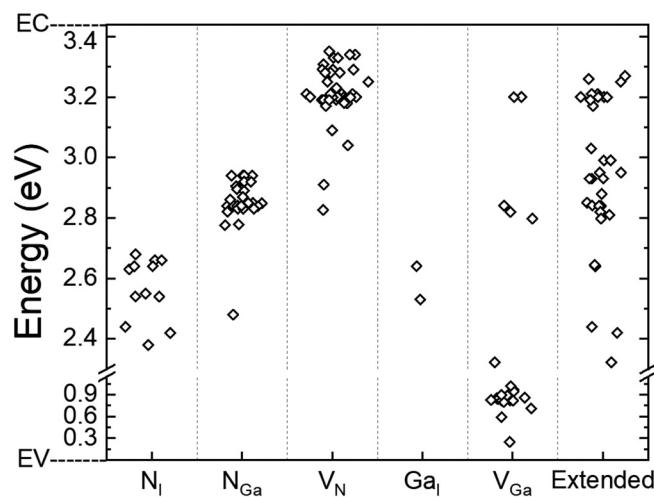


FIG. 71. Energy states detected in GaN and associated with native or extended defects. The reference level, assumed to have energy equal to 0, is related to the top of the valence band. The scatter-like representation highlights the preferential energy assignment of the detected traps with respect to a specific type of defects.

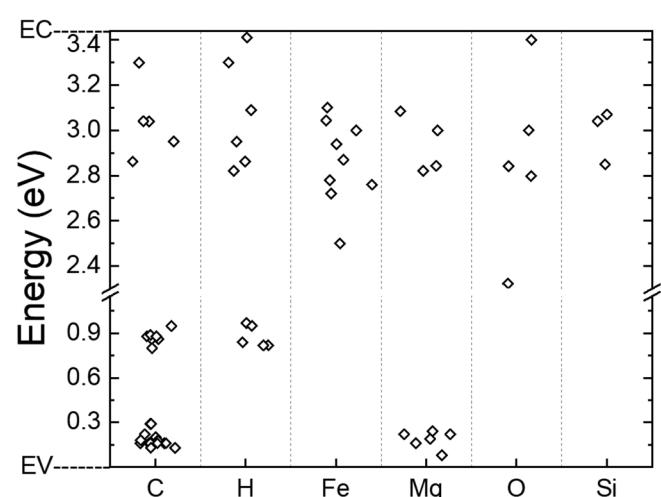
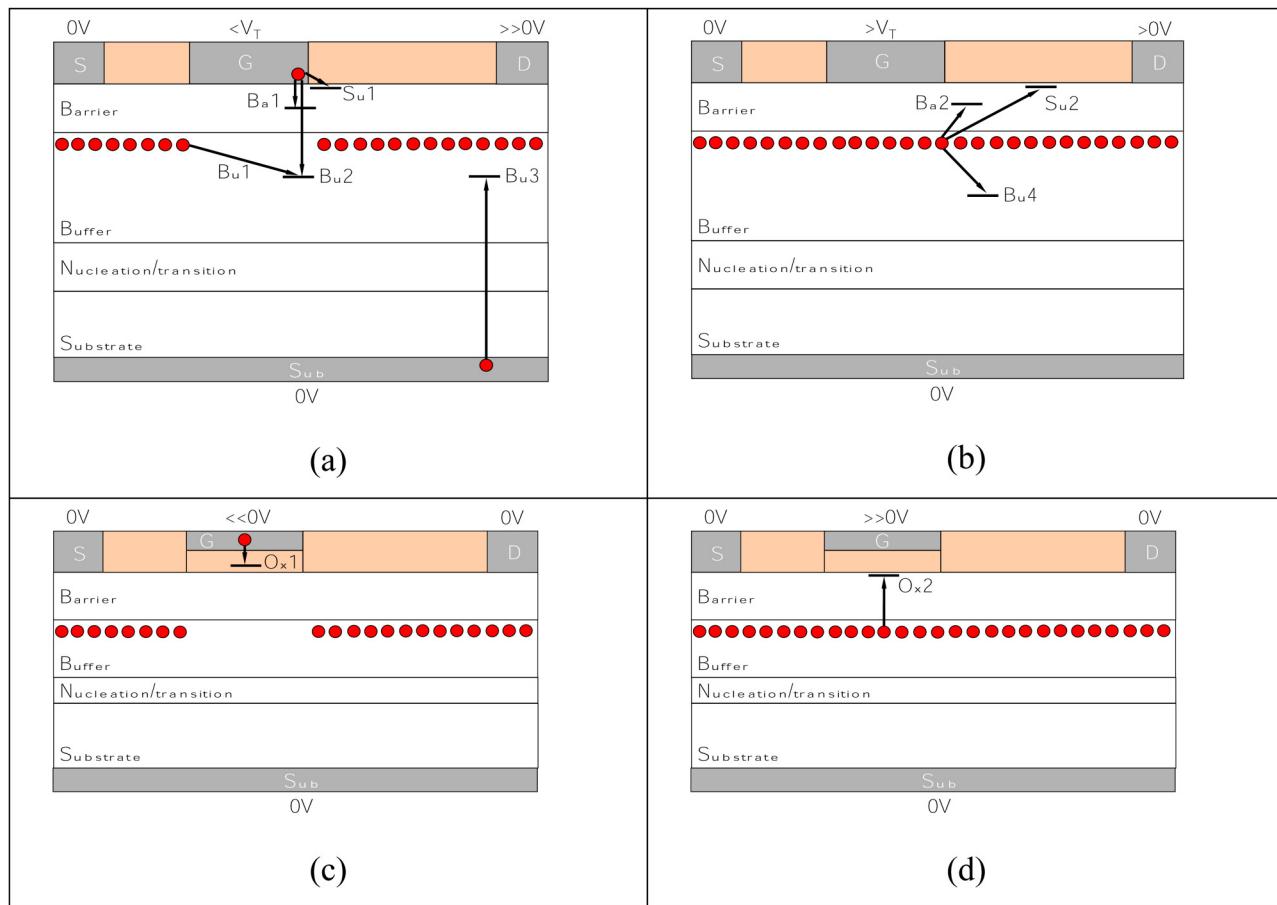


FIG. 72. Energy states detected in GaN and associated with impurities-related defects. The reference level, assumed to have energy equal to 0, is represented by the top of the valence band. The dispersion of the detected levels within the lower portion of the forbidden gap has been magnified with respect to Fig. 71.



19 January 2025 21:33:19

**FIG. 73.** Schematic illustration of a selection of trapping mechanisms listed in Table VIII, grouped according to bias conditions triggering the charging processes as follows: (a) OFF-state conditions at sub-threshold  $V_{GS}$  and large, positive  $V_{DS}$ ; (b) SEMI-ON or power-state conditions at above-threshold  $V_{GS}$  or large, positive  $V_{DS}$ , respectively; (c) negative gate bias; and (d) positive gate bias. Red circles and small bars represent electrons and traps, respectively. Arrows illustrate the charging path (not direct electron transfer into traps).

ascribed to generic Mg-related defects, whereas the  $E_C - 0.44$  eV level in Ref. 404 was associated with Mg–V<sub>N</sub> complexes.

Due to its unpaired valence electron, **hydrogen** is prone to form complexes with other chemical species in addition to magnesium. Different authors ascribe deep levels located between  $E_C - 2.62$  eV and  $E_C - 2.47$  eV to complexes formed between hydrogen and gallium vacancies,<sup>401,411</sup> even if the similarity between this range and the preferential energy positioning of V<sub>Ga</sub>-related defects indicates that those levels may be ascribed to the latter. Levels at  $E_C - 0.49$  eV and  $E_C - 0.578$  eV were tentatively assigned to carbon- and/or hydrogen-related defects, respectively, in Refs. 422 and 421.

Due to its very high electronegativity, **oxygen** also tends to bond with other impurities of native defects within the GaN crystal. One of the few literature reports investigating the formation of deep levels related to O in GaN associates the levels at  $E_C - 1.118$  eV,  $E_C - 0.642$  eV, and  $E_C - 0.599$  eV either to V<sub>Ga</sub>-O complexes or to dislocations.<sup>390</sup> In Ref. 423 the  $E_C - 0.44$  eV level

was ascribed to O<sub>N</sub>. The same interpretation was provided by the authors in Ref. 405 to tentatively explain the shallow  $E_C - 0.04$  eV donor level detected by means of photoluminescence (PL) measurements as part of a donor-acceptor pair.

**Iron** is often adopted in GaN-based transistors to intentionally reduce the intrinsic n-type conductivity of specific UID GaN layers. Several levels, ranging from  $E_C - 0.94$  eV to  $E_C - 0.34$  eV, have been detected and associated with Fe.<sup>389,409,424–427</sup> In particular, the authors in Refs. 427 and 426 agree when associating shallower deep states, respectively, detected at  $E_C - 0.34$  eV and  $E_C - 0.44$  eV, to transitions between, or related to, different charge states of the Fe atoms. Recent reports deeply investigated the signatures of Fe-related traps;<sup>162,438,439</sup> it was recently suggested that Fe<sub>Ga</sub> sites are related to a trap located at  $E_C - 0.58$  eV,  $\sigma = 2 \times 10^{-15} \text{ cm}^2$ .<sup>438</sup>

Like iron, **carbon** doping also is used to compensate the intrinsic n-type conductivity of the GaN crystal. This effect is achieved when C atoms occupy a substitutional position on the nitrogen site (C<sub>N</sub>). C<sub>N</sub> is a deep acceptor, with the (0/-) transition

level theoretically located at  $E_V + 0.9$  eV<sup>440</sup> and experimentally associated with a band of allowed states between  $E_C - 2.64$  eV and  $E_C - 2.49$  eV.<sup>384,385,419,430–432</sup> Being a deep acceptor, the  $C_N$  level does not generate large free hole density and strong p-type conductivity; large concentrations of  $C_N$  can pin the Fermi level at  $E_V + 0.9$  eV, leading to semi-insulating layers.  $C_N$  may also induce the formation of shallow acceptor-like levels in the  $E_C - 3.31$  eV to  $E_C - 3.15$  eV band.<sup>385,401,403,407,408,411–413,419,428–431</sup> On the other hand, if C occupies interstitial positions, the resulting  $C_I$  sites are believed to introduce a deep donor level in the upper part of the gap, with typical energies ranging from  $E_C - 1.35$  eV to  $E_C - 1.2$  eV.<sup>401,403,407,412</sup> Other shallower levels at  $E_C - 0.14$  eV,<sup>422</sup>  $E_C - 0.4$  eV,<sup>384</sup>  $E_C - 0.49$  eV,<sup>422</sup> and  $E_C - 0.578$  eV<sup>421</sup> have been tentatively ascribed to carbon- or hydrogen-related defects, with a speculative assignment of the  $E_C - 0.4$  eV to  $C_{Ga}$  sites.

## B. Trapping mechanisms

Traps influence the electrical behavior of transistors since they are characterized by relatively long capture/emission times<sup>356</sup> and thus they charge up or discharge following fast bias changes more slowly than device capacitances that govern the “prompt” device response.

Regardless of the nature of traps, i.e., whether they are associated with intrinsic crystallographic defects, unintentional or intentional impurities, or defect-impurity complexes, only those traps that have a chance to change their charge state during the device functioning through capture or emission of mobile carriers can induce electrical effects of concern for the dynamic device performance. Based on these considerations, trapping mechanisms can be categorized as the combination of a *trap location* plus an associated *charging/discharging path and type of involved mobile carriers*.

Traps can virtually be located in any semiconductor or dielectric layer as well as at interfaces, but locations that have more frequently been associated with harmful effects for GaN transistors include the device surface and the passivation within the gate-drain access region, the barrier, the buffer (including the interface with the barrier layer), and, if present, the gate dielectric (including the interface with the underlying semiconductor). The reported charging/discharging paths include all leakage currents from the device terminals (gate, source, drain, substrate), the 2DEG at the barrier/buffer interface in HEMTs and unrecessed or partially recessed MIS-HEMTs or the channel at the dielectric/GaN interface in fully recessed MIS-HEMTs, charge redistribution processes within floating C-doped buffer, as well as high-field mechanisms like field-enhanced emission, trap impact ionization, and Zener trapping. One or more of these paths can be activated depending on the applied device bias.

Two general remarks that will apply to all effects described below are as follows.

- (1) Since all-GaN transistors relevant for applications are n-channel field-effect transistors, traps can induce a reduction in the source-to-drain channel conductivity and, through this, in the drain current, if the negative trapped charge increases or the positive one decreases. These changes can either be the result of electron capture or hole emission. On the other hand, an increase in the channel conductivity and drain current can be promoted by electron emission or hole capture.

- (2) Trapping effects that take place in the device portion under the gate directly influence  $V_T$ , whereas those occurring in the gate-drain access region impact the drain access resistance and the transconductance peak.

**Table VIII** lists the major trapping mechanisms that have been reported in the literature classified in terms of trap location and corresponding charging/discharging path and type of involved mobile carriers. The different trapping mechanisms resulting from this classification will be described in more detail in Secs. VII C–VII H.

## C. Surface traps in the gate-drain access region

Surface traps in the gate-drain (G–D) access region (in the following, simply, surface traps) can capture electrons injected by the gate contact in GaN HEMTs (mechanism Su1 in **Table VIII**). This occurs as the device is biased under *OFF-state* conditions, i.e., when the gate is biased below threshold and a large, positive  $V_{DS}$  is applied. Gate-injected electrons can leak across the passivation<sup>358,441–443</sup> or propagate through surface traps by a hopping mechanism.<sup>444,445</sup> Trapped electrons are then slowly emitted by traps following the device switching to *ON-state* conditions, i.e., zero or positive  $V_{GS}$  with small, positive  $V_{DS}$ . To describe this mechanism, the “virtual gate”<sup>358</sup> concept has been used. In the early stage of the GaN HEMT development, this was the trapping process of major concern owing to the heavy limitation it could induce on the achievable RF output power and power-added efficiency. Passivation optimization<sup>446,447</sup> and field plate introduction<sup>448,449</sup> were key to minimize it, thanks to a combination of surface defect density reduction (passivation optimization) and gate-drain electric field mitigation (field plates).

Another possible charging path for surface traps is through trapping of 2DEG electrons gaining sufficient energy to overcome the barrier due to the AlGaN/GaN conduction band offset<sup>218,450–453</sup> (mechanism Su2 in **Table VIII**). This process requires the presence of channel hot electrons (CHEs) and, therefore, an accumulated device operation under *SEMI-ON* or *power-state* conditions (i.e., simultaneously high  $V_{GS}$  or  $I_D$  and  $V_{DS}$ ), like in RF power or hard-switching conditions.

As far as the physical nature of surface traps is concerned, dominant discrete levels<sup>57</sup> as well as distributed interface states<sup>58,454–456</sup> or border traps<sup>457</sup> have been reported.

Finally, since these traps are located within the drain access region, their primary, detrimental effect is an increase in the drain access resistance and, therefore, a reduction in the transconductance peak.

## D. Barrier traps

In GaN HEMTs, barrier traps located under the gate can capture electrons injected by the gate contact following OFF-state biasing and slowly emit them as the device is turned to ON-state conditions (mechanism Ba1 in **Table VIII**). Under power-state conditions, hot electrons from the 2DEG can instead be trapped by barrier traps located in the G–D access region<sup>451</sup> (mechanism Ba2 in **Table VIII**). The consequence is either a positive shift in  $V_T$  or an increase in the drain access resistance, depending on whether traps are located under the gate or in the G–D access region.

**TABLE VIII.** Classification of major trapping mechanisms in terms of trap location, charging/discharging path, and type of involved mobile carriers.

Mechanism label	Trap location	Charging/discharging path (type of involved carriers)
Su1	Surface in the G-D access region	Gate contact (electrons)
Su2	Surface in the G-D access region	2DEG (electrons)
Ba1	Barrier	Gate contact (electrons)
Ba2	Barrier	2DEG (electrons)
Ba3	Barrier	Field-enhanced ionization (electrons)
Ba4	p-GaN/AlGaN interface	p-GaN (holes)
Bu1	Buffer	Source contact (electrons)
Bu2	Buffer	Gate contact (electrons)
Bu3	Buffer	Substrate contact (electrons)
Bu4	Buffer	2DEG (electrons)
Bu5	Buffer	Zener trapping (valence-band electrons)
Bu6	Barrier/buffer interface	Zener trapping (valence-band electrons)
Bu7	Barrier/buffer interface	Trap impact ionization (electrons)
Bu8	C-doped buffer	"Leaky-dielectric" buffer
Bu9	C-doped buffer	C doping (holes)
Ox1	Gate dielectric	Gate contact (electrons)
Ox2	Dielectric/semiconductor interface	Channel/2DEG (electrons)
Ox3	Dielectric/semiconductor interface	C doping (holes)

During drain voltage sweeps, donor-like barrier traps can be ionized by field-enhanced electron emission<sup>458,459</sup> (mechanism Ba3 in Table VIII), in this case inducing an increase in the output conductance sometimes termed the "kink effect" (see Sec. VII G 4).

In normally OFF p-GaN HEMTs, hole trapping can take place at the p-GaN/AlGaN interface under positive gate bias<sup>88</sup> (mechanism Ba4 in Table VIII).

### E. Buffer traps

Buffer traps are probably the major source of trapping effects in present-day GaN transistors, following the already mentioned advancements in surface passivation and the introduction of field plates, which resulted in the effective minimization of surface trapping effects.

Buffer-trap effects have been associated with several different trapping mechanisms. The most straightforward charging path is through electrons originating, under OFF-state bias, from the source and/or gate contacts and forming the source-drain<sup>460–462</sup>

(mechanism Bu1 in Table VIII) and the gate-drain<sup>362</sup> (mechanism Bu2 in Table VIII) leakage currents, respectively. At very large drain voltages (always under OFF-state conditions), the substrate leakage current also comes into play, contributing to electron trapping into buffer traps mainly within the G-D access region under the drain contact<sup>463</sup> (mechanism Bu3 in Table VIII). Under SEMI-ON and power-state bias conditions, on the other hand, energetic 2DEG electrons can be injected deeply into the buffer and get thereby trapped, mainly in the G-D access region<sup>453,464</sup> (mechanism Bu4 in Table VIII).

Other buffer trapping mechanisms that have been invoked include the capture of valence band electrons through Zener processes involving traps in the buffer region under the gate edges<sup>465</sup> (mechanism Bu5 in Table VIII), and at the barrier/buffer interface<sup>466</sup> (mechanism Bu6 in Table VIII). Moreover, trap impact ionization by channel electrons has been proposed as a mechanism that can discharge traps at the barrier/buffer interface as the drain bias is increased above some critical voltage and resulting in the so-called "kink effect" in the device output characteristics<sup>374</sup> (mechanism Bu7 in Table VIII).

With relevance to power transistors with C-doped buffer, peculiar trapping effects taking place in the weakly p-type buffer characterizing these devices have been explained by the so-called "leaky-dielectric" model<sup>467</sup> to describe charge injection into the buffer region (mechanism Bu8 in Table VIII) or by hole redistribution within the buffer itself<sup>468</sup> (mechanism Bu9 in Table VIII).

As far as the physical origin of buffer traps is concerned, either GaN intrinsic defects<sup>462,469,470</sup> or intentional impurities have been correlated with the observed trapping effects. The latter are acceptor-like traps purposely introduced to suppress the n-type conductivity of GaN. Fe and C are the two species that are more commonly adopted.

Fe is generally adopted for RF transistors.<sup>462,471</sup> The dominant deep level introduced in the GaN bandgap by Fe doping is generally assumed to be energetically located at 0.5–0.6 eV from E<sub>C</sub>.<sup>389,424</sup> As a result, the Fe-related level behaves as an acceptor-like electron trap.

C is typically used for power devices<sup>1</sup> and can be incorporated (i) by tuning growth parameters to control the decomposition rate of TMGa and the incorporation of C from methyl group (autodoping<sup>135,472</sup>) or (ii) by adding a C precursor (propane, methane, ethylene)<sup>473</sup> to a CVD gas mixture (extrinsic doping). Early deep-level transient spectroscopy (DLTS)/deep-level optical spectroscopy (DLOS) measurements<sup>474</sup> and correlation with DFT calculations based on LDA approximation<sup>475</sup> suggested two deep levels related to C doping being the C<sub>N</sub> (acceptor) and C<sub>Ga</sub> (donor) centers, respectively, located at E<sub>V</sub> + 0.14 eV (or equivalently E<sub>C</sub> – 3.28 eV) and E<sub>C</sub> – 0.11 eV. More accurate and recent hybrid-functional DFT calculations yielded C<sub>N</sub> at E<sub>V</sub> + 0.9 eV and C<sub>Ga</sub> above E<sub>C</sub>, along with other C-related centers inside the bandgap like interstitial C<sub>I</sub> center at E<sub>C</sub> – 0.4 eV (acceptor) and the C<sub>Ga</sub>–V<sub>N</sub> complex at E<sub>C</sub> – 0.1 eV (donor<sup>440,476,477</sup>). While there is nowadays a rather general consensus that trapping effects in C-doped GaN transistors are mainly related to the dominant C<sub>N</sub> traps, many simulation-based works<sup>163,468,478–483</sup> suggest that some degree of auto-compensation between these acceptors and C-related donor traps must take place, reducing the effective acceptor density below the level of the introduced C concentration

(especially in the case of extrinsic C doping). On the other hand, higher donor concentration in GaN:C compared with donor density in undoped samples has been confirmed also experimentally.<sup>484</sup> The  $E_V + 0.9$  eV level is anyway able to induce the compensation of the buffer region, for suitable concentrations. As mentioned above, this may lead to peculiar trapping effects, which are still subject to investigation in the literature.<sup>479,485–488</sup>

Regardless of whether they are related to intrinsic defects or intentional impurities, buffer traps are essential to compensate the unintentional n-type conductivity (related to V<sub>N</sub>, Si, O) of nitrides, therefore allowing for an abrupt channel pinch-off, reducing the source-drain leakage current and increasing the OFF-state breakdown voltage. Owing to this, buffer optimization requires a trade-off between trapping effects and breakdown voltage. In the case of doped buffers, this is typically achieved by switching off the impurity flow during growth at a designed distance from the channel at the barrier/buffer interface.<sup>461,489</sup>

Similar to barrier traps, buffer electron traps can lead to a positive shift in  $V_T$  or an increase in the drain access resistance and  $R_{ON}$  depending on whether involved traps are located under the gate or in the G-D access region. Positive charge can also be accumulated in the buffer, leading to a decrease in  $R_{ON}$  under specific conditions.<sup>467,490</sup>

## F. Gate dielectric traps

In transistors with an insulated-gate structure, like AlGaN/GaN MIS-HEMTs, the gate oxide bulk and its interface with the underlying semiconducting region can also act as trapping sites.

As far as bulk oxide traps are concerned, the main charging/discharging path is through the gate electrode (mechanism Ox1 in Table VIII), which can inject electrons into the gate dielectric at large and negative  $V_{GS}$ <sup>491,492</sup> and remove trapped electrons out of the device under positive  $V_{GS}$ .<sup>493</sup>

For interface and border traps, the main charging path is through electron injection from the device channel at the AlGaN/GaN interface (in MIS-HEMTs) or the GaN surface (in MOSFETs) (mechanism Ox2 in Table VIII), which can be triggered at positive  $V_{GS}$  (forward gate bias<sup>368</sup>). These traps can instead emit electrons at negative  $V_{GS}$ .<sup>372</sup>

Another reported mechanism, specific to devices with a C-doped buffer, consists of hole capture into interface traps, where holes are provided by C-related acceptors in the buffer and not necessarily by a high-field electron-hole generation mechanism (mechanism Ox3 in Table VIII<sup>483</sup>).

Both bulk and interface dielectric traps affect the device performance through  $V_T$  by inducing instabilities on this crucial parameter.<sup>494</sup> These effects will be described in more detail in Sec. VII G 3.

## G. Trapping effects

In this section, the major charge-trapping effects observed in GaN transistors are reviewed and associated with the mechanism(s) put into evidence in Sec. VII F. The correlation between trapping effects and related mechanisms is summarized in Table IX.

### 1. RF current collapse

Considering RF amplification, the most harmful trap-related effect is the so-called *RF current collapse*<sup>358,359</sup> resulting in a reduction in the maximum drain current and simultaneous increase in the minimum drain-source voltage explorable by the operating point during the RF sweep. The increase in the minimum drain-source voltage is also referred to as *knee-voltage walkout*.<sup>358,495</sup> The overall result is a compression in the RF output power and a degradation of the power-added efficiency compared to the theoretical limits achievable by the given transistor that can be calculated from the DC output characteristics.

Responsible mechanisms are related to electron trapping taking place under OFF-state or SEMI-ON bias. Channel conductivity is weakened by this and cannot promptly be restored as the dynamic operating point moves to the ON-state. Electrons can be provided by the gate through tunneling injection at large drain-gate voltage, by the source via source-drain leakage current due to the large drain-source voltage, or by the 2DEG channel under SEMI-ON conditions. Gate electrons can reach the surface, barrier, as well as buffer traps, whereas source electrons can only get trapped into buffer traps. Channel hot electrons can be trapped by buffer, barrier, or surface traps. Either  $V_T$  or the drain access resistance or both parameters can, in principle, be increased, depending on whether electron trapping takes place under the gate, in the gate-drain access region, or both. A major impact is typically associated with electron trapping within the gate-drain access region. Optimization of surface passivation<sup>446,447</sup> and introduction of field plates<sup>448,449</sup> have comparatively decreased the role of surface and barrier traps as promoters of the RF current collapse, thanks to the mitigation of the electric field at the drain-end edge of the gate, leaving buffer electron trapping as the major responsible mechanisms, especially in technologies where compensating impurities (like Fe) are used in the buffer to increase the breakdown voltage.

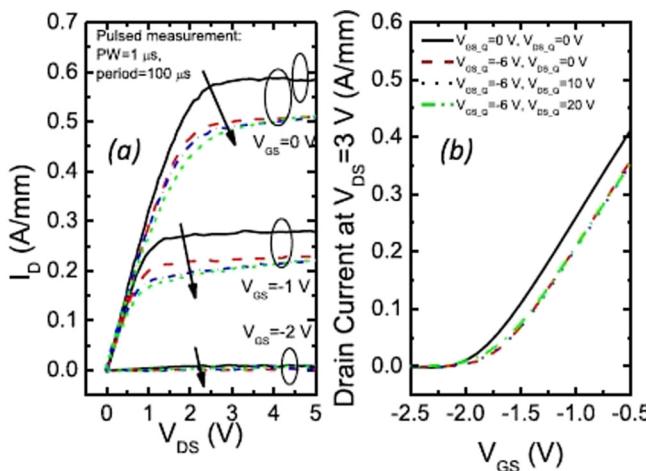
These effects are illustrated in Fig. 74, which shows the dispersion of the pulsed output characteristics from a Fe-doped AlGaN/GaN HEMT.

### 2. Dynamic $R_{ON}$ increase

When GaN transistors are used in power switching converters, the most detrimental trap-related effect is the increase in the

TABLE IX. Major trapping effects in GaN transistors with associated, responsible mechanism(s) (labeled according to Table I).

Trapping effect	Trapping mechanism(s)
RF current collapse	Su1, Su2, Ba1, Ba2, Bu1, Bu2, and Bu4
Dynamic $R_{ON}$	Su1, Su2, Ba1, Ba2, Bu1, Bu2, Bu3, Bu4, Bu5, Bu6, Bu8, and Bu9
Negative-gate-bias $V_T$ instabilities	Ox1, Ox2, Ox3, Bu5, and Bu8
Positive-gate-bias $V_T$ instabilities	Ox1 and Ox2
Kink effect	Ba3, Bu7, and Bu8



**FIG. 74.** (a) Pulsed  $I_D$ - $V_{DS}$  curves measured starting from different quiescent bias points, in the OFF-state, on a sample of wafer D (highest Fe content). (b) Pulsed  $I_D$ - $V_{GS}$  curves measured starting from different quiescent bias points in the OFF-state [same sample as in (a)]. Reproduced with permission from Meneghini et al., IEEE Trans. Electron Devices 61(12), 4070–4077 (2014). Copyright 2014 IEEE.

dynamic  $R_{ON}$  compared to its DC value, resulting in an undesirable increment in power losses.<sup>365,497</sup>

Possible underlying mechanisms include all electron trapping processes already described for RF current collapse, also taking place during the OFF-state phase of the switch-mode operation or during hard switching when large  $V_{DS}$  and  $I_D$  can temporarily co-exist. Channel conductivity, which is reduced by this increase in negative trapped charge, cannot be restored promptly as the device is driven to the ON-state, thus leading to the dynamic  $R_{ON}$  increase.

In addition to these mechanisms, there are additional trapping processes leading to dynamic  $R_{ON}$  increase that are specific to power transistors. These include the electron trapping into buffer traps within the gate-drain access region induced by the substrate leakage current.<sup>365,498</sup> The latter becomes comparable with gate and source leakage currents only at the very high drain voltages that are typically achieved in GaN power transistors only.

Carbon doping is commonly adopted in the buffer region of power transistors to increase the blocking voltage. When this is the case, the carbon-doped buffer can be the site for peculiar trapping mechanisms that are mainly governed by the  $C_N$  acceptor state at  $E_V + 0.9$  eV.<sup>135,470,474</sup> Holes are emitted by these traps within the gate-drain access region when the device is in the OFF-state, leading to an increase in the density of negatively ionized  $C_N$  acceptors, and therefore to a dynamic increase in the channel conductivity and  $R_{ON}$ .<sup>468,479</sup> It has been shown that both  $R_{ON}$  increasing transients under OFF-state bias stress and subsequent  $R_{ON}$  recovery transients may be thermally activated with the same activation energy of 0.9 eV.<sup>499,500</sup> This has been explained as the result of a thermally activated electron capture process<sup>365,498</sup> or, alternatively, by means of a hole redistribution model.<sup>468,501</sup> Recently, it was demonstrated that discharging and charging events in carbon-

doped GaN layers (GaN:C) can be governed by transport properties of GaN:C (details can be found in Ref. 488).

Recent works have shown that the dynamic  $R_{ON}$  can exhibit a non-monotonic dependence on the OFF-state drain voltage,<sup>502–504</sup> recovering to smaller values after reaching a maximum. This behavior has been explained by means of a “leaky-dielectric” buffer model: at high OFF-state bias, band-to-band tunneling through the UID channel layer may promote the generation of holes, which can be pushed to the bottom of the buffer, partially compensating the effect of the negatively ionized carbon acceptors.<sup>505</sup> A similar behavior was also attributed to holes generated by impact ionization, discharging the ionized  $C_N$  traps and thus attenuating the dynamic  $R_{ON}$  increase mechanism.<sup>482</sup>

Some of the above effects are illustrated in Fig. 75, which shows the dynamic  $R_{ON}$  variation measured on GaN-based power HEMTs and a schematic representation of the related processes.<sup>506</sup>

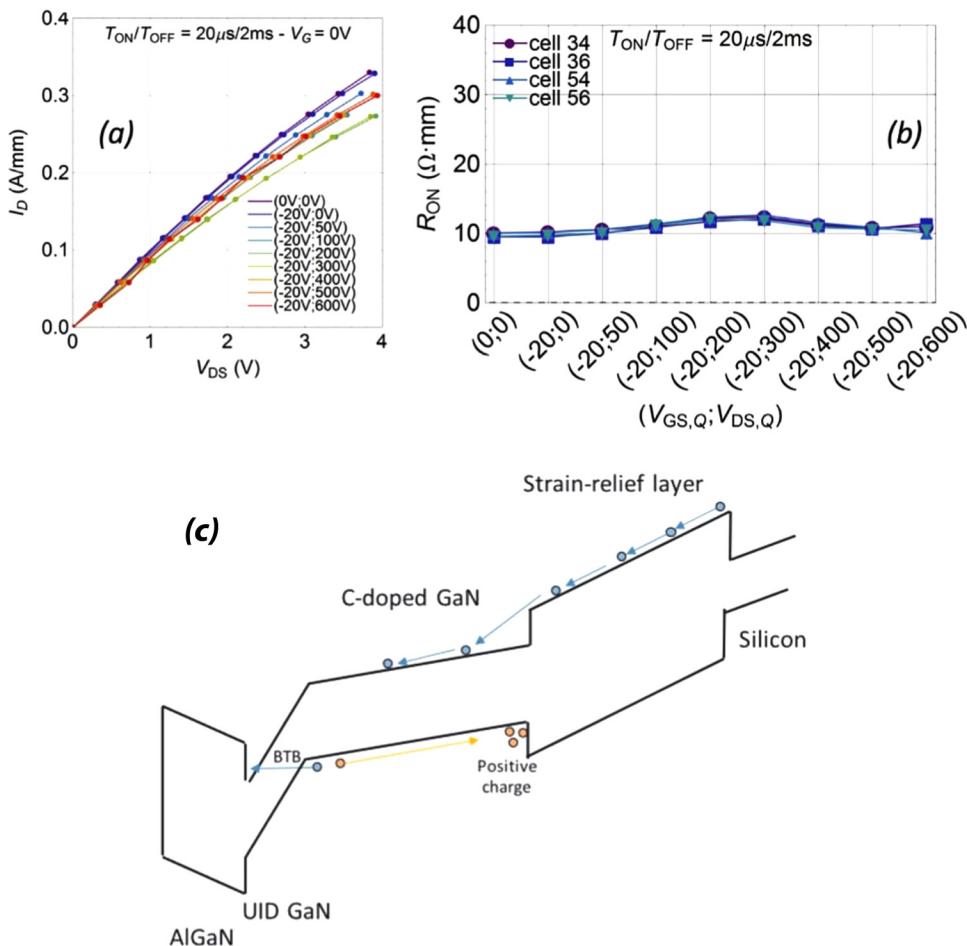
### 3. Threshold voltage instabilities in isolated-gate and p-GaN transistors

To suppress the gate current, which is a requirement particularly for power transistors, isolated-gate AlGaN/GaN MIS-HEMTs have been proposed and developed.<sup>1,507</sup> These include both un recessed or partially recessed MIS-HEMTs, in which the gate dielectric is deposited onto the AlGaN barrier, and fully recessed MIS-HEMTs, where the AlGaN barrier is completely removed under the gate region so that the gate dielectric is formed onto the GaN buffer region (while the 2DEG at the AlGaN/GaN interface survives in the two access regions).

In these transistor types, the gate dielectric bulk and its interface with the underlying semiconductor can also act as trapping sites. The most serious effects for device performance are the  $V_T$  instabilities adding up to other trapping effects like dynamic  $R_{ON}$ . These instabilities are typically analyzed by applying either negative gate bias (NGB) or positive gate bias (PGB) stress voltages with zero drain-source voltage, with the aim of isolating  $V_T$  effects from the drain access resistance ones.<sup>508</sup>

For normally ON devices with negative threshold voltages of several volts,  $V_T$  stability under NGB is, in particular, a critical aspect that needs careful evaluation during technology development. In normally OFF devices,  $V_T$  stability under PGB is instead of major concern. In the latter devices, assessing the  $V_T$  stability under NGB can be important as well, since a negative gate voltage can be applied to switch off the transistor, in order to prevent false turn-on and ensure safe operation against voltage spikes on the gate.<sup>509</sup> Moreover, NGB measurements are in any case a proxy for the OFF-state operation, as similar large values of drain-gate voltage can be achieved with both biasing conditions.

As far as NGB effects are concerned,  $V_T$  shifts of either negative (i.e.,  $V_T$  becoming more negative<sup>372,373,510</sup>) or positive (i.e.,  $V_T$  becoming more negative<sup>491,509,511</sup>) sign, as well as of both signs depending<sup>465,492</sup> on applied bias, temperature, and stress time have been reported. The trapping mechanisms that have been held responsible for the negative  $V_T$  shifts are (a) electron emission from interface and/or border traps;<sup>372,373,492</sup> (b) decrease in the negatively ionized C-related acceptors in the buffer region under the gate;<sup>510</sup> and (c) hole capture into interface traps, where holes



**FIG. 75.** (a) Pulsed IV curves measured at room temperature on a GaN-based power HEMT. (b) Dependence of ON-resistance on the applied trapping bias (the four lines refer to four devices sitting on different locations on the wafer).<sup>506</sup> Schematic representation of the mechanisms responsible for non-monotonic dynamic  $R_{ON}$  as a function of trapping voltage. Reproduced with permission from Meneghini *et al.*, J. Mater. Sci. Semicond. Process. **78**, 118–126 (2018). Copyright 2018 by the authors of the cited paper, licensed under CC BY 4.0.

19 January 2025 21:33:19

are provided by C-related acceptors and not necessarily by a high-field electron-hole generation mechanism.<sup>483</sup> Positive  $V_T$  shifts have instead been attributed to (d) electron injection from the gate and consequent electron capture into gate dielectric traps;<sup>491,492</sup> (e) hole-induced defect generation in the gate insulator<sup>509,511,512</sup> or interface state generation;<sup>465</sup> (f) Zener electron trapping into GaN traps localized under the gate edges,<sup>465</sup> and (g) the recombination of holes provided by the C doping (and attracted to the device surface) with electrons injected from the gate.<sup>483</sup>

Also PGB experiments can produce  $V_T$  instabilities of both signs. More commonly, positive  $V_T$  shifts are observed.<sup>373,513,514</sup> These are attributed to channel electron injection into interface or border traps.<sup>368,513,514</sup> Negative  $V_T$  shifts under PGB have instead been explained as the result of electron removal from dielectric traps through the gate.

$V_T$  stability of devices with p-GaN gate after PGB stress is of a great concern because of the normally OFF operation.<sup>515</sup> By

focusing on trap-related instabilities, electron injection from the 2DEG into pre-existing defects in the AlGaN barrier (also occurring in HEMT and MIS-HEMT structures) has been reported to cause  $V_T$  to shift positively. On the other hand, negative  $V_T$  shifts have been attributed to trapping of holes at the p-GaN/AlGaN interface.

Some of the above effects are illustrated by Fig. 76, showing  $V_T$  instability effects induced by NGB (up<sup>372</sup>) and PGB (bottom<sup>516</sup>).

#### 4. “Kink” effect

The “kink” effect is an operational instability emerging during a  $V_{DS}$  sweep, by which the drain current in the saturation region is initially compressed and then increases, over a relatively narrow voltage range, to a higher value.<sup>375,459,517</sup> This behavior is detrimental particularly in transistors for RF amplifiers because it can

result in transconductance compression and output conductance increase.<sup>374,518,519</sup>

Most recent works on this issue proposed that the kink effect can be caused by (i) impact ionization of traps in the channel or the barrier, with consequent emission of electrons,<sup>374,520,521</sup> (ii) trapping of holes generated by trap-assisted tunneling into C-related traps, and<sup>487,522</sup> (iii) field-enhanced ionization of AlGaN barrier traps under the gate and near the GaN/AlGaN interface.<sup>459</sup>

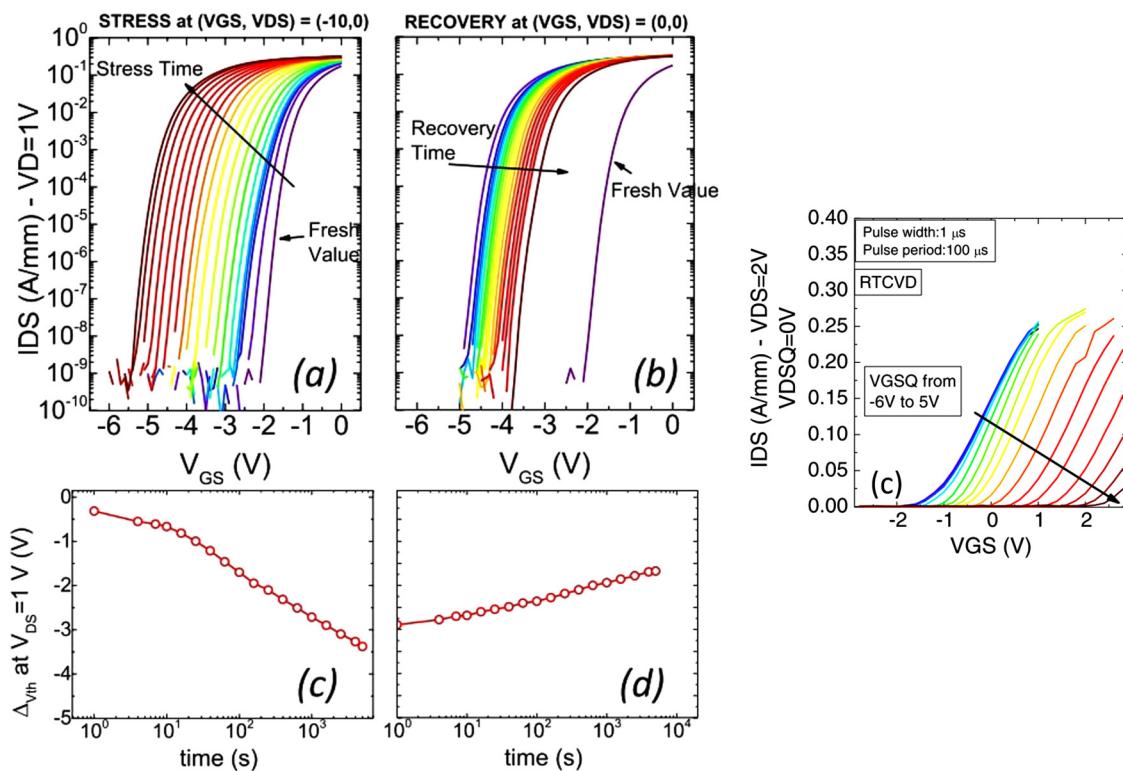
## H. Trap characterization techniques

Within this section, an overview of different techniques adopted for the characterization of trapping phenomena will be provided. Pulsed I-V (PIV) characterization will initially be introduced. Even if it does not provide a quantitative characterization of trap activation energies, it is a widely used tool to highlight the presence of trapping phenomena. Deep-level transient spectroscopy and deep-level optical spectroscopy will then be discussed. Their combination provides the characterization of trap levels located within the full gap of GaN. Nevertheless, specific test structures are needed, making them difficult to apply directly on actual transistors. Characterization techniques based on the monitoring of

device drain current evolution will then be introduced and the different methods will be commented. Monitoring of drain current for emission process characterization supposes that the emission process takes place when the device is biased in the ON-state. If traps experience said emission when the device is biased in the OFF-state, it would be thus impossible to properly characterize them. On-the-fly characterization overcomes this issue, allowing for the characterization of traps experiencing charge emission during the OFF-state operation. Interface states can be characterized by specific measurement based on capacitance-voltage (C-V) and conductance-voltage (G-V). Finally, the photoluminescence (PL) measurement technique will be briefly described.

### 1. Pulsed I-V

As previously introduced, trap characterization can be carried out by means of several techniques. The most important measurement adopted to quickly identify the presence of trapping phenomena is pulsed I-V (PIV) characterization. The concept of this measurement is rather simple. The device is held into a quiescent bias point (QBP), also called baseline, with its source terminal grounded. Synchronous and short voltage pulses, typically in the



19 January 2025 21:33:19

**FIG. 76.**  $V_T$  instabilities effects induced by NGB [(a) and (b)]. Reproduced with permission from Meneghini *et al.*, IEEE Electron Device Lett. **37**(4), 474–477 (2016). Copyright 2016 IEEE. VT instabilities effects induced by PGB (c). Reproduced with permission from Rossetto *et al.*, Microelectron. Reliab. **55**, 1692–1696 (2015). Copyright 2015 Elsevier.

100 ns–10  $\mu$ s range with a duty-cycle in the 0.1%–1% range, are applied to the gate and drain terminals to evaluate the device I–V characteristics. The basic idea is that traps are not able to reach their equilibrium condition during the short duration of the pulses. Therefore, the measurement yields the I–V characteristics of the device obtained with the traps filled at the condition set by the quiescent bias point. Since trap filling condition strongly depends on the applied voltages, comparing pulsed I–V obtained at different quiescent bias points quickly allows us to evaluate the presence and in some way the amount of trapping phenomena. A typical set of pulsed I–V is performed by comparing at least three or more different quiescent bias points:<sup>445,523,524</sup> (i) the  $V_{GS} = 0$  V,  $V_{DS} = 0$  V QBP, which sets also the reference of the “fresh” device conditions; (ii) gate-lag effect is then evaluated with a QBP where  $V_{GS}$  is held below the device threshold voltage and  $V_{DS} = 0$  V; and (iii) drain-lag effect is finally evaluated by a QBP with the device in OFF-state conditions and large  $V_{DS}$ . Obviously, many other combinations can be considered but the three reported are the most used for device characterization. PIV characterization quickly offers an overview on device operation and a qualitative evaluation of the reduced device performance due to trapping phenomena. Some information on trap spatial localization might also be obtained by comparing results from different QBPs. If the device experiences a threshold voltage shift, trapping phenomena are likely to be confined within the device buffer layer and/or the barrier or insulator layer under the gate terminal.<sup>500</sup> On the other hand, a decrease in its transconductance might be related to an increase in access region resistance, which might be induced by surface, barrier, or buffer traps.<sup>445</sup>

## 2. DLTS/DLOS

Trap investigation has been an important topic since the beginning of the semiconductor device development. Capacitance transients are used to obtain information about an impurity level in the depletion region of a Schottky barrier or a p–n junction. The measurement consists in observing the capacitance transient associated with the return to thermal equilibrium of the occupation of the level, following an initial nonequilibrium condition.<sup>525,526</sup> One can thus measure the time constant of this capacitance transient as a function of temperature and obtain the activation energy for the level. An alternative method named deep-level transient spectroscopy (DLTS) was introduced in Ref. 527 (see Fig. 77). DLTS is still based on capacitance transients but it allows faster characterization. The essential feature of DLTS is the ability to set an emission rate window such that the measurement apparatus only responds when it sees a transient with a rate within this window. Thus, if the emission rate of a trap is varied by varying the sample temperature, the instrument will show a response peak at the temperature where the trap emission rate is within the window. These emission rates are thermally activated and by the principle of detailed balance can be given as

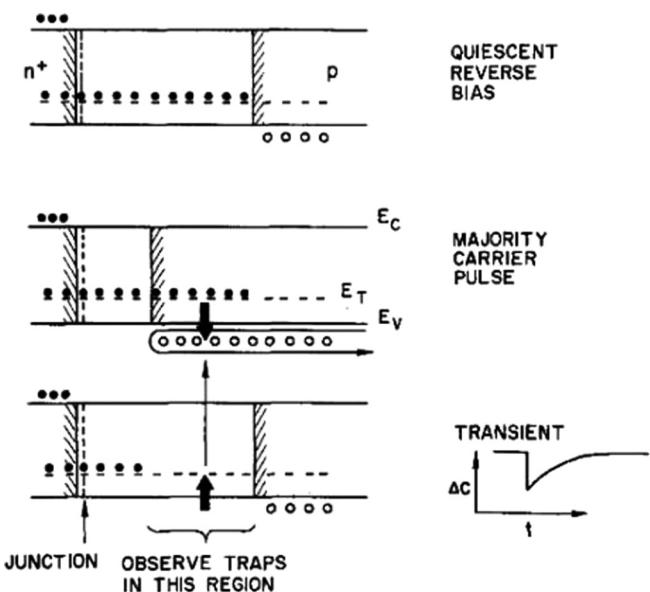
$$e_1 = (\sigma_1 v_1 N_{D1}/g_1) \exp(-\Delta E/kT), \quad (32)$$

where  $\sigma_1$  is the minority-carrier capture cross section,  $v_1$  is the mean thermal velocity of minority carriers,  $N_{D1}$  is the effective

density of states in the minority-carrier band,  $g_1$  is the degeneracy of the trap level, and  $\Delta E$  is the energy separation between the trap level and the minority-carrier band.

While DLTS is still one of the most used techniques, it also shows some limitations. Impurity levels with a large activation energy result in a low emission rate, leading to transients with large time constants whose evaluation could be masked by slow drifts.<sup>528</sup> A novel methodology was thus introduced in Ref. 529 with the name of deep-level optical spectroscopy (DLOS). DLOS is based on photostimulated capacitance transient measurements after electrical, thermal, or optical excitation of the sample. By increasing the energy of the photons impinging on the device, the optical cross section for the transition between the deep level and the conduction and valence band can be extracted. DLOS can provide information not only about the ionization energies of the levels but also about the electron–phonon interaction and temperature dependence of the levels, i.e., about their relations with each band.<sup>529</sup>

Due to its wide bandgap, the characterization of the GaN material was typically carried out by combining both DLTS and DLOS measurements. DLTS is adopted for evaluating levels with activation energies below approximately 1 eV, while deeper levels are typically investigated by means of DLOS.<sup>474,530,531</sup> The combination of the two measurement techniques allows a full investigation of the trap level within the whole GaN bandgap.



**FIG. 77.** Majority-carrier pulse sequence which is used to produce a capacitance transient for a majority-carrier trap. The energy-vs-distance diagrams (with band bending omitted for simplicity) show the p+n junction depletion region (edges denoted by shaded lines) as well as the capture and emission processes and trap occupation before, during, and after a majority-carrier pulse. Reproduced with permission from Lang, J. Appl. Phys. **45**, 3023–3032 (1974). Copyright 1974 AIP Publishing LLC.<sup>527</sup>

19 January 2025 21:33:19

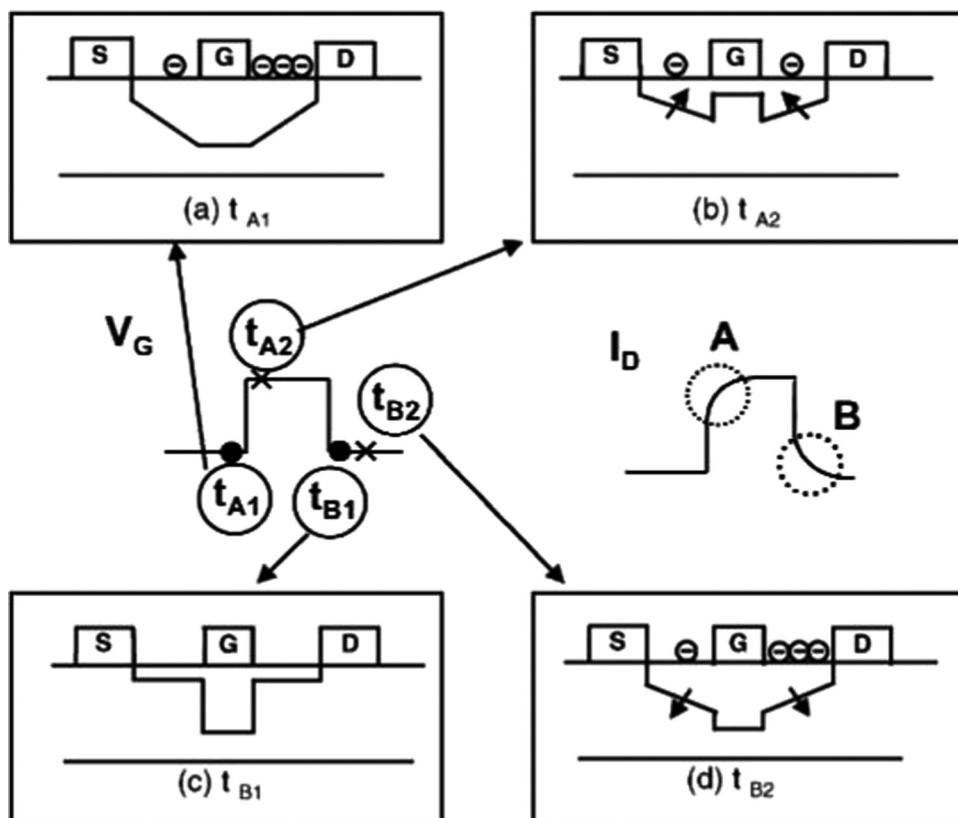
### 3. Current transients

DLTS and DLOS techniques are typically applied to large-area diodes, in order to have a well measurable capacitance value. When three-terminal devices are tested, these techniques suffer from the low device capacitance (typically in the pF range), making them less appealing for trap characterization. Furthermore, the electric field distribution in actual transistors in normal bias conditions can be significantly different from that in large-area diodes. Consequently, while DLTS and DLOS can definitely provide useful information on crystal impurities, they might not be able to provide a clear indication on the effects of said impurities on actual device dynamic operation. Trapping sensing in DLTS and DLOS is provided by evaluating capacitance transients induced by depletion region variations linked to the emission of trapped charge. On an actual device, the effect of charge emission can be monitored by evaluating the drain current evolution as the emission process takes place. In fact, an emission of trapped electrons will lead to a decrease in the fixed negative charge within the device, leading to an increase in its 2DEG concentration,<sup>532</sup> and, therefore, an increase in its drain current. Drain current transients (DCTs) are typically evaluated by monitoring the device current in the ON-state, after applying for a certain time a different bias condition typically in OFF-state condition (corresponding to the application of a  $V_{GS}$  below device  $V_{TH}$  and large  $V_{DS}$ ). It should be stressed though that this is only one of the possible biasing conditions. Generally speaking, any variation in the device bias point can,

in principle, lead to a variation in traps occupancy and thus cause during the emission process the observation of a DCT. On the practical side, traps' characterization based on device current variations can be performed by means of drain current DLTS (ID-DLTS),<sup>533,534</sup> constant drain current DLTS/DLOS (CID-DLTS/DLOS),<sup>428,535</sup> or multiple DCTs measurements carried out at different temperatures.<sup>445,536</sup> Pulsed drain current methodologies have also been proposed to characterize the de-trapping processes in the absence of applied bias.<sup>537</sup>

*a. ID-DLTS.* ID-DLTS<sup>533,534</sup> is typically performed by applying a constant  $V_{DS}$  voltage to have a readable drain current. The gate terminal is periodically pulsed between a filling condition and a sensing condition (see Fig. 78). The sensing condition is typically slightly above device threshold voltage, with the aim of obtaining a readable current level while at the same time reducing device self-heating effects. Monitoring the current transient over a certain temperature range allows us to obtain a plot of the DLTS signal vs temperature. The detection of peaks in DLTS spectra corresponds to the presence of a trap level, whose activation energy can be extracted by means of an Arrhenius plot.

*b. CID-DLTS/DLOS.* The CID-DLTS/DLOS<sup>428,535</sup> technique is based on a dynamic control of either the device gate or drain voltages with the aim of maintaining a fixed drain current in response



**FIG. 78.** Schematic illustration of response of the depletion layers: (a)-(d) represent the response of the depletion layer at the timing of  $t_{A1}$ ,  $t_{A2}$ ,  $t_{B1}$ , and  $t_{B2}$  on the gate bias pulse, respectively. Reproduced with permission from Okino et al., IEEE Electron Device Lett. **25**(8), 523–525 (2004). Copyright 2004 IEEE.

19 January 2025 21:33:19

to a thermally and optically stimulated trap emission. For a gate-controlled method, a constant and large enough  $V_{DS}$  is applied to the device to have it working in its saturation region. The gate terminal is pulsed to the ON-state to induce trap filling and then lowered near pinch-off conditions. The dynamic control on  $V_{GS}$  for maintaining a constant  $I_{DS}$  will thus give rise to a  $V_{GS}$  transient, which will thus be recorded. This condition is sensitive for trap levels located beneath the gate contact and affecting device  $V_{TH}$ . For a drain-controlled method, the device is biased in its linear region with low  $V_{DS}$  and a  $V_{GS}$  large enough to have a negligible forward transconductance  $g_m$ . Filling condition here is obtained by biasing the device in pinch-off conditions with large  $V_{DS}$ . The subsequent change in device resistance  $\Delta R_D = \Delta V_{DS}/I_{DS}$  is then recorded. This condition is particularly sensitive to traps located in the device access regions. The detection of peaks in either the temperature or optical spectra corresponds to the presence of a trap level, whose activation energy can be extracted by means of an Arrhenius plot.<sup>428,535</sup>

c. *Multiple DCTs.* Multiple DCT measurements provide an important advantage in reducing the number of measurements to be carried out, since DCTs are typically evaluated at some (5–10) temperature levels. On the one hand, this technique is rather simple and can be easily applied to actual transistors. Voltage pulse generators or a load-line drain biasing network are required to switch the device between a filling and a sensing condition<sup>538</sup> (see Fig. 79). Multiple DCTs, however, can yield results that might be strongly dependent from the device bias conditions used, and the method adopted for the analysis of DCTs required for Arrhenius plot extraction.<sup>536</sup> Additional comments on bias conditions and the DCT analysis will be provided in Secs. VII H 3 d and VII H 3 e.

d. *Bias conditions.* DCTs can be recorded with a sensing condition lying in the linear<sup>123,539,540</sup> or in the saturation region.<sup>445,541,542</sup> Significantly different results might be obtained when comparing results obtained in the linear and saturation region.<sup>536</sup> Nevertheless, an accurate evaluation of the different

DCTs response might be useful for spatially localize traps as suggested by Ref. 535: a sensing condition in the linear region of the device with reasonably high  $V_{GS}$  should highlight the effect of traps located within the device access regions. On the other hand, sensing in saturation near the pinch-off voltage, i.e., at low current level so that the effect of device access region can be minimized, should be more sensitive to the effect of traps located beneath the gate contact. Other phenomena that might significantly affect the results of DCTs analysis could be the presence of mechanisms affecting the DCTs time constants, i.e., device self-heating and electric field enhanced emission mechanisms. Self-heating by raising the local device temperatures enhances carrier emission process leading thus to an erroneous evaluation of the emission process. In other words, the de-trapping appears faster than it should be at the applied baseplate temperature.<sup>543</sup> Similarly field enhanced emission mechanisms such as Poole–Frenkel phenomena<sup>544</sup> will lead to an error like that introduced by device self-heating. Therefore, DCT results need to be carefully reviewed to avoid an erroneous estimation of the activation energy associated with the trap level causing the observed DCTs. Based on the comments and issues reported in this section, the authors would like to suggest that, to have an accurate estimation of the trap activation energy,  $V_{DS}$  voltages applied during the sensing condition should be as low as possible, in order to reduce self-heating and electric field related enhanced emission. The use of pulsed drain current transient (P-DCT) methodologies can also be effective to this aim, since the device is kept at zero bias during recovery, and short voltage pulses are used to sense the ON-resistance during the de-trapping phase.<sup>537</sup>

e. *Analysis of DCTs for time constant extraction.* The extraction of time constants at different temperatures is the process leading to the construction of the Arrhenius plot from which the trap activation energy is obtained. Several techniques can be used to this aim. A multi-exponential approach<sup>539</sup> can be adopted by least-square fitting the experimental data with the sum of several exponential functions, typically in the amount of few hundreds, with different amplitudes and time constants as described in the following equation:

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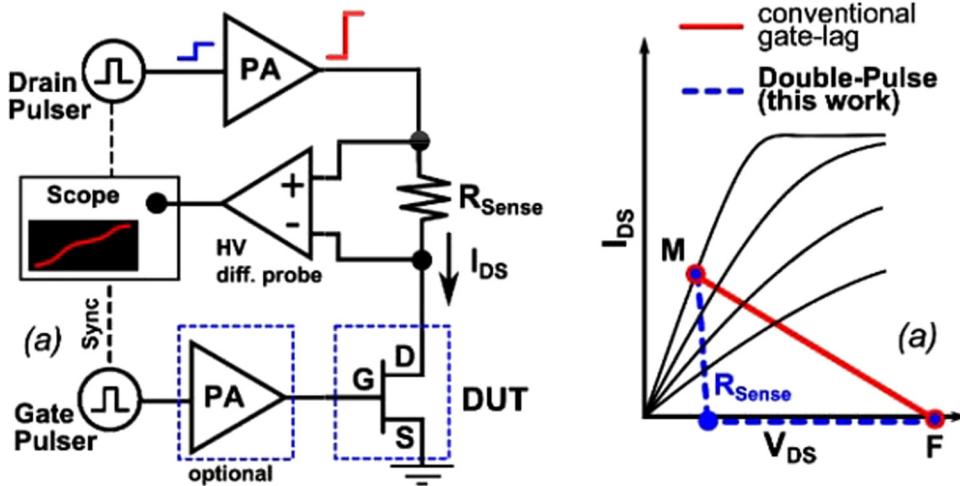
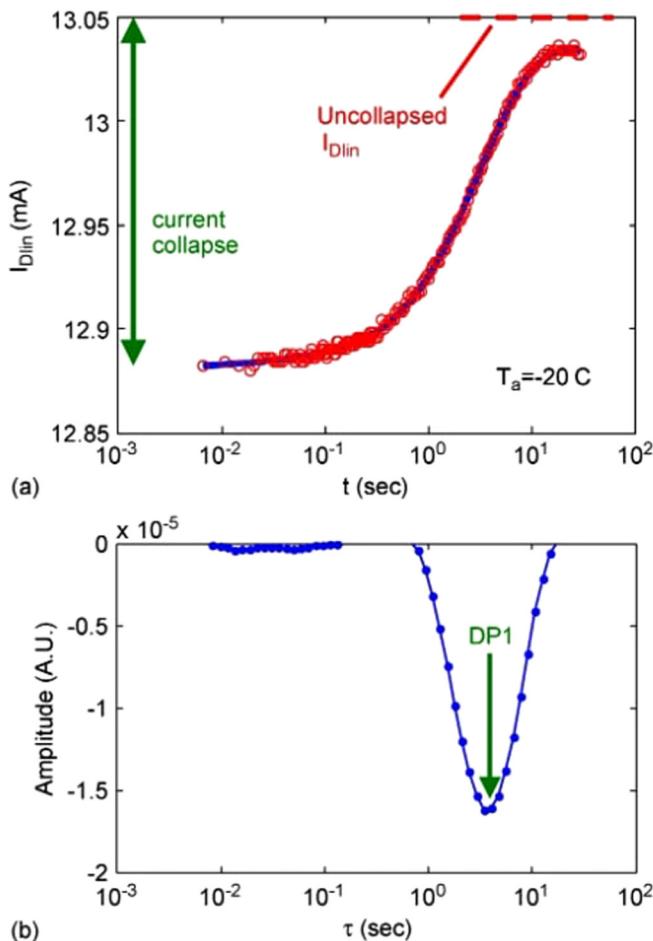


FIG. 79. (Left) Schematic representation of a system to switch the device between a filling and a sensing condition. (Right) Switching trajectories for device analysis. Reproduced with permission from Bisi et al., 2014 IEEE International Reliability Physics Symposium (IEEE, 2014), pp. CD.11.1–CD.11.4. Copyright 2014 IEEE.



**FIG. 80.** (a) Recovery transient of  $I_{Dlin}$  and (b) corresponding time-constant spectrum at  $-20^\circ C$  after applying a 1 s  $VDS=0$  and  $VGS=-10\text{ V}$  trapping pulses. Reproduced with permission from Joh and del Alamo, IEEE Trans. Electron Devices **58**(1), 132–140 (2011). Copyright 2011 IEEE.

$$I_{fitted} = \sum_{i=1}^n a_i \exp(-t/\tau_i) + I_\infty. \quad (33)$$

By plotting the amplitude coefficients  $a_i$  vs the time constants  $\tau_i$ , the trap associated time constants can be inferred by looking at the peaks of the spectra obtained, see, for example, Fig. 80.

A different approach relies on the so-called stretched exponential fitting.<sup>358,445</sup> This least-square method fits the experimental data by means of stretched exponential functions, one for each of the low-pass or high-pass transitions observed in DCTs according to the equation:

$$I_{fitted} = \sum_{i=1}^n a_i \exp(-t/\tau_i)^{\beta_i} + I_\infty, \quad (34)$$

where  $n$  here corresponds to the number of transitions observed in DCTs, which typically ranges between 1 and 3. Note that each exponential function corresponds to potentially a different charge emission/capture process. The Arrhenius plot of each of the  $i$ th process is then built using the  $\tau_i$  values obtained at different temperatures.

An alternative approach widely used is the analysis of the derivative of the DCT by the logarithm of time.<sup>423,540</sup> Peaks in the derived spectra are used to locate the characteristic time constants of different traps and used to derive the emission energies.

#### 4. On-the-fly characterization

The trap characterization methods based on the sensing of device drain current assume that the emission process takes place when the device is biased in the ON-state. Only in this way, it is possible to observe current variations linked to charge emission processes. If said emission process would take place instead in OFF-state conditions, it would be impossible to perform a proper characterization. An example of a trap level behaving in such a manner as been proposed in Ref. 479, where it has been suggested that carbon doping might introduce a hole-trap whose emission process takes place during the biasing in the OFF-state condition. The analysis of such a trap level can be performed then by means of the so-called on-the-fly characterization.<sup>366,545</sup> Basically, the device is biased in a condition promoting the charge emission process, and it is periodically turned on to sample within a short time interval the drain current evolution. This allows us to obtain a drain current evolution like that of DCTs and consequently extract trap activation energies using the methods previously described.

#### 5. Interface trap characterization by means of C-V and G-V measurements

Surface states at metal-insulator-semiconductor interfaces are typically characterized by means of capacitance-voltage (C-V) and conductance-voltage (G-V). C-V measurements were proposed as a tool for evaluating surface states density and energy distribution.<sup>546,547</sup> The combination of both C-V and G-V measurements<sup>548</sup> can also be used to calculate the interface state density NSS, whose most accurate calculation can be obtained by means of the Nicollian-Goetzberger theory.<sup>549</sup> The said method presents some issue related to the need of an extensive data acquisition. An alternative method based on single-frequency approximation can also be used,<sup>550</sup> which allows us to estimate the NSS from the equa-

$$N_{ss} = \frac{2}{qA} \frac{G_{m,max}/\omega}{\left(\frac{G_{m,max}}{\omega C_{ox}}\right)^2 + \left(1 - \frac{C_m}{C_{ox}}\right)^2}, \quad (35)$$

where  $q$  is the electronic charge,  $A$  is the area of the capacitor,  $G_{m,max}$  is the peak value of conductance,  $\omega = 2\pi f$  where  $f$  is the measurement frequency,  $C_{ox}$  is the capacitance in accumulation region, and  $C_m$  is the capacitance corresponding to  $G_{m,max}$ . This method has been successfully applied to the characterization of GaN-based devices.<sup>551,552</sup> in which the G-V measurement<sup>549</sup> relies upon the assumption that energy losses and leakage currents in dielectrics

are negligibly small.<sup>553</sup> To this end, quasi-static capacitance–voltage (QSCV) measurement<sup>554</sup> is rarely used in AlGaN/GaN HEMTs, because of the high leakage current associated with the Schottky gate.<sup>367</sup> To overcome the oxide leakage problem in GaN-based structures, high-frequency C–V measurements (HFCV) are typically adopted.<sup>555–557</sup> Nevertheless, standard HFCV measurements performed at room temperature (RT) may not be adequate to characterize wide-bandgap GaN and AlGaN interfaces<sup>558</sup> because of the extremely long time constants of deep interface traps. In fact, said deep levels are frozen at RT, thus requiring elevated temperature C–V measurement to accurately characterize the interface quality.<sup>551</sup> Recent papers pointed out that the conductance method may show limitations on AlGaN/GaN metal–insulator–semiconductor capacitors and discussed the related implications.<sup>559</sup> Other papers<sup>560</sup> proposed methodologies to analyze the interface state density of dielectric/GaN MIS devices. The wide bandgap of GaN limits hole generation at room temperature, allowing measurements in deep depletion. By a photoassisted high-frequency capacitance–voltage characterization, it is possible to measure the total interface state density throughout the bandgap, by using an above bandgap light source.

## 6. Photoluminescence (PL)

Photoluminescence (PL) spectroscopy is a commonly used technique for studying optical properties, measuring bandgap energy, determining phonon modes, and identifying energy levels due to impurities or defects.<sup>561,562</sup> During PL measurements, a light with fixed energy above the energy gap of the material being characterized is directed on the sample under test. Luminescence is then detected at different wavelengths, and peaks can be observed in correspondence of allowed (radiative) transitions within the energy gap of the semiconductor. One of the most famous result obtained by PL on GaN layer has been the so-called yellow-band YL.<sup>563,564</sup> PL is a relatively fast, contactless, and nondestructive technique and can provide very high spatial resolution. It thus offers the possibility to evaluate material properties from samples of various sizes (from micrometers to centimeters) without having to undergo a complex sample preparation.<sup>565</sup>

## VIII. DEGRADATION PROCESSES IN GaN DEVICES

The possible device types and structures based on GaN have a huge variety, as well as many applications, and therefore a high number of possible degradation and failure modes may take place. In this section, we will review the most relevant ones, with reference to lateral and vertical devices. The discussion will be organized based on the operating conditions that lead to the detected effects. In the first part, the ON-state and OFF-state bias conditions will be discussed, since they are the most relevant ones for a power device. Then, the transition between the two phases will be considered, leading to additional degradation in the SEMI-ON-state. Finally, reliability in a realistic environment will be analyzed, including the study of electrostatic discharge (ESD) and electrical overstress (EOS) events, and radiation hardness.

### A. ON-state

The ON-state bias condition can be heavily stressful for several reasons. A large gate overdrive is usually desired, in order to increase the channel carrier density and, therefore, the maximum current levels, but this leads to a high voltage drop and electric field across the gate stack. Moreover, although the desired voltage drop on the device should be zero in the ON-state, to ensure maximum power transfer and no power loss, real devices may have voltage drops in the range of hundreds of millivolts. At the high operating current levels, this may cause a significant power dissipation and self-heating that can be detrimental for long-term operation.

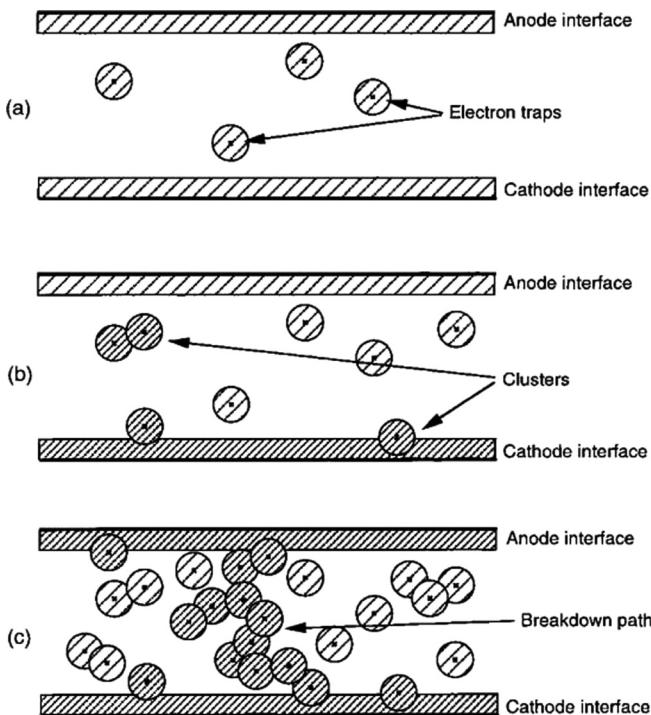
#### 1. Extrinsic degradation: The role of dielectrics

A high gate overdrive can be dangerous for insulated-gate devices, where the electric field in the gate dielectric has to be engineered in order not to exceed the breakdown value.

Even when this design rule is correctly achieved, the insulator can still show some degradation in its performance over time, due to a physical process called time-dependent dielectric breakdown (TDDB) and usually linked to defect percolation.<sup>566</sup> As shown in Fig. 81(a), before stress some defects are already present in the bulk of the oxide. When the device is stressed [Fig. 81(b)], additional defects can be created by the high electric field or by the current flowing through the insulator. The spatial distribution of these defects is, in principle, random, but the presence of a pre-existing defect can alter the local energy configuration, leading to a higher electric field and, therefore, to a larger defect creation probability. Once enough defects are created and link up in a complete conduction path, as shown in Fig. 81(c), a large current can flow through the oxide, leading to a loss in isolation and to the possible catastrophic failure of the oxide if the power dissipation is too high.

Since the defect creation process is field-assisted, operation of a device at a larger gate overdrive causes a faster degradation, as commonly observed; in reliability tests, a  $\beta$  parameter of the Weibull distribution larger than 1 may be extrapolated, consistently with a degradation related to intrinsic causes.<sup>567,568</sup> Before catastrophic failure occurs, detected effects on the device performance include increase in the gate leakage current due to the creation and destruction of the metastable conduction paths (see Fig. 82)<sup>569</sup> and the increase in gate leakage absolute value,<sup>570</sup> but the effects on the device performance in terms of threshold voltage and drain current are minor.<sup>570</sup> The possible presence of hole trapping in the oxide, originated by impact ionization under the high electric field, has also been speculated.<sup>568</sup>

The TDDB can affect not only lateral devices but also vertical ones, such as trench MOSFETs<sup>539,571</sup> and FinFETs.<sup>572</sup> The results quoted above demonstrate the possibility of using electroluminescence measurements to pinpoint the location of the failure spots in the device, and of limiting the current during the catastrophic failure to avoid extensive damage to the sample, leaving a failure analysis feasible on the detected spot. Additionally, a careful design of the insulator composition and bilayer structure can significantly improve robustness and lifetime.<sup>571</sup> In the case of trench transistors, numerical simulations show electric field crowding at the



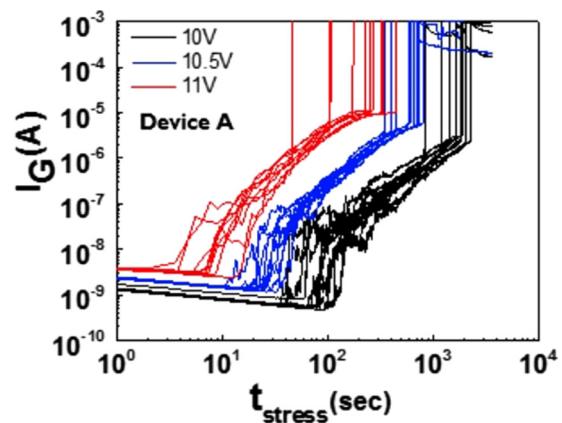
**FIG. 81.** Sketch of time-dependent dielectric breakdown caused by defect percolation. Reproduced with permission from Degraeve *et al.*, *Microelectron. Reliab.* **39**, 1445–1460 (1999). Copyright 1999 Elsevier.

trench edges,<sup>339</sup> whereas in the FinFETs, it is located at the corner of the dielectric, at the foot of the fin<sup>572</sup> (Fig. 83).

## 2. Degradation of p-GaN gate stacks

In order to achieve a normally OFF operation, the most common approach is to use a p-GaN gate layer, as discussed in Secs. V B 4. Under the strong gate overdrive of typical operating conditions and with the channel formed, a large voltage drop and electric field are present in the thin p-GaN layer (especially in the presence of a Schottky metal/p-GaN contact), leading to possible reliability issues.<sup>573–575</sup>

When a stress below the catastrophic failure is applied, a time-dependent degradation process might still be present, leading to sudden jumps and a larger noise in the gate current level.<sup>576</sup> The jumps are associated with the appearance of additional electroluminescence spots at the gate edge, suggesting that conductive paths are created in the gate stack due to a defect generation and percolation process, similar to what was found in the case of dielectrics in Sec. VIII A 1.<sup>577</sup> Early reports suggested that the traps are created due to impact ionization of electrons injected from the channel into the p-GaN region and accelerated by the high electric field.<sup>578</sup> This idea still needs to be supported by spectral electroluminescence measurements; so far, no band-to-band recombination and only bremsstrahlung and yellow luminescence,<sup>577</sup> or other sub-

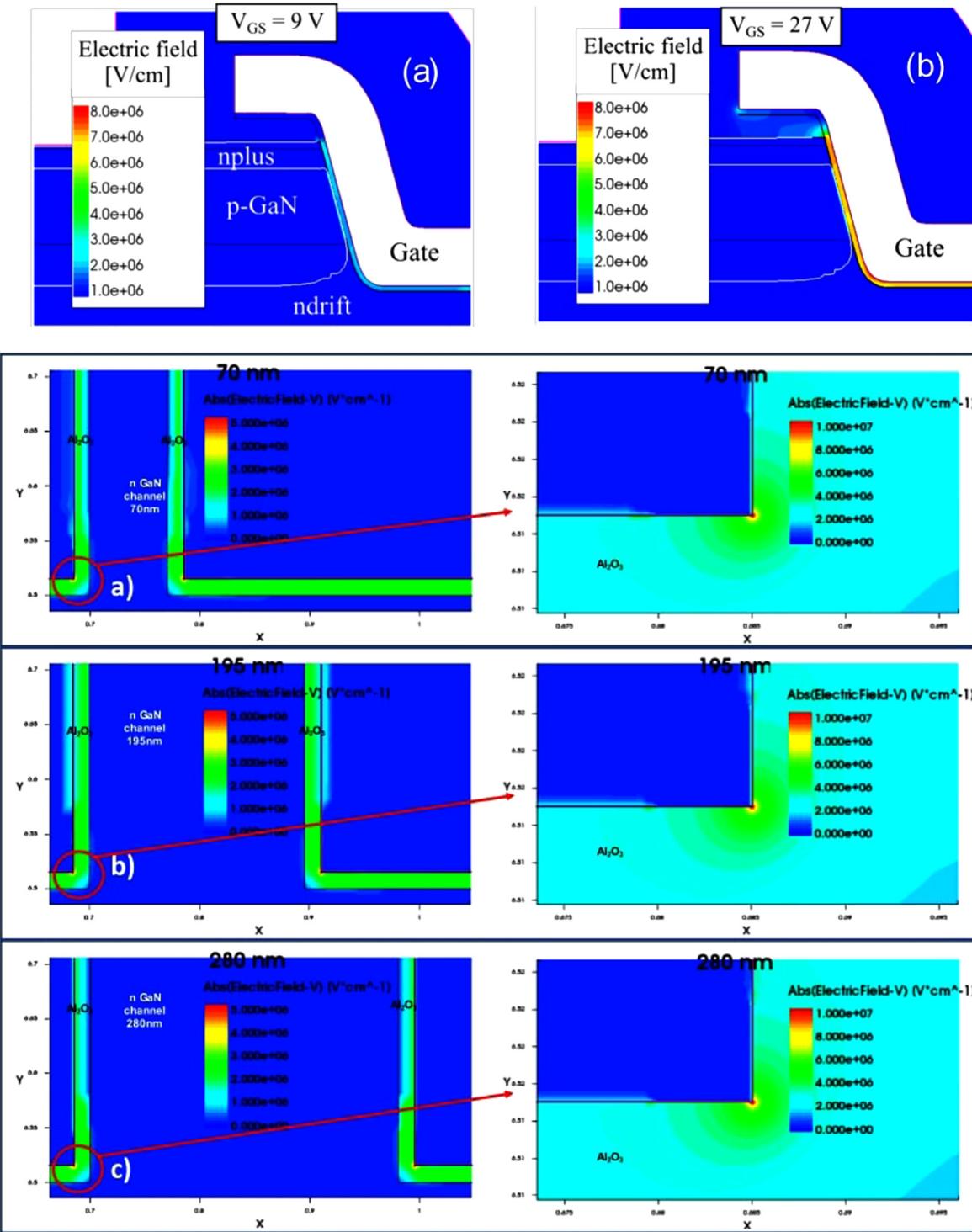


**FIG. 82.** Increase in gate leakage and metastable behavior caused by on-state stress in a MIS-HEMT. Reproduced with permission from Wu *et al.*, 2015 IEEE International Reliability Physics Symposium (IEEE, 2015), pp. 6C.4.1–6C.4.6. Copyright 2015 IEEE.

bandgap wavelengths have been detected.<sup>579</sup> Tallarico *et al.*<sup>580</sup> investigated HEMTs with a p-type gate, with a Schottky metal/p-GaN junction: they showed that during stress, a large voltage drop falls on the depleted region of the p-GaN, and this contributes to the percolation process.

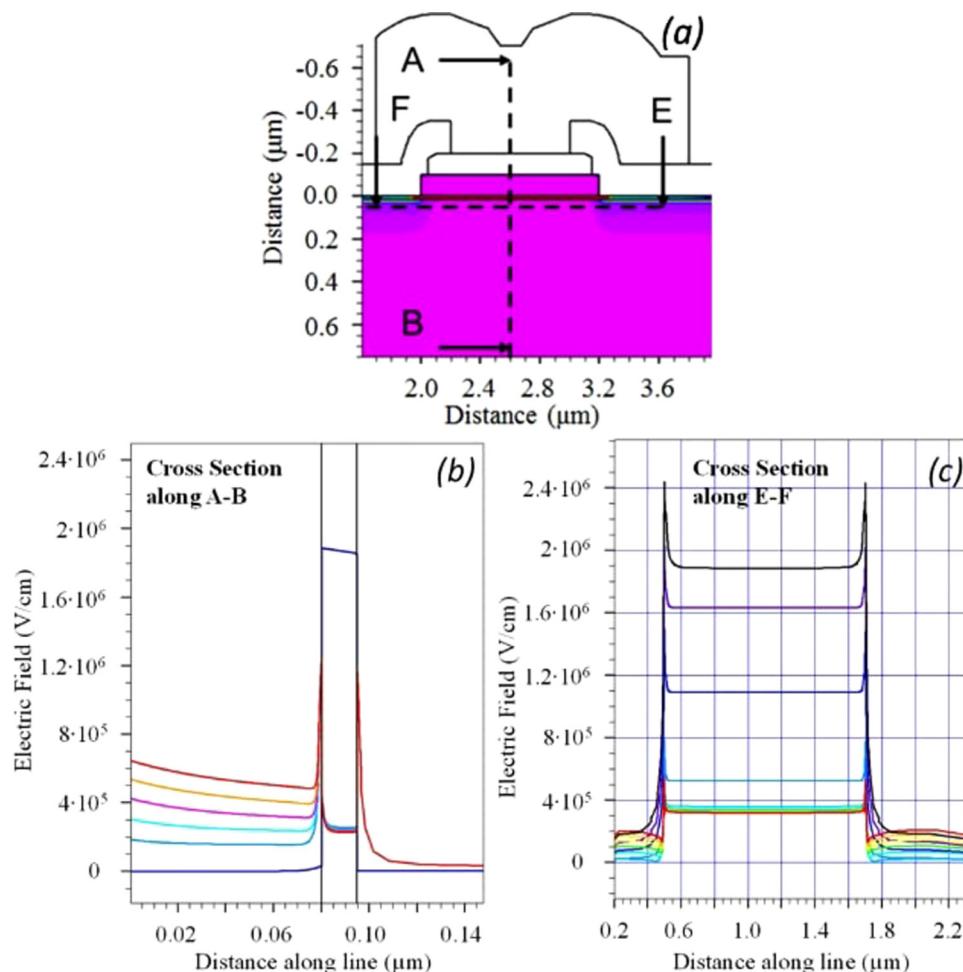
An additional similarity with the dielectric degradation is the exponential dependence of the time-to-failure on the stress voltage, which is also found to be Weibull distributed. The shape parameter  $\beta$  has been reported to be lower than 1, suggesting an extrinsic breakdown mechanism,<sup>577,581</sup> and greater than 1, as in recent reports.<sup>579,582</sup> The degradation should happen at the edge of the gate, as suggested by the aforementioned EL measurements and by tests of devices with different gate widths and gate lengths.<sup>583</sup> This is supported by results of numerical simulations (Fig. 84), showing that the electric field value is maximum at the edge of the p-GaN and lower in the center of the p-GaN.<sup>577</sup> Stoffels *et al.* suggested that under constant voltage stress, the pin diode formed by the p-GaN/AlGaN/GaN stack is positively biased. A current flows over the barrier, thus promoting a current-dependent degradation and the formation of percolation paths.<sup>584</sup> The properties of the percolation path depend on process conditions; an improvement in lifetime can be obtained by modifying the barrier growth conditions (e.g., by increasing the Al mole fraction from 20% to 25% as in Ref. 584).

Even though the degradation is found to be faster at higher temperature,<sup>583</sup> a different behavior can be seen in case of more complex degradation processes.<sup>585–587</sup> In Ref. 585, the degradation is supposed to be enhanced by the accumulation of positive charges at the p-GaN/AlGaN interface, which promotes the injection of electrons from the channel into the p-GaN, with consequent degradation. Higher temperature leads to more hole release, therefore improving the reliability. The presence of the hole trapping is confirmed by the fact that the gate current decreases during stress, due to the electrostatic repulsion between the injected and trapped



19 January 2025 21:33:19

FIG. 83. Numerical simulations of the electric field in (top) trench MOSFETs and (bottom) FinFETs. Reproduced with permission from Mukherjee *et al.*, Materials 13(21), 4740 (2020). Copyright 2020 by the authors of the cited paper, licensed under CC BY 4.0. Reproduced with permission from Ruzzarin *et al.*, Microelectron. Reliab. 88–90, 620–626 (2018). Copyright 2018 Elsevier.



**FIG. 84.** Numerical simulations of the electric field distribution in the p-GaN and AlGaN barrier during high gate bias stress. Reproduced with permission from Rossetto *et al.*, IEEE Trans. Electron Devices **63**(6), 2334–2339 (2016). Copyright 2016 IEEE.

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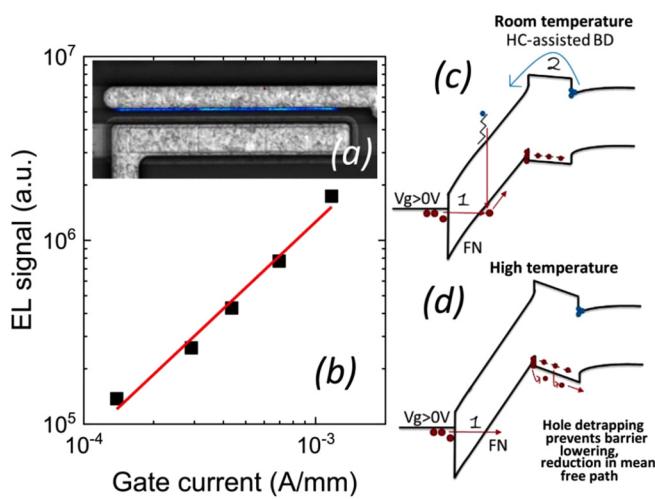
holes. This degradation process is sketched in Fig. 85, which also shows the electroluminescence distribution and the correlation between the electroluminescence intensity and the gate current. It is worth mentioning that carrier acceleration and impact ionization are also less prominent at high temperatures, due to the increased scattering, and this can also contribute to the positive temperature coefficient.

### 3. Vertical devices

Some results on the degradation of vertical devices were already discussed in Sec. VIII A 1, since they were related to dielectric degradation, but other processes are exclusive to vertical structures and will be discussed in this section.

In the case of vertical p-n<sup>-</sup>-n diodes and vertical junction field-effect transistors, most of the failures in common reliability tests (HTRB, HTOL, THB, and TC) are related to the substrate quality, the substrate miscut angle, and the morphology of the surface after the epitaxial growth.

More detailed studies on pn vertical diodes show that forward bias stress induces an increase in series resistance, in turn-on voltage, and in forward and reverse leakage current, as well as a reduction in the optical power emitted by diode due to band-to-band recombination in forward bias.<sup>588</sup> The variation in series resistance and optical power are well correlated, and their variation has a square root dependence on time, as shown in Fig. 86. All the experimental results can be explained according to the following model. During stress, the flow of carriers, aided by the temperature, can break the residual Mg-H bonds that are still present after the Mg activation phase done during growth. Hydrogen interstitials can then diffuse following the concentration gradient toward the n-type material. The diffusing hydrogen can passivate Mg atoms closer to the p-n interface, decreasing the hole concentration. This causes an increase in the turn-on voltage and the reduction in the amount of holes available for radiative recombination. The dependence on the square root of stress time is a common signature of diffusion-related degradation, being originated from the solution of Fick's second law of diffusion in one dimension.<sup>589</sup>



**FIG. 85.** (a) Spatial distribution of the electroluminescence and (b) its correlation with the gate current. (c) and (d) Sketch of the degradation process leading to a higher robustness at high temperature in p-GaN gate devices. Reproduced with permission from Masin *et al.*, Appl. Phys. Lett. **115**, 052103 (2019). Copyright 2019 AIP Publishing LLC.

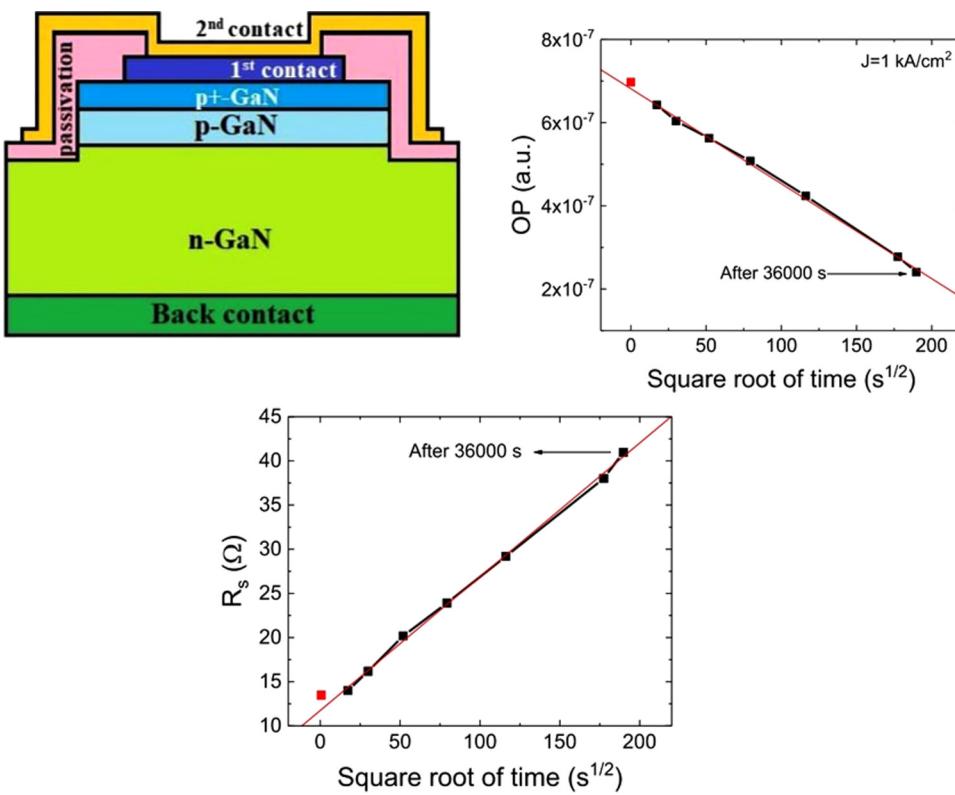
#### 4. RF stress

Operation in radio frequency (RF) conditions is not relevant for power devices but only for amplifiers, but a useful conclusion can be drawn by the analysis of the difference in degradation between DC and RF conditions.

In the case of RF devices, a common cause for degradation is the presence of hot electrons in near pinch-off conditions, especially when short channel effects and poor carrier confinement play a role due to the reduced gate length. Since the process is influenced by the source-drain leakage, a correct compensation of the buffer conductivity can significantly improve the reliability of the devices, with Fe and C co-doping leading to the best results.<sup>590</sup> The degradation mechanism is field-driven, as suggested by tests on devices with and without field plates.<sup>591</sup> A RF stress usually induces small variations in the DC performance of state-of-the art devices, mainly a lowering of the saturation current and a decrease in gate leakage,<sup>592</sup> but the generation of defects causes an increase in the dynamic current collapse.<sup>593</sup> A negative<sup>597</sup> or positive<sup>594</sup> shift in threshold voltage is also observed sometimes due to the presence of traps in the cap and barrier layer.<sup>595</sup>

The important conclusion comes from the comparison between devices stressed in DC and RF conditions, showing different degradation modes and a stronger degradation in the RF

19 January 2025 21:33:19



**FIG. 86.** (Top) Schematic cross section of the vertical GaN pn diode. (Bottom) Dependence of the increase in the series resistance and of the decrease in electroluminescence intensity on the square root of stress time. Reproduced with permission from Fabris *et al.*, Microelectron. Reliab. **88–90**, 568–571. Copyright 2018 Elsevier.

case.<sup>597</sup> This suggests that, even for power devices, it may be important to test the degradation not only in the ON-state, the OFF-state, and the SEMI-ON-state separately but also in the real switching pattern, to take into account the interplay between the different mechanisms and time dependence occurring in the various bias points of the switching locus.<sup>595</sup>

## B. OFF-state

The OFF-state bias condition can be highly stressful for a power device due to the high electric field present, on average, in the blocking region and peaking in critical device regions, such as the sharp corners and the gate edge. The electric field can cause damage to materials that are part of the device without being the semiconductor itself, such as the insulators for passivation and gate isolation. Other processes may involve the breakdown of GaN itself. In addition, interaction with the external atmosphere may promote field-assisted chemical reactions. In some cases, the high electric field can also be present together with a high current density, such as during avalanche conduction. In the following, we will discuss all these possibilities.

### 1. Extrinsic degradation: The role of dielectrics

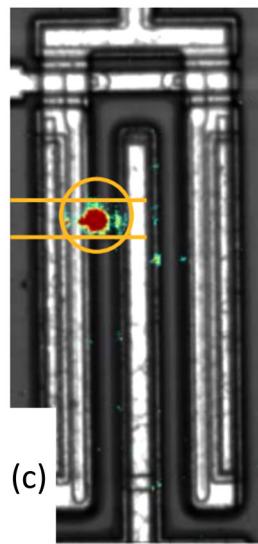
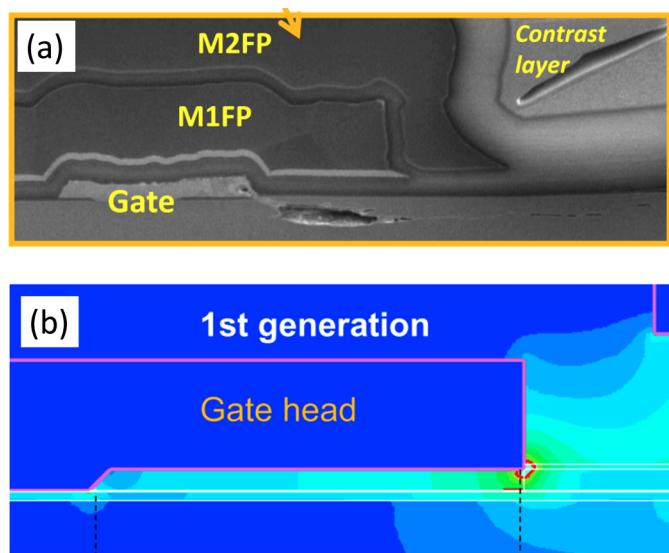
As discussed in Sec. VIII A 1, degradation of the dielectrics is usually present in ON-state stress conditions, since the voltage drop across the gate insulator is the highest, whereas in OFF-state stress, the large voltage drop in the depleted semiconductor mitigates the electric field across the gate stack. Therefore, some of the results already presented in Sec. VIII A 1 still hold, even when a larger bias is applied: the better reliability of engineered bilayer insulators,<sup>339,571</sup> the location of weak spots corresponding to electric field peaks,<sup>572</sup> and the negative<sup>566</sup> or positive<sup>596</sup> threshold voltage shift related to defect generation, which may also cause worse dynamic performance.<sup>566</sup>

Nevertheless, additional dielectrics are present in the complex structure of the state-of-the-art GaN power devices, such as the ones used for passivation and isolation of the field plates. Their degradation results in an increase in gate leakage level and noise, eventually leading to catastrophic failure even significantly below the breakdown voltage of the device; dielectric degradation is typically characterized by an exponential dependence of the average time to failure on the stress voltage.<sup>597</sup> In this case, the shape parameter  $\beta$  of the Weibull distribution is lower than 1, suggesting that reliability is limited by extrinsic factors. A possible origin for this experimental behavior is the degradation of the silicon nitride used for the passivation and field plate isolation. As can be seen through numerical simulations [Fig. 87(a)], in the case described in Ref. 597, in OFF-state conditions, the peak of the electric field is located in the silicon nitride, in proximity of the edge of the gate overhang on the drain side, and the value is  $\sim 6$  MV/cm, comparable with the theoretical breakdown electric field ( $\sim 6$  MV/cm).<sup>597</sup> The electric field in the AlGaN barrier is lower than 3 MV/cm; therefore, degradation in this layer is unlikely. This hypothesis can be confirmed by locating the failure spot by means of electroluminescence measurements [Fig. 87(c)] and performing cross-sectional transmission electron microscope (TEM) failure analysis on it.<sup>150</sup> As can be seen in Fig. 87(b), the damaged region starts at the edge of the gate region and extends into the channel region.

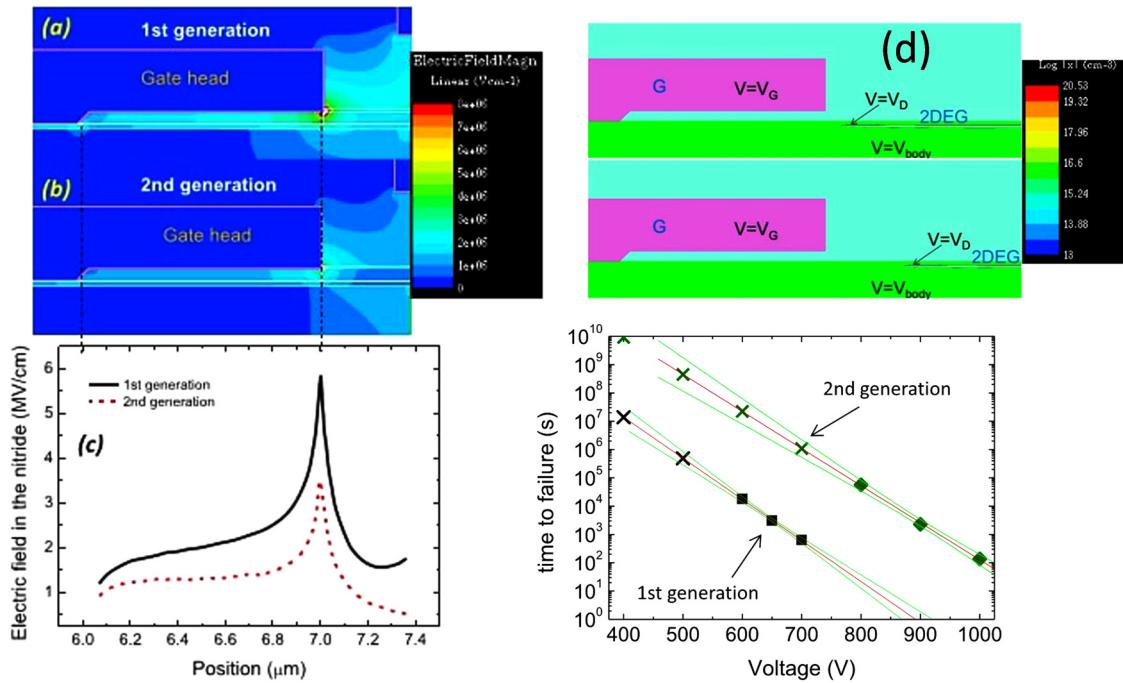
The mechanism can be further confirmed and solved by changing the vertical conductivity in the epilayer, leading to a different grounding of the floating buffer and, therefore, to a larger 2DEG retraction in the case of the improved devices, as shown in the numerical simulations in Fig. 88(d).<sup>597</sup> This leads to a significantly lower electric field in the silicon nitride for the second generation of devices [Figs. 88(a)–88(c)] and to an improvement in the time-to-failure of more than three orders of magnitude, as shown in Fig. 88(e).

A second possible solution is to change the length of the gate head at the drain side, limiting the peak electric field, or to add an extra SiN layer under the gate head.<sup>150,598</sup>

19 January 2025 21:33:19



**FIG. 87.** (a) TEM cross section analysis is able to identify the degradation caused by (b) the peak in electric field at the edge of the gate head (as obtained by numerical simulations), located by means of (c) electroluminescence measurements. Reproduced with permission from Meneghini *et al.*, IEEE Trans. Electron Devices **62**(8), 2549–2554 (2015). Copyright 2015 IEEE. Reproduced with permission from Rossetto *et al.*, IEEE Trans. Electron Devices **64**(1), 73–77 (2017). Copyright 2016 IEEE.



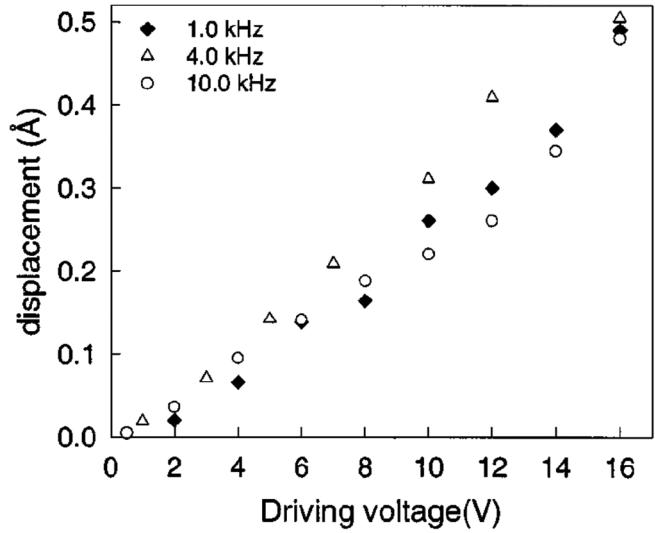
**FIG. 88.** (a)–(c) Improved devices with different grounding of the floating buffer have a lower electric field due to (d) the larger 2DEG retraction. (e) This change leads to an increase in time-to-failure by more than three orders of magnitude. Reproduced with permission from Meneghini et al., IEEE Trans. Electron Devices **62**(8), 2549–2554 (2015). Copyright 2015 IEEE.

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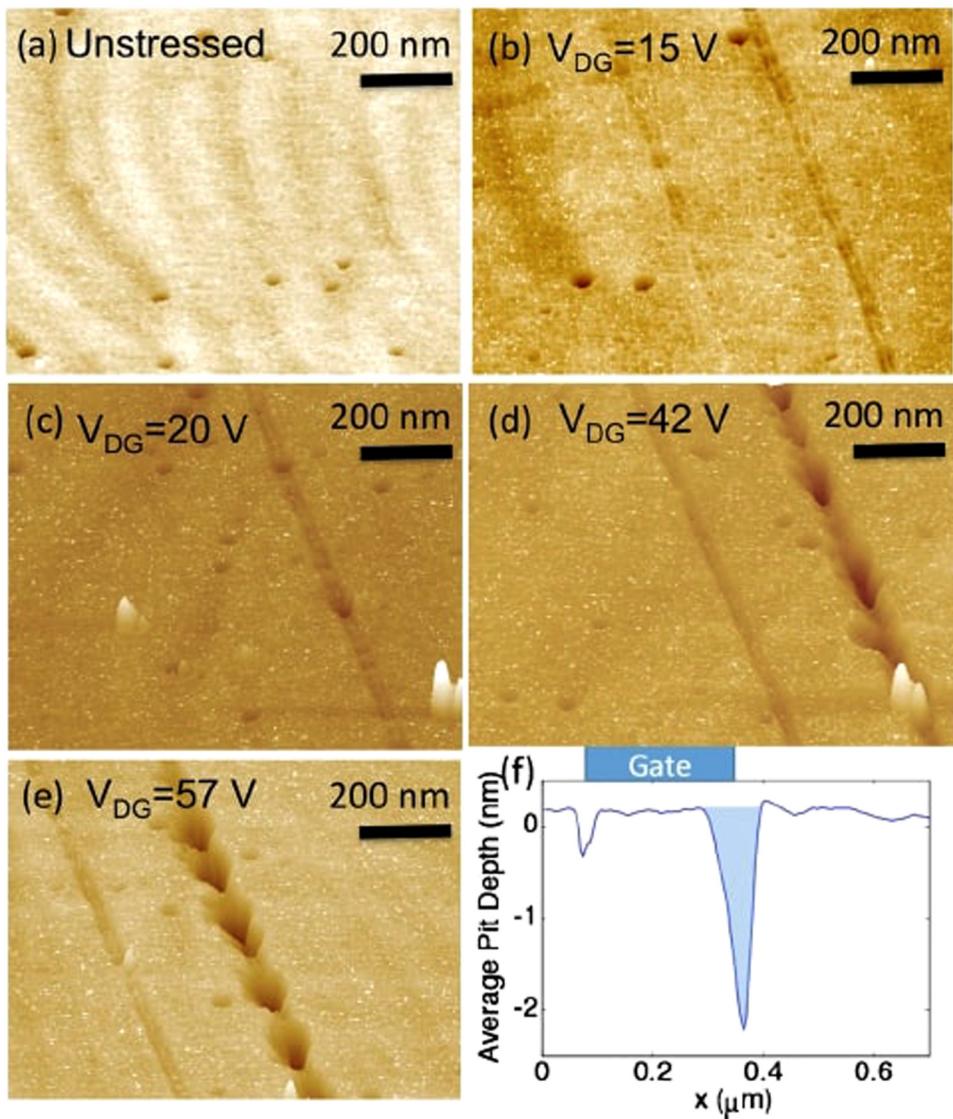
## 2. Degradation of GaN stacks

a. *Converse piezoelectric effect.* As discussed in Sec. III, GaN is a polar material. Any polar material, when submitted to a compressive or tensile mechanical stress, builds a potential across itself, and this behavior is called the direct piezoelectric effect. In polar materials, the opposite is also true. An external voltage applied in the direction of the polarization vector may cause an expansion or a contraction of the material: this is called the converse (or inverse) piezoelectric effect.

This behavior is not only theoretical but can be experimentally measured by means of interferometric techniques on GaN crystals.<sup>599</sup> The amount of displacement caused by different voltages applied to a 2.5 μm thick single crystal [0001] GaN film is shown in Fig. 89, corresponding to a displacement of 0.05 nm at an electric field of 64 000 V/cm, i.e., to a displacement of 1.56 nm at an electric field of 2 MV/cm. The electric field peak found close to the gate edge at the drain side in common HEMT devices is close or can even exceed this value, even in the presence of multiple field plates, in common high power operation. Therefore, one may wonder if this level of displacement (without considering the different value of the piezoelectric coefficients between the reported GaN film and the AlGaN of the barrier) can cause damage to the device and limit its reliability. Of course, a localized electric field



**FIG. 89.** GaN displacement measured at various applied voltages. Reproduced with permission from Guy et al., Appl. Phys. Lett. **75**, 4133–4135 (1999). Copyright 1999 AIP Publishing LLC.



**FIG. 90.** Formation of grooves and pits in devices stressed at increasing drain-gate voltage. Reproduced with permission from Makaram *et al.*, Appl. Phys. Lett. **96**, 233509 (2010). Copyright 2010 AIP Publishing LLC.<sup>606</sup>

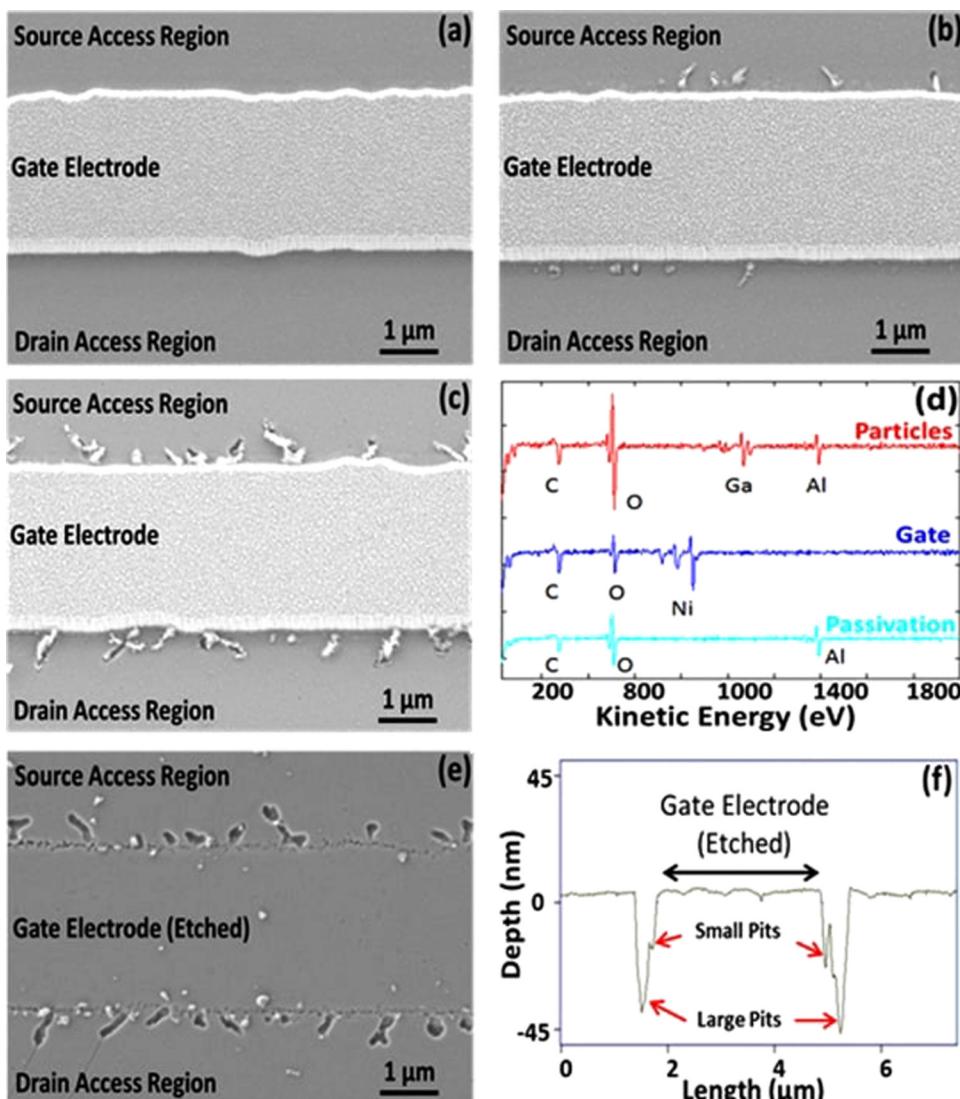
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would not be enough to produce a displacement, since the lattice would build up strain to accommodate for the expected local displacement, but the levels of piezoelectric stress originated by the expected variation can be very high, in the order of hundreds of MPa.<sup>600,601</sup>

This idea was proposed for the first time in 2006,<sup>602</sup> and much work has been done to identify this mechanism in the following years. Specific tests have found the presence of a critical gate or drain voltage for the degradation, consistent with the buildup of a critical amount of strain in the structure before relaxation and formation of defects takes place.<sup>602</sup> When stressed above the critical voltage, an increase in charge trapping inside the AlGaN barrier takes place, consistently with the generation of defects in that region, whereas the trapping in the buffer remains unaffected.<sup>603</sup> By means of stresses at different gate voltages and

current levels, it was possible to exclude any effect of the hot electrons in the process, since the stress current was found to have no impact on the critical voltage value.<sup>604</sup> The generation of cracks only at the drain side of the gate taking place above the critical voltage, without any impact in the degradation of temperature or hot electrons, was reported by TEM measurements.<sup>605</sup>

The generation of indentations, pits, and grooves at the drain side of the gate edge was confirmed also by atomic force microscope (AFM) and scanning electron microscope (SEM) testing of stressed devices after chemical etching of the gate metal, as shown in Fig. 90. At least some of the new pits form without the presence of any pre-existing defects, consistently with the inverse piezoelectric effect. The defects act as gate leakage paths, may reduce the maximum drain current, and favor the charge trapping in the device.



**FIG. 91.** (a)–(c) Top view SEM images of an HEMT stressed at reverse gate bias for increasing periods of time. The chemical composition of the stringers is shown in (d), and (e) shows the pits that form below them. (f) shows an AFM profile of a representative source to drain region. Reproduced with permission from Gao *et al.*, Appl. Phys. Lett. **99**, 223506 (2011). Copyright 2011 AIP Publishing LLC.

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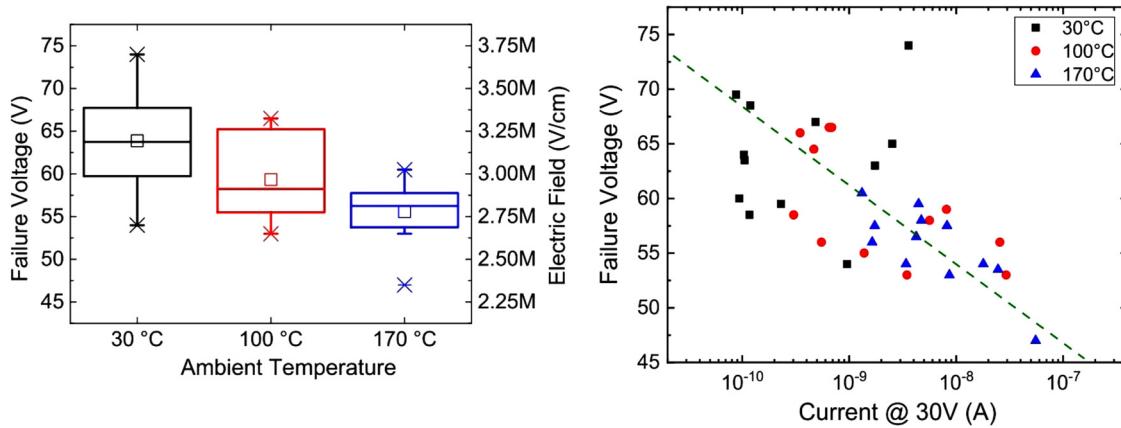
*b. Electrochemical degradation.* The formation of localized damage at the edge of the gate can be visible even below the critical voltage, due to other processes involving chemical reactions.

When devices are stressed in reverse gate bias conditions, particles and stringers appear along the gate edge, both at the source and the drain sides, as shown in Figs. 91(a)–91(c).<sup>607</sup> Their chemical composition can be determined by Auger electron spectroscopy (AES), reported in Fig. 91(d), highlighting an oxygen-rich composition and the presence of gallium. The quantitative analysis is compatible with the formation of  $\text{Ga}_2\text{O}_3$  and  $\text{Al}_2\text{O}_3$ . After metal removal, the presence of large pits below each oxide particle is clearly visible [Fig. 91(e)]. By changing the polarity of the stress bias on the gate-source and gate-drain diodes, it is possible to demonstrate that the oxide forms where the electric field is the

highest. By testing devices in vacuum, it was possible to demonstrate that the oxide only forms when oxygen is present in the atmosphere, and it is supposed that oxygen diffuses through the passivation layer and locally oxidizes the  $\text{AlGaN}/\text{GaN}$  layers.

Similar effects can be produced by reaction with hydroxyl groups ( $\text{OH}^-$ ) or water.<sup>608</sup> In this case, the degradation happens due to anodic oxidation of the  $\text{AlGaN}$  layer in the electrochemical cell composed of the gate metal, the passivation layer, and the barrier, aided by water and by the presence of holes. The main effects are degradation in drain current and dynamic performance, whereas in this case, the increase in gate leakage is not caused by the presence of the pits.

It is also suggested that an exclusion zone can appear around the pits, where no additional degradation spots can be formed, as a



**FIG. 92.** Dependence on temperature of the failure voltage of AlN/Si layers and its correlation with the leakage level. Reproduced with permission from Tajalli et al., *Micromachines* 11(1), 101 (2020). Copyright 2020 by the authors of the cited paper, licensed under CC BY 4.0.<sup>615</sup>

result of the consumption of mobile species in the electrochemical reaction.<sup>609</sup>

*c. Time-dependent breakdown of GaN epitaxial stacks.* The results presented in Sec. VIII A 2 for the p-GaN degradation show trends comparable to the ones reported in Sec. VIII A 1 for the time-dependent dielectric breakdown degradation, namely, the Weibull distribution of the failure time and its exponential dependence on the stress voltage. One can then wonder if GaN itself, when deeply depleted, can behave as a dielectric and experience a TDDB-like degradation process. In general, detecting a TDDB process in a full GaN power device can be complex due to the large number of parts and materials it is composed of, each of them possibly contributing to the degradation as discussed in this Sec. VIII. Moreover, if a device is not fully vertical, both lateral and vertical electric fields are present, further complicating the analysis. Therefore, even though the presence of GaN TDDB was suggested in the past, no demonstration excluding other possible causes was provided.<sup>610,611</sup> For this reason, the first conclusive demonstration of time-dependent dielectric breakdown in the GaN itself was done on optoelectronic devices.<sup>612</sup> LEDs have an intrinsic vertical structure; no complex parts such as field plates, gate with various geometries, blocking dielectrics, or engineered passivation; and are already at a high technology readiness level, allowing for testing of stable and reliable devices with no reliability and behavioral issues, which is not the case for fully vertical power devices. The experimental tests, carried out in the reverse bias condition, confirm that GaN behaves as a leaky dielectric when deeply depleted, that the time-to-failure has an exponential dependence on the stress electric field, and that it is Weibull distributed.<sup>612</sup> The extrapolated shape parameter  $\beta$  is 4.43, confirming that the devices under test show an intrinsic failure behavior. Consistent results were obtained also on GaN-on-Si stacks used for the fabrication of GaN transistors. It was demonstrated that when submitted to drain-to-substrate (two terminal) stress, AlGaN/GaN transistors can show a time-dependent degradation, which is Weibull distributed, significantly field-dependent, and weakly thermally activated ( $E_a = 0.25$  eV).

Degradation was ascribed to a percolation process, leading to the generation of localized shunt paths between drain and substrate.<sup>613</sup>

*d. Buffer decomposition experiments.* When a lateral power device is biased in the off-state, a large voltage drop is present in all the layers from the drain to the substrate, which usually includes the AlN nucleation layer, an AlGaN buffer, and a carbon-doped GaN buffer. Understanding which of these layers has the strongest impact on the vertical breakdown voltage and on device reliability is a critical task for improving the final behavior. This can be done by testing separate structures, where the growth has been stopped after each of the single layers above the Si substrate, to form AlN/Si, AlGaN/AlN/Si, and C:GaN/AlGaN/AlN/Si stacks.<sup>614,615</sup> This way, the variation in reliability (and charge trapping) induced by each layer can be analyzed independently. In order to do this, a mandatory technical requirement is the processing of good ohmic contacts on top of each layer, a non-trivial task on low-conductivity, and wide-bandgap materials.

The analysis of AlN layers directly grown on a Si substrate indicated a breakdown field of 3.25 MV/cm, which is significantly lower than that of high-quality crystalline AlN. The difference is ascribed to the presence (and high density) of vertical leakage paths, involving V-pits and threading dislocations. This value further decreases with temperature (see Fig. 92).<sup>615</sup> To explain this temperature dependence, the failure voltage was plotted against the leakage current. Samples with higher leakage showed a lower breakdown voltage, and a lower breakdown field, of the AlN nucleation layers. The flow of current at localized defects may lead to premature breakdown. This argument was used to explain why the breakdown field of AlN grown on Si (3.25 MV/cm) is much lower than that of high-quality crystalline AlN (up to 12 MV/cm).

In addition, it was demonstrated that the AlN/Si structures show trapping of negative charge, which has been ascribed to the injection of electrons from the Si substrate toward deep traps located in the AlN. By adding an AlGaN layer on top of the AlN, it is possible to significantly reduce the density of defects, and this results in a more uniform sample-to-sample leakage current. A

**TABLE X.** Estimated impact ionization coefficients in GaN.<sup>617</sup>

	$\alpha$ (cm <sup>-1</sup> )	$\beta$ (cm <sup>-1</sup> )
Ji <i>et al.</i> <sup>618</sup>	$2.11 \times 10^9 \exp(-3.689 \times 10^7/E)$	$4.39 \times 10^6 \exp(-1.8 \times 10^7/E)$
Cao <i>et al.</i> <sup>619</sup>	$4.48 \times 10^8 \exp(-3.39 \times 10^7/E)$	$7.13 \times 10^6 \exp(-1.46 \times 10^7/E)$
Maeda <i>et al.</i> <sup>620</sup>	$2.69 \times 10^7 \exp(-2.27 \times 10^7/E)$	$4.32 \times 10^6 \exp(-1.31 \times 10^7/E)$

strong increase in the breakdown voltage can be reached by adding a C:GaN layer on top of the stack. In this case, the structures analyzed in Ref. 615 showed breakdown voltages larger than 800 V. It is worth noticing that the presence of a C:GaN layer can result in positive charge trapping. This is ascribed to the presence of holes from C:GaN, which are trapped at the GaN/AlGaN interface, leading to the storage of positive charge in the buffer.

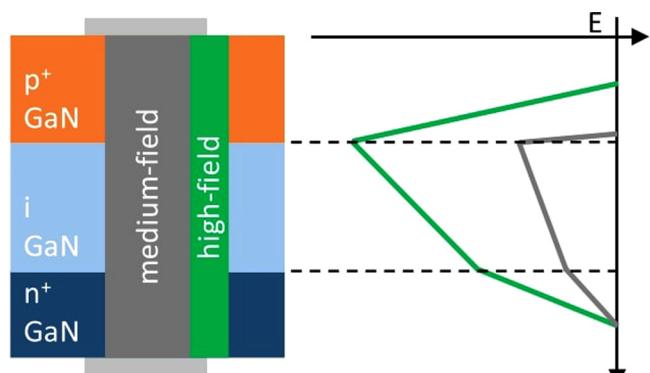
In the case of the AlN/Si stacks under analysis, the leakage current originates, as confirmed by numerical simulations, from the series connection of equivalent AlN/n<sup>+</sup>-Si and n<sup>+</sup>-Si/p-Si junctions, due to the presence of an inversion layer at the interface.<sup>616</sup> The limiting factors are the p-doping level of the Si substrate and the electric field at the interface, since both of them control the tunneling injection from the Si substrate into the AlN layer.

*e. Avalanche operation and walkout (in vertical devices).* As already mentioned for AlN in Sec. VIII B 2 d, in general, the breakdown of (Al)GaN-on-Si is not ascribed to avalanche, but to the presence of large densities of defects: vertical GaN-on-GaN devices (having significantly lower dislocation densities compared to GaN-on-Si) can withstand higher electric fields and reach the avalanche regime. The impact ionization coefficients for GaN have been recently estimated, as summarized in Table X.<sup>617</sup>

Avalanche operation is not an unwanted side-effect but a desired feature, especially in power diodes, since it allows them to withstand surge events.

However, one needs to consider that if the structure is not optimized, operation in the avalanche mode may be detrimental for the reliability of the devices due to the high electric field and to the presence of a large number of highly energetic carriers. The former can cause failure due to non-optimal termination and electric field peak at the bevel surface,<sup>621</sup> whereas the latter can create significant lattice damage.

The actual defect species responding during the avalanche operation is not yet clear, but a possible hypothesis is that carbon in nitrogen substitutional position (C<sub>N</sub>) may be involved. These defects create a wide range of effects, including an increase in series resistance and leakage current, a variation in the turn-on voltage, an increase in the avalanche breakdown voltage (avalanche walkout<sup>622</sup>), and a worsening of the dynamic performance. The analysis is made more complex by the large variations in the vertical electric field in the lateral direction, as summarized in Fig. 93. In the high-field region, the avalanche condition and the high current conduction cause damage creation and trapping of a part of the flowing charges, whereas in the medium field region, no avalanche is present, and



#### Stress phase, high reverse bias:

- high-field region: current-driven carrier trapping
- medium-field region: (field-assisted) de-trapping

#### Measure phase, lower bias:

- high-field region: effect of trapped carriers, dominates in avalanche bias (higher field)
- medium-field region: effect of de-trapping, dominates in forward bias (wider area)

**FIG. 93.** Summary of the possible effects taking place in a vertical GaN power diode during stress in avalanche conduction. Reproduced with permission from De Santi *et al.*, IEEE Electron Device Lett. **41**(9), 1300–1303 (2020). Copyright 2020 IEEE.<sup>227</sup>

19 January 2025 21:33:19

only a negligible amount of current is flowing; therefore, the main effect is field-assisted de-trapping of native charge. When the device is moved to measure the bias condition, the trapped carriers cause the increase in the avalanche breakdown voltage, the de-trapped ones modify the turn-on voltage, and the lattice damage impacts on the leakage current and the series resistance.<sup>626</sup>

## C. SEMI-ON-state

In real operating conditions, a power switch is not limited only to ON-state and OFF-state bias points. During the turn-on and turn-off transitions, the presence of the internal and parasitic capacitances prevents an instantaneous variation of the voltage at the terminals of the device; therefore, a relatively high voltage at the drain can still be present when the gate voltage is already close to the threshold value. This bias condition is called SEMI-ON-state, because the conductive channel is partially formed. Depending on the residual drain voltage during the transition, in the SEMI-ON-state state, a relatively large amount of electrons in the channel can be accelerated by a large electric field, causing the flow of highly energetic (hot) carriers in the device that can be detrimental for its reliability.

The main effects a SEMI-ON-state stress can cause on a transistor include worsening of the isolation properties of the gate diode, threshold voltage shifts, increase in ON-resistance, decrease in transconductance peak value, change in peak electric field, knee walkout, and increase in drain-lag transient amplitude.<sup>623,624</sup> These

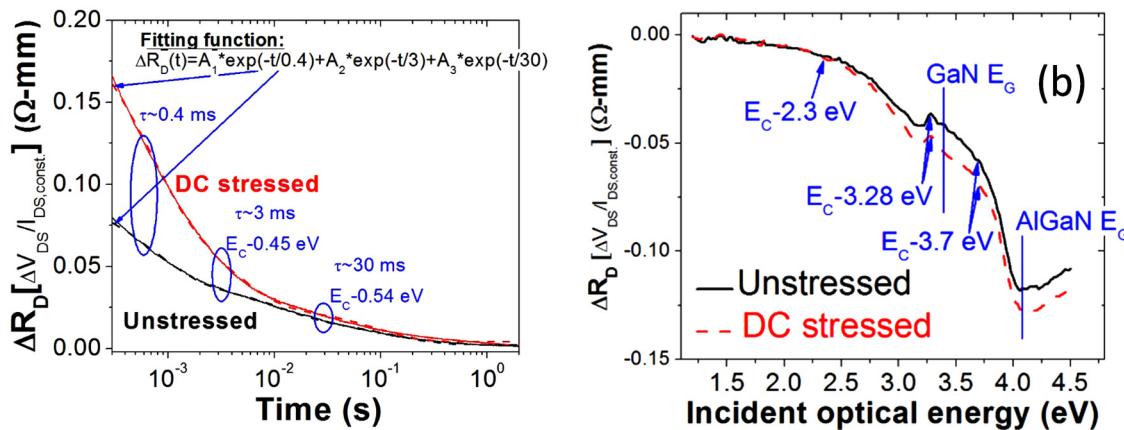


FIG. 94. (a) Increase in amplitude of the drain-lag transient caused by SEMI-ON-stress and (b) corresponding increase in defect density detected by  $\text{Cl}_D$ -DLOS. Reproduced with permission from Sasikumar *et al.*, 2012 IEEE International Reliability Physics Symposium (IRPS) (IEEE, 2012), pp. 2C.3.1–2C.3.6. Copyright 2012 IEEE.

changes may be ascribed to the increase in defect concentration close to the channel region, shown in Fig. 94, caused by the energy exchange between the hot electrons and the crystal lattice, as can be detected by several deep-level characterization techniques applied during stress.<sup>624</sup> The specific microscopic configuration of the deep level causing the detected variations can change depending on the device growth conditions, structure, and processing. Recent papers investigated the effect of hot electrons on the dynamic ON-resistance of AlGaN/GaN high-electron mobility transistors subject to SEMI-ON stress. The additional dynamic  $R_{ON}$  detected in the SEMI-ON-state was ascribed to hot-electron trapping at the passivation/AlGaN interface.<sup>625</sup>

Specific circuits<sup>453,626–628</sup> can be used to test the degradation of GaN HEMTs induced by hot electrons. A promising approach was proposed in Refs. 628 and 629 based on the use of switching

setups capable of monitoring on-wafer the effects of SEMI-ON stress. By tuning the capacitance at the drain node, it is possible to control the amount of energy/charge released during hard-switching events and to evaluate the effect of stress on the devices. The comparison of results obtained via different techniques<sup>537</sup> indicated that hot-electron trapping is a very fast process that takes place in few nanoseconds. The developed methodologies allowed us to assess the trajectory of the switching locus, the power dissipated during the turn-on transitions, and the dynamic ON-resistance of the devices (see an example in Fig. 95). The kinetics of hot-electron trapping were modeled analytically in a recent publication, based on rate equations.<sup>630</sup>

In the specific case of gate injection transistors (GITs), a destructive positive feedback loop initiated by the hot electrons created during SEMI-ON stress can lead to a rapid increase in the

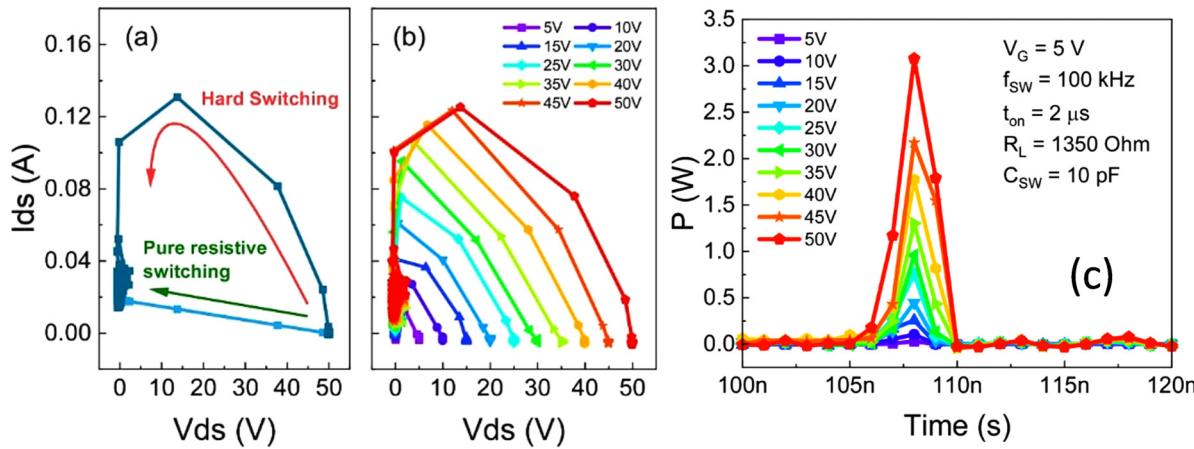
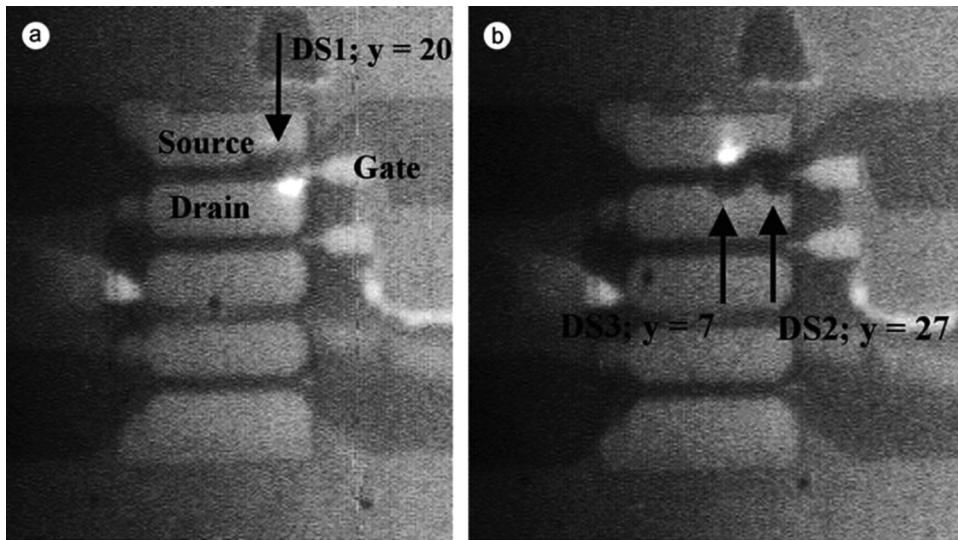


FIG. 95. Switching locus curve (a) comparing purely resistive switching and hard switching and (b) applying different stress voltages ( $V_{DD}$ ). The trajectory confirms the hard switching condition during the turn-on transition. (c) Power dissipated during the turn-on transition. The power peak increases with increasing the stress voltage  $V_{DD}$ . Reproduced with permission From Modolo *et al.*, J. Semicond. Sci. Technol. 36(1), 014001 (2020). Copyright 2020 IOP Publishing. All rights reserved.<sup>537</sup>



**FIG. 96.** Backside infrared camera measurements, showing the appearance of dark spots on the contact [source in part (a), drain in part (b)] grounded during the ESD event. Reproduced with permission from Kuzník et al., Solid State Electron. 48(2), 271–276 (2004). Copyright 2004 Elsevier.<sup>632</sup>

electric field at the drain side and to the failure of the device.<sup>595,631</sup> This issue can be solved by using hybrid drain gate injection transistors (HD-GITs) device configuration, since the hole injection from the p-GaN at the drain partially reduces the amount of trapped charge caused by the hot electrons and the electric field peak.<sup>595</sup>

#### D. Electrostatic discharges and electrical overstress

Dangerous bias points for the reliability of a device can originate not only from the expected behavior during operation but also from external unwanted stimuli. A frequent example is the application of short voltage or current pulses to one of the terminals, nanoseconds to seconds long, as a consequence of the interaction with users, the ambient conditions, or machinery during fabrication, assembly, and handling. Collectively, these phenomena are called electrostatic discharges (ESD) and electrical overstress (EOS).

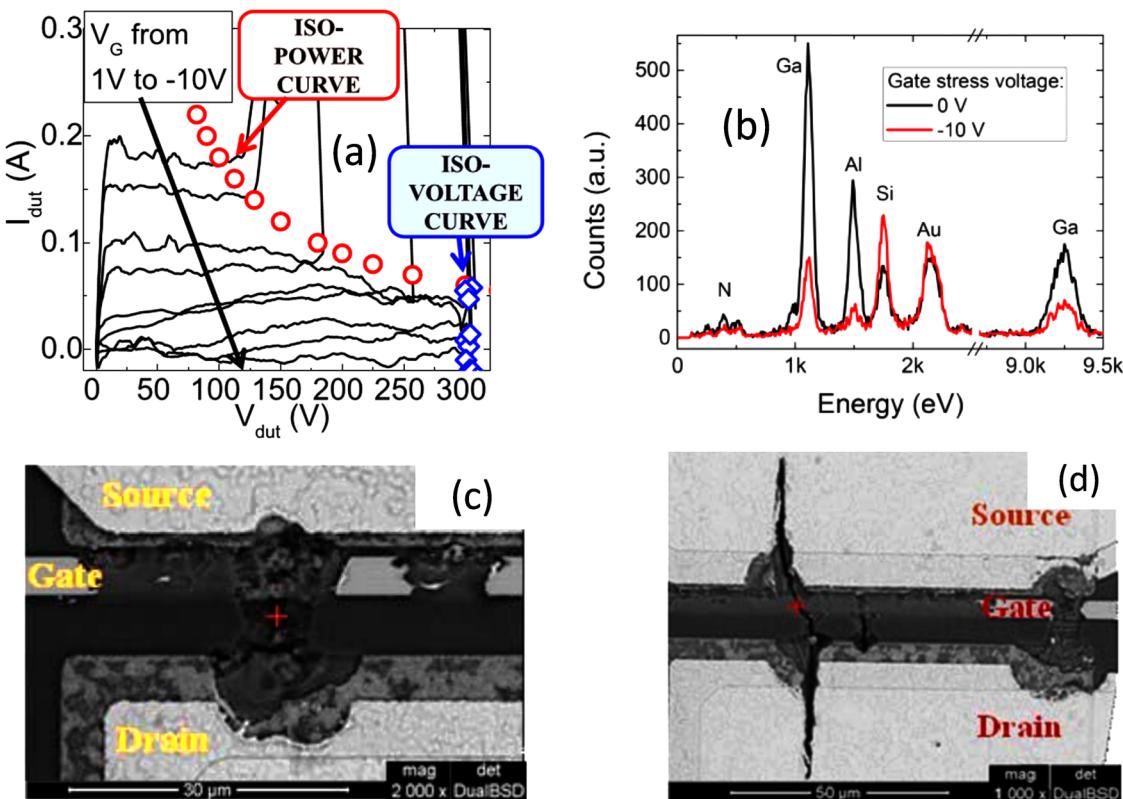
Under such high power dissipation conditions, several parts of the device can show degradation. One of them is the ohmic contacts at the source and the drain, as can be evaluated by tracking their specific resistance without any contribution by the channel resistance.<sup>632</sup> At increasing current stress levels in the floating gate condition, the values of the contact resistance can significantly increase, up to a factor of  $\approx 30$ . Backside infrared camera measurements, reported in Fig. 96, show the creation of dark spots, attributed to electromigration leading to current filamentation. The spots are always present on the grounded contact, suggesting that not only the high power dissipation but also the current flow or electric field direction plays a role in the degradation. In this case, no variation in material parameters, charge density, or electron mobility is observed.

In general, issues related to contacts can be solved by an improvement in device processing, leaving other parts as the causes of degradation and failure. The substrate is no exception, especially if semiconductors with worse breakdown fields, such as Si, are used in order to lower the cost and increase wafer size. This can easily

be evaluated by testing lateral Schottky diodes, since additional structures can be tested to gain more information, as will be described in the following.<sup>633</sup> Schottky diodes tested in the reverse conduction mode show no dependence of the failure voltage on diode length after a critical length, suggesting that the breakdown is not related to the lateral direction anymore. In order to investigate if the vertical electric field is causing the issue, specific buffer isolation structures can be fabricated, without and with Si substrate removal, composed of isolated ohmic contacts connected only through the substrate. The structures with Si substrate are found to fail at a significantly lower voltage, confirming that the vertical electric field and the Si breakdown field define the ESD robustness. If the ESD testing is carried out in the forward conduction mode, the limiting factor is the high local power dissipation.

In a state-of-the-art transistor, the list of the possible effects caused by an ESD/EOS event extends beyond contact and substrate damage, depending on device structure and test conditions.<sup>634</sup> In normally ON devices and gate-grounded testing configuration, the melting of the gate metal and the formation of cracks from source to drain can be observed. In the case of shorter events ( $<10$  ns), heating of the device is not high enough to lead to metal melting and catastrophic failure. Instead, several damaged regions can be found at the drain side of the gate edge, attributed to the converse piezoelectric effect caused by the high electric field during the event. Another possible failure mode is the breakdown of the parasitic diode between the gate finger and the drain and source contacts at the mesa edge.

If the gate reliability is not the main goal of the analysis, it is possible to test devices without the gate metal.<sup>634</sup> If a mesa-type isolation is not present, the migration of the contact metal from drain to source, leading to a drain-source short, is a relevant process, especially at the corners of the contacts, where the electric field is the highest. The process is started by the melting of the metal at the high power dissipation condition, which is expected to happen at temperatures  $1.5\times$  to  $4\times$  lower than the GaN one. If a



**FIG. 97.** (a) Failure caused by critical electric field and power dissipation in a device submitted to drain ESD discharges at various gate voltages. EDX measurements in (b) of the failed region in a device failed due to (c) power dissipation and (d) electric field confirm the driving force of the failure. Reproduced with permission from Rossetto *et al.*, IEEE Trans. Electron Devices **62**(9), 2830–2836 (2015). Copyright 2015 IEEE. De Santi *et al.*, IET Power. Electron. **11**(4), 668–674 (2018). Copyright 2017 The Institution of Engineering and Technology.

19 January 2025 21:33:19

mesa isolation is present, short-circuit instead forms along the channel due to the presence of surface states that act as low-energy paths for the metal migration.

One of the main shortcomings with ESD/EOS testing on transistors is the fact that a single pulse is applied to the device under test, whereas it was demonstrated that GaN-based devices suffer from cumulative effects.<sup>634</sup> Another problem is that the protocol is usually based only on gate-floating and gate-grounded configurations. Unfortunately, in the real application, the gate voltage will sweep the entire operating range, and there is no way to guarantee that the ESD event will happen only when the device is biased in one of the two tested configurations. For this reason, in a three-terminal device, it is important to analyze the dependence of the robustness on the applied gate voltage.<sup>635</sup>

As shown in Fig. 97(a), when the ESD event is applied in the OFF-state and the SEMI-ON-state, the catastrophic failure of the device always takes place at the same voltage on the device under test. This finding is consistent with a failure related to reaching the breakdown electric field of the material, which always happens at the same drain-source voltage regardless of the applied gate voltage. When the ESD event is applied in the ON-state,

detected robustness is lower, and the failure voltage and current points closely follow an iso-power curve. This behavior confirms that, in the ON-state, the reliability is limited by the power dissipation that the device can withstand. These assumptions are confirmed by the results of a scanning electron microscope (SEM) inspection [see Fig. 97(c) for a device failed after testing in the ON-state and Fig. 97(d) for a device tested in the OFF-state]. The energy-dispersive x-ray spectroscopy (EDX) analysis corresponding to the failure points [red crosses in Figs. 97(c) and 97(d)] is reported in Fig. 97(b). The failed region of the device tested in the ON-state has a high gallium and aluminum content, possibly originated by the melting of the barrier and channel layers. The crack in the device tested in the OFF-state has a lower gallium and aluminum concentration, since the GaN-based layers are separated side-by-side, and a high Si signal, because the electron beam is able to reach a larger part of the Si substrate through the crack.<sup>635,636</sup>

#### E. Radiation hardness

Owing to their very high operating limits and reliability, GaN-based devices are attractive for a wide range of special uses in

extreme ambient conditions, such as space applications. In order to be a viable option, their robustness against radiation doses has to be analyzed and confirmed. Different types of irradiation can lead to different effects; therefore, in the following, we will analyze each of them separately. For the interested reader, an extensive discussion can be found in recent reviews.<sup>637–639</sup>

### 1. Proton irradiation

The irradiation with protons can cause a wide range of effects in GaN-based devices, which can be related to the creation of new defects (or to the increase in concentration of pre-existing ones) caused by the interaction between the crystal lattice and the energetic protons.

The increase in defect concentration leads to a lowering of the mobility of the material, due to the scattering between the carriers and the defects, and to a reduction in carrier density, caused by the charge trapping in the defects and by the corresponding electrostatic effects. On the final devices, this corresponds to an increase in ON-resistance, a positive shift in the threshold voltage, and a reduction in the saturation current and in the peak transconductance value. The larger defect concentration causes a worsening of the dynamic behavior due to the increased density of states available for the trapping of charge.

In some cases, the dynamic  $R_{ON}$  is found to be decreased rather than increased by the proton irradiation:<sup>640</sup> on irradiated devices, an increase in OFF-state leakage is observed, indicating an increase in the unintentionally doped GaN layer conductivity. This conductivity increase leads to an increased deionization rate, thus reducing the dynamic ON-resistance.<sup>640</sup>

The level of damage depends on the energy of the protons, and it is found to be higher for lower energy.<sup>641,642</sup> This behavior may seem unexpected but is related to the larger non-ionizing energy loss of the lower energy particles in the barrier and channel region, whereas higher energy protons cause damage deeper in the device structure. Concerning the number of irradiated protons, a typical threshold value (at 1.8 MeV) for the variation in device performance is a fluence of  $10^{12}$ – $10^{13}$  p<sup>+</sup>/cm<sup>2</sup> at 1.8 MeV,<sup>643–645</sup>  $5 \times 10^9$  p<sup>+</sup>/cm<sup>2</sup> at 40 MeV.<sup>646</sup> Based on the energy dependence discussed above, the lower threshold fluence at higher energy is unexpected, and may be related to different device structure and quality in the various papers. It is worth pointing out that values for variation in dynamic performance may be lower than the ones reported for variation in DC characteristics.<sup>647</sup>

Specific defects created by proton irradiation include both deep donor and deep acceptor levels, as well as de-hydrogenation and reconfiguration of O<sub>N</sub>–H complexes.<sup>648,649</sup>

Most of the degradation caused by proton irradiation is related to displacement damage and is recoverable by high temperature annealing.<sup>650,651</sup>

### 2. Neutron irradiation

Neutron irradiation produces two main effects: an increase in threshold voltage and a decrease in the material mobility. The threshold voltage variation originates from the increase in concentration of pre-existing acceptor states in the barrier, and the amount of variation increases linearly with the neutron

fluence.<sup>637–639</sup> The cause of the lower material mobility is attributed to barrier acceptors too, which cause local threshold voltage and channel density variations and, therefore, additional scattering.

In general, neutrons are found to be less damaging than protons, both in terms of ON-resistance and breakdown voltage,<sup>648</sup> but cause extended damage rather than the creation of point defects found by other irradiation species.<sup>637</sup>

### 3. Electron irradiation

The main effect of electron irradiation is to cause a negative threshold voltage shift at lower fluence, which becomes positive at higher fluence, originated by the generation of traps with different charge states. Additionally, a monotonic decrease in channel mobility has been reported. The defects responsible for these variations have been extensively studied and include nitrogen vacancies and additional traps with 0.3, 0.45, 0.55, and 0.8 eV activation energy.<sup>638</sup>

### 4. Gamma ray irradiation

The irradiation with gamma rays is less tested, but some information is available from the literature. Reported effects include increase in ON-resistance, negative shift in threshold voltage, increased saturation current, decreased gate current, and increased reverse breakdown voltage.<sup>652</sup> The generated defects are supposed to be nitrogen vacancies (V<sub>N</sub>), which act as donors in GaN. Conflicting results have been reported, indicating instead a reduction in current.<sup>653,654</sup> The difference may originate from different device structure and quality or from the impact of different dose levels, showing improvements at lower dose and damage at high dose.<sup>655</sup>

### 5. Other ionizing species

Additional ionizing species have been tested on GaN devices, including helium and carbon.<sup>656</sup> Effects include increase in the ON-resistance, positive shift in threshold voltage, and reduction in saturation current, linearly proportional to the fluence, with no influence of the particle mass or energy. No variation in gate leakage was found.

## IX. CONCLUSIONS

In summary, with this Tutorial, we reviewed the properties and advantages of GaN and the characteristics, technology, and reliability of GaN-based transistors. These devices are expected to play a significant role in next-generation power converters: competition with Si and SiC is expected to become stronger and stronger in the coming years. A substantial improvement in device technology will be possible through extensive research, both at academic and industrial levels.

If, on the one hand, current GaN transistors can significantly improve the performance and reliability of switching mode power converters, next-generation scaled devices will enable monolithic integration, thus paving the way for the fabrication of miniaturized and MHz-range power converters. Further competition with Si and SiC will come from the development of vertical GaN transistors,

which have great potential for high power/high-voltage applications, and can be fabricated on inexpensive and large substrates.

A deep understanding of the material and device properties will allow us to further extend the operating ranges of the devices, thus enabling robust kV-range operations (for large-size devices) and sub-microsecond switching (for scaled transistors). Finally, a deep knowledge of trapping and reliability-limiting processes will allow us to push the devices to the limits, thus fully exploiting the competitive advantage of GaN, as a ground-breaking semiconductor for power electronics.

This paper provides a comprehensive overview on the properties of GaN and related devices and can be used as a reference for researchers willing to enter this interesting and complex field or looking for an update on the most recent advancements on device technology.

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## AUTHOR DECLARATIONS

### Conflict of Interest

The authors have no conflicts to disclose.

## DATA AVAILABILITY

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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