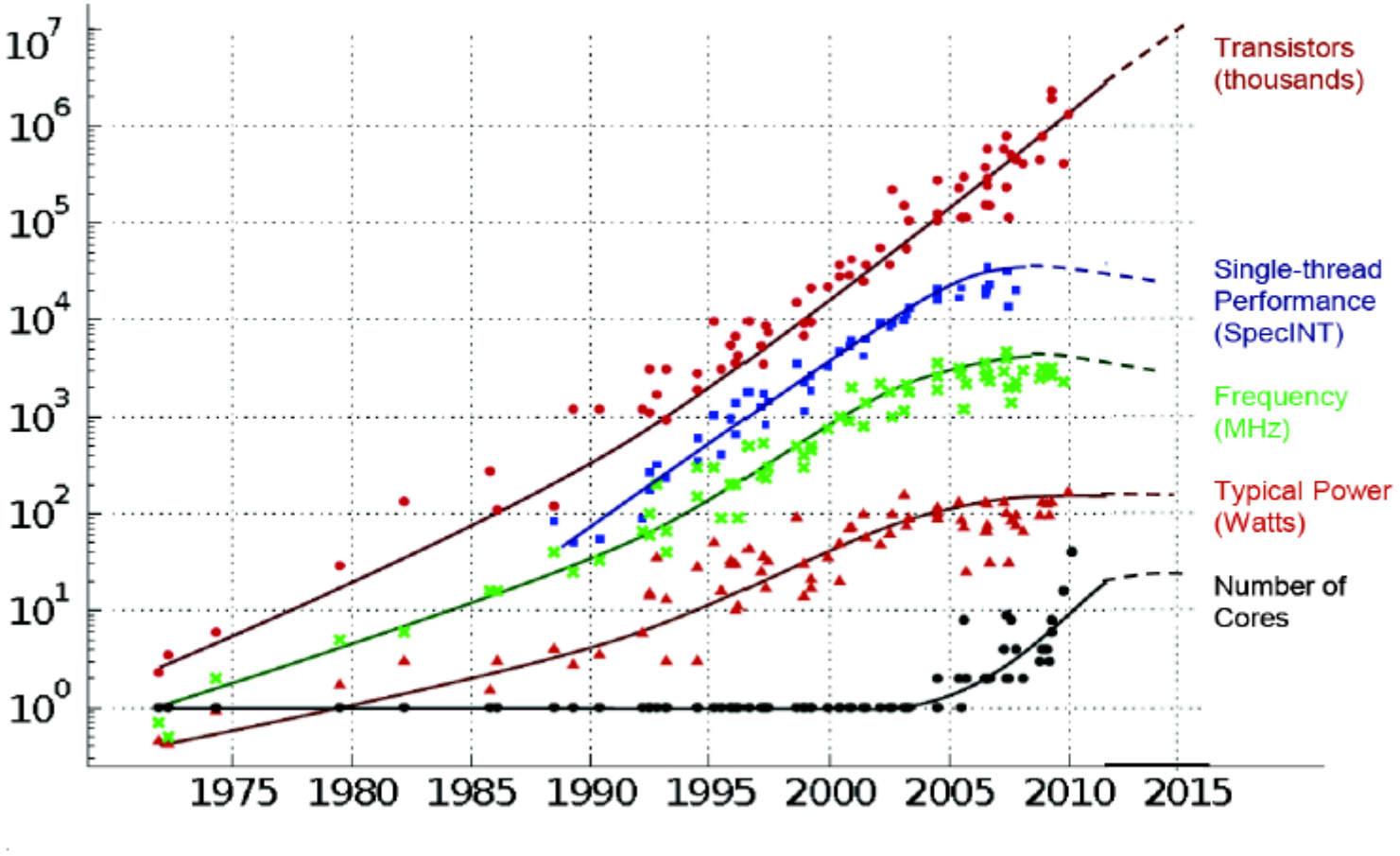
Sujet de contrôle Conception Conjointe SoC

Polytech Nice Sophia Antipolis

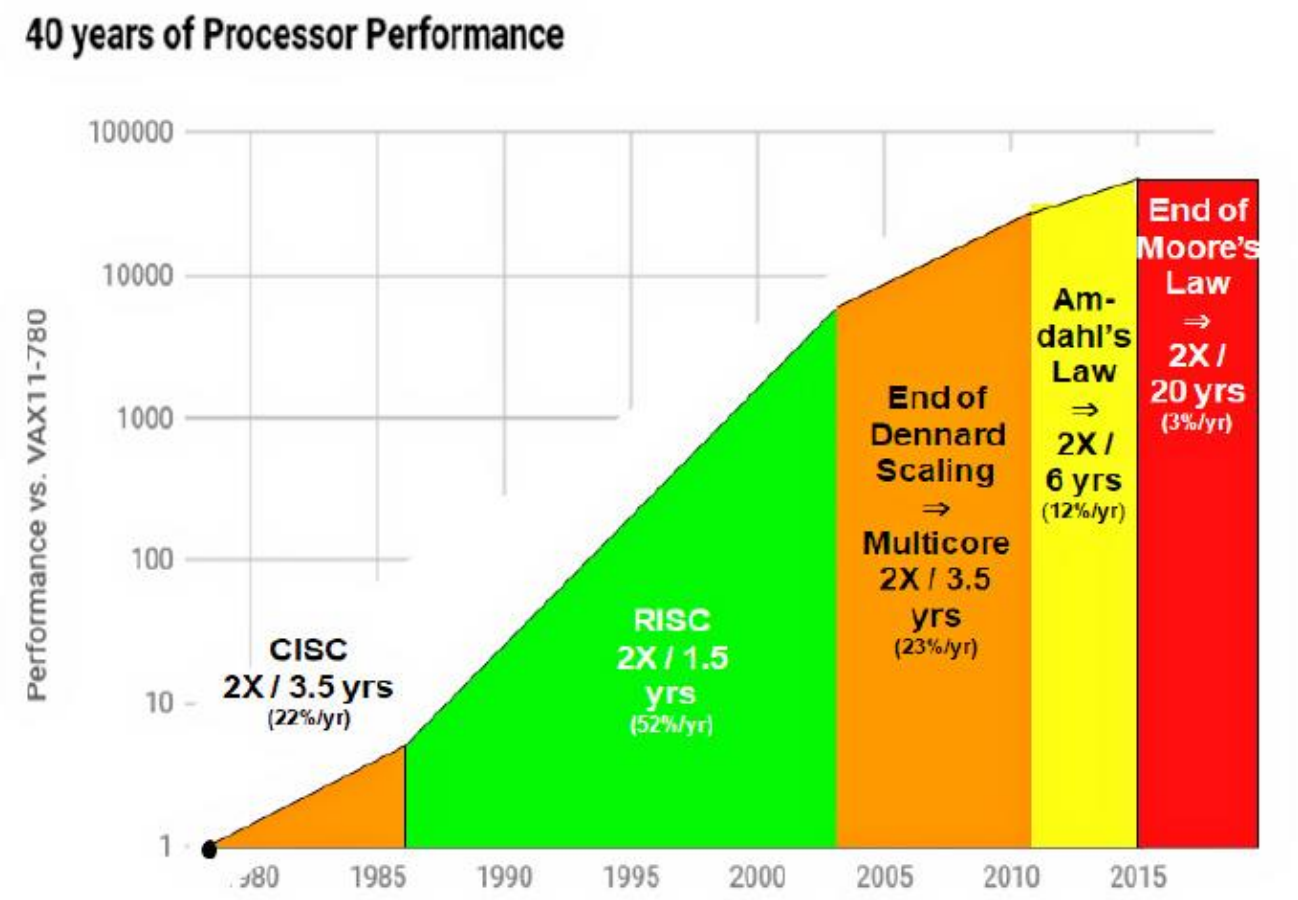
35 YEARS OF MICROPROCESSOR TREND DATA



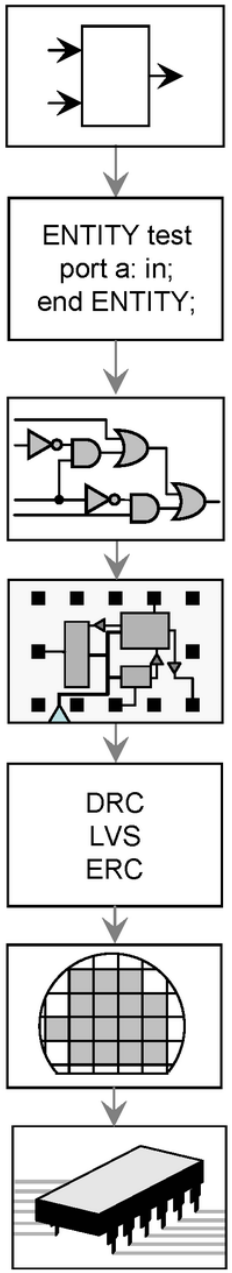
Original data collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond and C. Batten
Dotted line extrapolations by C. Moore

No more Moore

Hennessy & Patterson, Computer Architecture, a quantitative approach, 6e Ed., 2018



From system description to standard cells



System Specification

Architectural Design

Functional Design and Logic Design

Circuit Design

Physical Design

Physical Verification and Signoff

Fabrication

Packaging and Testing

Chip

Partitioning

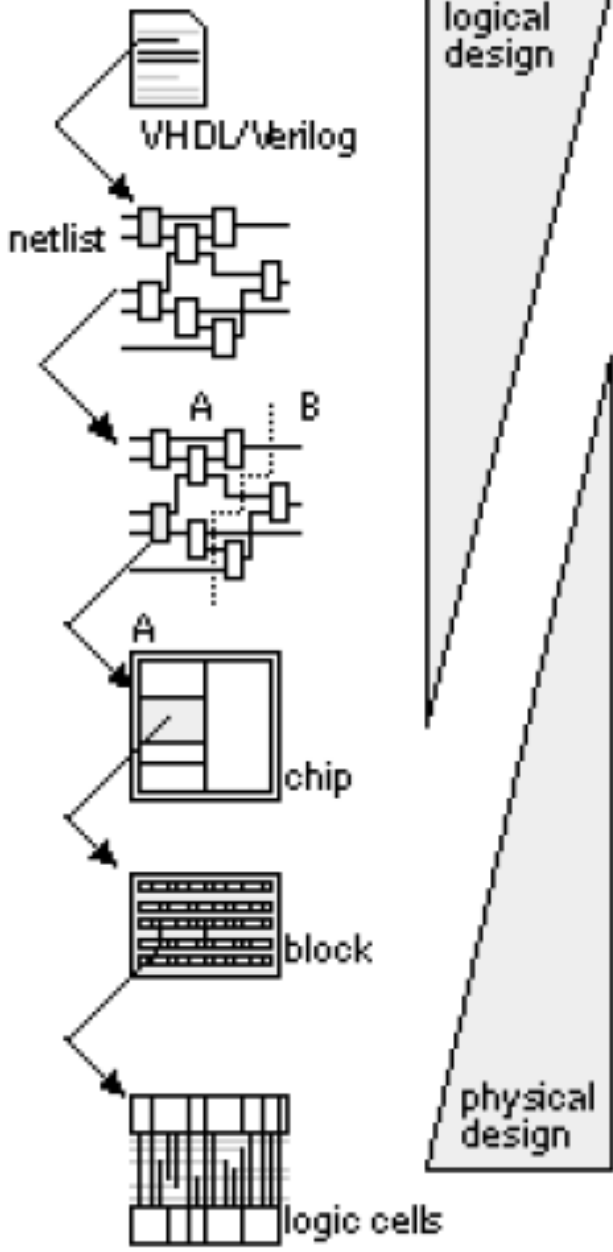
Floorplanning

Placement

Clock Tree Synthesis

Signal Routing

Timing Closure



Evolution of number of foundries

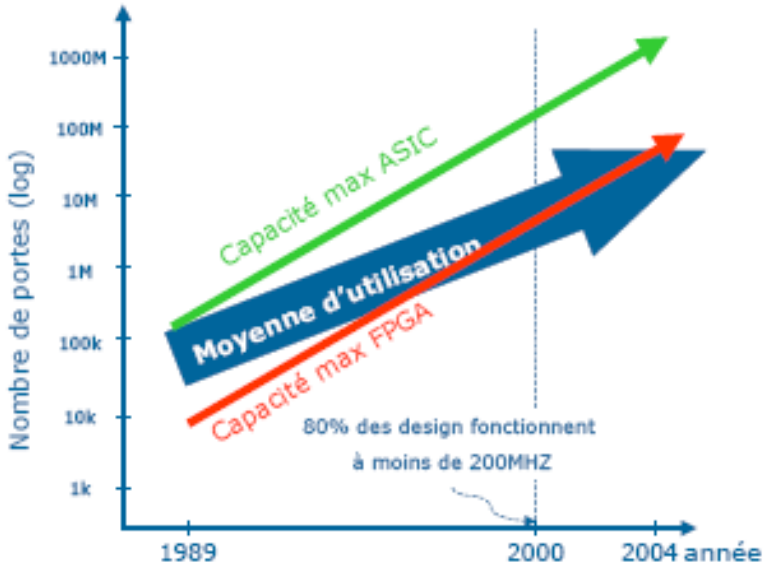
Number of Foundries with a Cutting Edge Logic Fab										
SilTerra X-FAB Dongbu HiTek ADI Atmel Rohm Sanyo Mitsubishi ON Hitachi Cypress Sony Infineon Sharp Freescale Renesas (NEC) SMIC Toshiba Fujitsu TI Panasonic STMicroelectronics UMC IBM AMD Samsung TSMC Intel	ADI Atmel Rohm Sanyo Mitsubishi ON Hitachi Cypress Sony Infineon Sharp Freescale Renesas SMIC Toshiba Fujitsu TI Panasonic STM UMC IBM AMD Samsung TSMC Intel	Cypress Sony Infineon Sharp Freescale Renesas SMIC Toshiba Fujitsu TI Panasonic STM UMC IBM AMD Samsung TSMC Intel	Renesas SMIC Toshiba Fujitsu TI Panasonic STM UMC IBM GlobalFoundries Samsung TSMC Intel	Renesas SMIC Toshiba Fujitsu TI Panasonic SMT UMC IBM GF Samsung TSMC Intel	Panasonic STM UMC IBM GF Samsung TSMC Intel	IBM GF Samsung TSMC Intel	GF Samsung TSMC Intel	Samsung TSMC Intel	Samsung TSMC Intel	Future
180 nm	130 nm	90 nm	65 nm	45 nm/40 nm	32 nm/28 nm	22 nm/20 nm	16 nm/14 nm	10 nm	7 nm	5 nm

Source: wikichip.org

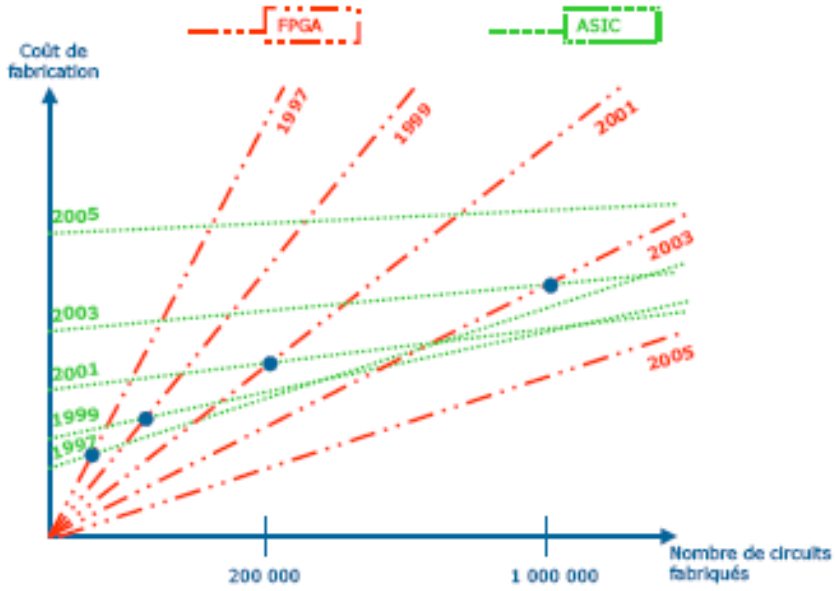
Comparaison ASIC - FPGA

	FPGA	Gate array	Standard cell	Full custom	Macro cell
Density	Low	Medium	Medium	High	High
Flexibility	Low (high)	Low	Medium	High	Medium
Analog	No	No	No	Yes	Yes
Performance	Low	Medium	High	Very high	Very high
Design time	Low	Medium	Medium	High	Medium
Design costs	Low	Medium	Medium	High	High
Tools	Simple	Complex	Complex	Very complex	Complex
Volume	Low	Medium	High	High	High

Pourquoi les FPGAs ?



Source : Altera, SOPC World Seminar 2001

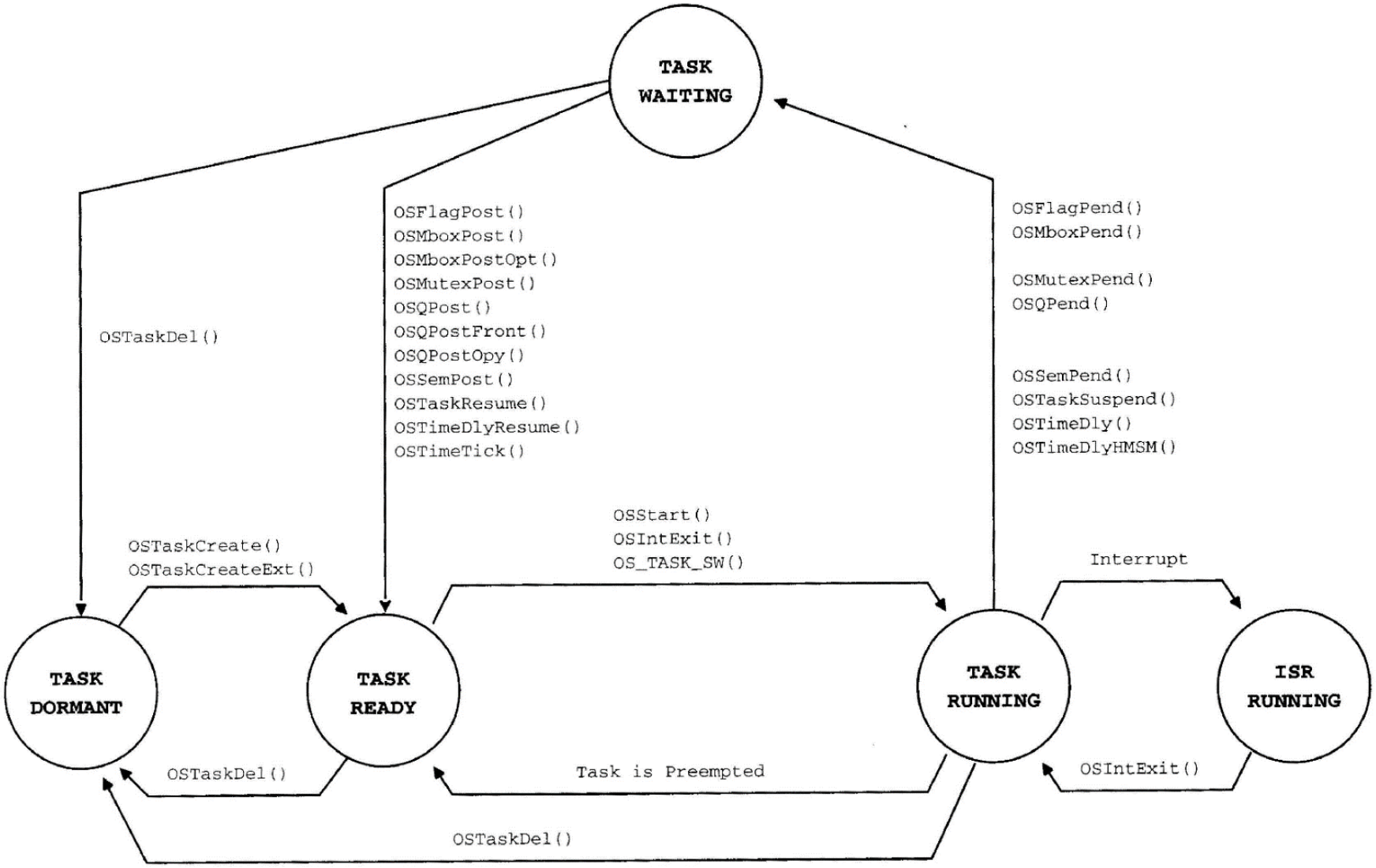


S. Tredennick, The Rise of Reconfigurable Systems, ERSA 2003

Systèmes embarqués temps réel

- Exemples :
  - Catégorie 1 :
    - Pilotage automatique de la ligne 14
    - Dispositif de surveillance d'une centrale nucléaire
    - Système de guidage de missiles
    - Régulateur de vitesse en automobile
  - Catégorie 2 :
    - Téléphone portable
    - Lecteur DVD, électroménager

State diagram



Comparison of memory technologies

	SRAM	DRAM	NAND Flash	PC-RAM	STT-RAM	R-RAM & Memristor
Data Retention	N	N	Y	Y	Y	Y
Memory Cell Factor (F^2)	50-120	6-10	2-5	6-12	4-20	<1
Read Time (ns)	1	30	50	20-50	2-20	<50
Write /Erase Time (ns)	1	50	106-10^5	50-120	2-20	<100
Number of Rewrites	10^{16}	10^{16}	10^5	10^{10}	10^{15}	10^{15}
Power Read/Write	Low	Low	High	Low	Low	Low
Power (Other than R/W)	Leakage Current	Refresh Power	None	None	None	None

Human, a thinking machine…

- Processeur principal : Cerveau
- Type : Processeur analogique
- Consommation : 10 W
- Fréquence d'horloge : de l'ordre de 100 Hz
- Débit : 1Tb/s
- Efficacité énergétique : Seul 1 à 16% des neurones fonctionnent à un moment donné
- Nombre d'éléments : ~100 Milliards de neurones
- Nombre de connexions : ~20 000 connexions par neurone
- Volume : 22 dm3

- Capacité de calcul : 10^{15} (100 Tera)opérations/sec

- Capacité mémoire : 10 bits à chacun des 10^{14} synapses

*estimations