Low Frequency Noise Characteristics in Multilayer $MoTe_2$ FETs with Hydrophobic Amorphous Fluoropolymers

Seung Gi Seo, Jong Hun Hong*, Jae Hyeon Ryu and Sung Hun Jin⊥, Member, IEEE*

***Abstract*— This paper investigates the low-frequency noise (LFN) properties of multilayer $MoTe_2$ field effect transistors (FETs) before and after hydrophobic amorphous polymer (CYTOP) encapsulation in the subthreshold and linear regimes. Noise spectrum density of drain current (S_{ID}) shows that the low-frequency noise in multilayer $MoTe_2$ FETs nicely fits to a $1/f^{\gamma}$ power law with $\gamma \sim 1$ in the frequency range of 10 Hz to 200 Hz. From the dependence of S_{ID} on the drain current, carrier number fluctuation(Δn) is considered as a dominant low frequency noise mechanism from all operation regimes in multilayer $MoTe_2$ FETs. Extracted trap density(N_t) based on McWhorter model in this study was reduced at least more than one order level, as compared to multilayered $MoTe_2$ FETs without CYTOP passivation.**

***Index Terms*—$MoTe_2$ FETs, 1/f noise, CYTOP**

I. Introduction

Recently transition metal dichalchogenides (TMDCs) have been actively researched toward various electronic applications due to their novel electrical, optical, and chemical properties as well as ideal two dimensional structure [1], [2]. Among various TMDCs, many research activities have been predominantly focused on MoS_2 FETs because of its abundance, nontoxicity, easy preparation of MoS_2 films through exfoliation or/and CVD [3], [4]. However, as one of promising TMDCs, $MoTe_2$ has been actively explored for the application of logic circuits and optical/chemical sensors [5]-[7]. This is particularly attributed to its smaller semiconducting energy band gap (i.e., E_g~0.8 (or 1.24 eV) for multilayers (or single layer) $MoTe_2$, respectively), suitable for near infrared wavelength and ambipolar electronic applications. However, most of research activities in $MoTe_2$ field effect transistors have been focused on high performance device implementation, understanding on gas (or chemical) adsorption effects, along with transport behaviors in ultra-low temperature [5]-[7], [11], [12]. Interestingly there have been very limited reports on investigation of device instability of $MoTe_2$ FETs, even though the in-depth understanding on the device instability is highly necessary. As one of the most powerful diagnostic tools to understand physics on the flicker noise and device instability mechanism owing to charge scattering and trapping (or de-trapping), low frequency noise characterization has been utilized to investigate into origins of device instabilities in FETs.

In recent years, several studies on low noise characteristics in $MoTe_2$ FETs were reported, but most of $MoTe_2$ FETs were based on n-type or ambipolar properties in lieu of p-type properties [8]-[10]. Typically, p-type behaviors on $MoTe_2$ FETs are more frequently observed in literatures [11]-[12], thereby their understanding on low noise characteristics in conventional p-type $MoTe_2$ FETs comparatively remain elusive at present. Furthermore, implemented $MoTe_2$ FETs have unrealistic gate dielectric thickness of thermal oxide (T_{ox}=300nm) in the respects of next-generation device operation, leading to a large operating voltage around 60V range [8]-[10]. In addition, in a recent past high-k layers such as Al_2O_3 and HfO_2 based on atomic layer deposition (ALD)were conveniently adopted for reliable operation of $MoTe_2$ FETs [8]-[10]. Even though hysteresis gap for $MoTe_2$ FETs after Al_2O_3 passivation is negligibly achieved in transfer characteristics, intrinsic low noise characteristics in $MoTe_2$ FETs were easily distorted owing to either positive fixed trap charges in high-k layers or dipole charges at the back channel interface [13]-[15]. Thus, the afore-mentioned issues have led to limited understanding on device instabilities and their mechanisms for multi-layered $MoTe_2$ FETs.

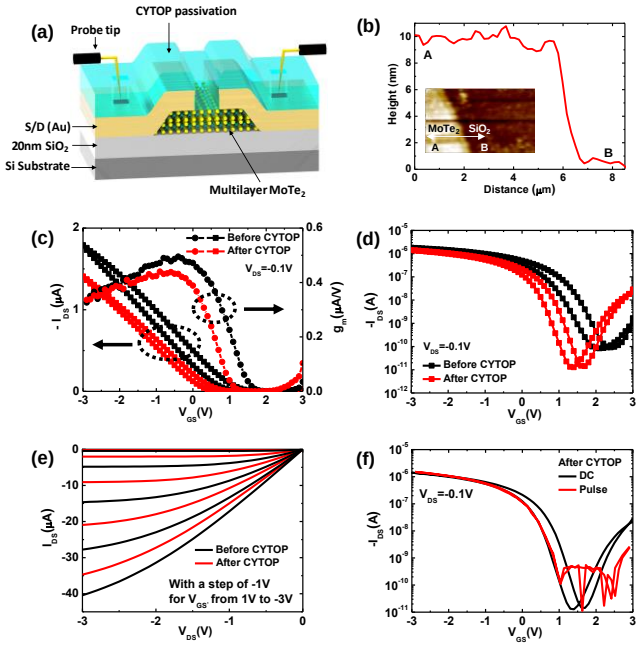

FIG. 1. (a) A Schematic diagram for multi-layer $MoTe_2$ FETs with Au contact. (b) Height profile for a multilayer in the channel of representative $MoTe_2$ FETs which has been scanned along the red line from A to B in the channel by atomic force microscope. The AFM images for the channel regime for $MoTe_2$ FETs. The channel length and width is 10 μm and 30 μm, respectively. (c) Transfer and transconductance(g_m) characteristics for multilayer $MoTe_2$ FETs before and after CYTOP passivation measured in the linear operation regime at the drain bias of V_{DS}= -0.1V. (d) Transfer characteristics of $MoTe_2$ FETs before and after CYTOP passivation, displayed in the log scale (e) Output characteristics of $MoTe_2$ FETs before and after CYTOP passivation. (f) Transfer characteristics of $MoTe_2$ FETs measured in DC and pulsed mode.

Manuscript received xxxx xx, 2018; revised xxxx xx, xxxx. Date of publication xxxxxx xx, xxxx; date of the current version xxxxx xx, xxxx. This work was supported by National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT & Future Planning (NRF-2017R1A2B2009042). S. G. Seo, J.H. Hong, J.H. Ryu, and S. H. Jin are affiliated with the Department of Electronic Engineering, Incheon National University, 406-772, Incheon, Korea. (e-mail: shjin@inu.ac.kr). *S. G. Seo and J. H. Hong contributed equally to this work.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2018.2889904, IEEE Electron Device Letters

Herein, we implemented 3V operational $MoTe_2$ FETs with 20 nm-thick thermal gate oxide(SiO_2) which show typical p-type behaviors. Thereafter, we immediately evaluated low noise characteristics and analyzed electrical properties for p-type $MoTe_2$ FETs, consecutively followed by cyclized transparent optical polymer (CYTOP) encapsulation. As one of representative hydrophobic polymers, CYTOP passivation has been reported to improve the instability of TMDC FETs and optical sensors in diodes [16]. Thus, we adopted CYTOP encapsulation for the investigation of internal instability issues in multi-layered $MoTe_2$ FETs because this encapsulation was well known to secure removal of external gas (i.e., H_2O and O_2) ambient effects with the minimal change of intrinsic properties of TMDC FETs [16] as compared to that before passivation. With the confirmed devices, to the best of our knowledge, the LFN characteristics of $MoTe_2$ FETs in air were firstly characterized in the subthreshold and linear regimes with systematic ways. Moreover, direct comparison on low noise characteristics before and after CYTOP passivation was thoroughly analyzed. The measured noise characteristics were nicely matched with carrier number of fluctuation model(Δn), thereby trap density(N_t) before and after CYTOP passivation was extracted by using McWhorter model [23].

II. Fabrication and Device Structure

Fig. 1 (a) shows the perspective view of multilayer $MoTe_2$ FETs with a bottom gate structure. An n-type silicon wafer with heavy phosphorus doping (ρ~0.005 ohm·cm) was utilized as a starting substrate for back gate electrodes. 20nm-thick-silicon dioxide was thermally grown on heavy doped Si wafers, followed by serving as a gate dielectric. Mechanical exfoliation from bulk $MoTe_2$ crystals were executed by using PDMS stamps and immediately transferred onto SiO_2/Si substrates, yielding multi-layered $MoTe_2$ layers on thermal oxide. In the ambient with a mixed gas of argon and hydrogen, annealing process at 350°C for 1 hour was performed to relieve organic residues which might be contaminated on multi-layered $MoTe_2$ during transfer processes [17]. Source and drain electrode regions were phtolithographically defined, followed by thermal evaporation of Au (~40 nm). Right after lift-off process in the acetone during overnight, good Ohmic contact properties between source (or drain) Au electrodes and $MoTe_2$ layers were obtained. In the interim, layer thickness of multi-layered $MoTe_2$ films on thermal oxide was measured by using atomic force microscopy (AFM) as shown in Fig. 1(b). The AFM analysis identified the thickness of $MoTe_2$ as 10.6 nm which approximately corresponds to 16 layers [18]. After measuring basic electrical characteristics on $MoTe_2$ FETs including transfer/output characteristics as well as 1/f noise properties, the backside of $MoTe_2$ flake was encapsulated by amorphous fluorinated polymer (CYTOP; CTL-809M, Asahi Glass Co., Ltd) with typical spin coating process, followed by baking at 150°C for 1 hour in a glove box with Ar ambient. Thereafter, probing pads (~Au) were selectively open for electrical addressing by dry etching (~O_2/CF_4) via photolithographic pattern on the CYTOP.

III. Results and Discussion

Fig. 1(c) and (d) shows the transfer characteristics of a

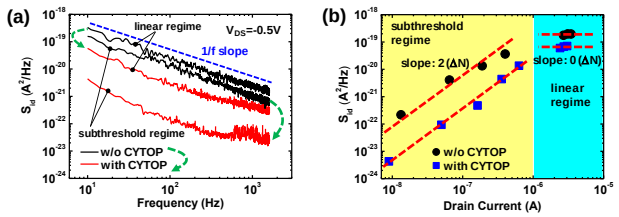

Fig. 2 (a) Drain-current noise spectral densities S_{ID}'s for the device which were measured at different operation regimes, respectively; sub-threshold (V_{GS} = -0.03 V, V_{DS} = -0.5 V), linear (V_{GS} = -0.8 V, V_{DS} = -0.5 V). (b) Measured noise power spectral densities (S_{ID}) vs drain current (I_D) at a fixed frequency of 10 Hz. The carrier number fluctuations before and after CYTOP passivation were observed in the subthreshold and linear regimes. Solid symbol and dot-line curves correspond to experimentally measured and theoretically estimated data, respectively. Solid circles(●) and squares(■) stand for $MoTe_2$ FETs before and after CYTOP passivation. Electrical characterization for LNAs were evaluated at V_{DS}=-0.5V, as compared with other transfer characteristics at V_{DS}=-0.1 V.

fabricated multilayer $MoTe_2$ FET before and after CYTOP passivation at a drain-to-source voltage (V_{DS}) of -0.1 V. The ratio of width to length for this device is W/L=30/10 µm. The electrical characteristics of the devices were measured by using a precision semiconductor parameter analyzer (Agilent 4155B). The curves before (or after) CYTOP passivation show typically observed p-type behaviors with a sub-threshold swing (S*S*) of 430 (or 320) mV/decade, a field effect mobility (μ_{FE}) of 9.56±0.14 (or 8.49±0.18) $cm^2/V \cdot s$, a threshold voltage (V_{th}) of 0.93±0.10 (or 0.62±0.15) V, and an on/off ratio of ~4×10^4 (or ~1×10^5), respectively, where V_{th} was calculated by fitting a straight line to the measured transfer curve. The field effect mobility was extracted from maximum point of transconductance (g_{m_max}) of 0.49 ±0.02 (or 0.44±0.03) μS according to $\mu_{eff}=L \cdot g_m(WC_iV_{DS})^{-1}$, where C_i and g_m are the gate capacitance per unit area and the transconductance, respectively. For the accurate estimation of electrical properties excluding contact resistance effects, Y-function method(YFM) [19]-[20] has been used in this work. By using analysis of YFM, field effect mobilities and contact resistance (R_c) for multilayer $MoTe_2$ FET before (or after) CYTOP passivation, were extracted as 17.37 ±0.38 (or 15.96 ±0.31) cm^2/Vsec and 4.69±1.50 (or 7.92±0.96) kΩ, respectively. After CYTOP passivation, output characteristics as shown in Fig.1(e) were slightly reduced due to V_{th} shift toward negative direction. Fig.1(f) shows transfer characteristics in pulsed mode ($t_{period}=t_{on}+t_{off}$~1 ms, t_{on}=0.5 ms, V_{base}=0 V), confirming that hysteresis gap was reduced to a negligible level. For the better understanding on origins of device instability, i.e., front (or back) channel in $MoTe_2$ FETs, we tested $MoTe_2$ FETs with (or without) CYTOP in DC and pulse mode under vacuum ambient (~10^{-6} torr). Subthreshold slope (ΔSS), threshold voltage (ΔV_{th}) and hysteresis gap (ΔV_{hys}) for $MoTe_2$ FETs without CYTOP were significantly improved in vacuum ambient. Thus, most of key factors to cause device instability are engaged in the back channel. Furthermore, front channel effects are confirmed by back channel passivation of CYTOP, followed by pulse-mode measurement as shown in Fig. 1(f).

Fig. 2(a) shows the S_{ID} of the device measured in the sub-threshold and linear regimes by using low-noise current preamplifier (SR570) and dynamic signal analyzer (Agilent 35670A). Measured S_{ID} is nicely governed by the relationship

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2018.2889904, IEEE Electron Device Letters

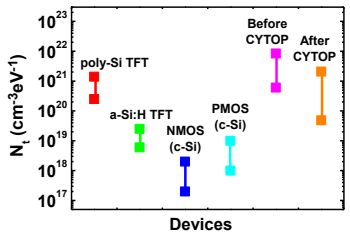

Fig. 3 Extracted trap density (N_t) by using McWhorter model for a-Si:H TFTs (■), NMOS (c-Si)(■), PMOS(c-Si)(■), $MoTe_2$ FETs before (■) and after (■) CYTOP passivation, respectively. Trap densities for a-Si: H TFTs (■), NMOS (c-Si)(■), PMOS(c-Si)(■) which have been reported in the literature. Trap densities were extracted for $MoTe_2$ FETs before and after CYTOP passivation.

of $1/f^{\gamma}$ where the γ is close to 1 in the frequency less than ~200 Hz in all operation regimes. Historically 1/f noise characteristics in metal-oxide-semiconductor (MOS) FETs have been comprehended by two distinct mechanisms [21]; (1) carrier mobility fluctuation (Δμ; Hooge) [22] and (2) carrier number fluctuation (Δn; McWhorter) [23]. In this regard, carrier mobility fluctuation is mainly attributed to lattice scattering of carriers [22]. On the other hand, carrier number fluctuation is predominantly caused by carrier number fluctuation associated with trapping (or de-trapping) process [23]. In order to distinguish the origin of fluctuations coming from carrier mobility (or carrier number) in FETs, noise spectrum density of drain current (S_{ID}) is systematically analyzed under a gate and drain bias condition. In a sub-threshold and linear regime, the drain bias was fixed at -0.5 V and the gate bias was changed from 0.4 V to -2.0 V. Fig. 2(a) shows that the S_{ID} is proportional to the square of drain current (I_{DS}^2) in sub-threshold regime. In the linear regime, a constant S_{ID} depending on I_{DS} was observed. The S_{ID} relationship, observed in Fig.2(a), unveils that multi-layered $MoTe_2$ FETs are excellently governed by the McWhorter theory,

$$S_{ID}(f) = \frac{k^*}{f}\frac{\mu_{eff}}{C_i L_{eff}}\frac{I_D V_{DS}}{(V_{GS}-V_T)} \quad \text{---------- (1)}$$

where k* takes into account the electron tunneling from insulator traps near the interface to the conducting channel and vice versa. In crystalline Si MOSFETs, we have $k^*=(q^2 D_t(E_F)kT\times (\ln(\tau_2/\tau_1))^{-1}$, where $D_t(E_F)$ is the active trap density in the vicinity of Fermi level (E_F), and τ_1 and τ_2 are the lower and upper boundaries of time constants involved in the trapping (or de-trapping) process [24]. Furthermore, in the subthreshold conduction regime, the S_{ID} relationship for I_{DS} was governed by the relationship (2) which can be linked to the trap density, N_t.

$$\frac{S_{ID}(f)}{I_D^2} = \frac{\lambda kTqN_t}{fWL_g n_s^2} \approx \frac{\lambda kTq^2 t_{ox}^2 N_t}{fWL_g(\varepsilon_o\varepsilon_{ox})^2(V_{GS}-V_{th})^2} \quad \text{-------- (2)}$$

where N_T the trap concentration in the oxide ($eV^{-1}cm^{-3}$), tunneling constant ($\lambda=(h/4\pi)\times(2m_e\phi_B)^{-0.5} \approx 10^{-8}$ cm), n_s is the channel electron concentration, k is the Boltzmann constant, T is the temperature in kelvin, t_{ox} is the oxide thickness, q is the carrier charge, m_e is the mass of the electron tunneling in the oxide layer, h is Planck's constant, and ϕ_B is the oxide tunneling barrier height [25]. The result hints that mechanism of low frequency noise in subthreshold regime is mainly coming from carrier number (Δn) fluctuation. Fig.2(b) shows that multi-layered $MoTe_2$ FETs show the reduced S_{ID} after CYTOP passivation. This indicates that carrier number (Δn) fluctuation could be reduced by novel scheme of the external passivation. For the quantitative analysis on trap density(N_t) of gate insulators in $MoTe_2$ FETs, we plotted all extracted N_t′s in the same graph as shown in Fig.3. N_t of multi-layered $MoTe_2$ FETs before CYTOP passivation was extracted in the range from 1.02×10^{15} to 2.64×10^{16} $eV^{-1}cm^{-3}$. On the other hand, N_t value after CYTOP passivation was extracted in the range from 9.67×10^{13} to 6.11×10^{15} $eV^{-1}cm^{-3}$, indicating that at least one order of magnitude of N_t level was reduced as compared to the device before backside passivation. This behavior is possibly attributed to the reduction of interface trap density at front or/and back channel. The interface traps are strongly involved in charge trapping and de-trapping events, nearby front channel interface between $MoTe_2$ layers and SiO_2. The charge trapping (or de-trapping) events could be significantly suppressed due to reduction of moisture and oxygen diffusion toward main channel interface by CYTOP encapsulation. Fig. 3 shows representative N_t values which correspond to a-Si thin film transistors(TFTs) (N_t~ 10^{18}~10^{19}) [25], single crystalline Si FETs with n (or p)-type channel (n-type; N_t~2.3×10^{16}~5×10^{16}, p-type; N_t~ 3×10^{16}~6×10^{16}) [26]-[27], and multi-layered $MoTe_2$ FETs in this work, before (N_t~6.0×10^{20}~8.4×10^{21}) and after (N_t~ 4.8×10^{19}~2.1×10^{21}) CYTOP passivation. For reliable comparison on extracted electrical parameters via LNF analysis, we extracted trap levels (D_{it}) from subthreshold slope. As similar to the extracted trap levels with the relationship of McWhorter model, trap reduction trends are exactly same. As per quantitative analysis on the change of N_t level after CYTOP passivation, % reduction of N_t, extracted from a subthreshold slope, was 29.7%, whereas % reduction extracted from LNA characteristics was 96.7%, respectively. Even though % reduction level was different for each extraction method, the trend of decrease in N_t level after CTYOP passivation is consistently within the same behavior. All results indicate that multi-layered $MoTe_2$ FETs have trap levels within similar order of magnitudes, as compared to poly-Si (or a-Si) TFTs, but inferior to c-Si FETs. Moreover, at least one order of N_t reduction can be achieved by novel passivation scheme, possibly due to reduction of O_2 and moisture effects of back channel. In addition, as compared to linear regime, noise level in subthreshold regime is relatively low. The origin of difference is not clear, but the main difference is possibly coming from the different current level, leading to the increase of chances in trapping and release events associated with fully accumulated charge layers in the channel of $MoTe_2$.

IV. Conclusion

In summary, we have investigated low frequency noise characteristics of multi-layered $MoTe_2$ FETs. Novel passivation scheme can dramatically reduce S_{ID}, leading to reduction of N_t levels. As compared with analysis via mixed models for $MoTe_2$ FETs previously reported in the literatures [8]-[10], carrier number fluctuation(Δn) in this study is exhibited as a predominant noise model, which is, to the best of our knowledge, the first reports for multi-layered $MoTe_2$ FETs. Extracted N_t values in this work is at least comparable to poly-Si (or a-Si) TFTs in the previously reported literature [25]-[27].

REFERENCES

[1] X. Huang, Z. Zeng, and H. Zhang, "Metal dichalcogenide nanosheets: preparation, properties and applications," *Chem. Soc. Rev.*, vol. 42, pp. 1934-1946, 2013, doi: 10.1039/c2cs35387c.

[2] D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, and M. C. Hersam, "Emerging Device Applications for Semiconducting Two-Dimensional Transition Metal Dichalcogenides," *ACS Nano*, vol. 8, pp. 1102-1120, Jan. 2014, doi: 10.1021/nn500064s.

[3] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nat. Nanotechnol.*, vol. 6, pp. 147-150, Jan. 2011, doi: 10.1038/NNANO.2010.279.

[4] Y. P. Venkata Subbaiah, K. J. Saji, and A. Tiwari, "Atomically Thin MoS_2: A Versatile Nongraphene 2D Material," *Adv. Funct. Mater.*, vol. 26, pp. 2046-2069, 2016, doi: 10.1002/adfm.201504202.

[5] Y.-F. Lin, Y. Xu, S.-T. Wang, S.-L. Li, M. Yamamoto, A. Aparecido-Ferreira, W. Li, H. Sun, S. Nakaharai, W.-B. Jian, K. Ueno, and K. Tsukagoshi, "Ambipolar $MoTe_2$ Transistors and Their Applications in Logic Circuits," *Adv. Mater.*, vol. 26, pp. 3263-3269, 2014, doi: 10.1002/adma.201305845.

[6] H. Huang, J. Wang, W. Hu, L. Liao, P. Wang, X. Wang, F. Gong, Y. Chen, G. Wu, W. Luo, H. Shen, T. Lin, J. Sun, X. Meng, X. Chen, and J. Chu, "Highly sensitive visible to infrared $MoTe_2$ photodetectors enhanced by the photogating effect," *Nanotechnology*, vol. 27, p. 445201, Sep. 2016, doi: 10.1088/0957-4484/27/44/445201.

[7] F. Zhihong, X. Yuan, C. Jiancui, Y. Yuanyuan, Z. Shijun, Z. Rui, Q. Li, X. Chen, C. Sun, H. Zhang, W. Pang, J. Liu and D. Zhang, "Highly sensitive $MoTe_2$ chemical sensor with fast recovery rate through gate biasing," *2D Mater.*, vol. 4, p. 025018, Feb. 2017, doi: 10.1088/2053-1583/aa57fe.

[8] H. Ji, M.-K. Joo, Y. Yun, J.-H. Park, G. Lee, B. H. Moon, H. Yi, D. Suh, and S. C. Lim, "Suppression of Interfacial Current Fluctuation in $MoTe_2$ Transistors with Different Dielectrics," *ACS Appl. Mater. Interfaces*, vol. 8, pp. 19092-19099, Jun. 2016, doi : 10.1021/acsami.6b02085.

[9] H. Ji, M.-K. Joo, H. Yi, H. Choi, H. Z. Gul, M. K. Ghimire, and S. C. Lim, "Tunable Mobility in Double-Gated $MoTe_2$ Field-Effect Transistor: Effect of Coulomb Screening and Trap Sites," *ACS Appl. Mater. Interfaces*, vol. 9, pp. 29185-29192, Aug. 2017, doi: 10.1021/acsami.7b05865.

[10] Y.-F. Lin, Y. Xu, C.-Y. Lin, Y.-W. Suen, M. Yamamoto, S. Nakaharai, K. Ueno, and K. Tsukagoshi, "Origin of Noise in Layered $MoTe_2$ Transistors and its Possible Use for Environmental Sensors," *Adv. Mater.*, vol. 27, pp. 6612-6619, 2015, doi: 10.1002/adma.201502677.

[11] S. Fathipour, N. Ma, W. S. Hwang, V. Protasenko, S. Vishwanath, H. G. Xing, and A. Seabaugh., "Exfoliated multilayer $MoTe_2$ field-effect transistors," *Appl. Phys. Lett.*, vol. 105, p. 192101, Nov. 2014, doi: 10.1063/1.4901527.

[12] N. R. Pradhan, D. Rhodes, S. Feng, Y. Xin, S. Memaran, B.-H. Moon, H. Terrones, M. Terrones, and L. Balicas, "Field-Effect Transistors Based on Few-Layered α-$MoTe_2$," *ACS Nano*, vol. 8, pp. 5911-5920, May. 2014, doi: 10.1021/nn501013c

[13] A. D. Franklin, S. O. Koswatta, D. B. Farmer, J. T. Smith, L. Gignac, C. M. Breslin, C. M. Breslin, S.-J. Han, G. S. Tulevski, H. Miyazoe, W. Haensch, and J. Tersoff , "Carbon Nanotube Complementary Wrap-Gate Transistors," *Nano Lett.*, vol. 13, pp. 2490-2495, May. 2013, doi: 10.1021/nl400544q.

[14] N. Moriyama, Y. Ohno, T. Kitamura, S. Kishimoto, and T. Mizutani, "Change in carrier type in high-k gate carbon nanotube field-effect transistors by interface fixed charges," *Nanotechnology*, vol. 21, p. 165201, Mar. 2010, doi: 10.1088/0957-4484/21/16/165201.

[15] J. Zhang, C. Wang, Y. Fu, Y. Che, and C. Zhou, "Air-Stable Conversion of Separated Carbon Nanotube Thin-Film Transistors from p-Type to n-Type Using Atomic Layer Deposition of High-k Oxide and Its Application in CMOS Logic Circuits," *ACS Nano*, vol. 5, pp. 3284-3292, Apr. 2011, doi: 10.1021/nn2004298.

[16] J. Roh, I.-T. Cho, H. Shin, G. W. Baek, B. H. Hong, J.-H. Lee, S. H. Jin, and C. Lee, "Fluorinated CYTOP passivation effects on the electrical reliability of multilayer MoS_2 field-effect transistors," *Nanotechnology*, vol. 26, p. 455201, Oct. 2015, doi: 10.1088/0957-4484/26/45/455201.

[17] J. H. Ryu, G.-W. Baek, S. J. Yu, S. G. Seo, and S. H. Jin, "Photosensitive Full-Swing Multi-layer MoS_2 Inverters with Light Shielding Layers," *IEEE Electron Device Lett.*, vol. 38, pp. 67-70, Jan. 2016, doi: 10.1109/LED.2016.2633479.

[18] C. Ruppert, O. B. Aslan, and T. F. Heinz, "Optical Properties and Band Gap of Single- and Few-Layer $MoTe_2$ Crystals," *Nano Lett.*, vol. 14, pp. 6231-6236, Oct. 2014, doi: 10.1021/nl502557g.

[19] J. Na, M. Shin, M.-K. Joo, J. Huh, Y. J. Kim, H. J. Choi, J. H. Shim, and G.-T. Kim, "Separation of interlayer resistance in multilayer MoS_2 field-effect transistors," *Appl. Phys. Lett.*, vol. 104, p. 233502, Jun. 2014, doi: 10.1063/1.4878839.

[20] H.-Y. Chang, W. Zhu, and D. Akinwande, "On the mobility and contact resistance evaluation for transistors based on MoS_2 or two-dimensional semiconducting atomic crystals," *Appl. Phys. Lett.*, vol. 104, p. 113504, Mar. 2014, doi: 10.1063/1.4868536.

[21] L. K. J. Vandamme, X. Li, and D. Rigaud, "l/f Noise in MOS Devices, Mobility or Number Fluctuations?," *IEEE Electron Device Lett.*, vol. 41, pp 1936-1945, Nov. 1994, doi: 10.1109/16.333809.

[22] F. N. Hooge, "1/f noise sources," *IEEE Trans. Electron Devices*, vol. 41, pp. 1926-1935, Nov. 1994, doi: 10.1109/16.333808.

[23] A. L. McWhorter, Semiconductor Surface Physics (University of Pennsylvania Press, 1957), p.207.

[24] D. Rigaud, M. Valenza, and J. Rhayem, "Low frequency noise in thin film transistors," *IEE Proceedings - Circuits, Devices and Systems*, vol. 149, pp. 75-82, Feb. 2002, doi: 10.1049/ip-cds:20020063.

[25] S. L. Rumyantsev, S. H. Jin, M. S. Shur, and M.-S. Park, "Low frequency noise in amorphous silicon thin film transistors with SiN_x gate dielectric," *J. Appl. Phys.*, vol. 105, p. 124504, Jun. 2009, doi: 10.1063/1.3147928.

[26] G. Reimbold, "Modified 1/f trapping noise theory and experiments in MOS transistors biased from weak to strong inversion—Influence of interface states," *IEEE Trans. Electron Devices*, vol. 31, pp. 1190-1198, Sep. 1984, doi: 10.1109/T-ED.1984.21687.

[27] M. Fadlallah, G. Ghibaudo, J. Jomaah, M. Zoaeter, and G. Guegan, "Static and low frequency noise characterization of surface- and buried-mode 0.1 μm P and N MOSFETs," *Microelectron Reliab.*, vol. 42, pp. 41-46, Jan. 2002, doi: 10.1016/S0026-2714(01)00232-3.