On the Impact of PWM Modulation Strategies on the Discrete-Time Modeling of a Boost Converter

Nicolas Dimate
MSc Graduate, ENSTA Paris
Institut Polytechnique de Paris
Paris, France
junmorenodi@gmail.com

Sergio A. Dorado-Rojas , Daniel K. Molzahn Georgia Institute of Technology School of Electrical and Computer Engineering Atlanta, GA {sadr, molzahn}@gatech.edu

Abstract—Accurate control design of power electronic systems requires a detailed understanding of how the chosen modulation influences converter behavior. This paper explores the integration of single- and double-edge modulation strategies into the discrete-time (DT) modeling of DC-DC converters. By revisiting a mathematical framework, large- and small-signal models are derived via a sampled-data approach. Open-loop analysis of a boost converter reveals that the modulation strategy significantly affects the control-to-output transfer function. Trailing-edge modulation yields better phase margins than leading-edge and triangular strategies. Nonlinear simulations confirm that PWM-aware DT models are valuable in critical applications for targeted control design and improved converter performance.

I. INTRODUCTION

Control actions in semiconductor power converters is executed exclusively through switching, driven by pulse width modulation (PWM) modules. Although PWM is widely regarded as the heart of modern converters [1], it is often treated as a black box or overlooked at the macro level. In doing so, the several degrees of freedom available for a PWM module are neglected. Some of these features can have a profound impact on dynamic system performance. The work in [2] reviews some of the principal PWM schemes for switching converters, listed in Figure 1.

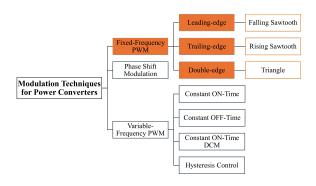


Fig. 1. Classification of PWM techniques for power converters. The high-lighted fixed-frequency modulation methods are within the scope of the paper.

While a PWM module by itself does not possess intrinsic "dynamics" (i.e., it does not store energy), it is more than a "duty cycle-to-switching function generator." The chosen modulation strategy may critically impact the performance of a converter. Factors such as the periodic carrier $v_{\rm c}(t)$, the

(carrier) switching frequency f_s , quantization, the sampling strategy, the noise response, or the intrinsic propagated delays, among others, may influence severely the effectiveness of control designs and closed-loop performance [1], [3], [4]. Although a PWM module compounds with the compensation network and the plant's power-stage, affecting the overall gain and phase-delay profiles, a PWM is often overlooked and treated as a static gain in the analysis of switching converters.

Recently, there has been a renewed interest in modeling the dynamic behavior of power converters and their control systems in detail. For example, the increasing share of converters in bulk power systems [5] has propelled this topic again, as converter-interfaced generation is said to be "controls dominated," in contrast with synchronous generators whose dynamic responses are dominated by inertia [6]. Capturing conventionally neglected behaviors, such as that of PWM blocks, may help improve the general accuracy of mathematical models of converter devices.

As most converter control systems now operate on digital microcontrollers in a sampled-data fashion, DT modeling is a natural approach and an alternative to traditional continuous-time (CT) averaged representation. DT modeling is well suited to capture behaviors that are difficult to represent through CT averaged models, leading to improved accuracy for both low-and high-frequency system dynamics.

The exploration of DT models of power converters is not entirely new. While CT average modeling was being formally developed [7], DT modeling emerged as shown in [8] and [9]. These foundational works introduced a sampled-data approach to design switching regulators with special attention in the explanatory properties of the models for high-frequency analysis. [10] provides a unified general framework for this sampled-data approach, offering a method to represent converters as cyclically switched systems and giving systematic steps for deriving DT small-signal models.

Under this ground, [11] makes use of the DT approach to discuss the PWM influence and delay effects on digitally controlled converters. In the same line, [12] and [13] analyze the stability implications of trailing- versus leading-edge PWM in classic converter topologies via DT modeling. The authors in [2], [14] propose an analytical framework to derive large- and small-signal models for a variety of converter topologies under

both fixed- and variable-frequency modulation schemes. [15] introduces a hybrid frequency-domain model that combines CT averaging of the converter and controller dynamics with a DT representation of the modulation scheme. [16] presents a bifurcation behavior analysis on voltage-mode control (VMC) for buck converters under various PWM schemes.

Although these recent studies have discussed the influence of modulation schemes on converter response, most focus exclusively on single-edge PWM, largely ignoring the equally widespread double-edge strategy. Additionally, the recent literature does not explicitly establish the distinctions between DT representations and the discretized CT averaged models, offering little insight into the practical advantages that purely discrete formulations might provide.

To address these gaps, this work systematically investigates how single-edge and double-edge PWM strategies affect the DT modeling and closed-loop stability of switching converters, in particular, a boost DC-DC converter. We develop a rigorous mathematical framework capable of deriving large- and small-signal discrete-time models for various PWM strategies. Using a digitally compensated boost converter as a representative case, the models are analyzed both in open- and closed-loop configurations, and results are compared against traditional discretized CT averaged models. Nonlinear simulations validate the analytical findings, underscoring the importance of PWM-aware modeling in achieving sought performance in DC-DC converter control systems.

The rest part of this paper is structured as follows. Section II reviews the fundamental concepts concerning PWM modules and the derivation of a DT model for a modulation strategy. The derived models and assumptions for the case of study are presented in Section III. The theoretical analysis and the simulation results are discussed in Section IV. Section V concludes the work and outlines future research directions.

II. GENERALIZED DT MODELING FRAMEWORK

A. Overview of PWM Techniques

$$v_c(t) \underset{v_m(t)}{\underset{m \leftarrow m}{\text{MMM}}} \underbrace{\qquad \qquad q(t)}$$

Fig. 2. Analog PWM generator using an op amp comparator.

Fixed-frequency PWM is the most widely used modulation technique. It operates by comparing a periodic carrier signal $v_c(t)$, generated at a fixed switching frequency, f_s , with a modulation signal, $v_m(t)$. This binary comparison yields the PWM control signal q(t), which determines the converter's switches conduction state. In DT modeling, f_s , is typically synchronized with the sampling frequency f_{samp} , i.e., $f_s = f_{\text{samp}}$, simplifying the model, accurately capturing switching dynamics, and avoiding undersampling ($f_{\text{samp}} < f_s$) [3].

A purely analog comparison between the modulating signal and the carrier leads to a naturally sampled pulse width modulation (NSPWM), where the information carried by the pulses encodes the low frequency content of $v_m(t)$. In digital

systems, the modulation process relies on ADC/DAC converters, where $v_m\left(t\right)$ is sampled. The sampled version $v_m\left(k\right)$ is used in the comparison against v_c to generate the control signal. This process introduces delays [3], which propagate through $q\left(t\right)$, affecting the dynamic performance of the converter. When $v_m\left(t\right)$ is sampled at regular intervals, remaining constant between samples (zero-order hold), this method is referred to as uniformly sampled pulse width modulation (USPWM) [4]. USPWM is the most common modulation strategy in converters with a digital control system.

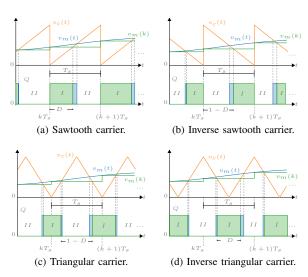


Fig. 3. Fixed-frequency PWM generation schemes for different carriers $v_c(t)$.

PWM schemes can be classified according to the carrier signal $v_c(t)$ into single-edge and double-edge techniques, as illustrated in Figure 3. In single-edge modulation, a sawtooth carrier produces either trailing-edge switching (positive ramp) or leading-edge switching (negative ramp, i.e., inverse sawtooth wave). In contrast, double-edge modulation employs a triangular carrier waveform, which may be symmetric (isosceles triangular wave) or asymmetric (scalene triangular wave). This paper focuses exclusively on symmetric triangular carriers, as they are the most commonly used in commercial applications. We want to underline that the choice among different carrier types has appreciable effects on converter operation, which are omitted in averaged models.

Next, we discuss a converter modeling framework that implicitly accounts for the effects of the PWM strategy. The resulting models represent both large- and small-signal behavior of a power converter.

B. Analytical Large-Signal Model

For our purposes, a converter is defined as an interconnection of elementary components: sources, linear passive elements, and switches. Switches are assumed to be ideal, i.e., an on-switch behaves as an ideal short circuit, while an offswitch is modeled as an ideal open circuit.

Suppose a converter has m controllable switches and, therefore, $n:=2^m$ possible configurations. The state of the $k{\rm th}$

switch is given by $q_k(t) \in \{0,1\}$. The vector $\mathbf{q}(t) \in \{0,1\}^m$ captures the on-off states of all switches at time t.

A configuration is set by a fixed switch state, i.e., a specific value of q(t) and is described as an linear time-invariant (LTI) system. For the ℓ th configuration, $\ell=1,\ldots,n$, the converter dynamics are given by the state-space representation:

$$\dot{\boldsymbol{x}}(t) = \boldsymbol{A}^{(\ell)} \boldsymbol{x}(t) + \boldsymbol{B}^{(\ell)} \boldsymbol{u}(t),
\boldsymbol{y}(t) = \boldsymbol{C}^{(\ell)} \boldsymbol{x}(t) + \boldsymbol{D}^{(\ell)} \boldsymbol{u}(t),$$
(1)

where $\boldsymbol{x} \in \mathbb{R}^d$ is the state vector (e.g., capacitor voltages and inductor currents), $\boldsymbol{u} \in \mathbb{R}^p$ the exogenous signal vector (e.g., source voltages or currents and disturbances), $\boldsymbol{y} \in \mathbb{R}^q$ the desired outputs, and $\boldsymbol{\mathcal{C}}_\ell := \left(\boldsymbol{A}^{(\ell)}, \boldsymbol{B}^{(\ell)}, \boldsymbol{C}^{(\ell)}, \boldsymbol{D}^{(\ell)}\right)$ the configuration matrices, which depend on the circuit parameters and the particular value of $\boldsymbol{q}(t)$ that "fixes" the configuration.

Let $\sigma_{\ell} \colon \mathbb{R} \times \mathbb{R}^{d} \times \mathbb{R}^{p} \times \{0,1\}^{m} \to \{0,1\}$ be a state-dependent indicator function, i.e., $\sigma_{\ell}(t, \boldsymbol{x}, \boldsymbol{u}, \boldsymbol{q})$. σ_{ℓ} determines the active converter configuration at time t. The overall "ensemble" dynamics of the system, or large-signal model, is

$$\dot{\boldsymbol{x}}(t) = \sum_{\ell=1}^{n} \left(\boldsymbol{A}^{(\ell)} \boldsymbol{x}(t) + \boldsymbol{B}^{(\ell)} \boldsymbol{u}(t) \right) \sigma_{\ell}(t, \boldsymbol{x}, \boldsymbol{u}, \boldsymbol{q}),$$

$$\boldsymbol{y}(t) = \sum_{\ell=1}^{n} \left(\boldsymbol{C}^{(\ell)} \boldsymbol{x}(t) + \boldsymbol{D}^{(\ell)} \boldsymbol{u}(t) \right) \sigma_{\ell}(t, \boldsymbol{x}, \boldsymbol{u}, \boldsymbol{q}).$$
(2)

The model in (2) is a piecewise CTLTI nonlinear system that captures the converter's behavior under different switching configurations. Because states normally correspond to capacitor voltages and inductor currents, the model has continuous states with discontinuous derivatives [2], which is a particular characteristic of converter dynamics. A given PWM scheme affects the indicator function $\sigma_{\ell}(t, \boldsymbol{x}, \boldsymbol{u}, \boldsymbol{q})$, which changes the state and output equations as seen in (2).

To illustrate the DT modeling approach, consider a generic power converter operating at a constant switching frequency $f_s=1/T_s$, where the sampling interval $T_{\rm samp}$ is chosen to match the switching period, $T_{\rm samp}=T_s$. Let t=0 denote the beginning of a switching period. The system undergoes a finite number of configuration transitions, denoted by L, representing the number of switching events within a period. The corresponding switching instants are defined as $\{t_\ell\}_{\ell=1}^L$, where $0 < t_\ell < T_s$. For notation consistency, let $t_0 := 0$ and $t_{L+1} := T_s$. The timing of the switching instants is determined by the particular PWM strategy (cf, Figure 3). Specifically, a transition from configuration $\mathcal{C}_{\ell-1}$ to \mathcal{C}_{ℓ} occurs at switching instant t_ℓ . The duration of each configuration interval is given by $\Delta t_\ell := t_{\ell+1} - t_\ell$, representing the time interval during which the system remains in configuration \mathcal{C}_ℓ .

As an example, in Figure 4, L=4. The original configuration is \mathcal{C}_0 , maintained for $\Delta t_0=t_1-t_0$ seconds. At $t=t_1$, the circuit topology changes to \mathcal{C}_1 , until a new configuration change occurs at $t=t_2$. The last transition happens at $t=t_4$. The circuit operates in mode \mathcal{C}_4 until $t=t_5=T_s$. At the sampling instants, measurements are taken (i.e., the modulating signal is sampled). During the commutation times,

the external inputs to the system are assumed constant, in accordance with the Zero-Order Hold (ZOH) assumption.

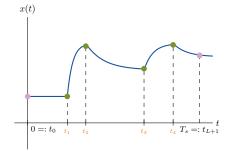


Fig. 4. Illustration of the DT modeling paradigm.

Without loss of generality, suppose that a converter transitions from configuration C_0 to C_1 between t_0 and t_1 . The states at each time are related by

$$\boldsymbol{x}(t_1) = \exp\left(\boldsymbol{A}^{(0)}\Delta t_0\right)\boldsymbol{x}(t_0)$$
$$+ \int_{t_0}^{t_1} \exp\left(\boldsymbol{A}^{(0)}(\Delta t_0 - \tau)\right)\boldsymbol{B}^{(0)}\boldsymbol{u}(\tau) d\tau.$$

The states at t_1 become the initial states for the next transition. Repeating this procedure sequentially for all subintervals yields a DT mapping of the form

$$x(k+1) = A_d x(k) + B_d u(k),$$

$$y(k) = C_d x(k) + D_d u(k),$$
(3)

where k indexes the switching period and

$$\mathbf{A}_{d} = \prod_{\ell=0}^{L} \exp\left(\mathbf{A}^{(\ell)} \Delta t_{\ell}\right),$$

$$\mathbf{B}_{d} = \sum_{\ell=0}^{L} \left(\prod_{j=\ell+1}^{n} \exp\left(\mathbf{A}^{(j)\Delta t_{j}}\right)\right) \mathbf{\Gamma}\left(\ell\right), \qquad (4)$$

$$\mathbf{C}_{d} = \mathbf{C}^{(L)},$$

$$\mathbf{D}_{d} = \mathbf{D}^{(L)}.$$

with
$$\Gamma(\ell) := \left(\boldsymbol{A}^{(\ell)} \right)^{-1} \left(\exp \left(\boldsymbol{A}^{(\ell)} \, \Delta t_{\ell} \right) - \boldsymbol{I} \right) \boldsymbol{B}^{(\ell)}$$
.

Although the model in (3) has a "state-space-like" structure, the matrices (A_d, B_d) are generally nonlinear, as they depend on the circuit configuration and the PWM scheme. As a result, the model is nonlinear in the control inputs. However, this DT model, derived under ZOH assumption, captures the state evolution exactly at $\{t_\ell\}_{\ell=0}^{L+1}$, with no numerical approximations in the discretization [8].

C. Analytical Small-Signal Model

A DT small-signal model can be derived by linearizing (3) through a Taylor series expansion around a nominal cyclic steady-state operating point [10]. Define

$$f(k, x, u) := A_d x(k) + B_d u(k) = x(k+1),$$

$$g(k, x, u) := C_d x(k) + D_d u(k) = y(k).$$
(5)

 $\label{eq:table_interpolation} TABLE\ I$ State-space Matrices for Boost Converter.

Matrix	Expression
$A^{(1)}$	$ \kappa \begin{bmatrix} -R_L/kL & 0 \\ 0 & -1/CR_{Load} \end{bmatrix} $ $ \kappa \begin{bmatrix} -(R_L + R_C)/L - R_LR_C/R_{Load}L & -1/L \\ 1/C & -1/CR_{Load} \end{bmatrix} $
$A^{(2)}$	$\kappa \begin{bmatrix} -(R_L + R_C)/L - R_L R_C/R_{Load} L & -1/L \\ 1/C & -1/C R_{Load} \end{bmatrix}$
\boldsymbol{B}	$\begin{bmatrix} 1/L & 0 \end{bmatrix}^{ op}$
$oldsymbol{C}^{(1)}$	$\stackrel{\leftarrow}{\kappa} \begin{bmatrix} 0 & 1 \end{bmatrix} \\ \kappa \begin{bmatrix} R_C & 1 \end{bmatrix}$

A steady-state operating point (x_{ss}, u_{ss}) is such that $f(k, x_{ss}, u_{ss}) = x(k)$. Let δx and δu be small perturbations around (x_{ss}, u_{ss}) , and δy the resulting variation in the outputs. For sufficiently small disturbances, we have that

$$x - x_{ss} = \delta x$$
, $u - u_{ss} = \delta u$, $y - y_{ss} = \delta y$.

Next, we apply a Jacobian operator on f and g and evaluate the result at the steady-state operating point,

$$egin{aligned} ilde{m{A}}_d &:= rac{\partial m{f}}{\partial m{x}}igg|_{(m{x}_{ss},m{u}_{ss})}, & ilde{m{B}}_d &:= rac{\partial m{f}}{\partial m{u}}igg|_{(m{x}_{ss},m{u}_{ss})}, \ ilde{m{C}}_d &:= rac{\partial m{g}}{\partial m{x}}igg|_{(m{x}_{ss},m{u}_{ss})}, & ilde{m{D}}_d &:= rac{\partial m{g}}{\partial m{u}}igg|_{(m{x}_{ss},m{u}_{ss})}. \end{aligned}$$

The resulting matrices define the DT small-signal model:

$$\delta x (k+1) \approx \tilde{A}_{d} \delta x (k) + \tilde{B}_{d} \delta u (k),
\delta y (k) \approx \tilde{C}_{d} \delta x (k) + \tilde{D}_{d} \delta u (k).$$
(6)

III. APPLICATION CASE: BOOST CONVERTER

To illustrate the DT modeling approach developed in Section II, we analyze a boost converter, a common and scalable topology illustrated in Figure 5. The PWM signal governs the switching of Q, assumed to have negligible on-resistance, while the diode S is treated as ideal. We use the inductor current i_L and capacitor voltage v_C as states, $x := (i_L, v_C)$.

Assuming the converter operates in continuous conduction mode (CCM), only two circuit configurations are possible: Q on $(\ell=1)$ or off $(\ell=2)$. The corresponding state-space matrices are given in Table I, where $\kappa:=R_{Load}/(R_{Load}+R_C)$.

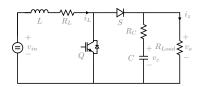


Fig. 5. Circuit diagram of a boost (step-up) converter.

We derive a large-signal DT model for the boost converter for various modulation schemes using (3) under the USPWM assumption. Table II lists expressions in terms of the steady-state duty cycle D and its complement D' = 1 - D.

The output vector $C^{(\ell)}$ varies depending on the circuit configuration at the sampling instant, due to the boost converter's

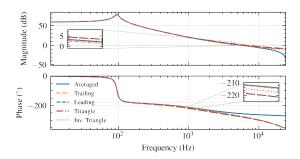


Fig. 6. Bode plot of the DT control-to-output transfer function $G_{vd_{dis}}(z)$.

discontinuous output voltage. Since $C^{(1)} \neq C^{(2)}$, the actual output vector is determined by the chosen PWM strategy, directly influencing the output equation $\boldsymbol{y}(t) = \boldsymbol{C}^{(\ell)} \boldsymbol{x}(t) = v_o$. For our converter, $\boldsymbol{y}(t) = \boldsymbol{C}^{(1)} \boldsymbol{x}(t)$ under trailing-edge and inverse triangular modulation, while $\boldsymbol{y}(t) = \boldsymbol{C}^{(2)} \boldsymbol{x}(t)$ under leading-edge and triangular modulation.

The DT small-signal model is represented by the pair $(\tilde{A}_d, \tilde{B}_d)$. For the boost converter, the small-signal system matrix is the same as in large-signal, i.e., $\tilde{A}_d = A_d$. However, the small-signal input vector \tilde{B}_d differs from its large-signal counterpart. The expressions in Table II are parametrized using $\alpha = ((A^{(1)} - A^{(2)})x_{ss} + (B^{(1)} - B^{(2)})v_{in})T_s$.

IV. NUMERICAL SIMULATIONS AND ANALYSIS

A. Analysis of open-loop control-to-output transfer function

The control-to-output transfer function, $G_{vd_{dis}}(z)$ represents the variation in the converter's voltage output \tilde{v}_o as a function of a control signal perturbation \tilde{d} . It is computed as

$$G_{vd_{dis}}(z) = \tilde{\boldsymbol{C}}_d(z\boldsymbol{I} - \tilde{\boldsymbol{A}}_d)^{-1}\tilde{\boldsymbol{B}}_d. \tag{7}$$

The frequency response of the four modulation schemes considered in this paper and the Tustin-discretized CT model at T_s are shown in Figure 6. The phase response between the CT averaged model and the DT models differs significantly at high frequencies. Trailing-edge strategy results in the highest phase margin (PM) (-74.55°) , whereas leading-edge and triangular carrier give lower values (-90.64°) and -102.47° , respectively). These PM values arise from the non-minimum phase nature of the boost converter. However, unlike the CT model, the DT models may be minimum-phase depending on the circuit parameters.

B. Control Design and Closed-Loop Performance Evaluation

To quantify how a DT model of a PWM impacts a closed-loop control strategy, consider a boost VMC scheme tuned to a 10° PM. This razor-thin margin represents a realistic worst-case scenario to evaluate robustness. We select a lead-lag network as a compensator. Tuning is done in two ways: first, without consideration of the modulation strategy (i.e., we employ the CT averaged model); and second, accounting for the PWM using a small-signal DT model.

Figure 8 shows nonlinear time-domain simulations of the boost converter for both trailing- and leading-edge PWM under

TABLE II

ANALYTICAL EXPRESSIONS FOR DISCRETE-TIME LARGE-SIGNAL AND SMALL-SIGNAL MODELS.

Carrier	$m{A}_d/ar{m{A}}_d$	B_d	$ $ \tilde{B}_d
Sawtooth	$\exp\left(\mathbf{A}^{(2)}D'T_s\right)\exp\left(\mathbf{A}^{(1)}DT_s\right)$	$\exp\left(\boldsymbol{A}^{(2)}D'T_{s}\right)\boldsymbol{\Gamma}(1)+\boldsymbol{\Gamma}(2)$	$\left \exp \left(\mathbf{A}^{(2)} D' T_s \right) \boldsymbol{\alpha} \right $
Inv. Sawtooth	$\exp\left(\mathbf{A}^{(1)}DT_{s}\right)\exp\left(\mathbf{A}^{(2)}D'T_{s}\right)$	$\exp\left(\mathbf{A}^{(1)}DT_{s}\right)\mathbf{\Gamma}(2)+\mathbf{\Gamma}(1)$	$\exp \left(\mathbf{A}^{(1)}DT_{s} \right) \boldsymbol{\alpha}$
Triangle	$\exp\left(\mathbf{A}^{(1)}D\frac{\dot{T_s}}{2}\right)\exp\left(\dot{\mathbf{A}}^{(2)}D'\dot{T_s}\right)\exp\left(\dot{\mathbf{A}}^{(1)}D\frac{T_s}{2}\right)$	$\exp\left(\boldsymbol{A}^{(1)}D\frac{T_s}{2}\right)\exp\left(\boldsymbol{A}^{(2)}D'T_s\right)\boldsymbol{\Gamma}(1) + \exp\left(\boldsymbol{A}^{(1)}D\frac{T_s}{2}\right)\boldsymbol{\Gamma}(2) + \boldsymbol{\Gamma}(1)$	$\exp \left(\mathbf{A}^{(1)} D \frac{T_s}{2} \right) \boldsymbol{\alpha}$
Inv. Triangle	$\exp\left(\mathbf{A}^{(2)}D'\frac{T_s}{2}\right)\exp\left(\mathbf{A}^{(1)}DT_s\right)\exp\left(\mathbf{A}^{(2)}D'\frac{T_s}{2}\right)$	$\exp\left(\mathbf{A}^{(2)}D'\frac{T_s}{2}\right)\exp\left(\mathbf{A}^{(1)}DT_s\right)\mathbf{\Gamma}(2) + \exp\left(\mathbf{A}^{(2)}D'\frac{T_s}{2}\right)\mathbf{\Gamma}(1) + \mathbf{\Gamma}(2)$	$\exp\left(\mathbf{A}^{(2)}D'\frac{T_s}{2}\right)\boldsymbol{\alpha}$

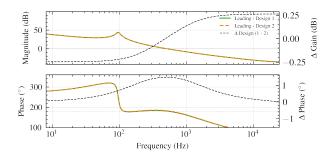


Fig. 7. Uncompensated loop gain under two compensators (leading-edge DT).

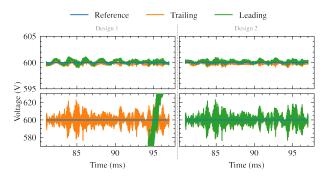


Fig. 8. Closed-loop output voltage v_o of the VMC-controlled boost converter under (top row) normal operation and (bottom row) noisy conditions. Left and right columns correspond to different controller designs, as indicated.

nominal conditions and a sensing-failure scenario (added measurement noise). Although the two controllers behave similarly in normal operation, the leading-edge loop, whose CT model overestimates the PM, becomes unstable when noise affects the system. The revised compensator (Design 2), synthesized using a DT model, accounts for the true phase characteristics, and restores a robust, stable performance.

V. CONCLUSIONS AND FUTURE WORK

Our results demonstrate that modulation schemes captured by DT modeling significantly impact converter dynamics, revealing differences often overlooked by the CT averaged model. For the boost converter, trailing-edge modulation performs the best, whereas leading-edge and triangular carriers yield degraded behavior under extreme conditions. These differences underscore the importance of employing more descriptive models to avoid biases that may lead to erroneous stability assessments, suboptimal control design, or undesired performance (as seen with the leading-edge modulation). The proposed approach lays the groundwork for incorporating more descriptive models into grid-tied applications, offering

dynamic performance benefits in PV systems, where cascaded PWM-based DC-DC stages and inverters are deeply integrated.

APPENDIX

Typical PV boost converter parameters are used with rated output power $P_{out}=4\,\mathrm{kW}$, switching frequency $f_s=50\,\mathrm{kHz}$, input voltage $V_{in}=370\,\mathrm{V}$, output voltage $V_o=600\,\mathrm{V}$, $L=3.5\,\mathrm{mH}$, $R_L=100\,\mathrm{m}\Omega$, $C=3.3\,\mathrm{mF}$, $R_C=10\,\mathrm{m}\Omega$.

REFERENCES

- D. Holmes and T. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice, ser. IEEE Press Series on Power and Energy Systems. Wiley. 2003.
- [2] S. Kapat and P. T. Krein, "A Tutorial and Review Discussion of Modulation, Control and Tuning of High-Performance DC-DC Converters Based on Small-Signal and Large-Signal Approaches," *IEEE Open J. Power Electron.*, vol. 1, pp. 339–371, 2020.
- [3] R. W. Erickson and D. Maksimović, Fundamentals of Power Electronics, 3rd ed. Springer, 2020.
- [4] L. Corradini, D. Maksimović, P. Mattavelli, and R. Zane, Digital Control of High-Frequency Switched-Mode Power Converters. Wiley, 2015.
- [5] PES-TR113, Simulation Methods, Models, and Analysis Techniques to Represent the Behavior of Bulk Power System Connected Inverter-Based Resources.
- [6] F. Dörfler and D. Groß, "Control of Low-Inertia Power Systems," Annual Review of Control, Robotics, and Autonomous Systems, vol. 6, pp. 415– 445, May 2023.
- [7] S. M. Ćuk, "Modeling, Analysis, and Design of Switching Converters," Ph.D. dissertation, Caltech, Pasadena, CA, 1977.
- [8] Packard, D. J., "Discrete Modeling and Analysis of Switching Regulators," Ph.D. dissertation, Caltech, Pasadena, CA, 1976.
- [9] A. R. Brown and R. Middlebrook, "Sampled-data Modeling of Switching Regulators," in 1981 IEEE Power Electronics Specialists Conference, 1981, pp. 349–369.
- [10] G. C. Verghese, M. E. Elbuluk, and J. G. Kassakian, "A General Approach to Sampled-Data Modeling for Power Electronic Circuits," *IEEE Trans. Power Electron.*, vol. PE-1, no. 2, pp. 76–89, Apr. 1986.
- [11] D. Maksimovic and R. Zane, "Small-signal Discrete-time Modeling of Digitally Controlled PWM Converters," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2552–2556, Nov. 2007.
- [12] X. Li, X. Ruan, Q. Jin, M. Sha, and C. K. Tse, "Approximate Discrete-Time Modeling of DC–DC Converters with Consideration of the Effects of Pulse Width Modulation," *IEEE Trans. Power Electron.*, vol. 33, no. 8, Aug. 2018.
- [13] X. Li, X. Ruan, X. Xiong, M. Sha, and C. K. Tse, "Approximate Discrete-Time Small-Signal Models of DC–DC Converters with Consideration of Practical Pulsewidth Modulation and Stability Improvement Methods," *IEEE Trans. Power Electron.*, vol. 34, no. 5, May 2019.
- [14] S. Kapat, "An Analytical Approach of Discrete-Time Modeling of Fixed and Variable Frequency Digital Modulation," in 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Jun. 2021.
- [15] Y. Chen, B. Zhang, Y. Jiang, F. Xie, D. Qiu, and Y. Chen, "A General Frequency-Domain Model of Trailing-Edge and Leading-Edge Carrier pwm DC–DC Converter Based on Hybrid Continuous and Discrete-Time Descriptions," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4175–4187, 2021.
- [16] S. Zhou, G. Zhou, M. He, S. Mao, H. Zhao, and G. Liu, "Stability Effect of Different Modulation Parameters in Voltage-Mode PWM Control for CCM Switching DC–DC Converter," *IEEE Trans. Transport. Electrific.*, vol. 10, no. 2, pp. 2408–2422, 2024.