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Project (1) DSP48A1

1-RTL:

```
module reg_mux (CLK,RST,d,q,E);
parameter RSTTYPE="SYNC";
parameter PYPLINE=1;
parameter N=18 ;
input [N-1:0]d;
input CLK,RST,E;
output reg [N-1:0]q;
reg  [N-1:0] q_reg;

generate
    if (RSTTYPE=="SYNC") begin
        always @(posedge CLK ) begin
            if (RST) begin
                q_reg<=0;
            end
            else begin
               if (E) begin
                q_reg<=d;
               end
               else
                q_reg<=0;
            end
            q<=(PYPLINE==1)? q_reg : d ;
        end
    end
    else begin
        always @(posedge CLK,posedge RST) begin
            if (RST) begin
                q_reg<=0;
            end
            else begin
                if (E) begin
                    q_reg<=d;
                end
                else
                q_reg<=0;
            end
        q<=(PYPLINE==1)? q_reg : d ;
        end
    end
endgenerate
endmodule
```

M: > kareem wasem digital design > Digital Design Diploma > projects > project1 > codes > DSP48A1.v

```v
module DSP48A1 (CLK,OPMODE,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP,RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP,BCOUT,PCIN,PCOUT,A,B,C,D,CARRYIN,M,P,CARRYOUT,CARRYOUTF,BCIN);
parameter A0REG=0,A1REG=1,B0REG=0,B1REG=1,CREG=1,DREG=1,MREG=1,PREG=1,CARRYINREG=1,CARRYOUTREG=1,OPMODEREG=1;
parameter CARRYINSEL=1,B_INPUT=1,RSTTYPE="SYNC";
input [17:0]A,B,D,BCIN;
input [47:0]C,PCIN;
input CARRYIN,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP;
input RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP,CLK;
input [7:0]OPMODE;
output [35:0]M;
output [47:0]P,PCOUT;
output [17:0]BCOUT;
output CARRYOUT,CARRYOUTF;
wire [17:0]D_w,A_w,B_mux,B_w,add_sub1,add_sub1_w,B1_reg_w,A1_reg_w;
wire [47:0]C_w,mux_x,mux_z,add_sub2_w,P_w;
wire [35:0]mult_w,mult1_w;
wire [7:0]OPMODE_w;
wire carryin0_w,CIN,carry_w,CARRYOUT_reg;
reg_mux #(.RSTTYPE(RSTTYPE),.PYPLINE(DREG),.N(18)) D0 (.d(D),.CLK(CLK),.RST(RSTD),.E(CED),.q(D_w));
reg_mux #(.RSTTYPE(RSTTYPE),.PYPLINE(A0REG),.N(18)) A0 (.d(A),.CLK(CLK),.RST(RSTA),.E(CEA),.q(A_w));
reg_mux #(.RSTTYPE(RSTTYPE),.PYPLINE(CREG),.N(48)) C0 (.d(C),.CLK(CLK),.RST(RSTC),.E(CEC),.q(C_w));
assign B_mux=(B_INPUT==1)? B :(B_INPUT==0)? BCIN : 0;
reg_mux #(.RSTTYPE(RSTTYPE),.PYPLINE(B0REG),.N(18)) B0 (.d(B_mux),.CLK(CLK),.RST(RSTB),.E(CEB),.q(B_w));
reg_mux #(.RSTTYPE(RSTTYPE),.PYPLINE(OPMODEREG),.N(8)) opmode0 (.d(OPMODE),.CLK(CLK),.RST(RSTOPMODE),.E(CEOPMODE),.q(OPMODE_w));
assign add_sub1=(OPMODE_w[6]==0)? (D_w + B_w) : (D_w - B_w);
assign add_sub1_w=(OPMODE_w[4]==0)? B_w : add_sub1;
reg_mux #(.RSTTYPE(RSTTYPE),.PYPLINE(B1REG),.N(18)) B1 (.d(add_sub1_w),.CLK(CLK),.RST(RSTB),.E(CEB),.q(B1_reg_w));
reg_mux #(.RSTTYPE(RSTTYPE),.PYPLINE(A1REG),.N(18)) A1 (.d(A_w),.CLK(CLK),.RST(RSTA),.E(CEA),.q(A1_reg_w));
assign mult_w=A1_reg_w * B1_reg_w ;
reg_mux #(.RSTTYPE(RSTTYPE),.PYPLINE(MREG),.N(36)) M0 (.d(mult_w),.CLK(CLK),.RST(RSTM),.E(CEM),.q(mult1_w));
assign M=mult1_w;
assign mux_x=(OPMODE_w[1:0]==0)? 0 :(OPMODE_w[1:0]==1)? {12'b0,mult1_w} : (OPMODE_w[1:0]==2)? P_w : {D_w[11:0],A1_reg_w[17:0],B1_reg_w[17:0]};
assign mux_z=(OPMODE_w[3:2]==0)? 0 :(OPMODE_w[3:2]==1)? PCIN : (OPMODE_w[3:2]==2)? P_w : C_w ;
assign carryin0_w=(CARRYINSEL==1)? OPMODE_w[5] : (CARRYINSEL==0)? CARRYIN : 0;
reg_mux #(.RSTTYPE(RSTTYPE),.PYPLINE(CARRYINREG),.N(1)) carryin0 (.d(carryin0_w),.CLK(CLK),.RST(RSTCARRYIN),.E(CECARRYIN),.q(CIN));
assign {carry_w,add_sub2_w}=(OPMODE_w[7]==0)? mux_z+mux_x+CIN : mux_z - (mux_x + CIN);
reg_mux #(.RSTTYPE(RSTTYPE),.PYPLINE(PREG),.N(48)) P0 (.d(add_sub2_w),.CLK(CLK),.RST(RSTP),.E(CEP),.q(P_w));
assign P=P_w;
assign PCOUT=P_w;
reg_mux #(.RSTTYPE(RSTTYPE),.PYPLINE(CARRYOUTREG),.N(1)) cout0 (.d(carry_w),.CLK(CLK),.RST(RSTCARRYIN),.E(CECARRYIN),.q(CARRYOUT_reg));
assign CARRYOUT=CARRYOUT_reg;
assign CARRYOUTF=CARRYOUT_reg;
assign BCOUT=B1_reg_w;
endmodule
```

2-testbench:

```
module DSP48A1_tb ();
    reg [17:0]A,B,D,BCIN,BCOUT_exp;
    reg [47:0]C,PCIN,P_exp;
    reg CARRYIN,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP,CARRYOUT_exp;
    reg RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP,CLK;
    reg [7:0]OPMODE;
    reg [35:0]M_exp;
    wire [35:0]M;
    wire [47:0]P,PCOUT;
    wire [17:0]BCOUT;
    wire CARRYOUT,CARRYOUTF;
    DSP48A1 #(.CARRYINSEL(0)) DSP1 (.*);
    initial begin
     CLK=0;
     forever #2 CLK=~CLK;
    end
    initial begin
        RSTA  = 1;      CEA   = 0;
        RSTB  = 1;      CEB       = 0;
        RSTC  = 1;      CEC       = 0;
        RSTD  = 1;      CED       = 0;
        RSTCARRYIN = 1; CECARRYIN = 0;
        RSTM       = 1; CEM       = 0;
        RSTOPMODE  = 1; CEOPMODE  = 0;
        RSTP       = 1; CEP       = 0;
        A=0; B=0; C=0; D=0; CARRYIN=0; OPMODE=0; PCIN=0; BCIN=0;
        M_exp=0; P_exp=0; BCOUT_exp=0;
        @(negedge CLK);
        if(M != M_exp || P != P_exp || BCOUT != BCOUT_exp) begin
            $display("Error in reset operation.");
        end
```

```
RSTA  = 0;      CEA   = 1;
RSTB  = 0;      CEB       = 1;
RSTC  = 0;      CEC       = 1;
RSTD  = 0;      CED       = 1;
RSTCARRYIN = 0; CECARRYIN = 1;
RSTM       = 0; CEM       = 1;
RSTOPMODE  = 0; CEOPMODE  = 1;
RSTP       = 0; CEP       = 1;
OPMODE[4] = 1;
OPMODE[1:0] = 1;
OPMODE[3:2] = 0;
CARRYIN = 0;
OPMODE[6] = 0; D = 70; B = 30; A = 1;
BCOUT_exp    = 100;
M_exp        = 100;
P_exp        = 100;
CARRYOUT_exp = 0;
if(M != M_exp || P != P_exp || BCOUT != BCOUT_exp || CARRYOUT != CARRYOUT_exp) begin
    $display("Error in Pre-Adder Check operation. M=%0d,M_exp=%0d",M,M_exp);
    $display("P=%0d,P_exp=%0d,BCOUT=%0d,BCOUT_exp=%0d,CARRYOUT=%0d,CARRYOUT_exp=%0d",P,P_exp,BCOUT,BCOUT_exp,CARRYOUT,CARRYOUT_exp);
end
OPMODE[6]=1; D=50; B=20;
BCOUT_exp    = 30;
M_exp        = 30;
P_exp        = 30;
CARRYOUT_exp = 0;
repeat(4) @(negedge CLK);
if(M != M_exp || P != P_exp || BCOUT != BCOUT_exp || CARRYOUT != CARRYOUT_exp) begin
    $display("Error in Pre-Subtract Check operation. M=%0d,M_exp=%0d",M,M_exp);
    $display("P=%0d,P_exp=%0d,BCOUT=%0d,BCOUT_exp=%0d,CARRYOUT=%0d,CARRYOUT_exp=%0d",P,P_exp,BCOUT,BCOUT_exp,CARRYOUT,CARRYOUT_exp);
end
```

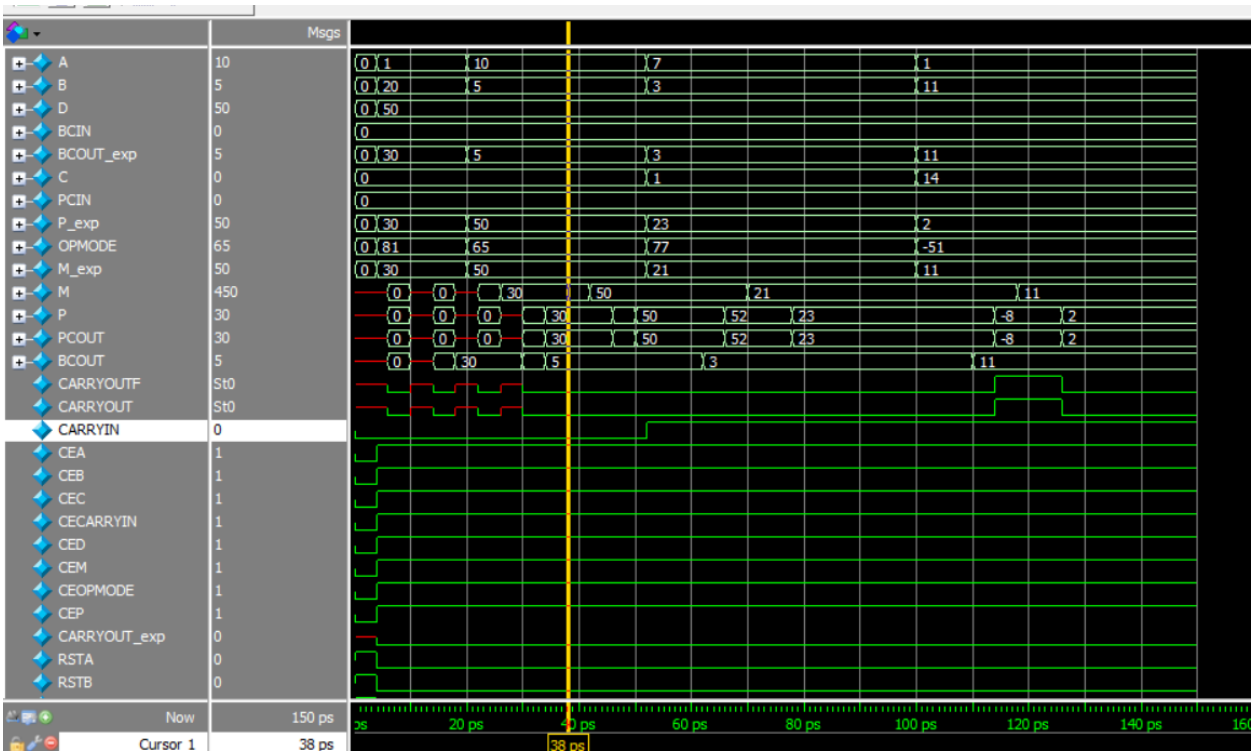
```
OPMODE[4] = 0;
A=10; B=5;
BCOUT_exp    = 5;
M_exp        = 50;
P_exp        = 50;
CARRYOUT_exp = 0;
repeat(8) @(negedge CLK);
if(M != M_exp || P != P_exp || BCOUT != BCOUT_exp || CARRYOUT != CARRYOUT_exp) begin
    $display("Error in multiplier Check operation. M=%0d,M_exp=%0d",M,M_exp);
    $display("P=%0d,P_exp=%0d,BCOUT=%0d,BCOUT_exp=%0d,CARRYOUT=%0d,CARRYOUT_exp=%0d",P,P_exp,BCOUT,BCOUT_exp,CARRYOUT,CARRYOUT_exp);
end
OPMODE[1:0]=1;
OPMODE[3:2]=3;
OPMODE[7]=0;
A=7;
B=3;
C=1;
CARRYIN=1;
BCOUT_exp    = 3;
M_exp        = 21;
P_exp        = 23;
CARRYOUT_exp = 0;
repeat(12) @(negedge CLK);
if(M != M_exp || P != P_exp || BCOUT != BCOUT_exp || CARRYOUT != CARRYOUT_exp) begin
    $display("Error in post-ADDER Check operation. M=%0d,M_exp=%0d",M,M_exp);
    $display("P=%0d,P_exp=%0d,BCOUT=%0d,BCOUT_exp=%0d,CARRYOUT=%0d,CARRYOUT_exp=%0d",P,P_exp,BCOUT,BCOUT_exp,CARRYOUT,CARRYOUT_exp);
end
```

```
91              OPMODE[7]=1;
92          A=1;
93          B=11;
94          C=14;
95          CARRYIN=1;
96          BCOUT_exp    = 11;
97          M_exp        = 11;
98          P_exp        = 2;
99          CARRYOUT_exp = 0;
100         repeat(12) @(negedge CLK);
101           if(M != M_exp || P != P_exp || BCOUT != BCOUT_exp || CARRYOUT != CARRYOUT_exp) begin
102             $display("Error in post-subtractor Check operation. M=%0d,M_exp=%0d",M,M_exp);
103             $display("P=%0d,P_exp=%0d,BCOUT=%0d,BCOUT_exp=%0d,CARRYOUT=%0d,CARRYOUT_exp=%0d",P,P_exp,BCOUT,BCOUT_exp,CARRYOUT,CARRYOUT_exp);
104         end
105           #2;
106         $stop;
107     end
108 endmodule
```

3-Do file:

```
1   vlib work
2   vlog DSP48A1.v DSP48A1_tb.v reg_mux.v
3   vsim -voptargs=+acc work.DSP48A1_tb
4   add wave *
5   run -all
6   #quit -sim
```

4-QuestaSim wave , transcript :




```
ModelSim> do run_DSP48A1.do
# ** Warning: (vlib-34) Library already exists at "work".
#
# Model Technology ModelSim ALTERA vlog 10.4b Compiler 2015.05 May 27 2015
# Start time: 21:52:27 on Mar 10,2025
# vlog -reportprogress 300 DSP48A1.v DSP48A1_tb.v reg_mux.v
# -- Compiling module DSP48A1
# -- Compiling module DSP48A1_tb
# -- Compiling module reg_mux
#
# Top level modules:
#       DSP48A1_tb
# End time: 21:52:27 on Mar 10,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# vsim -voptargs="+acc" work.DSP48A1_tb
# Start time: 21:52:27 on Mar 10,2025
# Loading work.DSP48A1_tb
# Loading work.DSP48A1
# Loading work.reg_mux
# ** Note: $stop    : DSP48A1_tb.v(106)
#    Time: 150 ps  Iteration: 0  Instance: /DSP48A1_tb
# Break in Module DSP48A1_tb at DSP48A1_tb.v line 106
```

No error messages in the transcript.

5-constraint file:

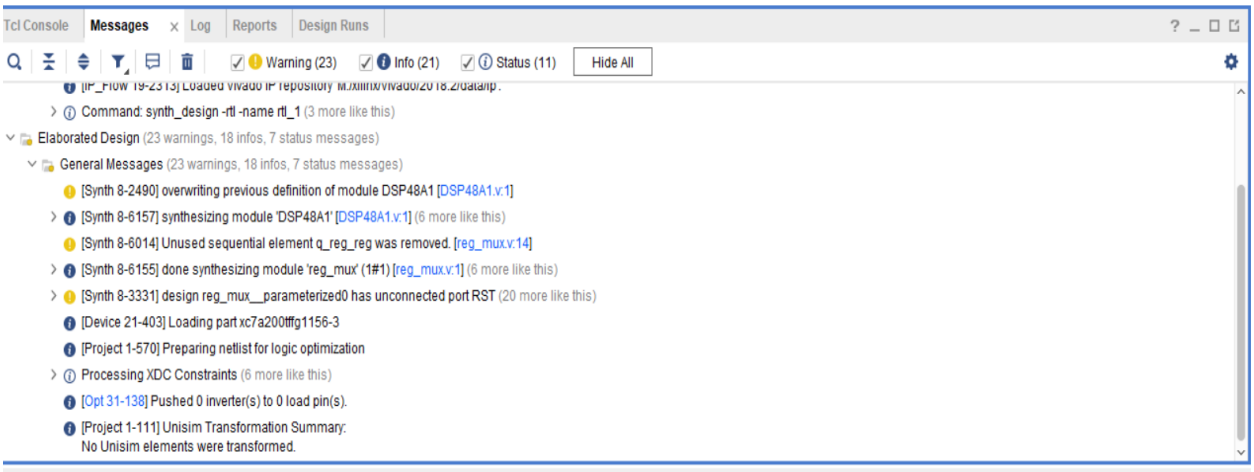
M: > kareem wasem digital design > Digital Design Diploma > projects > project1 > codes > constraints_DSP48A1.xdc

```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project

## Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports CLK]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]


## Switches
#set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports {sw[0]}]
#set_property -dict { PACKAGE_PIN V16   IOSTANDARD LVCMOS33 } [get_ports {sw[1]}]
#set_property -dict { PACKAGE_PIN W16   IOSTANDARD LVCMOS33 } [get_ports {sw[2]}]
#set_property -dict { PACKAGE_PIN W17   IOSTANDARD LVCMOS33 } [get_ports {sw[3]}]
#set_property -dict { PACKAGE_PIN W15   IOSTANDARD LVCMOS33 } [get_ports {sw[4]}]
#set_property -dict { PACKAGE_PIN V15   IOSTANDARD LVCMOS33 } [get_ports {sw[5]}]
#set_property -dict { PACKAGE_PIN W14   IOSTANDARD LVCMOS33 } [get_ports {sw[6]}]
#set_property -dict { PACKAGE_PIN W13   IOSTANDARD LVCMOS33 } [get_ports {sw[7]}]
#set_property -dict { PACKAGE_PIN V2    IOSTANDARD LVCMOS33 } [get_ports {sw[8]}]
#set_property -dict { PACKAGE_PIN T3    IOSTANDARD LVCMOS33 } [get_ports {sw[9]}]
#set_property -dict { PACKAGE_PIN T2    IOSTANDARD LVCMOS33 } [get_ports {sw[10]}]
#set_property -dict { PACKAGE_PIN R3    IOSTANDARD LVCMOS33 } [get_ports {sw[11]}]
#set_property -dict { PACKAGE_PIN W2    IOSTANDARD LVCMOS33 } [get_ports {sw[12]}]
#set_property -dict { PACKAGE_PIN U1    IOSTANDARD LVCMOS33 } [get_ports {sw[13]}]
#set_property -dict { PACKAGE_PIN T1    IOSTANDARD LVCMOS33 } [get_ports {sw[14]}]
#set_property -dict { PACKAGE_PIN R2    IOSTANDARD LVCMOS33 } [get_ports {sw[15]}]


## LEDs
#set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports {led[0]}]
#set_property -dict { PACKAGE_PIN E19   IOSTANDARD LVCMOS33 } [get_ports {led[1]}]
#set_property -dict { PACKAGE_PIN U19   IOSTANDARD LVCMOS33 } [get_ports {led[2]}]
#set_property -dict { PACKAGE_PIN V19   IOSTANDARD LVCMOS33 } [get_ports {led[3]}]
#set_property -dict { PACKAGE_PIN W18   IOSTANDARD LVCMOS33 } [get_ports {led[4]}]
#set_property -dict { PACKAGE_PIN U15   IOSTANDARD LVCMOS33 } [get_ports {led[5]}]
#set_property -dict { PACKAGE_PIN U14   IOSTANDARD LVCMOS33 } [get_ports {led[6]}]
```

And the rest of the file is #

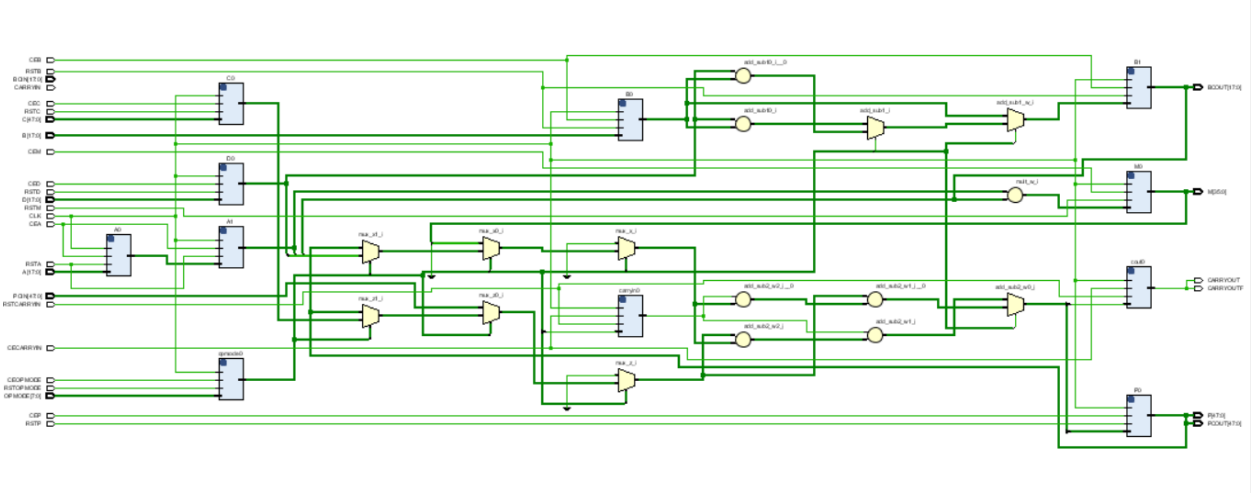
6-Elaboration:

Message tap:



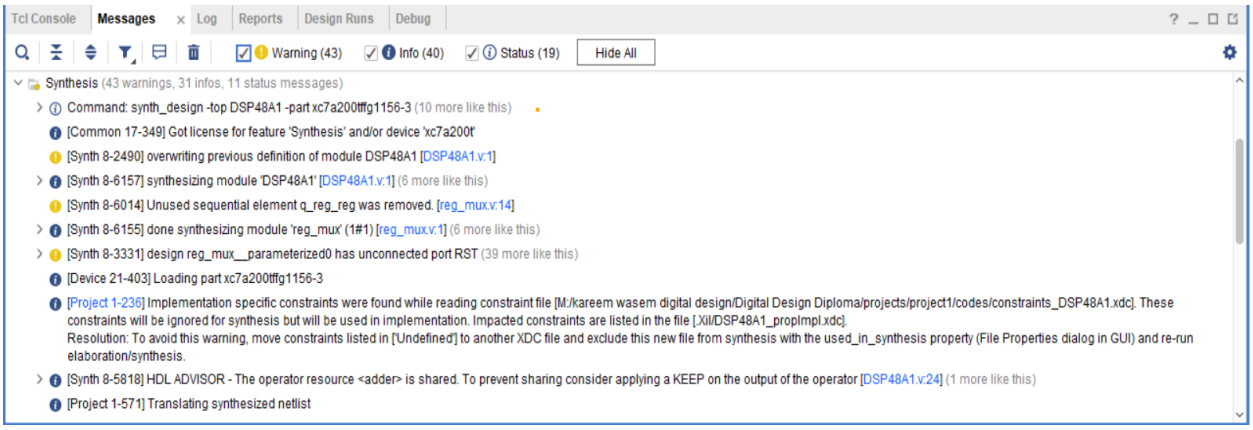
No critical warnings.

Schematic:



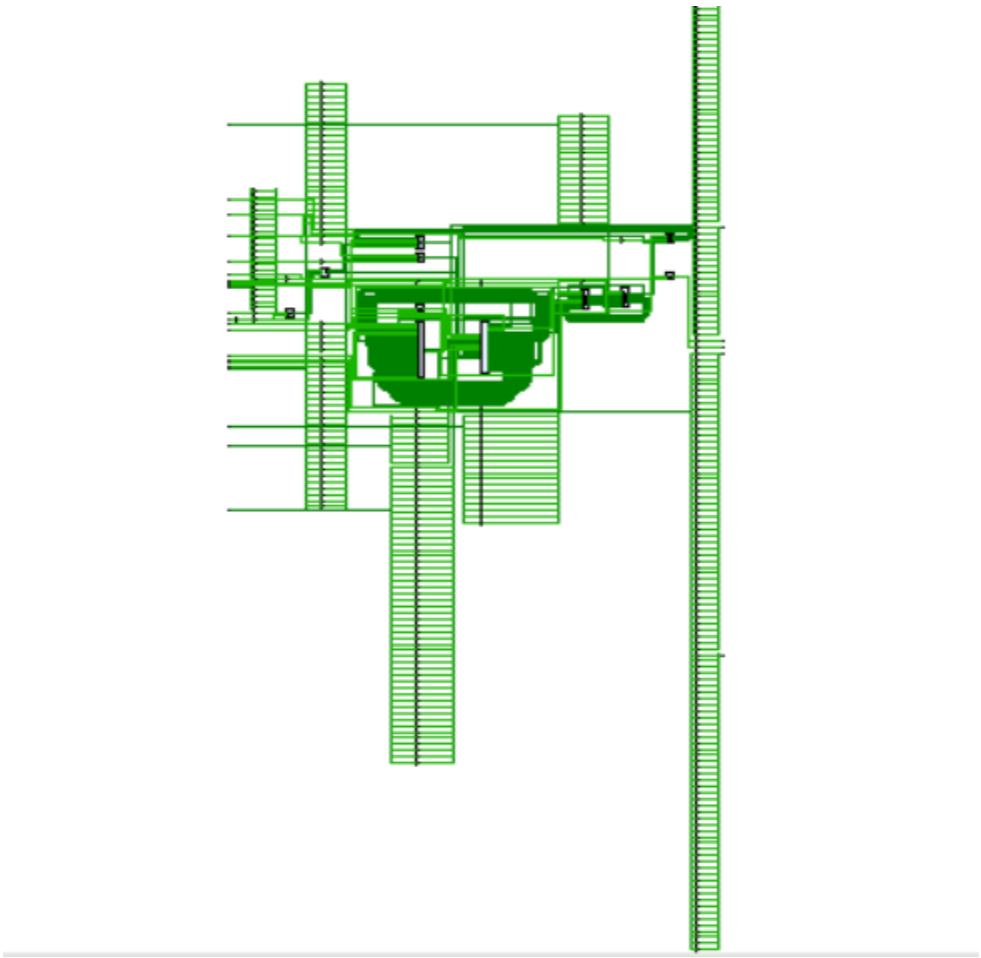
7-synthesis:

Message tab:

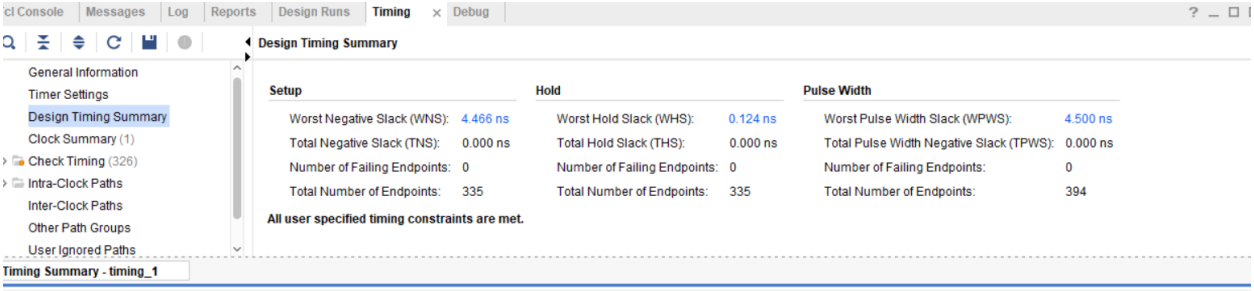


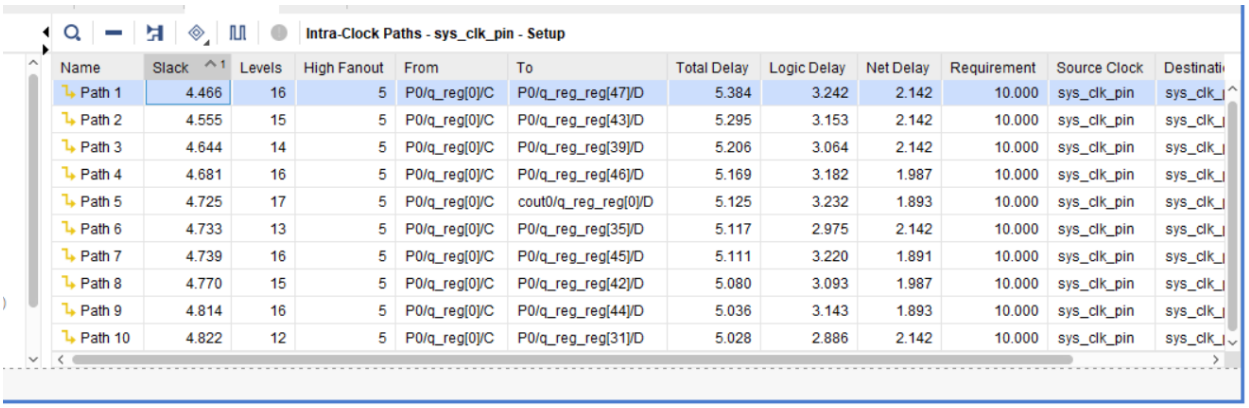
No critical warnings.

Schematic:

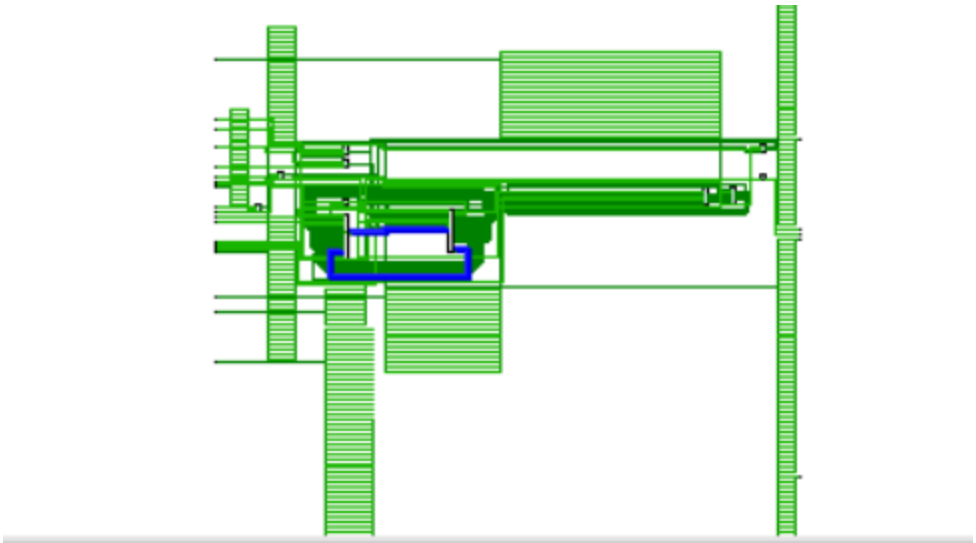


Timing report:



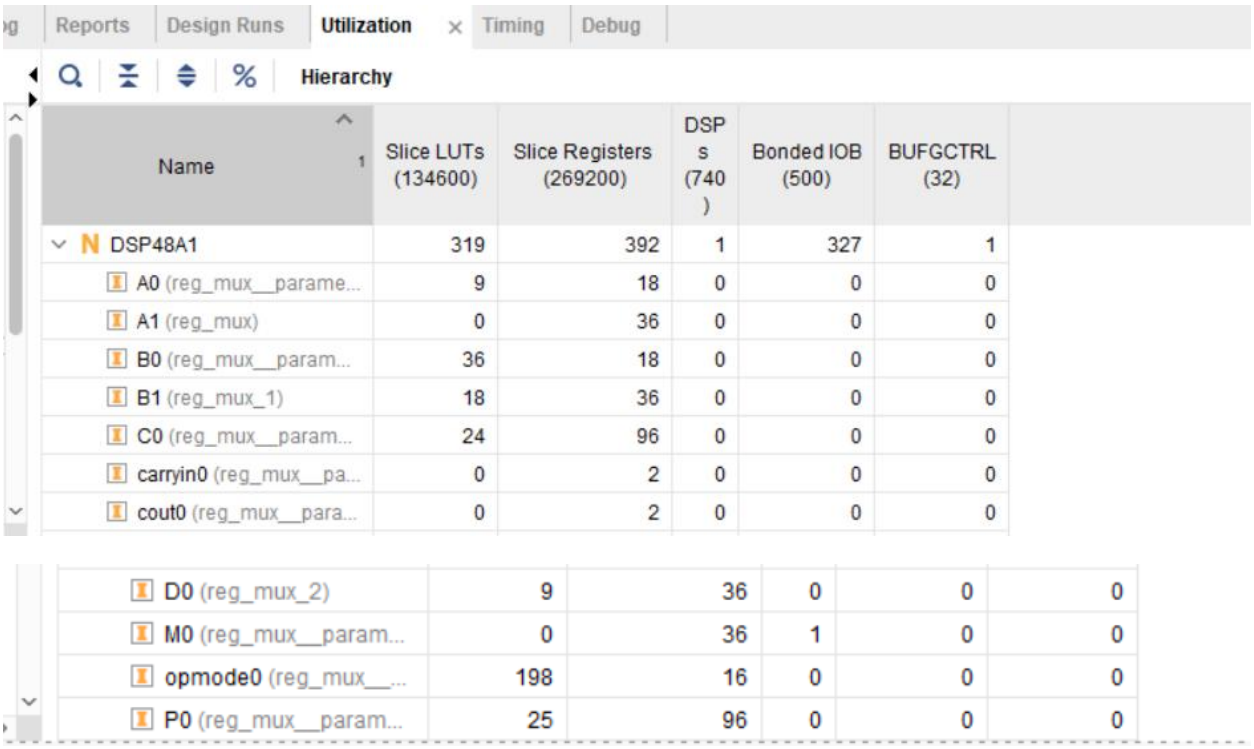


Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destinati
Path 1	4.466	16	5	P0/q_reg[0]/C	P0/q_reg_reg[47]/D	5.384	3.242	2.142	10.000	sys_clk_pin	sys_clk_i
Path 2	4.555	15	5	P0/q_reg[0]/C	P0/q_reg_reg[43]/D	5.295	3.153	2.142	10.000	sys_clk_pin	sys_clk_i
Path 3	4.644	14	5	P0/q_reg[0]/C	P0/q_reg_reg[39]/D	5.206	3.064	2.142	10.000	sys_clk_pin	sys_clk_i
Path 4	4.681	16	5	P0/q_reg[0]/C	P0/q_reg_reg[46]/D	5.169	3.182	1.987	10.000	sys_clk_pin	sys_clk_i
Path 5	4.725	17	5	P0/q_reg[0]/C	cout0/q_reg_reg[0]/D	5.125	3.232	1.893	10.000	sys_clk_pin	sys_clk_i
Path 6	4.733	13	5	P0/q_reg[0]/C	P0/q_reg_reg[35]/D	5.117	2.975	2.142	10.000	sys_clk_pin	sys_clk_i
Path 7	4.739	16	5	P0/q_reg[0]/C	P0/q_reg_reg[45]/D	5.111	3.220	1.891	10.000	sys_clk_pin	sys_clk_i
Path 8	4.770	15	5	P0/q_reg[0]/C	P0/q_reg_reg[42]/D	5.080	3.093	1.987	10.000	sys_clk_pin	sys_clk_i
Path 9	4.814	16	5	P0/q_reg[0]/C	P0/q_reg_reg[44]/D	5.036	3.143	1.893	10.000	sys_clk_pin	sys_clk_i
Path 10	4.822	12	5	P0/q_reg[0]/C	P0/q_reg_reg[31]/D	5.028	2.886	2.142	10.000	sys_clk_pin	sys_clk_i



The schematic of the critical path.

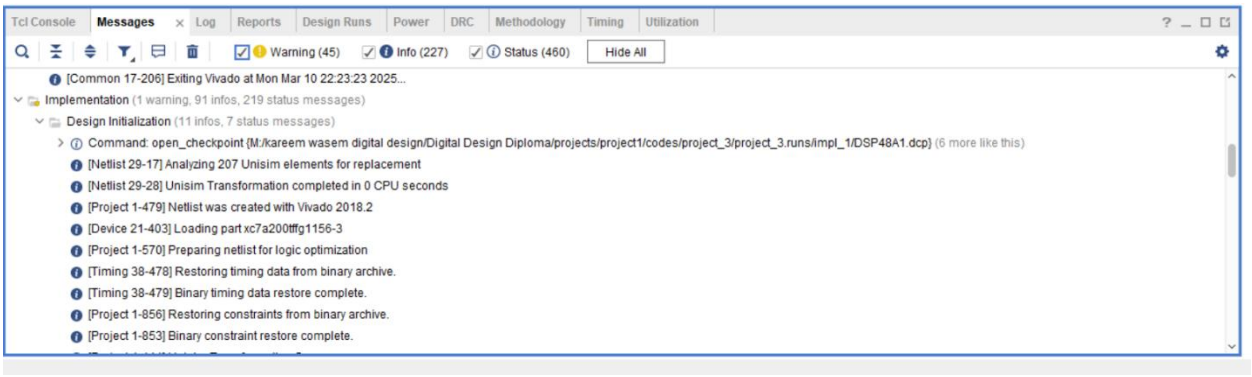
Utilization:



Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP48A1	319	392	1	327	1
A0 (reg_mux__parame...	9	18	0	0	0
A1 (reg_mux)	0	36	0	0	0
B0 (reg_mux__param...	36	18	0	0	0
B1 (reg_mux_1)	18	36	0	0	0
C0 (reg_mux__param...	24	96	0	0	0
carryin0 (reg_mux__pa...	0	2	0	0	0
cout0 (reg_mux__para...	0	2	0	0	0
D0 (reg_mux_2)	9	36	0	0	0
M0 (reg_mux__param...	0	36	1	0	0
opmode0 (reg_mux__...	198	16	0	0	0
P0 (reg_mux__param...	25	96	0	0	0

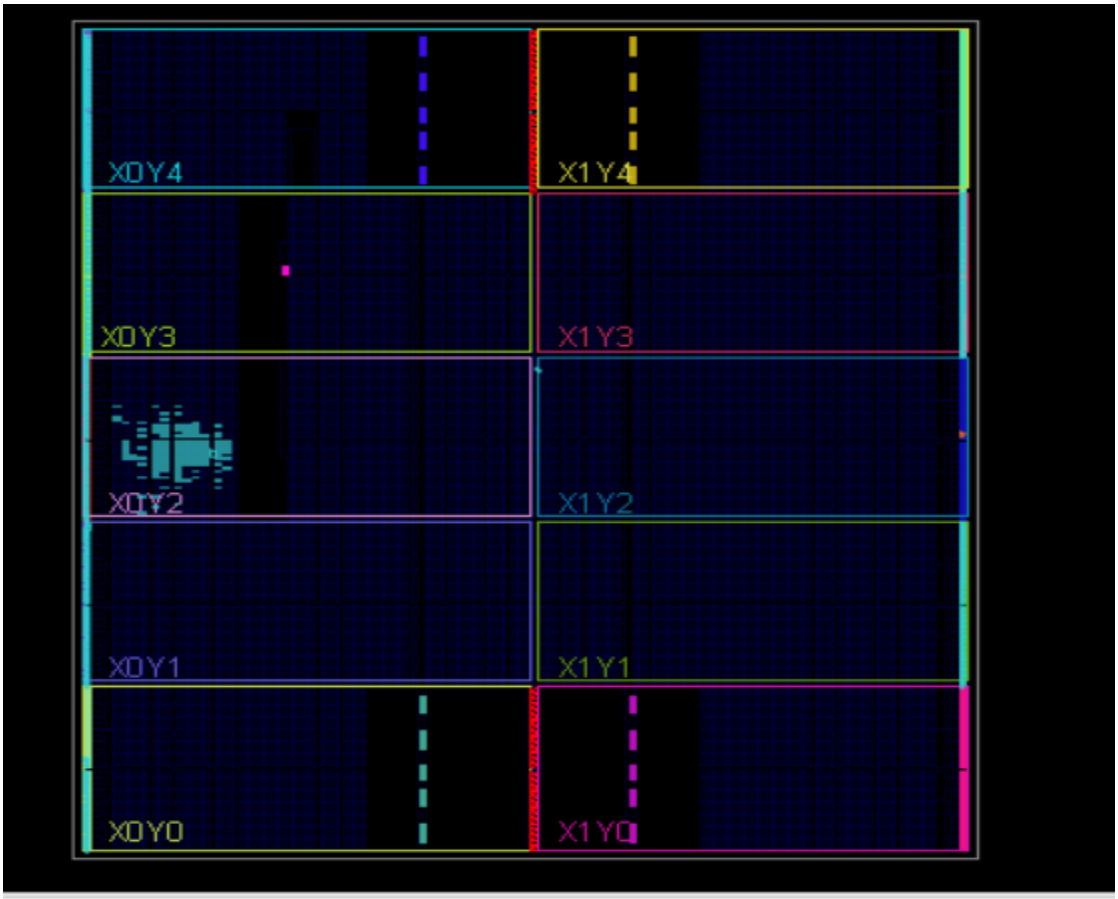
8- Implementation:

Messages tab:

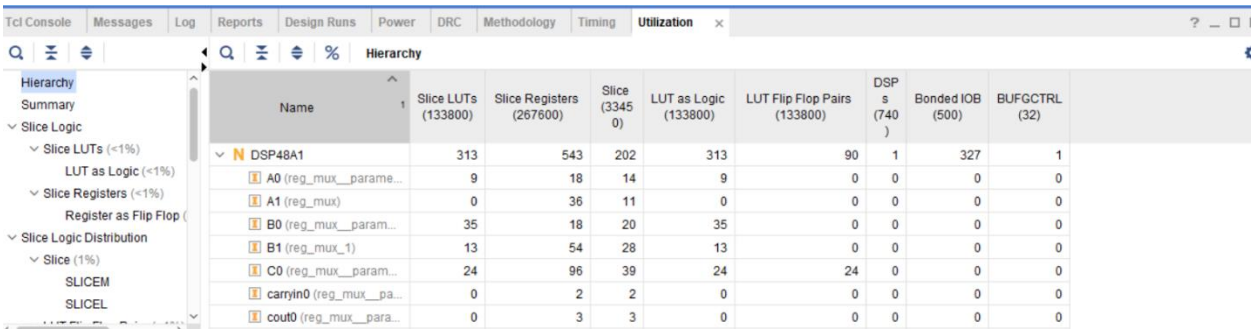


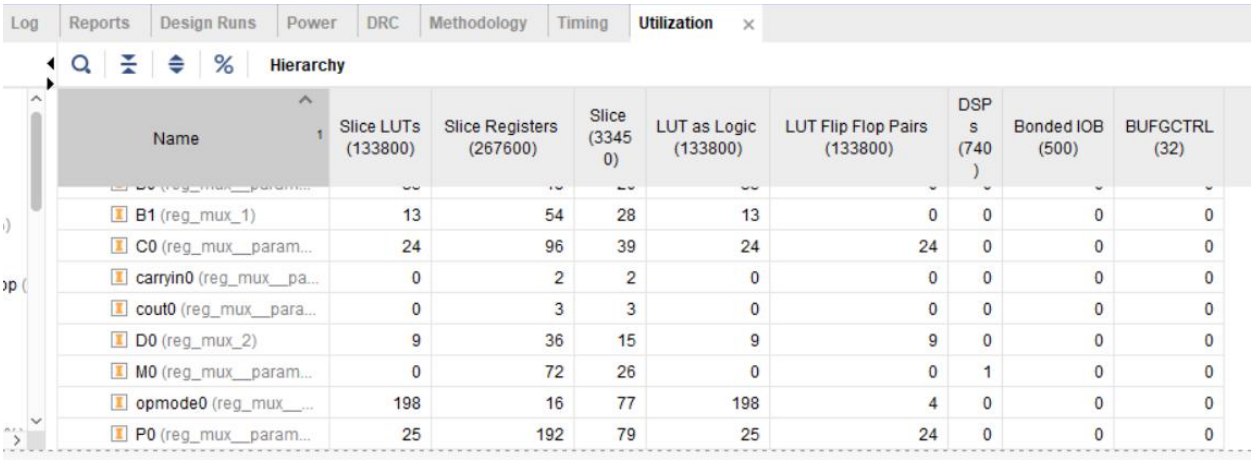
No extra warnings and no critical warnings as well.

Device snippets:



Utilization:





Timing report:

ts | Design Runs | Power | DRC | Methodology | Timing ×

Design Timing Summary

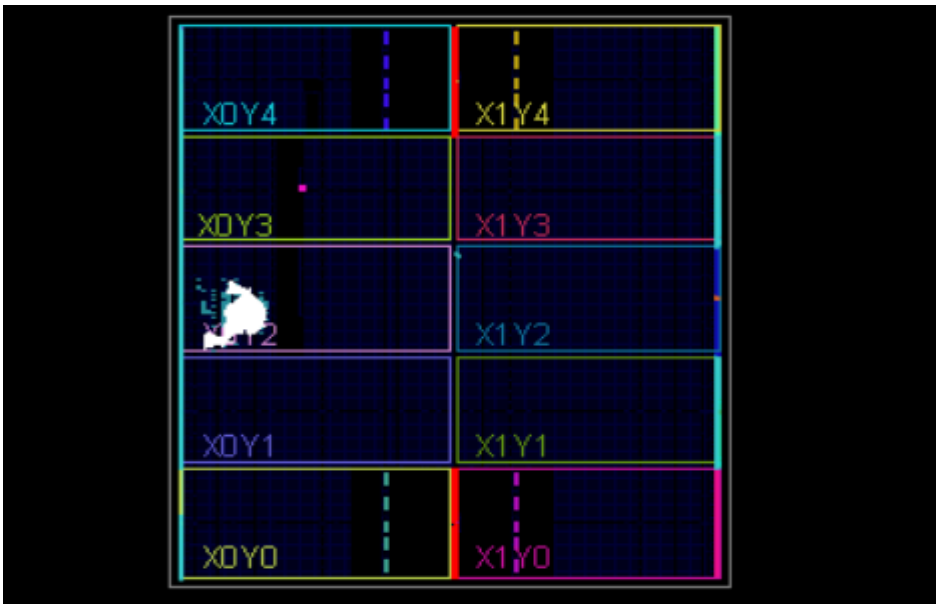
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.706 ns	Worst Hold Slack (WHS):	0.150 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	486	Total Number of Endpoints:	486	Total Number of Endpoints:	545

All user specified timing constraints are met.

ts | Design Runs | Power | DRC | Methodology | Timing ×

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	De
Path 1	3.706	17	96	opmode0/q_reg[0]/C	cout0/q_reg_reg[0]/D	6.255	3.047	3.208	10.0	sys_clk_pin	sy
Path 2	4.105	16	96	opmode0/q_reg[0]/C	P0/q_reg_reg[47]/D	5.878	3.048	2.830	10.0	sys_clk_pin	sy
Path 3	4.160	16	96	opmode0/q_reg[0]/C	P0/q_reg_reg[46]/D	5.823	2.990	2.833	10.0	sys_clk_pin	sy
Path 4	4.216	15	96	opmode0/q_reg[0]/C	P0/q_reg_reg[43]/D	5.801	2.961	2.840	10.0	sys_clk_pin	sy
Path 5	4.288	13	96	opmode0/q_reg[0]/C	P0/q_reg_reg[35]/D	5.726	2.775	2.951	10.0	sys_clk_pin	sy
Path 6	4.292	16	96	opmode0/q_reg[0]/C	P0/q_reg_reg[45]/D	5.658	3.028	2.630	10.0	sys_clk_pin	sy
Path 7	4.370	12	96	opmode0/q_reg[0]/C	P0/q_reg_reg[31]/D	5.660	2.681	2.979	10.0	sys_clk_pin	sy
Path 8	4.382	15	96	opmode0/q_reg[0]/C	P0/q_reg_reg[41]/D	5.607	2.936	2.671	10.0	sys_clk_pin	sy
Path 9	4.385	14	96	opmode0/q_reg[0]/C	P0/q_reg_reg[39]/D	5.631	2.880	2.751	10.0	sys_clk_pin	sy
Path 10	4.398	15	96	opmode0/q_reg[0]/C	P0/q_reg_reg[42]/D	5.619	2.912	2.707	10.0	sys_clk_pin	sy



Critical path snippet of the device.