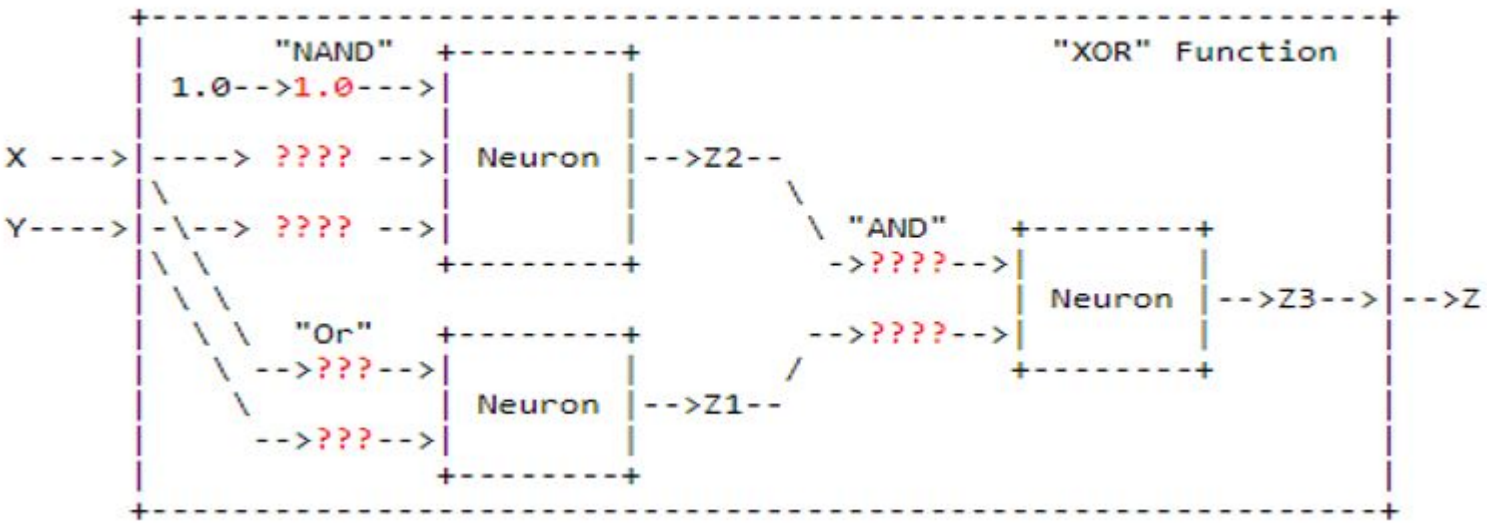
ML Project: Design XOR Gate



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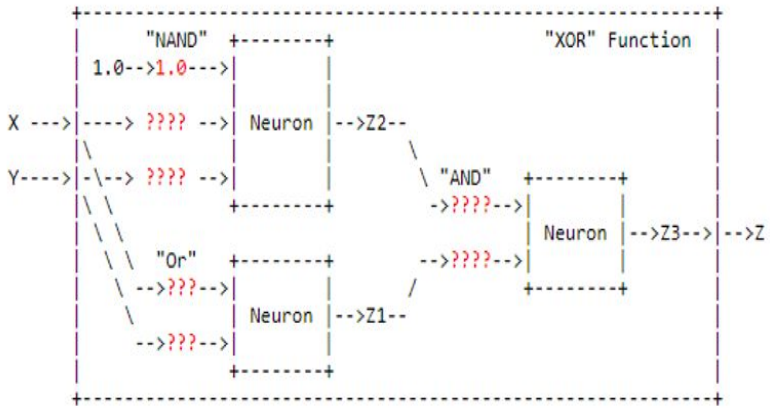
Step 1: How to design [XOR Gate]

a. Construct the truth table for XOR
b. Obtain the network equation



a. Construct the truth table for XOR

- The truth-table for the "XOR" function.

OR				NAND				XOR			
X	Y	Z1		X	Y	Z2		X	Y	Z3
0	0	0		0	0	1		0	0	0
0	1	1	AND	0	1	1	=	0	1	1
1	0	1		1	0	1		1	0	1
1	1	1		1	1	0		1	1	0

b. Obtain the network equation

The neural network equation can be created by combining neural equations.

Z1 := X "Or" Y
Z2 := X "NAND" Y
Z := Z3 := Z1 "AND" Z2
Z := (X "Or" Y) "AND" (X "NAND" Y)

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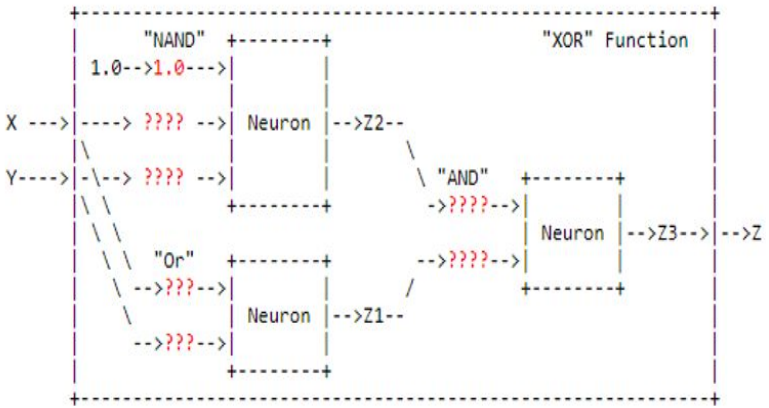
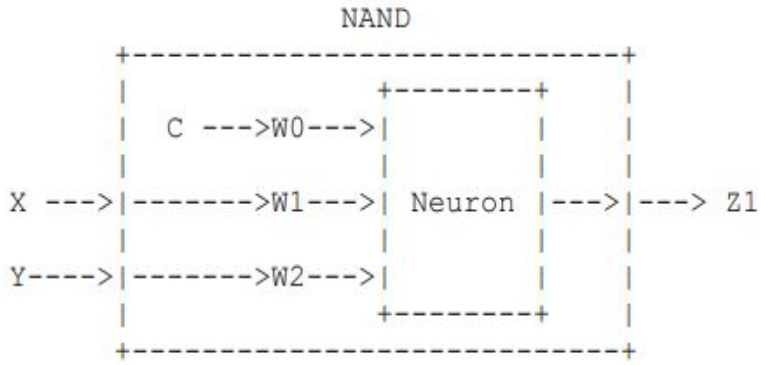
Step 2: Calculate Z1, Z2, and Z3 transfer functions



a. Z1:= X "NAND" Y



Z1 := (W0 * C + W1 * X + W2 * Y >= T)

Train NAND gate to get **w0,w1, W2** ?

Z:=Z1= (W0 * C + W1 * X + W2 * Y >= T)
where T:= 1.0.

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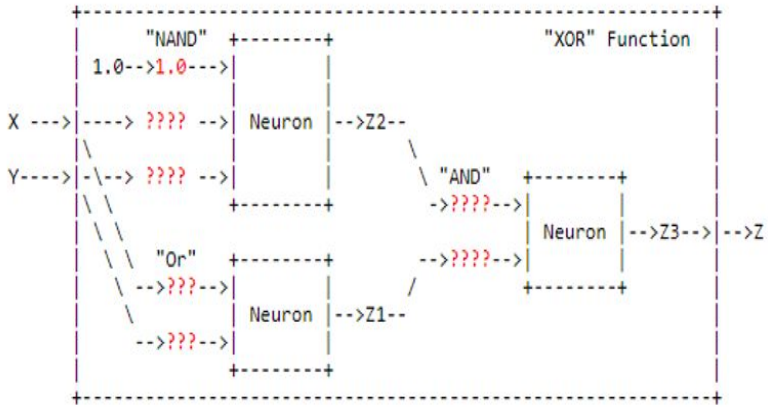
Step 2: Calculate Z1, Z2, and Z3 transfer functions



a. Z1:= X "NAND" Y

Desired "NAND" Function	Loop 1 W0=0.0 W1=W2=0.5 Function	Loop 2 W0=0 W1=W2=1 Function	Loop 3 W0=0.5 W1=W2=1 Function
C X Y | Z --------- 1 0 0 | 1 1 0 1 | 1 1 1 0 | 1 1 1 1 | 0	C X Y | Z --------- 1 0 0 | 0 1 0 1 | 0 1 1 0 | 0 1 1 1 | 0	C X Y | Z --------- 1 0 0 | 0 1 0 1 | 1 1 1 0 | 1 1 1 1 | 1	C X Y | Z --------- 1 0 0 | 0 1 0 1 | 1 1 1 0 | 1 1 1 1 | 1
Loop 4 W0= 1 W1=W2=1 Function	**Loop 5 W0= 1 W1=W2=0.5 Function**	**Loop 6 W0= 1 W1=W2=0 Function**	**Loop 7 W0= 1 W1=W2=-0.5 Function**
C X Y | Z --------- 1 0 0 | 1 1 0 1 | 1 1 1 0 | 1 1 1 1 | 1	C X Y | Z --------- 1 0 0 | 1 1 0 1 | 1 1 1 0 | 1 1 1 1 | 1	C X Y | Z --------- 1 0 0 | 1 1 0 1 | 1 1 1 0 | 1 1 1 1 | 1	C X Y | Z --------- 1 0 0 | 1 1 0 1 | 0 1 1 0 | 0 1 1 1 | 0
Loop 7 W0= 1.5 W1=W2=-0.5 Function			
C X Y | Z --------- 1 0 0 | 1 1 0 1 | 1 1 1 0 | 1 1 1 1 | 0			

Therefor :

W0= 1.5, W1=W2=-0.5

Z1: = (1.5 * 1.0 + -0.5 * X + -0.5 * Y >= 1.0)

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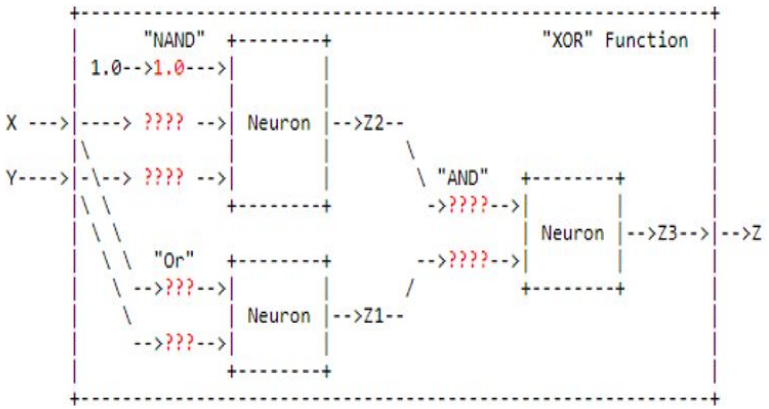
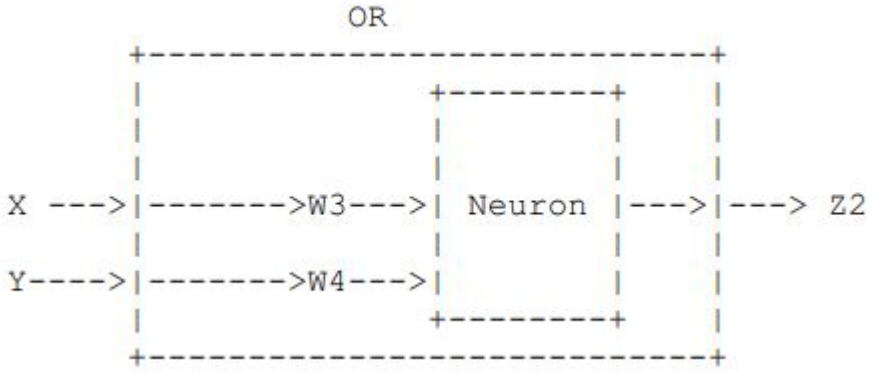
Step 2: Calculate Z1, Z2, and Z3 transfer functions



b. Z2:= X "or" Y



Z2 := (W3 * X + W4 * Y >= T)

Train NAND gate to get **w3, W4 ?**

Z2:= (W3 * X + W4 * Y >= T)

where T:= 1.0.

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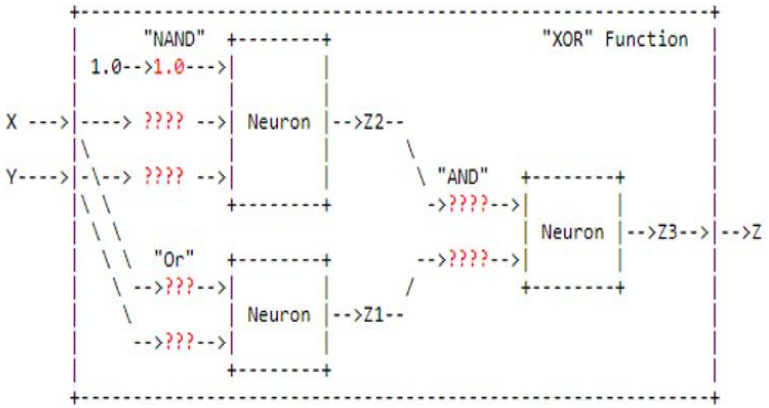
Step 2: Calculate Z1, Z2, and Z3 transfer functions



b. Z2:= X "or" Y

Desired "OR" Function			Loop 1 W3=W4=0.5 Function			Loop 2 W3=W4= 1 Function		
X	Y	Z	X	Y	Z	X	Y	Z
0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	1	0	1
1	1	1	1	1	1	1	1	1

Therefor:

W3=W4= 1

Z2: = (1* X + 1* Y >= 1.0)

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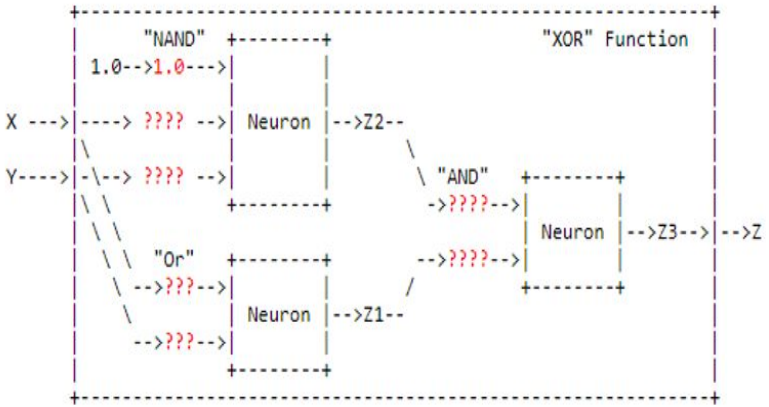
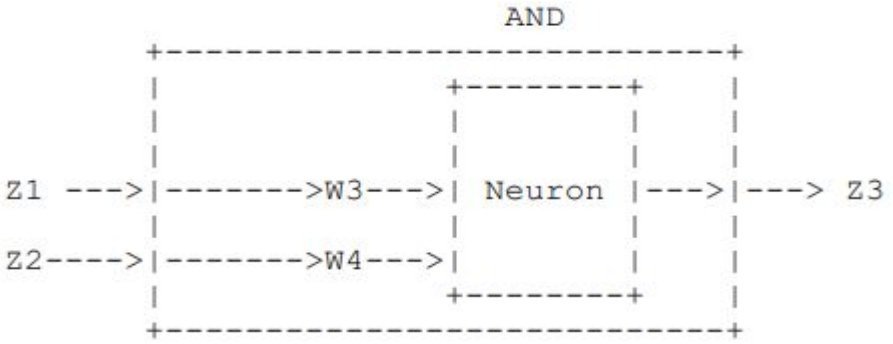
Step 2: Calculate Z1, Z2, and Z3 transfer functions



c. Z := Z3 := Z1 "AND" Z2



Z3 := (W5 * Z1 + W6 * Z2 >= T)

Train the AND gate to get w5, W6

let Z1 := X, and Z2:= Y

Z3:= (W5 * X + W6* Y >= T)

where T:= 1.0.

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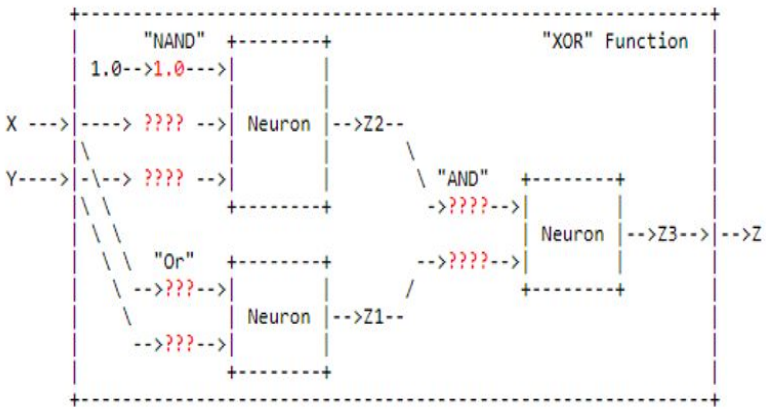
Step 2: Calculate Z1, Z2, and Z3 transfer functions



c. Z := Z3 := Z1 "AND" Z2

Desired "AND" Function	Loop 1 W4=W5=0.5 Function
X Y | Z	X Y | Z
0 0 | 0	0 0 | 0
0 1 | 0	0 1 | 0
1 0 | 0	1 0 | 0
1 1 | 1	1 1 | 1

Therefor:

W5=W6= 0.5

Z3: = (0.5* X + 0.5* Y >= 1.0) = (0.5* Z1 + 0.5* Z2 >= 1.0)

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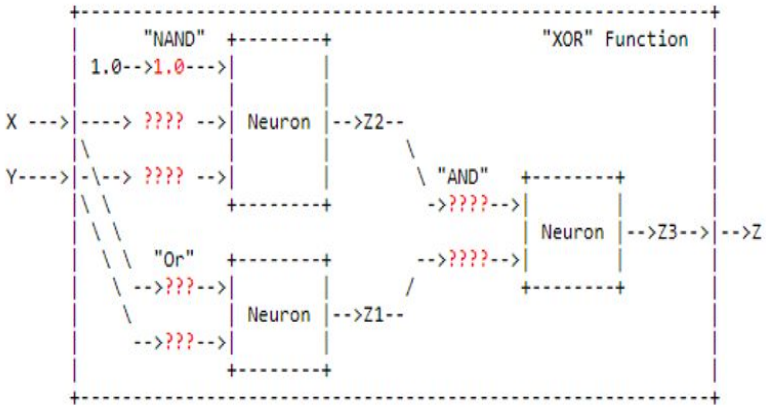
Step 2: Calculate Z1, Z2, and Z3 transfer functions



D. Complete XOR neural network circuit diagram

W0= 1.5 , W1=W2=-0.5

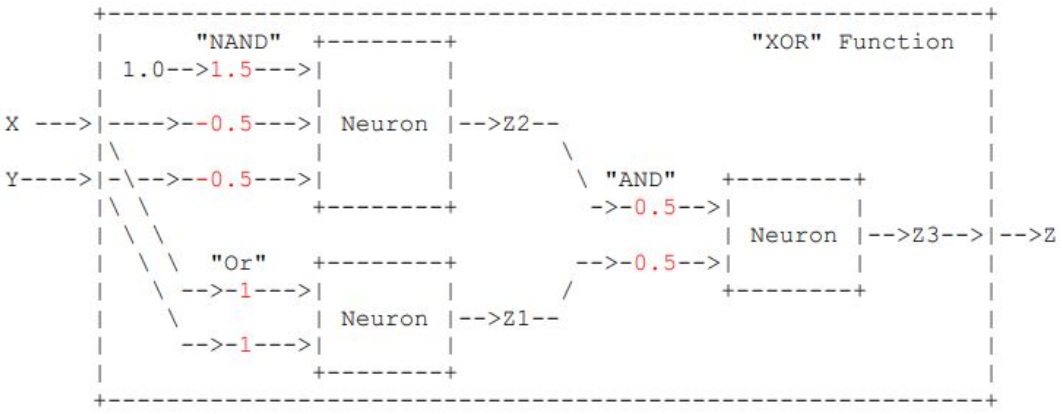
Z1: = (1.5 * 1.0 + -0.5 * X + -0.5 * Y >= 1.0)

W3=W4= 1

Z2: = (1* X + 1* Y >= 1.0)

W5=W6= 0.5

Z3: = (0.5* X + 0.5* Y >= 1.0) = (0.5* Z1 + 0.5* Z2 >= 1.0)



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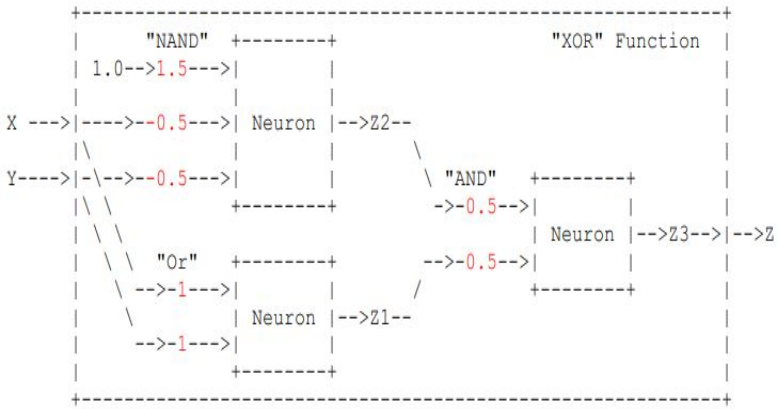
Step 3: Prove results



Prove result:

Test cases:

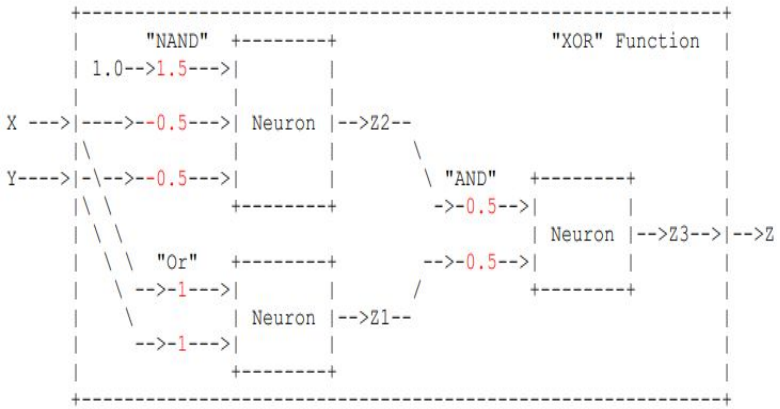
- X=1, Y=1
- X=1, Y=0
- X=0, Y=1
- X=0, Y=0

Test 1: X=1, Y=1	Desired Result
Z1: = (1.5 * 1.0 + -0.5 * X + -0.5 * Y >= 1.0) = 1.5-0.5-0.5 := 0 Z2: = (1* X + 1* Y >= 1.0) = 1 + 1 := 1 Z3: = (0.5* Z1 + 0.5* Z2 >= 1.0) = 0.5*0 + 0.5*1 := 0	XOR X Y | Z 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0

Test 2: X=1, Y=0	Desired Result
Z1: = (1.5 * 1.0 + -0.5 * X + -0.5 * Y >= 1.0) = 1.5-0.5*1-0.5*0 := 1 Z2: = (1* X + 1* Y >= 1.0) = 1*1 + 1*0 := 1 Z3: = (0.5* Z1 + 0.5* Z2 >= 1.0) = 0.5*1 + 0.5*1 := 1	XOR X Y | Z 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0

ML Project: Design XOR Gate

Step 3: Prove results



Prove result:

Test cases:

- X=1, Y=1
- X=1, Y=0
- X=0, Y=1
- X=0, Y=0

Test 3: X=0, Y=1

```
Z1: = ( 1.5 * 1.0 + -0.5 * X + -0.5 * Y >= 1.0 )
    = 1.5*1.0-0.5*0-0.5*1 := 1

Z2: = (1* X + 1* Y >= 1.0 )
    = 1*0 + 1*1 := 1
Z3: = (0.5* Z1 +  0.5* Z2 >= 1.0 )
    = 0.5*1 + 0.5*1 := 1
```

Desired Result

XOR		
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

Test 2: X=0, Y=0

```
Z1: = ( 1.5 * 1.0 + -0.5 * X + -0.5 * Y >= 1.0 )
    = 1.5-0.5*0-0.5*0 := 1

Z2: = (1* X + 1* Y >= 1.0 )
    = 1*0 + 1*0 := 0
Z3: = (0.5* Z1 +  0.5* Z2 >= 1.0 )
    = 0.5*1 + 0.5*0 := 0
```

Desired Result

XOR		
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

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Conclusion:

The test results obtained based on the final parameters agree with the desired values. Hence, for the given XOR gate, below are the final parameters values and the complete ANN circuit diagram.

W0= 1.5
W1=W2=-0.5

W3=W4= 1

W5=W6= 0.5