2022 Digital IC Design
Homework 4: Edge-Based Line Average interpolation

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Clock width	20(ns)	Gate-level simulation time	84168(ns)

your pre-sim result of test patterns

```
#
# ------------------------S U M M A R Y--------------------------
#
#     Congratulations!
#
#     Result image data are generated successfully!
#
#     The result is PASS!!!
#
# ---------------------------------------------------------------
#
# ** Note: $finish    : C:/Users/P7610/Downloads/newHW4/file/testfi
#    Time: 84160 ns  Iteration: 0  Instance: /TB_ELA
```

your post-sim result of test patterns

```
# ------------------------S U M M A R Y--------------------------
#
#     Congratulations!
#
#     Result image data are generated successfully!
#
#     The result is PASS!!!
#
# ---------------------------------------------------------------
#
# ** Note: $finish    : C:/altera/13.0sp1/modelsim_ase/win32aloem/ne
#    Time: 84168575 ps  Iteration: 0  Instance: /TB_ELA
```

Synthesis Result

Total logic elements	158
Total memory bit	0
Embedded multiplier 9-bit element	0

your flow summary

Flow Summary	
Flow Status	Successful - Thu May 05 14:25:03 2022
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	ELA
Top-level Entity Name	ELA
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	158 / 68,416 (< 1 %)
Total combinational functions	158 / 68,416 (< 1 %)
Dedicated logic registers	71 / 68,416 (< 1 %)
Total registers	71
Total pins	39 / 622 (6 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

我的設計流程是分 3 個部分，首先先把奇數列的資料搬過去，完成第一部分，再來是偶數列的最左與最右的元數，之後才是偶數列中間的元數，我的設計流程大致是這樣完成的。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*