Symica
Design Environment

QuickStart

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Symica Design Environment Quick Start

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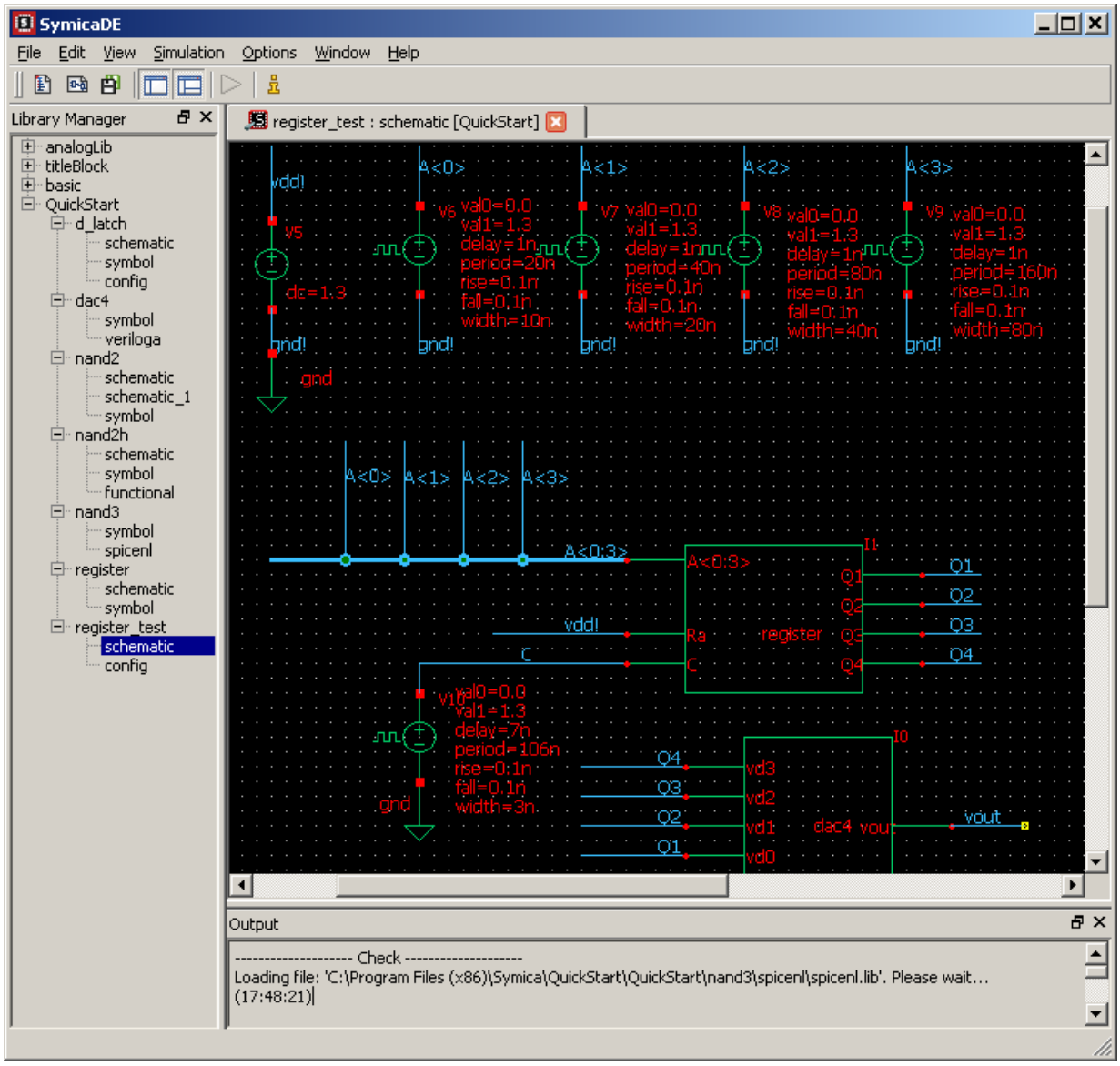
Introduction

This Quick Start guide demonstrates how to start working with the Symica Design Environment.

You will learn how to:

- create libraries, cells and views,
- setup simulation environment and simulate your schematics,
- add behavioral (digital and analog) cells described in Verilog AMS,
- add SPICE netlists of IP blocks to your project,
- use other beneficial features of Symica tools.

The Quick Start describes the main steps to create a custom mixed signal project. The process of working in Symica DE is shown using the example circuit below, a four-bit register with a digital-to-analog converter at output:



- this sign indicates useful advice or recommendation.

Project structure

The Symica project structure:

- **Library** is a collection of cells. In the Symica DE you can work with several Libraries at the same time. The list of attached Libraries is represented in the *Library Manager* window and resides in the "cfg.lib" file.
- **Cell** is a functional block that can be described in one or several formats (Cellviews).
- **Cellview** is a representation of the Cell in various formats, i.e. schematic, symbol etc.

For example, in the library *QuickStart* for an *nand2* cell (Fig. 1) there can be both a *schematic* view (Fig. 2) and a *symbol* view (Fig. 3):

Fig. 1

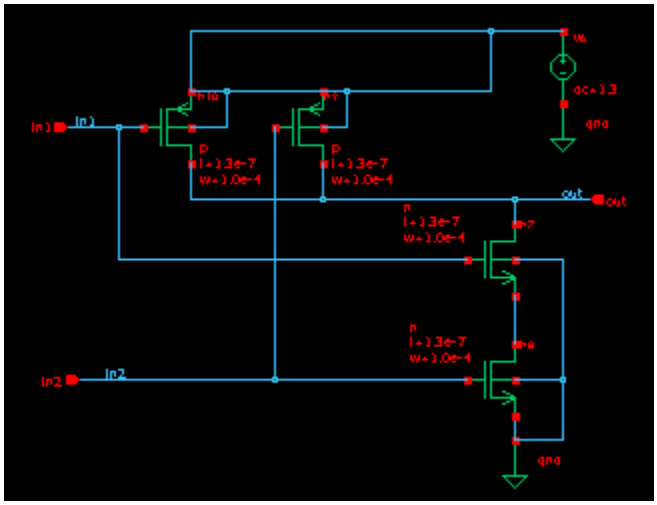


Fig. 2

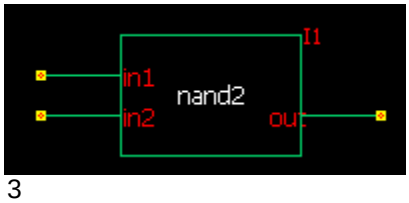


Fig. 3

Overview of the cfg.lib file

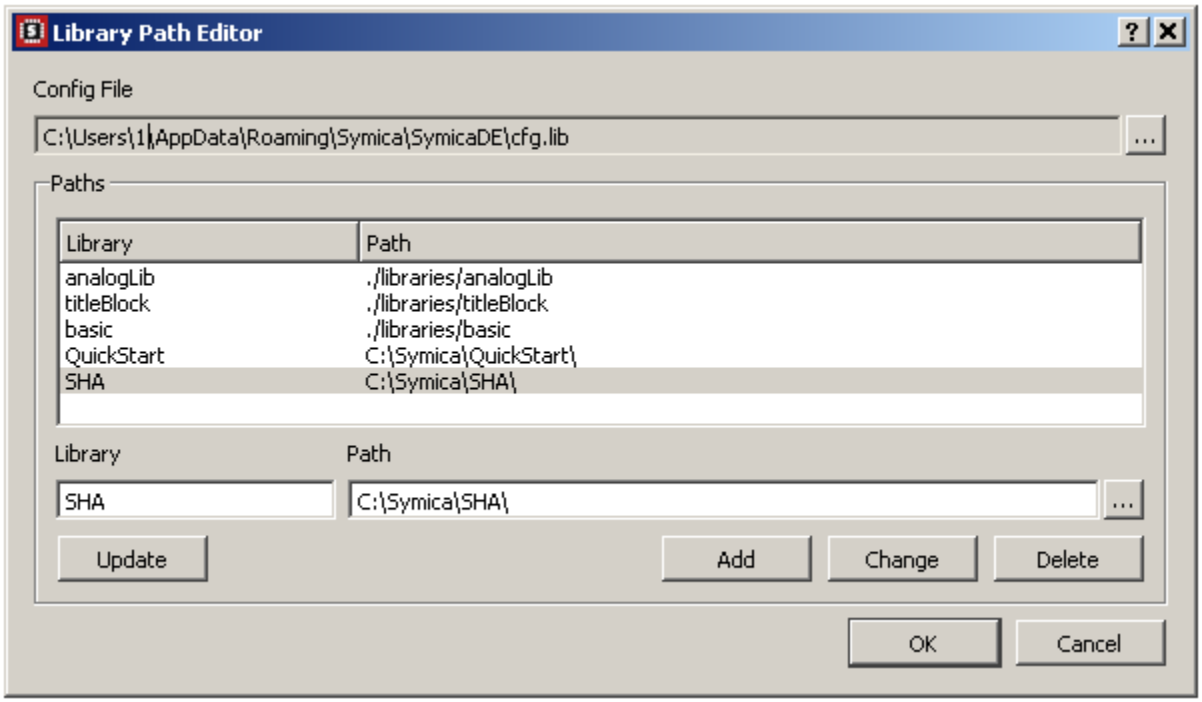
The "cfg.lib" file contains a list of attached libraries which are displayed in *Library Manager*.

If you want Symica example projects (QuickStart and SHA) to be added to Library Manager select *Help -> SymicaDE Examples* and in the opened *Copy Symica DE Examples* window specify the path where

to place example projects.

When you launch the Symica DE, the system looks in the user`s home directory for the "cfg.lib" file (the system creates it automatically the first time design Environment is started).

The path to cfg.lib is shown in the *Library Path Editor* window - field *Config file* (*File -> Library Paths..*):
If you want to edit cfg.lib file press ... button located on the right of the Config File field.



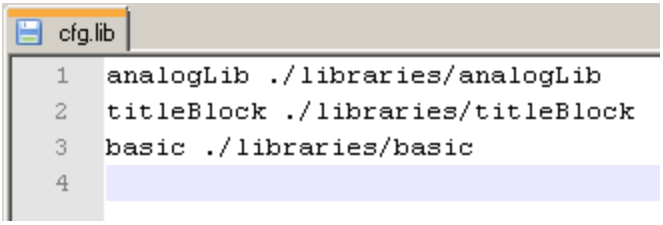
Default path to the cfg.lib under Microsoft Windows 7 — C:\Users\UserName\AppData\Roaming\Symica\SymicaDE\cfg.lib

In this cfg.lib file the command "INCLUDE_DEFAULT_LIB" attaches all libraries from default cfg.lib located in the Symica setup folder:

1. cfg.lib located in the user`s home directory:

```
cfg.lib
1  INCLUDE_DEFAULT_LIB
2  "QuickStart" "C:\Symica\QuickStart\"
3  "SHA" "C:\Symica\SHA\"
4
```

2. Default cfg.lib located in the Symica setup folder:



Structure of the cfg.lib

Syntax:

```
include other_cfg_file
name_of_the_library path
```

For example:

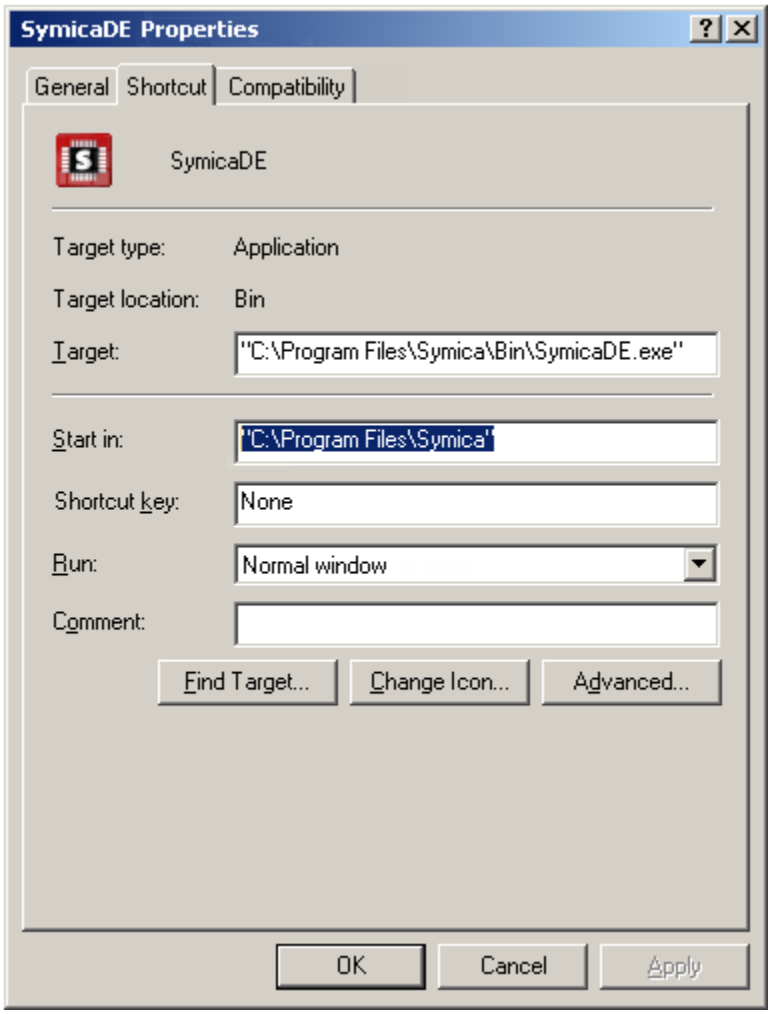
```
INCLUDE C:\Program Files\Symica\Bin\cfg.lib
Lib1 C:\Lib1\
```

The `include` directives can be added, modified or deleted only by editing cgf.lib file manually in any text editor. The library names listed in *Library Path Editor* added using `include` directive can`t be deleted or changed in the *Library Path Editor* window.

Priority in opening "cfg.lib":

- User`s system default directory.
- Current launching directory.

You can setup current launching directory for example in shortcut properties. Right click on the shortcut and specify the path in the field *Start in*:

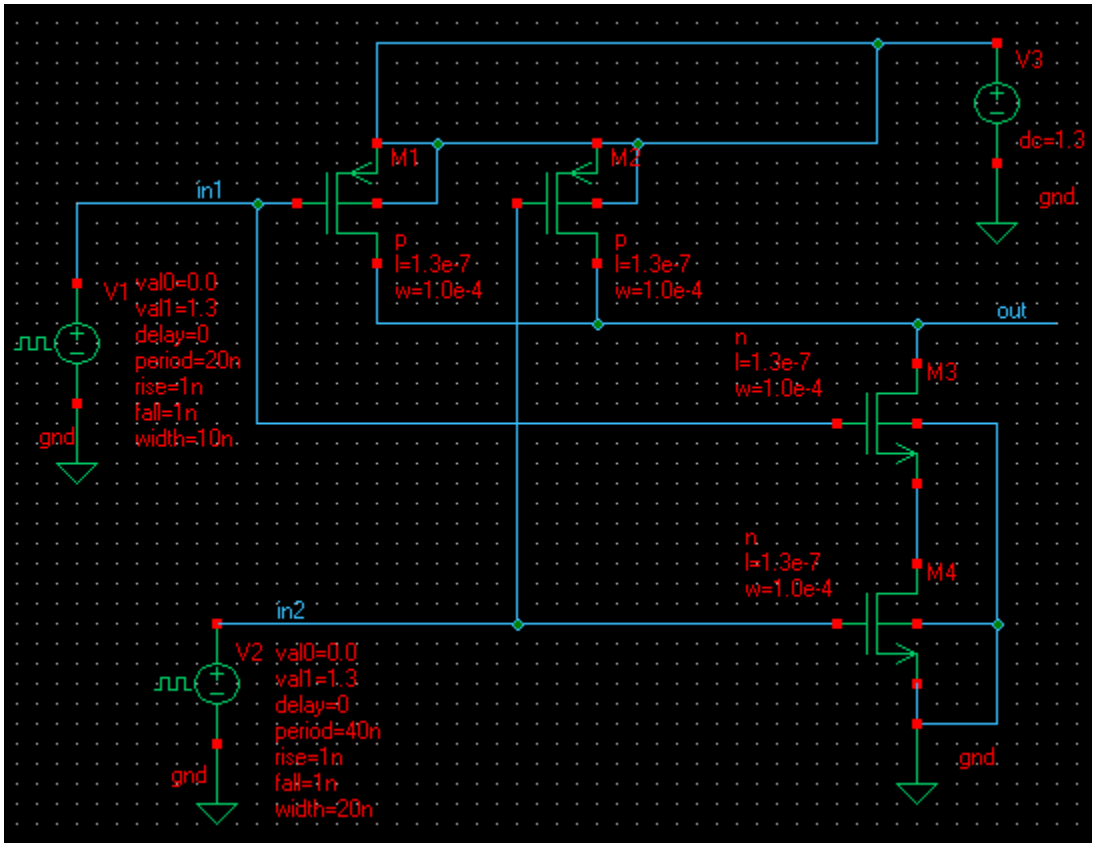


If "cfg.lib" file is not found a warning message will appear.

Creating the Analog Design

- After you install and open Symica DE for the first time you can add the QuickStart library described in this guide by Help -> SymicaDE Examples. Specify path to place it.
- To go through this QuickStart you can create your own library with unique name.
- If you changed QuickStart library you can reload original state also by Help -> SymicaDE Examples.

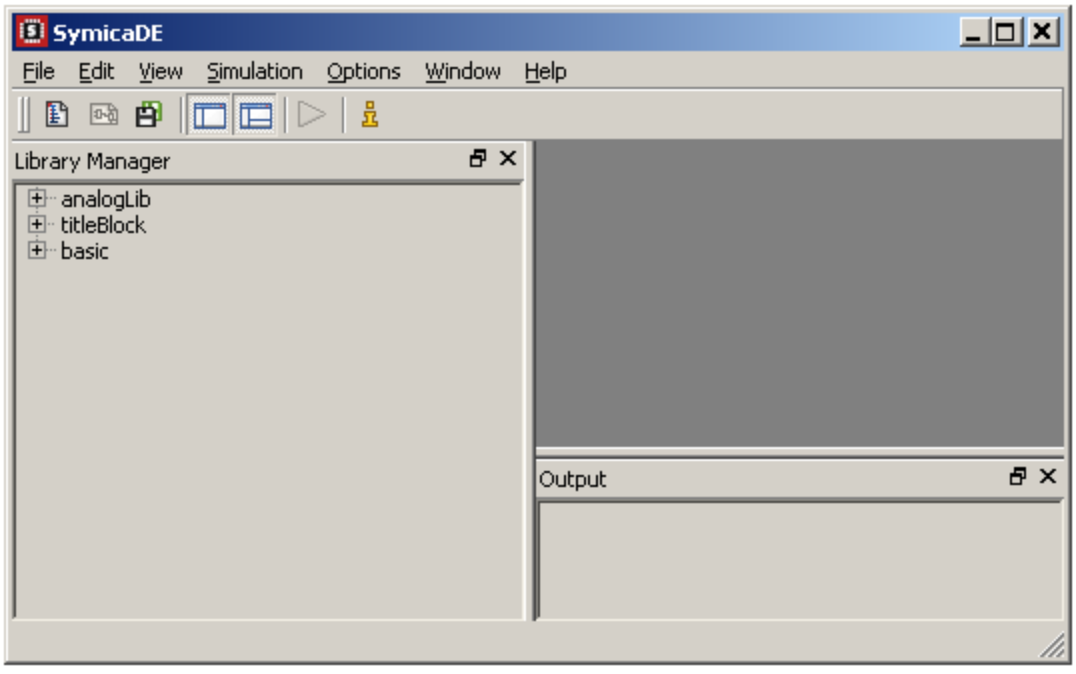
This chapter shows how to create a *nand2* circuit in the schematic editor.



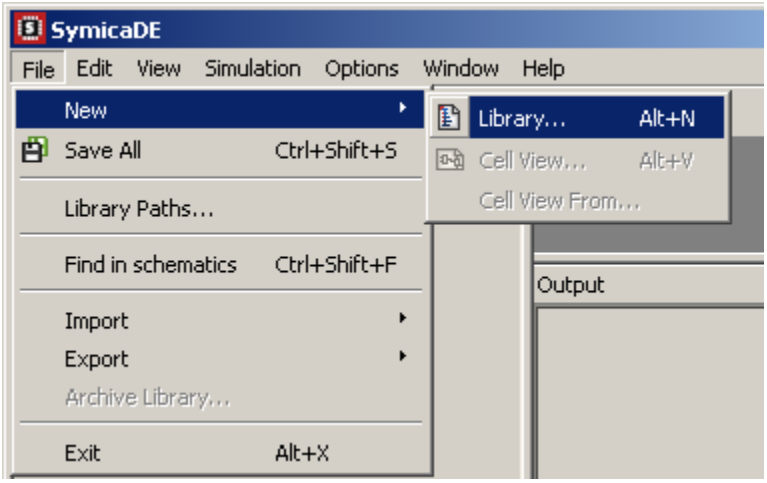
Creating the Library

To create a new library:

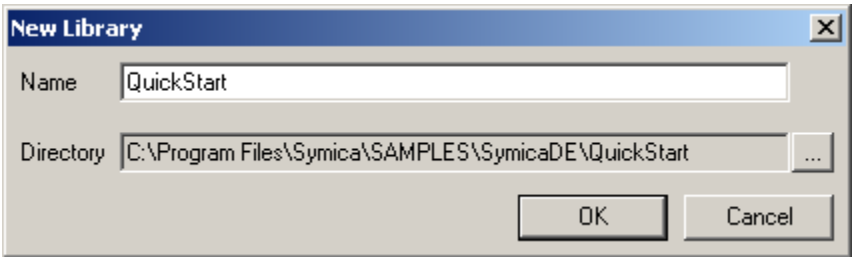
1. Run SymicaDE by clicking on shortcut *Start->Programs->Symica->SymicaDE*. An empty window will be opened:



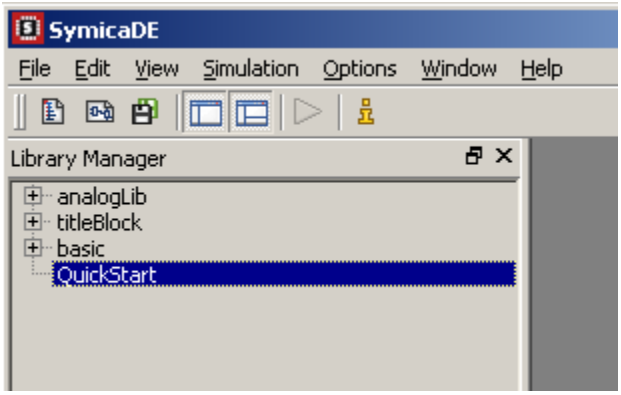
2. Choose *File -> New -> Library* or press 'Alt+n'.



3. Enter a name for the new library and select the path to new folder (a new folder will be created with the name of the library). Press *OK*.



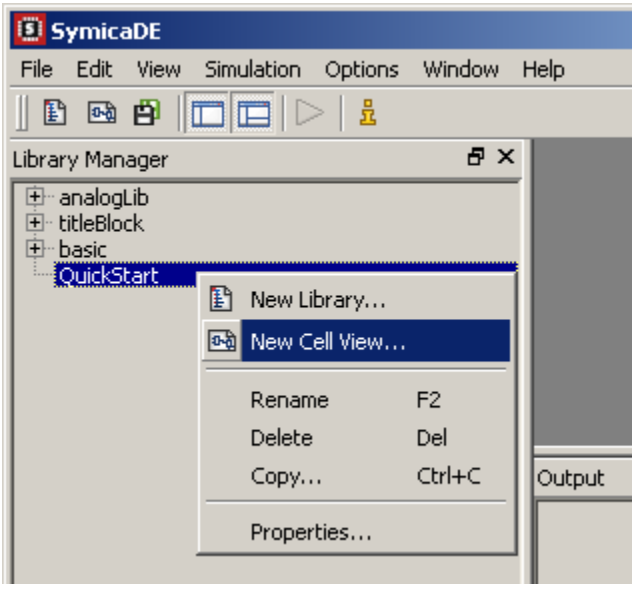
4. New library will appear in the *Library Manager* window.



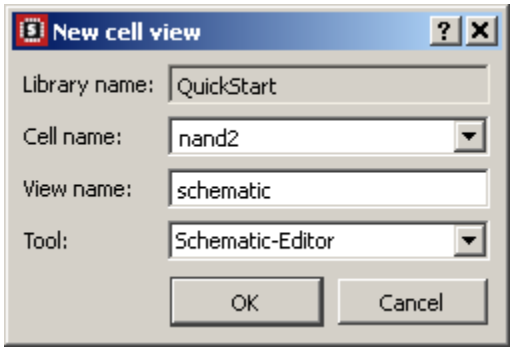
Creating the Schematic View

Creating a new cell and *schematic* view:

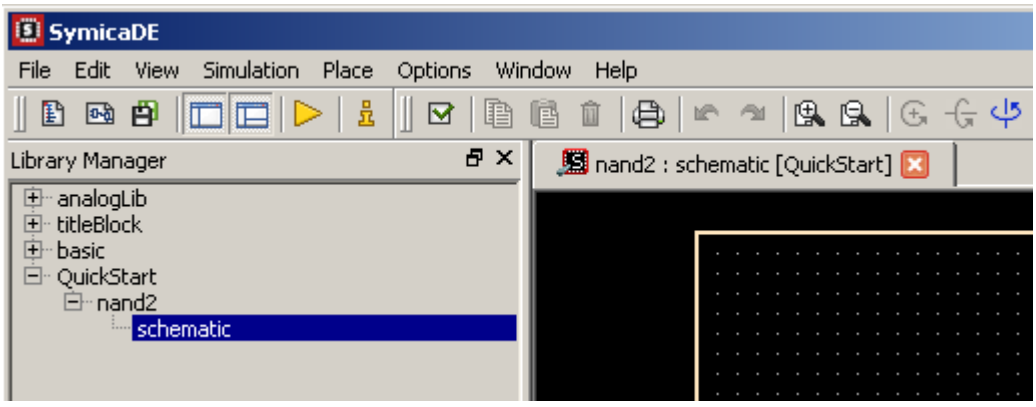
1. Right click mouse button on the name of the library and choose *New Cell View*...



2. In the pop-up dialog box, enter *Cell Name* = `nand2`; (*View Name* = `schematic`); choose for field *Tool* = `Schematic-Editor`.



3. To start entering the circuit activate *Schematic Editor* window by clicking on *schematic* view name; a drawbar menu will appear on the top.



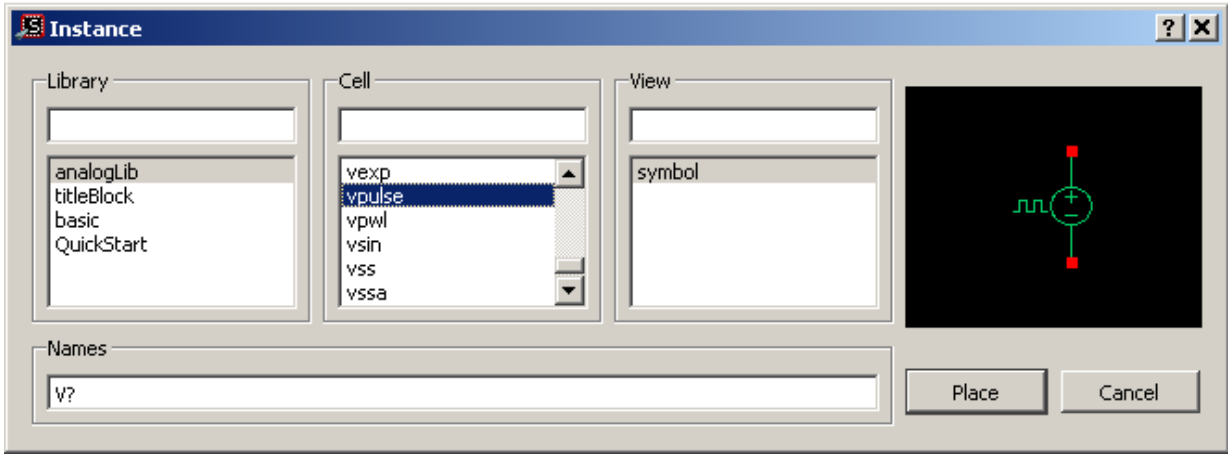
To start entering schematic:

1. Library *analogLib* (library with basic elements like voltage sources, grounds etc.) should already be added in *Library manager* by default. If not,

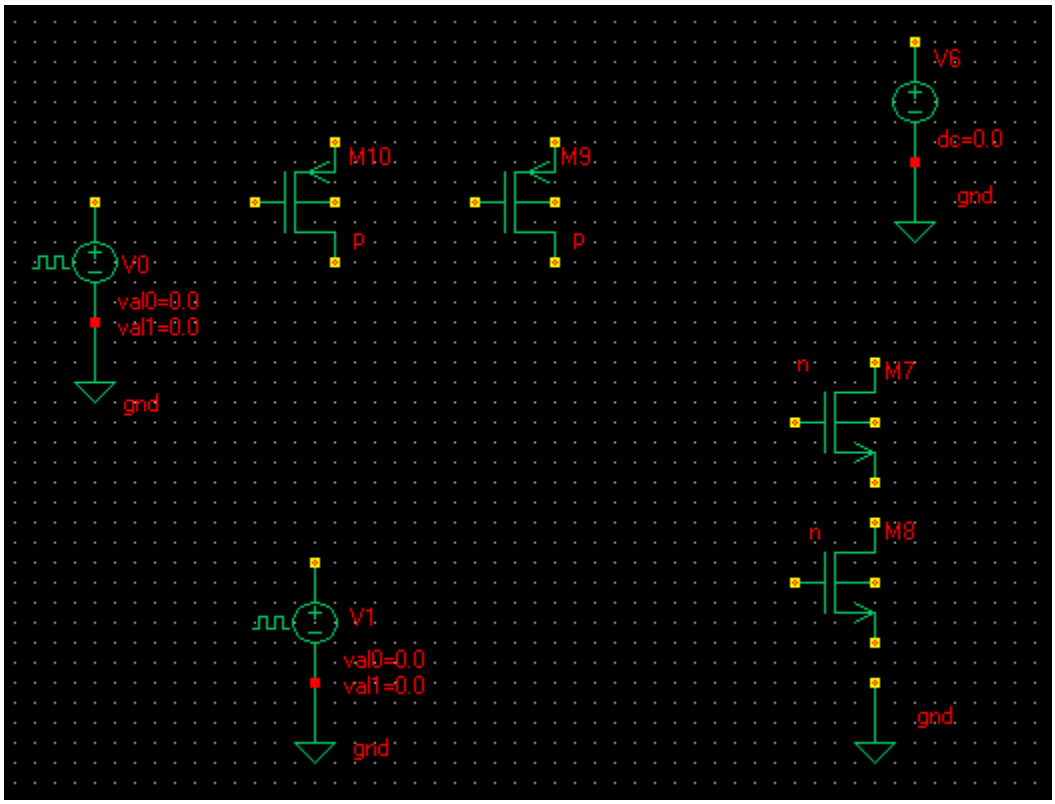
choose *File -> Library Paths* and in the Library Path Editor window press the browse button and select ...C:*\Program Files\Symica\share\libraries\analogLib\analogLib.grf.*

(under Microsoft Windows 7 (64-bit) — ..*Program Files(x86)**Symica**share**libraries**analogLib**analogLib.grf)*

2. Click on *Instance* button (, shortcut key 'i'), select `analogLib` in the left column, and then *vpulse* from the list of cells. Press *Place*:



3. Place all circuit elements as shown in the picture below (select: *vpulse, nmos4, pmos4, vdc, gnd*):



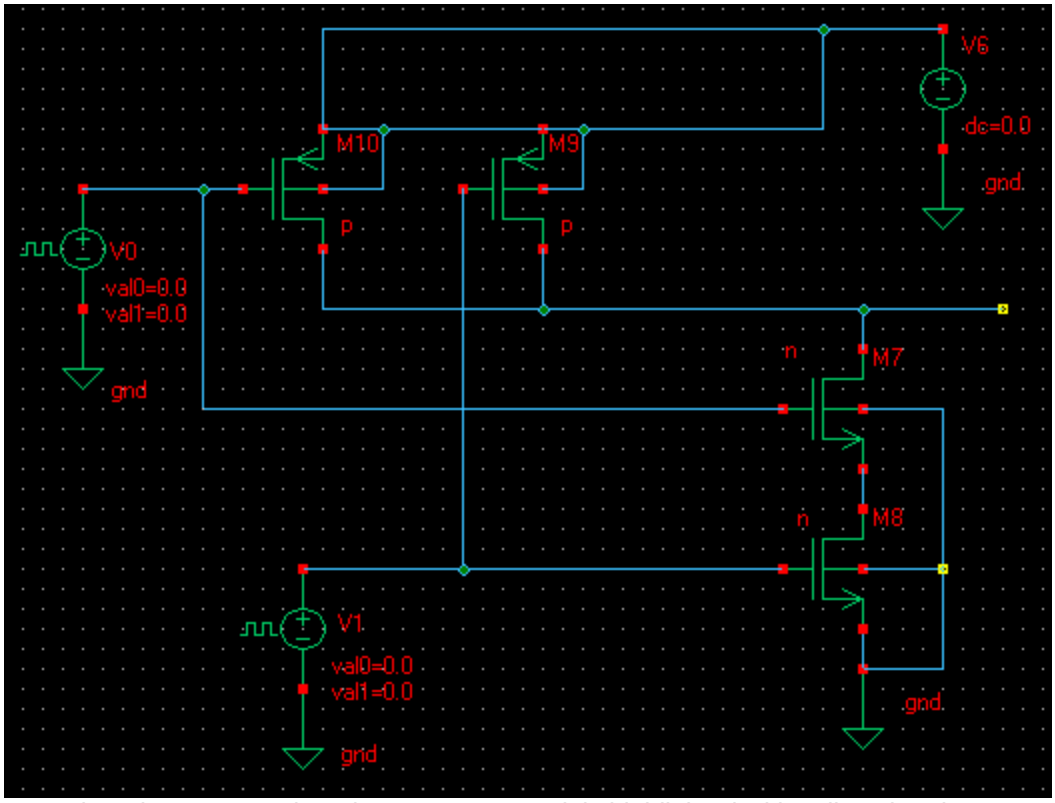
Use *Instance* drawbar for quick access to cells of special types:

- transistors,
- current and voltage sources,
- passive elements,
- ground elements,

- common cells.

4. Connect the elements using *wire* function: click on button or press key 'w'. Yellow squares are used to mark contacts.

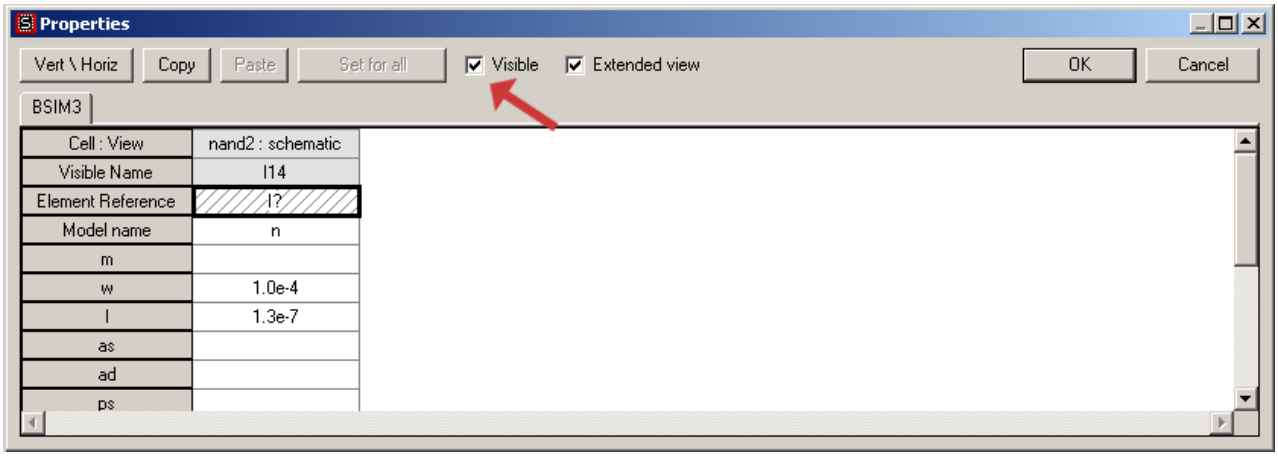
Click to place the first point of the wire, then repeat clicks for additional wire segments/points, then finish the wire with a double click or press 'Esc' key.



When the mouse pointer is near a contact, it is highlighted with yellow rhomb. Press 's' key to link wire at the contact.

5. Double click on the instance to open its *Properties* dialog box, then double click on the property field to enter its value (shortcut key 'F2'). Enter transistor properties as shown below. Model name, *l* (length) and *w* (width) values are taken from SPICE model decks which will be specified in *Running simulation* chapter.

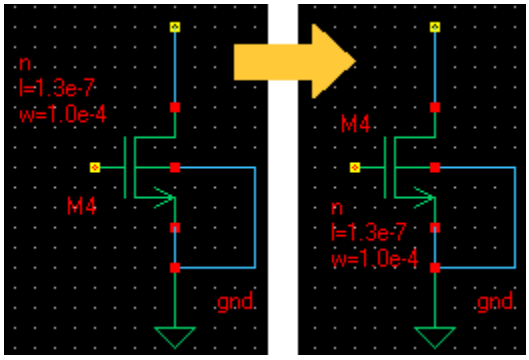
In this example model name for n-transistor - 'n', for p- transistor -'p')



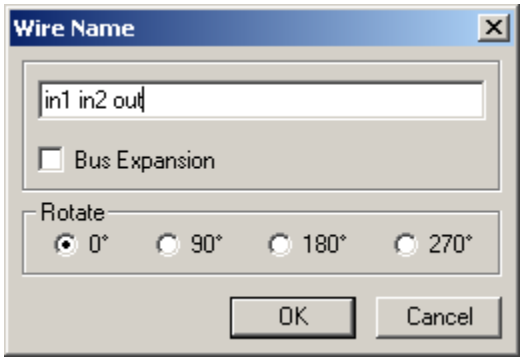
Position mouse pointer on the parameter name to see its description.

Select property line and check *Visible* option to display the parameter value visible on the schematic.

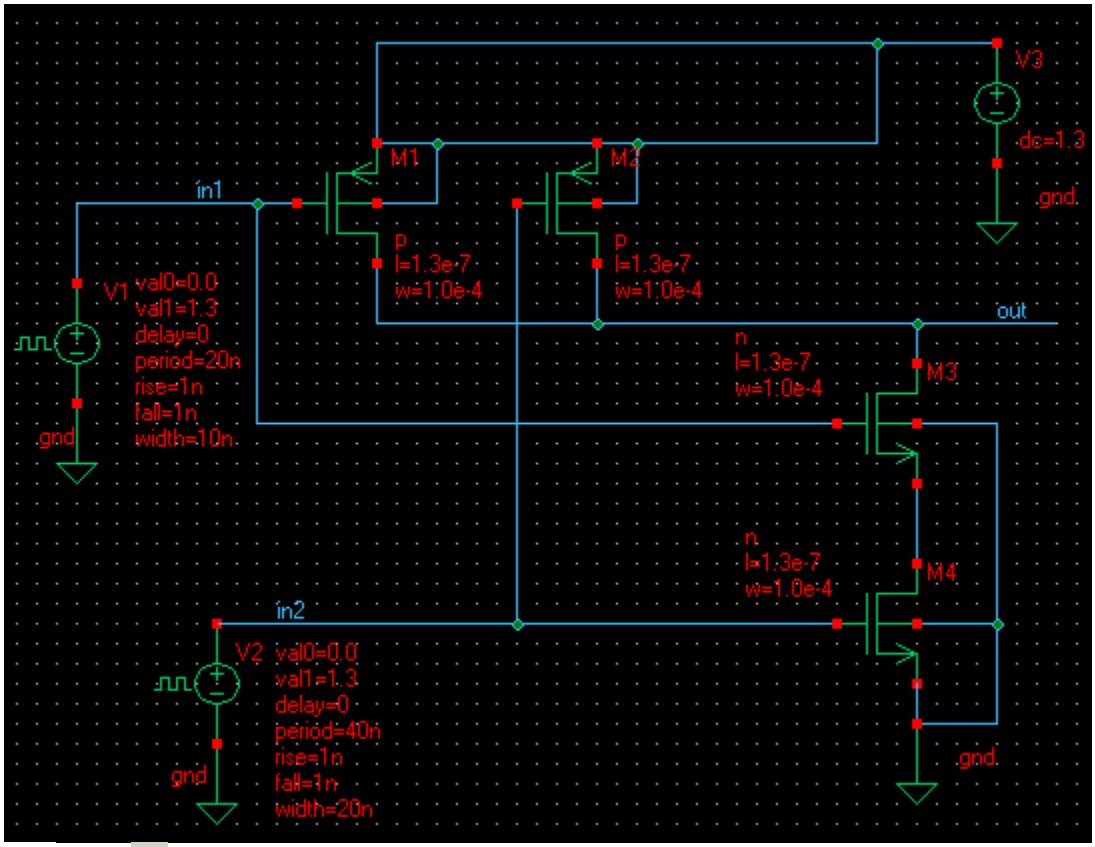
To move displayed element properties on the schematic drag and drop them keeping left mouse button pressed.



6. Click on N1 button to specify wire name. Type `in1` and select wire (see picture in 7th paragraph), select next wire to name `in2` (number will increase automatically), then name `out`. To accelerate wire naming type desired names in *Wire Name* dialog box at once, for example `in1 in2 out`.



7. Enter values for all circuit element as shown in the picture below:

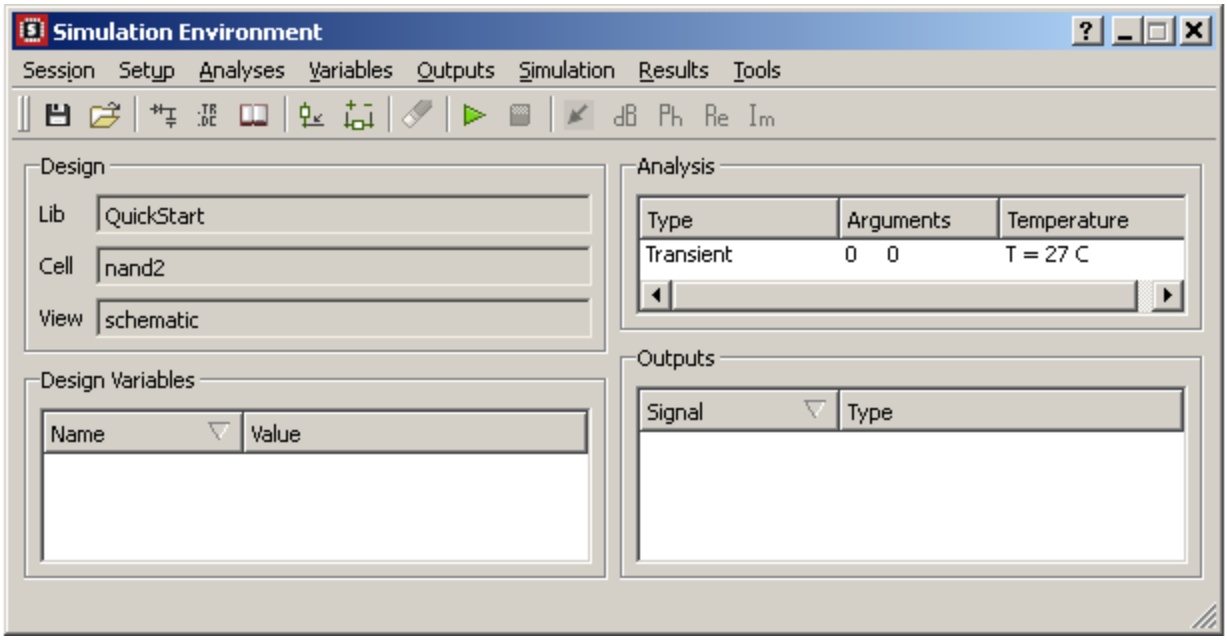


Press (Check & Save) button in the drawbar to check the electrical rules and save the schematic.

Running simulation

In the *Simulation Environment* window you can create simulation setup, specify simulation analysis, select outputs etc.

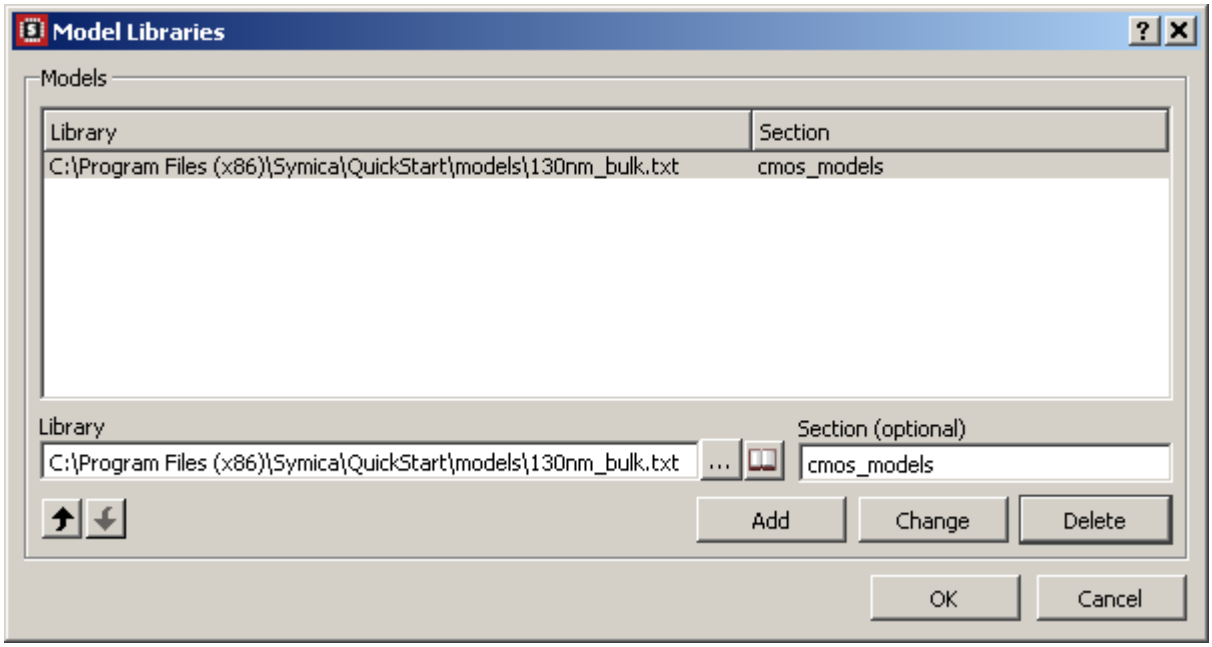
1. Click on button to open *Simulation Environment* window for the currently selected view:



2. Click on  button to specify SPICE model libraries. In the opened dialog box type library path and name or choose it from *Browse* dialog box (button ). Field *Section* is optional and intended to select part of model file. If no *Section* value is specified, the file from the field *Library* will be included in the final netlist "as is".

Examples:

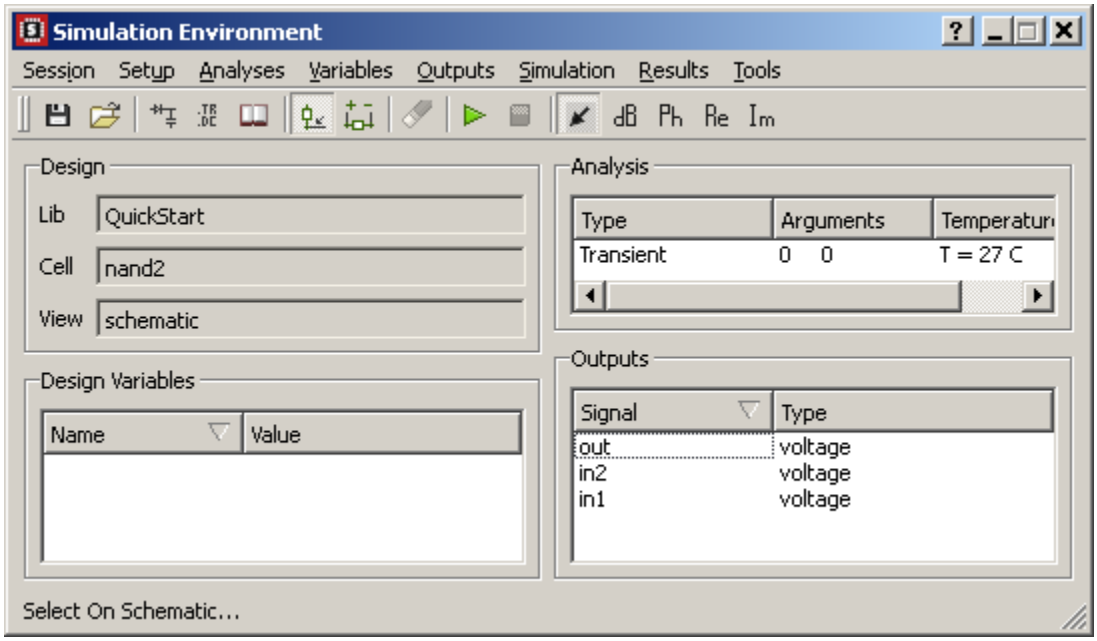
```
include "C:\Program Files (x86)\Symica\QuickStart\models\130nm_bulk.txt"
section=cmos_models
```



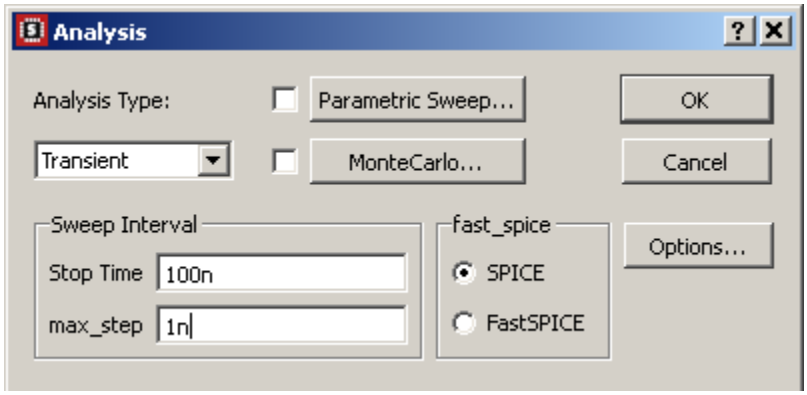
3. To specify output voltage or current click on  button and then click on the circuit node or the element pin on schematic. To deselect press on it one more time. All selected wires and pins will be highlighted by different colors.

To remove an item from *Outputs* list, select it and press key 'Del' (or click on  button).

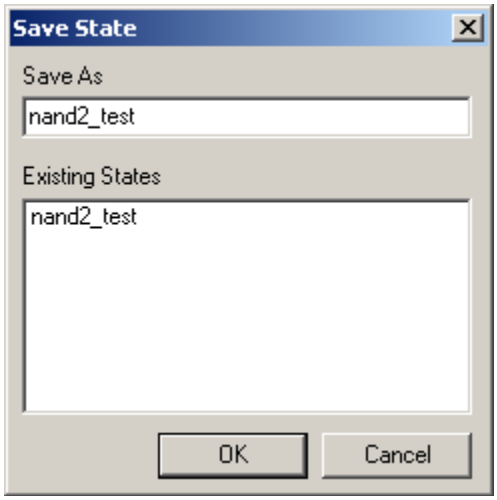
Double click on the name in *Outputs* list to highlight it on schematic.

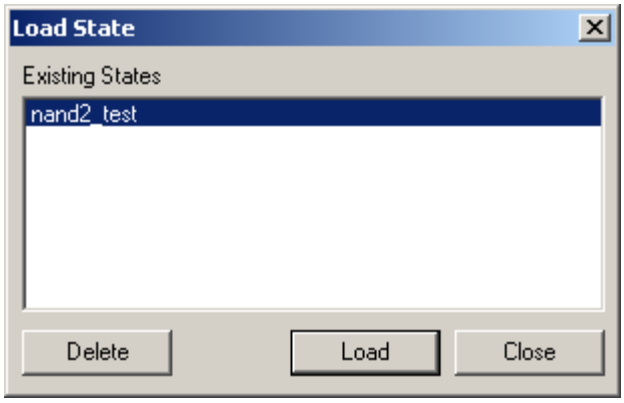


4. Select *Analyses* > *Choose...* in menu or click on  button to specify parameters of circuit analysis. Enter values as shown below and press *OK*:

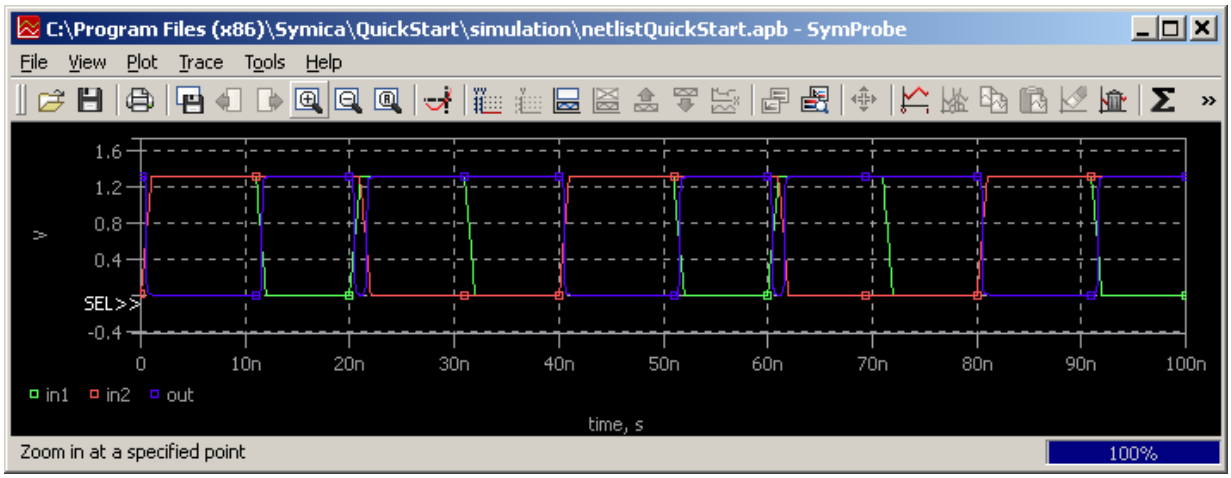


5. Select *Session -> Save State As...* in menu or click on  to save current simulation setup. All settings including model files, parameters of circuit analysis, outputs etc. will be saved. To load the state select *Session -> Load State...* or click on  .

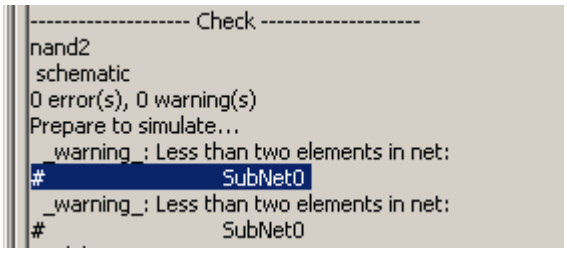




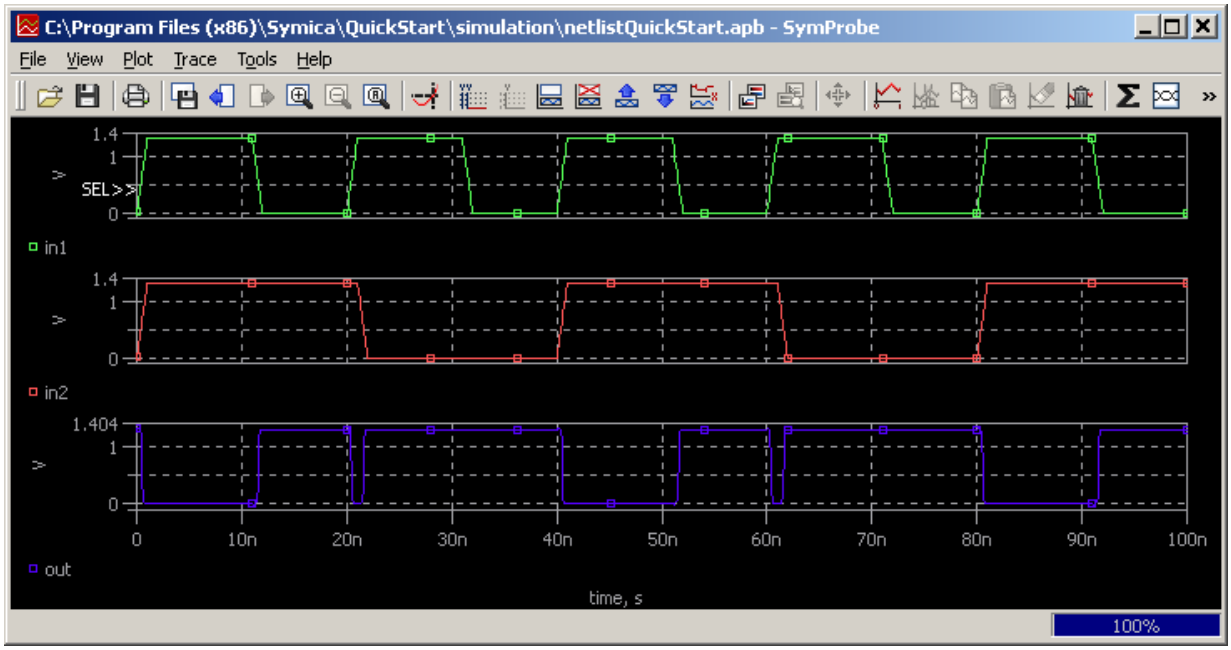
6. Click the  button to start simulation. When the simulation begins *SymProbe* window will open and waveforms will appear during the simulation process:



Electrical Rules Check always runs before simulation. If any warnings or errors appear you can see them in *Output* window. Double click on the string starting with '#' to highlight and position error or warning at schematic.



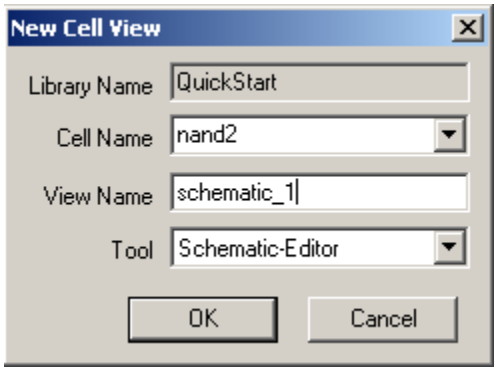
7. Press  button to separate waveforms. To combine waveforms, press  .



Creating Multiple Views

Any cell can have several views. Let's create a new schematic for the nand2 circuit which will be used as a sub-circuit in a larger circuit. For the sub-circuit, we change the voltage sources to ports.

1. Create new *schematic_1* cellview for *nand2* cell:

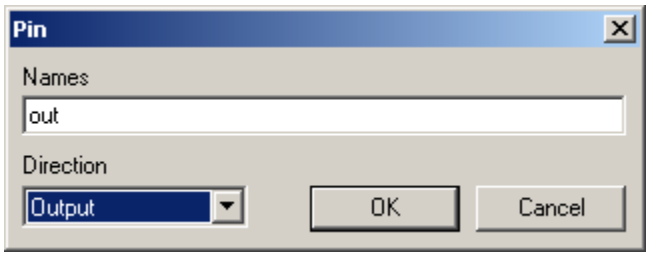


2. The new view will appear:

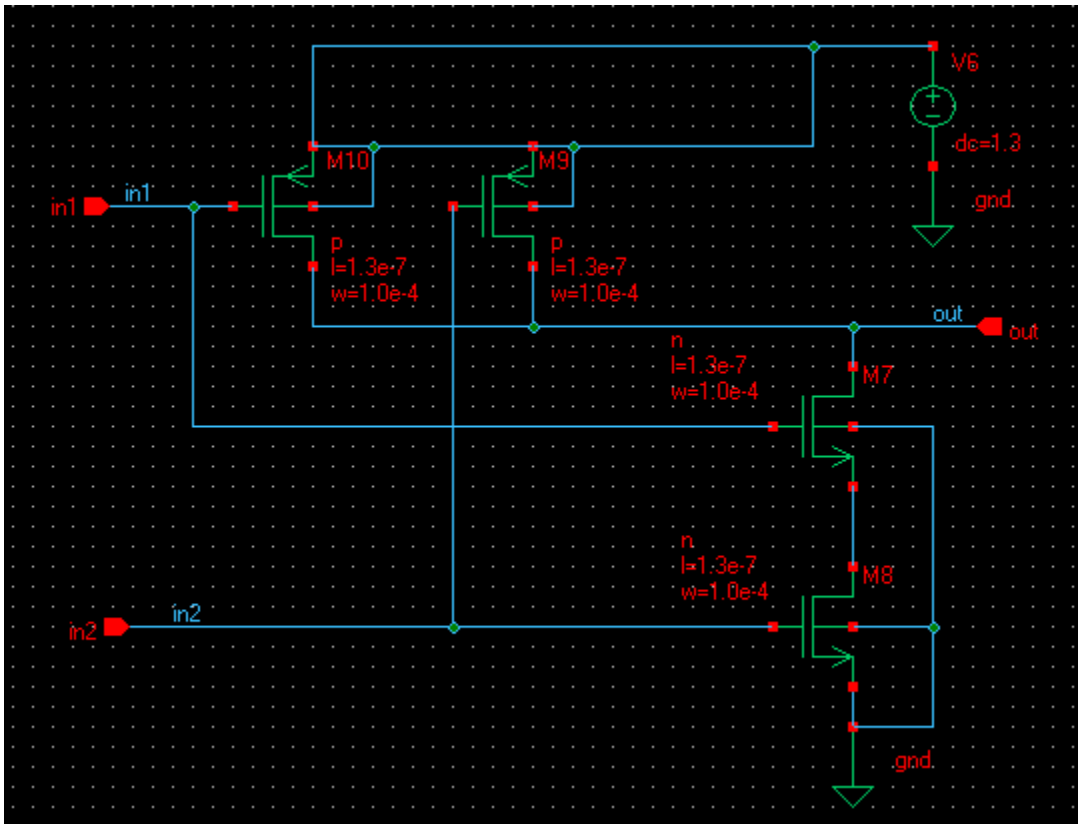
3. Copy the original circuit from *schematic* to *schematic_1* (select entire schematic by pressing 'Ctrl+a', copy it pressing 'Ctrl+c' and paste it pressing 'Ctrl+v'). Another way to copy the cellview, to use "*Copy ...*" dialog box (menu: *Edit -> Copy*).

Also use drag and drop function to copy cell or view in *Library Manager.*

4. In the view *schematic* remove input voltage sources and add ports. Click on  button (shortcut key 'p') and in the pop-up dialog box type the port name and specify its direction:



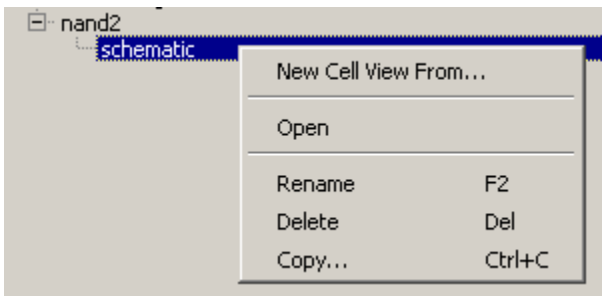
5. Place the ports as shown below:



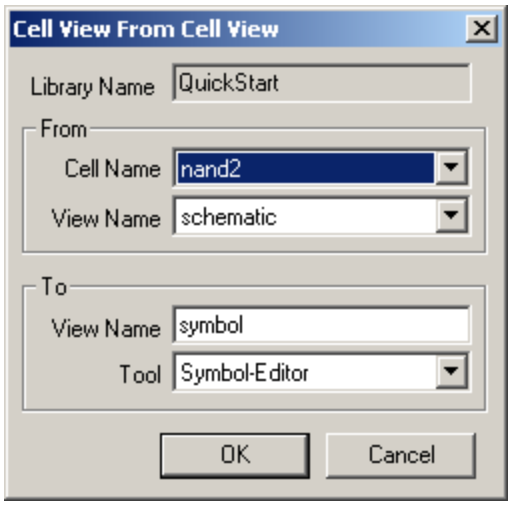
Creating the Symbol View

Most complex circuits have hierarchical structure and are built up from several subcircuits. At the upper hierarchical levels subcircuits represented with *symbol* views, which must have compatible pins with corresponding views (such as the *schematic* view).

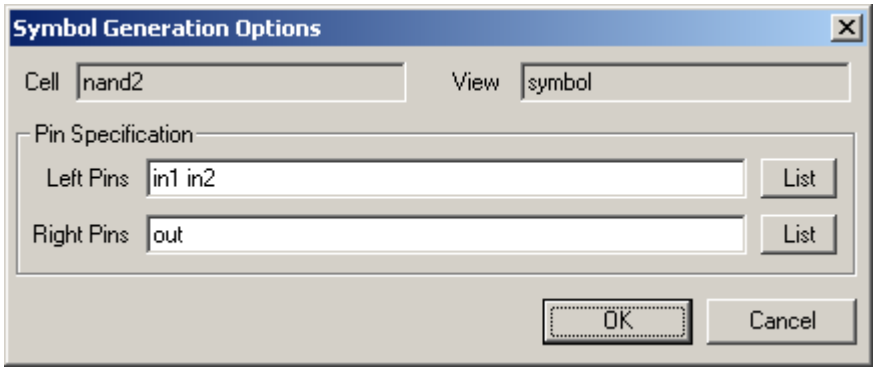
1. The easiest way to create the *symbol* view is to generate it from the *schematic* view. In the *Library manager* window, right click on the cell name, and select *New -> Cell View From...*:



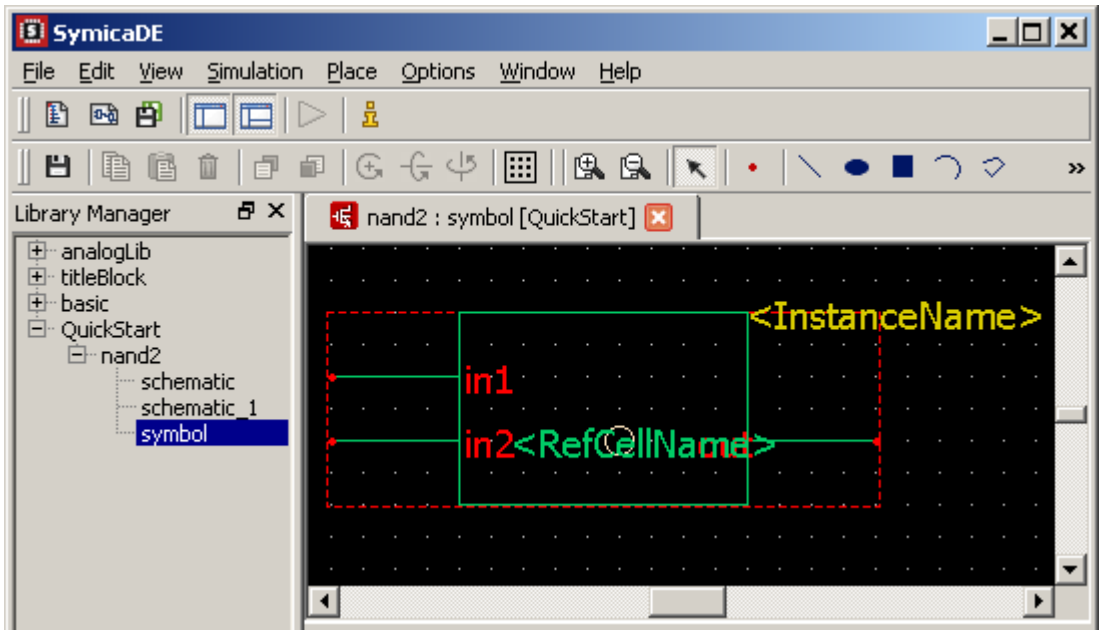
2. Setup form fields: *Cell Name* - `nand2`, *View Name* - `schematic`. In the group *'To'* set field *View Name* = `symbol`, *Tool* = `Symbol-Editor`. Press *OK.*



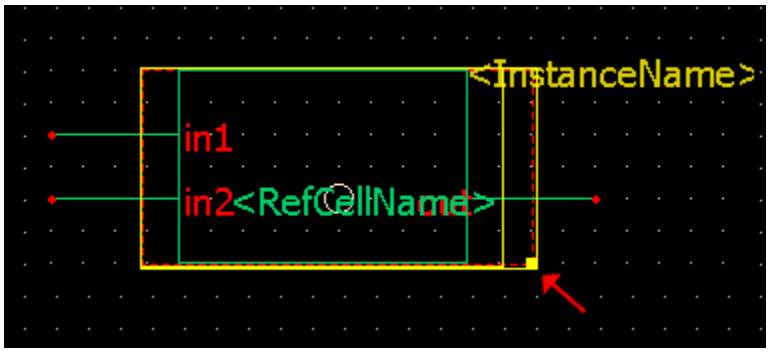
3. Check pin positions, press *OK.*



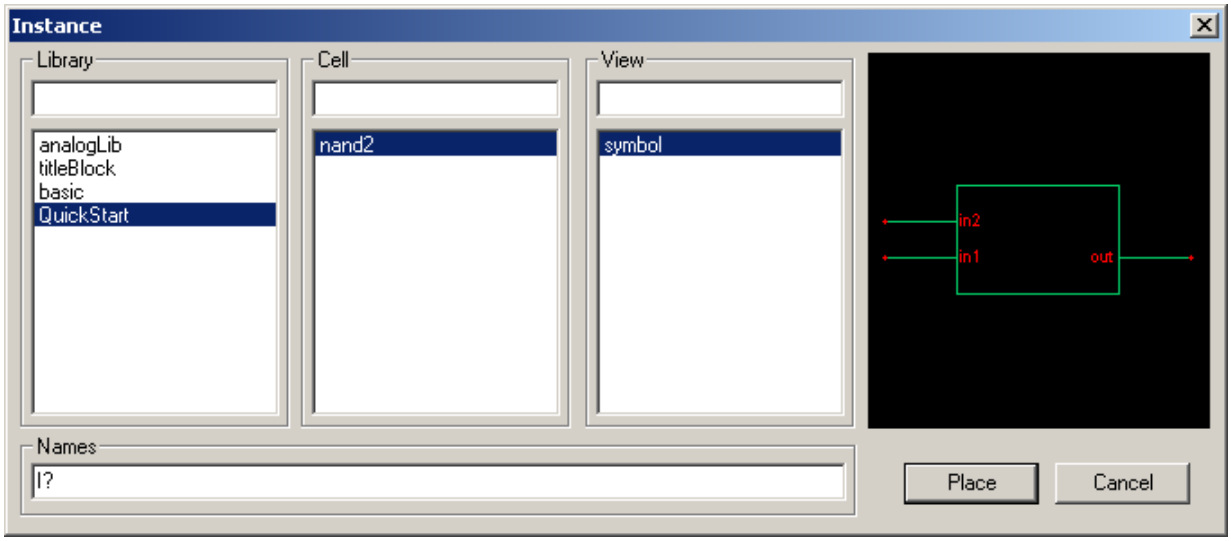
4. The new *symbol* view for cell *nand2* is created. If necessary modify the view using the *Symbol editor*.



5. Select symbol, the yellow dotted rectangle in the *Symbol editor* is a sensitivity rectangle. When clicking inside this rectangle on the schematic, the cell instance placed is selected. Sensitivity rectangle is only visible in the *Symbol editor*.



6. Within in any schematic you can open the *Instance dialog box* (press button) and place instance *nand2*.



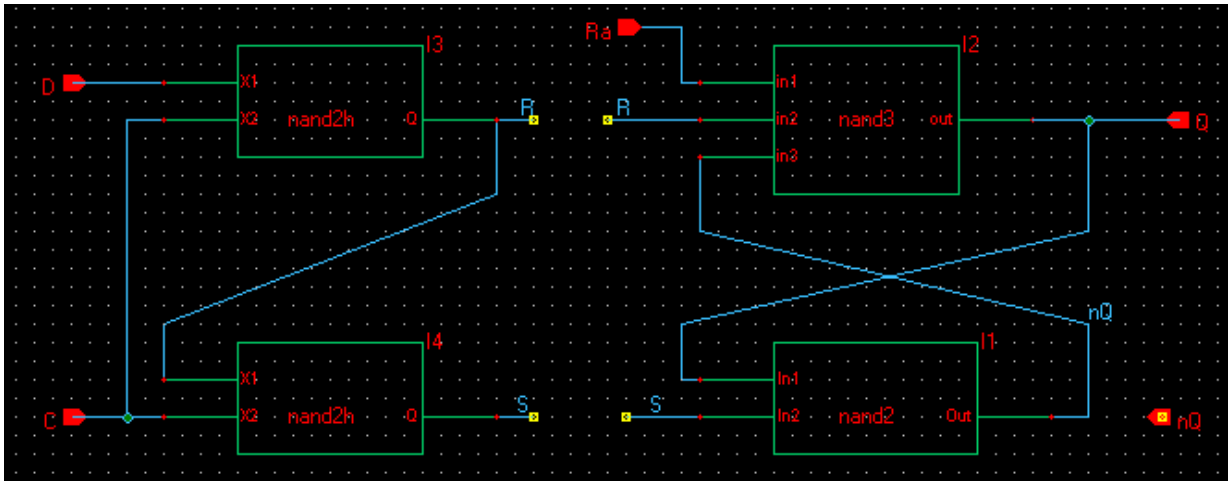
Creating the Mixed-Signal Design

This chapter shows how to create and simulate cells that contain different types of views:

- VerilogHDL
- VerilogA
- Spice Netlist

The creation of the mixed analog-digital circuit is described by designing example circuit d-latch, where:

- *nand2h* element is represented by Verilog-HDL view
- *nand3* element is represented by SPICE netlist view

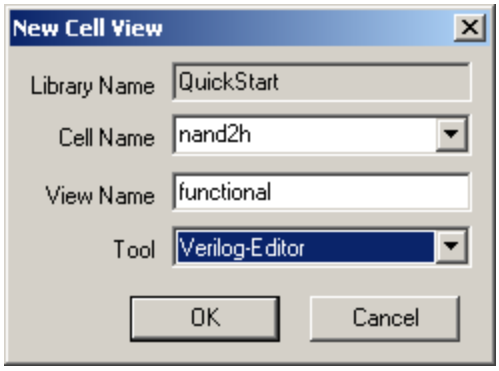


Creating the VerilogHDL View (nand2h)

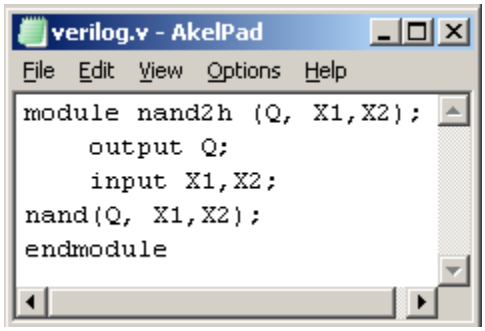
Verilog-HDL description of the nand2 element:

```
module nand2h (Q, X1,X2);
   output Q;
   input X1,X2;
nand(Q, X1,X2);
endmodule
```

1. In the *Library Manager* window right click mouse button on the library name and select *New -> New Cell View* then in pop-up dialog box select `Verilog-Editor` in the *Tool* field. The *Cell Name* must be the same as the verilog module name. Press *OK*.

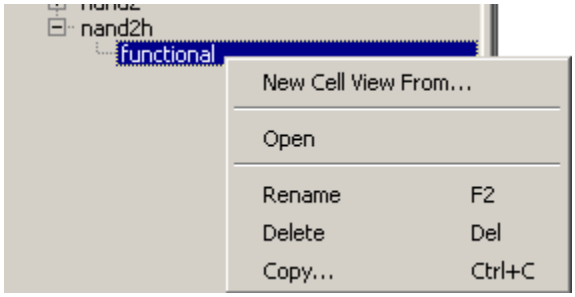


2. A text editor with the new text document "verilog.v" will be opened. Enter VerilogHDL description, save it and close text editor.

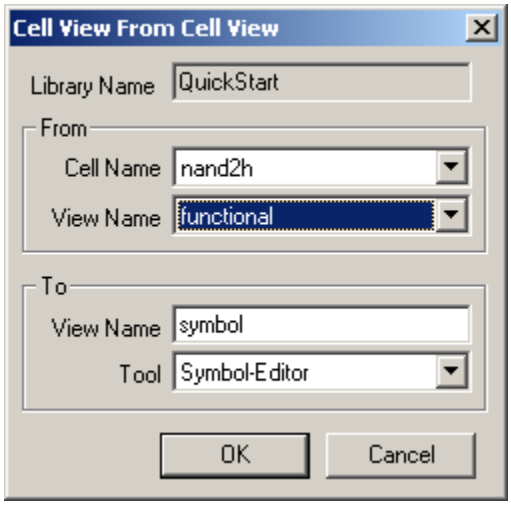


3. To create *symbol* view from the VerilogHDL description, right-click mouse button on the *functional* view in

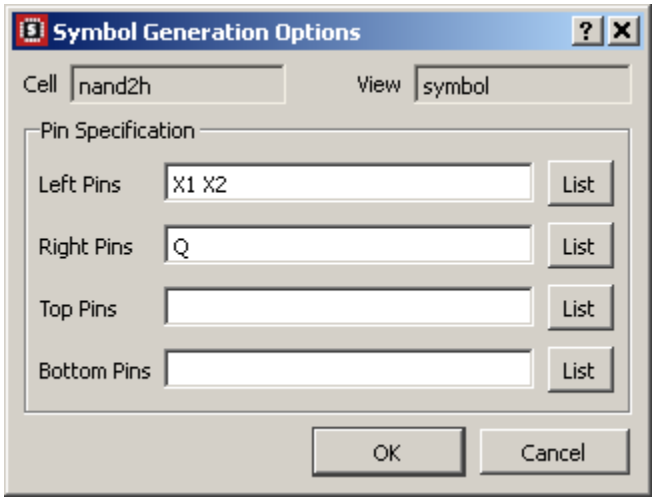
the *Library Manager* and select *New Cell View From...*



4. Press *OK.*



5. Names and pin directions will be automatically filled in. Press *OK*



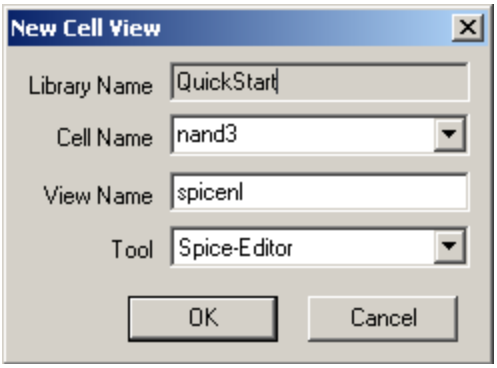
Creating the Spice Netlist View (nand3)

Spice Netlist for nand3 element:

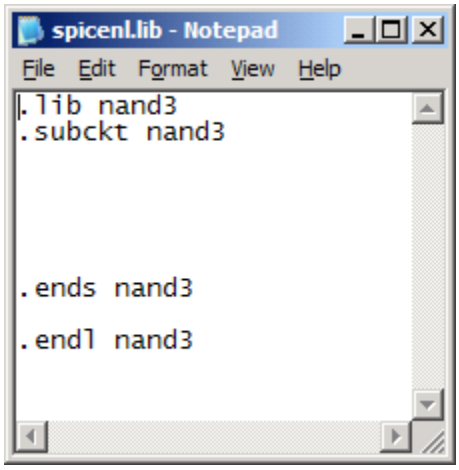
```
.lib nand3
.subckt nand3 Out In3 In1 In2
m7 n_7 in3 gnd gnd n l=1.3e-007 w=0.0001
```

```
m1 out in1 n_4 n_4 p l=1.3e-007 w=0.0001
m3 out in2 n_4 n_4 p l=1.3e-007 w=0.0001
m6 n_6 in2 n_7 gnd n l=1.3e-007 w=0.0001
m4 out in3 n_4 n_4 p l=1.3e-007 w=0.0001
m5 out in1 n_6 gnd n l=1.3e-007 w=0.0001
v2 n_4 gnd 1.3
.ends nand3
.endl nand3
```

1. Create a new cell - *nand3* (you can use button in the horizontal menu). In the field *Tool* select `Spice-Editor`.



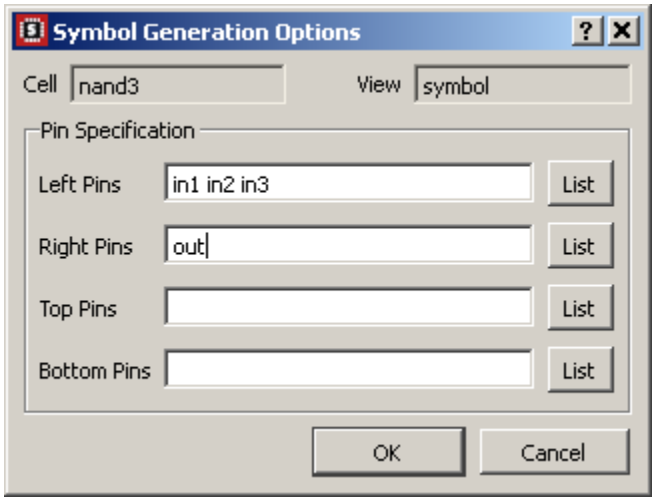
2. A text editor with a new text document "spicenl.lib" will be opened:



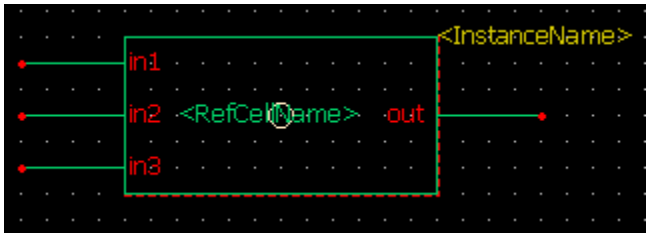
3. Enter SPICE netlist description of nand3 element, save it and close text editor.

4. Create *symbol* view for this cell (press right mouse button on the *spicenl* view and select *New Cell View From...*)

Do not forget to correct pins specification if necessary.



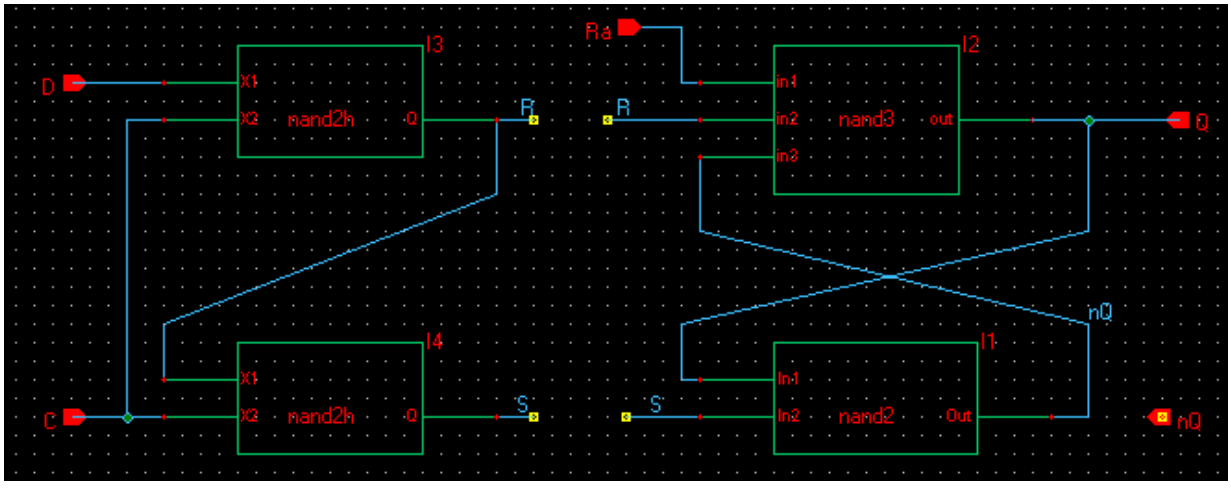
5. *Symbol* view will be created:



Creating a d-latch

The following D-latch consists of two nand2h, one nand2 and one nand3 cell.

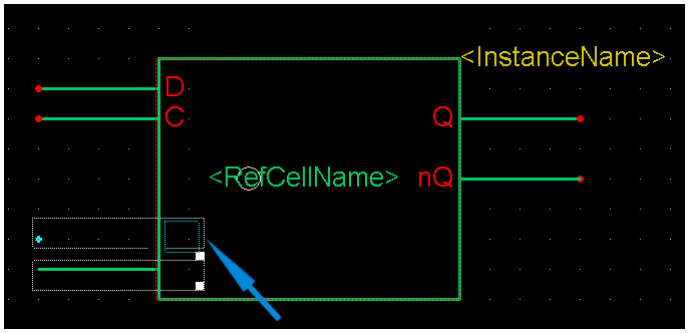
1. Draw the schematic of the d-latch as shown below:



To turn on rubber-band mode while drawing wires keep the 'Shift' button pressed.

Wires can be connected by their names (e.g. *R, S, nQ*); this can reduce wire congestion and make the schematic easier to read.

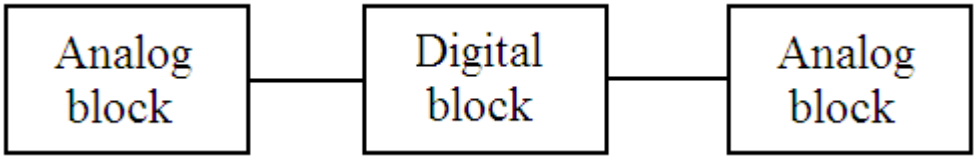
2. Create a *symbol* view of d-latch.



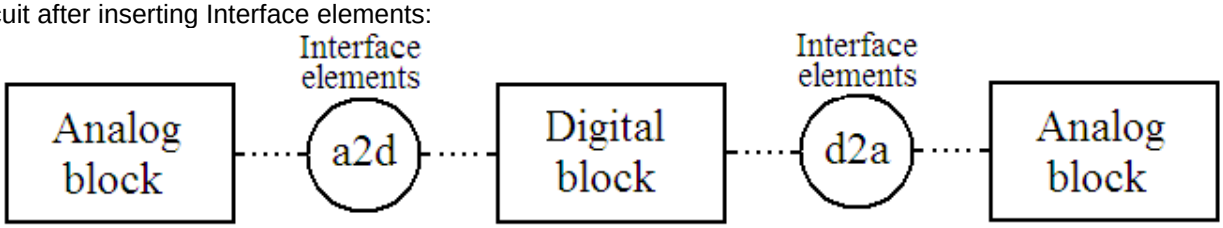
Setting a2d and d2a elements

A2d and *d2a* are the interface elements between the digital and analog sub-blocks/cells in the circuit. Interface Elements convert analog signals to logic levels and the converse. Interface elements are inserted automatically at every input and output port of each cell represented with a digital description, but they are not visible in the schematic.

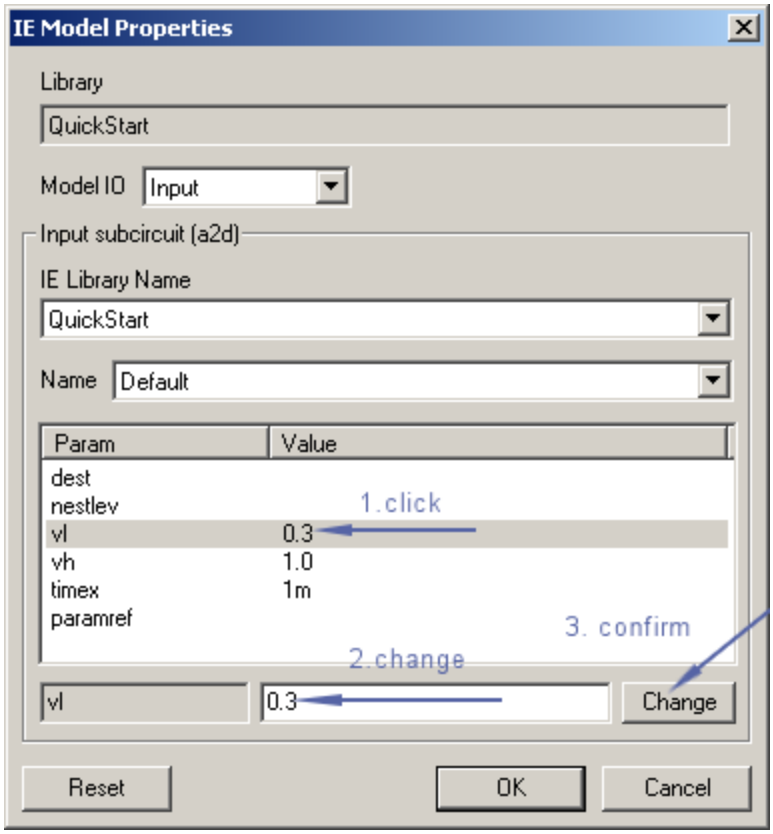
Original circuit:



Circuit after inserting Interface elements:



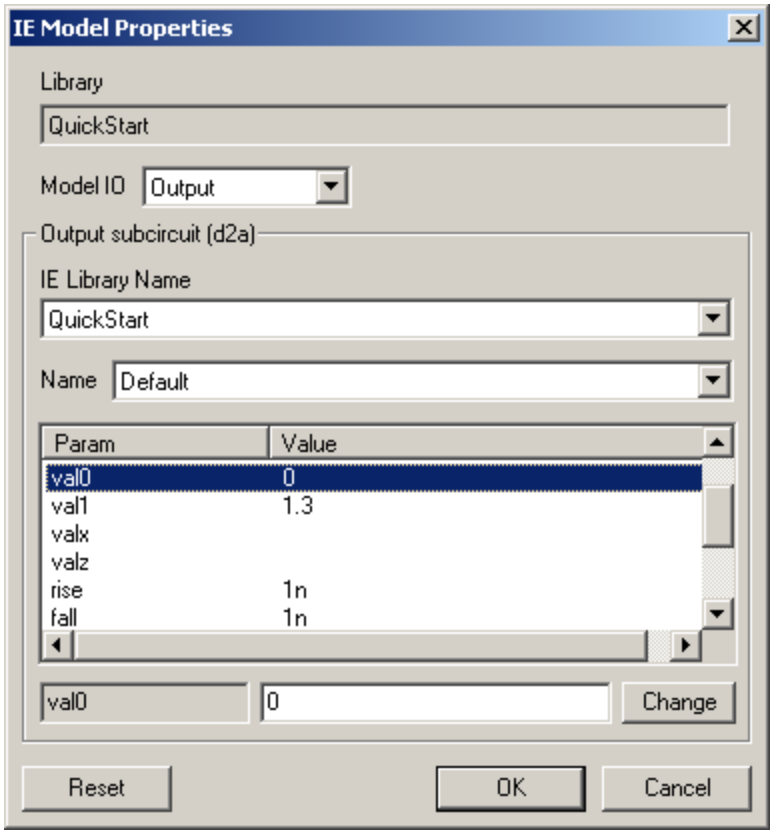
1. To configure Interface Elements select: *Simulation -> Mixed-Signal -> Interface Elements -> Cell* and click on the *nand2h* instance in the schematic. In the pop-up dialog box select and modify the values for *a2d* elements: `timex`, `vl` and `vh` as shown in the following:



`vl` - the low threshold. Voltages below this will be logical 0.
`vh` - the high threshold. Voltages above this will be logical 1.
`timex` - a voltage level between vl and vh for longer than timex yields a logic X.

If you select *Simulation -> Mixed-Signal -> Interface Elements -> Library.* Interface elements will be configured for all library cells.

2. Change values for *d2a* elements (select `Output` in the *Model IO* field):

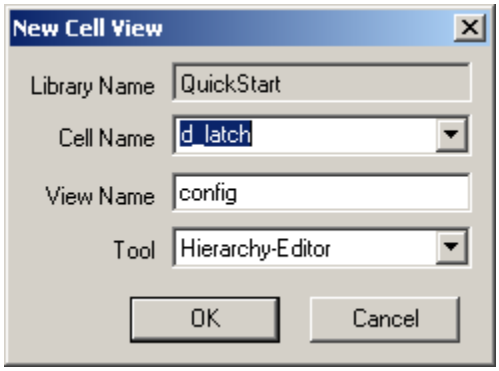


`val0` - final analog value for logical 0.
`val1` - final analog value for logical 1.
`rise` - time for transition from val0 to val1.
`fall` - time for transition from val1 to val0.

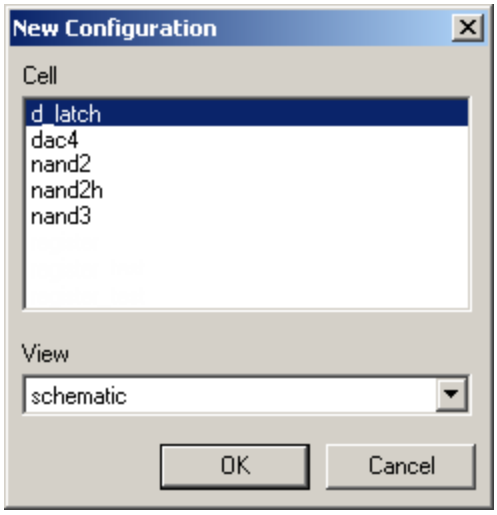
Creating the Config View

The config view allows you manage the active cellviews in a mixed-signal project while creating a netlist for further simulation.

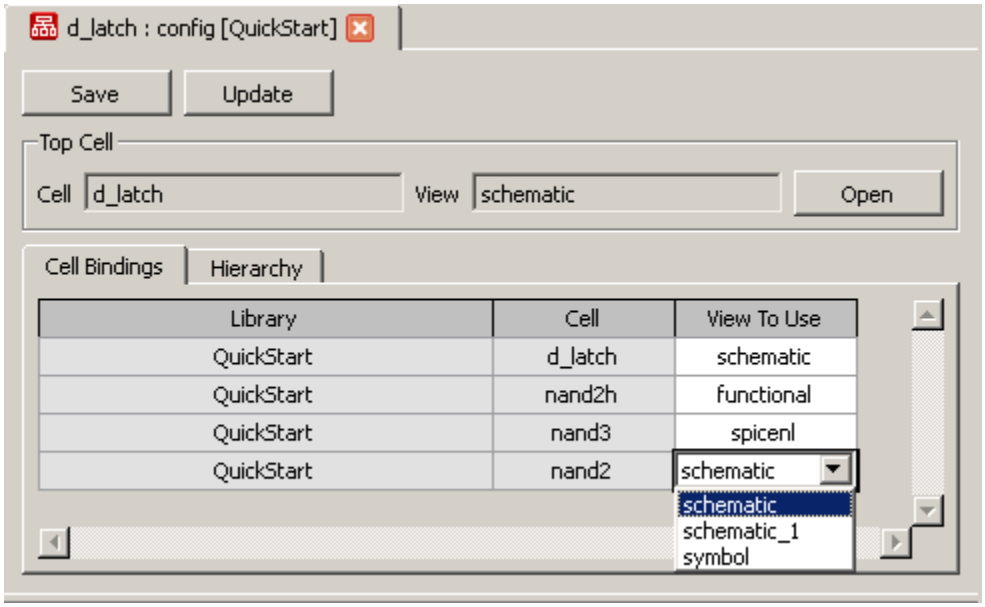
1. To create new *config* view, right click mouse button on the top-level cell in the *Library manager* window, select *New Cell View* and fill in the fields of the dialog box as shown below:



2. Select *d_latch* as a top-level cell:

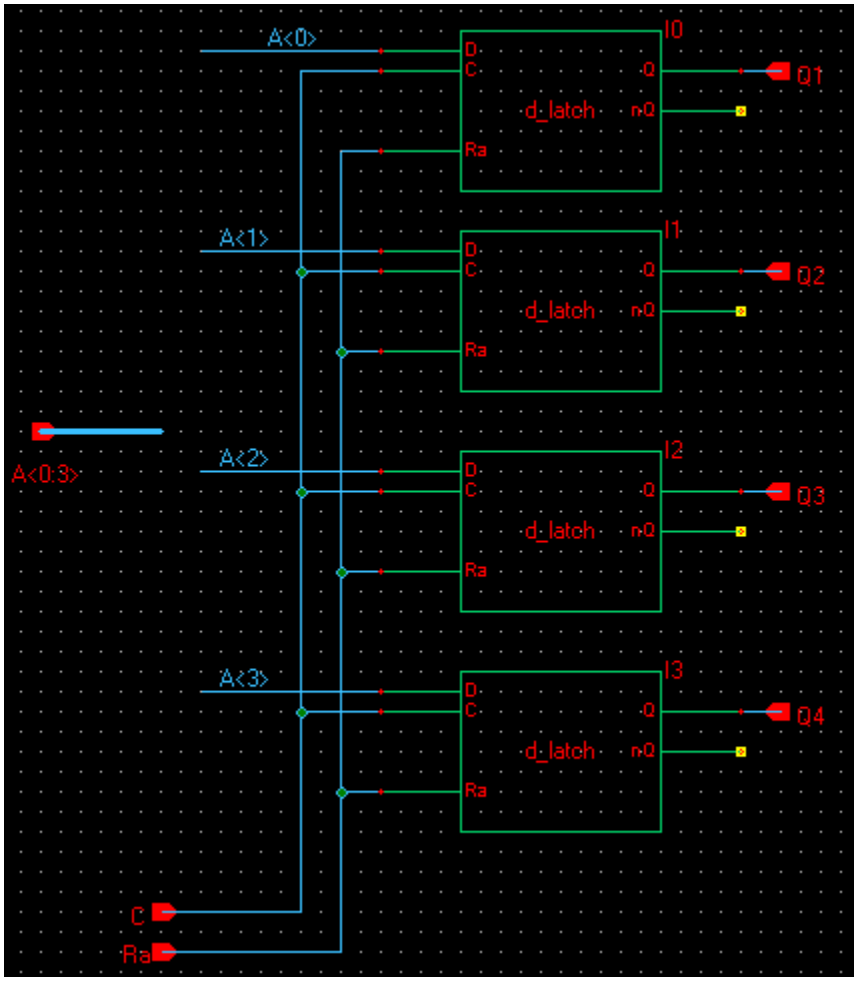


3. Double click on the name of the new *config* view. A *config* window will appear where you can specify the active cellviews that will be used to create the netlist:



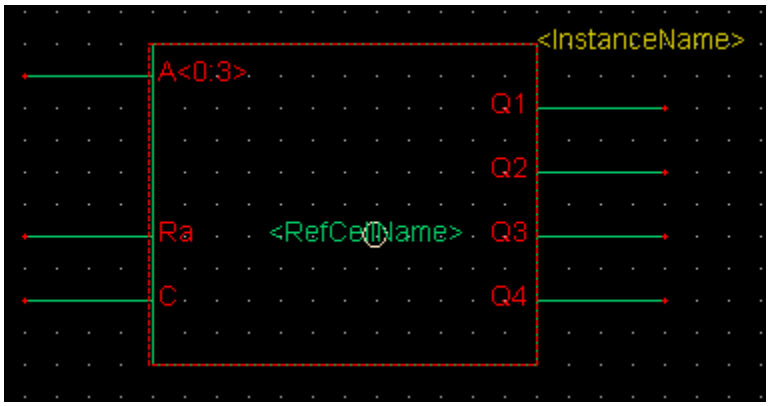
Creating a register

1. To create the new cell *register* and its *schematic* view, draw the circuit draft of the register circuit as shown below:

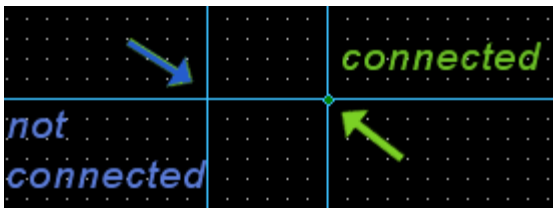


Click on button to draw bus. There are no functional differences between wire and buses; use buses to decrease congestion and increase schematic readability. To specify bus range use symbols '<' and '>'.

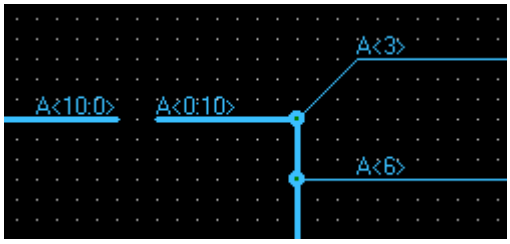
2. Create *symbol* view for register circuit:



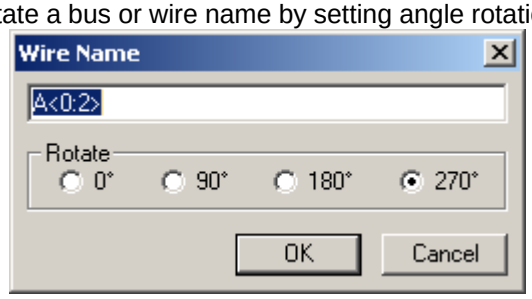
To solder two intersecting wires - press in the drawbar menu and click on the wire intersection.



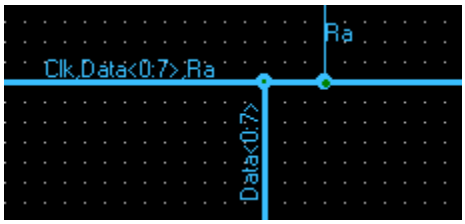
Bus-to-wire example connections:
Order doesn't matter: A<10:0> = A<0:10>



Rotate a bus or wire name by setting angle rotation in their properties:



You can combine different wires to one bundle, entering their names one by one separated with commas:



Creating the VerilogA View (dac4)

Creating a VerilogA view is identical to creating the VerilogHDL view. Let's create a Digital-to-Analog Converter cell represented in VerilogA.

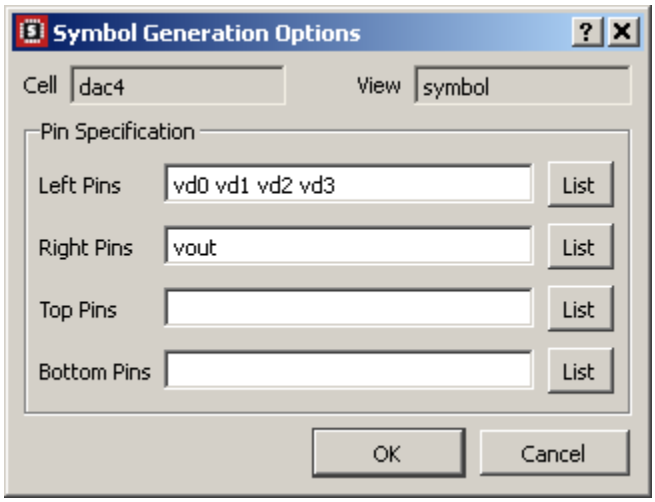
1. Create a new cell *dac4* and a new view *veriloga* by selecting tool `VerilogA-Editor` in the *New Cell View* dialog box. A text editor with a new text document "veriloga.va" will be opened. Type VerilogA description, save it and close text editor.

dac4 module description:

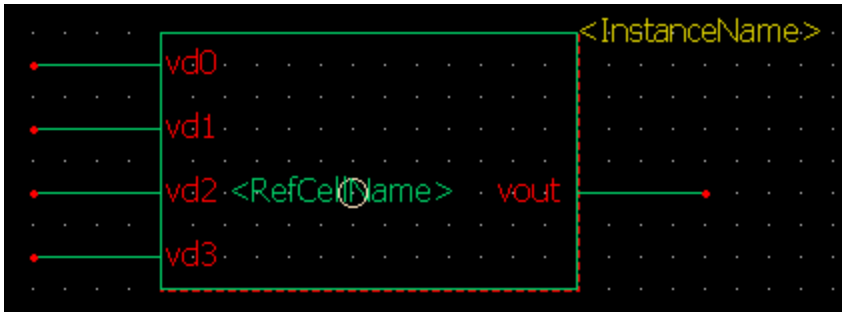
```
`include "discipline.h"
`include "constants.h"
// dac4
//
// -  4 bit digital analog converter
//
// vd0..vd3:        data inputs [V,A]
// vout:  [V,A]
//
```

```
// INSTANCE parameters
//    vref   = reference voltage that conversion is with respect to [V]
//    vtrans = transition voltage between logic high and low [V]
//    tdel,trise,tfall = {usual} [s]
//
// MODEL parameters
//    {none}

module DAC4 (vd3,vd2,vd1,vd0,vout);
input vd3, vd2, vd1, vd0;
output vout;
electrical vd3, vd2, vd1, vd0, vout;
parameter real vref  = 1 from [0:inf);
parameter real trise = 1n from [0:inf);
parameter real tfall = 1n from [0:inf);
parameter real tdel  = 1n from [0:inf);
parameter real vtrans  = 0.65;

   real out_scaled; // output scaled as fraction of 16

   analog begin
                  out_scaled = 0;
                  out_scaled = out_scaled + ((V(vd3) > vtrans) ? 8 : 0);
                  out_scaled = out_scaled + ((V(vd2) > vtrans) ? 4 : 0);
                  out_scaled = out_scaled + ((V(vd1) > vtrans) ? 2 : 0);
                  out_scaled = out_scaled + ((V(vd0) > vtrans) ? 1 : 0);
                  V(vout) <+ transition( vref*out_scaled/16, tdel, trise, tfall );
   end
endmodule
```

2. Fill in pin names:

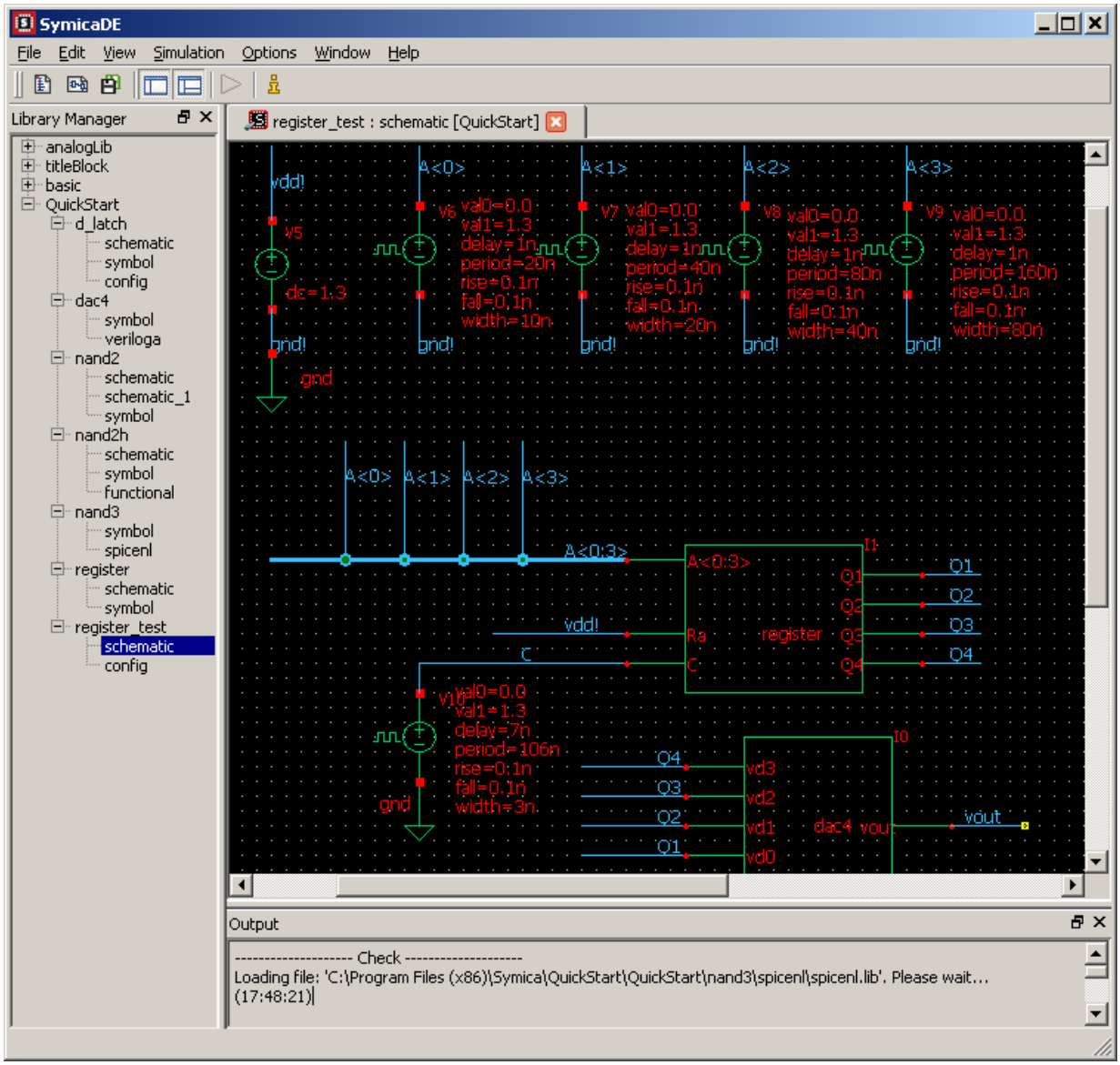


3. *Symbol* view of *dac4*:



Creating the register_test circuit

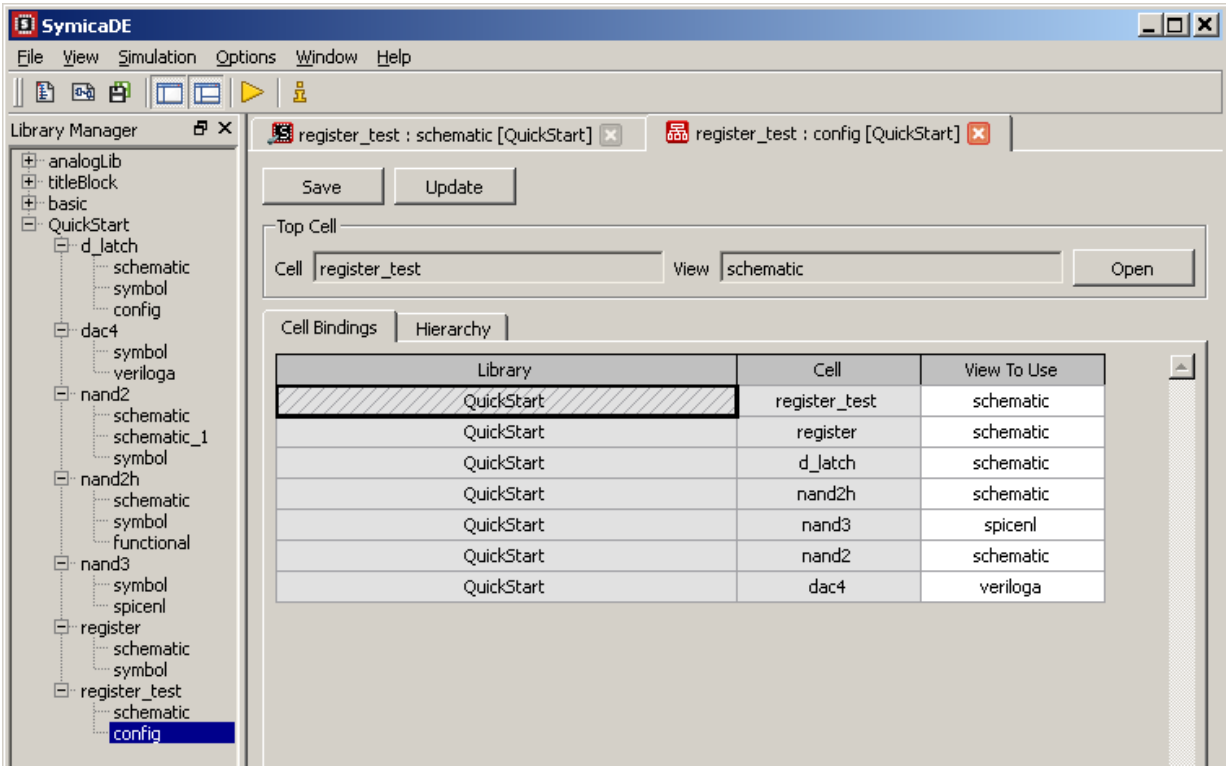
In this chapter you create the top-level test register circuit. Draw the schematic draft as shown in the picture below.



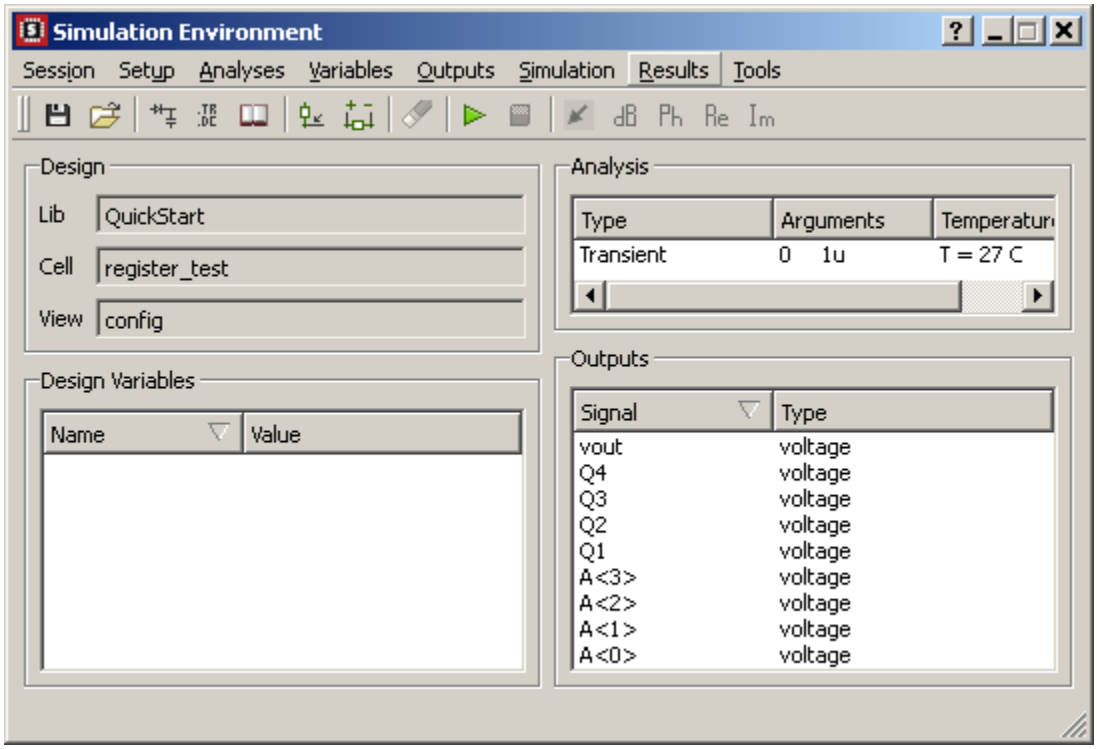
Global net is specified by '!' at the end of name.

Simulating the register_test circuit

1. Create the view *config* for the cell *register_test*.



2. Select config view and press  button to open *Simulation Environment* window, select the input and output signals that need to be displayed in SymProbe, add models library and save state as `reg_test`:

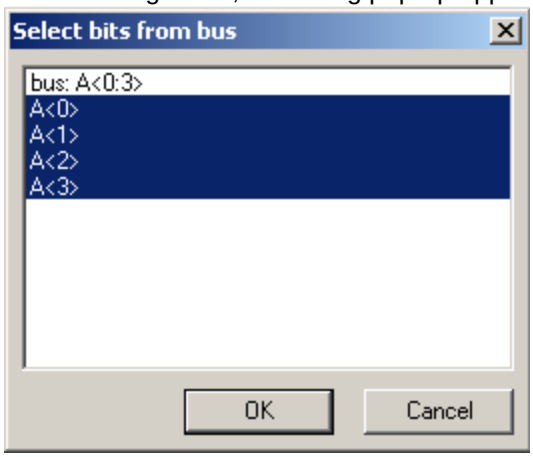


To change top-level view for current simulation task, choose *Setup -> Design* (or press).

To display netlist of the schematic, choose *Simulation -> Netlist -> Display*.

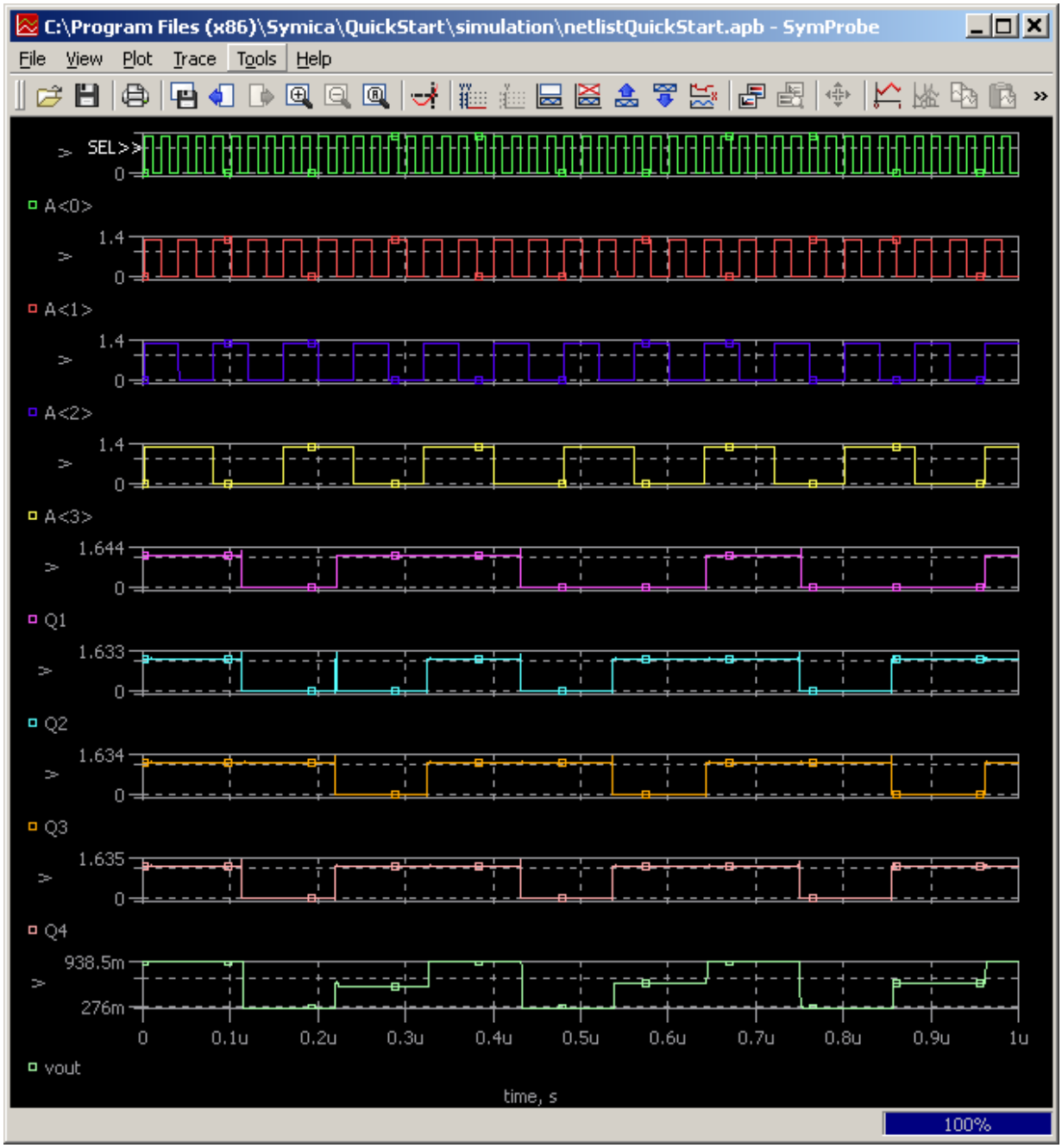
Double click on the output name to find and highlight it in schematic.

When adding a bus, the dialog pop-up appears so you can choose the individual bus bits.



3. Check the parameters of the interface elements "a2d" and "d2a" are set (*Simulation -> Mixed Signal -> Interface elements*).

4. Press to run simulation. The following waveforms should be calculated:

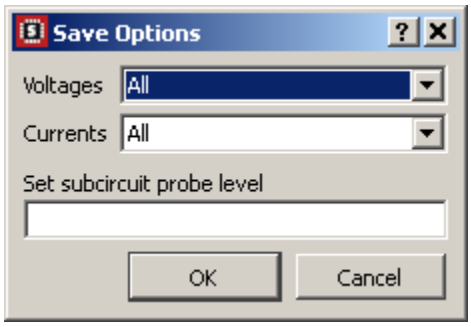


Appendix

Direct Plot

Another approach to display waveforms is the Direct Plot. In this case you can run the simulation first and then add signals to plot.

1. Before running simulation go to Simulation Environment\Outputs -> Save All... to save all required signals.



2. Run Simulation.

Direct Plot supports two ways for the plotting:

3a. Plotting one waveform immediately after you selected it in the Schematic window.
To enter this mode go to Results -> Direct Plot -> Main Form... and start selecting signals.

3b. Plotting several waveforms together after you press ESC.
To enter this mode go to Results -> Direct Plot -> Transient Signal..., then click on the signals you want to plot and press ESC.

Toolbars

Toolbar, Drawbar and Element toolbar description:

Button	Name	Description
	Create Library	Create a new library
	Create Cell View	Create a new cell in active library
	Save All	Save all
	Library manager	Hide/display *Library manager* window
	Output	Hide/display *Output window*
	Simulation Environment	Open *Simulation Environment* window
	About program	Information about the program

Button	Name	Description
	Check&Save	Electrical rules check and save

	**Copy**	Copy the selected object or group of objects on the Clipboard
	**Paste**	Paste the object or group of objects from the Clipboard
	**Delete**	Delete the selected object or group of objects
	**Print**	Print the draft
	**Undo**	Cancel previous command
	**Redo**	Cancel Undo command
	**Rotate**	Rotate the selected object or group of objects to 90° counterclockwise
	**Zoom in**	Scale up the image
	**Zoom out**	Scale down the image
	**Select**	Select mode
	**Element**	Place element from the library
	**Wire(narrow)**	Draw wires
	**Wire(wide)**	Draw bus
	**Net\bus alias**	Place net\bus alias
	**Solder dot**	Place junction – point of two connections
	**Port**	Place port
	**Line**	Draw line
	**Rectangle**	Draw rectangle
	**Text**	Place text

Button	Name	Description
	**Source**	Place current or voltage source
	**Basic**	Place resistor, capacitor, inductor or diode
	**Transistor**	Place bipolar or MOS transistor
	**Common Cell**	Place cell from your library
	**Ground**	Place ground

Hotkeys

File

New library	`Alt + n`
New cellview	`Alt + v`
Open Library	`Ctrl + o`
Exit	`Alt + x`

Simulation

Next error	`F4`
Previous error	`Shift + F4`
Simulation Environment	`F5`

Schematic

Check & Save	`x`

Schematic - > **Edit**

Undo	`Ctrl + z, u`
Redo	`Ctrl + y, U`
Cut	`Ctrl + x`

Copy	Ctrl + c
Paste	Ctrl + v
Delete	Del
Select all	Ctrl + a
Find	Ctrl + f
Property	q
Rotate	r
Mirror (vertical)	v
Mirror (horizontal)	h

Schematic - > **View**

Ascend hierarchy	Ctrl + e
Descend hierarchy	Shift + e
Zoom in	+(NumPad),]
Zoom out	−(NumPad), [
Region	z
Fit the window	*(NumPad), f

Schematic - > **Place**

Instance...	i
Wire (narrow)	w
Wire (wide)	W
Wire Name	l
Solder Dot	j
Pin	p
Text	t

Schematic - > **Print**

Print	Ctrl + p

Symbol

Subst. field	l
Text	L

Help

User`s Manual	F1

Transistor Models

```
.lib cmos_models

.model N NMOS
+Level = 49

+Lint = 2.5e-08 Tox = 3.3e-09
+Vth0 = 0.332 Rdsw = 200

+lmin=1.3e-7 lmax=1.3e-7 wmin=1.3e-7 wmax=1.0e-4 Tref=27.0 version =3.1
+Xj= 4.5000000E-08          Nch= 5.6000000E+17
+lln= 1.0000000            lwn= 0.00                   wln= 0.00
+wwn= 1.0000000            ll= 0.00
+lw= 0.00                  lwl= 0.00                   wint= 0.00
+wl= 0.00                  ww= 0.00                    wwl= 0.00
+Mobmod= 1                 binunit= 2                  xl= 0
+xw= 0                     binflag=  0
+Dwg= 0.00                 Dwb= 0.00
```

```
+K1= 0.3661500              K2= 0.00
+K3= 0.00                   Dvt0= 8.7500000           Dvt1= 0.7000000
+Dvt2= 5.0000000E-02        Dvt0w= 0.00               Dvt1w= 0.00
+Dvt2w= 0.00               Nlx= 3.5500000E-07        W0= 0.00
+K3b= 0.00                  Ngate= 5.0000000E+20

+Vsat= 1.3500000E+05        Ua= -1.8000000E-09        Ub= 2.2000000E-18
+Uc= -2.9999999E-11         Prwb= 0.00
+Prwg= 0.00                 Wr= 1.0000000             U0= 1.3400000E-02
+A0= 2.1199999              Keta= 4.0000000E-02       A1= 0.00
+A2= 0.9900000              Ags= -0.1000000           B0= 0.00
+B1= 0.00

+Voff= -7.9800000E-02       NFactor= 1.1000000        Cit= 0.00
+Cdsc= 0.00                 Cdscb= 0.00               Cdscd= 0.00
+Eta0= 4.0000000E-02        Etab= 0.00                Dsub= 0.5200000

+Pclm= 0.1000000            Pdiblc1= 1.2000000E-02    Pdiblc2= 7.5000000E-03
+Pdiblcb= -1.3500000E-02    Drout= 0.2800000          Pscbe1= 8.6600000E+08
+Pscbe2= 1.0000000E-20      Pvag= -0.2800000          Delta= 1.0100000E-02
+Alpha0= 0.00               Beta0= 30.0000000

+kt1= -0.3400000            kt2= -5.2700000E-02       At= 0.00
+Ute= -1.2300000            Ua1= -8.6300000E-10       Ub1= 2.0000001E-18
+Uc1= 0.00                  Kt1l= 4.0000000E-09       Prt= 0.00

+Cj= 0.0015                 Mj= 0.7175511             Pb= 1.24859
+Cjsw= 2E-10                Mjsw= 0.3706993           Php= 0.7731149
+Cta= 9.290391E-04          Ctp= 7.456211E-04         Pta= 1.527748E-03
+Ptp= 1.56325E-03           JS=2.50E-08               JSW=4.00E-13
+N=1.0                      Xti=3.0                   Cgdo=2.75E-10
+Cgso=2.75E-10              Cgbo=0.0E+00              Capmod= 2
+NQSMOD= 0                  Elm= 5                    Xpart= 1
+Cgsl= 1.1155E-10           Cgdl= 1.1155E-10          Ckappa= 0.8912
+Cf= 1.113e-10              Clc= 5.475E-08            Cle= 6.46
+Dlc= 2E-08                 Dwc= 0                    Vfbcv= -1


.model P PMOS
+Level = 49

+Lint = 2.e-08 Tox = 3.3e-09
+Vth0 = -0.3499 Rdsw = 400

+lmin=1.3e-7 lmax=1.3e-7 wmin=1.3e-7 wmax=1.0e-4 Tref=27.0 version =3.1
+Xj= 4.5000000E-08          Nch= 6.8500000E+18
+lln= 0.00                  lwn= 0.00                 wln= 0.00
+wwn= 0.00                  ll= 0.00
+lw= 0.00                   lwl= 0.00                 wint= 0.00
+wl= 0.00                   ww= 0.00                  wwl= 0.00
+Mobmod=  1                 binunit= 2                xl=  0
+xw=  0                     binflag=  0
+Dwg= 0.00                  Dwb= 0.00

+K1= 0.4087000              K2= 0.00
+K3= 0.00                   Dvt0= 5.0000000           Dvt1= 0.2600000
+Dvt2= -1.0000000E-02       Dvt0w= 0.00               Dvt1w= 0.00
+Dvt2w= 0.00               Nlx= 1.6500000E-07        W0= 0.00
+K3b= 0.00                  Ngate= 5.0000000E+20

+Vsat= 1.0500000E+05        Ua= -1.4000000E-09        Ub= 1.9499999E-18
+Uc= -2.9999999E-11         Prwb= 0.00
+Prwg= 0.00                 Wr= 1.0000000             U0= 5.2000000E-03
+A0= 2.1199999              Keta= 3.0300001E-02       A1= 0.00
```

```
+A2= 0.4000000              Ags= 0.1000000              B0= 0.00
+B1= 0.00

+Voff= -9.10000000E-02      NFactor= 0.1250000          Cit= 2.7999999E-03
+Cdsc= 0.00                 Cdscb= 0.00                 Cdscd= 0.00
+Eta0= 80.0000000           Etab= 0.00                  Dsub= 1.8500000

+Pclm= 2.5000000            Pdiblc1= 4.8000000E-02      Pdiblc2= 5.0000000E-05
+Pdiblcb= 0.1432509         Drout= 9.0000000E-02        Pscbe1= 1.0000000E-20
+Pscbe2= 1.0000000E-20      Pvag= -6.0000000E-02        Delta= 1.0100000E-02
+Alpha0= 0.00               Beta0= 30.0000000

+kt1= -0.3400000            kt2= -5.2700000E-02         At= 0.00
+Ute= -1.2300000            Ua1= -8.6300000E-10         Ub1= 2.0000001E-18
+Uc1= 0.00                  Kt1l= 4.0000000E-09         Prt= 0.00

+Cj= 0.0015                 Mj= 0.7175511               Pb= 1.24859
+Cjsw= 2E-10                Mjsw= 0.3706993             Php= 0.7731149
+Cta= 9.290391E-04          Ctp= 7.456211E-04           Pta= 1.527748E-03
+Ptp= 1.56325E-03           JS=2.50E-08                JSW=4.00E-13
+N=1.0                      Xti=3.0                    Cgdo=2.75E-10
+Cgso=2.75E-10              Cgbo=0.0E+00               Capmod= 2
+NQSMOD= 0                  Elm= 5                     Xpart= 1
+Cgsl= 1.1155E-10           Cgdl= 1.1155E-10           Ckappa= 0.8912
+Cf= 1.113e-10              Clc= 5.475E-08             Cle= 6.46
+Dlc= 2E-08                 Dwc= 0                     Vfbcv= -1

.endl
```

Netlist

```
*** Title: "C:\Program Files\Symica\SAMPLES\SymicaDE\QuickStart\simulation\netlistQuickStart.cir"
*** Generated by:  Symica
*** © 2009-2011 Symica. All rights reserved. (www.symica.com)
*** Generated for: SymSpice
*** Generated on:  Mon Mar 14 16:47:12 2011
************************************************************************
*** This is a root file of the project
************************************************************************

simulator lang=local

global gnd vdd!

include "C:\Program Files\Symica\SAMPLES\SymicaDE\QuickStart\..\models\130nm_bulk.txt" section=cmos_models
include "C:\Program Files\Symica\SAMPLES\SymicaDE\QuickStart\nand3\spicenl\spicenl.lib" section=nand3
ahdl_include "C:\Program Files\Symica\SAMPLES\SymicaDE\QuickStart\dac4\veriloga\veriloga.va"



*** Title: "C:\Program Files\Symica\SAMPLES\SymicaDE\QuickStart\simulation\netlistQuickStart.dcv"
*** Generated by:  Symica
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*** Generated for: SymSpice
*** Generated on:  Mon Mar 14 16:47:12 2011
************************************************************************

simulator lang=local



*** Title: "C:\Program Files\Symica\SAMPLES\SymicaDE\QuickStart\simulation\netlistQuickStart.net"
*** Generated by:  Symica
*** © 2009-2011 Symica. All rights reserved. (www.symica.com)
*** Generated for: SymSpice
```

```
*** Generated on:  Mon Mar 14 16:47:12 2011
**********************************************************************

simulator lang=local


parameters

v9 a_3 gnd vsource type=pulse val0=0 val1=1.3 delay=1e-009 period=1.6e-007 rise=1e-010 fall=1e-010 width=8e-008
v8 a_2 gnd vsource type=pulse val0=0 val1=1.3 delay=1e-009 period=8e-008 rise=1e-010 fall=1e-010 width=4e-008
v7 a_1 gnd vsource type=pulse val0=0 val1=1.3 delay=1e-009 period=4e-008 rise=1e-010 fall=1e-010 width=2e-008
v6 a_0 gnd vsource type=pulse val0=0 val1=1.3 delay=1e-009 period=2e-008 rise=1e-010 fall=1e-010 width=1e-008
v10 c gnd vsource type=pulse val0=0 val1=1.3 delay=7e-009 period=1.06e-007 rise=1e-010 fall=1e-010 width=3e-009
v5 vdd! gnd vsource type=dc dc=1.3
_ie999997 c gnd a2d dest="999997" vl=0.3 vh=1.0 timex=1m
_ie999996 a_0 gnd a2d dest="999996" vl=0.3 vh=1.0 timex=1m
_ie999995 a_1 gnd a2d dest="999995" vl=0.3 vh=1.0 timex=1m
_ie999994 a_2 gnd a2d dest="999994" vl=0.3 vh=1.0 timex=1m
_ie999993 a_3 gnd a2d dest="999993" vl=0.3 vh=1.0 timex=1m
i1 q2 q3 q4 a_0 a_1 a_2 a_3 vdd! c q1 register
i0 q4 q3 q2 q1 vout dac4

subckt register q2 q3 q4 a_0 a_1 a_2 a_3 ra c q1
i0 q1 n_0 ra c a_0 d_latch
i1 q2 n_1 ra c a_1 d_latch
i2 q3 n_2 ra c a_2 d_latch
i3 q4 n_3 ra c a_3 d_latch
ends

subckt d_latch q nq ra c d
_ie999999 s gnd d2a src="999999" val0=0 val1=1.3 rise=3n fall=2n
_ie999998 r gnd d2a src="999998" val0=0 val1=1.3 rise=3n fall=2n
i2 q nq ra r nand3
i0 s q nq nand2
ends

subckt nand2 in2 in1 out
v6 n_3 gnd vsource type=dc dc=1.3
m7 out in1 n_5 gnd n w=0.0001 l=1.3e-007
m8 n_5 in2 gnd gnd n w=0.0001 l=1.3e-007
m9 out in2 n_3 n_3 p w=0.0001 l=1.3e-007
m10 out in1 n_3 n_3 p w=0.0001 l=1.3e-007
ends

*** Title: "C:\Program Files\Symica\SAMPLES\SymicaDE\QuickStart\simulation\netlistQuickStart.sim"
*** Generated by:  Symica
*** © 2009-2011 Symica. All rights reserved. (www.symica.com)
*** Generated for: SymSpice
*** Generated on:  Mon Mar 14 16:47:12 2011
**********************************************************************

simulator lang=local


timesweep tran start=0.000000e+000 stop=1.000000e-006 maxstep=1.000000e-009 method=trap lteratio=3.500000e+000

save a_0 a_1 a_2 a_3 q1 q2 q3 q4 vout

saveoptions options save=selected currents=selected

default_options options tnom=2.700000e+001 temp=2.700000e+001  fast_spice=0 reltol=1.000000e-003
```

Netlist Verilog

```
// Generated by:  Symica(r), Copyright (c) 2008, Symica
// Generated for: verilog
// Generated on:  Mon Mar 14 16:47:12 2011

`timescale 1 ns / 1 ns

`include "C:\Program Files\Symica\SAMPLES\SymicaDE\QuickStart\nand2h\functional\verilog.v"
```

```
`timescale 1 ns / 1 ns

`define _VMX_SIMULATOR_NAME_ "local"
`define _VMX_MAX_DC_ITER_ 0
`define _VMX_DC_INTERVAL_ 0

module register_test ();

	integer dc_mode_flag;
	integer output_change_count;
	integer max_dc_iter;
	integer dc_iterations;
	time vmx_time_offset;


	initial begin
		$vmx_initialize( `_VMX_SIMULATOR_NAME_ , dc_mode_flag);
		$vmx_define_export(register_test.I1.I0.net4, "i1/i0/999999");
		$vmx_define_export(register_test.I1.I1.net4, "i1/i1/999999");
		$vmx_define_export(register_test.I1.I2.net4, "i1/i2/999999");
		$vmx_define_export(register_test.I1.I3.net4, "i1/i3/999999");
		$vmx_define_export(register_test.I1.I0.net3, "i1/i0/999998");
		$vmx_define_export(register_test.I1.I1.net3, "i1/i1/999998");
		$vmx_define_export(register_test.I1.I2.net3, "i1/i2/999998");
		$vmx_define_export(register_test.I1.I3.net3, "i1/i3/999998");
		$vmx_define_import(register_test.mixedNet999997, "999997");
		$vmx_define_import(register_test.mixedNet999996, "999996");
		$vmx_define_import(register_test.mixedNet999995, "999995");
		$vmx_define_import(register_test.mixedNet999994, "999994");
		$vmx_define_import(register_test.mixedNet999993, "999993");
		$vmx_end_definition;

		vmx_time_offset = 0;
		max_dc_iter = `_VMX_MAX_DC_ITER_ ;
		dc_mode_flag = 1;
		$vmx_start_sim( `_VMX_SIMULATOR_NAME_ );
		dc_iterations = 0;
		while(dc_mode_flag !=  0)
		begin
			# `_VMX_DC_INTERVAL_ $vmx_do_dc( `_VMX_SIMULATOR_NAME_ , output_change_count);
			dc_iterations = (dc_iterations + 1);
			if( (output_change_count == 0) ||  (dc_iterations >= max_dc_iter) )
			begin
				dc_mode_flag = 0;
				vmx_time_offset = $time;
			end
		end

	end


	wire net3;
	reg mixedNet999997;
	assign net3 = mixedNet999997;
	wire net2;
	reg mixedNet999996;
	assign net2 = mixedNet999996;
	wire net4;
	reg mixedNet999995;
	assign net4 = mixedNet999995;
	wire net9;
	reg mixedNet999994;
	assign net9 = mixedNet999994;
	wire net10;
	reg mixedNet999993;
	assign net10 = mixedNet999993;

	register		I1 (net7, net6, net5, net2, net4, net9, net10, net1, net3, net8);

endmodule

module register (Q2, Q3, Q4, A_0, A_1, A_2, A_3, Ra, C, Q1);

	output	Q2, Q3, Q4;
	input	A_0, A_1, A_2, A_3, Ra, C;
```

```
        output    Q1;


        d_latch         I0 (Q1, net0, Ra, C, A_0);
        d_latch         I1 (Q2, net1, Ra, C, A_1);
        d_latch         I2 (Q3, net2, Ra, C, A_2);
        d_latch         I3 (Q4, net3, Ra, C, A_3);

endmodule

module d_latch (Q, nQ, Ra, C, D);

        output    Q, nQ;
        input     Ra, C, D;


        nand2h          I4 (net4, net3, C);
        nand2h          I3 (net3, D, C);
        nand2           I0 (net4, Q, nQ);

endmodule

module nand2 (in2, in1, out);

        input     in2, in1;
        output    out;



endmodule


module symspice_globals;

        supply1   vdd_, vdda_, vddd_, vcc_, vcca_, vccd_;
        supply0   gnd_, gnda_, gndd_, vss_, vssa_, vssd_, vee_, veea_, veed_;

endmodule
```