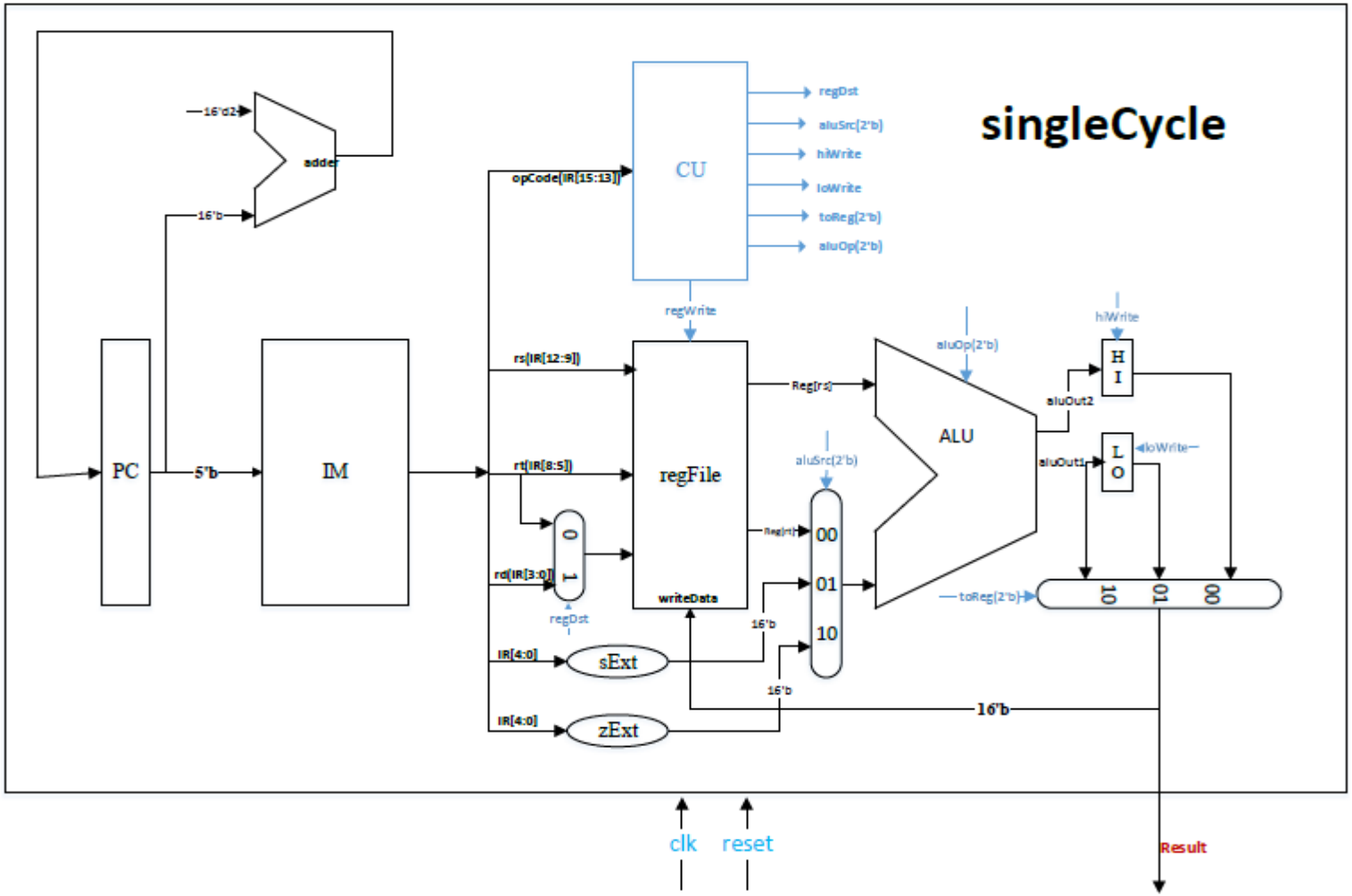
BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
First Semester 2015-2016
CS F342 Computer Architecture
Lab – 3, 8th September 2015

Implement the following using verilog HDL in **Modelsim software** with the following specifications.
Download and modify the singleCycle.v file .



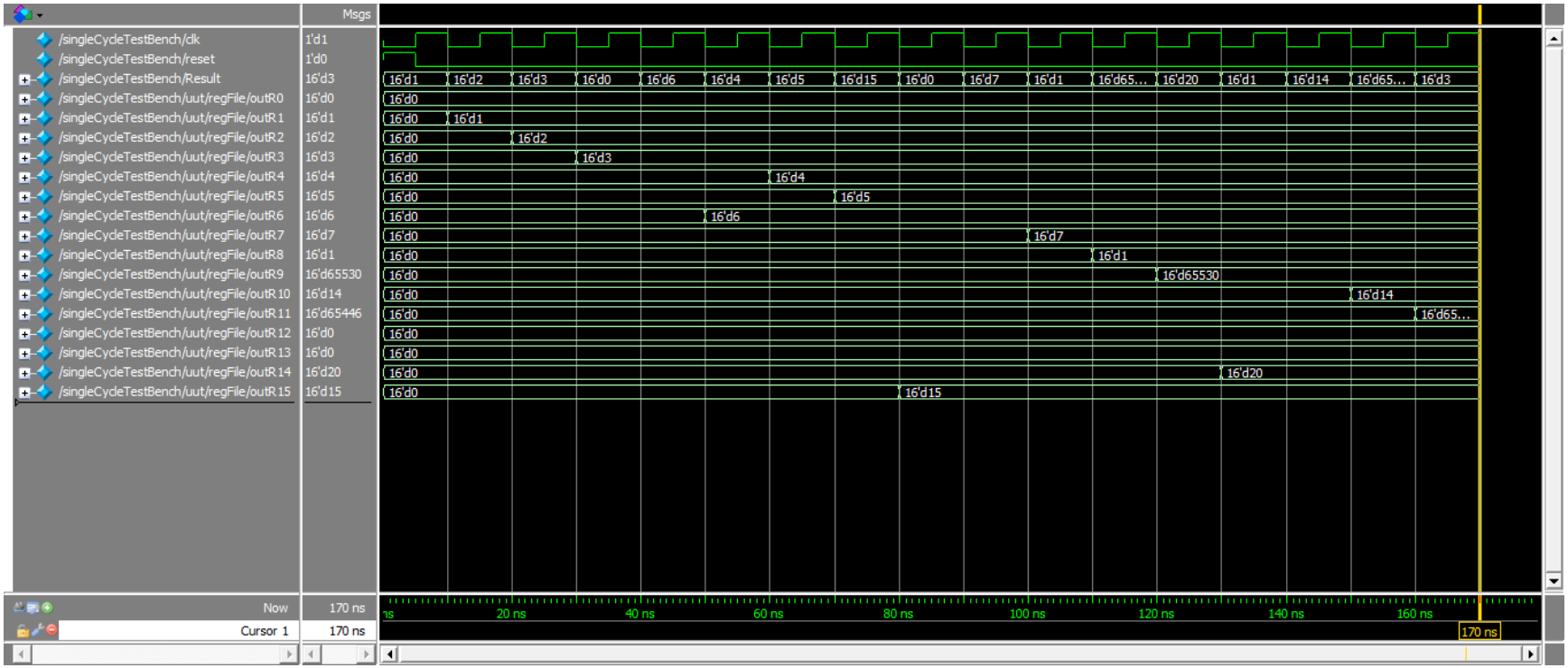
Instruction Format

Instruction	Instruction Format															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
add	0	0	0	Rs				Rt				X	Rd			
or	0	0	1	Rs				Rt				X	Rd			
mul	0	1	0	Rs				Rt				X	Rd			
div	0	1	1	Rs				Rt				X	Rd			
mfhi	1	0	0	X	X	X	X	X	X	X	X	X	Rd			
mflo	1	0	1	X	X	X	X	X	X	X	X	X	Rd			
ori	1	1	0	Rs				Rt				Imm(5bits)				
addi	1	1	1	Rs				Rt				Imm(5bits)				

Control circuit

Instruction	Opcode			Control Circuit						
				regWrite	regDst	aluSrc	aluOp	hiWrite	loWrite	toReg
add	0	0	0	1	1	0	0	0	0	2
or	0	0	1	1	1	0	1	0	0	2
mul	0	1	0	0	X	0	2	1	1	X
div	0	1	1	0	X	0	3	1	1	X
mfhi	1	0	0	1	1	X	X	0	0	0
mflo	1	0	1	1	1	X	X	0	0	1
ori	1	1	0	1	0	2	1	0	0	2
addi	1	1	1	1	0	1	0	0	0	2

WaveForm:


Msgs
/singleCycleTestBench/clk
/singleCycleTestBench/reset
/singleCycleTestBench/Result
/singleCycleTestBench/uut/regFile/outR0
/singleCycleTestBench/uut/regFile/outR1
/singleCycleTestBench/uut/regFile/outR2
/singleCycleTestBench/uut/regFile/outR3
/singleCycleTestBench/uut/regFile/outR4
/singleCycleTestBench/uut/regFile/outR5
/singleCycleTestBench/uut/regFile/outR6
/singleCycleTestBench/uut/regFile/outR7
/singleCycleTestBench/uut/regFile/outR8
/singleCycleTestBench/uut/regFile/outR9
/singleCycleTestBench/uut/regFile/outR10
/singleCycleTestBench/uut/regFile/outR11
/singleCycleTestBench/uut/regFile/outR12
/singleCycleTestBench/uut/regFile/outR13
/singleCycleTestBench/uut/regFile/outR14
/singleCycleTestBench/uut/regFile/outR15
1'd1
1'd0
16'd3
16'd0
16'd1
16'd2
16'd4
16'd5
16'd6
16'd7
16'd65530
16'd14
16'd65446
16'd20
16'd15
Now
170 ns
Cursor 1
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns