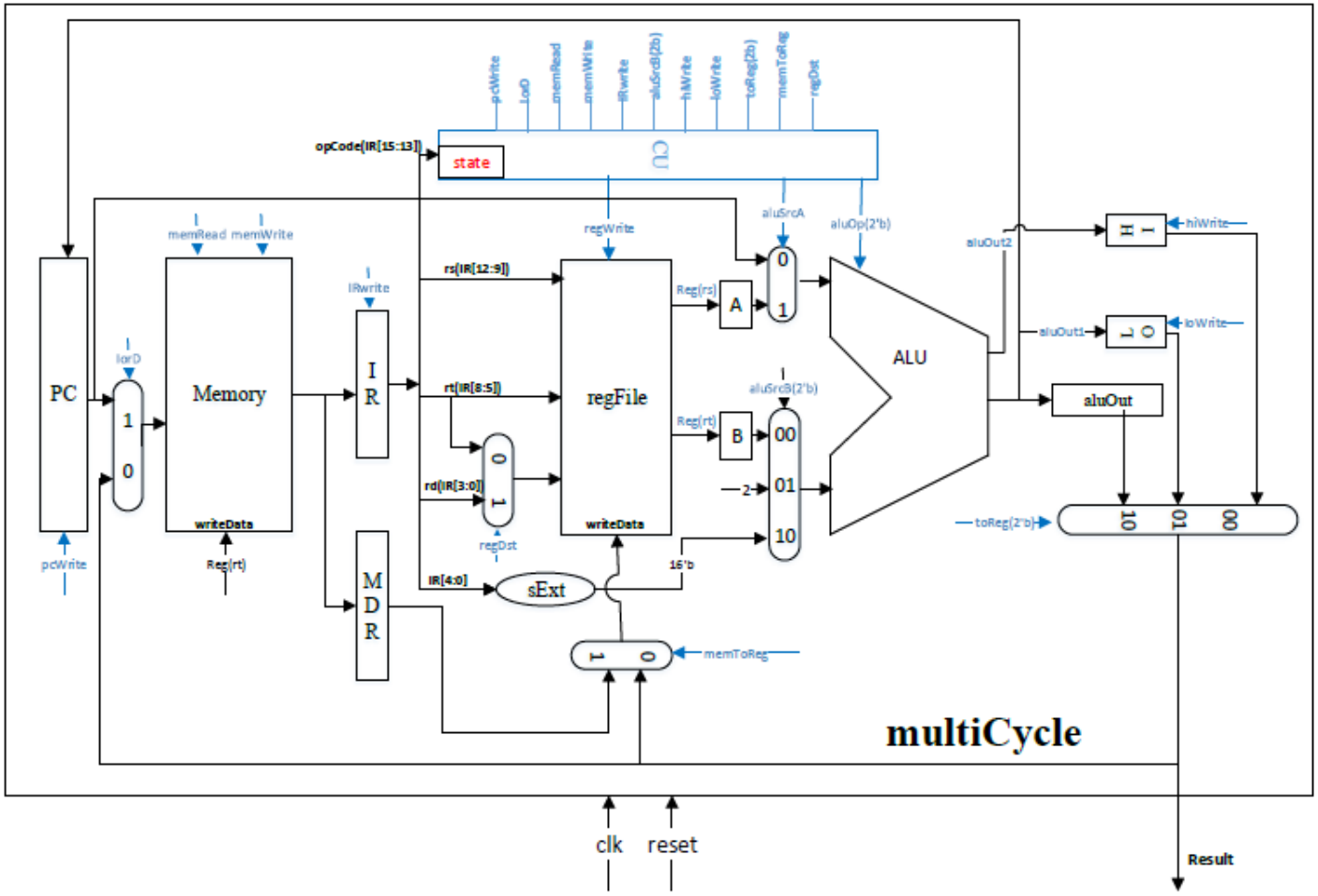
BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
First Semester 2015-2016
CS F342 Computer Architecture
Lab – 4, 6th October 2015

Implement the following using verilog HDL in **Modelsim software** with the following specifications.
Download and modify the multiCycle.v file .

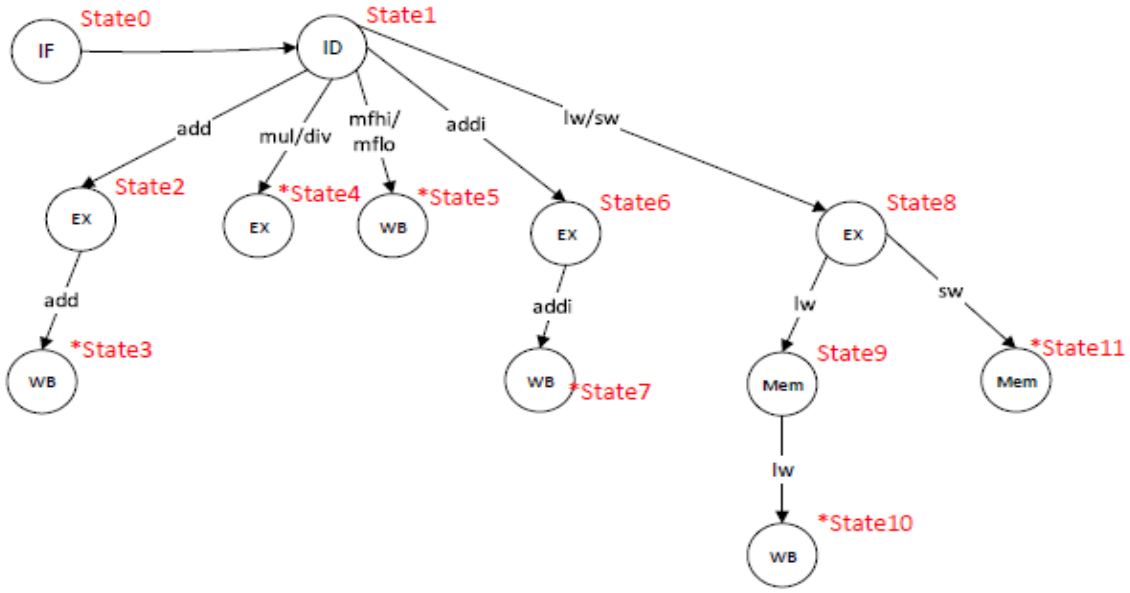


Instruction Format

Instruction	Instruction Format															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
add	0	0	0	Rs				Rt				X	Rd			
mul	0	0	1	Rs				Rt				X	Rd			
div	0	1	0	Rs				Rt				X	Rd			
mfhi	0	1	1	X	X	X	X	X	X	X	X	X	Rd			
mflo	1	0	0	X	X	X	X	X	X	X	X	X	Rd			
addi	1	0	1	Rs				Rt				Imm(5bits)				
lw	1	1	0	Rs				Rt				Imm(5bits)				
sw	1	1	1	Rs				Rt				Imm(5bits)				

Control circuit

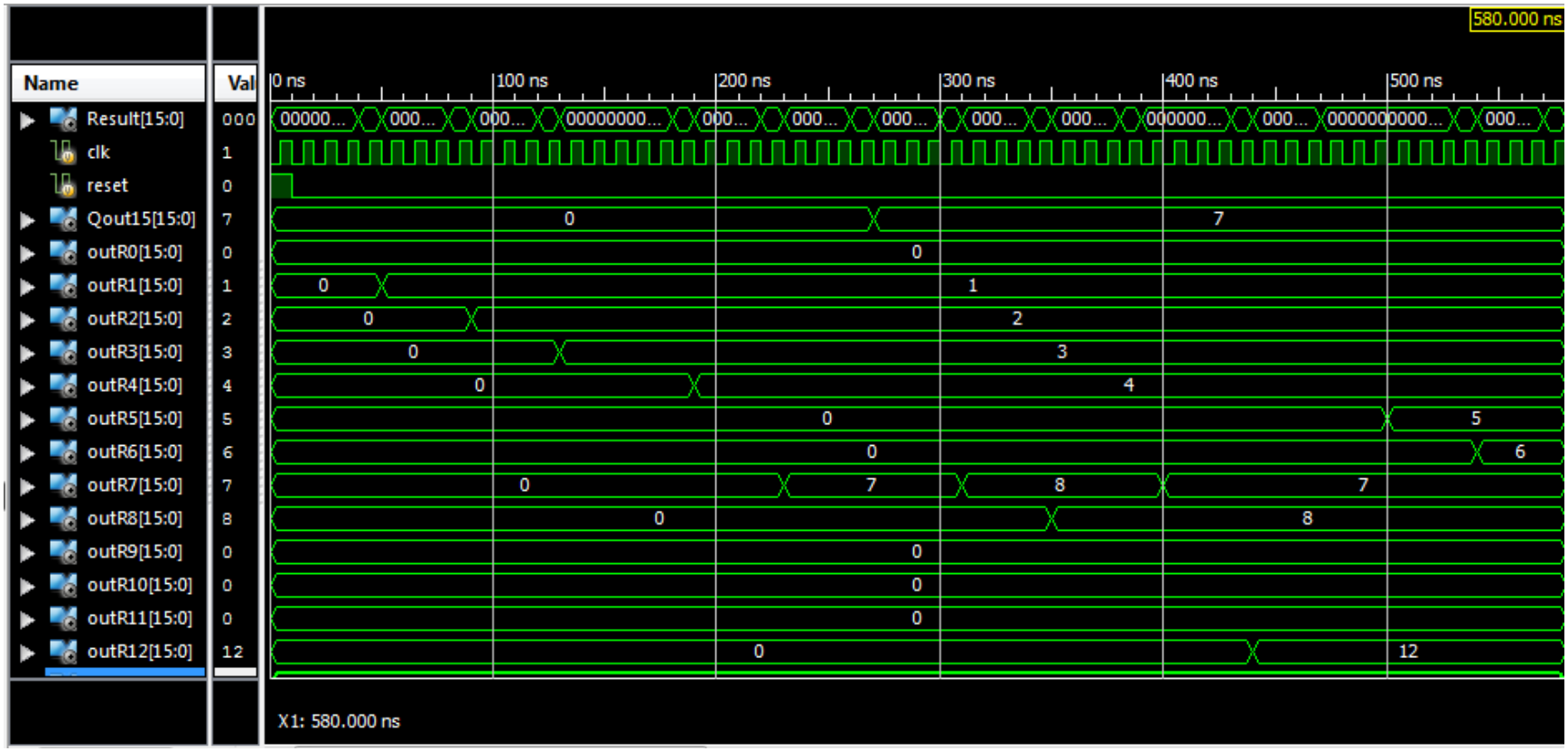
State Diagram:



*State goes back to State0

		pcWrite	IorD	mem Read	mem Write	IR Write	alu SrcA	alu SrcB (2b)	aluOp (2b)	hiWrite	loWrite	toReg (2b)	mem ToReg	regDst	reg Write
State0	IF	1	1	1	0	1	0	1	0	0	0	X	X	X	0
State1	ID	0	X	0	0	0	X	X	X	0	0	X	X	X	0
State2	EX(add)	0	X	0	0	0	1	0	0	0	0	X	X	X	0
State3	WB(add)	0	X	0	0	0	X	X	X	0	0	2	0	1	1
State4	EX(mul/div)	0	X	0	0	0	1	0	1/2(mul /div)	1	1	X	X	X	0
State5	WB(mflo /mfhi)	0	X	0	0	0	X	X	X	0	0	1/0 (mflo/mfhi)	0	1	1
State6	EX(addi)	0	X	0	0	0	1	2	0	0	0	X	X	X	0
State7	WB(addi)	0	0	0	0	0	X	X	X	0	0	2	0	0	1
State8	EX(lw/sw)	0	X	0	0	0	1	2	0	0	0	X	X	X	0
State9	Mem(lw)	0	0	1	0	0	X	X	X	0	0	2	X	X	0
State10	WB(lw)	0	X	0	0	0	X	X	X	0	0	X	1	0	1
State11	Mem(sw)	0	0	0	1	0	X	X	X	0	0	2	X	X	0
***Consider all don't care(X) values as 0**															

WaveForm:



***Content of Register File and memory location 15 is shown in waveform**