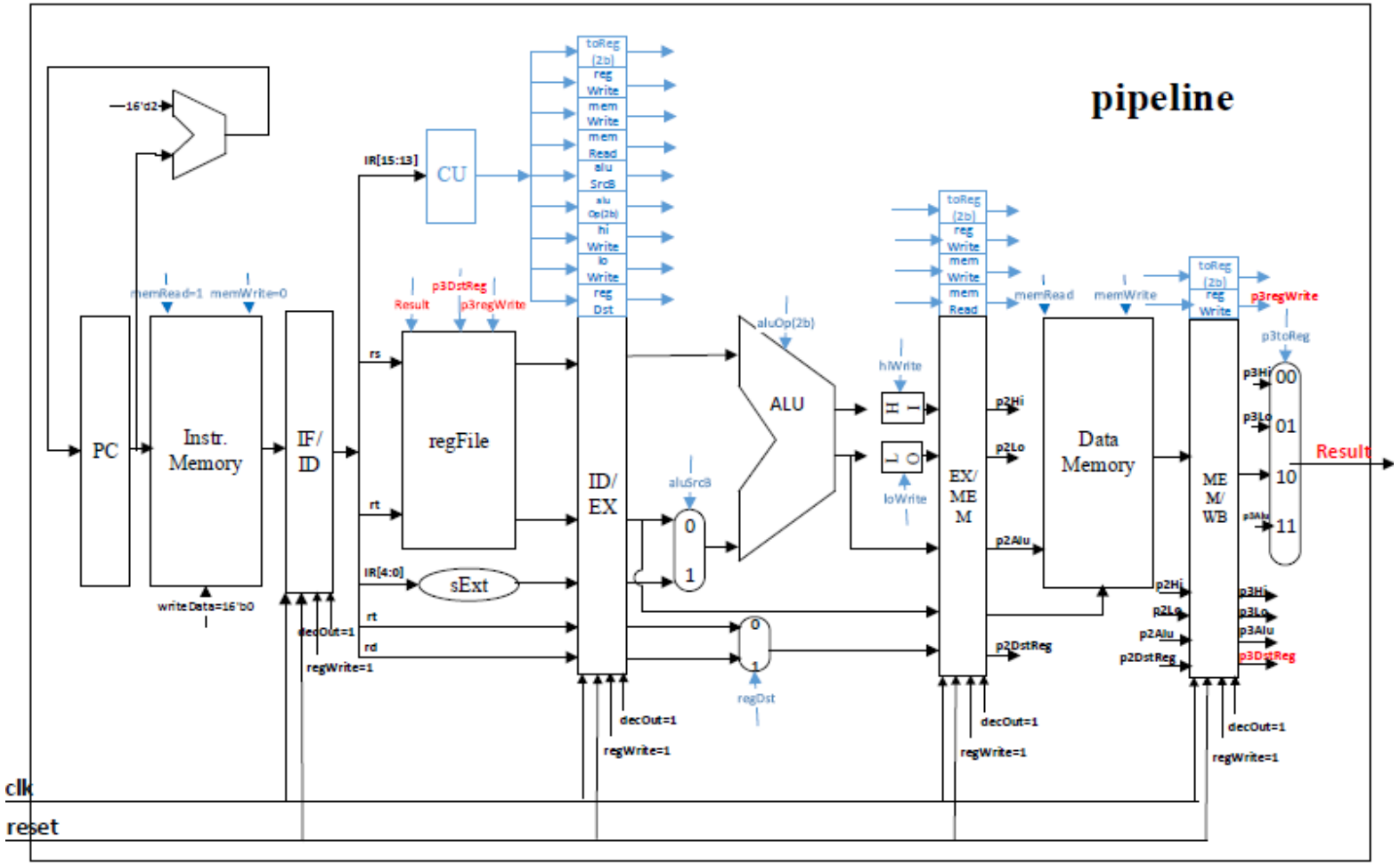
BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
First Semester 2015-2016
CS F342 Computer Architecture
Lab – 5, 20th October 2015

Implement the following using verilog HDL in **Modelsim software** with the following specifications.
Download and modify the pipeline.v file .



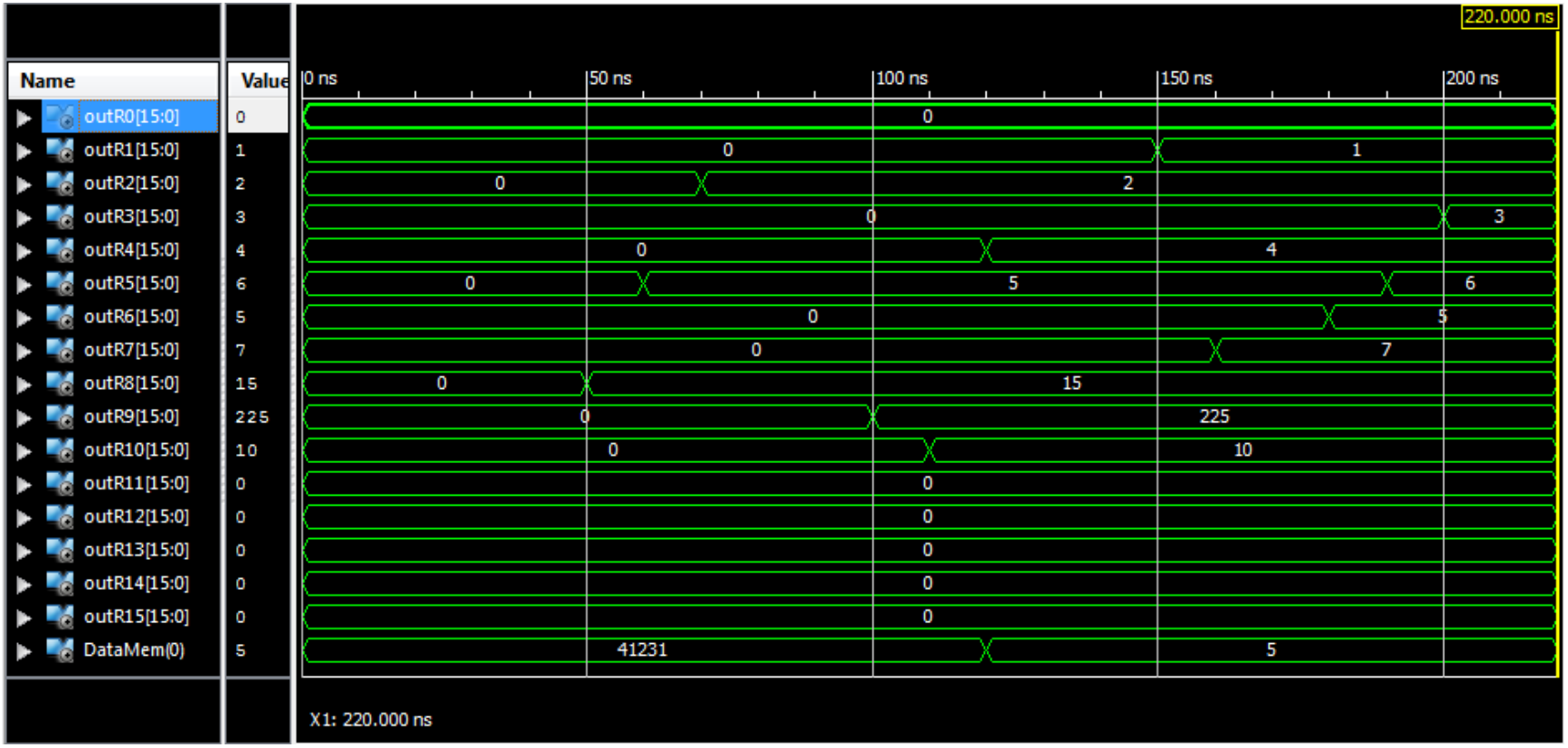
Instruction Format

Instruction	Instruction Format															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
add	0	0	0	Rs				Rt				X	Rd			
mul	0	0	1	Rs				Rt				X	Rd			
div	0	1	0	Rs				Rt				X	Rd			
mfhi	0	1	1	X	X	X	X	X	X	X	X	X	Rd			
mflo	1	0	0	X	X	X	X	X	X	X	X	X	Rd			
addi	1	0	1	Rs				Rt				Imm(5bits)				
lw	1	1	0	Rs				Rt				Imm(5bits)				
sw	1	1	1	Rs				Rt				Imm(5bits)				

Control circuit

Instruction	opCode			Control Signals								
				aluSrcB	aluOp(2b)	regDst	hiWrite	loWrite	memRead	memWrite	regWrite	toReg(2b)
add	0	0	0	0	0	1	0	0	0	0	1	3
mul	0	0	1	0	1	0	1	1	0	0	0	0
div	0	1	0	0	2	0	1	1	0	0	0	0
mfhi	0	1	1	0	0	1	0	0	0	0	1	0
mflo	1	0	0	0	0	1	0	0	0	0	1	1
addi	1	0	1	1	0	0	0	0	0	0	1	3
lw	1	1	0	1	0	0	0	0	1	0	1	2
sw	1	1	1	1	0	0	0	0	0	1	0	0

WaveForm:



*Waveform shows contents of register file and data memory location 0.