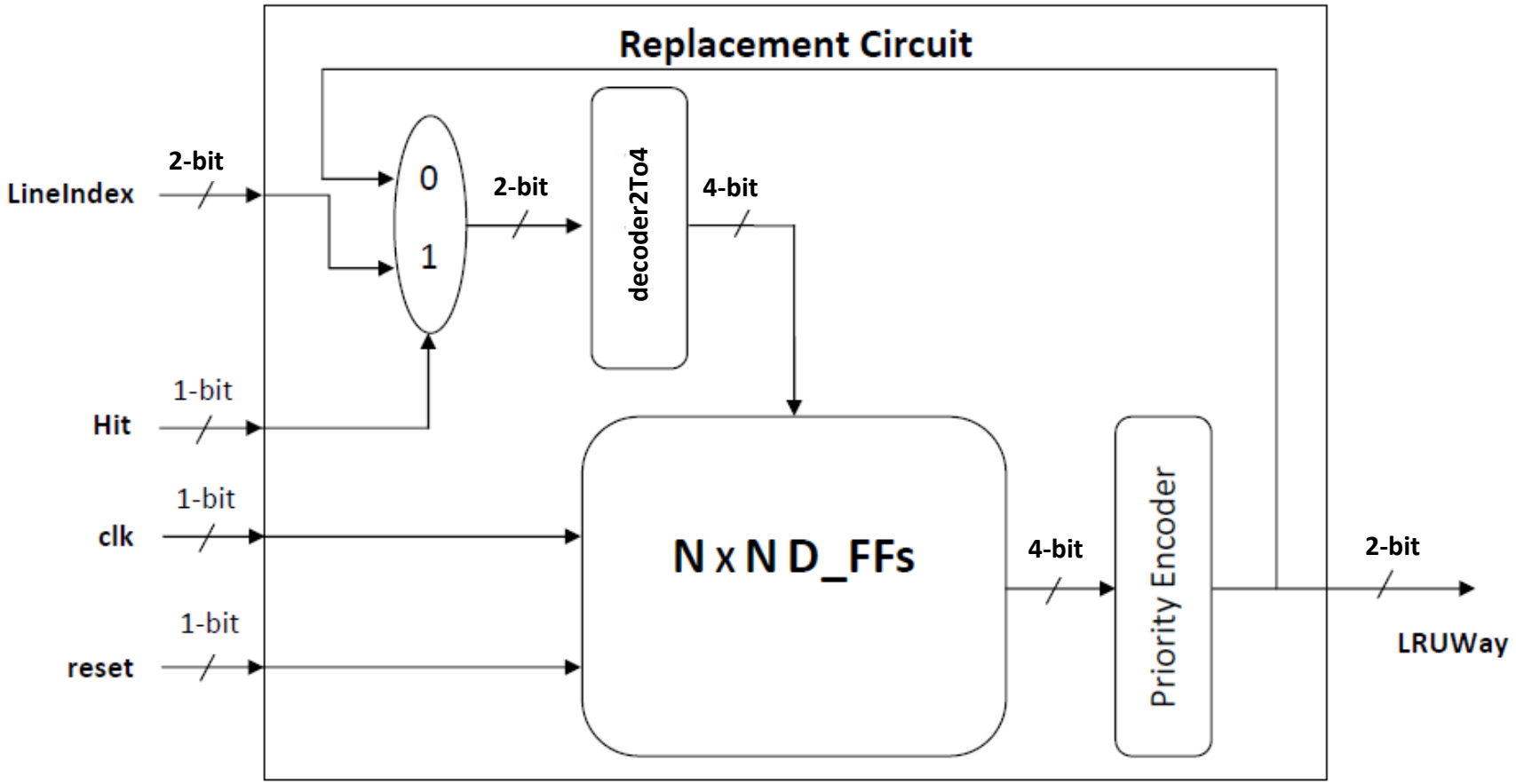
BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
First Semester 2015-2016
CS F342 Computer Architecture
Lab – 6, 3rd November 2015

Implement the following using verilog HDL in **ModelSim software** with the following specifications.



Modules

1. module D_FF(input clk,input set,input reset,output reg Q);

```
        always@(negedge clk)
        begin
                if(reset==1'b1)
                        Q=0;
                else
                begin
                        if(set)
                                Q=1;
                end
        end
```

endmodule

2. module decoder2to4(input [1:0] muxOut,output reg[3:0] decOut);

3. module mux(input [1:0] LineIndex,input[1:0] LRUWay,input Hit,output reg [1:0] muxOut);

4. module NxN_DFFs(input clk,input reset,input[3:0] decOut,output [3:0] NxNOut);

5. module prio_Enc(input reset, input [3:0]NxNOut,output reg [1:0] LRUWay);

6. module LRU(input [1:0] LineIndex,input clk,input reset, input Hit , output [1:0] LRUWay, output [1:0] mOut, output [3:0] dOut, output [3:0] nOut);

7. module testbench;

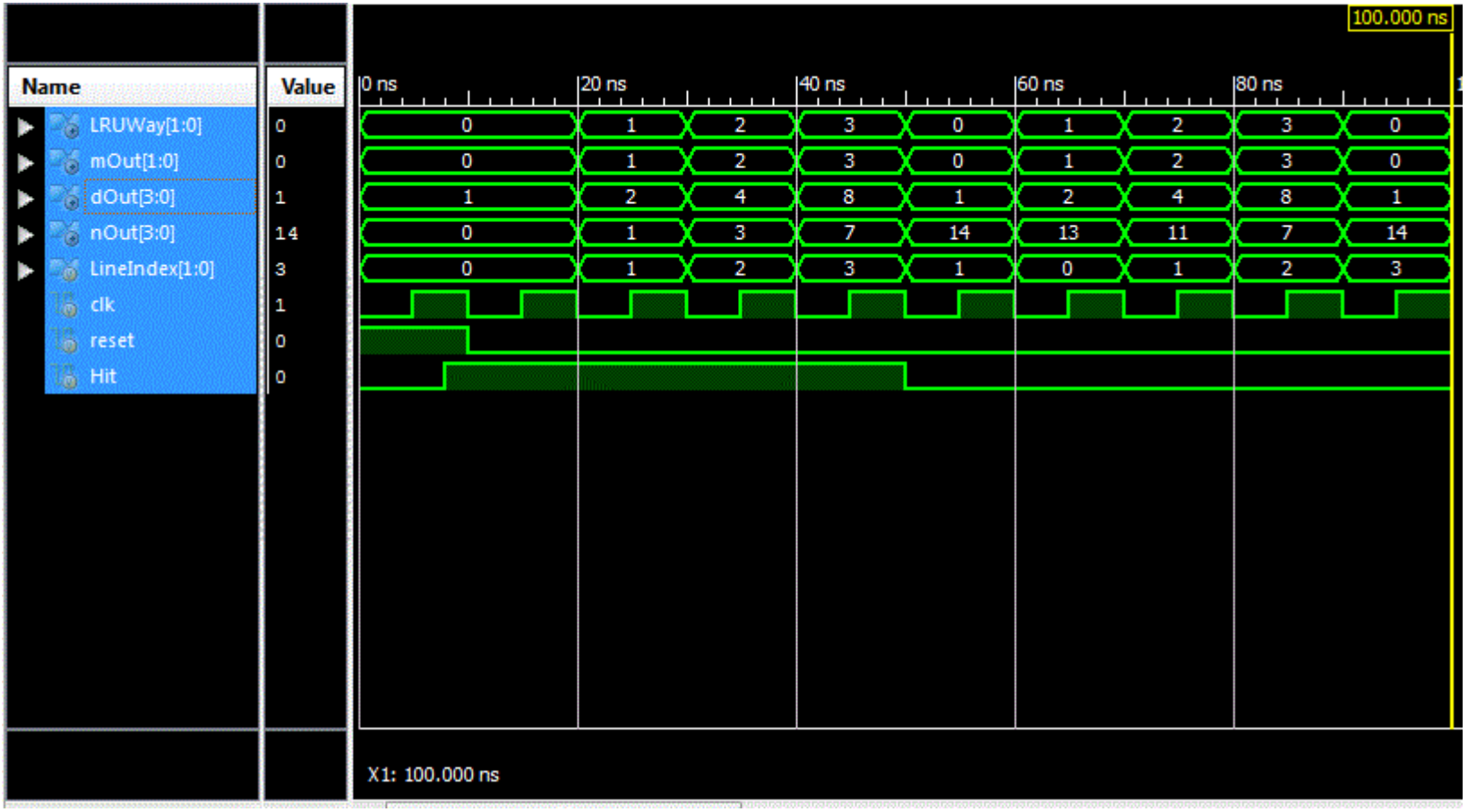
```
        reg [1:0] LineIndex;
        reg clk;
        reg reset;
        reg Hit;
        wire [1:0] LRUWay;
        wire [1:0] mOut;
        wire [3:0] dOut, nOut;

        LRU uut (.LineIndex(LineIndex), .clk(clk), .reset(reset), .Hit(Hit), .LRUWay(LRUWay), .mOut(mOut), .dOut(dOut),
.nOut(nOut) );
        always
                #5 clk=~clk;
        initial
```

```
        begin
                LineIndex = 0;
                reset = 1;
                Hit = 0;
                clk = 0;
$monitor($time," Current_LRUWay=%d      Hit=%d LineIndex=%d  ",LRUWay,Hit,LineIndex);
                #8 Hit=1;
                #2 reset=0; LineIndex=3'd0;
                #10 LineIndex=3'd1;
                #10 LineIndex=3'd2;
                #10 LineIndex=3'd3;

                #10 Hit=0; LineIndex=3'd1;
                #10 LineIndex=3'd0;
                #10 LineIndex=3'd1;
                #10 LineIndex=3'd2;
                #10 LineIndex=3'd3;
                #10 $finish;
        end
endmodule
```

WaveForm:


100.000 ns
Name
Value
0 ns
20 ns
40 ns
60 ns
80 ns
LRUWay[1:0]
0
0 1 2 3 0 1 2 3 0
mOut[1:0]
0
0 1 2 3 0 1 2 3 0
dOut[3:0]
1
1 2 4 8 1 2 4 8 1
nOut[3:0]
14
0 1 3 7 14 13 11 7 14
LineIndex[1:0]
3
0 1 2 3 1 0 1 2 3
clk
1
reset
0
Hit
0
X1: 100.000 ns