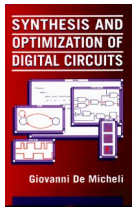
Design Technologies for Integrated Systems

Giovanni De Micheli

Integrated Systems Centre

EPF Lausanne



Module 1

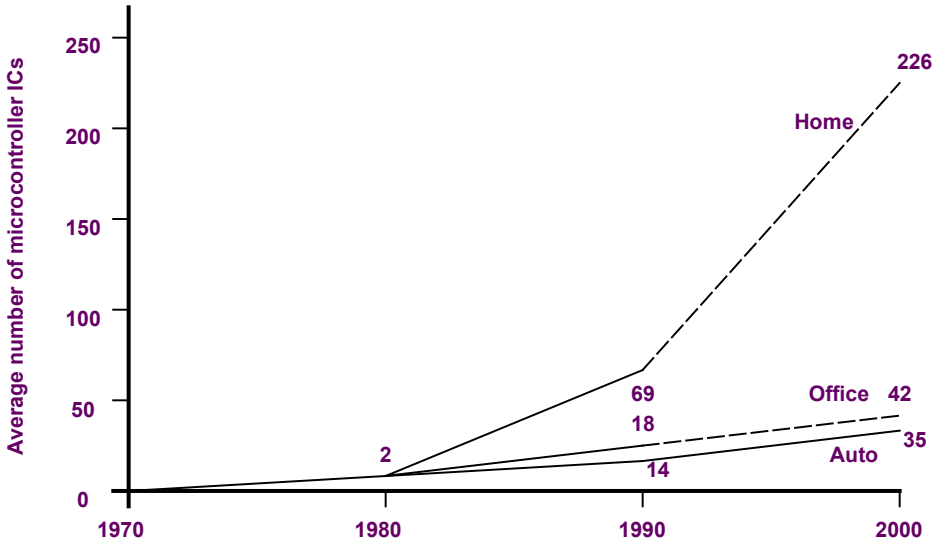
- Objective
  - Electronic systems and their requirements
  - Integrated circuits
  - Design styles

Electronic systems

- Systems on chip are everywhere

- Technology advances enable increasingly more complex designs
- Challenges:
  - Ride the technology wave
  - Cope with design complexity

Application of microcontrollers



Home

- Appliances
- Intercom
- Telephones
- Security system
- Garage door opener
- Answering machines
- Fax machines
- Home computers
- TVs
- Cable TV tuner
- VCR
- Camcorder
- Remote controls
- Video games
- Cellular phones
- Musical instruments
- Sewing machines
- Lighting control
- Paging
- Cameras
- Exercise equipment
- Microwave oven

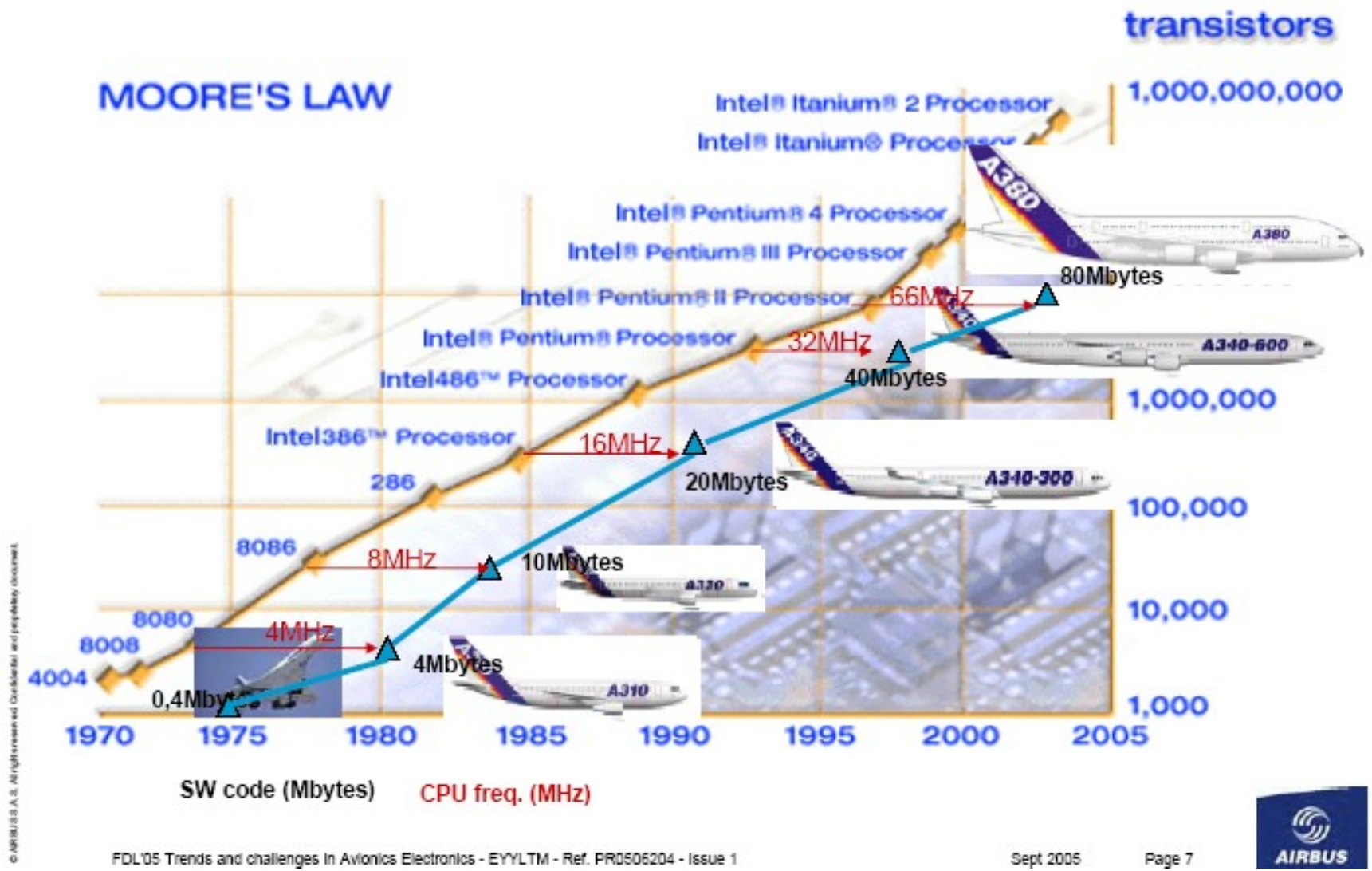
Office

- Telephones
- Computers
- Security system
- Fax machines
- Copier
- Printers
- Remote control
- Pagers

Automobile

- Drive by wire
- Trop computer
- Air bags
- ABS
- Instrumentation
- Security system
- Transmission control
- Enterainment
- Climate control
- Keyless entry
- Cellular phone
- GPS

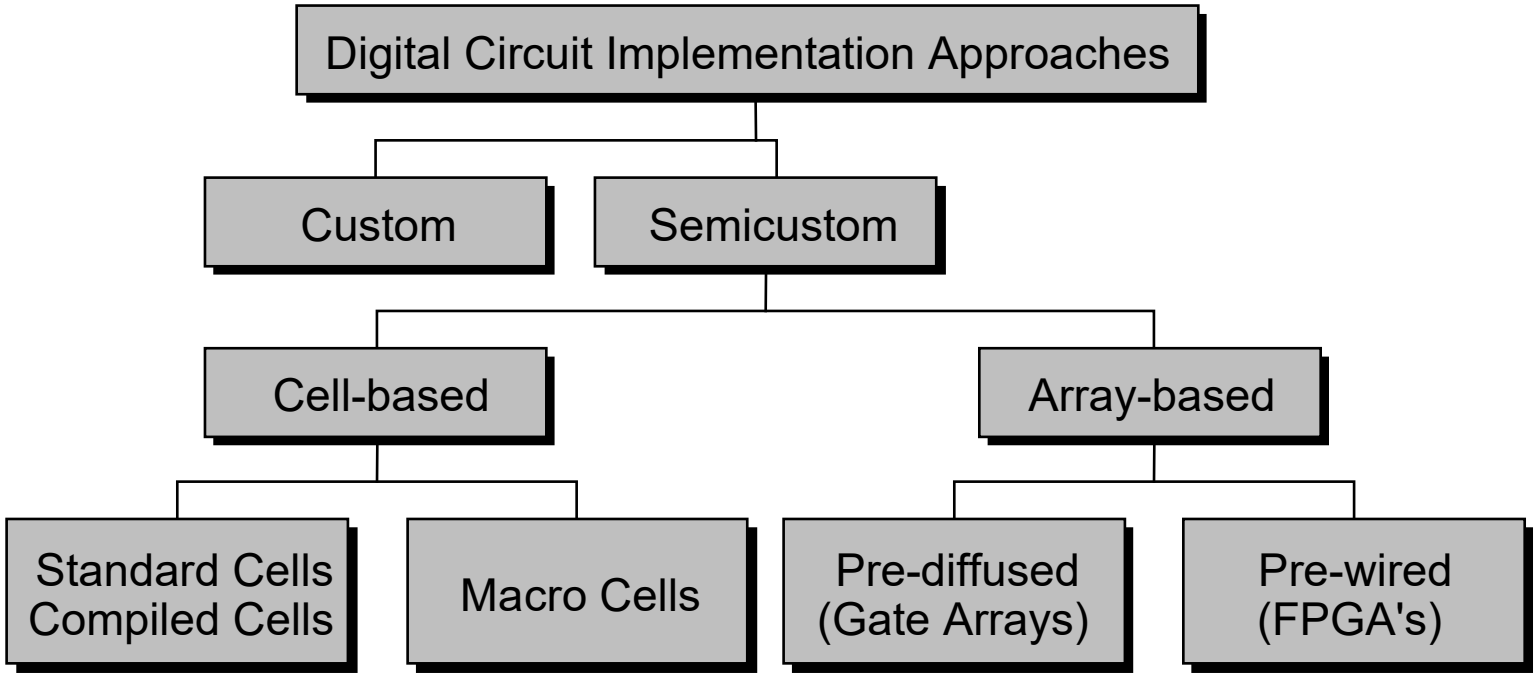
Moore’s law in avionics



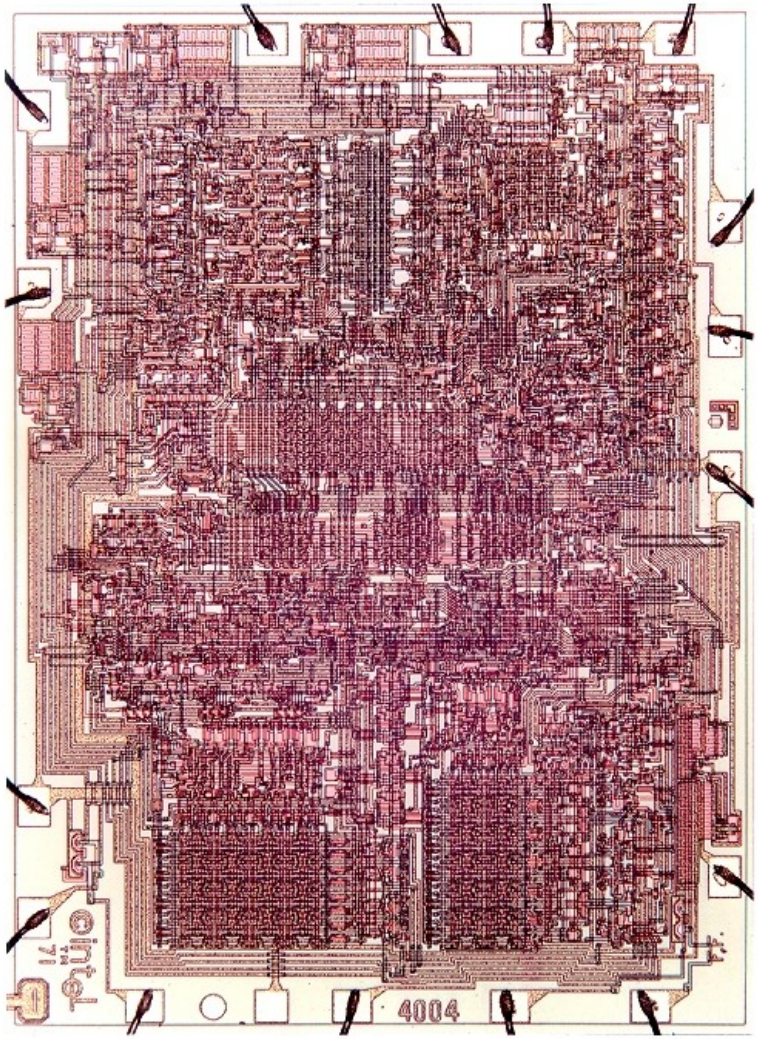
Integrated circuits

- Systems on Chip (SoC)
  - Multi-processing SoCs (MPSoCs)
- Systems in a package (SiP)
- Silicon technology (CMOS)
  - Down scaling of feature sizes
  - Nanotechnologies on the horizon …
- Different design styles
  - To address performance and cost issues

Integrated Circuit Design Styles



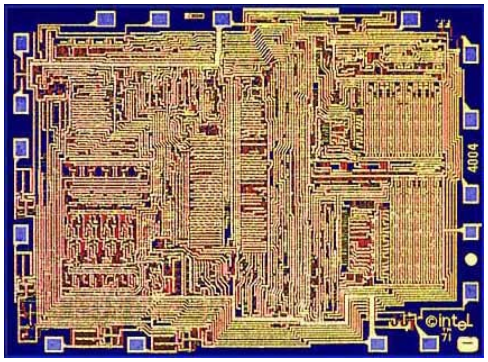
The Custom Approach



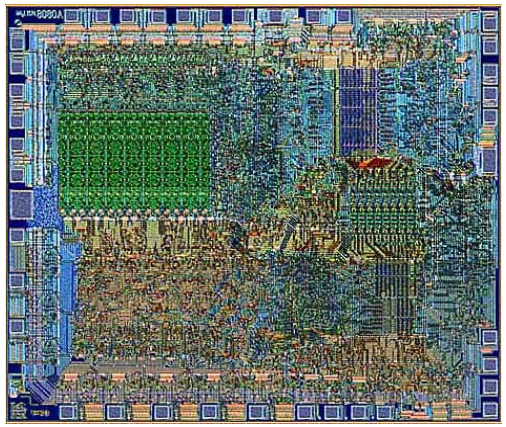
Intel 4004

Courtesy Intel

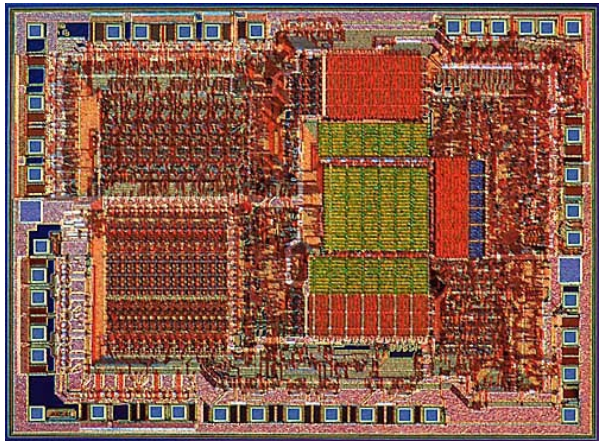
Transition to Automation and Regular Structures



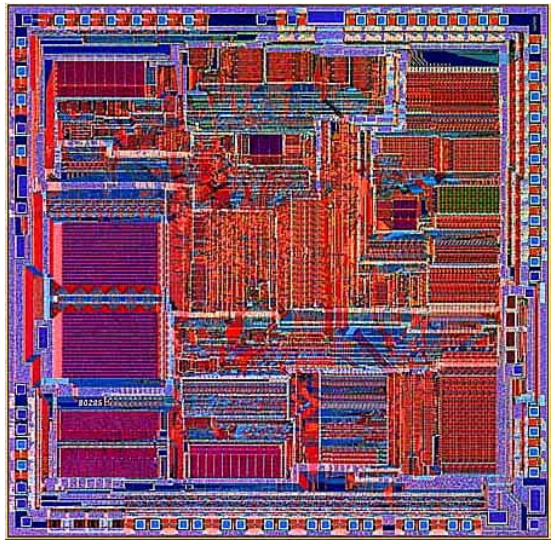
Intel 4004 (‘71)



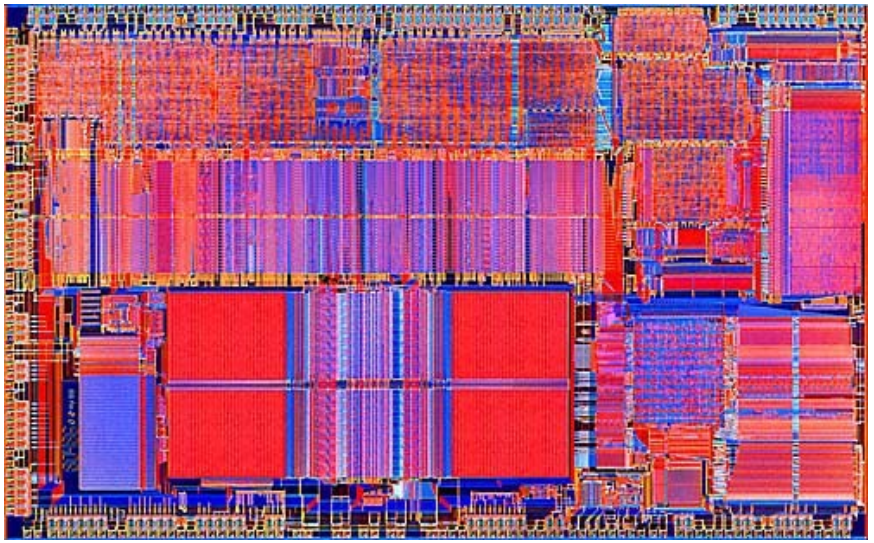
Intel 8080



Intel 8085



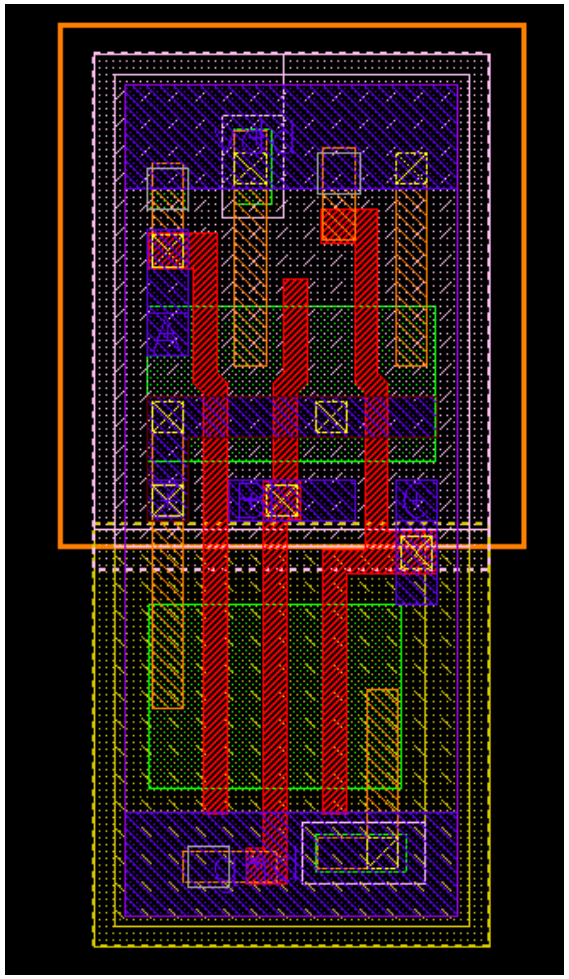
Intel 8286



Intel 8486

Courtesy Intel

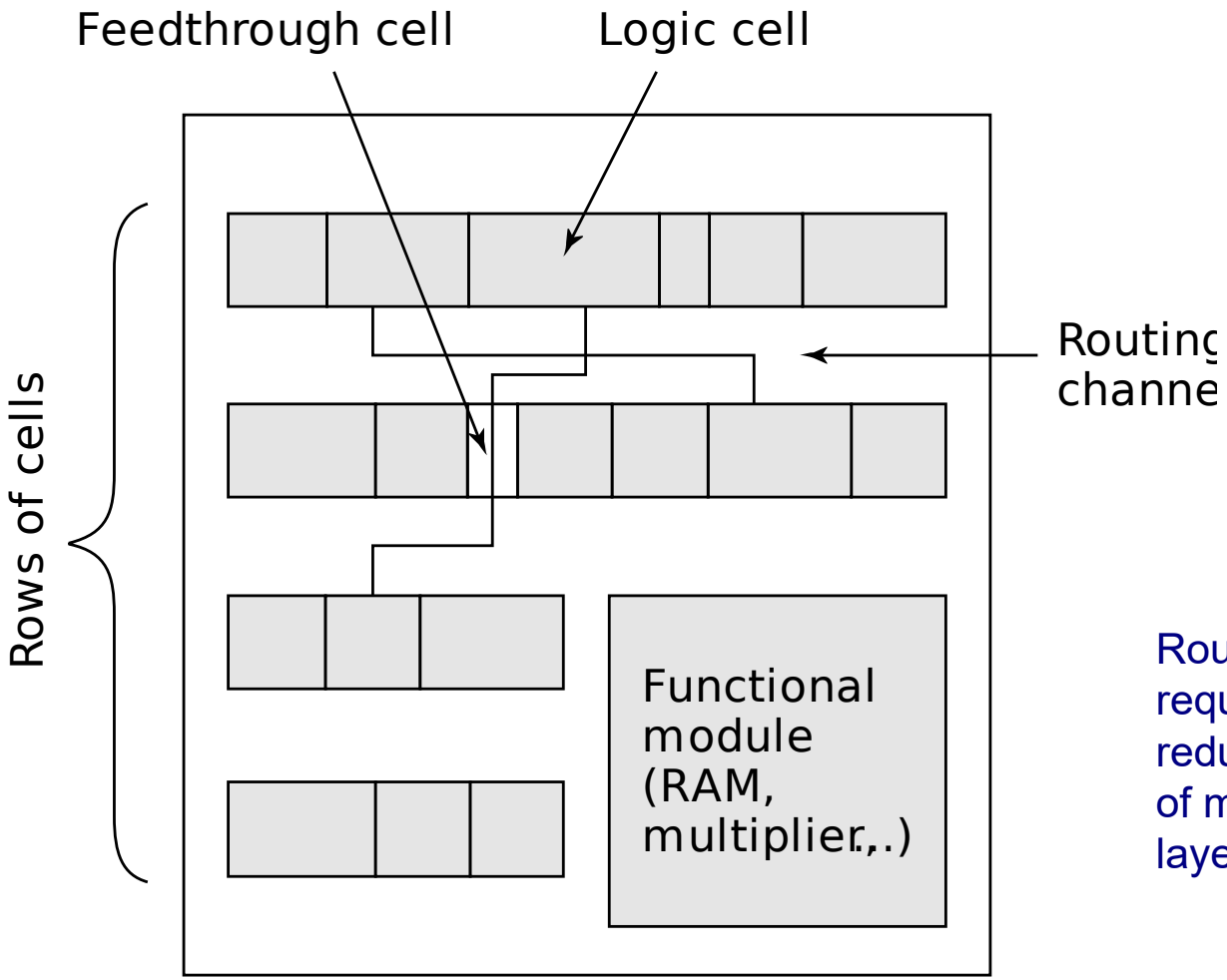
Standard Cell - Example



Path	1.2V - 125°C	1.6V - 40°C
$In1—t_{pLH}$	$0.073+7.98C+0.317T$	$0.020+2.73C+0.253T$
$In1—t_{pHL}$	$0.069+8.43C+0.364T$	$0.018+2.14C+0.292T$
$In2—t_{pLH}$	$0.101+7.97C+0.318T$	$0.026+2.38C+0.255T$
$In2—t_{pHL}$	$0.097+8.42C+0.325T$	$0.023+2.14C+0.269T$
$In3—t_{pLH}$	$0.120+8.00C+0.318T$	$0.031+2.37C+0.258T$
$In3—t_{pHL}$	$0.110+8.41C+0.280T$	$0.027+2.15C+0.223T$

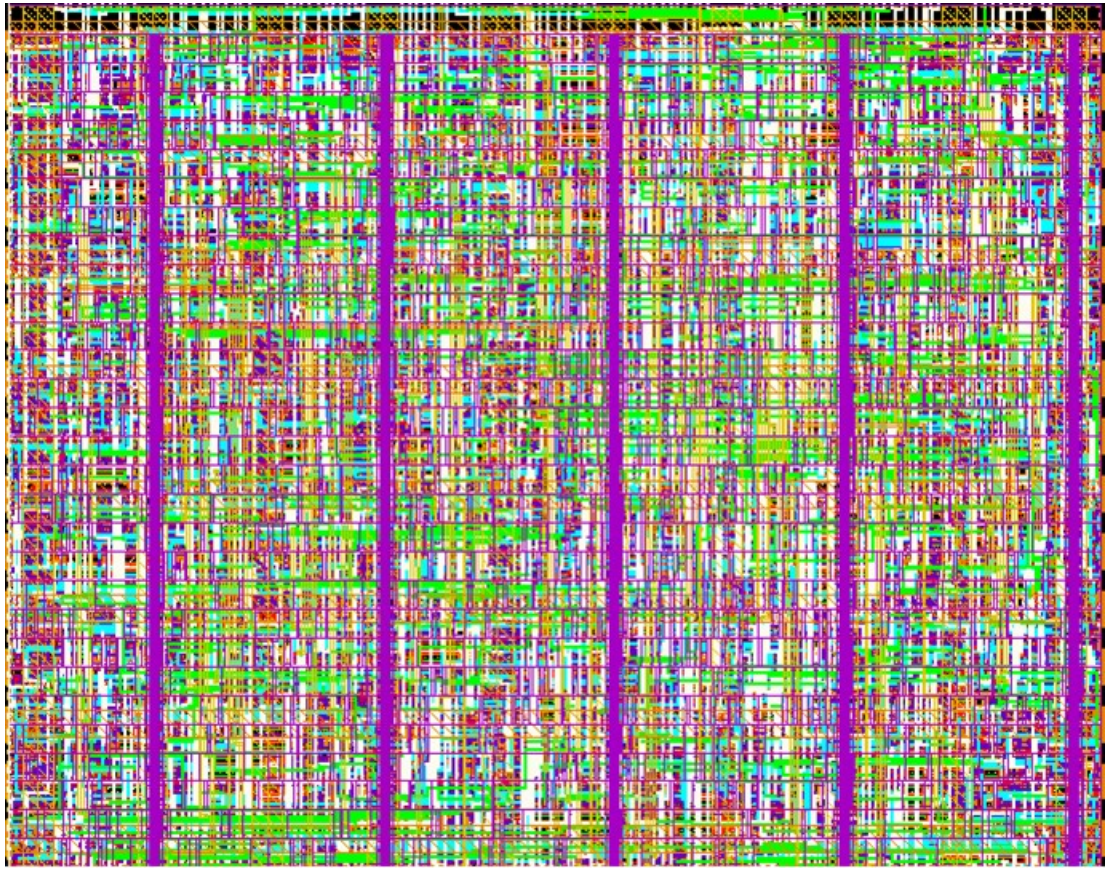
3-input NAND cell
(from ST Microelectronics):
C = Load capacitance
T = input rise/fall time

Cell-based Design (or standard cells)



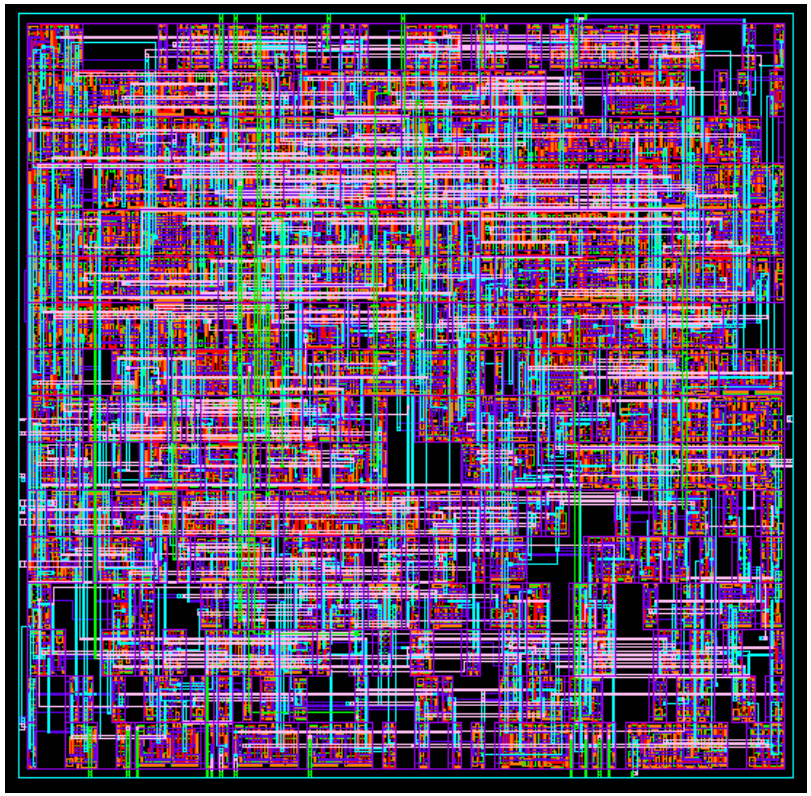
Routing channel requirements are reduced by presence of more interconnect layers

Standard Cell – The New Generation

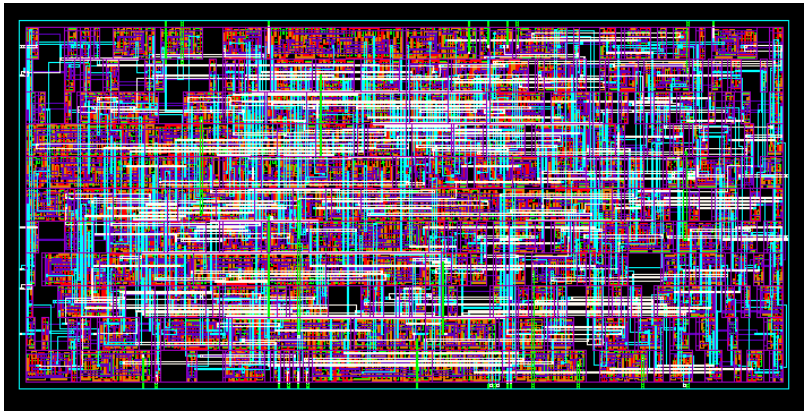


Cell-structure hidden under interconnect layers

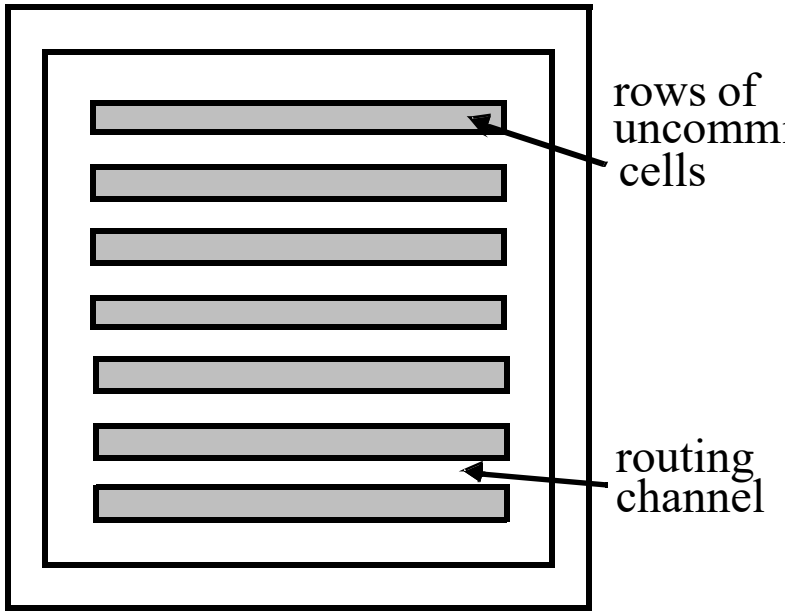
“Soft” MacroModules

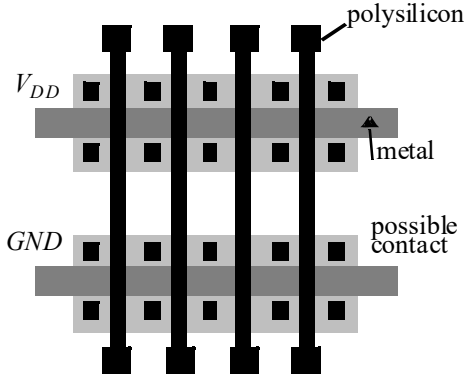


```
string mat = “booth”;
directive (multtype = mat);
output signed [16] Z = A * B;
```

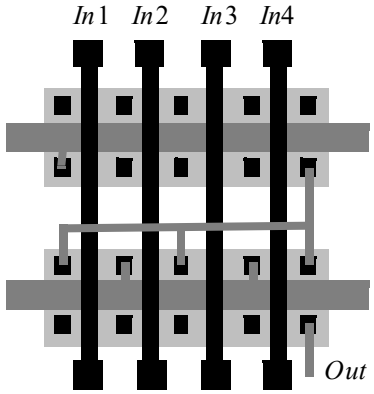


Gate Array — Sea-of-gates



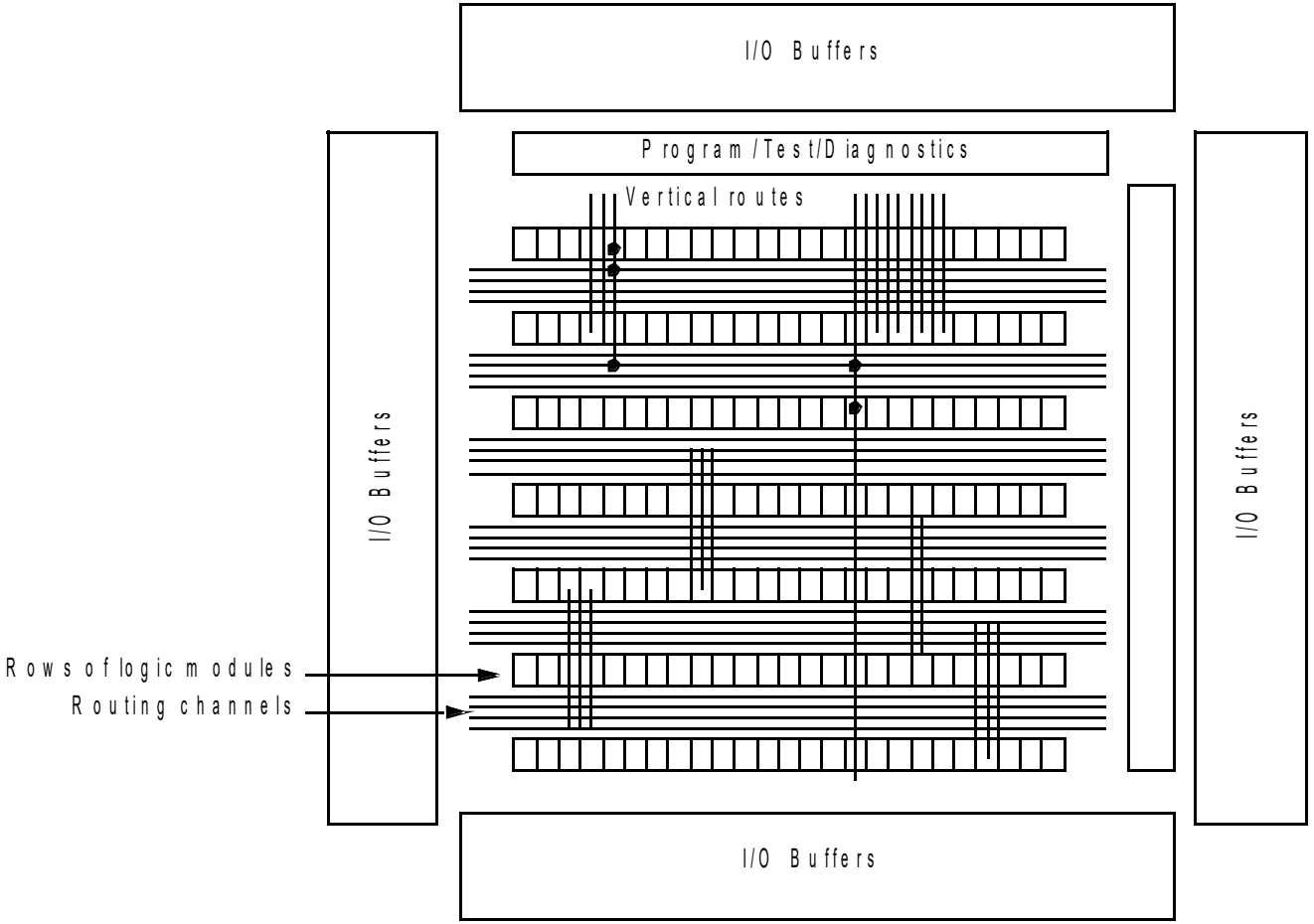


Uncommited Cell



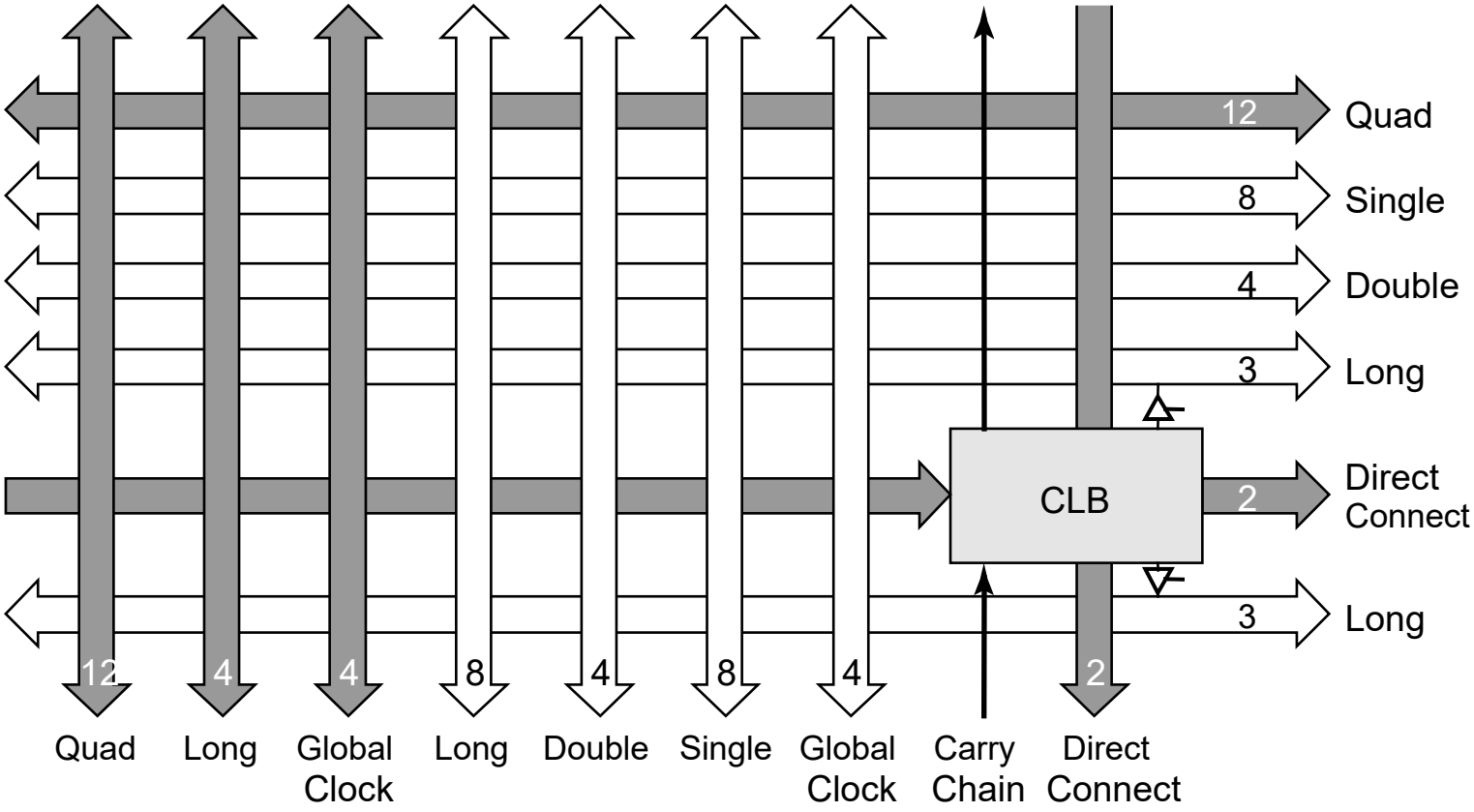
Committed Cell (4-input NOR)

Field-Programmable Gate Arrays
Fuse-based



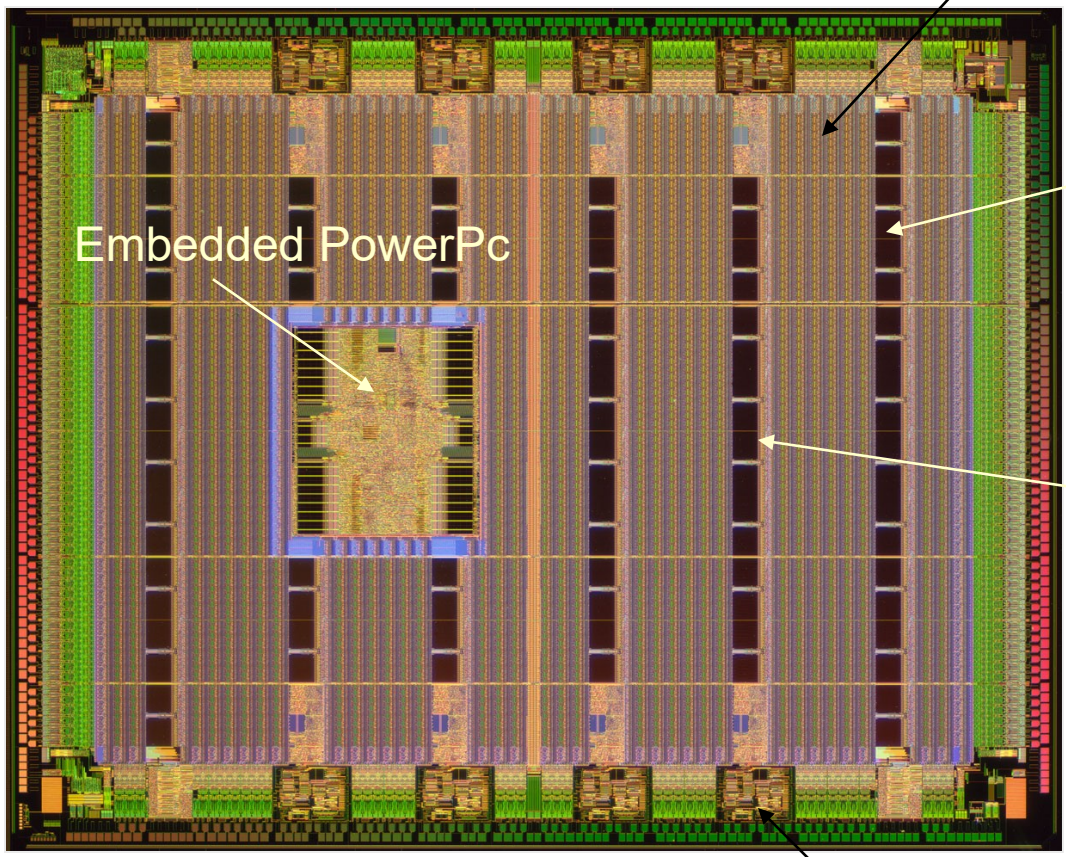
Standard-cell like floorplan

Field Programmable Gate Arrays
Xilinx 4000 Interconnect Architecture



Courtesy Xilinx

Heterogeneous Programmable Platforms



Xilinx Vertex-II Pro

Courtesy Xilinx

Module 2

- Objective
  - Electronic design automation
  - Synthesis and optimization
  - Multi-criteria optimization

Computer-aided design

- **Enabling design methodology**
  - **Support large scale system design**
  - **Design optimization, centering and trade-off**
  - **Reduce design time and time to market**
- **…** ***the only purpose of science is to ease the hardship of human existence*** **… [Galileo/Brecht]**

Microelectronic circuit design

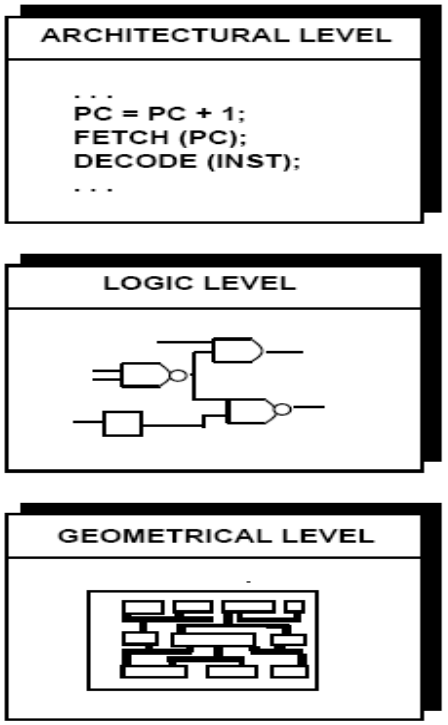
- Conceptualization and modeling
  - Hardware description languages
- Synthesis and optimization
  - Model refinement
- Validation
  - Check for correctness

Synthesis history

- Few logic synthesis algorithms and tools existed in the 70's
- Link to place and route for automatic design
  - Innovative methods at IBM, Bell Labs, Berkeley, Stanford
- First prototype synthesis tools in the early 80s
  - YLE [Brayton], MIS [Berkeley], Espresso
- First logic synthesis companies in the late 80's
  - Synopsys and others

Modeling abstractions

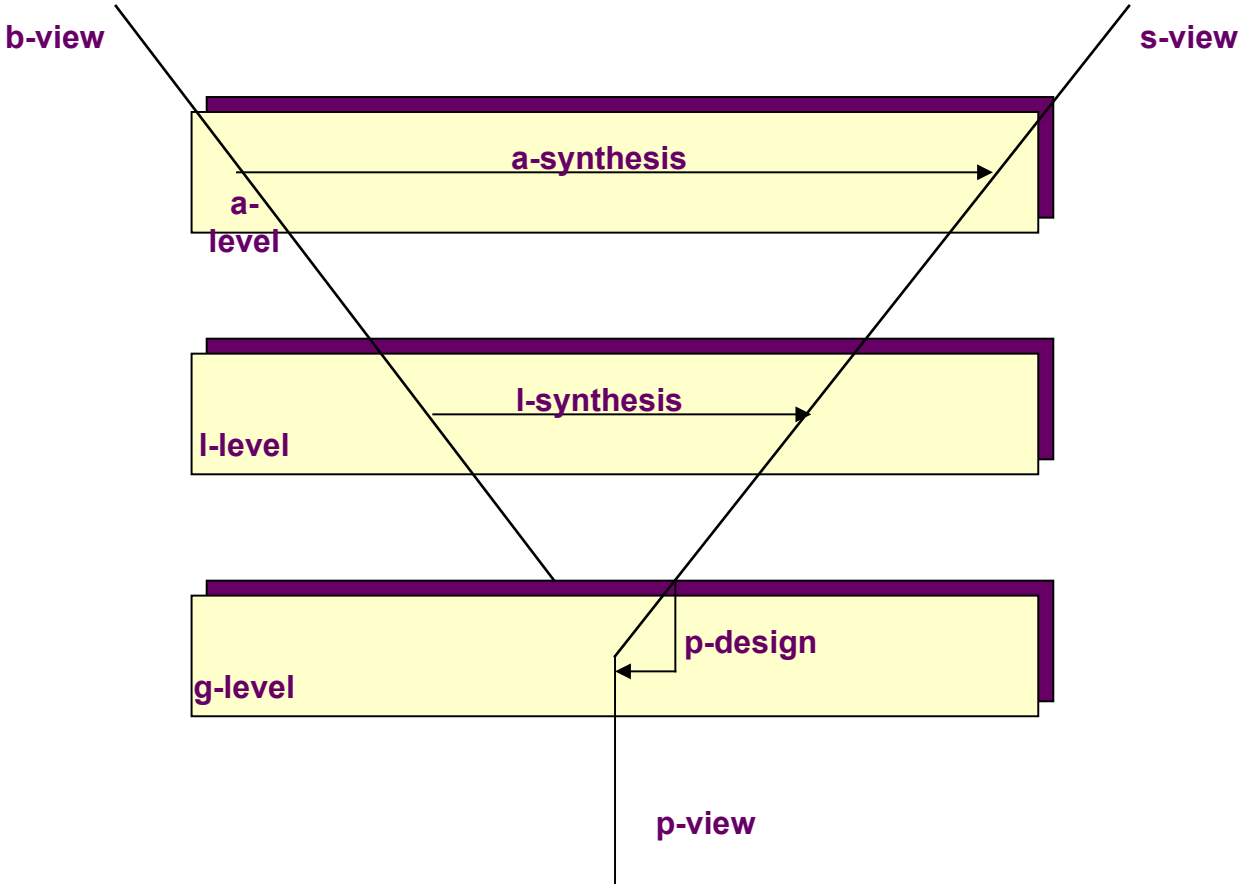
- Architectural level
  - Operations implemented by resources
- Logic level
  - Logic functions implemented by gates
- Geometrical level
  - Transistors and wires



Circuit synthesis

- Architectural-level synthesis
  - Determine macroscopic structure
    - Interconnection of major building blocks
- Logic-level synthesis
  - Determine the microscopic structure
    - Interconnection of logic gates
- Physical design
  - Geometrical-level synthesis
  - Determine positions and connections

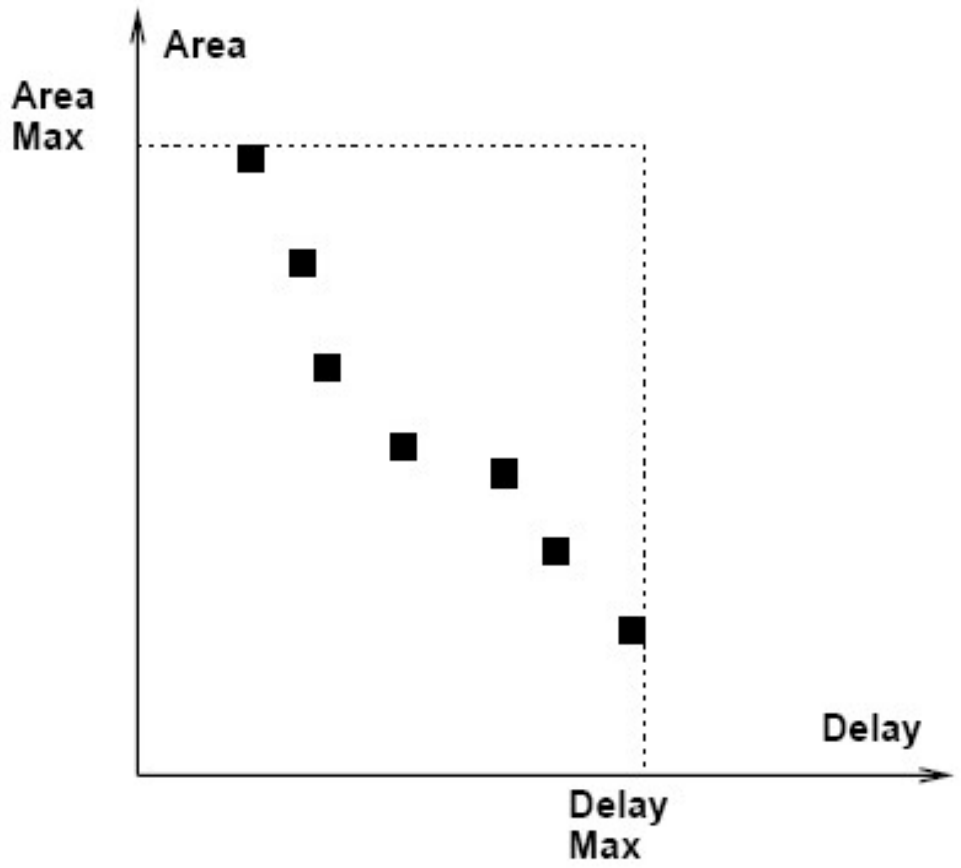
Synthesis levels



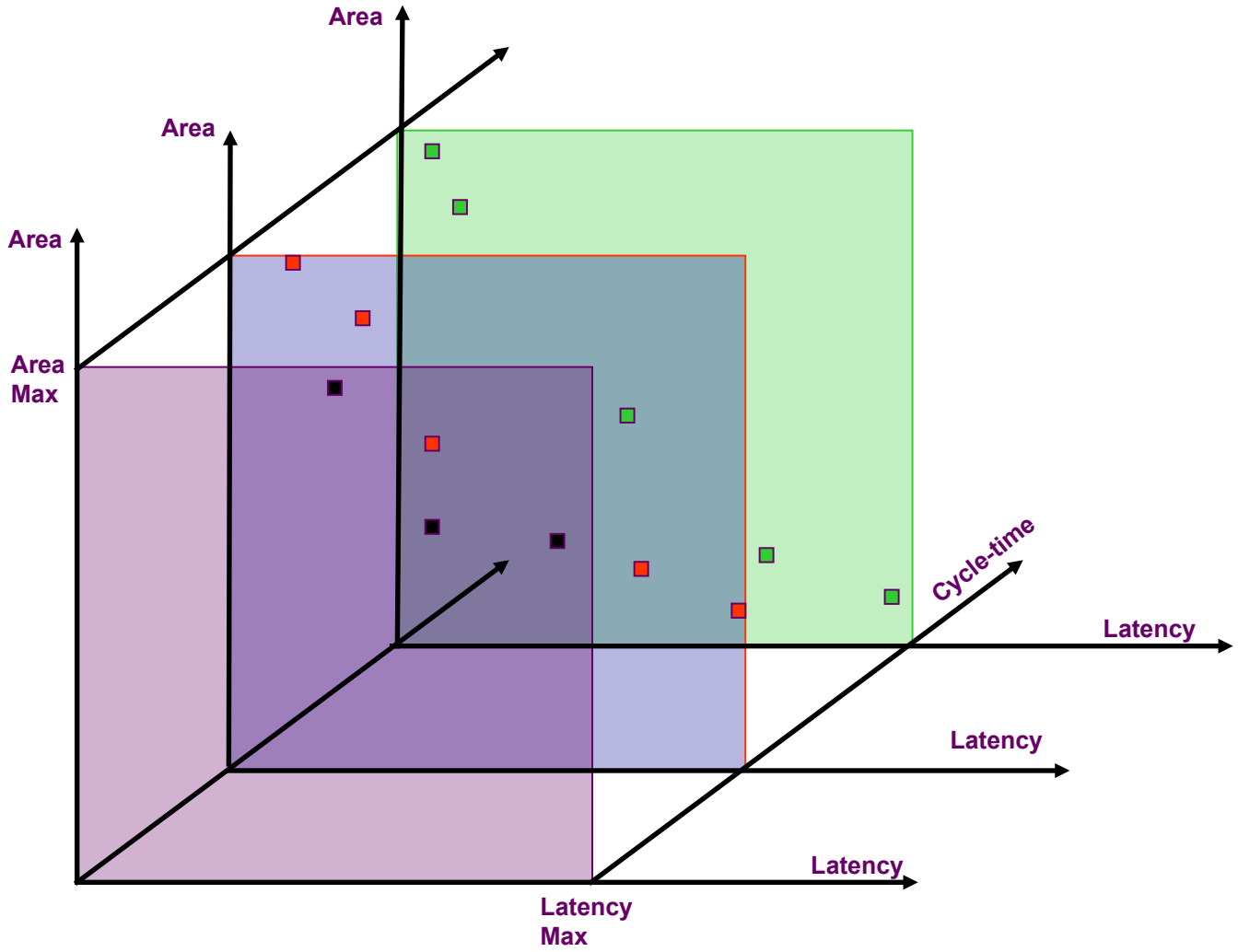
Synthesis and optimization

- Synthesis with no optimization has no value
- Optimization is the means to outperform manual design
- Objectives
  - Performance
    - Frequency, latency, throughput
  - Energy consumption
  - Area (yield and packaging cost)
  - Testability, dependability, ...
- Optimization has multiple objectives
  - Trade off

Combinational circuit optimization



Optimization trade-off in sequential circuits



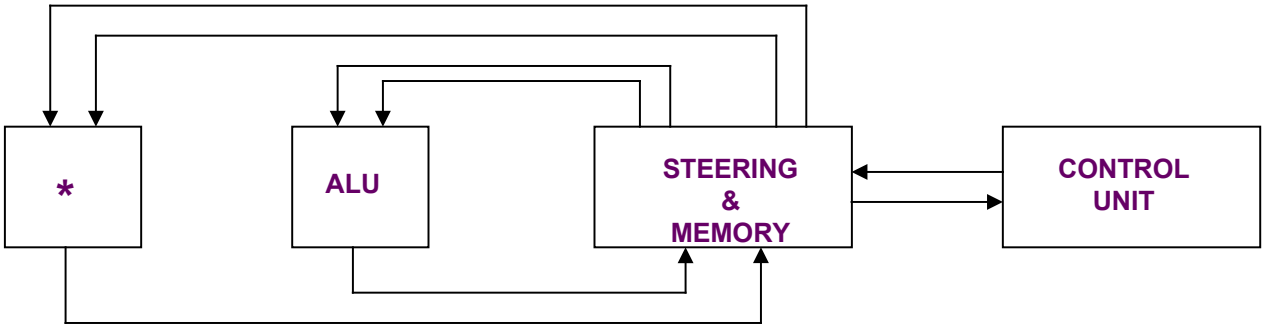
Pareto points

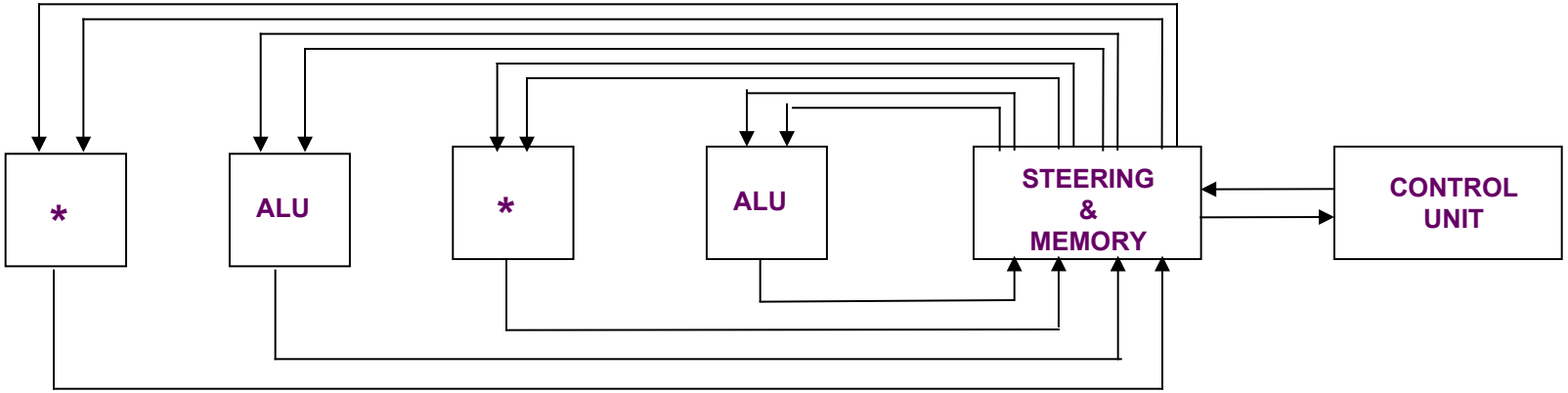
- Multi-criteria optimization
- Multiple objectives
- Pareto point:
  - A point of the design space is a Pareto point if there is no other point with:
    - At least one inferior objectives
    - All other objectives inferior or equal

Example
Differential equation solver

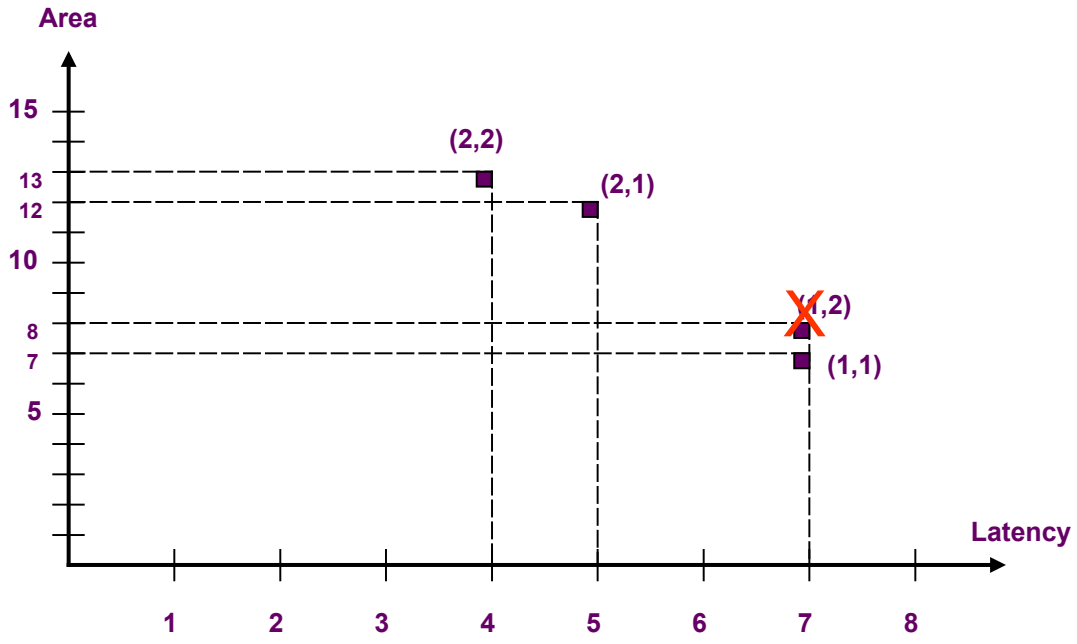
```
diffeq {
    read ( x, y, u, dx, a ) ;
    repeat {
        xl = x + dx;
        ul = u – ( 3 . x . u . dx ) – ( 3 . y . dx ) ;
        yl = y + u . dx ;
        c = x < a ;
        x = xl; u = ul; y = yl ;
    until ( c );
write ( y )
}
```

Example


*
ALU
STEERING
&
MEMORY
CONTROL
UNIT


*
ALU
*
ALU
STEERING
&
MEMORY
CONTROL
UNIT

Example



Summary

- Computer-aided IC design methodology:
  - Capture design by HDL models
  - Synthesize more detailed abstractions
  - Optimize circuit parameters
- Computer-aided system design methodology:
  - Support for Hardware/Software co-design
  - Synthesis of hardware, software and interfaces
- Evolving scientific discipline