Logic synthesis: exercises

November 25, 2020

1 Two-level minimization

Let us consider the following incompletely specified function, where f represents the on-set and d the don't care set:

$$\begin{aligned} f &= \bar{a}\bar{b}c + bc\bar{d} + \bar{a}b\bar{c}d + a\bar{b}c \\ d &= \bar{a}\bar{b}\bar{c} + \bar{a}\bar{c}\bar{d} + ab\bar{c}d \end{aligned}$$

- Compute all prime implicants and identify the essential primes.
- Find a cover that minimizes the number of literals of the SOP.
- Find a cover that minimizes the number of variables in the support of the SOP.

2 Multi-level optimization

Let us consider the following Boolean network with two nodes:

$$\begin{aligned} x &= abd + bc + be + abg + ae \\ y &= ade + cd + ce + ef + h \end{aligned}$$

- Calculate the kernels of both functions.
- Extract the best multi-cube common divisor.
- Create a new node with the divisor and substitute in the previous expressions.

3 Technology mapping

Consider a gate library that only has three gates: 2-input NAND, 2-input NOR and inverter. The area cost of the NAND and NOR gates is 2, whereas the inverter has cost 1. We want to do technology mapping using on ly 2-input NAND gates and inverters as base functions in the target graph. Answer the following questions:

- Draw the library patterns for the gates in the library using the base functions.
- Consider the following function:

  $$f = a_1b_1 + a_2b_2 + a_3b_3 + a_4b_4.$$

  Draw the most balanced target graph in terms of the base functions and find the most efficient mapping.
- Let us assume that every gate has delay=1 and that the arrival time of all signals is $t = 0$, except for b_4 whose arrival time is $t = 10$. Draw the target graph that minimizes delay and find the most efficient mapping.

4 Binary Decision Diagrams

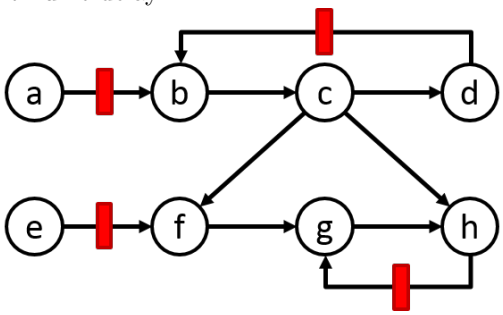
Let us consider two Boolean vectors, $(a_{n-1}, \ldots, a_0)$ and $(b_{n-1}, \ldots, b_0)$, representing the binary encoding of two natural numbers a and b. Let us consider the BDD of a Boolean function that is *true* when $a < b$ and *false* when $a \geq b$.

- What is the variable order that minimizes the BDD size?
- What is the variable order the maximizes the BDD size?

Justify the previous answers and give an asymptotic complexity (using O()) of the BDD size for each case. Draw the BDD of the function considering the best variable order.

5 Retiming

Consider the sequential network shown in the figure, where the rectangles represent registers and the circles represent combinational gates with unit delay.



Answer the following questions:

- What is the minimum period required for the network with the configuration of registers shown in the figure?
- What is the minimum period P_{min} achievable after retiming?
- is the minimum number of registers R_{min} achievable after retiming?
- For all solutions with period equal to P_{min} find one with the minimum number of registers.
- For all solutions with R_{min} registers, find one with minimum period.

Draw a picture with the solutions obtained from the previous questions.