Algorithms for VLSI: Final Exam

January 15th, 2018

1 Channel routing (2.5 points)

Given a channel with the following pin connections:

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TOP = [ACDCABEB]
BOT = [BFFCDDAE]
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- Draw the vertical constraint graph without splitting the nets.
- Determine the zone representation for the nets.
- Draw the vertical constraint graph with net splitting.
- Find the minimum number of required tracks with net splitting and without net splitting.
- Use the Dogleg Left-Edge algorithm to route this channel. For each track, state which nets are assigned. Draw the final routed channel.

2 Multi-level optimization (2.5 points)

Let us consider the following Boolean network with two nodes:

$$x = abd + bc + be + abg + ae$$
$$y = ade + cd + ce + ef + h$$

- Calculate the kernels of both functions.
- Extract the best multi-cube common divisor.
- \bullet Create a new node with the divisor and substitute in the previous expressions.

3 Binary Decision Diagrams (2.5 points)

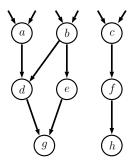
Let us consider two Boolean vectors, (a_{n-1}, \ldots, a_0) and (b_{n-1}, \ldots, b_0) , representing the binary encoding of two natural numbers a and b. Let us consider the BDD of a Boolean function that is *true* when a < b and *false* when $a \ge b$.

- What is the variable order that minimizes the BDD size?
- What is the variable order the maximizes the BDD size?

Justify the previous answers and give an asymptotic complexity (using O()) of the BDD size for each case. Draw the BDD of the function considering the best variable order.

4 High-level synthesis (2.5 points)

Consider the Data Flow Graph (DFG) shown in the figure where all operations use the same type of functional unit (e.g., an ALU). Answer the following questions:



- Give the ASAP and ALAP schedules of the DFG.
- Consider an ILP model for scheduling the DFG using binary variables, where each variable $x_{z,i}$ represents the fact that operation z is scheduled at cycle i. Consider a schedule with 4 cycles in which we want to minimize the number of ALUs.
 - Define the cost function.
 - Define the inequality for resource constraints at cycle 2.
 - Define the inequalities for scheduling operation f.
 - Draw a schedule of the previous DFG with 4 cycles an the minimum number of ALUs.