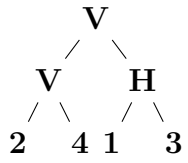
Algorithms for VLSI:
Final Exam

January 12th, 2021

1 Floorplanning (2 points)

Consider the slicing tree of the figure, where V and H represent | and — cuts, respectively. For V cuts, the left child is at the left of the right child. For H cuts, the left child is at the top of the right child. Consider the following dimensions for the blocks:



Block 1: height=2, width=2.
Block 2: height=1, width=1.
Block 3: height=3, width=1.
Block 4: height=1, width=1.

Question: Write the Polish expression of the slicing tree.

Question: Calculate the size of the optimum bounding box of the floorplan under two assumptions:

1. The blocks cannot be rotated.
2. The blocks can be rotated.

Let us assume that the following moves are allowed in the Polish expression that represents the slicing tree:

- Swap two adjacent operands (leaf nodes) in the expression.
- Take a chain of consecutive operators, e.g., HVHV, and complement it, e.g. VHVH.
- Swap an adjacent operator and operand (making sure that the expression is still legal).

Question: Identify **one move** that could be applied to the original Polish expression to obtain an optimum area floorplan with the assumption that no rotations are allowed.

2 Channel routing (2 points)

Given a channel with the following pin connections:

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TOP = [ A D B A C C E D C E ]
BOT = [ B E C B G D E F G F ]
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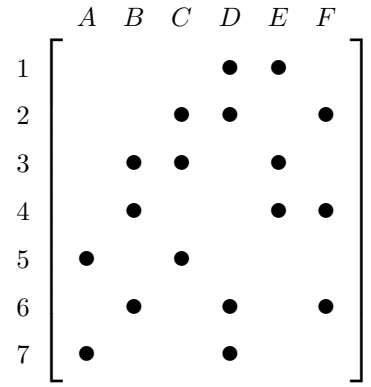
- Determine the zone representation for the nets.
- Draw the vertical constraint graph without splitting the nets.
- Use the Left-Edge algorithm to route this channel without splitting nets. For each track, state which nets are assigned. Draw the final routed channel.
- Draw the vertical constraint graph with net splitting.
- Use the Dogleg Left-Edge algorithm to route this channel. For each track, state which nets are assigned. Draw the final routed channel.

3 Unate covering (2 points)

Consider the following unate covering problem in which you have to select a minimum set of columns that cover the rows of the matrix.



1. Find a minimum-cost solution indicating all the steps and decisions taken during resolution of the problem (e.g., dominances, essential, etc.). Draw the remaining matrix after each step.
2. Find another minimum-cost solution that uses as many different columns from the first solution as possible.

Suggestion: Use column D for the first decision.

4 Multi-level logic synthesis (2 points)

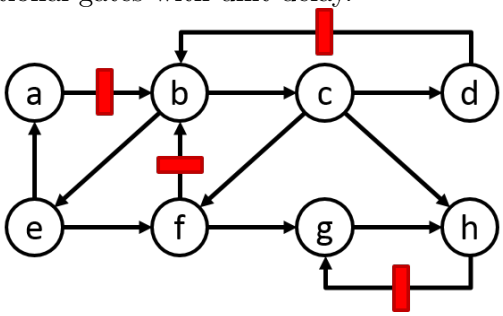
Consider the logic network defined by the following expressions:

$$\begin{aligned} x &= a\overline{d} + \overline{a}\overline{b} + \overline{a}\overline{d} + bc + b\overline{d} + ac \\ y &= a + b \\ z &= \overline{a}\ \overline{c} + \overline{a}\overline{d} + \overline{b}\overline{c} + \end{aligned}$$

- Draw the logic network graph. The outputs are $\{x, y, z, u\}$.
- Perform the algebraic division f_x/f_y, substitute y into f_x and redraw the network graph.
- Compute all kernels and co-kernels of z and u.
- Extract a multiple-cube subexpression common to f_z and f_u. Redraw the network graph.

5 Retiming (2 points)

Consider the sequential network shown in the figure, where the rectangles represent registers and the circles represent combinational gates with unit delay.



Answer the following questions:

- What is the minimum period required for the network with the configuration of registers shown in the figure?
- What is the minimum period P_{min} achievable after retiming?
- What is the minimum number of registers R_{min} achievable after retiming?

Draw a picture with the solutions obtained from the previous questions.