Algorithms for VLSI: Final Exam

January 15th, 2020

1 Floorplanning (2 points)

Consider the following Polish expression:

$$25V1H374VH6V8VH$$

where the (width,height) of the modules 1 through 8 are:

$$\{(2,4),(1,3),(3,3),(3,5),(3,2),(5,3),(1,2),(2,4)\}$$

1. Draw the slicing tree of the floorplan assuming that V and H represent | and — cuts, respectively.
2. Calculate the minimum area of the slicing floorplan assuming that no rotation is allowed. Annotate each node of the tree with its corresponding (width,height).
3. Give a Sequence Pair representation of the same floorplan.

2 Channel routing (2 points)

Given a channel with the following pin connections (0 means no pin):

```
TOP = [ 2 1 3 0 3 2 2 0 4 5 0 ]
BOT = [ 4 0 2 3 1 4 5 0 0 3 4 ]
```

- Determine the zone representation for the nets.
- Draw the vertical constraint graph without splitting the nets.
- Draw the vertical constraint graph with net splitting.
- Use the Dogleg Left-Edge algorithm to route this channel. For each track, state which nets are assigned. Draw the final routed channel.

3 Unate covering (2 points)

Consider the following unate covering problem in which you have to select a minimum set of columns that cover the rows of the matrix.

$$
\begin{array}{cc}
 & \begin{array}{cccccc} A & B & C & D & E & F \end{array} \\
\begin{array}{c} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \end{array} &
\begin{bmatrix}
\bullet & & & & & \bullet \\
\bullet & & \bullet & & \bullet & \\
\bullet & & & \bullet & & \\
 & \bullet & & & \bullet & \bullet \\
 & & \bullet & \bullet & & \\
\bullet & \bullet & & & \bullet & \\
 & \bullet & \bullet & & & \bullet
\end{bmatrix}
\end{array}
$$

1. Find a minimum-cost solution indicating all the steps and decisions taken during resolution of the problem (e.g., dominances, essential, etc.). Draw the remaining matrix after each step.
2. Find another minimum-cost solution that uses as many different columns from the first solution as possible.

4 ROBDDs (2 points)

Totally symmetric functions are characterized by the fact that the value of each such function is determined by the number of variables which are 1 under a truth assignment; it does not matter which particular variables are. For example, the functions:

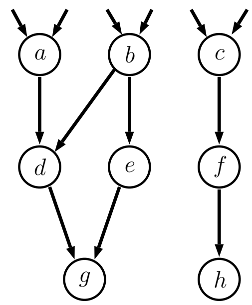
$$
\begin{aligned}
f_1 &= x_1 \wedge \cdots \wedge x_n \\
f_2 &= x_1 \vee \cdots \vee x_n \\
f_3 &= x_1 \oplus \cdots \oplus x_n
\end{aligned}
$$

are totally symmetric. A totally symmetric function on n variables can be described by a set $S \subseteq \{0, 1, \ldots n\}$ such that for a minterm $a \in B^n$, $f(a) = 1$ iff the number of 1's in a is a member of S. Comment on the following aspects of the ROBDD:

- Best and worst variable order of the ROBDD.
- Worst-case size of the ROBDD (in big-O notation).
- Sketch the shape of the ROBDD for a function in which all the minterms have k 1's.

5 High-level synthesis (2 points)

Consider the Data Flow Graph (DFG) shown in the figure where all operations use the same type of functional unit (e.g., an ALU). We want to consider the set of schedules with a latency of 4 cycles. Answer the following questions:



- Give the ASAP and ALAP schedules of the DFG (for a latency of 4 cycles).
- Consider an ILP model for scheduling the DFG using binary variables, where each variable $x_{z,i}$ represents the fact that operation z is scheduled at cycle i. Consider a schedule with a latency of 4 cycles in which we want to minimize the number of ALUs.
  - Define the cost function.
  - Define the inequality for resource constraints at cycle 3.
  - Define the inequalities for scheduling operation d.
  - Draw a schedule of the previous DFG with 4 cycles an the minimum number of ALUs.