**Project Specification Draft: RISC-V 5-Stage Pipelined CPU and Verification**

**Objective:**  
Design, implement, and verify a single-core, in-order, single-issue RV32I CPU with a classical 5-stage pipeline (IF, ID, EX, MEM, WB). Achieve full functional compliance with the RV32I base ISA.

**Scope:**

* RTL design of the CPU core written in SystemVerilog.
* Verification environment implemented in SystemVerilog using UVM methodology.
* Simulation and verification to be performed in Siemens Questa Sim.
* Compliance validation through the official riscv-compliance suite.
* 100% ISA compliance in simulation.
* CPU implemented on FPGA able to run riscv-compliance test programs.

**Design Requirements:**

1. **ISA Coverage**
   * Full implementation of RV32I base integer instruction set, v2.1 as specified by RISC-V Instruction Set Manual Volume I, Unprivileged Architecture.
   * All instruction formats (R, I, S, B, U, J) supported.
   * ECALL/EBREAK can be merged into one trap and still be compliant.
   * FENCE can be treated as NOP and still be compliant.
   * In order to run compiled programs, minimal subset of Privileged Architecture must be implemented: CSRRW, CSRRS, CSRRC, CSRRWI, CSRRSI, CSRRCI
   * For compliance suite: MRET instruction must be implemented to return from traps
2. **Pipeline Structure**
   * Classical 5-stage pipeline: IF, ID, EX, MEM, WB.
   * Single-issue, in-order execution.
   * Pipeline hazards must be resolved (forwarding, stalling, branch handling).
3. **Control Flow**
   * Support for conditional branches and unconditional jumps.
   * Proper PC update logic and flush on misprediction or control transfer.
4. **Memory Interface**
   * Simple synchronous memory interface for instruction fetch and data access.
   * Word-aligned accesses with correct handling of byte/halfword/word load and store.
   * Omit support for misaligned memory accesses
5. **Exception Handling**
   * Instruction alignment faults detected and handled per RV32I spec (instruction-address-misaligned).
   * Illegal instruction detection (illegal-instruction).
6. **Verification Requirements**
   * Testbench built using UVM methodology.
   * Randomized and directed stimulus where appropriate.
   * riscv-compliance suite must execute to completion with no failures.
7. **Tool Flow Requirements**
   * RTL and testbench written in synthesizable, tool-compatible SystemVerilog.
   * All simulations run on Siemens Questa Sim.
   * Synthesis performed using Xilinx Vivado’s synthesis tool
8. **Success Metrics**
   * 100% ISA compliance through riscv-compliance suite.
   * 100% functional coverage of all RV32I instructions in simulation.
   * 100% of directed hazard tests passed (data hazards, control hazards, structural hazards).
   * ≥ 95% code coverage (line, branch, toggle) of RTL from UVM testbench.
   * ≥ 95% functional coverage of UVM environment scenarios.

**Deliverables:**

1. SystemVerilog RTL source for the CPU core.
2. UVM testbench source, including directed and randomized tests.
3. Integration of the riscv-compliance suite with verification results demonstrating 100% compliance.
4. FPGA prototype demonstrating functional execution of RV32I instructions.