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EE 310

April 4, 2017

Lab 6: Memory Report

Introduction

We implemented a memory module on the FPGA board.

Activity 1

Inputs:	Outputs:
address (8 bits) clock (1 bit) data (8 bits) wren (1 bit)	q (8 bits)

What is the value of the generic parameter **operation_mode**? SINGLE_PORT

What is the value of **outdata_reg_a**? UNREGISTERED

What is the aspect ratio of this memory? 256 x 8

VHDL Code

```
-- megafunction wizard: %RAM: 1-PORT%

-- GENERATION: STANDARD

-- VERSION: WM1.0

-- MODULE: altsyncram


-- ============================================================

-- File Name: ramlpm.vhd

-- Megafunction Name(s):

--                          altsyncram

--

-- Simulation Library Files(s):

--                          altera_mf

-- ============================================================

-- ************************************************************
```

```
-- THIS IS A WIZARD-GENERATED FILE. DO NOT EDIT THIS FILE!
--
-- 16.0.2 Build 222 07/20/2016 SJ Standard Edition
-- ************************************************************
```



```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

LIBRARY altera_mf;
USE altera_mf.altera_mf_components.all;

ENTITY ramlpm IS
	PORT
	(
		address		: IN STD_LOGIC_VECTOR (7 DOWNTO 0);
		clock		: IN STD_LOGIC  := '1';
		data		: IN STD_LOGIC_VECTOR (7 DOWNTO 0);
```

```
		wren		: IN STD_LOGIC ;
		q		: OUT STD_LOGIC_VECTOR (7 DOWNTO 0)
	);
END ramlpm;


ARCHITECTURE SYN OF ramlpm IS

	SIGNAL sub_wire0	: STD_LOGIC_VECTOR (7 DOWNTO 0);

BEGIN
	q    <= sub_wire0(7 DOWNTO 0);

	altsyncram_component : altsyncram
	GENERIC MAP (
		clock_enable_input_a => "BYPASS",
		clock_enable_output_a => "BYPASS",
		intended_device_family => "Cyclone V",
		lpm_hint => "ENABLE_RUNTIME_MOD=NO",
		lpm_type => "altsyncram",
		numwords_a => 256,
		operation_mode => "SINGLE_PORT",
		outdata_aclr_a => "NONE",
		outdata_reg_a => "UNREGISTERED",
		power_up_uninitialized => "FALSE",
		ram_block_type => "M10K",
		read_during_write_mode_port_a => "NEW_DATA_NO_NBE_READ",
		widthad_a => 8,
		width_a => 8,
		width_byteena_a => 1
	)
	PORT MAP (
		address_a => address,
		clock0 => clock,
```

```
                data_a => data,
                wren_a => wren,
                q_a => sub_wire0
        );



END SYN;

-- ============================================================
-- CNX file retrieval info
-- ============================================================
-- Retrieval info: PRIVATE: ADDRESSSTALL_A NUMERIC "0"
-- Retrieval info: PRIVATE: AclrAddr NUMERIC "0"
-- Retrieval info: PRIVATE: AclrByte NUMERIC "0"
-- Retrieval info: PRIVATE: AclrData NUMERIC "0"
-- Retrieval info: PRIVATE: AclrOutput NUMERIC "0"
-- Retrieval info: PRIVATE: BYTE_ENABLE NUMERIC "0"
-- Retrieval info: PRIVATE: BYTE_SIZE NUMERIC "8"
-- Retrieval info: PRIVATE: BlankMemory NUMERIC "1"
-- Retrieval info: PRIVATE: CLOCK_ENABLE_INPUT_A NUMERIC "0"
-- Retrieval info: PRIVATE: CLOCK_ENABLE_OUTPUT_A NUMERIC "0"
-- Retrieval info: PRIVATE: Clken NUMERIC "0"
-- Retrieval info: PRIVATE: DataBusSeparated NUMERIC "1"
-- Retrieval info: PRIVATE: IMPLEMENT_IN_LES NUMERIC "0"
-- Retrieval info: PRIVATE: INIT_FILE_LAYOUT STRING "PORT_A"
-- Retrieval info: PRIVATE: INIT_TO_SIM_X NUMERIC "0"
-- Retrieval info: PRIVATE: INTENDED_DEVICE_FAMILY STRING "Cyclone V"
-- Retrieval info: PRIVATE: JTAG_ENABLED NUMERIC "0"
-- Retrieval info: PRIVATE: JTAG_ID STRING "NONE"
-- Retrieval info: PRIVATE: MAXIMUM_DEPTH NUMERIC "0"
-- Retrieval info: PRIVATE: MIFfilename STRING ""
-- Retrieval info: PRIVATE: NUMWORDS_A NUMERIC "256"
-- Retrieval info: PRIVATE: RAM_BLOCK_TYPE NUMERIC "2"
```

-- Retrieval info: PRIVATE: READ_DURING_WRITE_MODE_PORT_A NUMERIC "3"

-- Retrieval info: PRIVATE: RegAddr NUMERIC "1"

-- Retrieval info: PRIVATE: RegData NUMERIC "1"

-- Retrieval info: PRIVATE: RegOutput NUMERIC "0"

-- Retrieval info: PRIVATE: SYNTH_WRAPPER_GEN_POSTFIX STRING "0"

-- Retrieval info: PRIVATE: SingleClock NUMERIC "1"

-- Retrieval info: PRIVATE: UseDQRAM NUMERIC "1"

-- Retrieval info: PRIVATE: WRCONTROL_ACLR_A NUMERIC "0"

-- Retrieval info: PRIVATE: WidthAddr NUMERIC "8"

-- Retrieval info: PRIVATE: WidthData NUMERIC "8"

-- Retrieval info: PRIVATE: rden NUMERIC "0"

-- Retrieval info: LIBRARY: altera_mf altera_mf.altera_mf_components.all

-- Retrieval info: CONSTANT: CLOCK_ENABLE_INPUT_A STRING "BYPASS"

-- Retrieval info: CONSTANT: CLOCK_ENABLE_OUTPUT_A STRING "BYPASS"

-- Retrieval info: CONSTANT: INTENDED_DEVICE_FAMILY STRING "Cyclone V"

-- Retrieval info: CONSTANT: LPM_HINT STRING "ENABLE_RUNTIME_MOD=NO"

-- Retrieval info: CONSTANT: LPM_TYPE STRING "altsyncram"

-- Retrieval info: CONSTANT: NUMWORDS_A NUMERIC "256"

-- Retrieval info: CONSTANT: OPERATION_MODE STRING "SINGLE_PORT"

-- Retrieval info: CONSTANT: OUTDATA_ACLR_A STRING "NONE"

-- Retrieval info: CONSTANT: OUTDATA_REG_A STRING "UNREGISTERED"

-- Retrieval info: CONSTANT: POWER_UP_UNINITIALIZED STRING "FALSE"

-- Retrieval info: CONSTANT: RAM_BLOCK_TYPE STRING "M10K"

-- Retrieval info: CONSTANT: READ_DURING_WRITE_MODE_PORT_A STRING "NEW_DATA_NO_NBE_READ"

-- Retrieval info: CONSTANT: WIDTHAD_A NUMERIC "8"

-- Retrieval info: CONSTANT: WIDTH_A NUMERIC "8"

-- Retrieval info: CONSTANT: WIDTH_BYTEENA_A NUMERIC "1"

-- Retrieval info: USED_PORT: address 0 0 8 0 INPUT NODEFVAL "address[7..0]"

-- Retrieval info: USED_PORT: clock 0 0 0 0 INPUT VCC "clock"

-- Retrieval info: USED_PORT: data 0 0 8 0 INPUT NODEFVAL "data[7..0]"

-- Retrieval info: USED_PORT: q 0 0 8 0 OUTPUT NODEFVAL "q[7..0]"

-- Retrieval info: USED_PORT: wren 0 0 0 0 INPUT NODEFVAL "wren"

-- Retrieval info: CONNECT: @address_a 0 0 8 0 address 0 0 8 0

-- Retrieval info: CONNECT: @clock0 0 0 0 0 clock 0 0 0 0

-- Retrieval info: CONNECT: @data_a 0 0 8 0 data 0 0 8 0

-- Retrieval info: CONNECT: @wren_a 0 0 0 0 wren 0 0 0 0

-- Retrieval info: CONNECT: q 0 0 8 0 @q_a 0 0 8 0

-- Retrieval info: GEN_FILE: TYPE_NORMAL ramlpm.vhd TRUE

-- Retrieval info: GEN_FILE: TYPE_NORMAL ramlpm.inc FALSE

-- Retrieval info: GEN_FILE: TYPE_NORMAL ramlpm.cmp TRUE

-- Retrieval info: GEN_FILE: TYPE_NORMAL ramlpm.bsf TRUE

-- Retrieval info: GEN_FILE: TYPE_NORMAL ramlpm_inst.vhd TRUE

-- Retrieval info: LIB_FILE: altera_mf

Do Code

Part 1: Read first 16 addresses' initial data

add wave -in *

add wave -out *

restart -f

force clock 0 0ns, 1 50ns -r 100ns;

force data(7 downto 0) "11111111";

force wren 0;

force address(0) 0 0ns, 1 100ns -r 200ns;

force address(1) 0 0ns, 1 200ns -r 400ns;

force address(2) 0 0ns, 1 400ns -r 800ns;

force address(3) 0 0ns, 1 800ns -r 1600ns;

force address(7 downto 4) "0000";

run 1600ns;

Part 2: Testing read/write

add wave -in *

add wave -out *

restart -f

force wren 1

force clk 0 0ns, 1 20ns -r 40ns

force address x"00"

```
force data x"0F"
run 40ns

force address x"01"
force data x"1E"
run 40ns
force address x"02"
force data x"2D"
run 40ns
force address x"03"
force data x"3C"
run 40ns
force address x"04"
force data x"4B"
run 40ns
force address x"05"
force data x"5A"
run 40ns
force address x"06"
force data x"69"
run 40ns
force address x"07"
force data x"78"
run 40ns
force address x"08"
force data x"87"
run 40ns
force address x"09"
force data x"96"
run 40ns
force address x"0A"
force data x"A5"
run 40ns
force address x"0B"
```

```
force data x"B4"
run 40ns
force address x"0C"
force data x"C3"
run 40ns
force address x"0D"
force data x"D2"
run 40ns
force address x"0E"
force data x"E1"
run 40ns
force address x"0F"
force data x"F0"
run 40ns
```

Activity 2

VHDL Code

ramplminit.vhd

```
-- megafunction wizard: %RAM: 1-PORT%
-- GENERATION: STANDARD
-- VERSION: WM1.0
-- MODULE: altsyncram


-- ============================================================
-- File Name: ramlpminit.vhd
-- Megafunction Name(s):
--                                altsyncram
--
-- Simulation Library Files(s):
--                                altera_mf
-- ============================================================
-- ************************************************************
-- THIS IS A WIZARD-GENERATED FILE. DO NOT EDIT THIS FILE!
--
-- 16.0.2 Build 222 07/20/2016 SJ Standard Edition
```

```
-- ************************************************************


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--that your use is for the sole purpose of programming logic
--devices manufactured by Altera and sold by Altera or its
--authorized distributors.  Please refer to the applicable
--agreement for further details.


LIBRARY ieee;
USE ieee.std_logic_1164.all;

LIBRARY altera_mf;
USE altera_mf.altera_mf_components.all;

ENTITY ramlpminit IS
	PORT
	(
		address		: IN STD_LOGIC_VECTOR (7 DOWNTO 0);
		clock		: IN STD_LOGIC  := '1';
		data		: IN STD_LOGIC_VECTOR (7 DOWNTO 0);
		wren		: IN STD_LOGIC ;
		q		: OUT STD_LOGIC_VECTOR (7 DOWNTO 0)
	);
```

```
END ramlpminit;


ARCHITECTURE SYN OF ramlpminit IS

	SIGNAL sub_wire0	: STD_LOGIC_VECTOR (7 DOWNTO 0);

BEGIN
	q	<= sub_wire0(7 DOWNTO 0);

	altsyncram_component : altsyncram
	GENERIC MAP (
		clock_enable_input_a => "BYPASS",
		clock_enable_output_a => "BYPASS",
		init_file => "ramlpminit.mif",
		intended_device_family => "Cyclone V",
		lpm_hint => "ENABLE_RUNTIME_MOD=NO",
		lpm_type => "altsyncram",
		numwords_a => 256,
		operation_mode => "SINGLE_PORT",
		outdata_aclr_a => "NONE",
		outdata_reg_a => "UNREGISTERED",
		power_up_uninitialized => "FALSE",
		read_during_write_mode_port_a => "NEW_DATA_NO_NBE_READ",
		widthad_a => 8,
		width_a => 8,
		width_byteena_a => 1
	)
	PORT MAP (
		address_a => address,
		clock0 => clock,
		data_a => data,
		wren_a => wren,
		q_a => sub_wire0
```

```
	);



END SYN;


-- ============================================================
-- CNX file retrieval info
-- ============================================================
-- Retrieval info: PRIVATE: ADDRESSSTALL_A NUMERIC "0"
-- Retrieval info: PRIVATE: AclrAddr NUMERIC "0"
-- Retrieval info: PRIVATE: AclrByte NUMERIC "0"
-- Retrieval info: PRIVATE: AclrData NUMERIC "0"
-- Retrieval info: PRIVATE: AclrOutput NUMERIC "0"
-- Retrieval info: PRIVATE: BYTE_ENABLE NUMERIC "0"
-- Retrieval info: PRIVATE: BYTE_SIZE NUMERIC "8"
-- Retrieval info: PRIVATE: BlankMemory NUMERIC "0"
-- Retrieval info: PRIVATE: CLOCK_ENABLE_INPUT_A NUMERIC "0"
-- Retrieval info: PRIVATE: CLOCK_ENABLE_OUTPUT_A NUMERIC "0"
-- Retrieval info: PRIVATE: Clken NUMERIC "0"
-- Retrieval info: PRIVATE: DataBusSeparated NUMERIC "1"
-- Retrieval info: PRIVATE: IMPLEMENT_IN_LES NUMERIC "0"
-- Retrieval info: PRIVATE: INIT_FILE_LAYOUT STRING "PORT_A"
-- Retrieval info: PRIVATE: INIT_TO_SIM_X NUMERIC "0"
-- Retrieval info: PRIVATE: INTENDED_DEVICE_FAMILY STRING "Cyclone V"
-- Retrieval info: PRIVATE: JTAG_ENABLED NUMERIC "0"
-- Retrieval info: PRIVATE: JTAG_ID STRING "NONE"
-- Retrieval info: PRIVATE: MAXIMUM_DEPTH NUMERIC "0"
-- Retrieval info: PRIVATE: MIFfilename STRING "ramlpminit.mif"
-- Retrieval info: PRIVATE: NUMWORDS_A NUMERIC "256"
-- Retrieval info: PRIVATE: RAM_BLOCK_TYPE NUMERIC "0"
-- Retrieval info: PRIVATE: READ_DURING_WRITE_MODE_PORT_A NUMERIC "3"
-- Retrieval info: PRIVATE: RegAddr NUMERIC "1"
-- Retrieval info: PRIVATE: RegData NUMERIC "1"
```

-- Retrieval info: PRIVATE: RegOutput NUMERIC "0"

-- Retrieval info: PRIVATE: SYNTH_WRAPPER_GEN_POSTFIX STRING "0"

-- Retrieval info: PRIVATE: SingleClock NUMERIC "1"

-- Retrieval info: PRIVATE: UseDQRAM NUMERIC "1"

-- Retrieval info: PRIVATE: WRCONTROL_ACLR_A NUMERIC "0"

-- Retrieval info: PRIVATE: WidthAddr NUMERIC "8"

-- Retrieval info: PRIVATE: WidthData NUMERIC "8"

-- Retrieval info: PRIVATE: rden NUMERIC "0"

-- Retrieval info: LIBRARY: altera_mf altera_mf.altera_mf_components.all

-- Retrieval info: CONSTANT: CLOCK_ENABLE_INPUT_A STRING "BYPASS"

-- Retrieval info: CONSTANT: CLOCK_ENABLE_OUTPUT_A STRING "BYPASS"

-- Retrieval info: CONSTANT: INIT_FILE STRING "ramlpminit.mif"

-- Retrieval info: CONSTANT: INTENDED_DEVICE_FAMILY STRING "Cyclone V"

-- Retrieval info: CONSTANT: LPM_HINT STRING "ENABLE_RUNTIME_MOD=NO"

-- Retrieval info: CONSTANT: LPM_TYPE STRING "altsyncram"

-- Retrieval info: CONSTANT: NUMWORDS_A NUMERIC "256"

-- Retrieval info: CONSTANT: OPERATION_MODE STRING "SINGLE_PORT"

-- Retrieval info: CONSTANT: OUTDATA_ACLR_A STRING "NONE"

-- Retrieval info: CONSTANT: OUTDATA_REG_A STRING "UNREGISTERED"

-- Retrieval info: CONSTANT: POWER_UP_UNINITIALIZED STRING "FALSE"

-- Retrieval info: CONSTANT: READ_DURING_WRITE_MODE_PORT_A STRING "NEW_DATA_NO_NBE_READ"

-- Retrieval info: CONSTANT: WIDTHAD_A NUMERIC "8"

-- Retrieval info: CONSTANT: WIDTH_A NUMERIC "8"

-- Retrieval info: CONSTANT: WIDTH_BYTEENA_A NUMERIC "1"

-- Retrieval info: USED_PORT: address 0 0 8 0 INPUT NODEFVAL "address[7..0]"

-- Retrieval info: USED_PORT: clock 0 0 0 0 INPUT VCC "clock"

-- Retrieval info: USED_PORT: data 0 0 8 0 INPUT NODEFVAL "data[7..0]"

-- Retrieval info: USED_PORT: q 0 0 8 0 OUTPUT NODEFVAL "q[7..0]"

-- Retrieval info: USED_PORT: wren 0 0 0 0 INPUT NODEFVAL "wren"

-- Retrieval info: CONNECT: @address_a 0 0 8 0 address 0 0 8 0

-- Retrieval info: CONNECT: @clock0 0 0 0 0 clock 0 0 0 0

-- Retrieval info: CONNECT: @data_a 0 0 8 0 data 0 0 8 0

-- Retrieval info: CONNECT: @wren_a 0 0 0 0 wren 0 0 0 0

-- Retrieval info: CONNECT: q 0 0 8 0 @q_a 0 0 8 0

```
-- Retrieval info: GEN_FILE: TYPE_NORMAL ramlpminit.vhd TRUE
-- Retrieval info: GEN_FILE: TYPE_NORMAL ramlpminit.inc FALSE
-- Retrieval info: GEN_FILE: TYPE_NORMAL ramlpminit.cmp TRUE
-- Retrieval info: GEN_FILE: TYPE_NORMAL ramlpminit.bsf TRUE
-- Retrieval info: GEN_FILE: TYPE_NORMAL ramlpminit_inst.vhd TRUE
-- Retrieval info: LIB_FILE: altera_mf
```

Demux2.vhd

```
library ieee;
use ieee.std_logic_1164.all;

entity demux2 is

port(
        data: in std_logic_vector(7 downto 0);
        s: in std_logic;
        address: out std_logic_vector(7 downto 0);
        value_out: out std_logic_vector(7 downto 0)
);

end demux2;

architecture behav of demux2 is
begin
        process(data, s)
                begin
                --load address
                        if (s = '0') then
                                address <= data;
                        elsif (s = '1') then
                                value_out <= data;
                        end if;
        end process;
end behav;
```

Do Code

lab6_ramlpinit_sim.txt

```
add wave -in *

add wave -out *

restart -f


force clk 0 0ns, 1 20ns -r 40ns

force wren 0


force address x"00"

run 40ns

force address x"01"

run 40ns

force address x"02"

run 40ns

force address x"03"

run 40ns

force address x"04"

run 40ns

force address x"05"

run 40ns

force address x"06"

run 40ns

force address x"07"

run 40ns

force address x"08"

run 40ns

force address x"09"

run 40ns

force address x"0A"

run 40ns

force address x"0B"

run 40ns

force address x"0C"
```

run 40ns

force address x"0D"

run 40ns

force address x"0E"

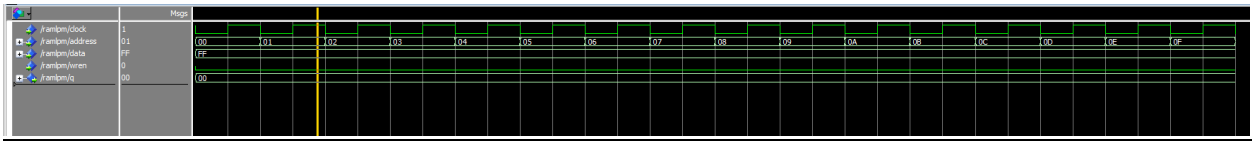
run 40ns

force address x"0F"

run 40ns

Screenshots

Activity 1: Part 1: First 16 addresses' initial values

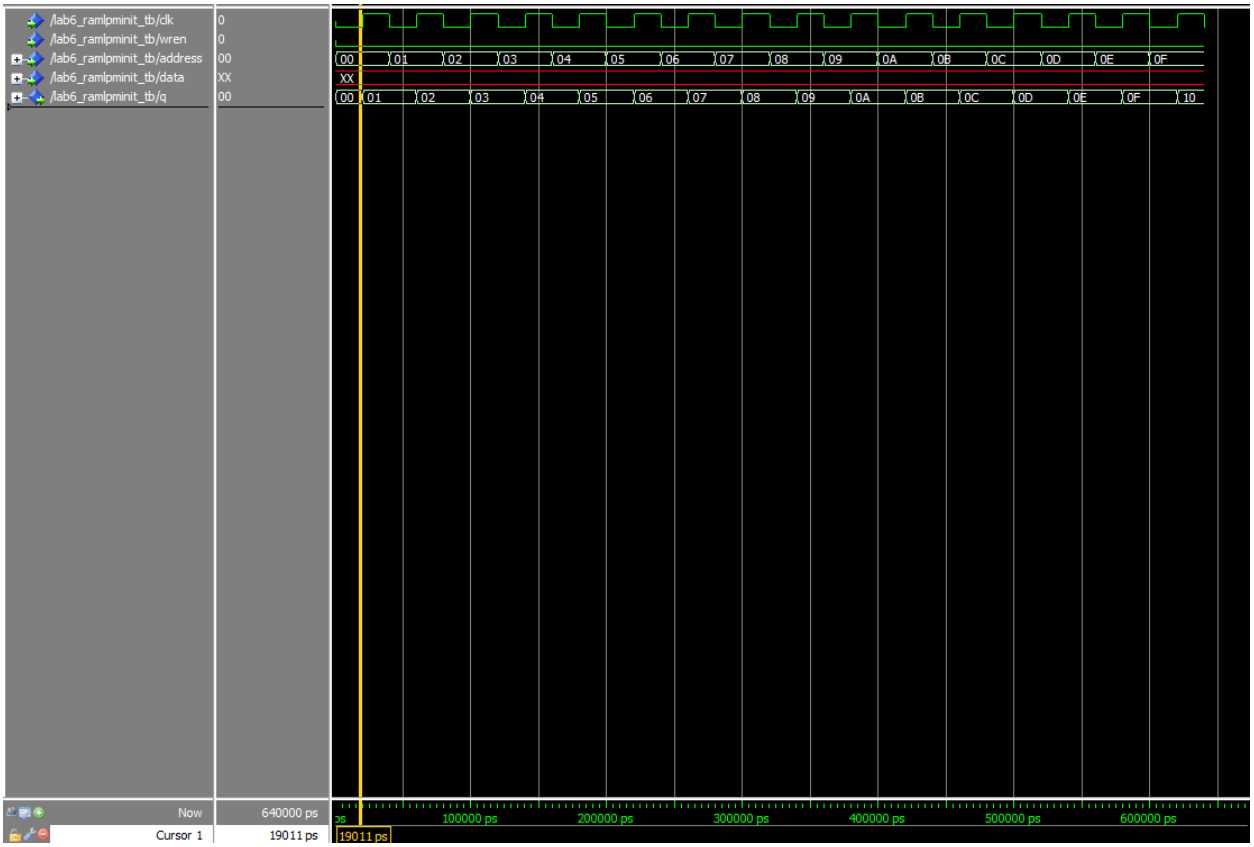


Activity 1: Part 2: Read/write test

Activity 2: mif file

Addr	+0	+1	+2	+3	+4	+5	+6	+7	ASCII
0	1	2	3	4	5	6	7	8	.....
8	9	10	11	12	13	14	15	16	.....
16	0	0	0	0	0	0	0	0	.....
24	0	0	0	0	0	0	0	0	.....
32	0	0	0	0	0	0	0	0	.....
40	0	0	0	0	0	0	0	0	.....
48	0	0	0	0	0	0	0	0	.....
56	0	0	0	0	0	0	0	0	.....
64	0	0	0	0	0	0	0	0	.....
72	0	0	0	0	0	0	0	0	.....
80	0	0	0	0	0	0	0	0	.....
88	0	0	0	0	0	0	0	0	.....
96	0	0	0	0	0	0	0	0	.....
104	0	0	0	0	0	0	0	0	.....
112	0	0	0	0	0	0	0	0	.....
120	0	0	0	0	0	0	0	0	.....
128	0	0	0	0	0	0	0	0	.....
136	0	0	0	0	0	0	0	0	.....
144	0	0	0	0	0	0	0	0	.....

Activity 2: ramlpminit.vhd sim



Conclusion

This was a great lab! It was easy going and we encountered very little errors. Looking forward to lab 7.