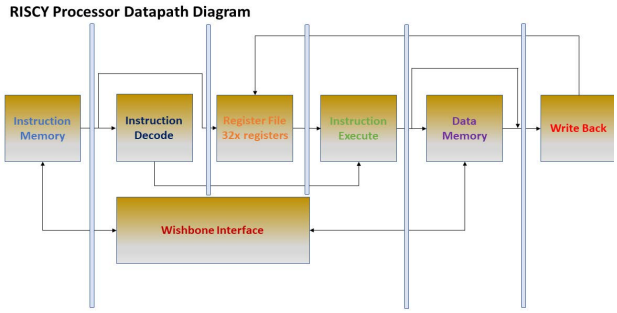
Architecture



Features

- Supports the complete 32-bit RISC-V base integer ISA (RV32I) version 2.0
- Supports machine mode from the RISC-V Privileged Architecture version 1.10
- Includes a hardware timer with microsecond resolution and compare interrupt
- Up to 8 IRQ inputs that can be individually enabled
- Classic 5-stage RISC pipeline
- Wishbone interface
- Optional instruction cache
- Automatic test suite

Interface

The processor includes a wishbone interface conforming to the B4 revision of the wishbone specification.

Interface type	Master
Address port width	32 bits
Data port width	32 bits
Data port granularity	8 bits
Maximum operand size	32 bits
Endianess	Little
Sequence of data transfer	In-order

Specifications

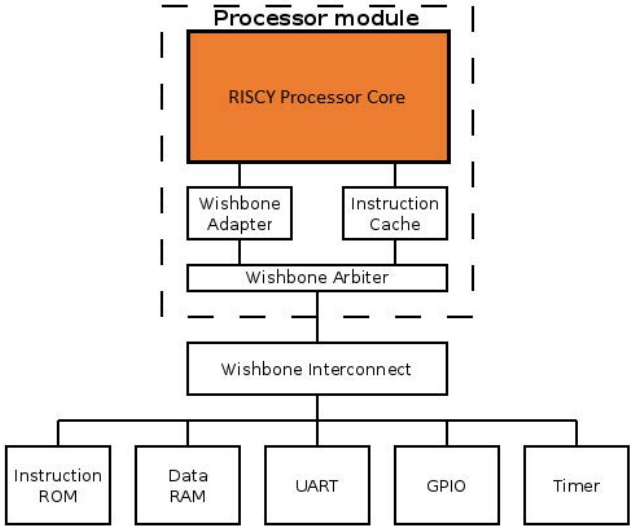
RISC-V

`http://riscv.org/specifications/`

OpenCores www.opencores.org

`http://opencores.org/opencores,wishbone`

Example Application



Signals

The processor is provided by a VHDL module named ry_riscy. All signals are active high and the following signals are provided:

Name	Width	Description
`clk`	1	Processor clock
`timer_clk`	1	10 MHz timer clock
`reset`	1	Reset signal
`irq`	8	IRQ inputs
`wb_adr_out`	32	Wishbone address
`wb_sel_out`	4	Wishbone byte select
`wb_cyc_out`	1	Wishbone cycle
`wb_stb_out`	1	Wishbone strobe
`wb_we_out`	1	Wishbone write enable
`wb_dat_out`	32	Wishbone data output
`wb_dat_in`	32	Wishbone data input
`wb_ack_in`	1	Wishbone acknowledge

An additional output, `test_context_out` is used to provide feedback to testbenches when running automated tests. This port should be left unconnected.

Tools and Utilities

Tools for writing applications for the RISC-V architecture are available from the RISC-V project, at:

`https://github.com/riscv/riscv-gnu-toolchain`