Open-Circuit Fault Detection and Localization in Five-Level Active NPC Converter

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***Abstract*—In this paper a novel and fast open-circuit fault detection and localization method is proposed for Five-level active-neutral-point-clamped (5L-ANPC) converter. The method is based on comparing the measured output voltage with the reference voltage and the voltage obtained from the fault analysis. The implementation scheme of the method is presented; and all the practical aspects including capacitors voltage ripple and system delays are considered. The implementation of the method needs no additional sensor, measurement and processor board. The performance of the proposed method is verified by numerical simulation of a five-level converter. The results confirm the effectiveness and accurate operation of the method for fault detection and localization.**

Keywords—Active-Neutral-Point-Clamped (ANPC) converter; fault detection; fault localization; fault tolerant converter; multilevel inverter; open-circuit fault

I. INTRODUCTION

The five-level Active-Neutral-Point-Clamped (5L-ANPC) converter is introduced by ABB in 2005 [1]. This converter uses four active switches and one floating capacitor for clamping each phase voltage and its sole DC-link is shared between three phases. Thus, it can overcome the drawbacks of traditional multilevel topologies like Neutral-Point-Clamped (NPC), Flying-Capacitor (FC) and Cascaded H-Bridge (CHB) [2], [3] and it is an attractive converter for high-power, wide speed range motor drive applications compare to Modular Multilevel Converter (MMC) [4], [5].

Reliability is one of the most important challenges in the multilevel converters with a high number of switching devices. The switching devices are considered as the main origin of their failure [6]. Some switch fault detection and localization methods are proposed for MMC [6], [7] and CHB [8], [9] converters. Also a few fault detection schemes are proposed for three-level ANPC converter [10-12]. The main drawback of these methods is lack of the attention to their implementation and practical issues.

For five-level ANPC, reconfiguration of the converter and its control after fault are investigated in [13], [14]. In both of them, it is assumed that the fault and its location have already been identified. Thus, proposing a new method for fault detection and localization in this converter seems necessary.

In an earlier work, a fast short circuit fault detection method based on voltage and time criterion is proposed for CHB converter [9]. In this method, fault can be detected by comparing the measured and estimated voltage. In this paper, the same concept is modified to be used for detection and localization of open circuit fault in 5L-ANPC converter. The simplicity of the algorithm and acceptable detection and localization time are the main advantages of the proposed method. This method can be implemented on ANPC converter with any number of levels but in this paper only five-level converter is investigated.

The proposed method detects the fault once the fault is detectable (i.e. affects the normal operation of the converter). The proposed localization method can identify the faulty switch in less than one output cycle in comparison to the impact time of the fault depending on the time of the fault occurrence, current direction and the faulty switch. Both detection and localization method uses DC-link voltage, switching signals and output voltage which DC-link and output voltage are measured for protection and control in the converter. Considering practical aspects like capacitor voltage ripples and delays in the system, make fault detection and localization method robust.

The remaining parts of the paper are organized as follows. Section II briefly introduces the 5L-ANPC VSC topology and its operation principles. The effects of semiconductor power switches open-circuit fault on operation of the converter are analyzed in section III. Sections IV and V propose the fault detection and localization method for this converter. Simulation results based on a realistic ANPC converter are presented in Section VI. Finally, Section VII concludes the paper.

II. FIVE-LEVEL ANPC CONVERTER: TOPOLOGY AND OPERATION PRINCIPLES

The single-phase leg of 5L-ANPC converter is shown in Fig. 1. Assuming that the DC-link voltage "*V*" is constant, the structural features of converter are as follows:

1) The DC-link is shared by three phases and the DC-link capacitors (C_1 and C_2) are charged to *V/2*.

2) Each phase of this converter consists of eight switches and one floating capacitor (C_f). The voltage across C_f is *V/4*.

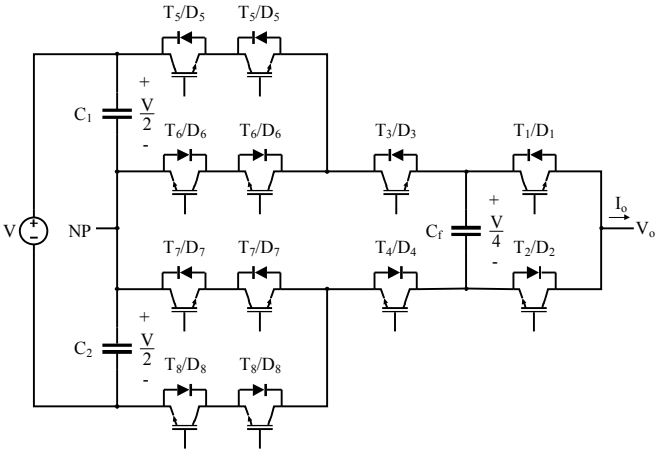

Fig. 1. The single-phase leg of 5L-ANPC converter

3) The switches T_5/D_5 to T_8/D_8 are comprised of two series connected devices. So, all switches are rated for *V/4*.

4) The phase voltage is defined with respect to the midpoint of DC-link (NP).

5) Positive phase current means it flows out of the phase.

Table I provides the switching states of the converter. Since, operation of the switch pairs (T_1, T_2), (T_3, T_4), (T_5, T_6) and (T_7, T_8) are complementary and the switch pairs (T_5, T_7) and (T_6, T_8) have the same switching signals, only T_1, T_3, and T_5 switching signals are listed in the table. According to Table I, the switching frequency of outer switches (T_5, T_6, T_7, and T_8) is same as output frequency while other switches operate at carrier frequency.

This converter generates five levels in the output phase voltage (*V/2*, *V/4*, *0*, *-V/4*, and *–V/2*) with eight switching states. The output phase voltage V_{xo} is given by

$$V_{xo} = [2(T_{x5} - 1) + T_{x3} + T_{x1}]. (V / 4) \quad (1)$$

Where *x* represents phase (*a*, *b*, or *c*) and T_{x1}, T_{x3}, and T_{x5} are equal to "1" or "0" when switches are on or off, respectively.

III. Switch Open-Circuit Fault Effect on 5L_ANPC Converter Operation

Fault in a switch influences normal operation of the converter once the current flows through it. Therefore, detection of faulty switch depends on switches command and output current direction. In following, fault in switches T_1, T_3, T_5, and T_6 is investigated. Due to the symmetric structure of this converter, analysis of other switches fault is similar.

Fault in T_1 affects normal operation of the converter when the output current is positive and the switching state is one of states V_1, V_3, V_5, or V_7. When the output current is negative, D_1 conducts and converter operates normally. Also, in other switching states T_1 is off and the fault is indistinguishable. For example, when T_1 fault occurs in state V_1, the positive current flows through D_2, D_4, and D_8 and the voltage becomes *–V/2* instead of *–V/4*. So, the converter is impressible of the fault and the fault can be detected.

TABLE I. Switching States of 5L-ANPC Converter

Switching States	Switches			Current Path		
	T_5	T_3	T_1	$I_o > 0$	$I_o < 0$	V_{on}
V_0	0	0	0	D_2, D_4, D_8	T_2, T_4, T_8	*-V/2*
V_1	0	0	1	T_1, D_4, D_8	D_1, T_4, T_8	*-V/4*
V_2	0	1	0	D_2, T_3, D_6	T_2, D_3, T_6	*-V/4*
V_3	0	1	1	T_1, T_3, D_6	D_1, D_3, T_6	*0*
V_4	1	0	0	D_2, D_4, T_7	T_2, T_4, D_7	*0*
V_5	1	0	1	T_1, D_4, T_7	D_1, T_4, D_7	*V/4*
V_6	1	1	0	D_2, T_3, T_5	T_2, D_3, D_5	*V/4*
V_7	1	1	1	T_1, T_3, T_5	D_1, D_3, D_5	*V/2*

When the output current is positive and the switching state is one of states V_2, V_3, V_6, or V_7, fault in T_3 is detectable and in other cases, the converter operates normally. For example, if T_3 fails in switching state V_2, the positive current flows through D_2, D_4, and D_8 and the voltage becomes *–V/2* instead of *–V/4*.

The switch T_5 is on during all the positive half-cycle of the phase voltage but the positive current flows through it only in switching states V_6 and V_7. Thus, T_5 fault is detectable in positive half-cycle (in switching states V_6 and V_7) when the output current is positive. For this reason, T_5 fault detection time can be longer than those of T_1, T_2, T_3, and T_4 faults. For example, when T_5 fails in switching state V_6, the positive current flows through D_2, D_4, and T_7 and the output voltage becomes 0 instead of *V/4*.

Fault in T_6 can be detected in negative half-cycle phase voltage when the switching states is V_2 or V_3 and negative output current flows the converter.

Table II provides the output voltage and current path under open-circuit fault situation for all the switches. This table shows only the switching states that are affected by the fault and in other cases, the output voltage is unchanged. Note that $V_{o,f}$ is defined as the output voltage under fault situation.

IV. The Proposed Open-Circuit Fault Detection Method for 5L-ANPCs

The principle of the proposed method is based on the impact of switching states, current direction and switches fault on the phase output voltage. In this method, the phase voltage is measured and compared with the reference voltage produced by DC-link voltage and switching signals according to (1).

The difference between the measured voltage ($V_{xo,m}$) and the reference voltage ($V_{xo,ref}$) is defined "$E_{Det,x}$" and is given by

$$E_{Det,x} = V_{xo,ref} - V_{xo,m} \quad (2)$$

where *x* represents the phase (*a*, *b*, or *c*). In normal operation, the measured voltage is close to the reference voltage. As soon as the switch fault occurs and based on the current direction and the switching state, the fault influences the normal operation of the converter and the measured voltage differs from the reference voltage.

TABLE II. THE OUTPUT VOLTAGE AND CURRENT PATH UNDER FAULT SITUATION

Faulty Switch	Switching State	Current Path	$V_{o,f}$	Current Direction
T_1	V_1	D_2, D_4, D_8	*-V/2*	$I_o > 0$
	V_3	D_2, T_3, D_6	*-V/4*	
	V_5	D_2, D_4, T_7	*0*	
	V_7	D_2, T_3, T_5	*V/4*	
T_2	V_0	D_1, T_4, T_8	*-V/4*	$I_o < 0$
	V_2	D_1, D_3, T_6	*0*	
	V_4	T_1, T_4, D_7	*V/4*	
	V_6	D_1, D_3, D_5	*V/2*	
T_3	V_2	D_2, D_4, D_8	*-V/2*	$I_o > 0$
	V_3	T_1, D_4, D_8	*-V/4*	
	V_6	D_2, D_4, T_7	*0*	
	V_7	T_1, D_4, T_7	*V/4*	
T_4	V_0	T_2, D_3, T_6	*-V/4*	$I_o < 0$
	V_1	D_1, D_3, T_6	*0*	
	V_4	T_2, D_3, D_5	*V/4*	
	V_5	D_1, D_3, D_5	*V/2*	
T_5	V_6	D_2, D_4, T_7	*0*	$I_o > 0$
	V_7	T_1, D_4, T_7	*V/4*	
T_6	V_2	T_2, D_3, D_5	*V/4*	$I_o < 0$
	V_3	D_1, D_3, D_5	*V/2*	
T_7	V_4	D_2, D_4, D_8	*-V/2*	$I_o > 0$
	V_5	T_1, D_4, D_8	*-V/4*	
T_8	V_0	T_2, D_3, T_6	*-V/4*	$I_o < 0$
	V_1	D_1, D_3, T_6	*0*	

Fig. 2 illustrates the implementation scheme of the fault detection method. Note that the method is separately used for each phase and the block diagram for one phase is shown in this figure.

In this block diagram, the reference voltage ($V_{xo,ref}$) is prepared by using the switching pulses (T_{x1}, T_{x3}, and T_{x5}) and DC-link voltage in the reference calculation block. Then this voltage is compared with the measured output voltage ($V_{xo,m}$) and "$E_{Det,x}$" signal is produced. It must be mentioned that the switching pulses are available in the control board and the output voltage and DC-link voltage are measured for control and protection of the converter. So, this method needs no additional sensor or measurement.

Once "$E_{Det,x}$" signal is nonzero, the fault is occurred and can be detected. However, in reality, due to the measurement and discretizing errors, the non-ideal behavior of switches and drivers and capacitors voltage ripple, "$E_{Det,x}$" signal is never zero even during the normal operation of the converter. Thus, considering a "voltage criterion" is necessary to prevent the false fault detection. For this purpose, first the absolute value of "$E_{Det,x}$" is calculated and then is compared with a threshold value of "V_{th}". Note that the threshold value of "V_{th}" can be selected "*V/8*" in 5L-ANPC where "*V*" is DC-link voltage.

On the other hand, in a real system, due to the sensors response time, the analogue to digital (A/D) converters delay, the turn-off and turn-on propagation time in switches and drivers and delays in the controller, always there is a delay between the reference and the measured output voltage. To avoid the false fault detection and consider the "time criterion", a counter is used in this block diagram, too.

When "$E_{Det,x}$" signal is large enough, it is considered as a fault and is applied to an up-counter that computes the number of pulses while the output of the first comparator is high. In the other words, the counter represents the time during which the measured voltage and the reference voltage are different with an error larger than "V_{th}". Then the output of counter is applied to the second comparator with a threshold value of "T_c". If the output counter exceeds the threshold "T_c", the fault signal is set by using a set/reset flip-flop and fault is detected. The output of the first comparator can be set due to the semiconductor switching and the counter starts counting. But, after a short time, the output of comparator becomes zero. Therefore, complementary of this signal is used to reset the counter.

It must be mentioned that the value of "T_c" is selected in such a way that the delay caused by the counter is longer than the sum of delays in the system. For example, if the maximum delay in the measurement and control loop is 20µs and the clock frequency of the counter is 1MHz, "T_c=30" can be selected. It means that after 30µs if the fault exists, "Fault" signal becomes set.

V. THE PROPOSED OPEN-CIRCUIT FAULT LOCALIZATION METHOD FOR 5L-ANPCS

The proposed fault localization method is based on the presented analysis in section III. In the following, this method is presented for the switches T_1, T_3, T_5, and T_6. Because of the symmetric structure of 5L-ANPCs, the method can be extended to other switches easily.

A. T_1 Fault Identification

The faulty switch T_1 can be identified when the output current is positive and the measured output voltage is as follows:

1) *-V/2* (instead of *-V/4*) in switching state V_1.

2) Zero (instead of *V/4*) in switching state V_5.

3) *-V/4* (instead of zero) in switching state V_3 and then *-V/4* in state V_2. In this case, a fault in T_1 or T_3 leads to *-V/4* in state V_3 but a fault in T_3 leads to *-V/2* (instead of *-V/4*) in state V_2, too. Thus, if the output voltage in state V_2 is equal to the

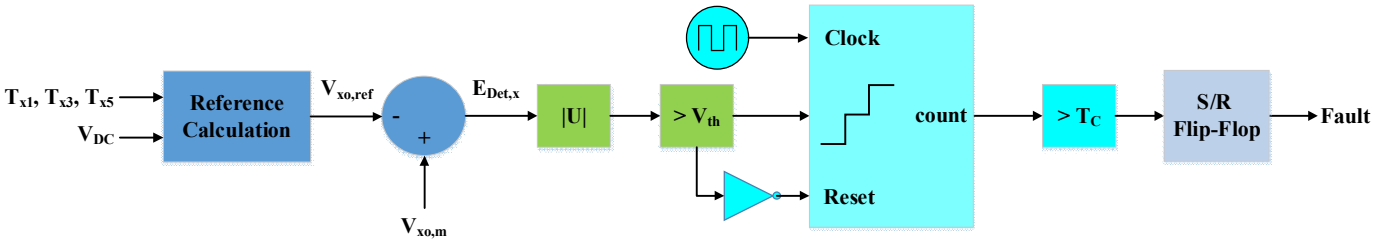

Fig. 2. The implementation scheme of the fault detection method

reference value, the fault is occurred in switch T_1, certainly.

4) *V/4* (instead of *V/2*) in switching state V_7 and then *V/4* in state V_6. Similarly, if the measured voltage in switching state V_7 is *V/4* (instead of *V/2*), the fault could be due to switches T_1, T_3, or T_5 but if the measured voltage in state V_6 is equal to the reference value (*V/4*), the fault is due to T_1. Thus, the output voltage should be *V/4* in V_7 and then *V/4* in V_6 to be able to identify the faulty switch T_1.

B. T_3 Fault Identification

The faulty switch T_3 can be identified when the output current is positive and the measured output voltage is as follows:

1) *-V/2* (instead of *-V/4*) in switching state V_2.

2) *-V/4* (instead of zero) in switching state V_3 and then *V/4* in state V_5 or zero (instead of *V/4*) in state V_6. Since, a fault in T_1 or T_3 leads to *-V/4* in state V_3 but if the measured voltage is equal to the reference value (*V/4*) in state V_5 or zero in state V_6, the fault is due to T_3.

3) Zero (instead of *V/4*) in switching state V_6 and then *-V/4* (instead of zero) in state V_3. Since, zero in V_6 can be also due to a fault in T_5 but if the measured voltage in state V_3 is equal to *-V/4*, the fault is due to T_3, certainly.

C. T_5 Fault Identification

The faulty switch T_5 can be identified when the output current is positive and the measured output voltage is zero (instead of *V/4*) in switching state V_6 and then in switching state V_3. Since, zero in state V_6 can be also due to a fault in T_3 but a fault in T_3 leads to *-V/4* in state V_3 too. Thus, if the output voltage in this state is equal to the reference value, the fault is due to T_5.

D. T_6 Fault Identification

The faulty switch T_6 can be identified when the output current is negative and the measured output voltage is as follows:

1) *V/4* (instead of *-V/4*) in switching state V_2.

2) *V/2* (instead of zero) in switching state V_3.

Table III provides the proposed fault localization method for the open-circuit fault in switches T_2, T_4, T_7, and T_8.

TABLE III. FAULT LOCALIZATION METHOD

Faulty Switch	First Step Switching State	First Step $V_{o,m}$	Second Step Switching State	Second Step $V_{o,m}$	Sign (I_o)
T_2	V_2	*0*	-	-	$I_o < 0$
	V_6	*V/2*	-	-	
	V_0	*-V/4*	V_1	*-V/4*	
	V_4	*V/4*	V_5	*V/4*	
T_4	V_5	*V/2*	-	-	$I_o < 0$
	V_4	*V/4*	V_2	*-V/4*	
	V_4	*V/4*	V_1	*0*	
	V_1	*0*	V_4	*V/4*	
T_7	V_4	*-V/2*	-	-	$I_o > 0$
	V_5	*-V/4*	-	-	
T_8	V_1	*0*	V_4	0	$I_o < 0$

E. Implementation of the Fault Localization method

The implementation of the fault localization method is shown in Fig. 3. This method is separately used for each phase.

In this block diagram, first the switching state is determined by using switching pulses (T_{x1}, T_{x3}, and T_{x5}). For this purpose, a decoder (3 to 8) is used and according to the values of switching pulses, the corresponding switching state is selected.

The faulty switch is detected by using the switching state, the measured output voltage and the current direction in the fault localization block according to the aforementioned algorithm. For this purpose, first the faulty voltage ($V_{xo,f}$) is prepared and then the difference between this voltage and the measured voltage is calculated in a specific switching state. For considering non-ideality factors like capacitor voltage ripple, the absolute value of this deference is compared with a threshold value of "V_{th}". After comparing, if this signal is large enough, it will be applied to an up-counter. This counter represents the time during which measured voltage is equal to $V_{xo,f}$ in this switching state with an error larger than "V_{th}". Then, the output of counter is applied to a comparator with a threshold value of "T_c". This value is determined based on system delays and selected similar to the corresponding value in the fault detection method.

After comparing, if the counter output exceeds the threshold of T_c, the fault is occurred and based on the switching state and the faulty voltage, the faulty switch is identified. Finally, the corresponding faulty switch function ($F(T_i)$, *i = 1 to 8*) becomes set by using a set/reset flip-flop.

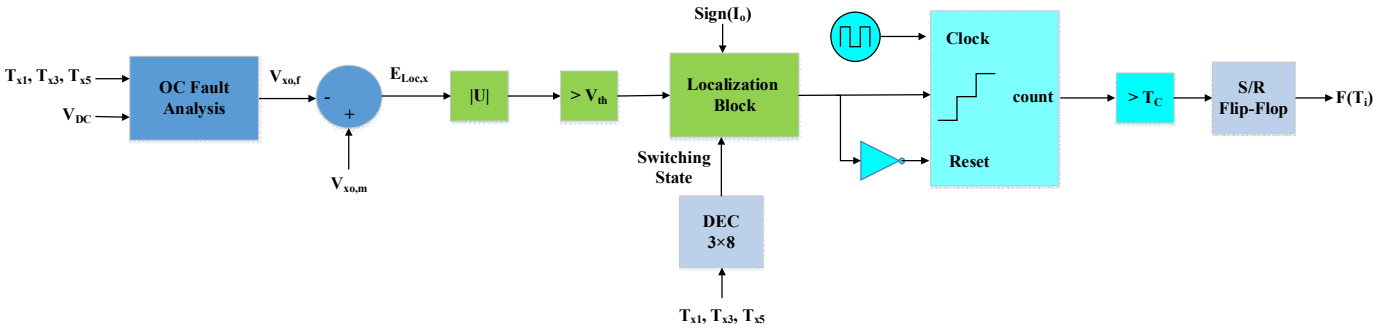

Fig. 3. The logic implementation of fault localization method

VI. Simulation Results

To verify the proposed fault detection and localization method, a five-level ANPC converter is simulated. In Table IV, the converter and load parameters are listed. In this simulation, the maximum delay in the measurement and the control loop is assumed to be 20µs and in the algorithm, counters operate with a clock frequency of 100kHz and the threshold value of $T_c = 3$. The Duration time that counters compute is longer than the sum of delays in the system and makes fault detection very fast. On the other hand, because of the capacitors voltage ripple and to prevent false fault detection V_{th} is selected to be 750V. Since the proposed method applies for each phase independently, the results are shown for one phase.

In the following, at first the converter operation under fault situation has been investigated and will be shown the necessity of fault detection. Then, the performance of the proposed method is verified by assuming the fault in a specific time.

Fig. 4 illustrates the output voltage and current and the capacitors voltage of the converter with an open-circuit fault in switch T_1 (phase a) at $t = 3.945$s. As shown in Fig. 4, when fault occurs, the pseudo-sinusoidal waveform of the output voltage is destroyed and the current has a non-zero dc value.

When the fault occurs at $t = 3.945$s, the output current is positive. So, the fault in T_1 can influence on normal operation of the converter in switching states V_1, V_3, V_5, and V_7. Thus, the fault can be detected in one of this states.

Fig. 5(a) shows the counter output and "Fault" signal in the fault detection method. Before fault occurrence, because of semiconductor switching, the counter output increases but it doesn't exceed the threshold value and the "Fault" signal is zero. This means that the converter operates normally and false fault detection is avoided. Thus, considering the "time criterion" is necessary. On the other hand, because of the capacitors voltage ripple (according to Fig. 4(c) and (d)), the reference voltage is not always equal to the measured voltage during the normal operation of the converter. So, the "voltage criterion" should be considered, too.

TABLE IV. Converter and Load Parameters

Symbol	Quantity	Value
V	DC-link voltage	6 kV
C_1, C_2	DC-link capacitors	5 mF
C_f	floating capacitor	2 mF
f	fundamental frequency	50 Hz
f_s	switching frequency	2 kHz
m_a	modulation index	0.9
S_o	output power	1 MW
V_o	output line voltage	3.3 kV
PF	load Power Factor	0.8

In this case, as shown in Fig. 5(a), the fault signal is set after 55µs in switching state V_7 which the fault affects the operation of converter after about 5 µs in comparison to fault occurrence time. Fig. 5(b) shows the counters outputs, the detection and localization signal for fault in T_1. Since, in the state V_7, the faults in T_1, T_3, and T_5 have the same effect on the output voltage, the faulty switch cannot be detected in this state and the counter output of the localization method is zero. It takes about 255µs to identify the faulty switch (T_1) in state V_6.

Note that in this method, the fault can be detected in a short time as soon as the fault affects the normal operation of the converter whereas the fault localization time depends on the time of fault occurrence and the faulty switch. However, by using the proposed method, the faulty switch can be detected in a time less than one output cycle in comparison to the impact time of the fault on the normal operation of the converter. Table V provides the fault detection and localization time in comparison to the fault occurrence time (Δt) and their corresponding switching states.

When the fault occurs in T_3 or T_5, the detection time is similar to fault in T_1 but it takes about 5ms to identify the faulty switch in switching state V_3. Since, for a fault in T_3 or T_5, the output voltage is zero in switching state V_6 and the faulty switch is determined in state V_3.

For open circuit fault in T_7, the fault localization with the fault detection occurs in a similar switching state. So, the faulty

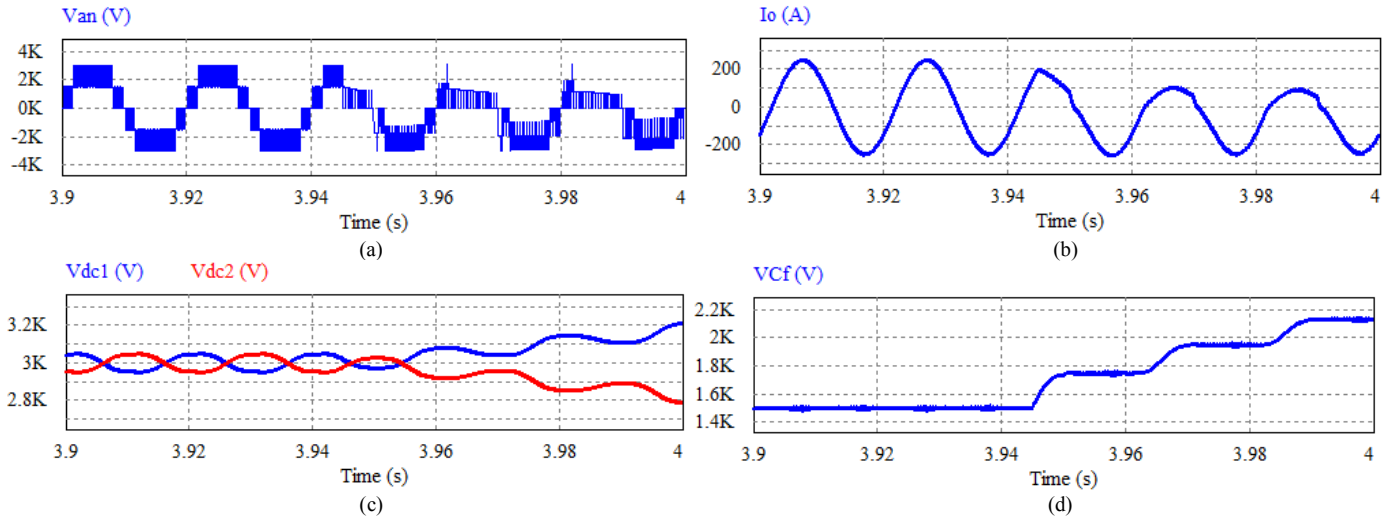

Fig. 4. The simulated waveform under failure operation. (a) The output voltage. (b) The output current. (c) The DC-link capacitors voltages. (d) The floating capacitor voltage.

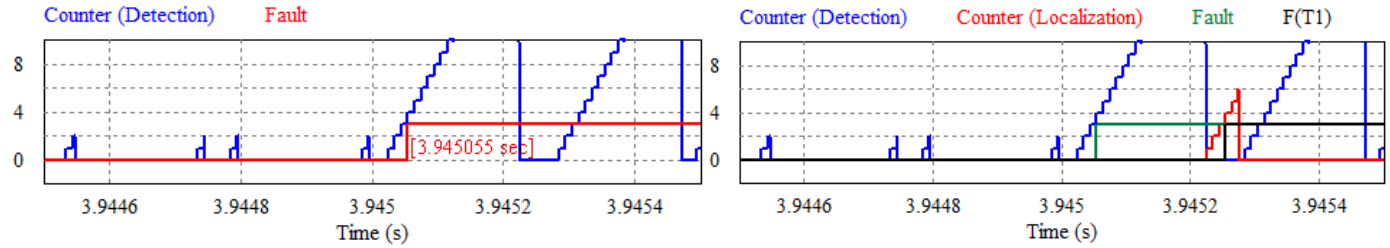

Fig. 5. The simulated waveforms of the proposed method. (a) Counter output with "Fault" signal. (b) The fault detection and localization time

TABLE V. THE DETECTION AND LOCALIZATION TIME FOR FAULT IN ALL SWITCHES

Faulty Switch	Fault Detection		Fault Localization	
	Δt (μs)	State	Δt (μs)	State
T_1	55	V_7	255	V_6
T_2	7195	V_2	7195	V_2
T_3	65	V_7	5055	V_3
T_4	7095	V_1	15055	V_4
T_5	65	V_7	5035	V_3
T_6	7175	V_1	7175	V_2
T_7	505	V_5	505	V_5
T_8	7095	V_1	15035	V_4

switch can be identified very fast once the fault affects the normal operation of the converter. For this simulation, it takes 505μs to detect the fault and identify the faulty switch.

Due to the current direction at the time of fault occurrence, fault in switches T_2, T_4, T_6, and T_8 does not affect the converter and should not care about it as long as the output current is negative. It should be noted that the fault detection is important once fault affects the converter. So, the detection time for fault in these switches is longer than fault in switches T_1, T_3, T_5, and T_7. For example, when fault occurs in T_2 at t = 3.945s, the converter operates normally as long as the current is negative and after about 7ms the fault is detected in switching state V_2. Since in this switching state the fault location can be identified certainly, the fault location and detection occur at the same time. It must be mentioned that in this period of time converter operates normally. The analysis of results for fault in switches T_4, T_6, and T_8 is similar. The Faults in T_4 and T_8 affect the converter after about 7ms due to the current direction and the faults are detected in state V_1 but the faulty switch is identified in state V_4.

For a fault in T_6, the fault localization with fault detection occurs in a similar switching state. Actually, fault in switches T_6 and T_7 can be identified in a very short time with the proposed method as soon as the fault is detectable.

VII. CONCLUSIONS

A new open-circuit fault detection and localization method for 5L-ANPC power switches is proposed. This method detects the fault once the fault affects the normal operation of the converter and the faulty switch is identified less than one output cycle in comparison to the impact time of the fault. The fast detection, high accuracy and simplicity are the main advantages of this method. Since it needs no additional measurement, sensor and processor board, the implementation of this algorithm has no extra cost. Because of considering the practical aspects, this method has ability to implement on a real fault-tolerant converter. The simulation results confirmed the effectiveness and accuracy of the method.

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