CryoCMOS Hardware Technology
A Classical Infrastructure for a Scalable Quantum Computer
Invited Paper

Harald Homulle[1], Stefan Visser[1], Bishnu Patra[1], Giorgio Ferrari[2], Enrico Prati[3], Carmen G. Almudéver[1], Koen Bertels[1], Fabio Sebastiano[1], Edoardo Charbon[1]

[1]QuTech, Delft University of Technology, Delft, The Netherlands

[2]Politecnico di Milano, Milano, Italy, [3]Consiglio Nazionale delle Ricerche, Milano, Italy

{h.a.r.homulle, f.sebastiano, e.charbon}@tudelft.nl

ABSTRACT

We propose a classical infrastructure for a quantum computer implemented in CMOS. The peculiarity of the approach is to operate the classical CMOS circuits and systems at deep-cryogenic temperatures (cryoCMOS), so as to ensure physical proximity to the quantum bits, thus reducing thermal gradients and increasing compactness. CryoCMOS technology leverages the CMOS fabrication infrastructure and exploits the continuous effort of miniaturization that has sustained Moore's Law for over 50 years. Such approach is believed to enable the growth of the number of qubits operating in a fault-tolerant fashion, paving the way to scalable quantum computing machines.

Keywords

CryoCMOS, cryogenics, quantum computation, qubit, error-correcting loop, (de)coherence, fault-tolerant computing, quantum micro-architecture.

1. INTRODUCTION

In a conventional computer, information is carried by classical bits, which can take only two states: '1' and '0'. In a quantum computer, information is carried by quantum bits (qubits), exploiting two fundamental phenomena of quantum mechanics: superposition and entanglement [1]. Qubits are implemented in several different technologies, based on trapped ions, electron/hole spin in semiconductors, superconducting circuits, and nitrogen-vacancies in diamond lattices, to name a few [2]-[13]. Most qubit implementations require cooling at deep-cryogenic temperatures (<<1 K) to extend qubit coherence time, which nonetheless is usually limited to few nanoseconds or few microseconds. Such short coherence timescale prompts the need for a classical error-correcting feedback loop to lengthen coherence times at least for the duration of the processing required by the quantum algorithm. A feedback loop of this kind must be capable of detecting any error in the state of each qubit and controlling such state based on a (localized) decision aimed at correcting it. To be effective, error-correcting loops need to perform a complete correction cycle (Figure 1) faster than the qubit decoherence time.

The process of reading a qubit requires a certain signal-to-noise ratio (SNR) and it should not interfere with proper qubit operation, whereas, to support scalable systems, error-correcting loops should be physically small and compatible with massively parallel operation. To promote scalability, it is likely that error-correcting loops will, in the future, be implemented in micro-architectures supported by a hardware infrastructure that operates and is dynamically reconfigured at cryogenic temperatures without any need for warming up the system to room temperature. Another advantage will be the increased proximity of classical infrastructure to qubits, thus avoiding the drawbacks of wiring the cryogenic quantum processor to room temperature instruments, including excessive thermal loading, increased interference, and lack of compactness.

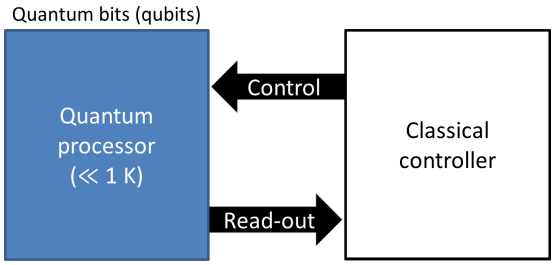


Figure 1. Quantum-classical interface.

Several technologies exist that could support logic circuits at deep-cryogenic temperatures: GaAs high electron mobility transistors (HEMTs) [14], rapid single flux quantum (RSFQ) devices [15],[16], and custom semiconductors [17]-[20]. These technologies are currently expensive and generally not scalable, while CMOS processes can leverage a mature infrastructure that is likely to continue improving for several more decades [21].

To meet the reconfigurability requirement, the obvious choice is a programmable logic device, such as an FPGA fabricated in a deep-submicron (DSM) CMOS process. FPGAs have been used in the past to emulate complex systems, including proposals for quantum FPGAs [22]. When used at deep-cryogenic temperatures, they enable fast prototyping without interruption of experimentation, so as to allow a faster and more effective development of error correction loops.

DSM CMOS circuits have been known to survive at deep-cryogenic temperatures, while maintaining most of their room temperature properties [17]-[20],[23],[24]. While cryogenic FPGAs have been shown to operate at 4K [25],[26], a low cost low power FPGA has been only recently proposed as a general-

purpose quantum controller operating continuously at 4K [25],[27].

The resulting infrastructure is scalable and versatile, efficiently integrated in CMOS and operating at relatively low power. This work shows the design and test of a subset of the components required to implement such a platform for error correction loops. Moreover, extensive characterization of the FPGA performance in cryogenic conditions is presented.

2. ERROR-CORRECTING ELECTRONICS

The architecture of the error correction loop is shown in Figure 2; it comprises multiplexers and demultiplexers, in close proximity to or integrated with the qubits, amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), oscillator(s), down- and up-converting mixers, and general-purpose digital logic.

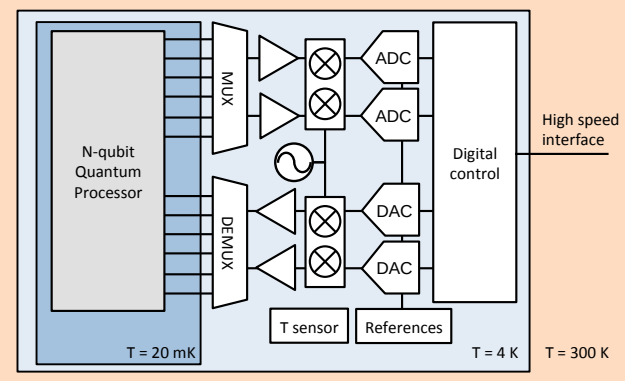


Figure 2. Platform for the infrastructure supporting qubit error correction. The platform comprises discrete components to amplify, mix, (de)multiplex, and digitize/reconstruct the analog signals generated by and directed towards qubits, and an FPGA for digital operations. In the future, a fully monolithic approach will become feasible, thus enabling higher levels of integration and miniaturization.

Operating a semiconductor device at deep-cryogenic temperatures is a challenge, due to freeze-out, non-idealities in transistor I-V characteristics, and increased mismatch [28]. While freeze-out effects at 4 K are less problematic in DSM CMOS technologies due to the high levels of doping, MOS transistors I-V characteristics exhibit a so-called 'kink', which causes elevated current levels at high drain-source voltage. Furthermore, hysteresis in the drain current when sweeping the drain voltage upwards or downwards appears at cryogenic temperatures.

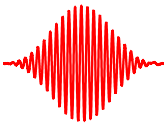
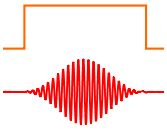
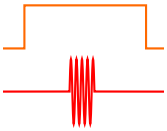
To overcome these limitations, it is preferable to design the error correction loop using digital circuits wherever possible, implemented, for example, in a DSM CMOS application-specific integrated circuit (ASIC) or an FPGA. Nonetheless, the interface with qubits is generally analog, and thus an analog frontend with low noise, moderate amplification, and matched impedance is generally used. A/D converters (ADCs) interface the analog signals generated in the frontend to ready them for processing in the digital backend. Although the redesign of fast analog circuits adjusted to cryogenic conditions cannot be completely avoided, a digitally assisted analog design [29] may be used to perform a partial compensation of the non-idealities in the analog blocks of Figure 2, in the digital domain.

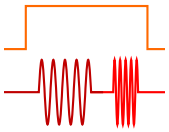
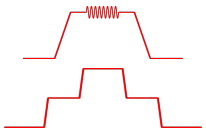
The acquired data is used to decide whether an error has occurred in the quantum processor and to identify its location. When errors occur, the controller synthesizes the appropriate correction feedback that comes in form of specific waveforms, which are generally applied to the qubit via the frontend with possible amplification. To avoid further unnecessary signal conversions, and thus maximizing SNR and/or signal integrity, control signals may be generated directly by the FPGA, whenever possible, or by D/A converters (DACs). Although DACs can be integrated in the FPGA, they will eventually be integrated in ASICs to maximize performance.

3. THE FRONTEND

The frontend has the task of interfacing the classical electronics with the qubits, so as to measure their state and to apply the appropriate analog voltages or currents to change their state. It usually comprises a low-noise wideband amplifier followed by an ADC for the measurement phase, and a DAC and/or a RF modulator to control the phase.

Table 1. Electrical signals applied to various qubits for controlling their state.

Qubit technology	Single qubit gate	
	Envelope/Mod.	Freq./width
Superconducting flux [10][11]	Gaussian/PAM 	7-9 GHz 8 ns
Superconducting flux [12][13]	Gaussian/PAM 	4-6 GHz 10-40 ns
Superconducting flux [14][30]	Gaussian/PAM 	5-8 GHz 16-40 ns
Superconducting flux [31]	Gaussian + DC pulses 	4-5 GHz 15-30 ns DC pulse: 0-200 ns
Spin [2][3][32]	Square + DC pulses 	12.9 GHz 70-1200 ns DC pulse: 1-4 ms
Electron/nuclear spin in Si [33][34][35]	Square+DC pulses	39-49 GHz (electrons) 14-75 MHz (nuclei) 0-30 µs

		
Spin 0[36]	Square + DC pulses 	10–12 GHz 0.1-20 ns

The measurement of the state of the qubit can be performed by measuring the amplitude and/or phase of either the transmission coefficient between two ports of the quantum processor electrical interface or the reflection coefficient at one port. This is accomplished by generating a tone at the appropriate frequency (from hundreds of MHz to tens of GHz) and reading out the modulated transmitted or reflected tone.

In spin qubits, one generally measures the impedance variation of a quantum-point contact (QPC) or a quantum dot (QD). This can be done by applying a DC voltage bias to the QPC/QD and acquiring the resulting rectangular current pulse. Alternatively, the impedance can be measured by RF reflectometry, which involves sending a RF carrier with typical frequencies of a few hundred MHz to the QPC/QD and measuring the variation in amplitude/phase of the reflection coefficient.

The control phase generally involves RF signals modulated in a specific way, depending on the type of qubit and the desired control operation. As an example, Table 1 lists the signals required to perform specific operations on a single qubit, depending on the technology used for the qubit. In current implementations, one generally uses high frequency carriers with Gaussian or rectangular envelope and duration ranging from few nanoseconds to few milliseconds. The carrier phase must be set to a fixed value and/or precisely modulated, depending on the specific operation to be performed.

Superconducting qubits typically require a carrier frequency ranging from 4 to 9 GHz, while spin qubits may require up to 49 GHz (for controlling electron spins) and only 14 MHz (for controlling nucleus spin). In addition, quasi-DC voltages and/or currents (not shown in the table) must be biased at the appropriate DC level in order to tune the qubit to the proper operating region and to overcome spread in the fabrication process. Rectangular multi-level pulses with fast edges must be applied to such quasi-DC lines to temporarily move the qubit energy levels and perform single or multi-qubit operations.

4. THE BACKEND

Most ASICs and FPGAs are designed to operate at room temperature, as it is not trivial to achieve a fully functional circuit at deep-cryogenic temperatures. In addition, power dissipation becomes a serious issue in these regimes, due to the limitations of today's refrigeration technology. Thus, special care must be taken in designing custom integrated circuits and firmware for the FPGA.

For these reasons, we have designed a platform to safely and effectively operate an Artix-7 FPGA at 4.2 K [27]. Figure 3 shows the front- and backside of the PCB. The most critical challenge is the operating condition and the corresponding behavior of the FPGA. Especially for high performance circuits, such as time-to-digital converters (TDCs) and ADCs, the FPGA behavior has to be well understood. Therefore, we constructed an *ad hoc* printed circuit board (PCB) hosting robust passive components and connectors that can reliably survive several cooling cycles without performance degradation. In our design, we used a minimal number of components, of which the FPGA is the sole active component on the board.

Table 2 lists the basic building blocks in the Xilinx 7-Series FPGA families. The components, described in detail in [37], operated correctly at 4.2 K, though exhibiting minor performance degradations that would not hinder their use in most applications required. We implemented numerous versions of oscillators with different performance in terms of jitter and oscillation frequency. The plot of Figure 4 shows the stability in temperature of these oscillators.

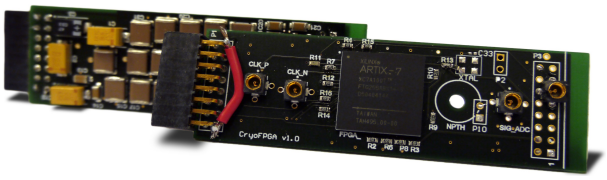


Figure 3. FPGA implementation of the backend. The circuit is based on an Artix 7 (XC7A100T- 2FTG256I) device.

Table 2. Components created within the FPGA and tested at 4.2K. For an explanation of a specific component, see [37].

Module	Chk.	Functional Test	Evolution
IOs	Yes	-	-
LVDS	Yes	-	-
LUTs	Yes	LUTs configured as a ring oscillator (100 MHz / 11.8 ps at RT)	Frequency change: <+5% Jitter change: <+15%
CARRY4	Yes	Carrychains configured as an oscillator (100 MHz / 11.5 ps at RT)	Frequency change: <+2% Jitter change: <+3%
BRAM	Yes	Transfer of 8kB (write & read)	No corruption over 80kB
MMCM	Yes	100 MHz differential input clock multiplied by 10 and divided by 20 to 50 MHz single-ended output (12.2 ps)	Jitter change: -20%
PLL	Yes	100 MHz differential input clock multiplied by 10 and divided by 20 to 50MHz single-ended output (11.4 ps)	Jitter change: -20%
IDELAYE2	Yes	IDELAYE2 configured as a tunable oscillator (13-70 MHz)	Delay change: <±30% Jitter change: <±50%

The delay change of look-up tables and carrychains was measured to be less than 5%. While this is negligible in most applications, the change in logic speed is significant for the performance of ADCs and TDCs implanted in an FPGA. Therefore the main structure of those two circuits must be designed with extra-care to minimize the sensitivity of the components from PVT variations or to calibrate for this speed change.

The operating voltage range of the FPGA changes significantly in temperature; the range is wider at room temperature (0.85V–1.1V) than the specified range (0.95V–1.05V). At low temperatures, it reduces significantly on both ends (0.92V–1.02V).

Table 3. Idle FPGA power dissipation as a function of temperature. Bias voltages for VCC_INT, VCC_AUX and VCC_O [37] are 1 V, 1.8 V and 2.5 V, respectively.

Temperature [K]	VCC_INT [mA]	VCC_AUX [mA]	VCC_O [mA]	Power [mW]
300	24	26	5	83
40	19	69	4	153
4	20	110	4	228

Table 4. TDC performance at deep-cryogenic temperature.

Temperature [K]	Sampling rate [MHz]	LSB [ps]	DNL [LSB]	INL [LSB]	Jitter [LSB]
300	400	20.1	[-1;4.6]	[-2.6;3.3]	0.9
4	400	20	[-2.6;3.3]	[-3.9;2.3]	1.6

Table 5. ADC performance at deep-cryogenic temperatures. The input range was 0.9 V to 1.6V.

Temperature [K]	Sampling rate [MHz]	ENOB [bits]	DNL [LSB]	INL [LSB]
300	1200	6.0	[-0.75;1.04]	[-0.36;0.52]
15	1200	5.0	[-0.85;1.04]	[-0.68;0.77]

The power dissipation of the FPGA was also characterized to verify its suitability in the overall platform. Results shown in Table 3 demonstrate a contained power dissipation that can easily be absorbed by today's refrigerators. However, with the increase of channels, larger FPGAs will be needed and this will increase the overall power dissipation. Given the large overhead of these devices, it is advantageous to maximize the number of channels handled by the FPGA, as scalability will be achieved using extensive sharing schemes.

One of the strengths of digital circuits is the resilience to noise, while Moore's Law has enabled CMOS circuits to 'catch up' in speed to most technologies emerged in the last 50 years. Thanks to the exceptional performance of the components making up the FPGA, TDCs implemented on FPGA typically achieve high resolution (LSB) and good linearity [38],[39],[40]. Recently, these designs have evolved to guarantee the same or better performance at deep cryogenic temperature [27]. These results are summarized in Table 4. Non-linearities and jitter are plotted in Figure 5.

Since ADCs are necessary in most embodiments of error correction loops, as they are part of the measurement phase, it is advisable to design an ADC capable of handling one or even multiple channels as outputted by the frontend. While ADCs will be optimized in the coming years to operate at deep-cryogenic temperatures, it is possible now to use the principle of voltage (or current) to time conversion and build FPGA-based ADCs.

In this context, we built one such ADC in an Artix-7 FPGA with a reconfigurable resolution from 6 to 10 bits and a reconfigurable sample rate from 200 to 2400 MS/s. The ADC is based on the ramp-compare architecture, whereas the reference ramp is generated by the charging and discharging of a parasitic capacitance through an external resistor; the comparator is an LVDS gate [41]. The principle of the conversion is shown in Figure 6, whereas the plot shows the crossing of the input signal with the rising and falling reference ramp signals that are precisely timed by a TDC to derive the conversion codes.

Recently, the design was modified to achieve a 10x sampling rate increase by means of parallelism and extensive calibration [42],[43]. The performance of the ADC from room to deep-cryogenic temperatures is summarized in Table 5.

The FPGAs internal temperature diode was characterized against a precise external reference (Lake Shore Cryotronics, DT-670 silicon diode), which is calibrated down to 1.4 K. During the test, the FPGA was switched off completely, to minimize self-heating effects. The FPGA diode was calibrated with a 10 µA current and the voltage stored as a function of the reference temperature (acquired by the reference sensor) as shown in Figure 7.

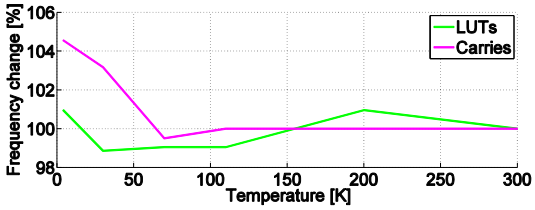


Figure 4. Stability in temperature of oscillators created on the FPGA.

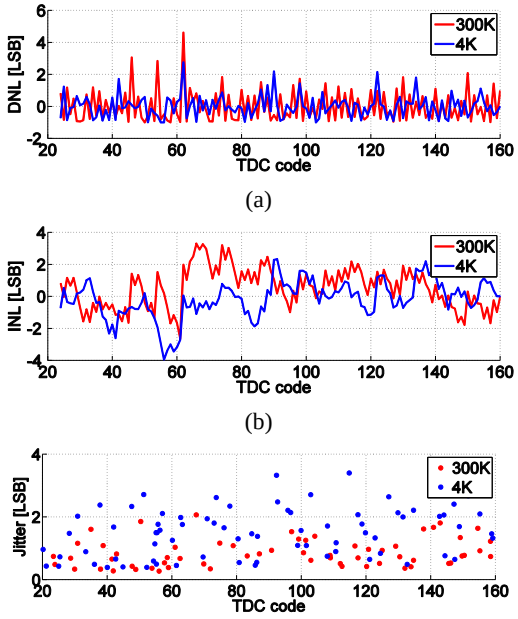


Figure 5. Performance of a programmable TDC operated at 300 K and 4 K: (a) differential nonlinearity; (b) integral nonlinearity obtained from a density test with over 30 million measurements; (c) jitter performance (1σ) captured with a synchronized clock that was shifted through the carrychain. All results were obtained without calibration.

5. MINIATURIZATION PERSPECTIVES

Currently, the interface between quantum devices and classical electronics is quickly evolving and the functionality/specifications are driven by the qubits and their properties. The waveforms of Table 1 may change, even significantly, in the future. Nonetheless, we believe that the basic architecture of Figure 2 is general enough to be sufficient for several generations of computers inspired by quantum principles. The (de)multiplexers in the figure serve the purpose of reducing physical wiring from classical circuits to quantum circuits, so as to reduce thermal loading into sub-Kelvin temperatures. However, other multiplexing techniques, next to time-division multiple access (TDMA), such as frequency-division multiple access (FDMA) and space-division multiple access (SDMA) might be adopted.

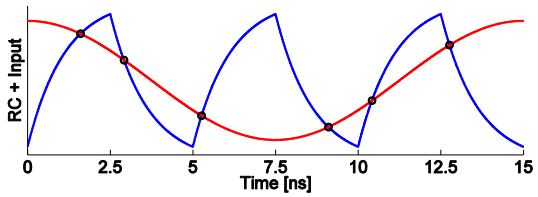


Figure 6. Analog to digital conversion principle of the ramp-compare architecture.

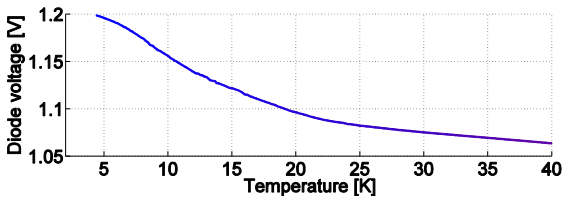


Figure 7. FPGA diode calibration against external reference diode; both diodes were biased at 10 µA. Over 3.000 measurement points were used to create the diode curve. As some hysteresis was present in the measurement data, the curve is averaged between temperature decrease and increase.

Furthermore, it might be possible to reduce the operating temperature of the classical error correction loops to 1 K or below, with the introduction of more advanced CMOS technology nodes, or to increase the temperature of operation of qubits, thus further reducing or eliminating the temperature gradient between the two technologies. Such option could enable chip stacking, whereas wiring could be replaced by low aspect-ratio through-silicon vias (TSVs) or high aspect-ratio through-substrate vias, or yet silicon (or other material) interposers. Figure 8 shows an artist's rendering of a potential construction of this kind. Such solution could be more compact, enabling an improvement in terms of parasitics and power dissipation at the interface and in the individual components of the overall machine.

Further miniaturization could be achieved if a fully monolithic approach were possible. Such approach would imply the creation of qubits in CMOS or modified-CMOS technologies. The work in this domain is currently ongoing.

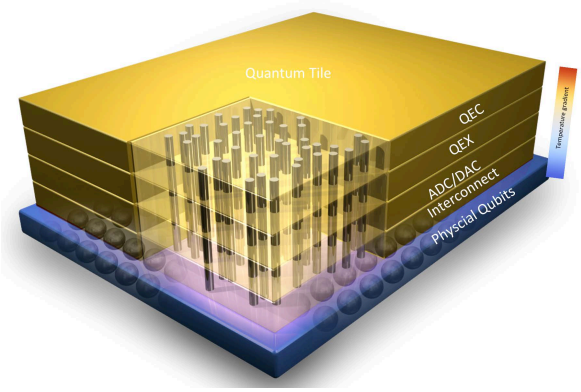


Figure 8. Possible implementation of quantum - classical interface, whereas the qubits will reside in the bottom layer, interconnects and classical error-correcting electronics in intermediate layers, and quantum-execution (QEX) / quantum correction (QEC) in the top layers (Courtesy of IBM).

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