Title: Design and Implementation of Shift-Register using DSCH, Microwind

1. Statement of the Problem:

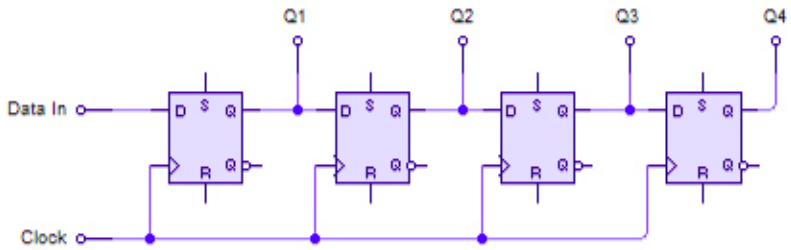
** In this experiment we're trying to design and implement shift-register. Using DSCH transistor level design will be implemented. And using Microwind we'll design the layout of the Shift-register.*
** In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the 'data' input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the 'bit array' stored in it, 'shifting in' the data present at its input and 'shifting out' the last bit in the array, at each transition of the clock input.*

2. Materials:

** Microwind and DSCH*

3. Procedure:

- In this experiment we're designing a Serial In Parallel Out Shift-register. The circuit diagram of the serial in parallel out shift register is as follows.



- We've added a seven segment display to check the out put of the shift-register. Seven segment display connection is as follows.

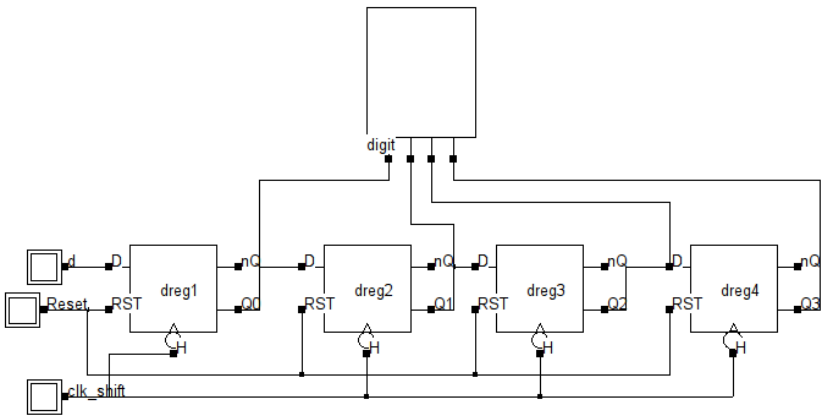
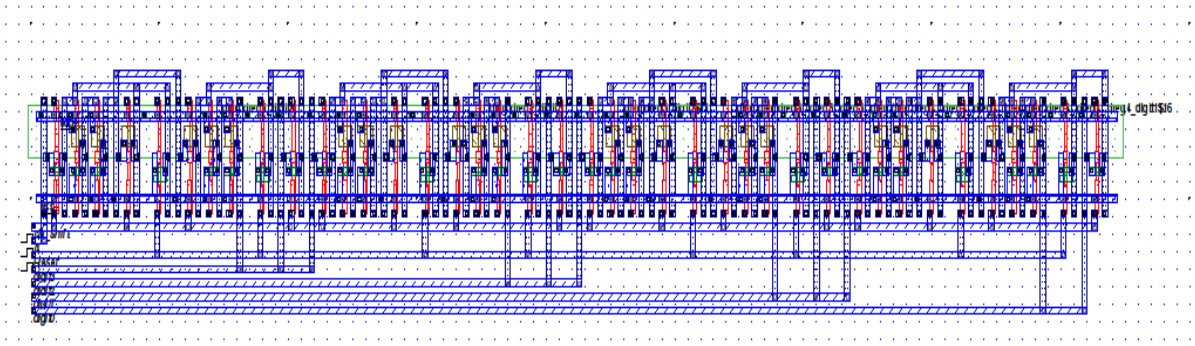


Fig 1: Shift-Register with 7-segment display

- D is the input to the register. On each clock cycle one bit of data goes into the register serially. Reset is used to clear all data and going back to initial state.



- From DSCH software we generate the equivalent verilog file and then compile the verilog file in Microwind to generate the layout diagram as follows.

4. Results (Data):

**In DSCH software we simulate the Shift-Register to verify its output. The output clock diagram is as follows:*