Experiment No: 01

Experiment Name: *Design & Implementation of a Full Adder circuit using Microwind/DSCH*

Statement of the Problem:

In this experiment we're going to implement a binary full adder using DSCH and will generate the layout level design of a full adder. Further in this experiment we'll be designing a 4bit parallel and Carry LookAhead adder using the design of a full adder and also generate the layout level design.

Hypothesis:

According to the basic principle of binary logic we can implement a single bit adder as follows: if A and B are two single bit number then, their sum

Sum = A (xor) B, and

Carry= A (AND) B

using the above principle, we can design a 4bit Adder.

Materials:

- ➢ gate level design software: DSCH
- ➢ layout level design software: Microwind
- ➢ Operating System: Windows/ Linux

Procedure:

Using the basic gates given in DSCH2 and logic design we implement a single bit adder, then using 2 half adder with some extra logic gate we can implement a Full Adder. Using 2 or more full adder we can implement a 4bit or 8bit (or more) parallel adder.

After implementing the adder we use the simulation option of DSCH & Microwind to simulate the output and check if it gives exact output as we've seen in theory.

We can generate the verilog file from DSCH which will be used in Microwind to automatically generate the Layout level design. Which gives us a view how does an adder hardware circuit looks like inside a IC.

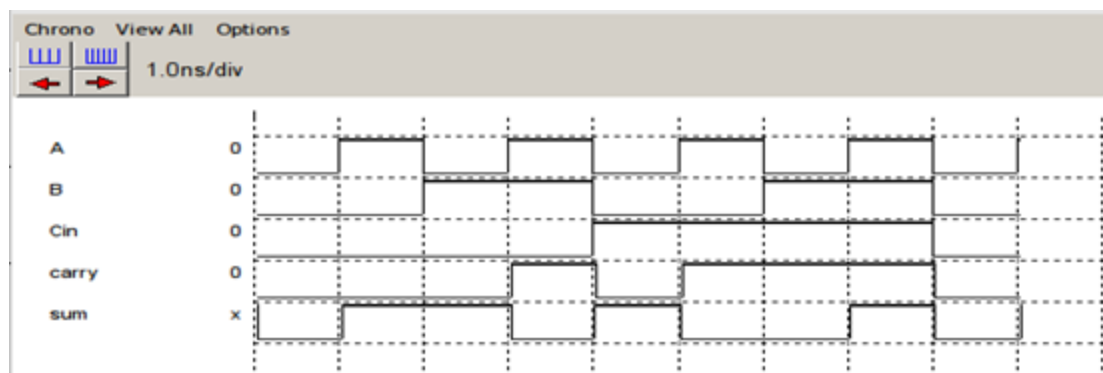*The detailed Design procedure is shown below with proper diagram:*
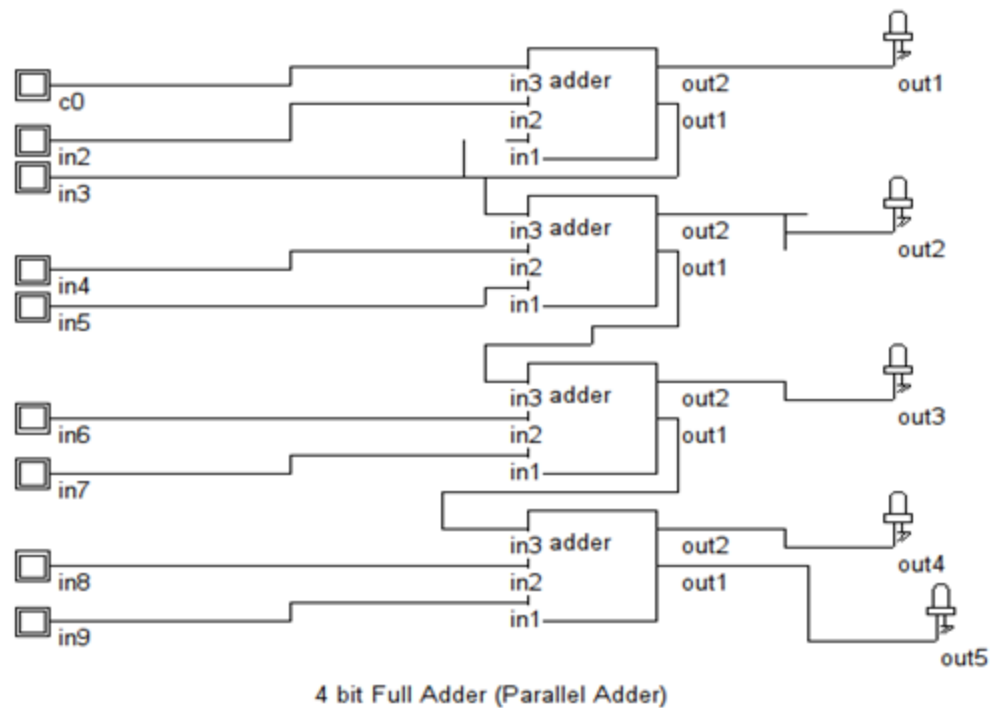
Schematic Diagram of Full Adder:

Single Bit Full Adder
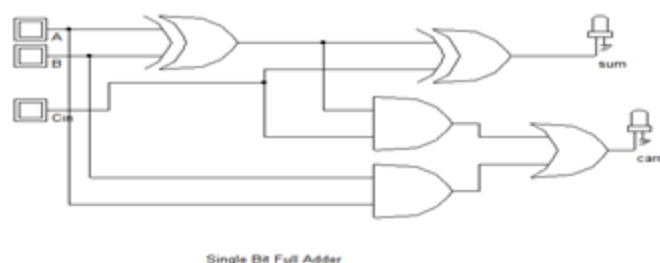
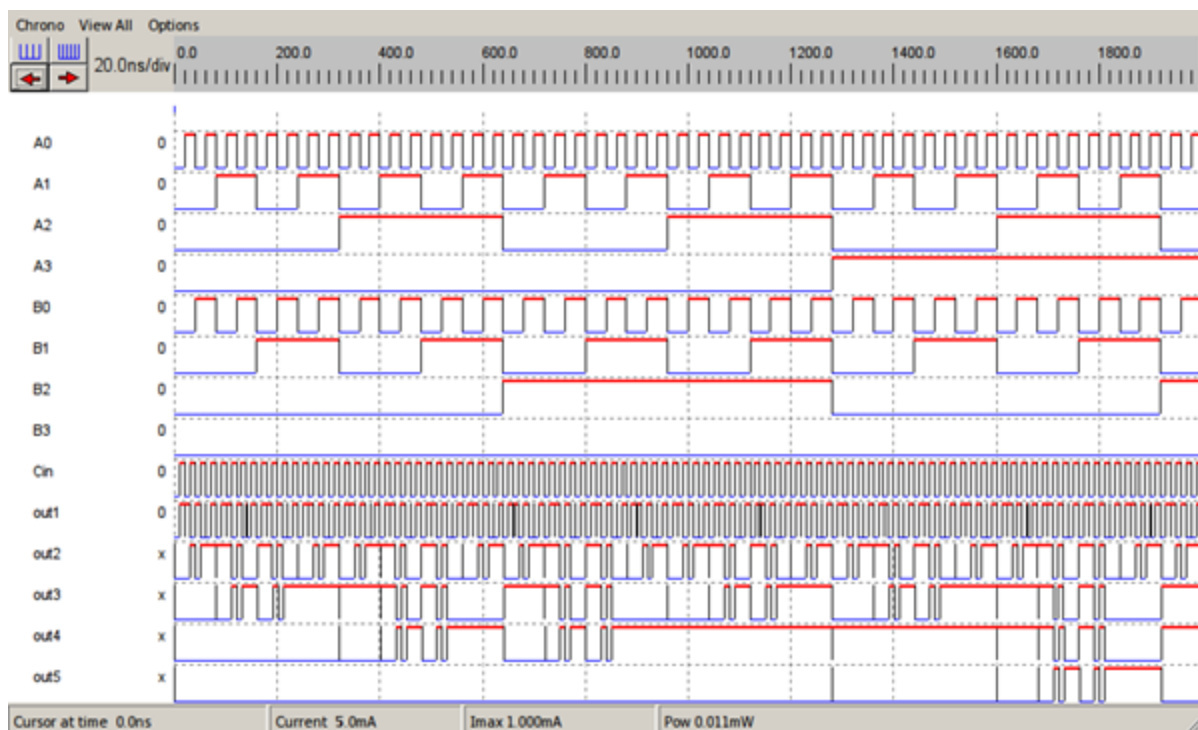➢ Layout Diagram of the above circuit is as follows

Full Adder Layout Diagram
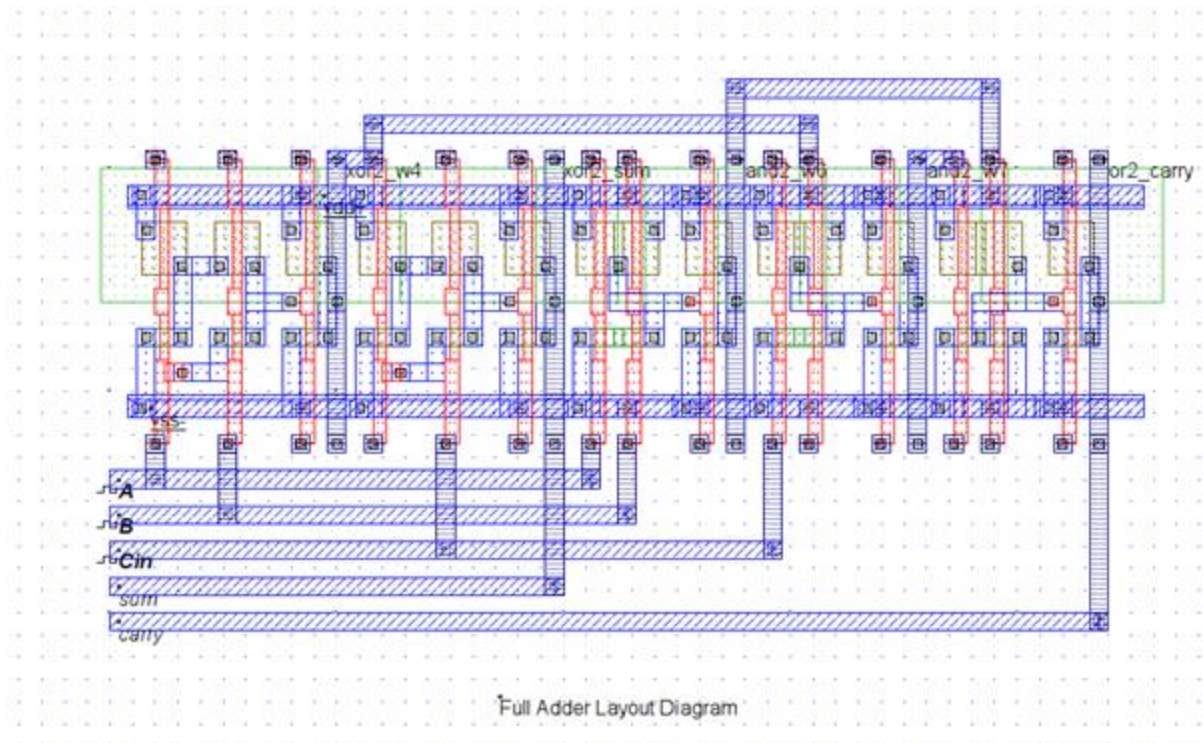
➢ Timing Diagram of the above circuit simulation:

➤ Using the above full Adder we've implemented the parallel adder below

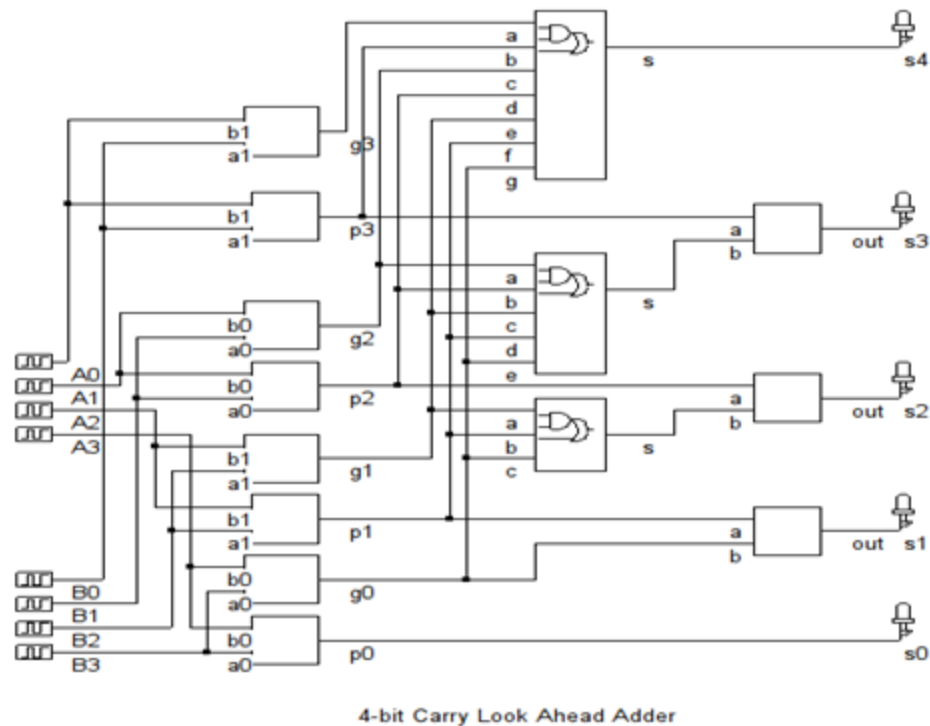4 bit Full Adder (Parallel Adder)

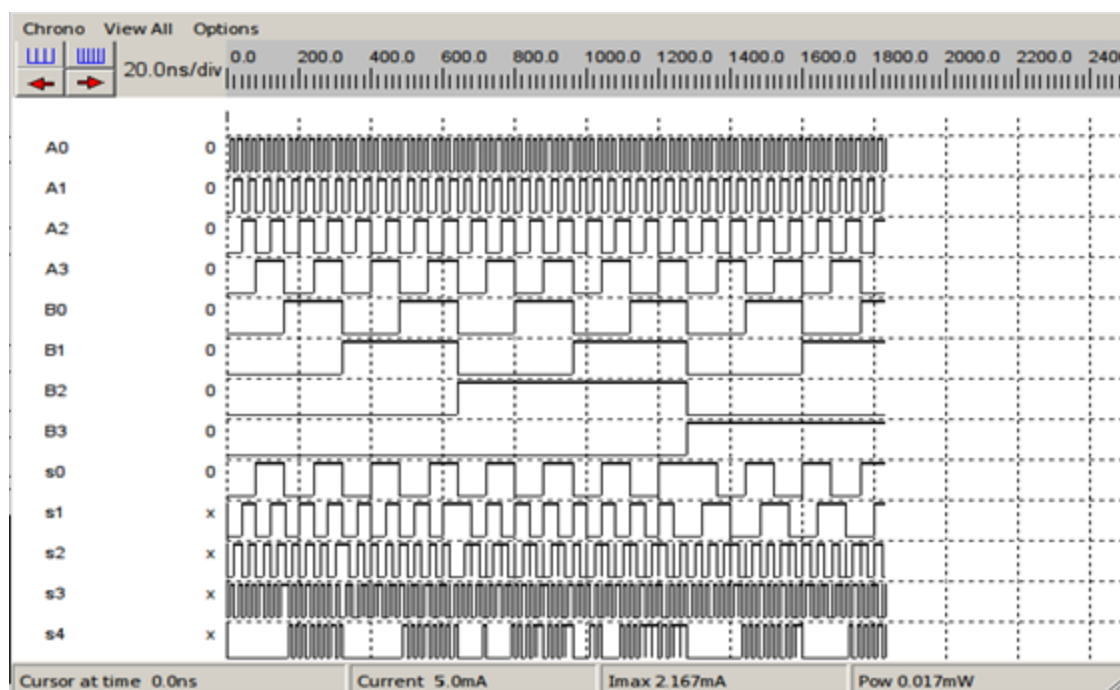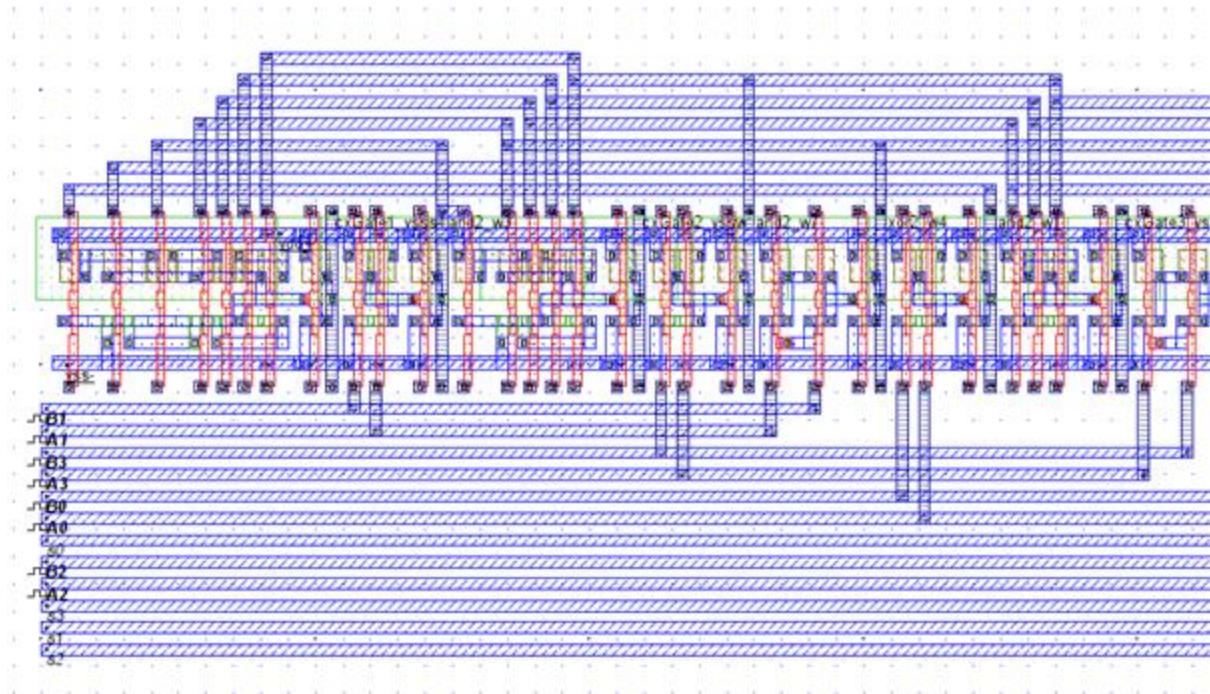Timing Diagram for the above Circuit:

4bit Adder Timing Diagram

➤ Now using the 4bit Parallel Adder and a Carry Look Ahead Unit we can easily design a Carry Look Ahead Adder which is better and faster than typical 4bit parallel adder. The Carry Look Ahead Adder design is given below:

4-bit Carry Look Ahead Adder

➤ Timing Diagram of the above Carry Look Ahead Adder:

> A portion of layout diagram of the above Carry Look Ahead Adder, Since the diagram is very large it is not possible to capture full diagram in one shot.

Results of this experiment is nothing but the timing diagram showing the output pulses of the circuit as shown above.

Conclusions:

There is different type of layout design principle, we've used the default design scheme provided by the DSCH software.