Experiment No: 6

Experiment Name: Design and Implementation of Shift-Register using DSCH, Microwind

Statement of the Problem:

In this experiment we're trying to design and implement shift-register. Using DSCH2 transistor level design will be implemented. And using MICROWIND, we'll design the layout of the Shift-register.

In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the 'data' input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the 'bit array' stored in it, 'shifting in' the data present at its input and 'shifting out' the last bit in the array, at each transition of the clock input.

Objectives:

- ✔ To implement a serial in parallel out (SIPO) shift-register capable of holding and shifting a word of four bits.
- ✔ Simulate the design using two different ways as:
  a) Circuit design and logic verification using DSCH2
  b) Circuit design and logic verification using DSCH2 and Microwind

Materials:

- ➢ *Microwind and DSCH2*

Theory:

Shift register are a type of sequential circuit, mainly for storage of digital data. The SIPO shift register is a group of flip-flop connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. All flip-flops are driven by a common clock therefore all of them are set or reset Simultaneously. The truth table and schematic diagram of SIPO are given below:

Reset	Shift	Data IN	Q0	Q1	Q2	Q3
0	X	X	0	0	0	0
0	0	1	1	0	0	0
0	0	1	1	1	0	0
0	0	1	1	1	1	0
0	0	1	1	1	1	1
0	0	0	0	1	1	1
0	0	0	0	0	1	1
0	0	0	0	0	0	1
0	0	0	0	0	0	0

Table-1: Truth table

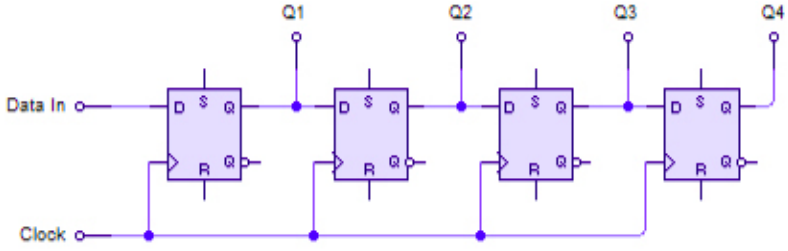


Figure : schematic diagram

Procedure:

(a) Circuit design and logic verification using DSCH2

- Drawing the schematic diagram o DSCH2 design space. Then, click on Simulate → Start simulation.

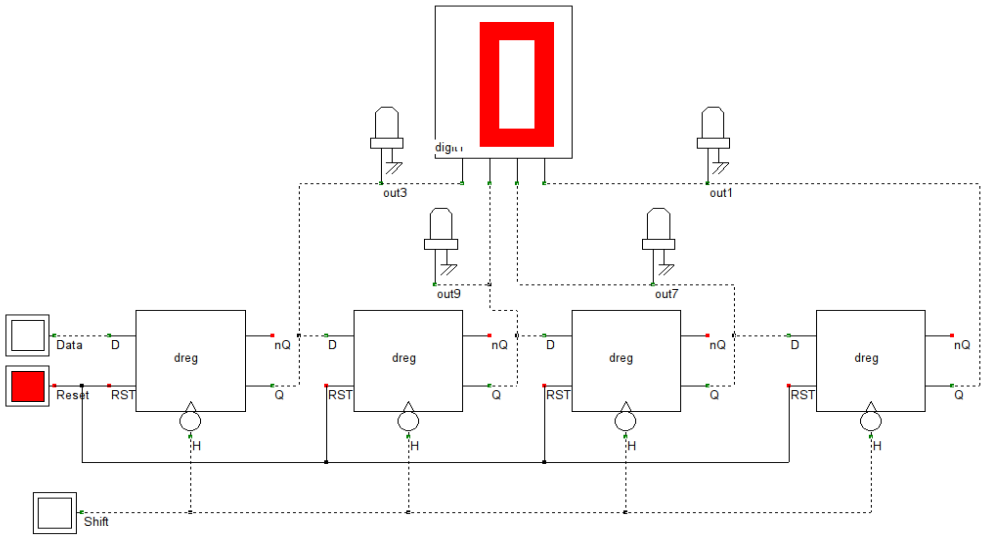
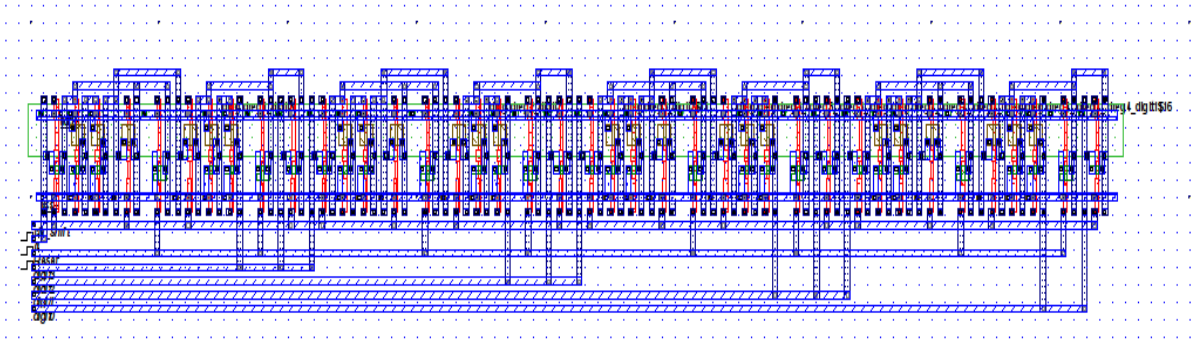


Figure: schematic diagram

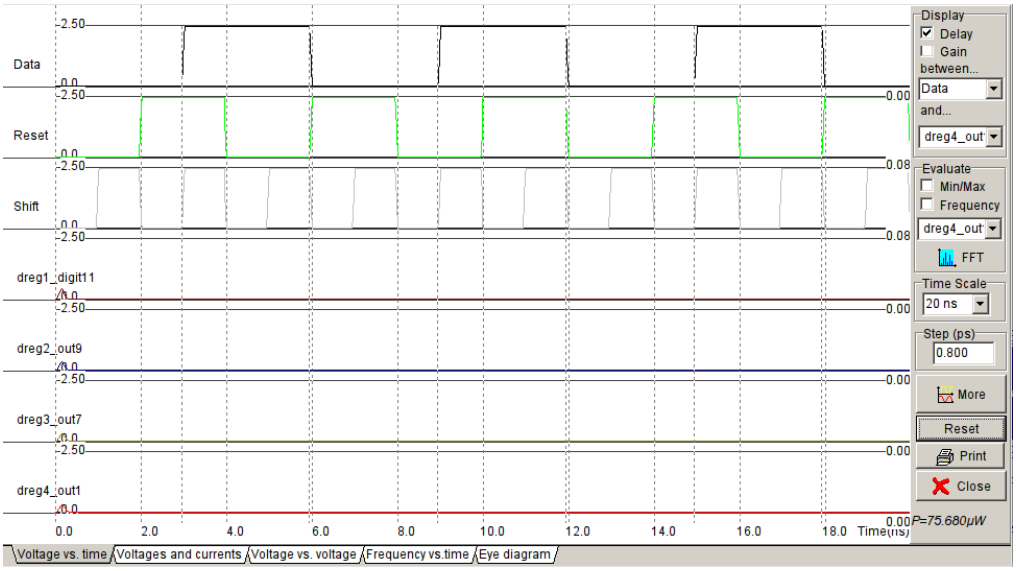
- We've added a seven segment display to check the out put of the shift-register. Seven segment display connection is as follows.

(b) Circuit design and logic verification using DSCH2 and Microwind

- Convert the schematic diagram into verilog file by DSCH2. Then compile the verilog file in Microwind to generate the layout diagram as follows. The Verilog, Hierachy anr Netlist window will appear. This window shows the verilog representation of our (SHIFT register in this example) circuit.



Now simulate the Shift-Register to verify its output. The output clock diagram is as follows:



Result:

The shift-register of serial-in parallel-out is implemented and the truth table is also verified successfully. The required waveform were obtained, observed and noted down using microwind.