Experiment No: 04
Experiment Title: *Observation and Verification of transfer characteristics of CMOS inverter.*

Statement of the Problem:

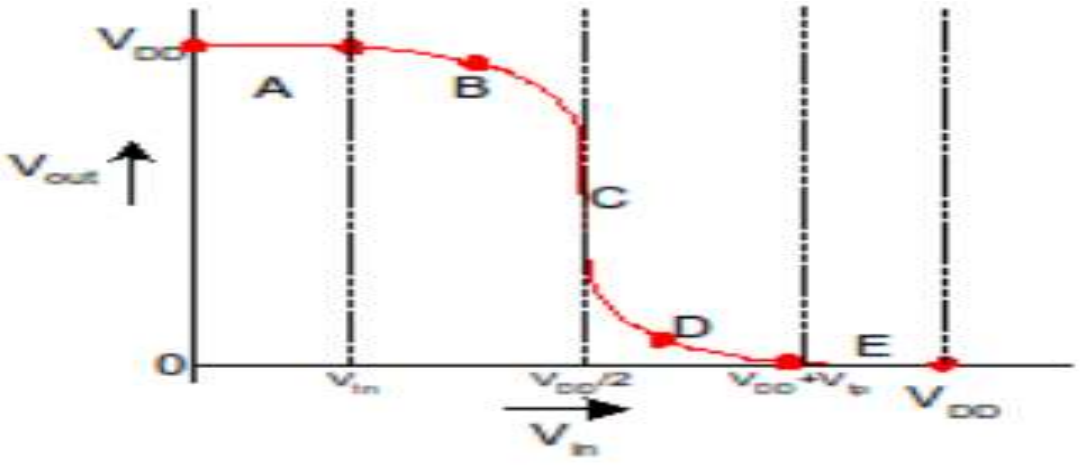
Here we are going to this:

i. We can see the change of the output rate in the graph of voltage vs voltage and the voltage vs time.
ii. Layout design simulation using Microwind.
iii. Here we use inverter to see the output result. Inverter is contained both pMOS and nMOS.
iv. To observe the deviation in results with default layout.

Hypothesis:

Transfer characteristics of CMOS inverter:

It has 5 region, A, B, C, D, E. Transistor operating regions are given below in chart.



For Region A.$0 \leq V_{in} \leq V_{tn}$. NMOS is off, $I_{dsn}= 0$; where pMOS is in linear region. In this circuit $I_{dsn} = -I_{dsp}$. Therefor both current will be zero, since $I_{dsn}= 0$Now $V_{dsp} = V_{DD}-V_{out}$ Or, $0 = V_{DD}-V_{out}$; in linear region $V_{dsp} \approx 0$. Therefor $V_{out} = V_{DD}$.In region B, the nMOS transistor starts to turn ON, pulling the output down. In region C, both transistors are in saturation. Notice that ideal transistors are only in region C for Vin = VDD /2 and that the slope of the transfer curve in this example is – 8 in this region, corresponding to infinite gain. Real transistors have finite output resistances on account of channel length modulation, described in Section 2.4.2, and thus have finite slopes over a broader region over a broader region C. Other 2 region D and E will be like this.

We can measure this change by the Beta ratio

If $\beta_p/\beta_n \neq 1$, switching point will move from $V_{DD}/2$.This is called *skewed* gate.

Other gates: collapse into equivalent inverter

βp=mobility of pMOS =constant=W/L

βn=mobility of nMOS =constant=W/L, Here w=width and L=Length

βp/ βn=constant which is depend on its transfer characteristics is changes.

Materials:

a. Microwind software.
b. Windows/Linux Operating System

Procedure:

Table:

Inverter	pMOS		nMOS		βp/ βn
	Width	Length	Width	Length	
1st	50	1	5	1	0.1
2nd	5	1	5	1	1
3rd	5	1	50	1	10

Schematic diagram and Stick diagram:

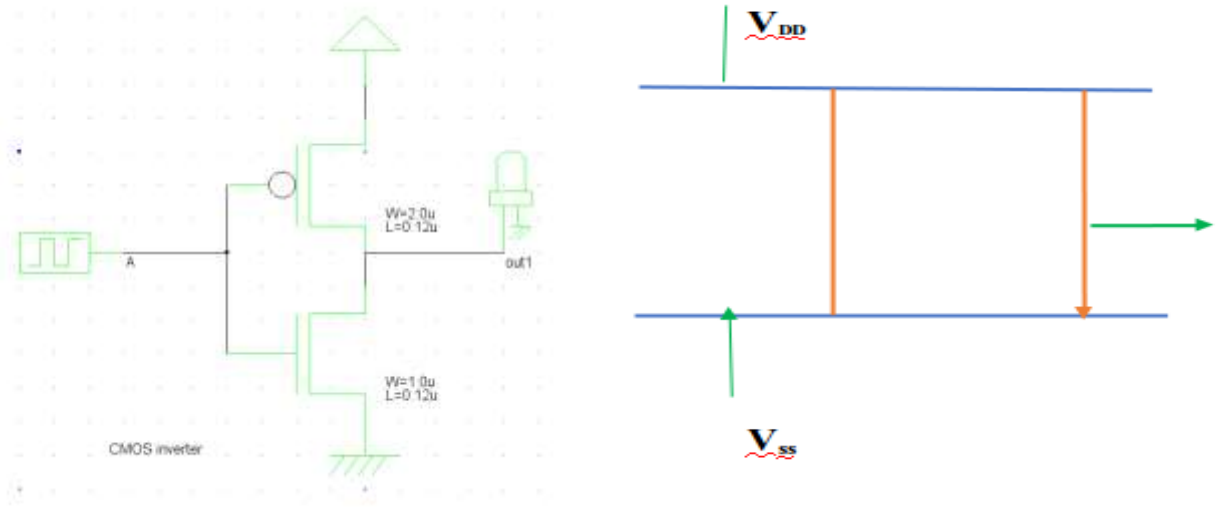


Illustration: Schematic and Stick diagram of CMOS inverter

Now, Open microwind and create a new file, then design the CMOS inveter layout with three pairs of nMOS and pMOS according to the given size in the table. The final figure is given below:

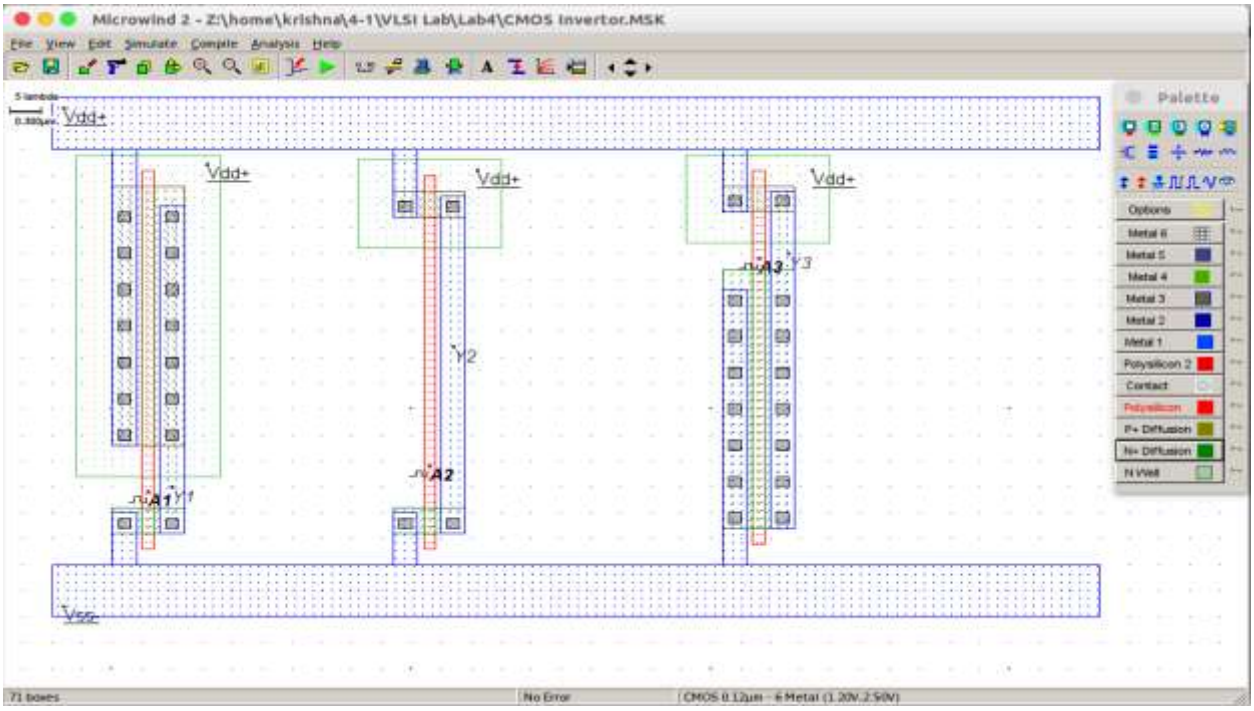


Illustration: layout of CMOS inverter

Now we simulate the circuit to evaluate different characteristics of the Inverter Circuit.

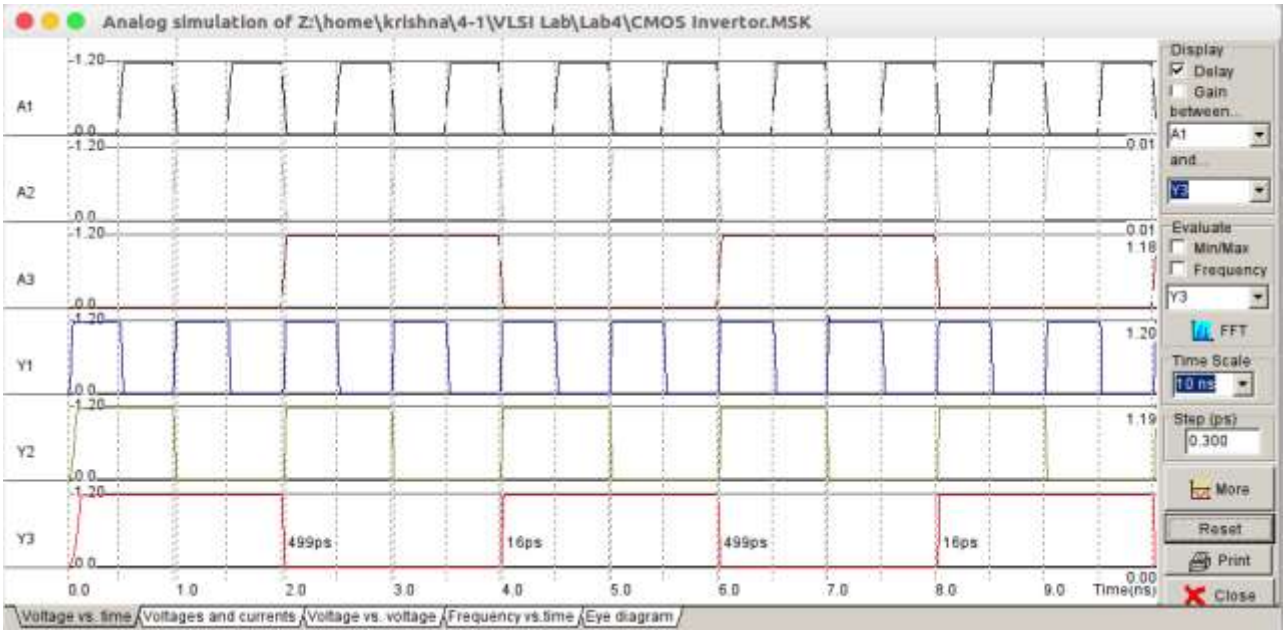


Illustration: Voltage vs Time characteristics Curve of CMOS inverter

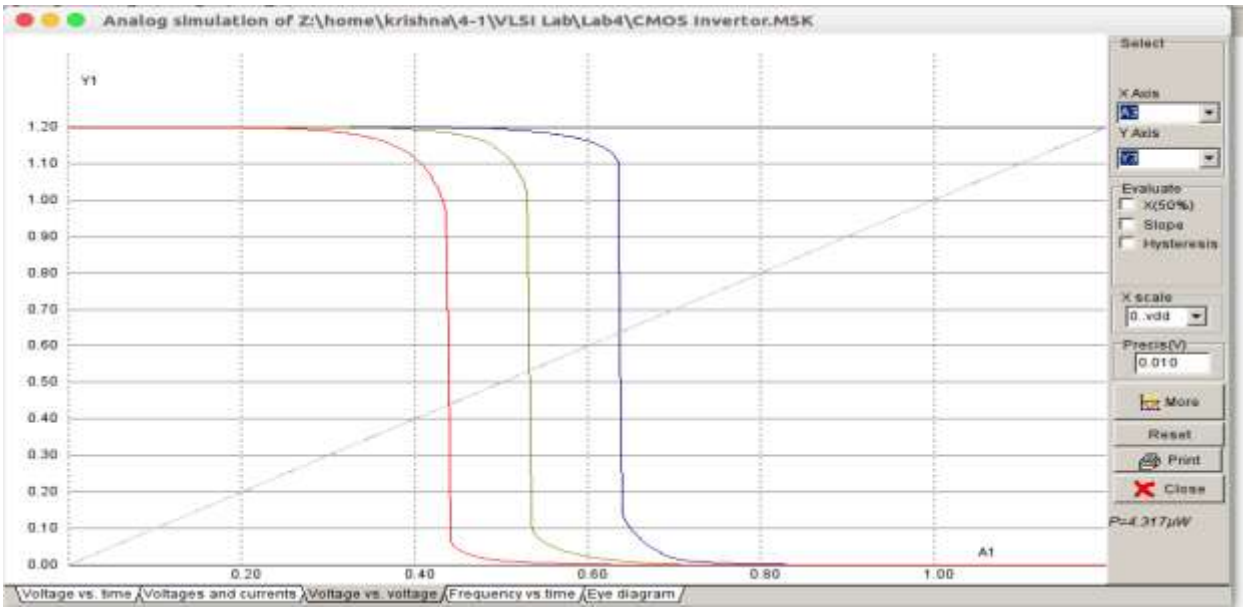


Illustration: Input Voltage vs Output Voltage Characteristics

Conclusion:

The CMOS INVERTER gate is implemented using three pMOS and three nMOS with different ratio. The required waveforms were obtained, observed and noted down using Microwind. And we observe the change of output in the voltage vs time graph and the voltage vs voltage graph .