Experiment No ***: 02***
Experiment Name ***:*** *(a) Implementation and Design of NAND gate.*
(b) Implementation and Design of NOR gate.

(a) Implementation and Design of NAND gate.

Objectives:

- To implement NAND gate
- Circuit design and logic verification using DSCH2
- Circuit design and logic verification using DSCH2 and Micro wind.
- To observe the deviation in results with default layout.

Procedure:

⇨ Circuit design and logic verification using DSCH2

- The truth-table and schematic diagram of NAND gate is given below:

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Figure: Truth-table

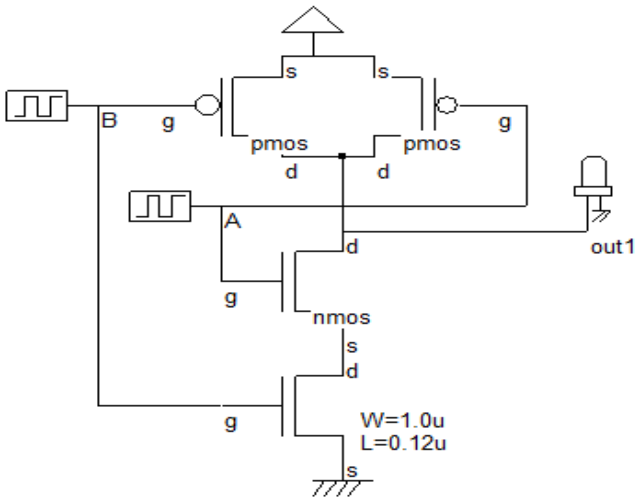
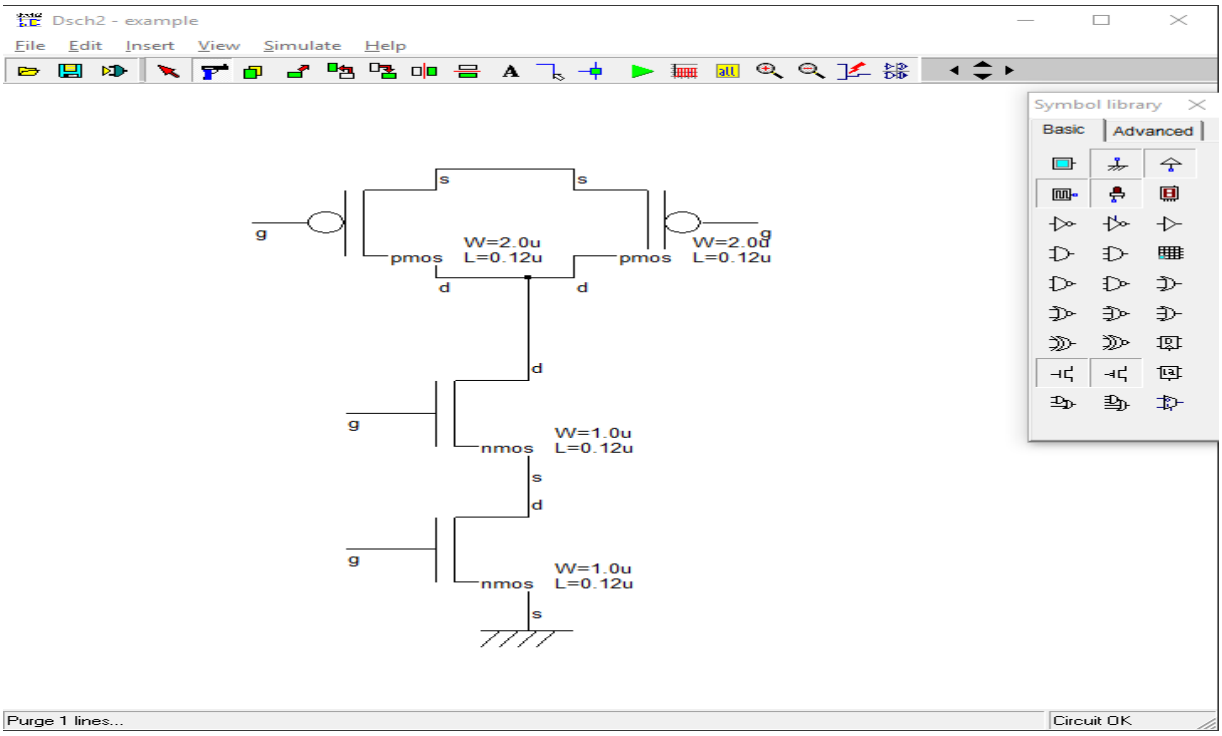
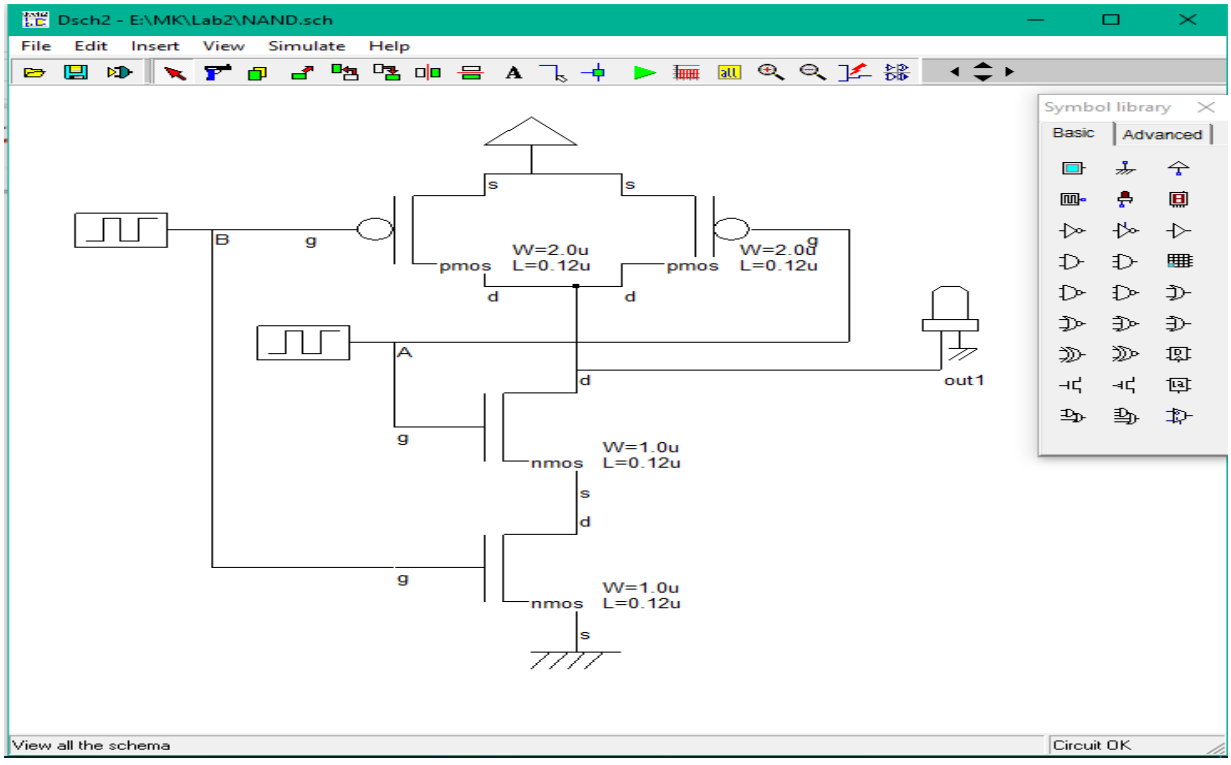


Figure: Schematic Diagram of NAND

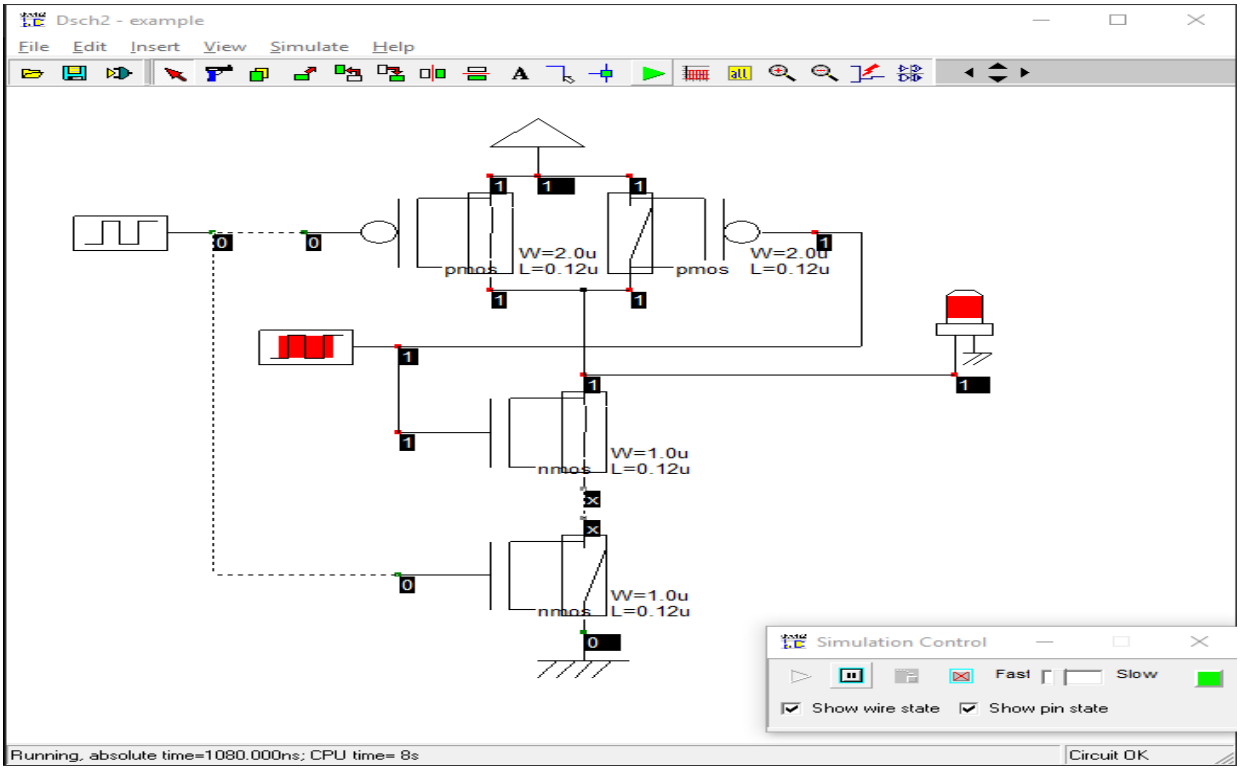
- Open the schematic editor called DSCH2. Instantiate nMOS or pMOS transistor (drag and drop) from the symbol library, place them in the editor window and connect them according to schematic diagram shown below:



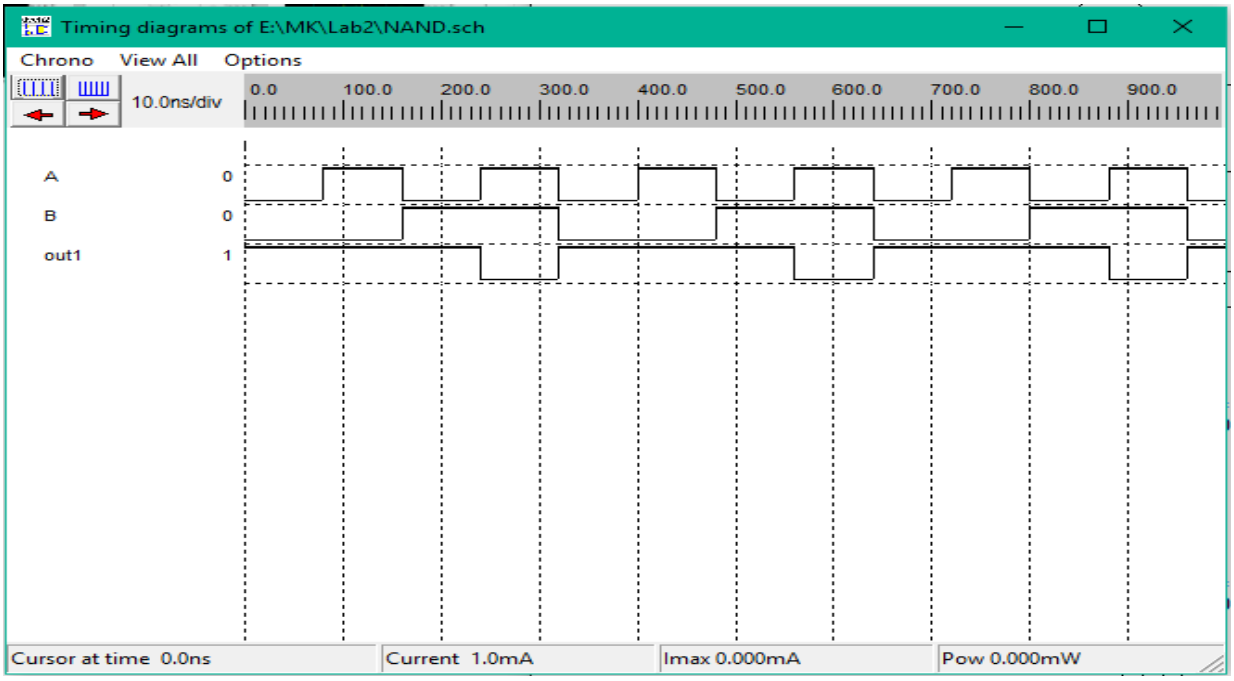
- Connect V_{dd}, G_{nd}, clock as input pulse A, B and output (out) from the symbol library. Figure is shown below:



- At this point, the NAND gate is ready to simulate. Before going to simulation work, check whether any floating line exists in the diagram. For this purpose, click "Check floating line" in the simulation menu. Then start the simulation. The figure is shown below:

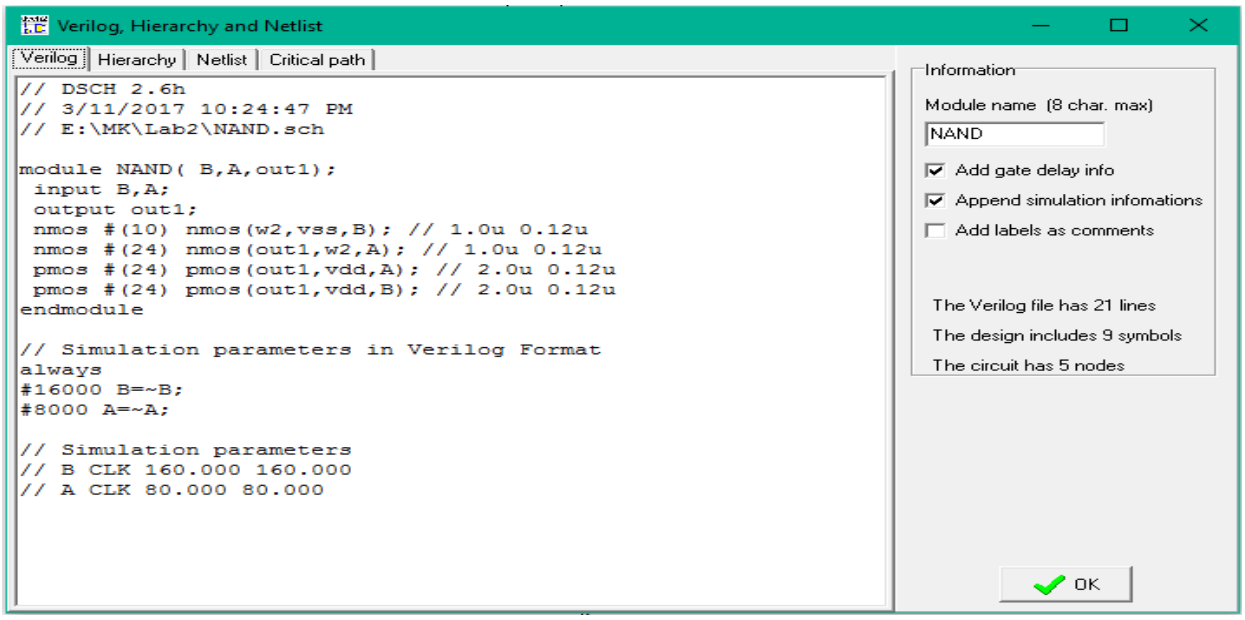


- The timing diagram of inputs and outputs pulses are shown below:

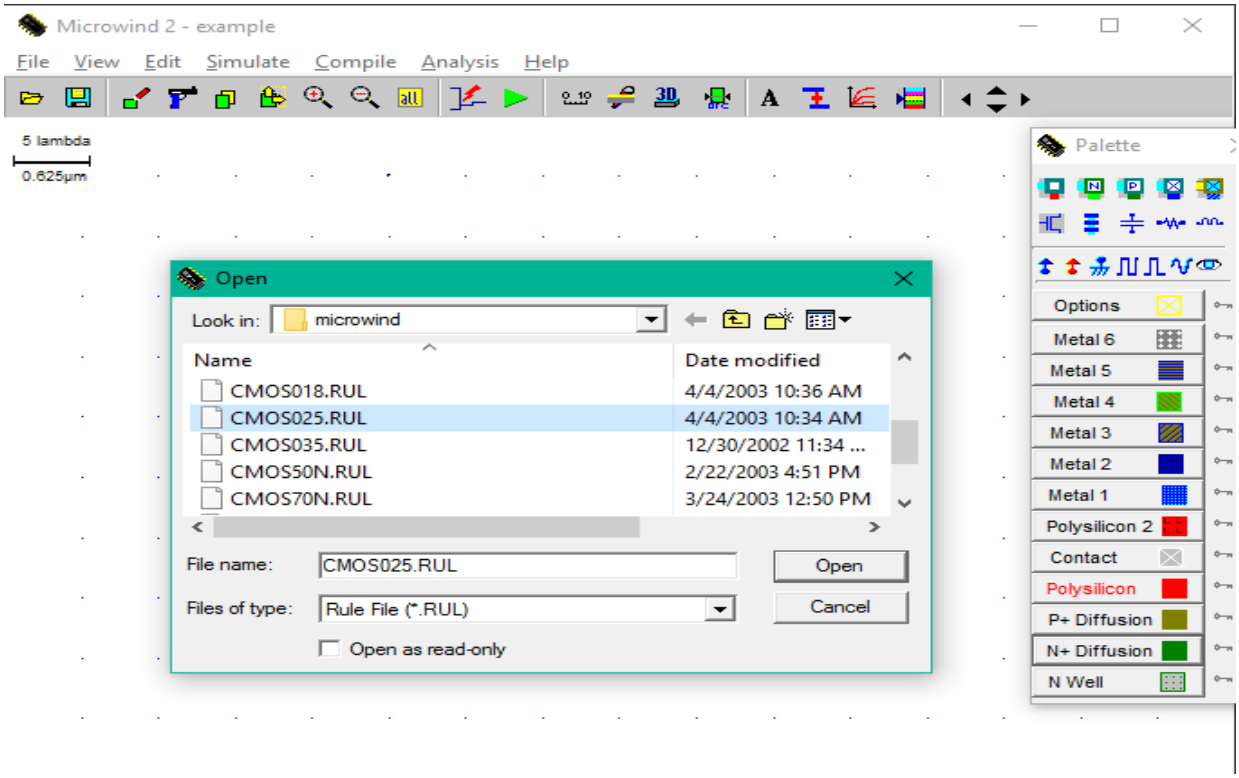


Circuit design and logic verification using DSCH2 and Micro wind.

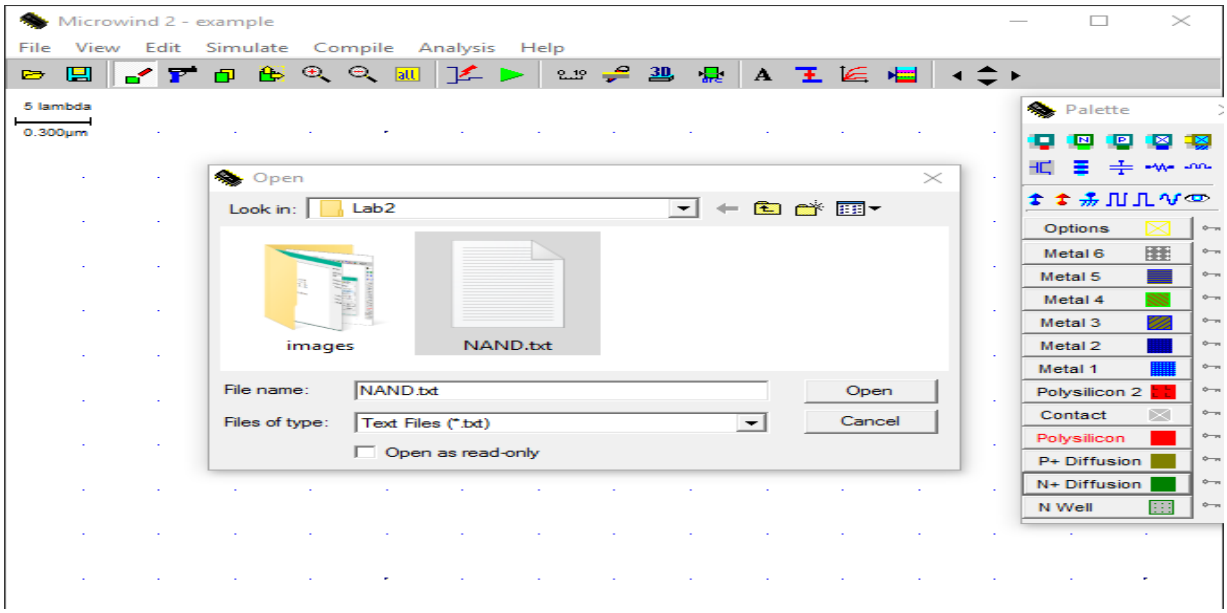
- Firstly, open the schematic in DSCH2 that we created. Convert the schematic into a Verilog representation. Click on File → make Verilog File. The verilog , Hierarchy ans Netlist window will appear shown below:



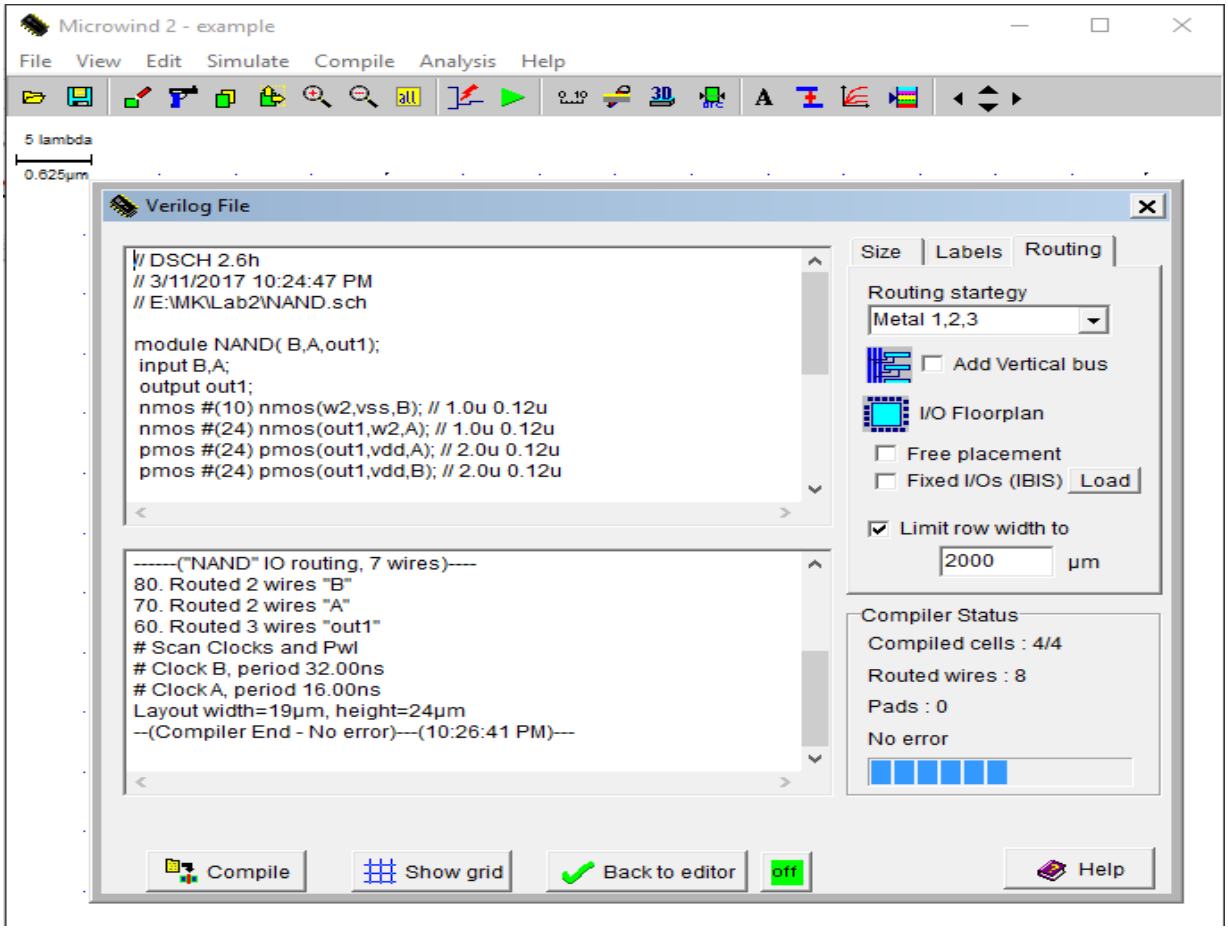
- Now open the layout editor window "Microwind2". Click on File → select Foundary and select cmos025.rul. This will set the layout design in 0.25u technology shown below:



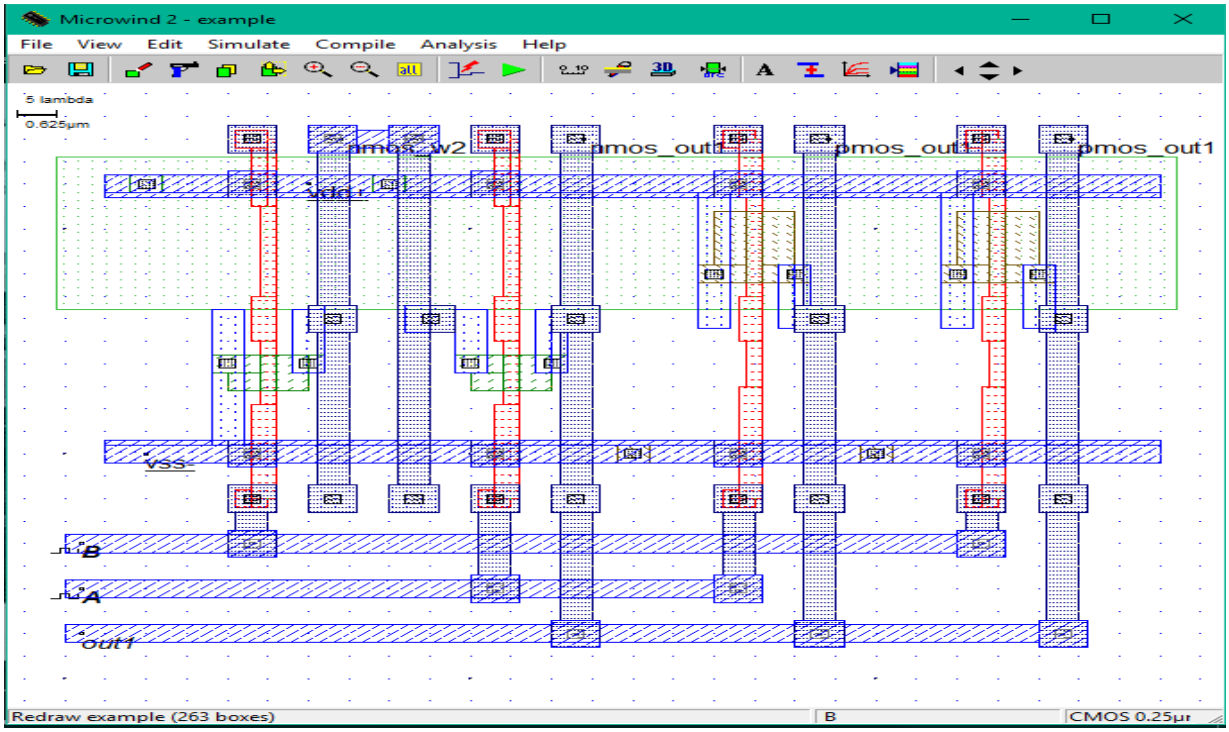
- Click on Compile → Compile Verilog File. A window will appear shown below and select the Verilog file as we saved before. Figure:



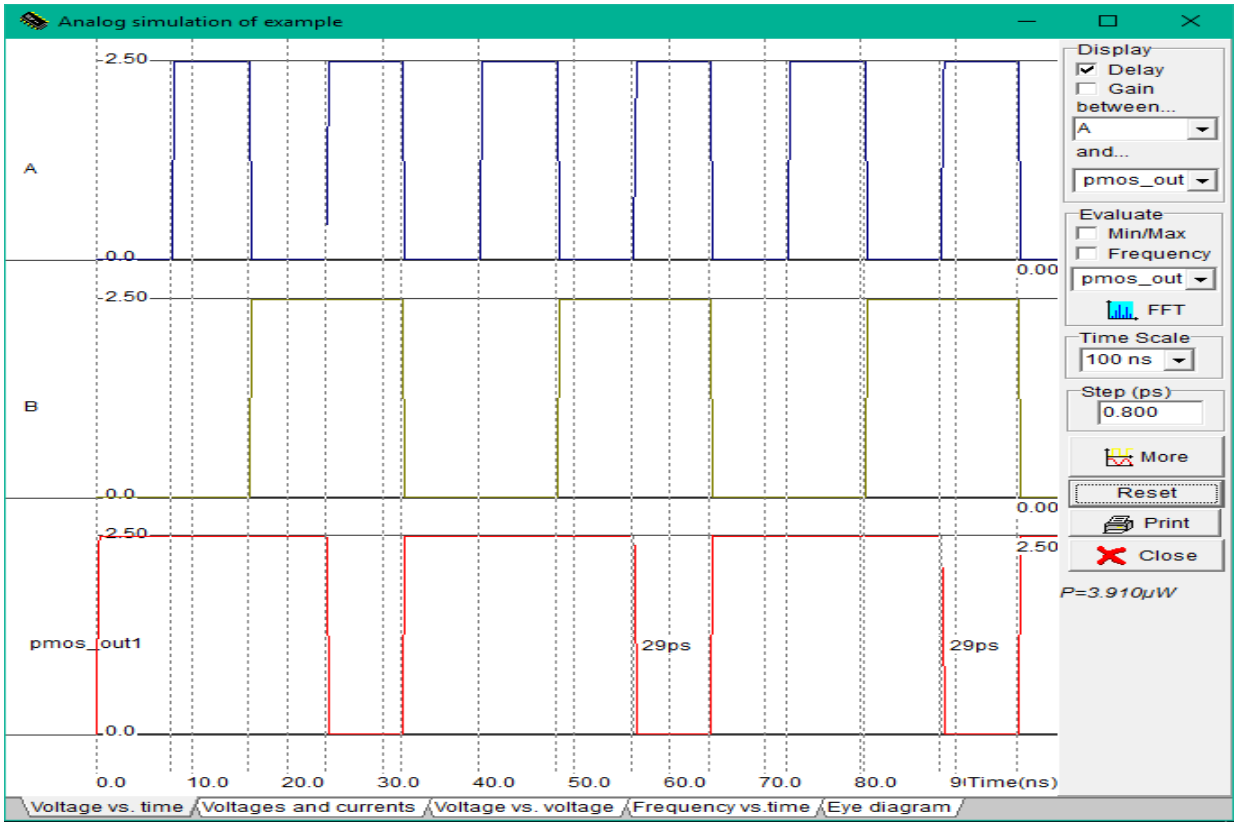
- The Verilog file after opening in microwind2:



- Now, Click on Compile Button. It will compile the verilog file and finally it shows the no error if th code is compiled successfully. Close the window to see the layout. Our design as shown below:



- Click on Simulate → Run Simulation. A simulation window will appear with th inputs and output shown below:



(b) Implementation and Design of NOR gate.

Objectives:

- To implement NOR gate
- Circuit design and logic verification using DSCH2
- Circuit design and logic verification using DSCH2 and Micro wind.
- To observe the deviation in results with default layout.

Procedure:

Circuit design and logic verification using DSCH2

- The truth-table and schematic diagram of NOR gate is given below:

A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Figure: Truth-table

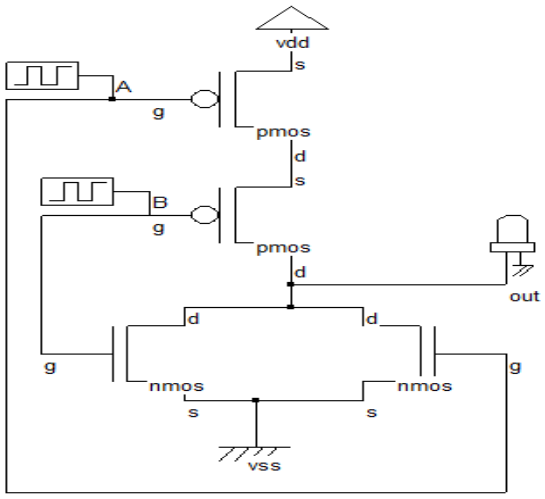
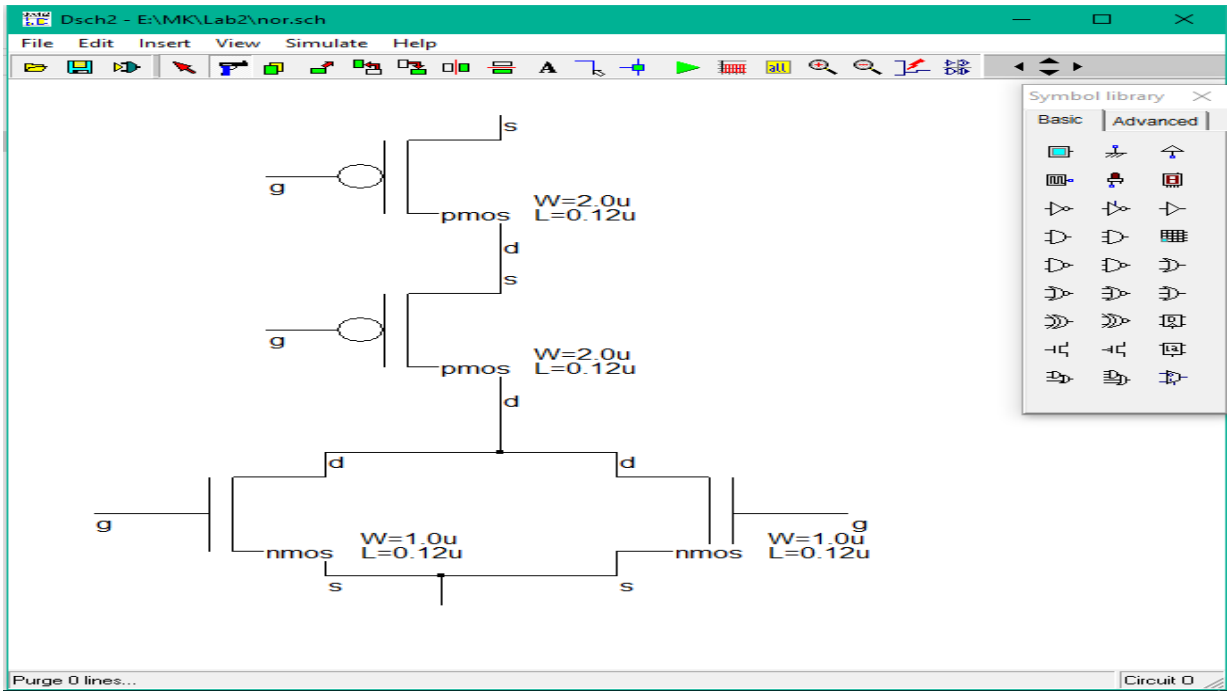
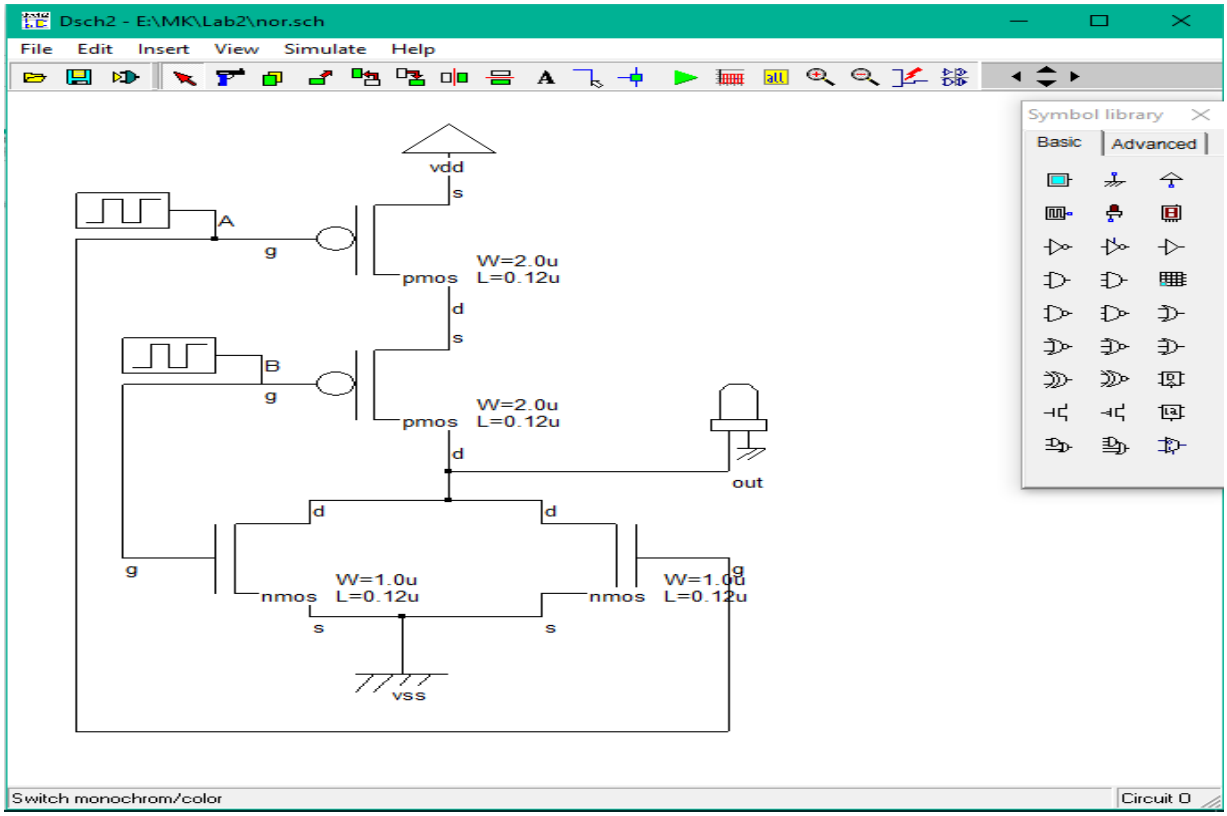


Figure: Schematic Diagram of NOR

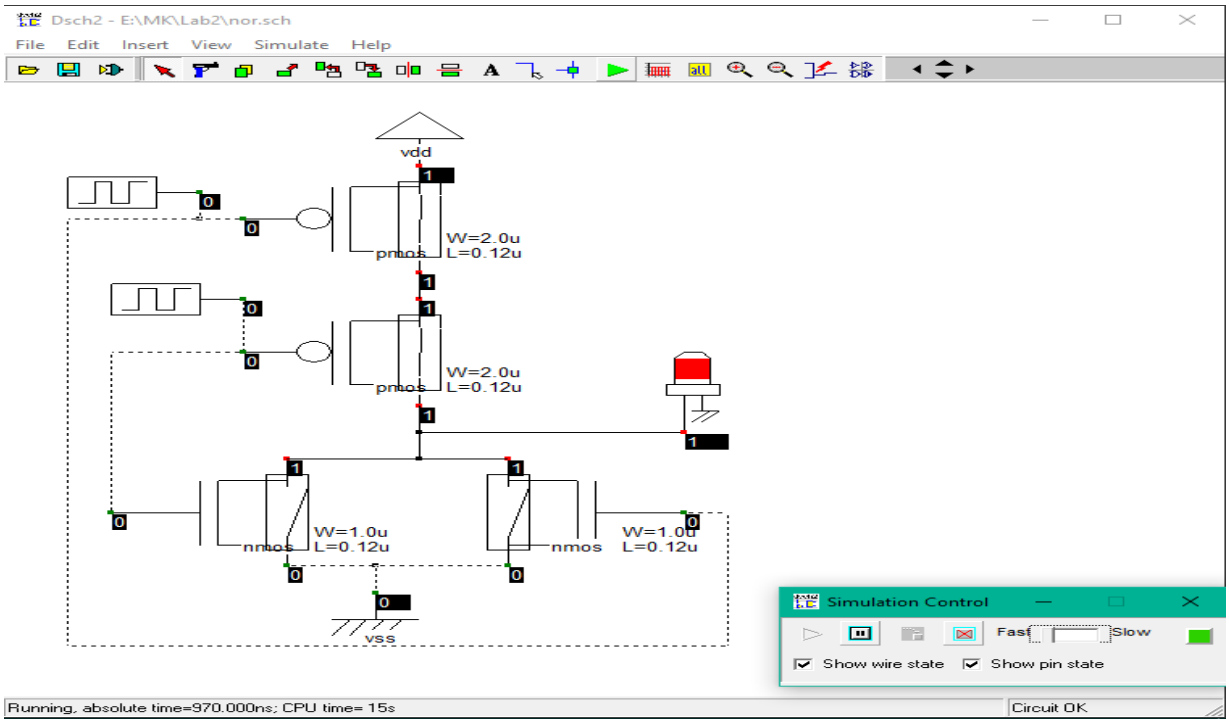
- Open the schematic editor called DSCH2. Instantiate nMOS or pMOS transistor (drag and drop) from the symbol library, place them in the editor window and connect them according to schematic diagram shown below:



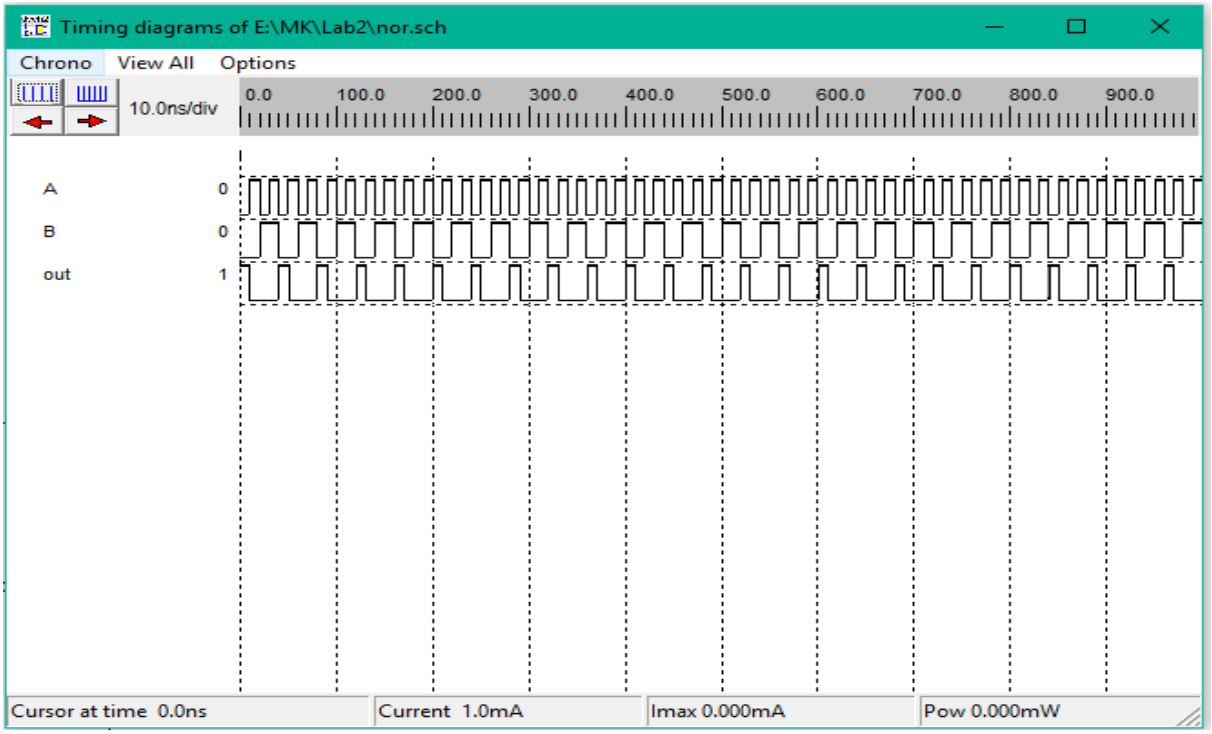
- Connect V_{dd}, G_{nd}, clock as input pulse A, B and output (out) from the symbol library. Figure is shown below:



- At this point, the NAND gate is ready to simulate. Before going to simulation work, check whether any floating line exists in the diagram. For this purpose, click "Check floating line" in the simulation menu. Then start the simulation. The figure is shown below:

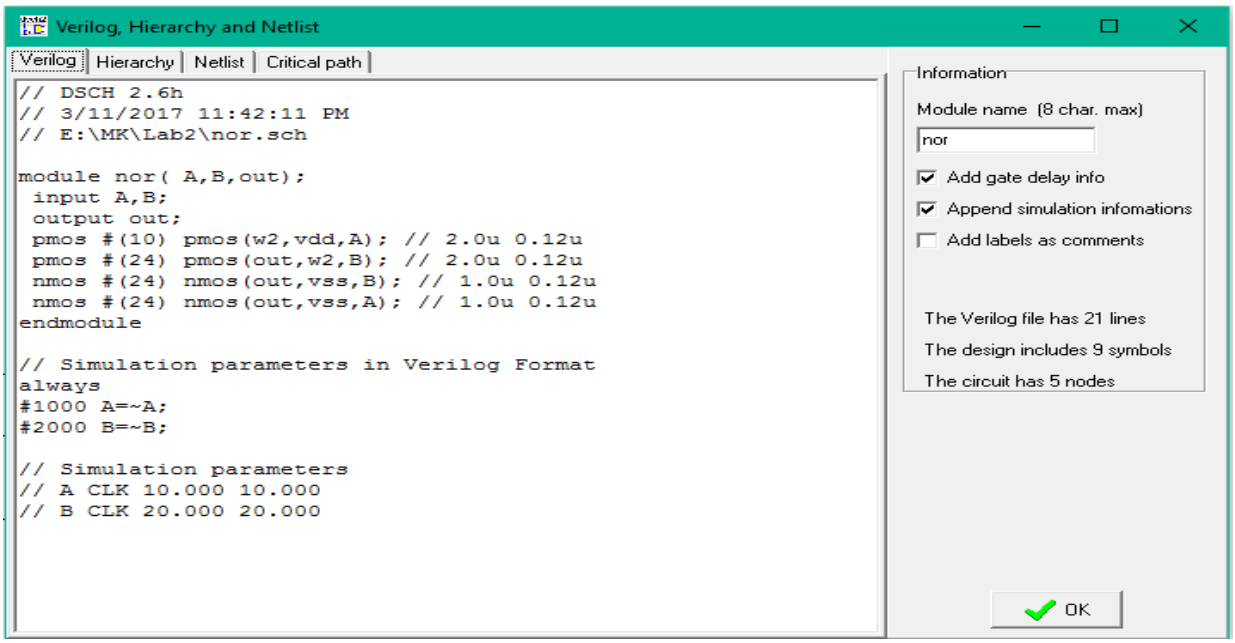


- The timing diagram of inputs and outputs pulses are shown below:

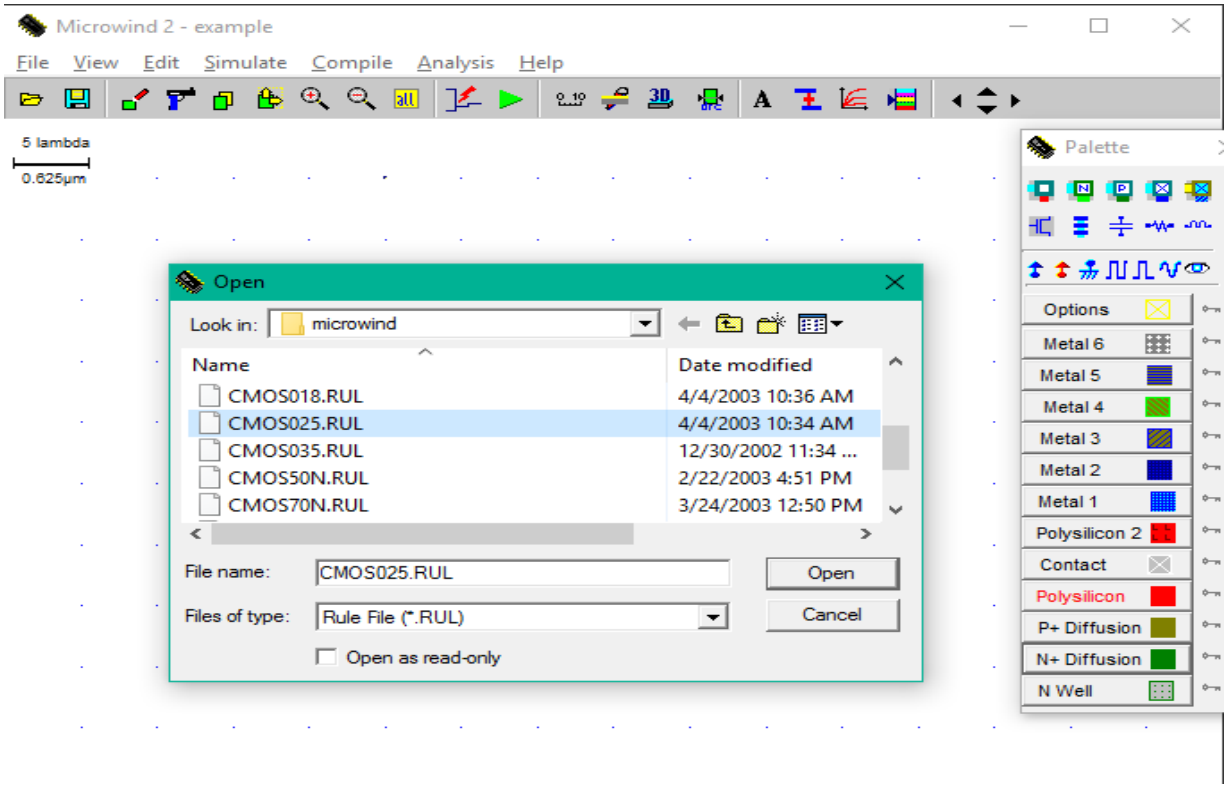


Circuit design and logic verification using DSCH2 and Micro wind.

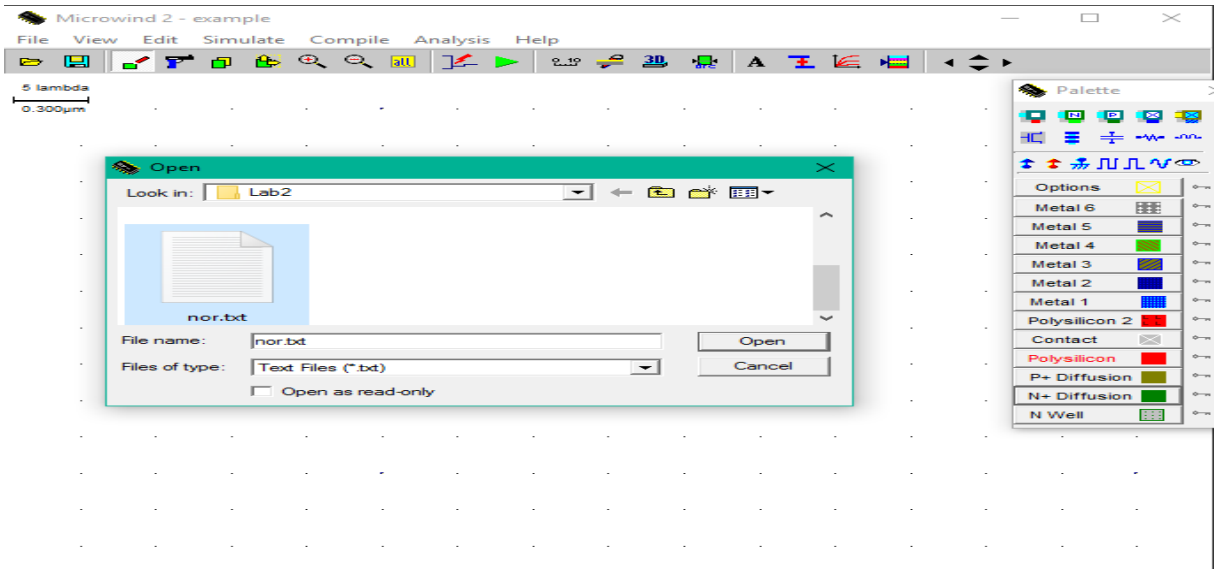
- Firstly, open the schematic in DSCH2 that we created. Convert the schematic into a Verilog representation. Click on File → make Verilog File. The verilog , Hierarchy ans Netlist window will appear shown below:



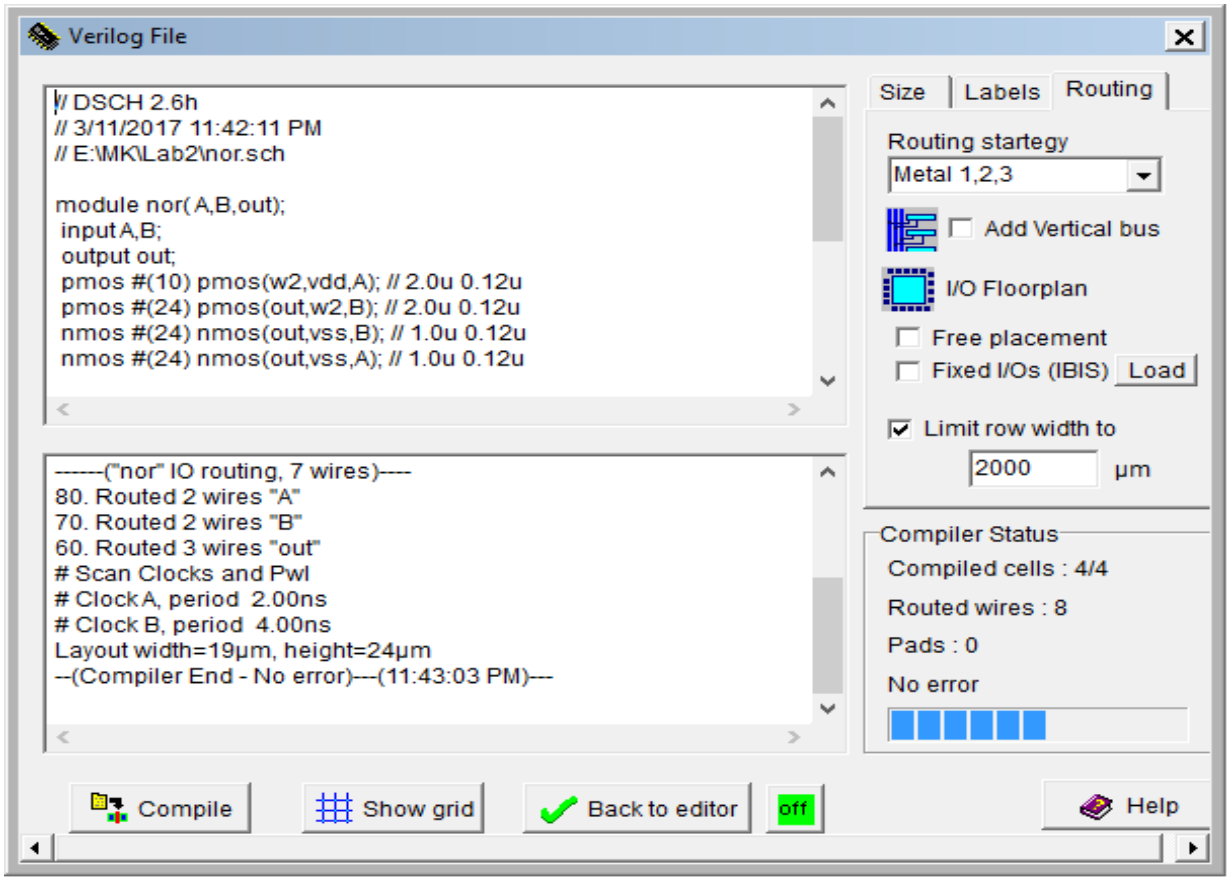
- Now open the layout editor window "Microwind2". Click on File → select Foundary and select cmos025.rul. This will set the layout design in 0.25u technology shown below:



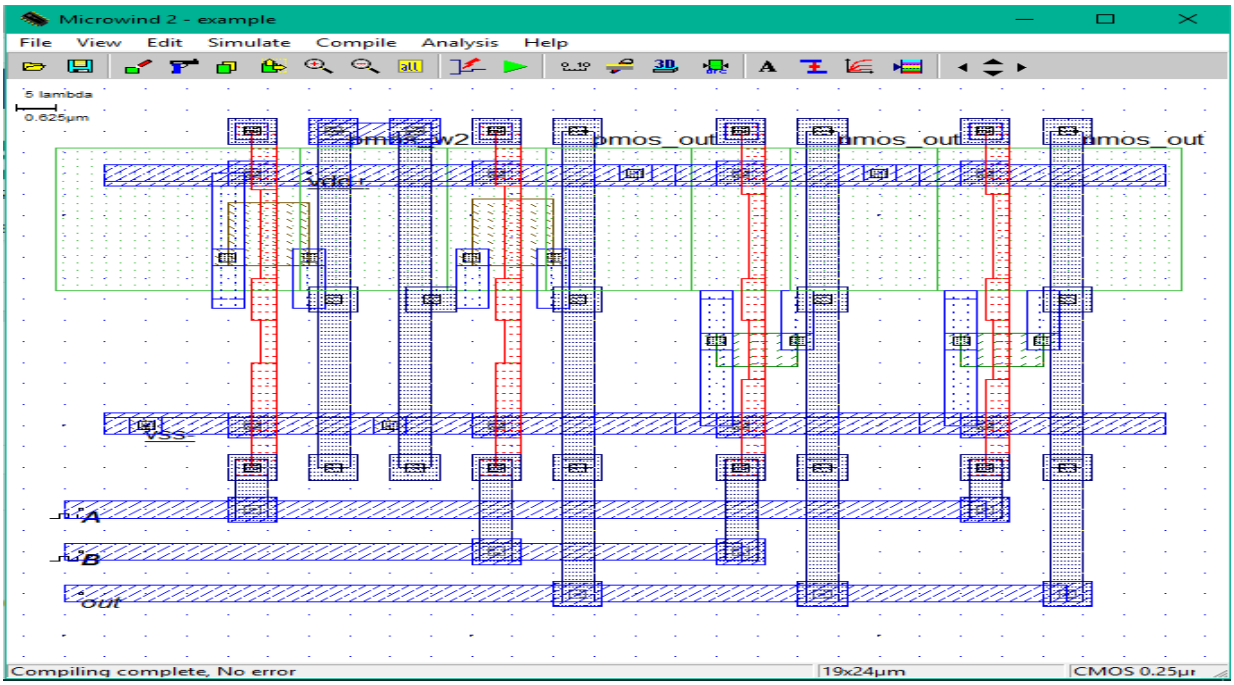
- Click on Compile → Compile Verilog File. A window will appear shown below and select the Verilog file as we saved before. Figure:



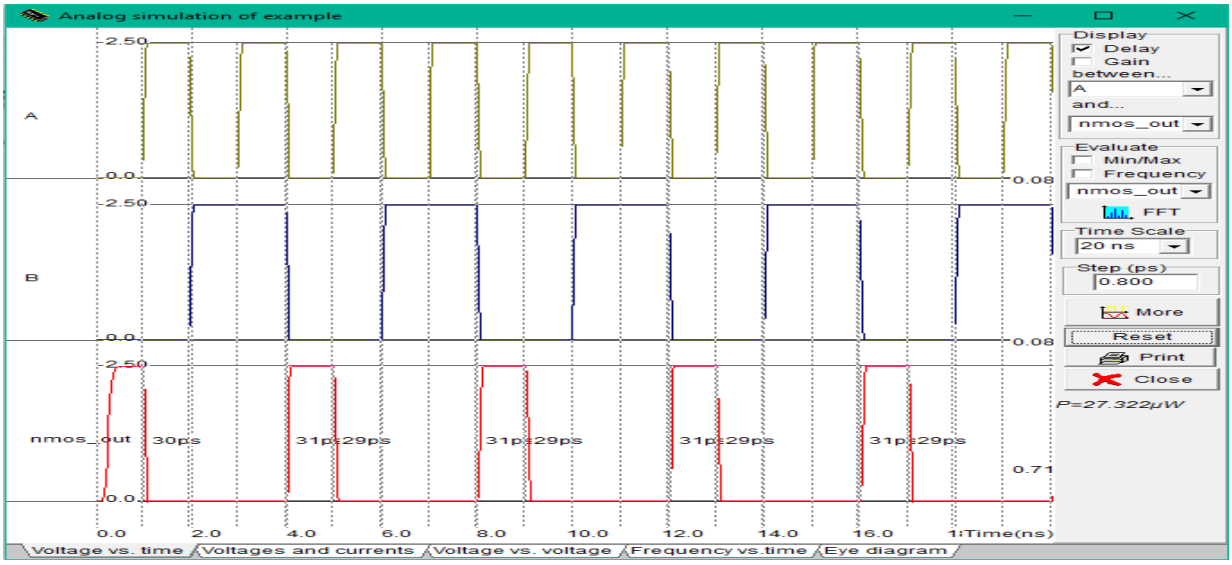
- The Verilog file after opening in microwind2:



- Now, Click on Compile Button. It will compile the Verilog file and finally it shows the no error if the code is compiled successfully. Close the window to see the layout. Our design as shown below:



- Click on Simulate → Run Simulation. A simulation window will appear with the inputs and output shown below:



Conclusion:

In this experiment we've used CMOS025 technology as foundary, there are several design principles which results a variety of performances of the same Logical Gates.