Experement Name: Observation and verification of transfer characteristics of CMOS inverter.

Objectives:

1. We can see the change of the output rate in the graph of voltage vs voltage and the voltage vs time .
2. 3.Layout design simulation using Micro wind.

3. Here we use inverter to see the output result. Inverter is contain both pMOS and nMOS.

4. To observe the deviation in results with default layout (automatic layout generation procedure) and our manual layout
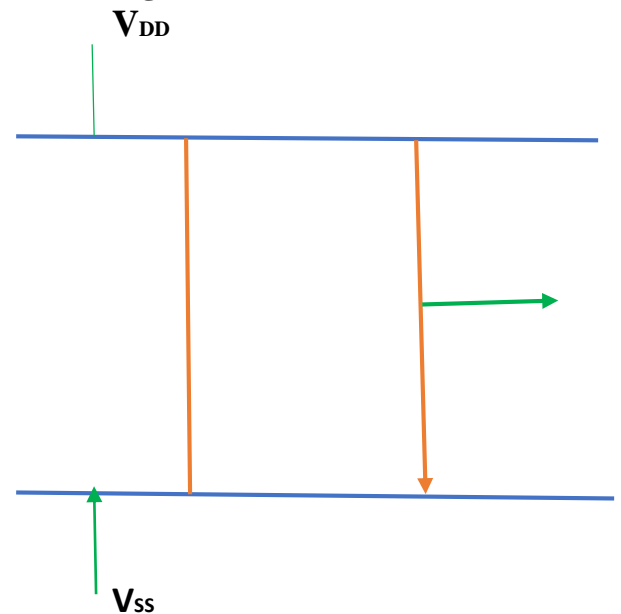
Apparatus: Here we use μ-wind software.

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   Table:

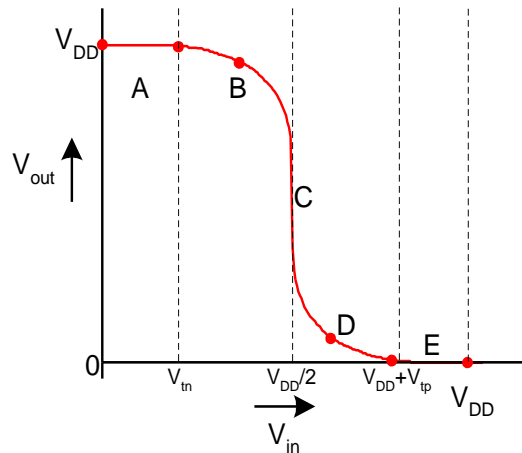| Inverter	pMOS		nMOS		β_p/ β_n
	Width	Length	Width	Length	
1st	50	1	5	1	0.1
2nd	5	1	5	1	1
3rd	5	1	50	1	10
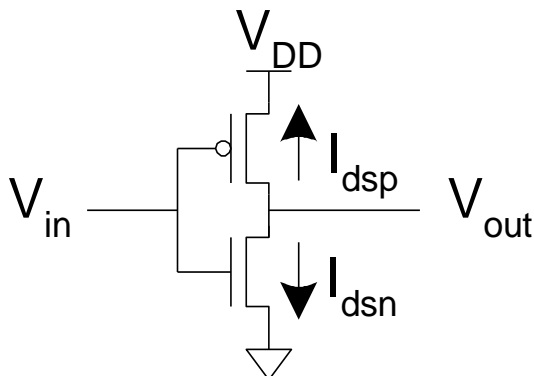
Schematic Diagram: **Stick Diagram:**

Transfer characteristics of CMOS inverter:

It has 5 region , A,B,C,D,E . Transistor operating regions are given below in chart.

For Region A.$0 \leq V_{in} \leq V_{tn}$.NMOS is off , $I_{dsn}= 0$; where PMOS is in linear region.In this circuit $I_{dsn} = -I_{dsp}$. Therefore both current will be zero,since $I_{dsn}= 0$Now $V_{dsp} = V_{DD}-V_{out}$Or, $0 = V_{DD}-V_{out}$; in linear region $V_{dsp} \approx 0$.Therefore $V_{out} = V_{DD}$.In region B, the nMOS transistor starts to turn ON, pulling the output down. In region C, both transistors are in saturation. Notice that ideal transistors are only in region C for Vin = VDD /2 and that the slope of the transfer curve in this example is –8 in this region, corresponding to infinite gain. Real transistors have finite output resistances on account of channel length modulation, described in Section 2.4.2, and thus have finite slopes over a broader region over a broader region C. Other 2 resion D and E will be like this .

We can measure this change by the, Beta ratio

If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$.This is called *skewed* gateOther gates: collapse into equivalent inverter

βp=mobility of pMOS =constant=W/L

βn=mobility of nMOS =constant=W/L, Here w=width and L=Length

βp/ βn=constant , Which is depend on its transfer characteristics is changes.

Working Procedure:

Step 1:- The automatic layout generated is not optimal layout in terms of area. Nor does it fit in the library specifications that we want. So the next step is to design the layout manually.

Step 2:- Use the layout editor to design a CMOS layout of our 4-input NAND gate. Attempt to minimize the width of the gate. Open microwind and click *File →Select Foundry* and select *cmos 025.rul*. this sets our layout editor designs 0.25u technology.

Step 3:- Let us consider the problem specifications are 100 lamda height and 20 lamda for Vdd and GND rails. So we will place Vdd and GND rails 20 lamda height and spaced 60 lamda apart. Vdd and GND rails are in Metal. The top rail is used as Vdd. And the buttom one is as GND. To create a metal rectangle click on Metal 1 in the palette and then the required rectangle in the layout window.
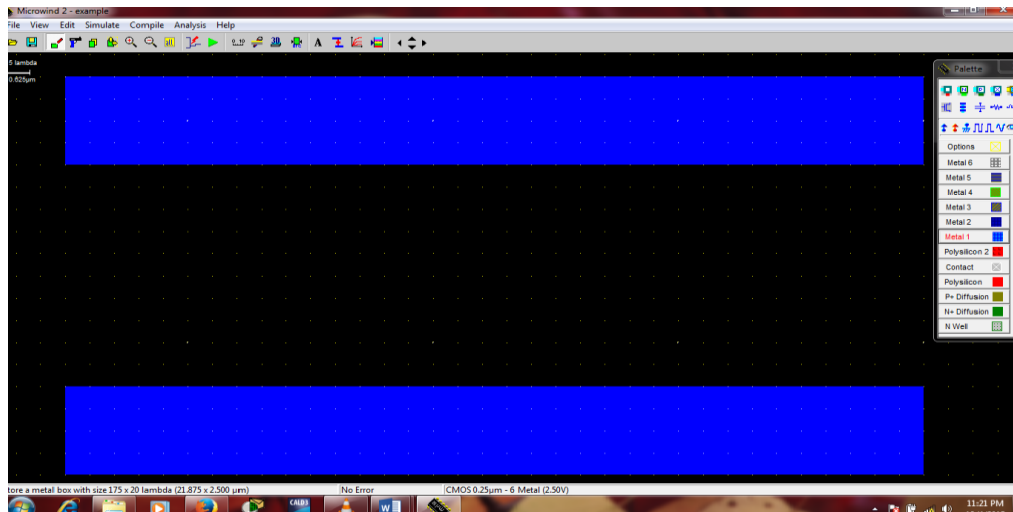
Step 4:- The next step is to place two pMOS transistor in parallel. The source of the transistor is connected to the Vdd to the top. Create another device in a similar manner to place it in parallel to the first pMOS device. We share the 50 devices drain diffusions. This saves on area as well as reduces capatences. At any stage of designing the layout, we can run DRC check to see if your design has any errors. A DRC check can be run by clicking an Analysis→ Design Rule Checker.

Step 5:- Adding pMOS for the 1st inverter with the ratio of 50 and 1. Place the pMOS transistor in our design.
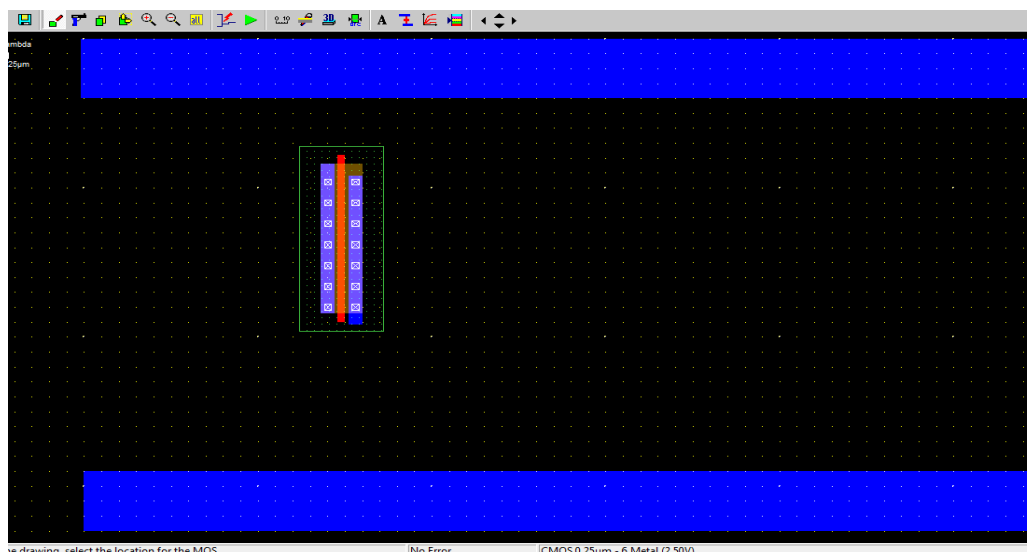

Fig 1: pMOS added

Step 6:- The next step is to build nMOS transistors. These are in series for a NAND gate. Click on the transistor symbol in the palette. A layout generator window will appears. Click on MOS tab and set W, L of the transistor. Set the type (nMOS/pMOS). Check the units of the sizes (lamda/micron)

Step 7:-. Adding pMOS for the 1st inverter with the ratio of 50 and 1. Place the pMOS transistor in our design.
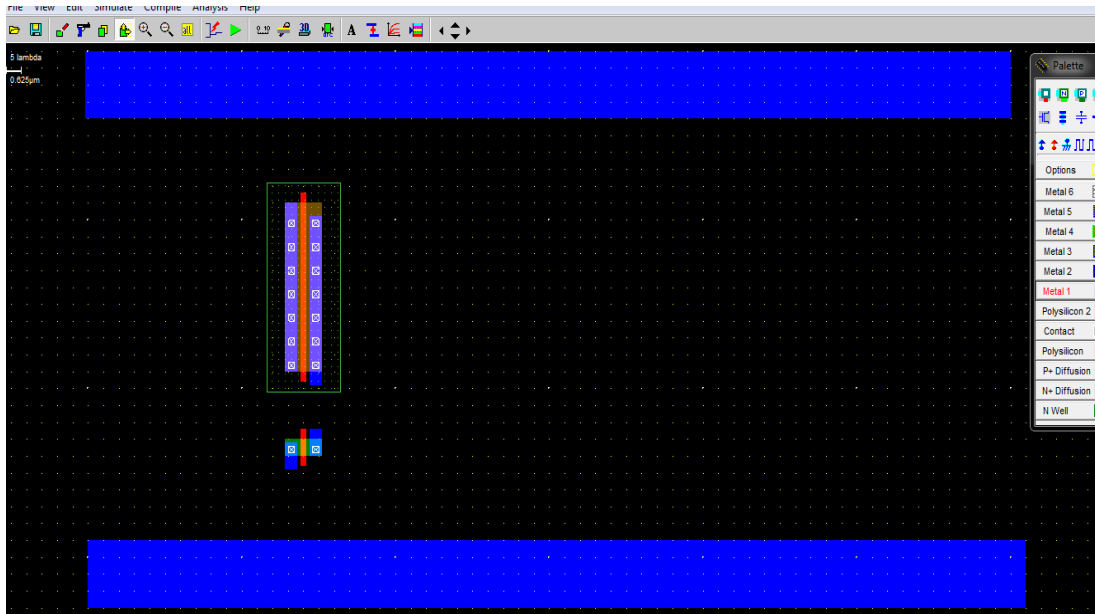

Fig2: nMOS added.

Step8:- Now metal and poly inputs are connected in 1st inverter.
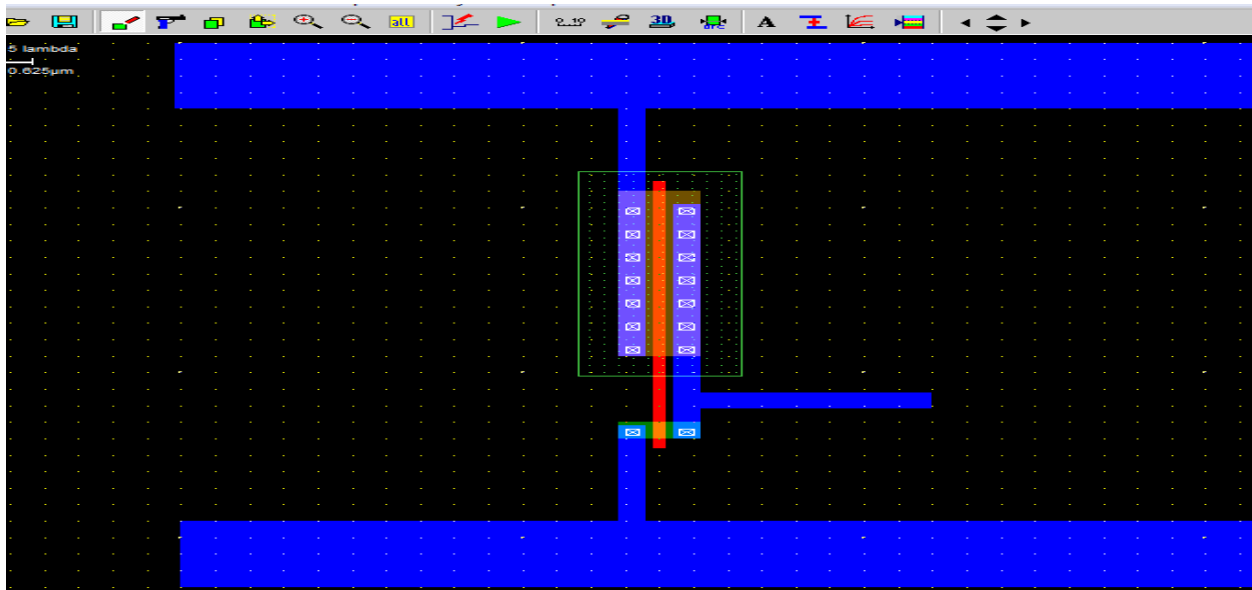
Fig 3: adding poly silicon connections

Step9:- Now adding the pMOS for the 2nd inverter, Here the width and length is 5 and 1 for pMOS. Place the pMOS transistor in our design.
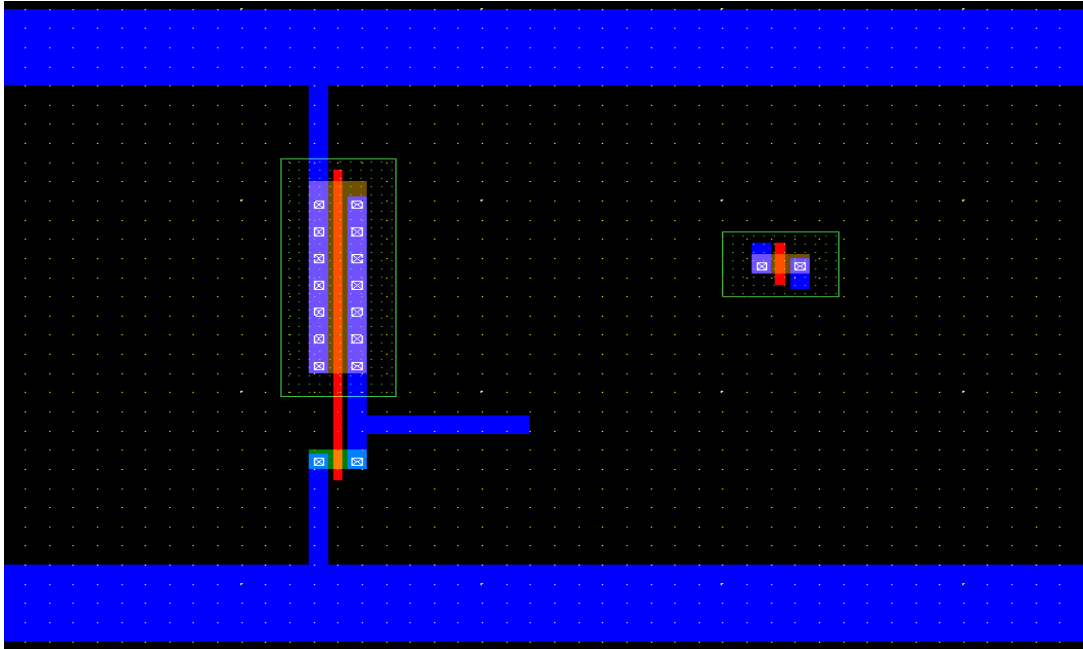

Fig4: pMOS added.

Step10:- Now adding the nMOS for the 2nd inverter, Here the width and length is 5 and 1 for nMOS. Now adding nMOS for the 2nd inverter.
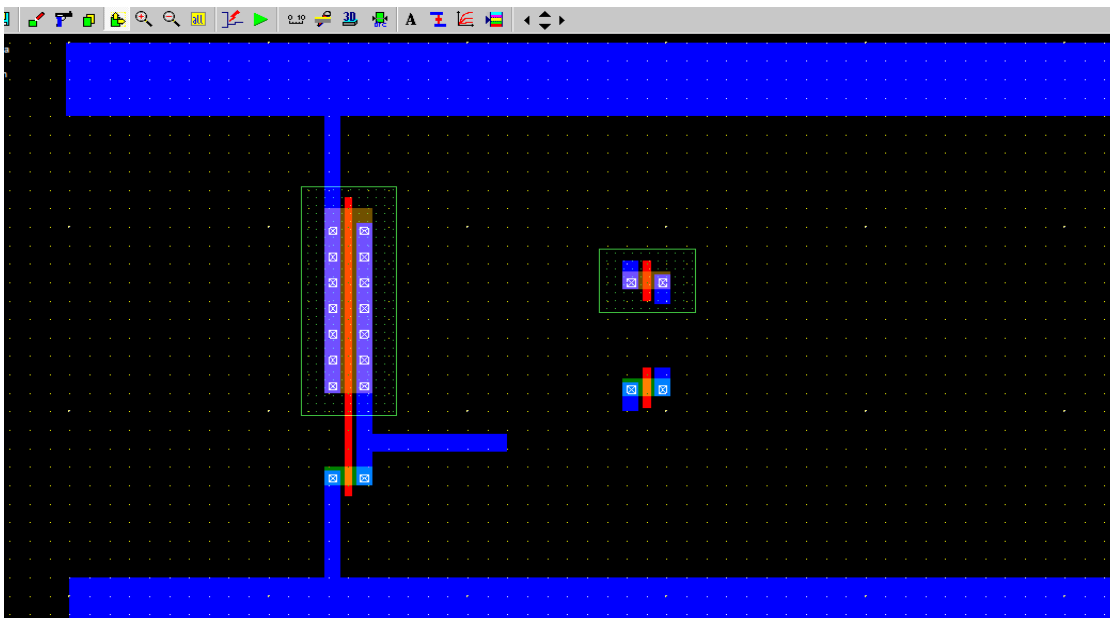

Fig5: nMOS added.

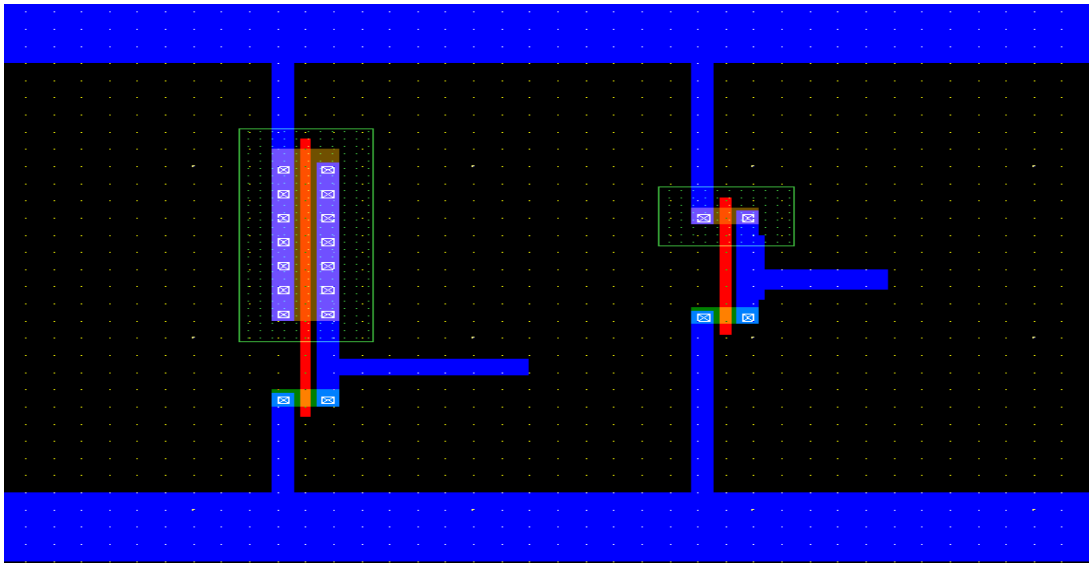**Step11:-** Now metal and poly inputs are connected in 2st inverter.

Fig 6: adding poly silicon connections

Step12:- Now adding pMOS for the 3rd inverter. Here the ratio of width and length is 5and 1. Now added pMOS for the 3rd inverter
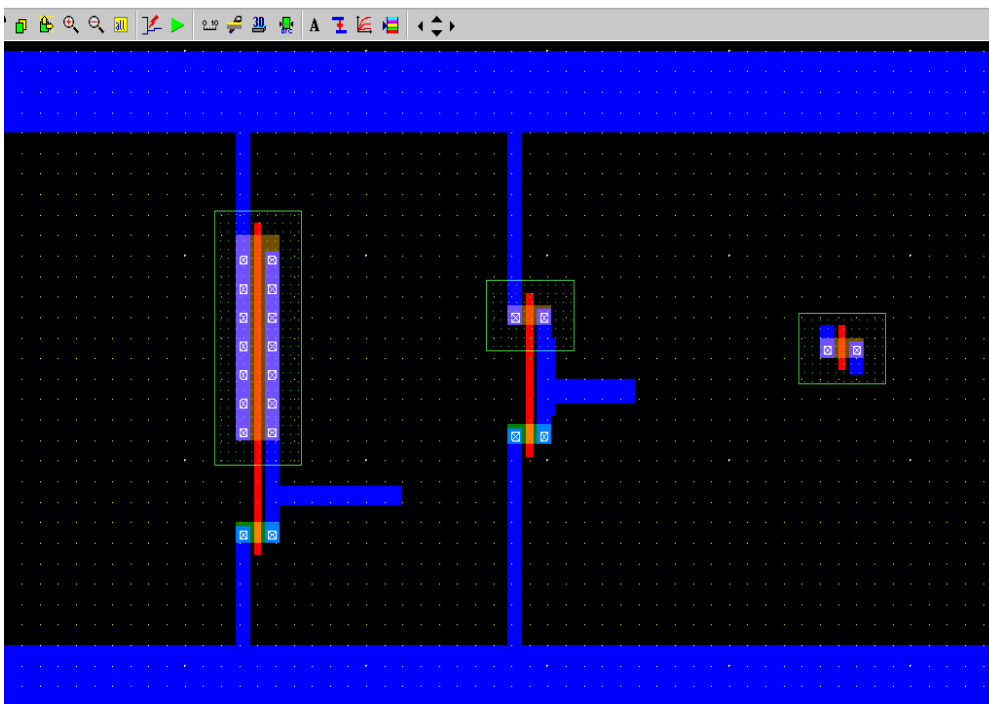

Fig7: pMOS added.

Step13:- Now adding nMOS for the 3rd inverter. Here the ratio of width and length is 50 and 1. Now added pMOS for the 3rd inverter
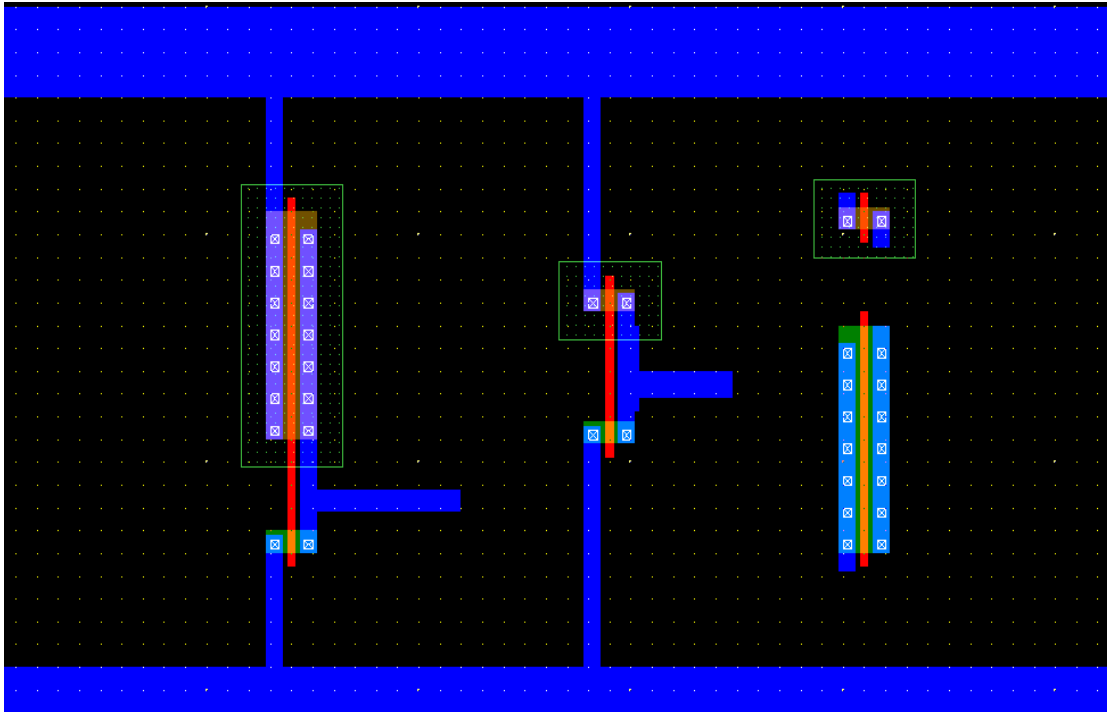

Fig8: nMOS added.

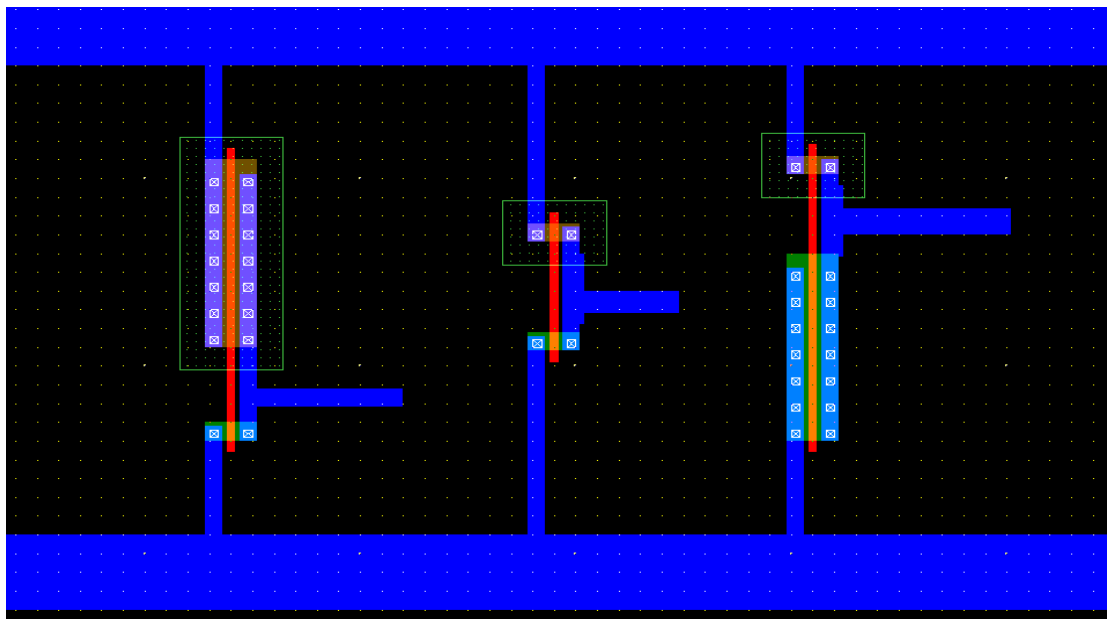**Step14:-** Now metal and poly inputs are connected in 2st inverter.

Fig 9: adding poly silicon connections

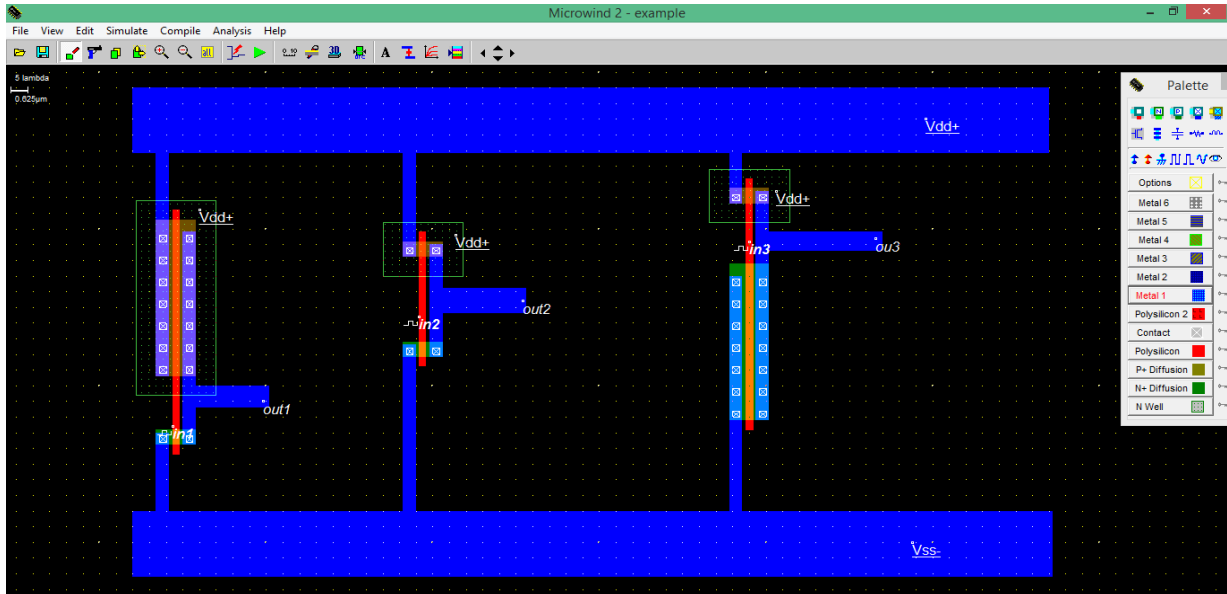**Step15:-** Finally the input and output are connected and we are now ready to run the simulation.

Fig 10: final diagram of CMOS inverter(with 3INVERT)

Step16:- To run the simulation of our circuit, click on *Simulate →Start Simulation.* Depending on the input sequences assigned at the input the output is observed. The power value is also taken. Make tphl, tplh and tp measurements, by changing the input sequences and clicking and dragging the mouse on the waveform in the horizontal direction. Most of the times, microwind automatically provides with the rise and fall delays on the waveforms. The power consumption is also provided at the bottom right of the window.
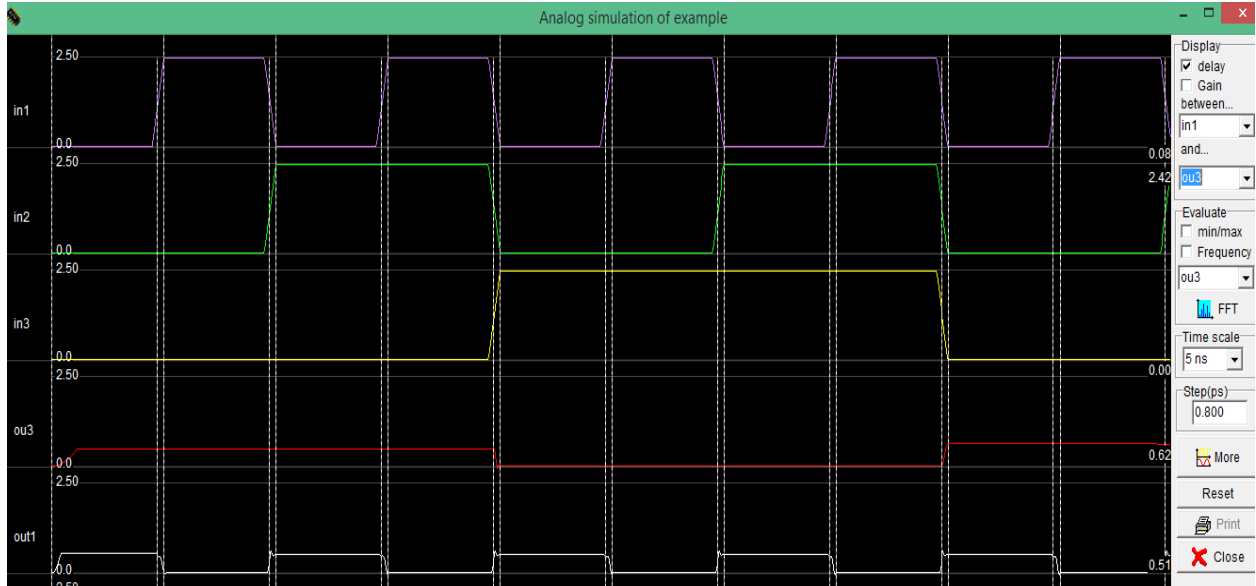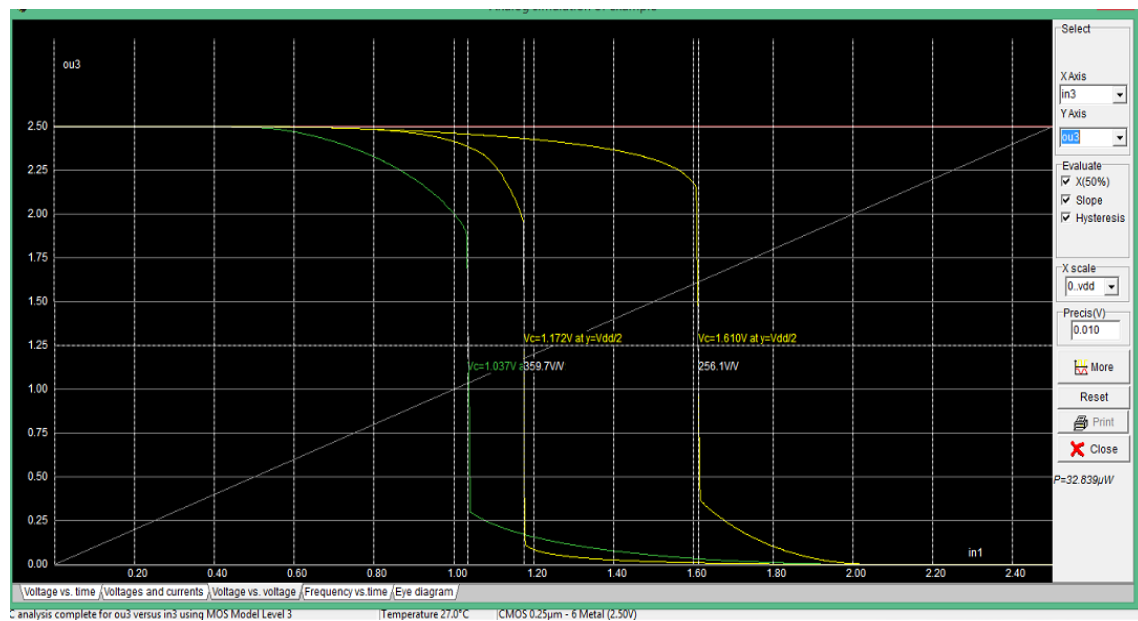
Timing diagram (Voltage Vs Time)

Fig 11: Timing diagram

Plot voltage Vs voltage

Conclusion:

The CMOS INVERT gate is implemented using three pMOS and three nMMOS with different ratio. The required waveforms were obtained, observed and noted down using µ-wind. And we observe the change of output in the voltage vs time graph and the voltage vs voltage graph .