

# Experiment 5

## Observation and Verification of Transfer Characteristics of CMOS INVERTER

### 5.1 Objectives

- ✓ Simulation of the inverter as a function of time
- ✓ To display the transfer characteristics curve of CMOS inverter.
- ✓ To verify the variation of transfer characteristics as a function of  $\frac{\beta_n}{\beta_p}$  ratio.
- ✓ Find the noise margins of a gate

### 5.2 Theory:

The CMOS inverter includes 2 transistors. One is a n-channel transistor, the other a p-channel transistor. The device symbols are reported below. In order to build the inverter, the nMOS and pMOS gates are interconnected as well as the outputs as shown in Figure 1.

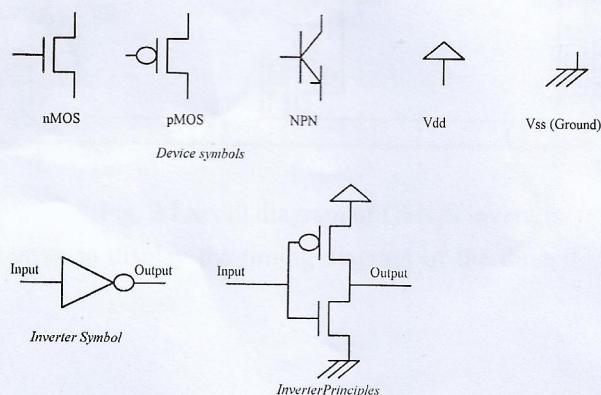


Fig. 1. The schematic diagram of the CMOS inverter with one nMOS at the bottom and one pMOS at the top.

### 5.3 Procedure

#### a) Simulation of CMOS inverter as a function of time

- ⇒ Open the microwind window and Check that the selected foundry is 0.25  $\mu\text{m}$  CMOS process from *file → select foundry* and choose *cmos025.rul*. Use *Level1 MOS* transistor model.
- ⇒ Generate the nMOS and pMOS transistors for creating CMOS inverter with width and length ratio specified in table 1. In this experiment we will generate three inverters that we need for experimenting  $\frac{\beta_n}{\beta_p}$  ratio effect. The layout diagram is shown in figure 2.

Table 1: Inverters width and length

Name	pMOS		nMOS		$\frac{\beta_n}{\beta_p}$
	Width ( $\gamma$ )	Length( $\gamma$ )	Width ( $\gamma$ )	Length( $\gamma$ )	
1 <sup>st</sup> Inverter	50	1	5	1	0.1
2 <sup>nd</sup> Inverter	5	1	5	1	1
3 <sup>rd</sup> Inverter	5	1	50	1	10

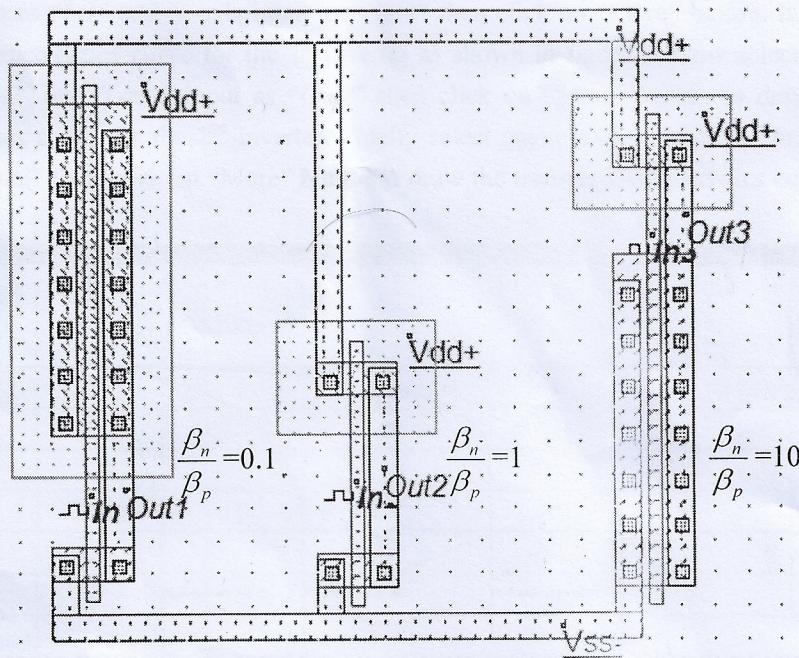


Fig. 2 Layout diagram of CMOS inverters

- ⇒ Run *Simulation* button to display the timing diagram of the three CMOS inverters as shown in figure 3.

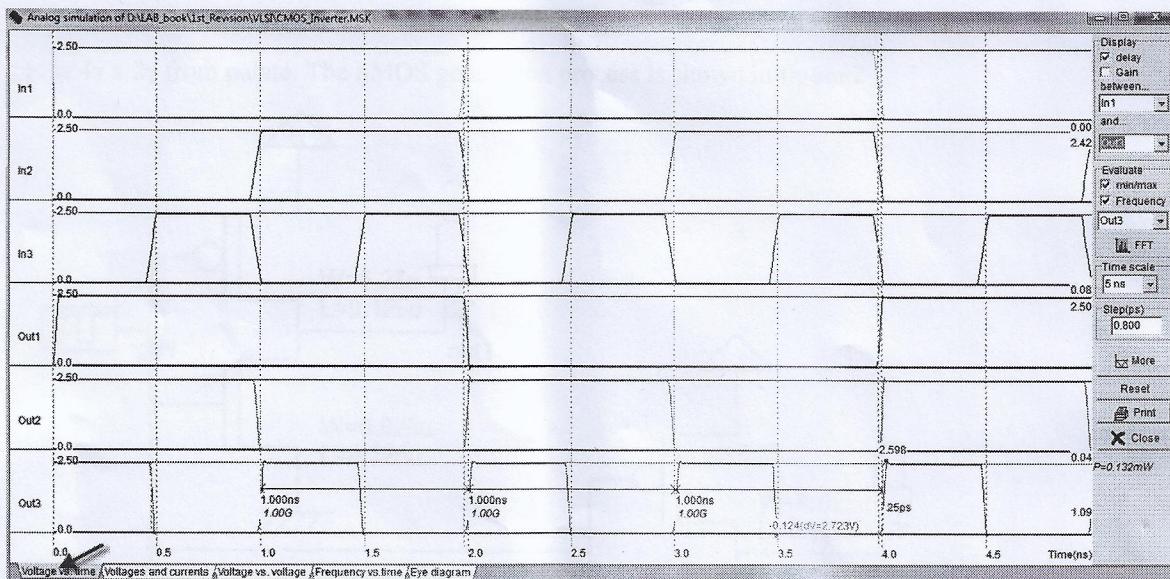


Fig. 3 Timing diagram of the three CMOS inverters

**b) Observe the transfer characteristics curve of CMOS inverter and ratio effects.**

- ⇒ In the simulation window, click on the voltage vs voltage tab and in the upper right corner select X-axis input as “In1” and Y-axis input as “Out1” then click on “More” button. It will draw the transfer characteristics curve for the 1<sup>st</sup> inverter as shown in figure 4. Now select again X-axis input as “In2” and Y-axis input as “Out2” then click on “More” button to draw the transfer characteristics curve for the 2<sup>nd</sup> inverter. Finally select again X-axis input as “In3” and Y-axis input as “Out3” then click on “More” button to draw the transfer characteristics curve for the 3<sup>rd</sup> inverter.

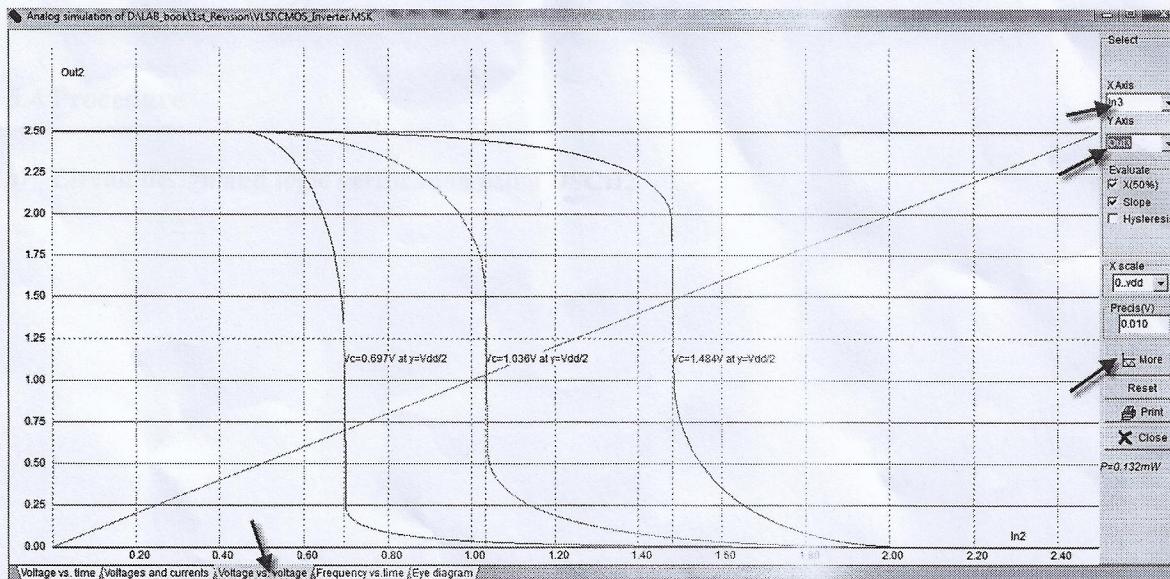
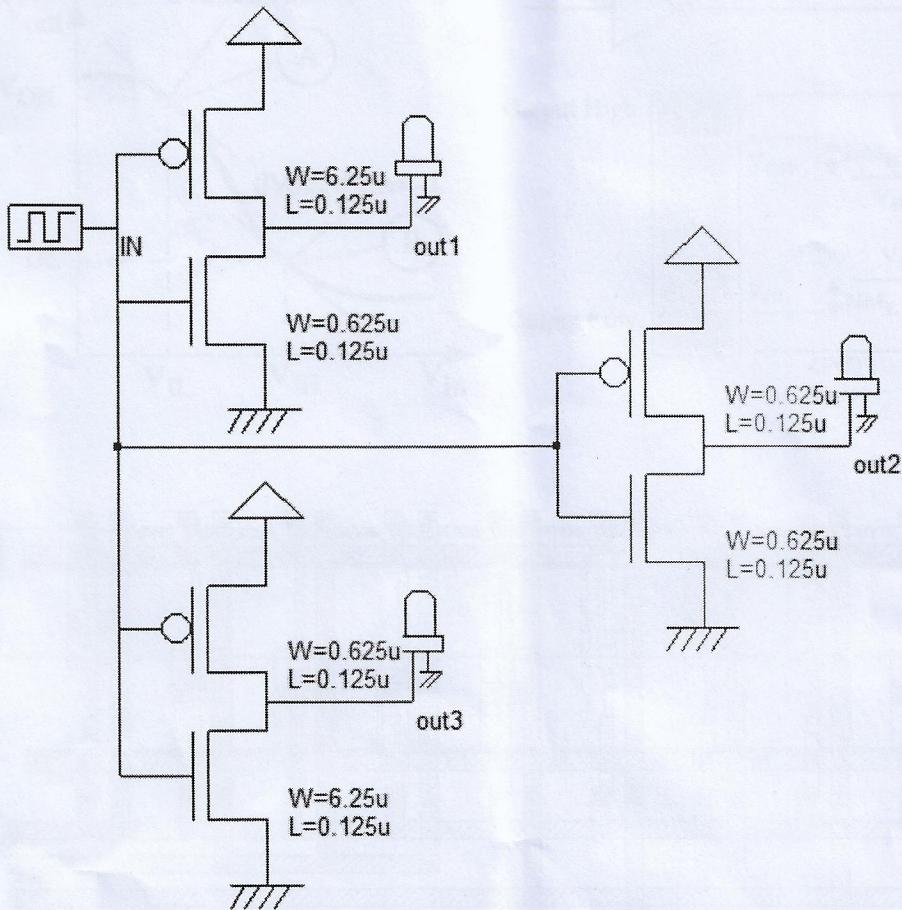


Fig. 4 The transfer characteristics curves the three inverters

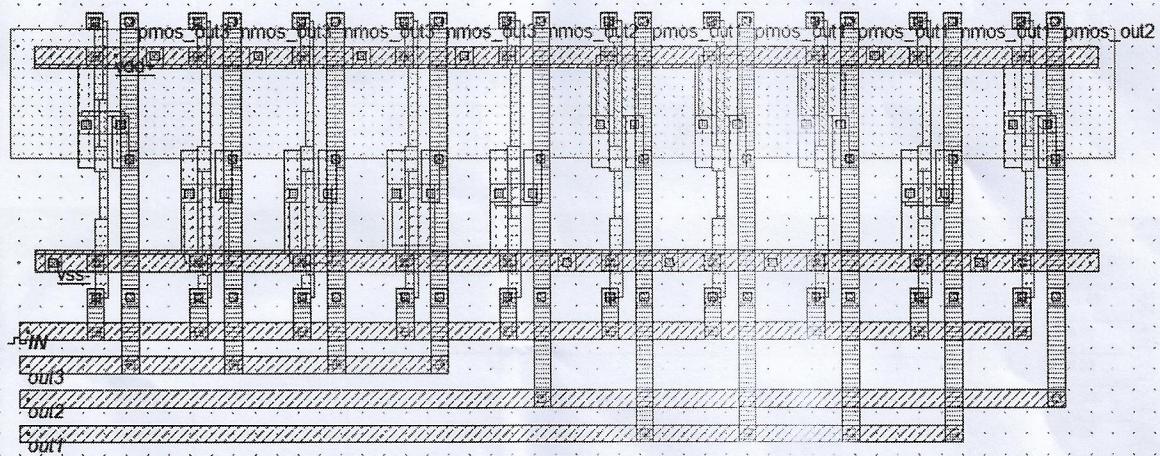
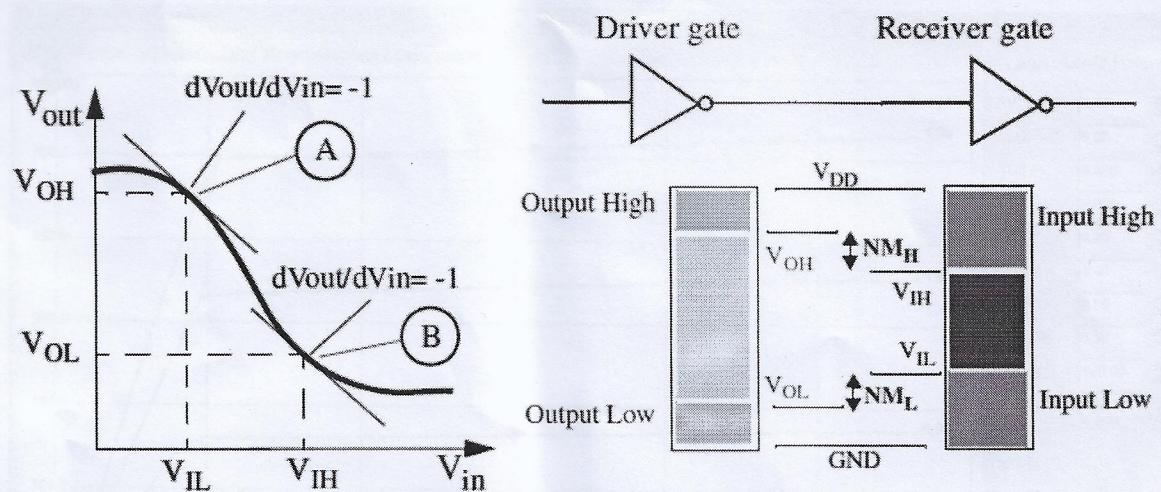
$\Rightarrow$  is  $4\gamma \times 2\gamma$  from palate. The nMOS generation process is shown in figure 2



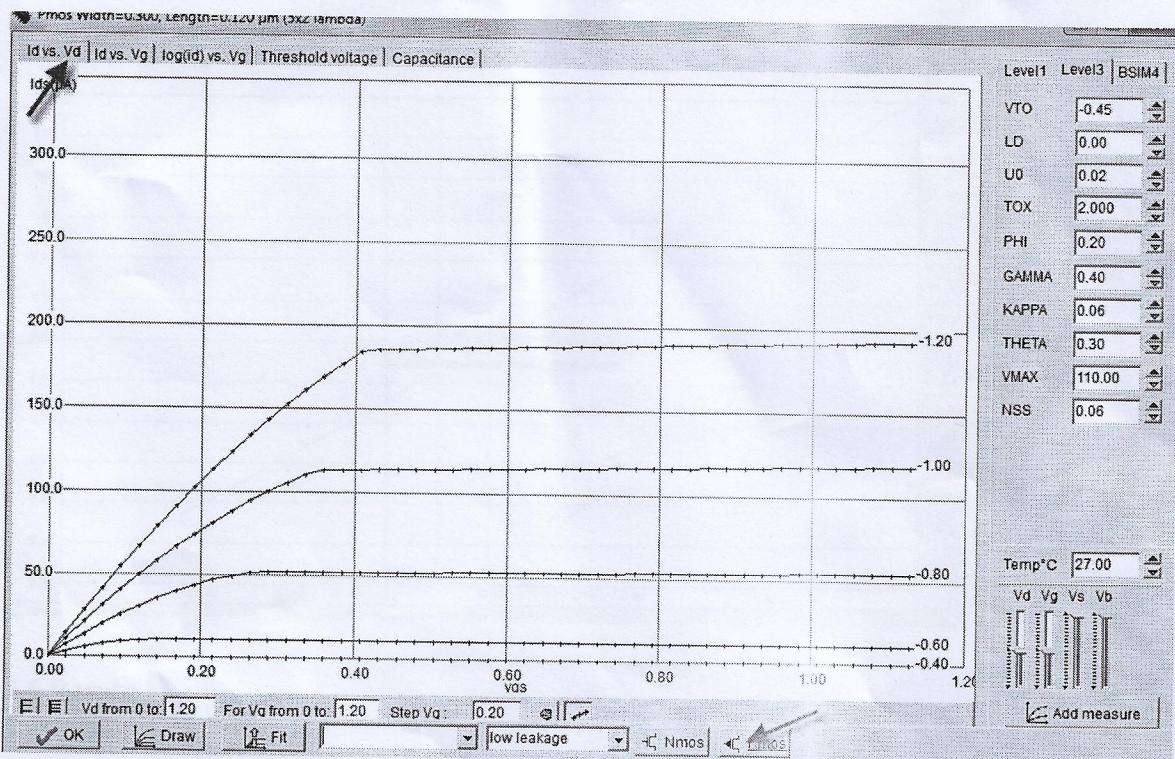
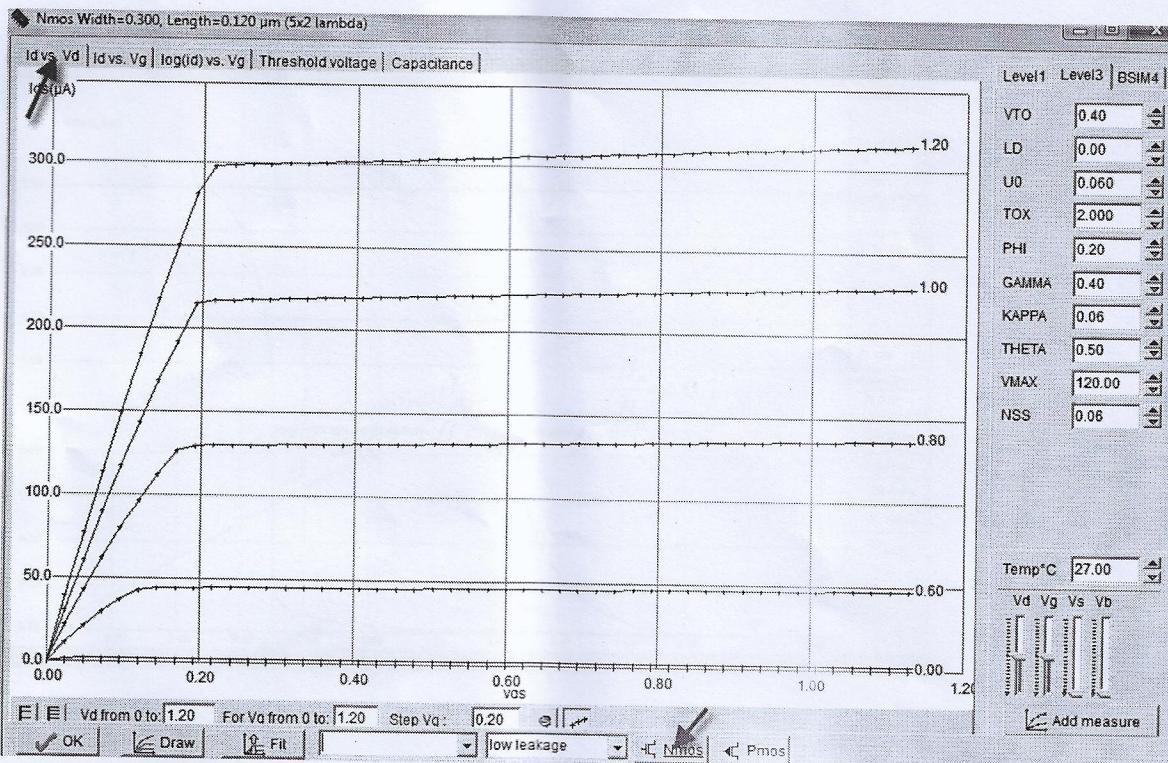
#### 5.4 Procedure

- a) Circuit design and logic verification using DSCH2

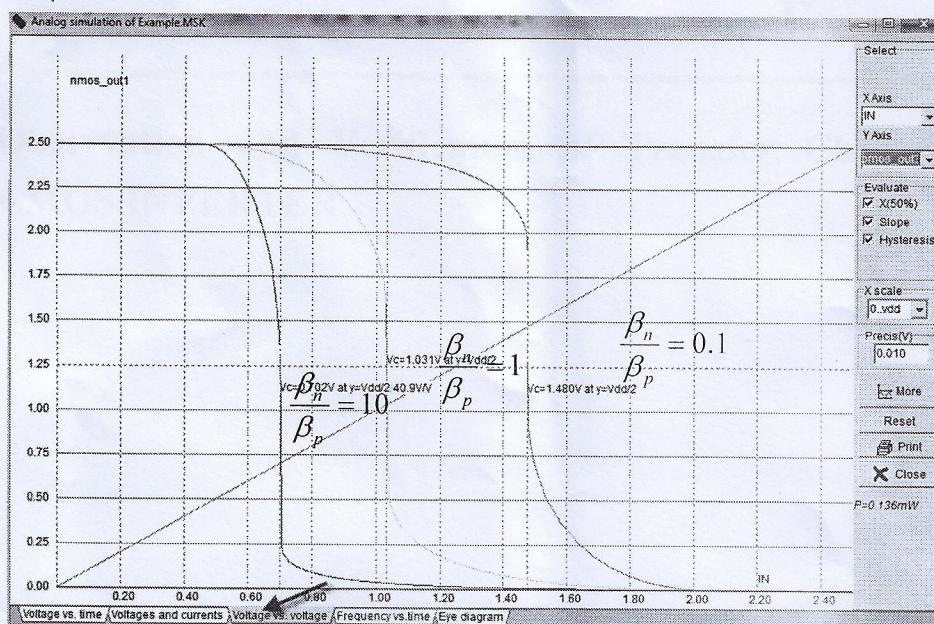
$\Rightarrow$



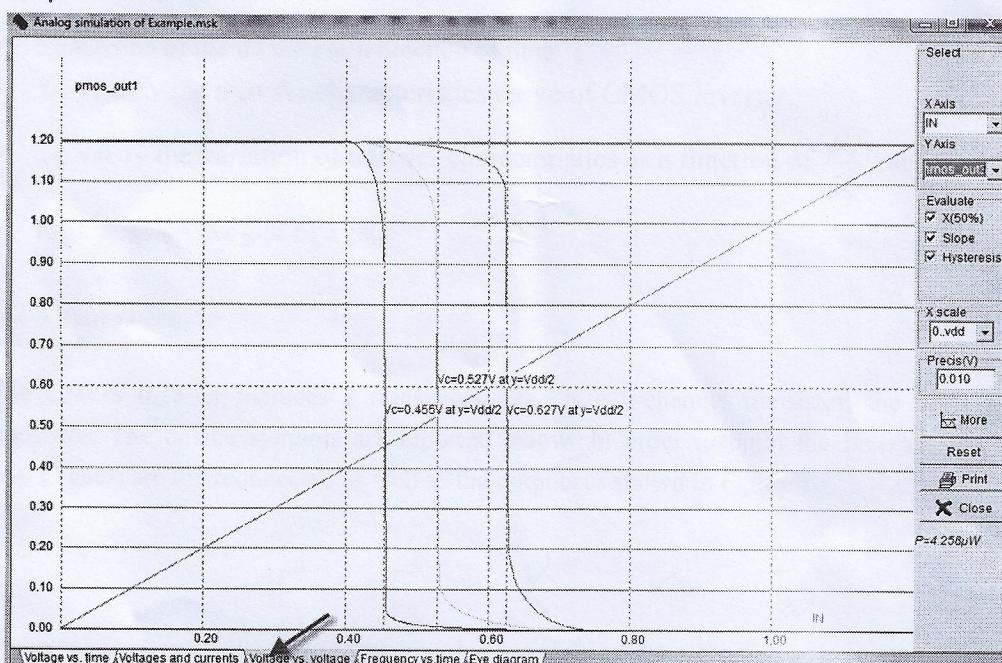
⇒ The above figures show the functionalities of the XOR gate according to the truth table. Click on the (last icon) timing diagram icon in the *icon menu* to see the timing diagram of inputs and outputs pulses are shown below:



## .25 μm CMOS Process



## .12 μm CMOS Process



## 5.5 Result:

The XOR is designed and the truth table is successfully verified. The required waveforms were obtained, observed and noted down using microwind2.