Title: Observation and Verification of nMOS characteristics.

1) Objectives:

i. To find the MOS model parameters for the transisotrs and then by "pencil & paper" manually calculate the DC characteristics of I_{DS} current vs V_{DS} voltage, using simple current equations for MOS model Level 1 to determine a number of corresponding value pairs of (I_{DS} ; V_{DS}) with gate-source voltage , V_{GS} = a constant > V_{th}.

ii. Use circuit simulator of Micro-wind to do a DC simulation of the I_{DS} current vs V_{DS} voltage and the result of the two methods compared

iii. Calculation of the threshold voltage.

2) Aparatus:

a) Microwind software.

3) **Theory:** The nMOS transistor I_{DS} current versus V_{DS} voltage equations are as follows:

a) **Cut-off mode**: $I_{DS} = 0$ when $V_{GS} < 0$.

b) **Triod/Linear region**: IDS = $k_n\{(V_{GS}-V_{Th})V_{DS}-\frac{1}{2}V_{DS}^2\}$ when $V_{DS} < V_{GS} - V_{th}$ ----(1)

In Level 1 SPICE model, IDS = $\mu_0.\frac{\epsilon_0\epsilon_{SiO_2}}{T_{ox}}.\frac{W}{L}\{(V_{GS}-V_{Th})V_{DS}-\frac{1}{2}V_{DS}^2\}$

c) **Saturation egion:** $I_{DS} = \frac{1}{2}k_n\{(V_{GS}-V_{Th})^2(1+\lambda V_{DS})\}$ when $V_{DS}>V_{GS}-V_{th}$ --------(2)

In level 1 SPICE model $I_{DS} = \mu_0.\frac{\epsilon_0\epsilon_{SiO_2}}{T_{ox}}.\frac{W}{L}(V_{GS}-V_{Th})^2$

when channel modulation effect is neglected the drain current equation (2) can be simplified as

$I_{DS} = \frac{1}{2}k_n\{(V_{GS}-V_{Th})^2\}$ when $V_{DS} > V_{GS} - V_{th}$ --(3)

The current gain factor k_n is a constant with unit . This is dependent on MOS transistor geometry (channel length L and channel width W), fabrication process parameters (electron mobility, μ_n and gate-oxide capacitance C_{OX}).

The factor k_n can be calculated as $k_n = k'_n\frac{W}{L}$ where the process conductance parameter

$k'_n=\mu_n C_{ox}[\frac{A}{V^2}]$. The parameters C_{OX} stands for gate oxide capacitance per unit area dependent on gate oxide thickness t_{OX}. This can be expressed as $C_{OX}=\frac{\epsilon_{ox}}{t_{ox}}$ where the $\epsilon_{ox}=3.97$ is the silicone dioxide permitivity which can be calculated with the knowledge of relative dielectric constant value of silicon dioxide ϵ_{SiO_2} and dielectric constant of vacuuam ϵ_0 . So $\epsilon_{ox}=\epsilon_{SiO_2}*\epsilon_0$. The additional parameter of the I_{DS} and V_{DS} is the threshold voltage V_T . The threshold voltage with zero source-substrate (bulk) voltage can be expressed as V_{T0} . When the source-substrate (bulk) voltage V_{SB} is not equal to zero then we call it for nMOS transistor is V_{tn} and for pMOS is V_{tp} can be expressed as follows:

$$V_{T_n}=V_{T_{0n}}+\gamma(\sqrt{2\phi_b+|V_{SB}|}-\sqrt{2\phi_b})$$

$$V_{T_p}=V_{T_{0p}}+\gamma(\sqrt{2\phi_b+(V_{DD}+|V_{BS}|)}-\sqrt{2\phi_b})$$

The table below shows the SPICE MOSFET parameters in level 1

Microwind SPICE symbol	Meaning	Theoritical Symbol	Unit
VTO	Threshold Voltage	V_{T0}	V
TOX	Oxide thickness	t_{ox}	nm
UO	Low-field obility	μ_0	$\frac{m^2}{V.sec}$
PHI	Surface potential	$2\|\phi\|$	V
GAMMA	Body-bias coefficient	γ	V^2

4) Procedure:

a) Level 1 MOS model equations to calculate DC values for the drain current I_{DS} vs drain-source voltage V_{DS}.

- First calculate with a gate-source voltage V_{GS} = +2.0 V, for each drain-source voltage V_{DS}; 0.5, 1.0, 1.5, 2.0, 2.5 the difference V_{DS} - (V_{GS} – V_{tn}) to determine in which region transistor work.. Mark in table 2 equation umber 1 or 2 that should be chosen to calculate the drain current I_{DS} for the correspondingpoint (I_{DS},V_{DS}) . If we consider the 0.25um CMOS processing technology then V_{th} = 0.45V, $\mu_0=\mu_n=0.06, \gamma=0.4, t_{ox}=0.5\,nm$
- Calculate for the voltages V_{DS}: 0.5, 1.0, 1.5, 2.0, 2.5 volts the drain-current I_{DS} for each point (I_{DS};V_{DS}) after having determined a region the transistor works in (linear or saturated) Fill in corresponding value pairs (I_{DS};V_{DS}) in table 2 for given drain-source DC voltages.

V_{DS}	0.5	1.0	1.5	2.0	2.5
V_{DS}-(V_{GS}-V_{tn})	eqn-1	eqn-1	eqn-1	eqn-2	eqn-2
Manual Calculation I_{DS} (uA)	547.56	884.52	1010.88	1011.933	1011.93

➢ Now plot the characteristics curve using excel based data-values of table 1 the curve is like as shown in figure

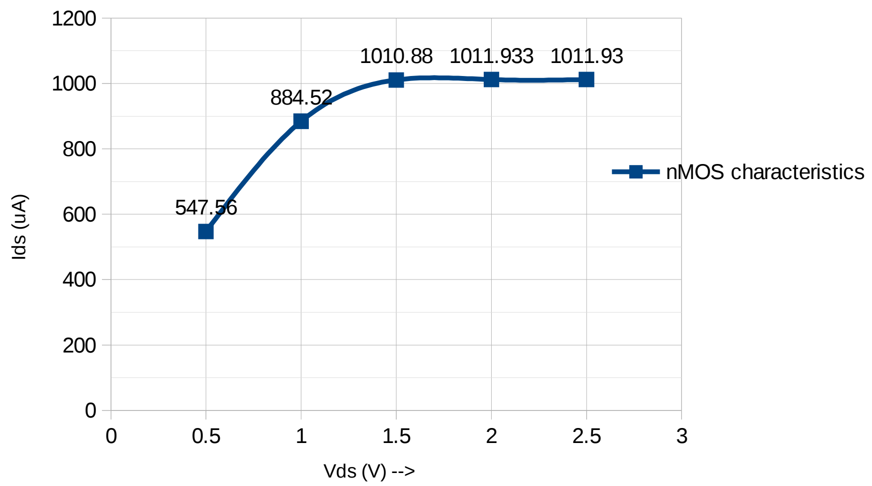

Fig 1: Characteristics of nMOS transistor

Use of "Simulate>MOS characteristics" to generate the DC characteristic I_{DSn} vs V_{DSn} for the nMOS transistor in microwind.

- Open the microwind window and check that the selected foundary is 0.25 um CMOS process from file→ select foundary and choose cmos025.rul. Use Level 1 MOS transistor model.
- Now generate the nMOS transistor of width and length ratio is $4\lambda x 2\lambda$ from palate. Then simulate the generated nMOS to check its characteristics curve and compare the curve with the manually generated curve.

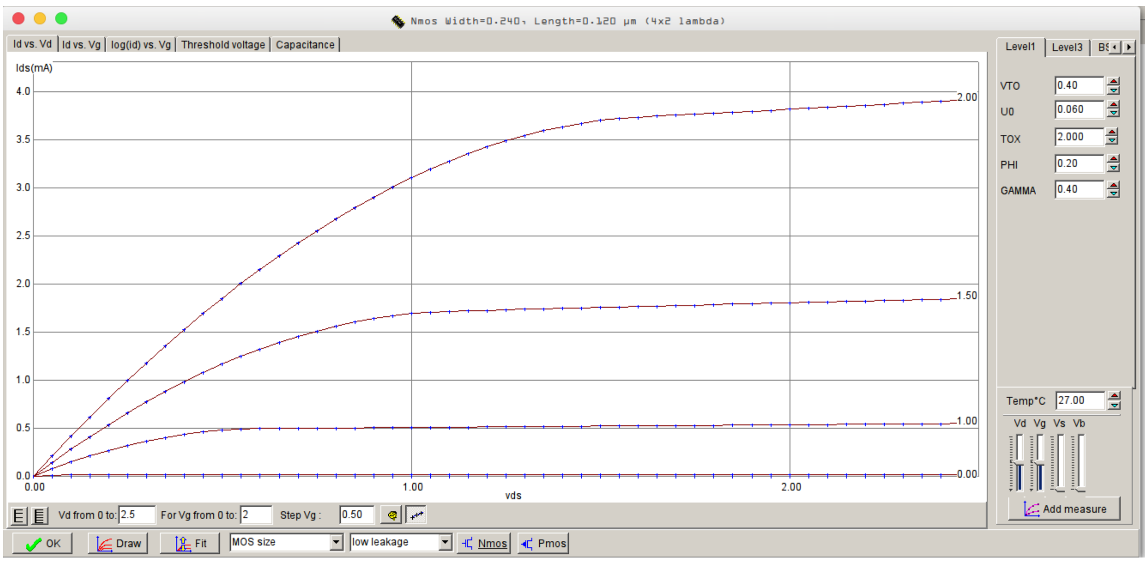

Fig 2: Microwind generated nMOS characteristics curve

Conclusion: The characteristics curve of nMOS from manually calculated values of I_{DS} doesn't vary significantly from automatically generated characteristics curve using Micro-wind. Micro-wind being a simulation software can include several influencing factor while plotting the characteristics curve.