**Experiment No:** 01

**Experiment Name:** Design and Verification of Full Adder, 4-bit Parallel Adder and Carry Look Ahead Adder.

**Objectives:**

(i)Designing and logical verification of the Full adder. Making the full adder block. And verifying them in DSCH2 and Microwind

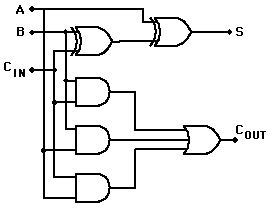
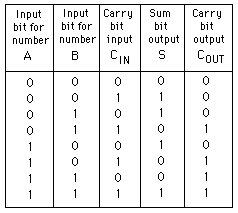
(ii)Designing and logic verification of 4-bit parallel Adders(Ripple Carry Adder) and verifying them in DSCH2 and Microwind

(iii) Designing and logic verification of Carry Look Ahead Adder and verifying them in DSCH2 and Microwind

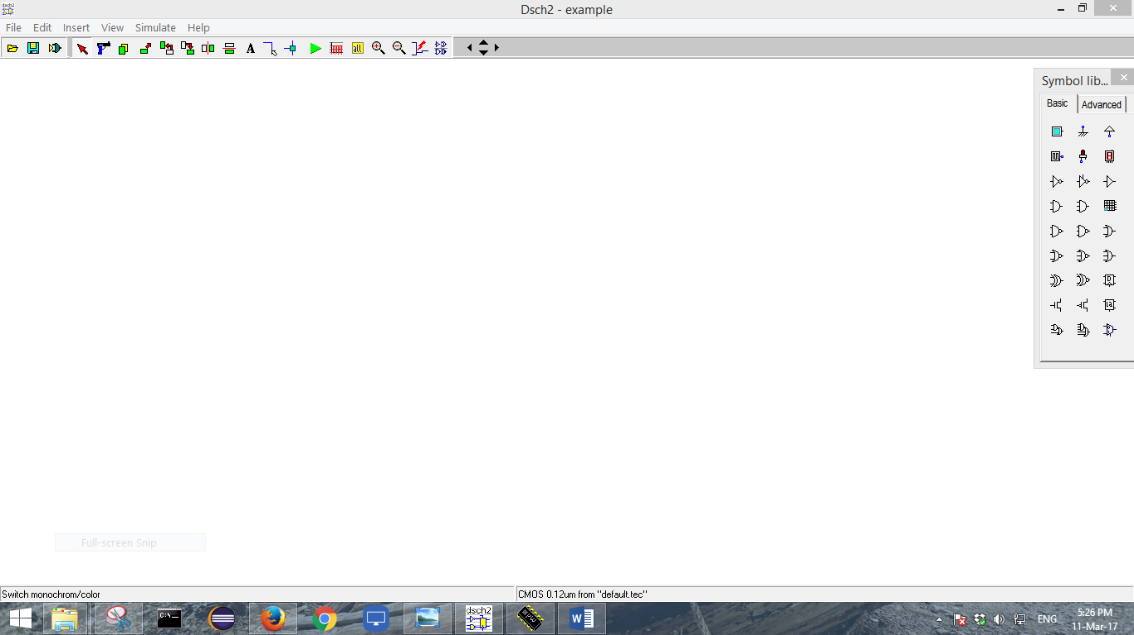
**Procedure:**

**Task-1:** Designing A Full Adder

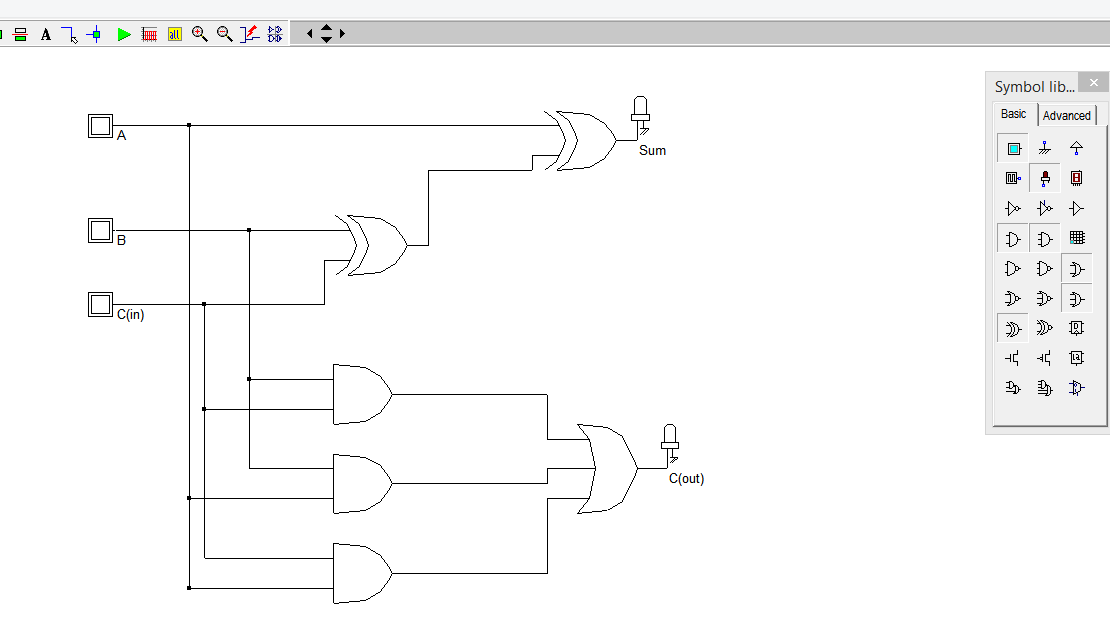
The Schematic Diagram and Truth Table of Full Adder is given below :

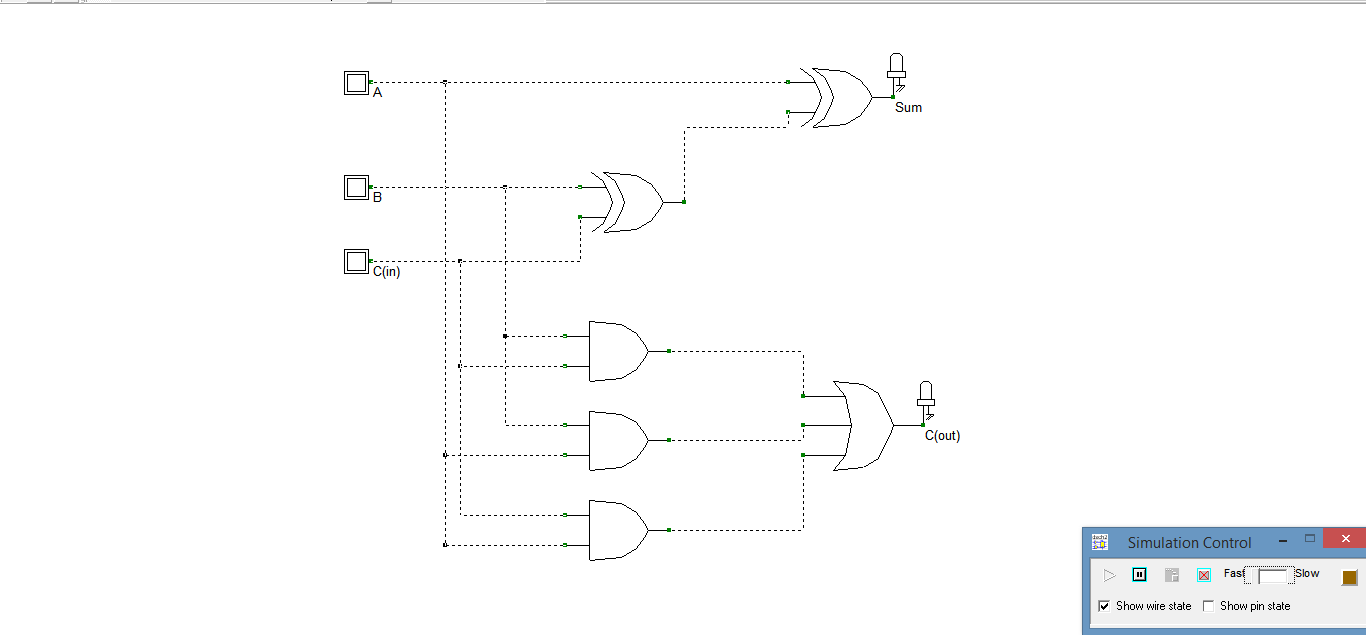
Now we should open the DSCH2 software.



Now we should take 2 Ex-Or gates , 3 And Gates and an OR gate. Then we should also take 3 inputs and two outputs one for sum and another for carry from rightmost panel and connect them with wire to make the full adder circuit. The circuit should look like this:



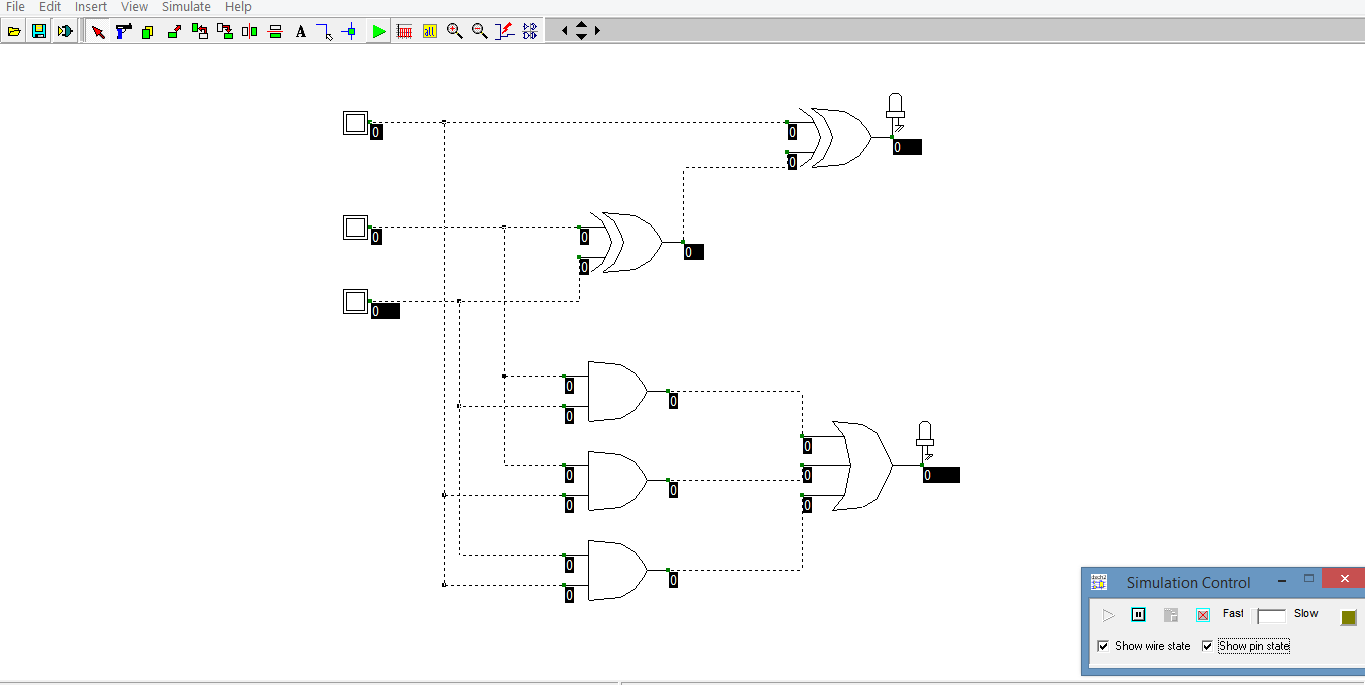
Now we should check the Floating Lines and then we will start simulation. When we simulate we see a simulation control panel at the right bottom. From the panel we should mark the show pin state option. It will show us the state of each and every pin.



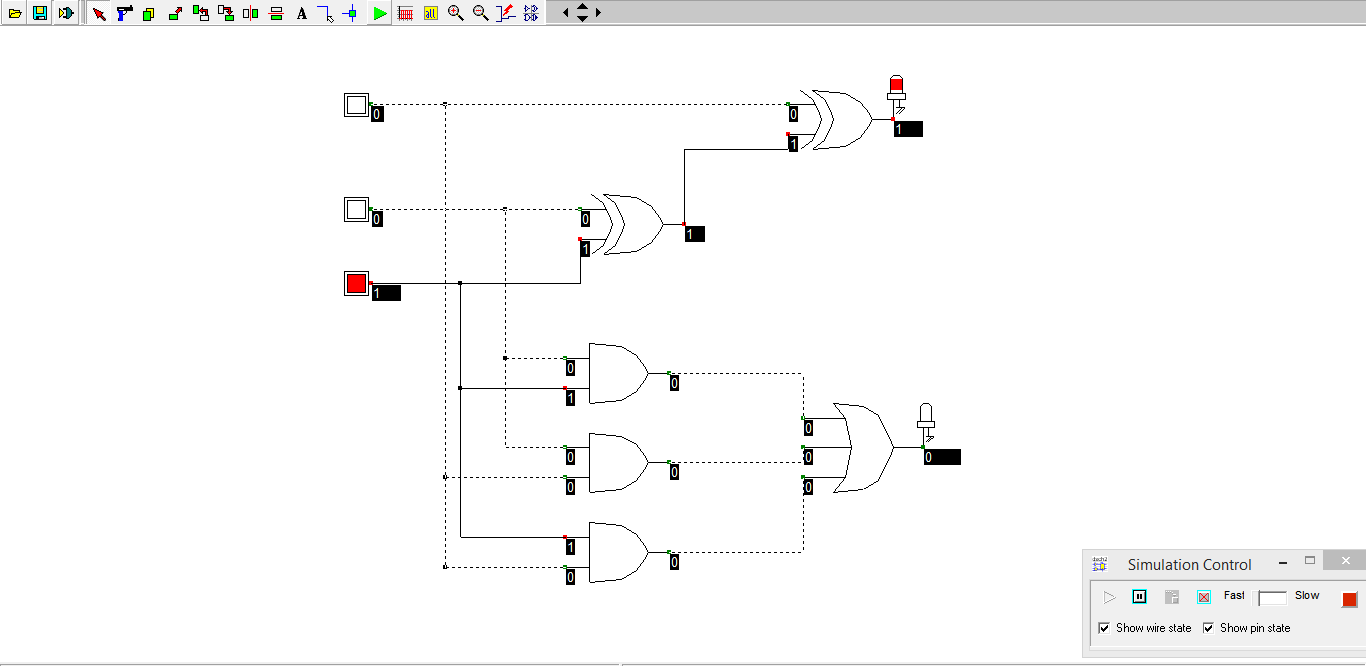
Now we should change the inputs of the circuit by pressing the buttons A and B and C(in).

The different outputs are :

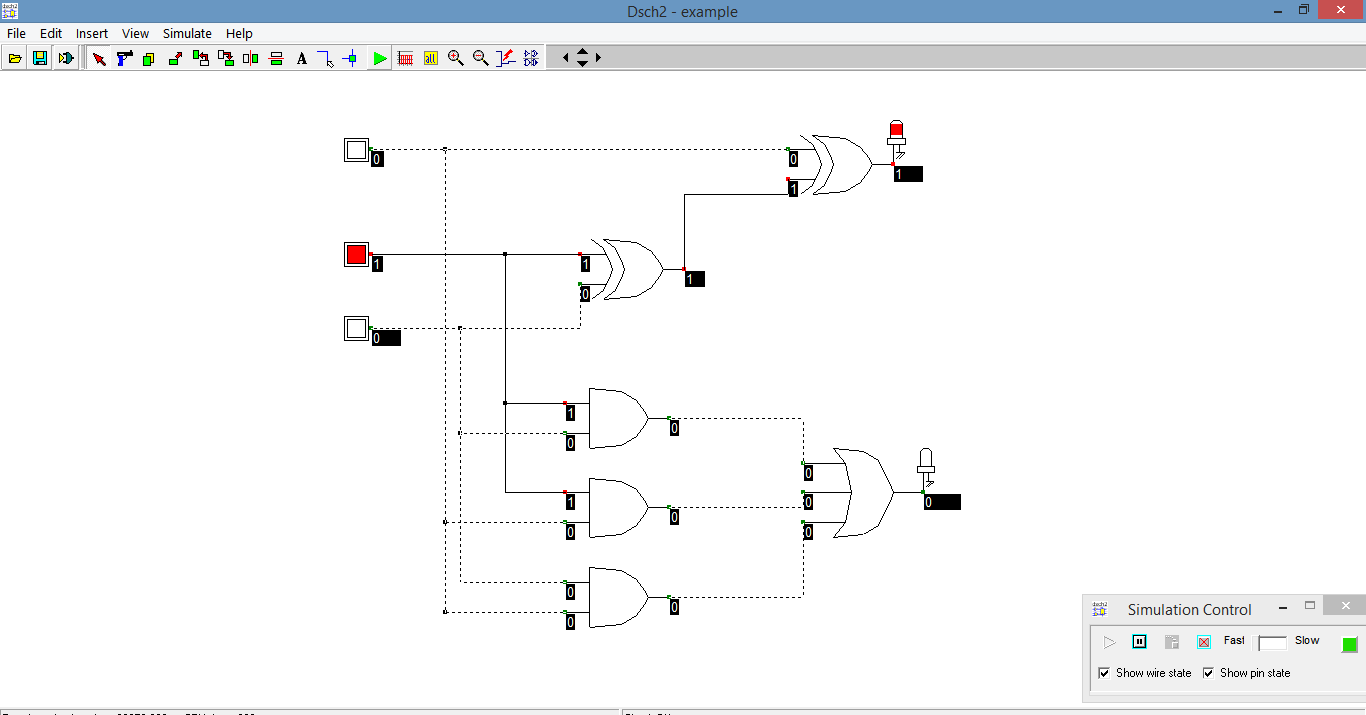
For A=0 and B=0 and C(in)=0



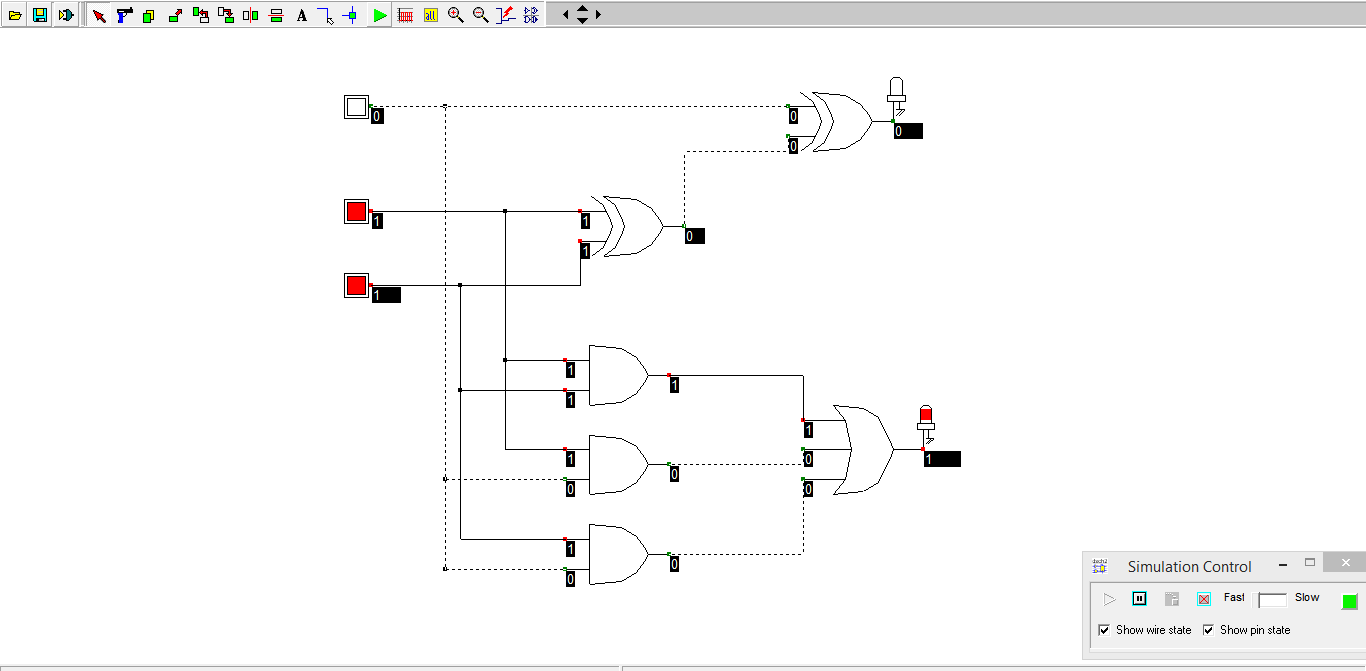
For A=0,B=0,C(in)=1



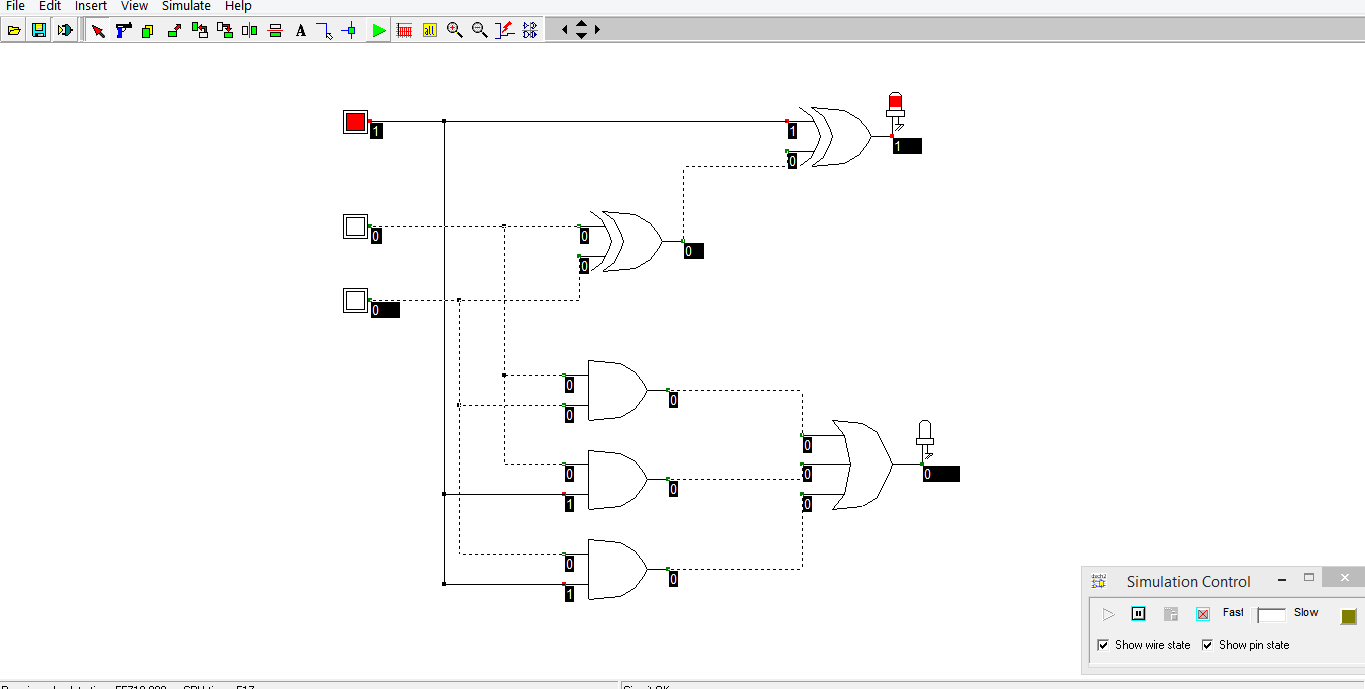
For A=0,B=1,C(in)=0



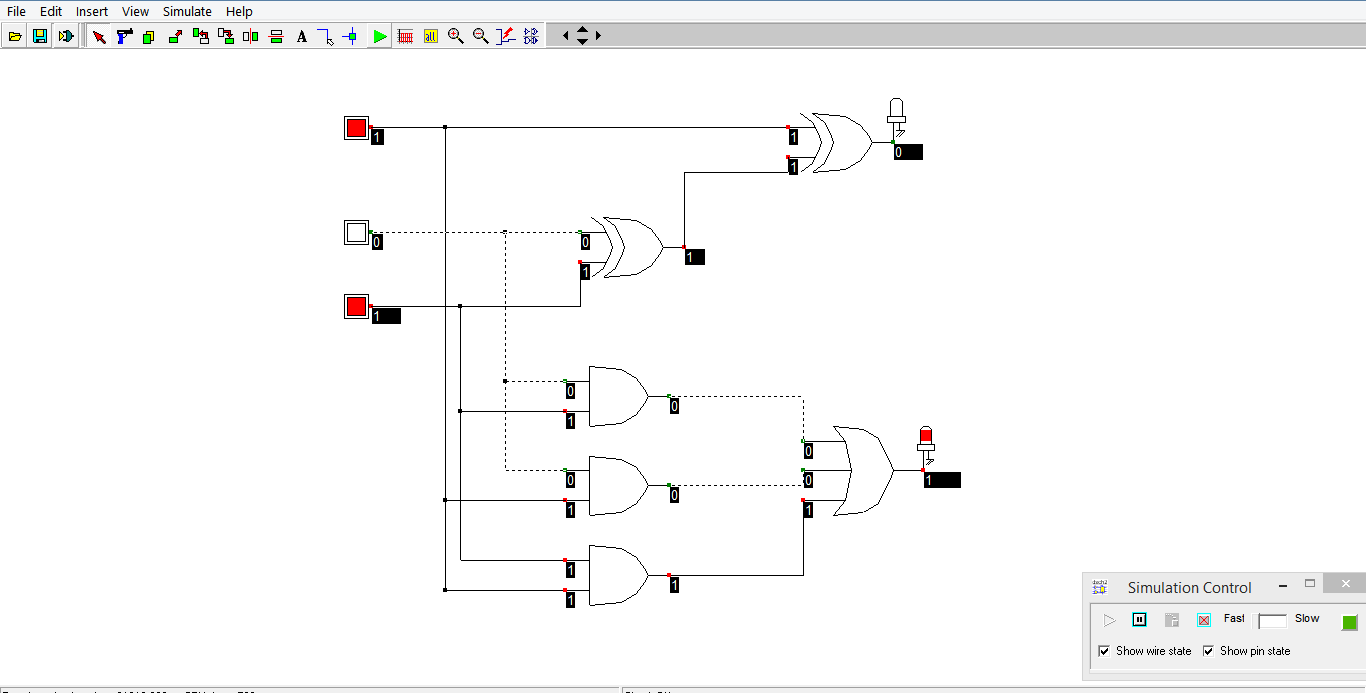
For A=0,B=1,C(in)=1



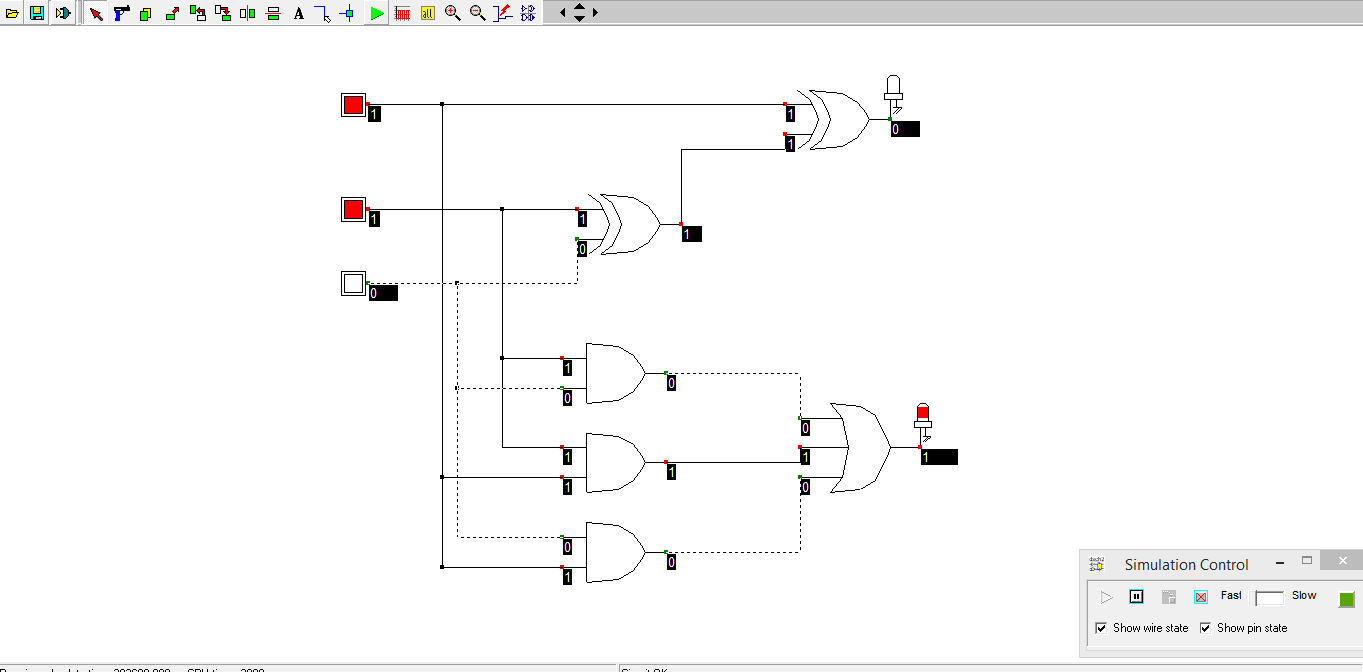
For A=1,B=0,C(in)=0



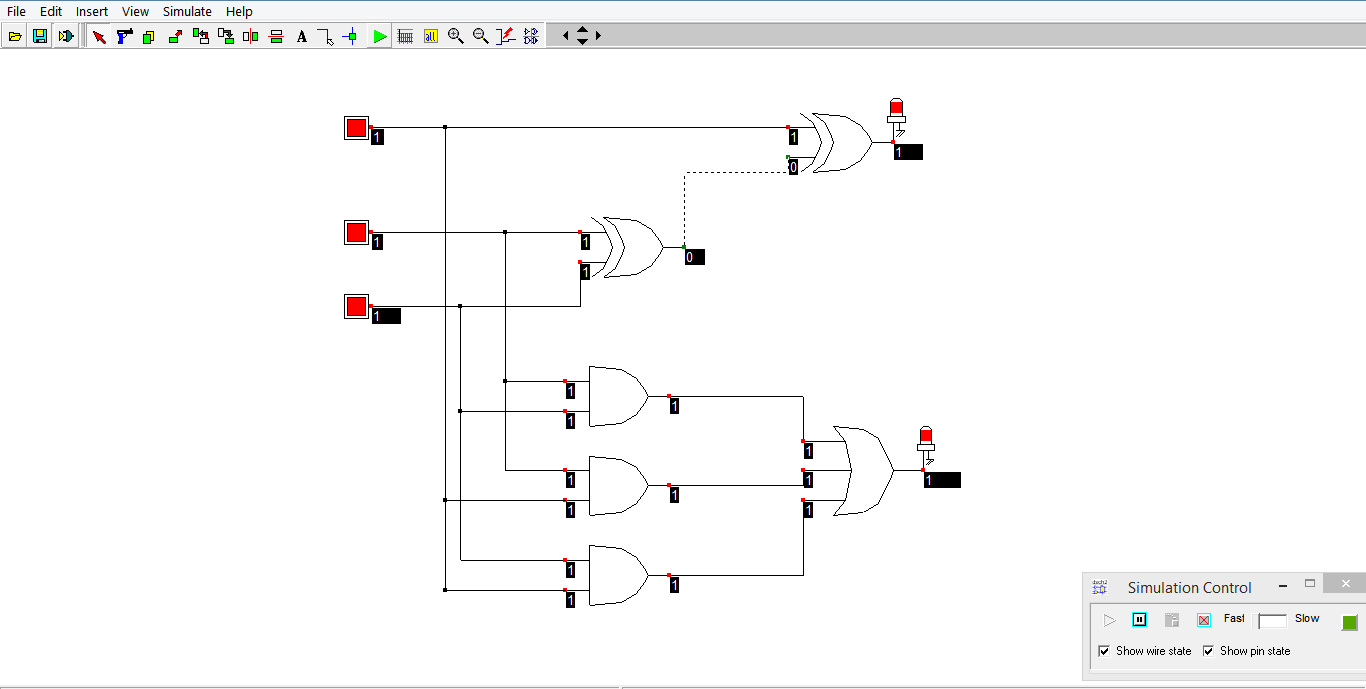
For A=1,B=0,C(in)=1



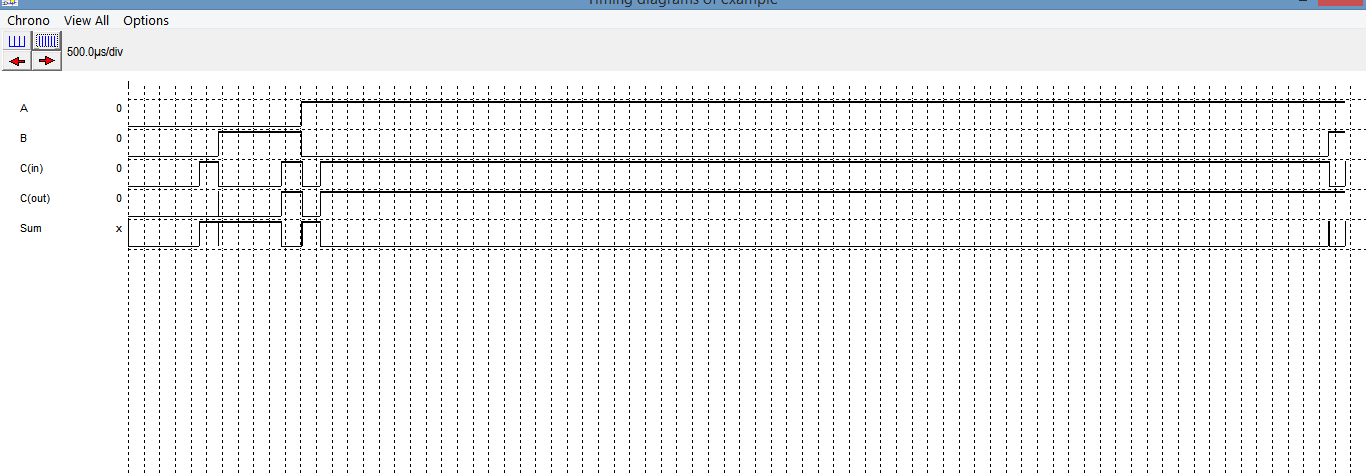
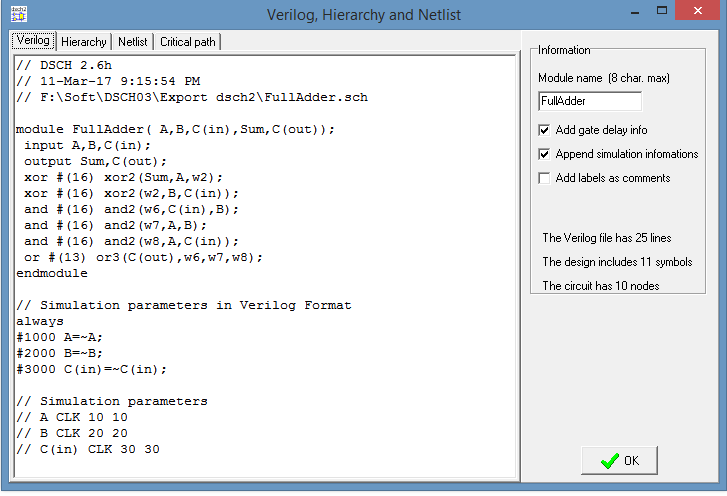
For A=1,B=1,C(in)=0



For A=1,B=1,C(in)=1

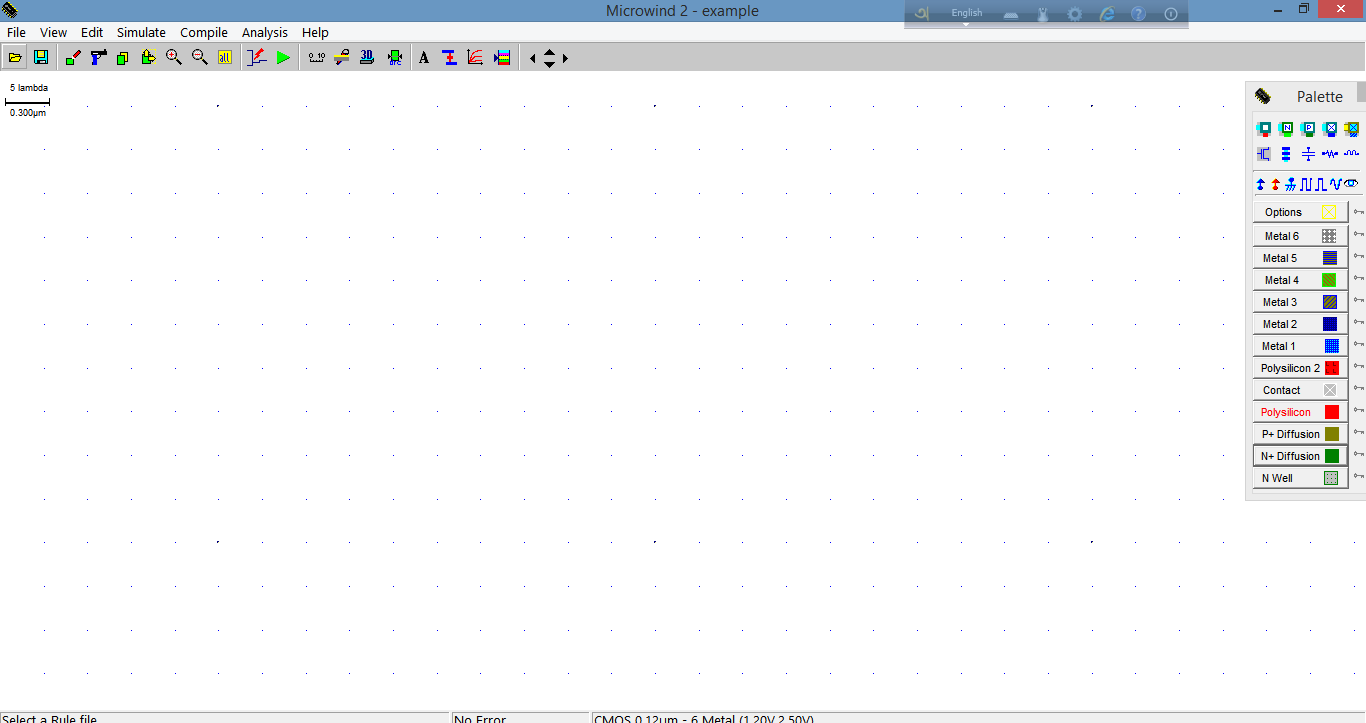


The Timing Diagram of the Simulation is given below:

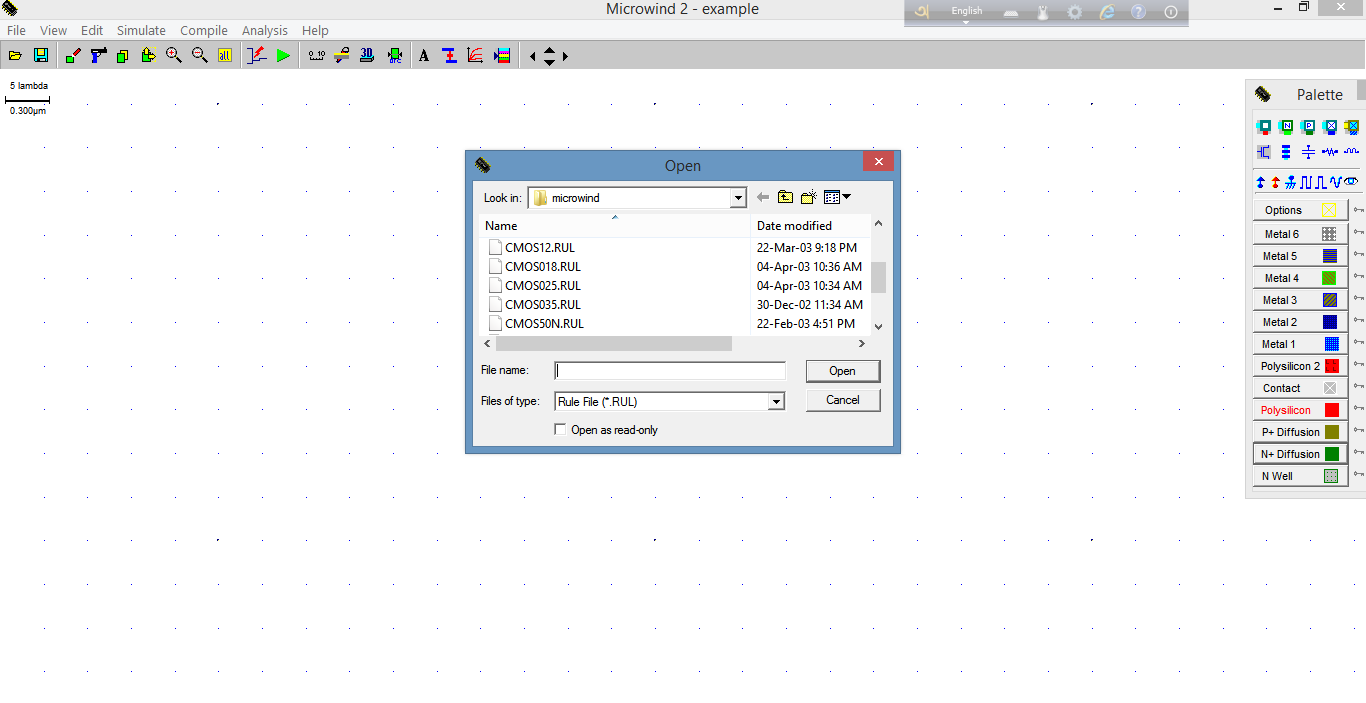
Then we should open the DSCH2 software and open the Full Adder that we have simulated before.Then we should go to file and select Make Verilog File .

Then we should click OK and it will create a Verilog file with .txt extension in the current location of the previous program.

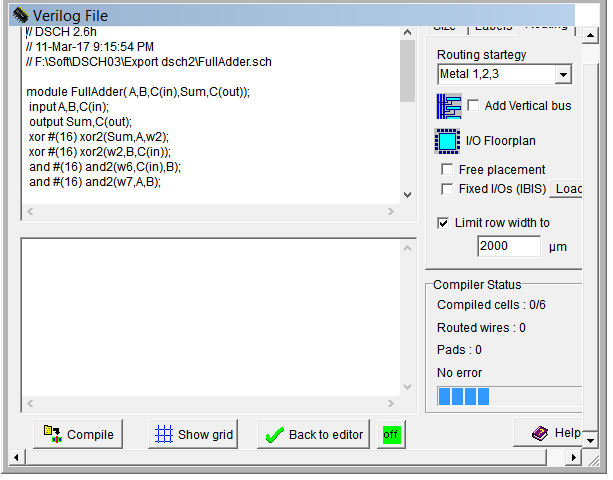
Then we should open the Microwind software.



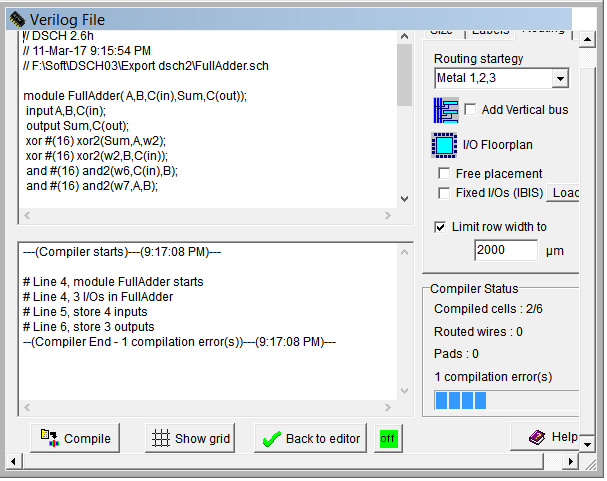
After opening it we should go to file, click the Select Foundary, and select CMOS025.RUL



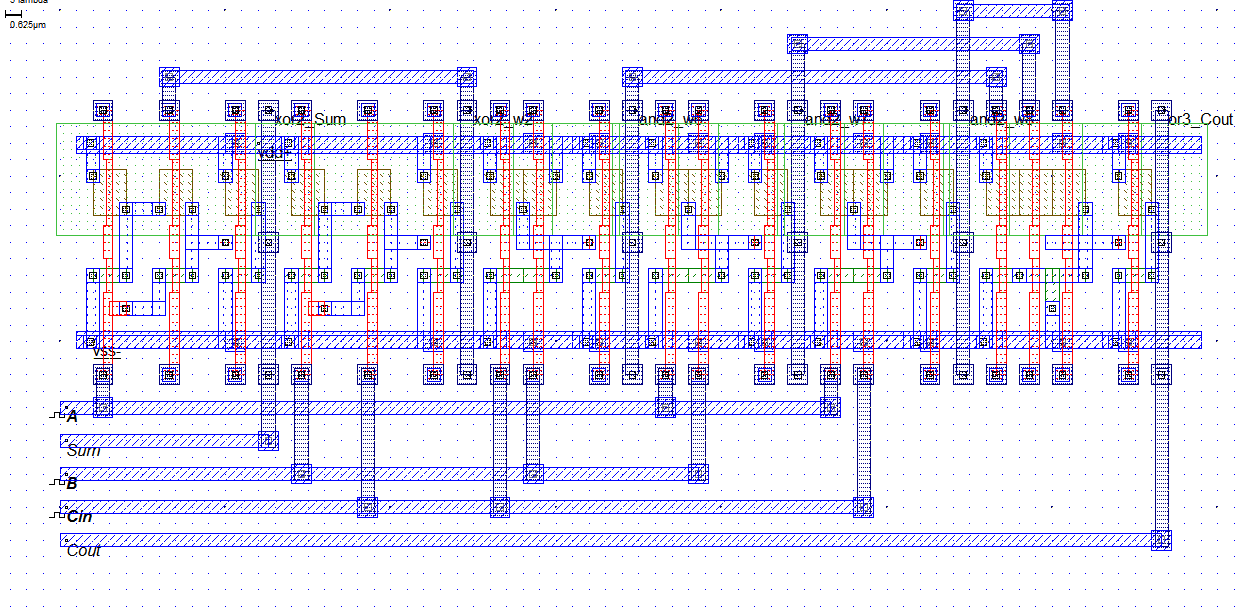
Then we should click on compile and select compile Verilog file, and then click on the file which has been generated before and then we should see the panel below:



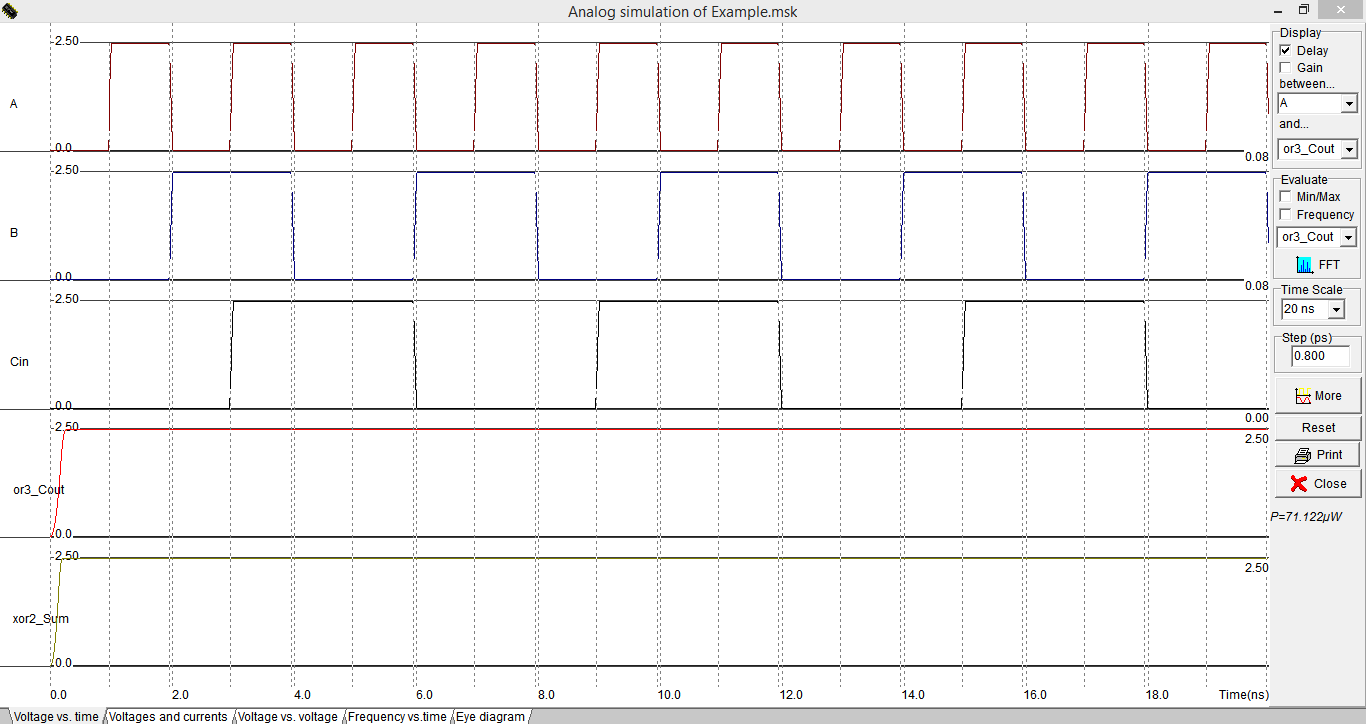
Then we should click the button compile and we should get an message , of successfully compilation.



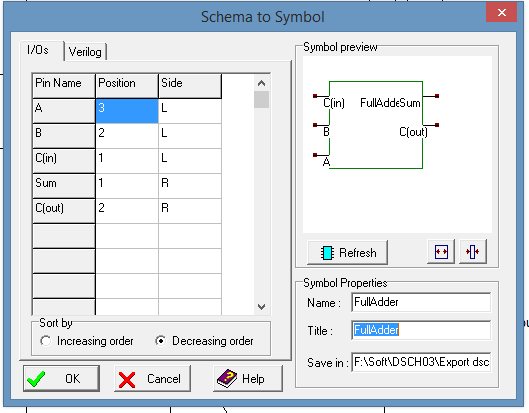
And then we get a layout design of the Full Adder.



The Timing Diagram is given below:



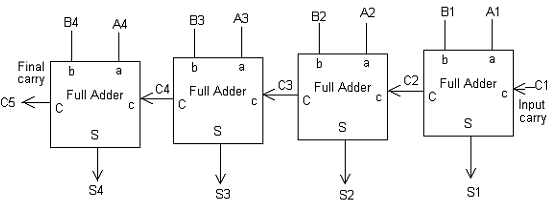
Now we should make the block of Full Adder by clicking schema to new symbol in DSCH2.



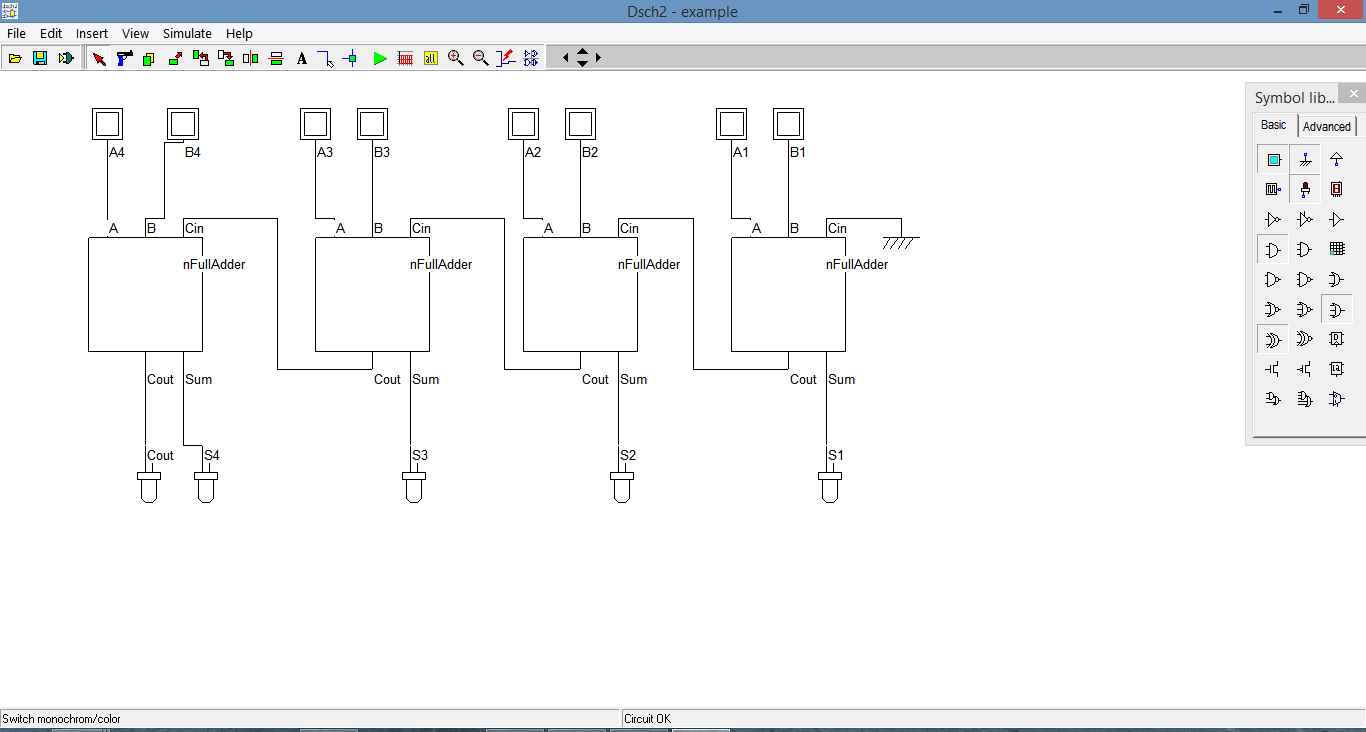
And make the block of Full Adder.

**Task-2:** Designing A 4-bit Parallel Adder(Ripple Carry Adder)

The schematic diagram of 4-bit parallel adder is given below:

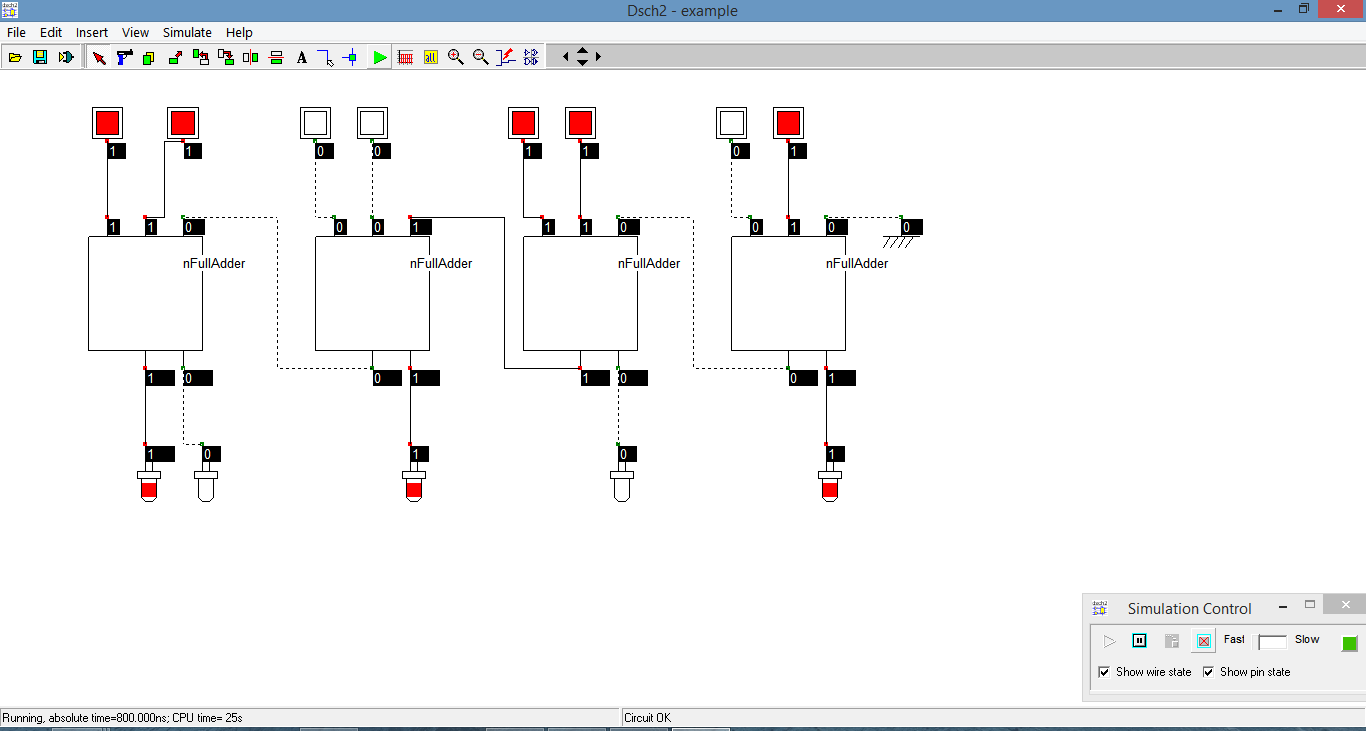


First We should open the DSCH2 software and click ‘insert’ then ‘user symbol’. And select the Full Adder that we have built in the first task. We should take 4 full adders ,8 inputs and 5 outputs. We should connect the carry of an adder to the C(in) of the next adder. The Carry of the last adder should be connected with an output and the C(in) of the first adder should be grounded. The circuit is given below:

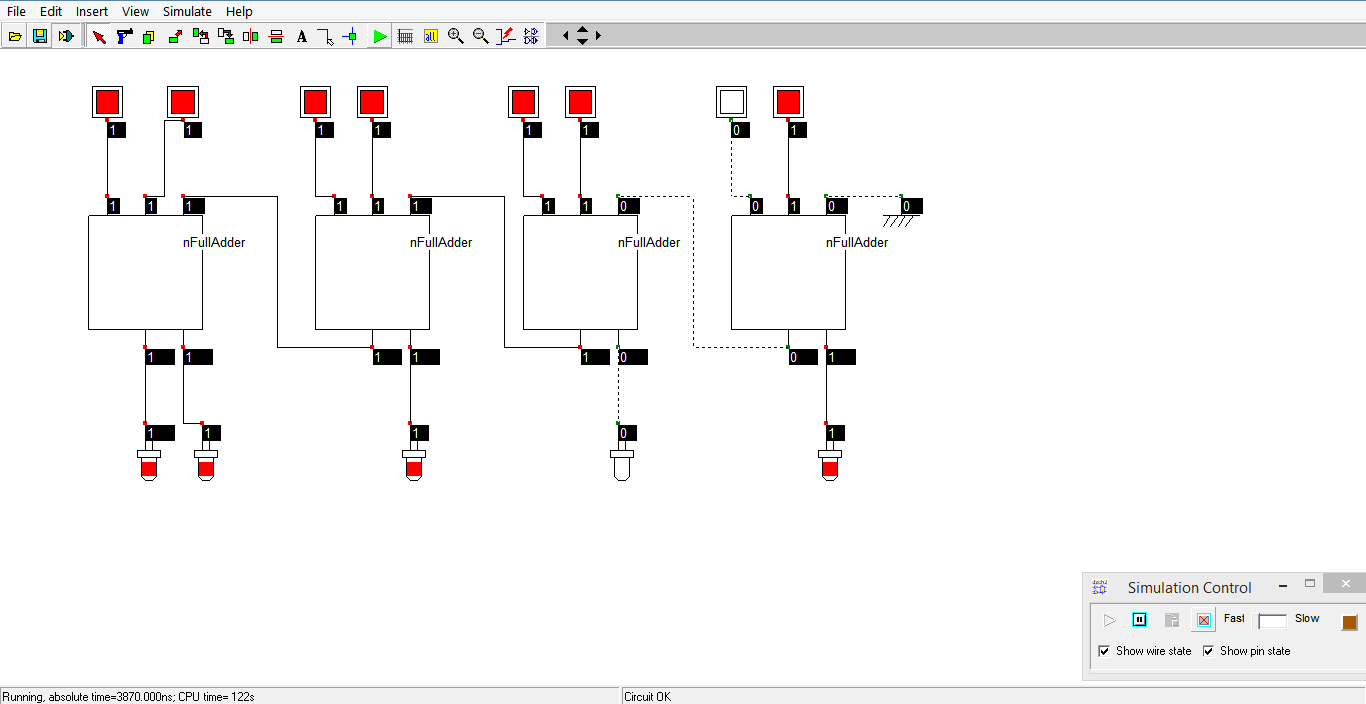


Now we should check the Floating Lines and then we will start simulation. When we simulate we see a simulation control panel at the right bottom. From the panel we should mark the show pin state option. It will show us the state of each and every pin. And Then we should give different inputs to find different Outputs.

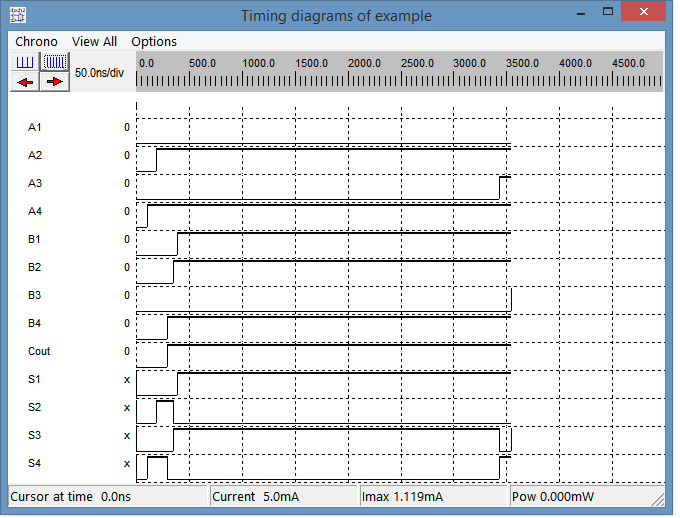
Output for A1A2A3A4=1010 and B1B2B3B4=1011



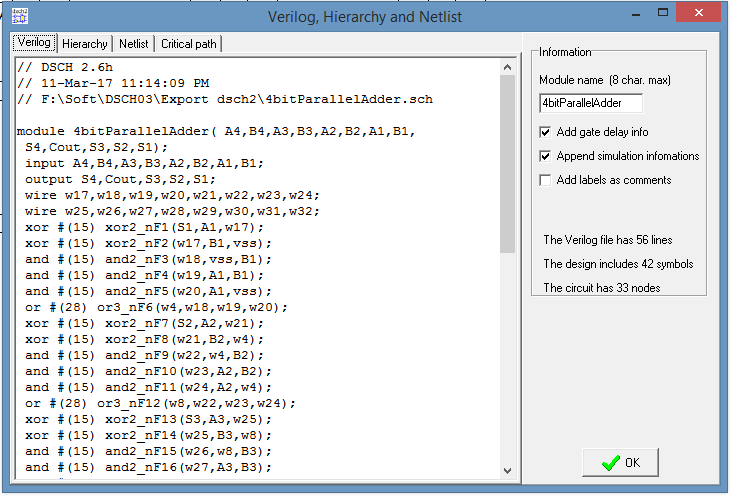
Output for A1A2A3A4=1110 and B1B2B3B4=1111



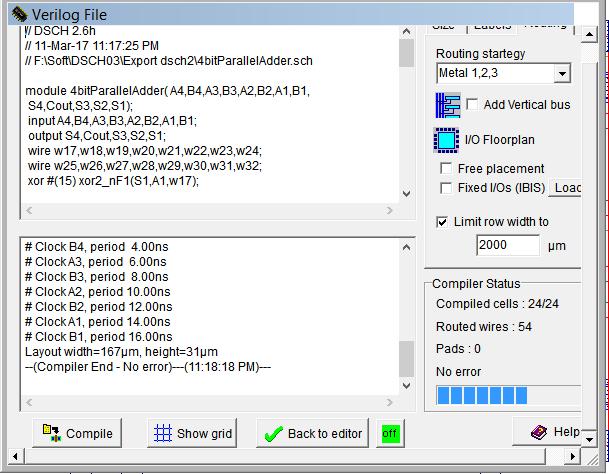
The Timing Diagram is Given Below :



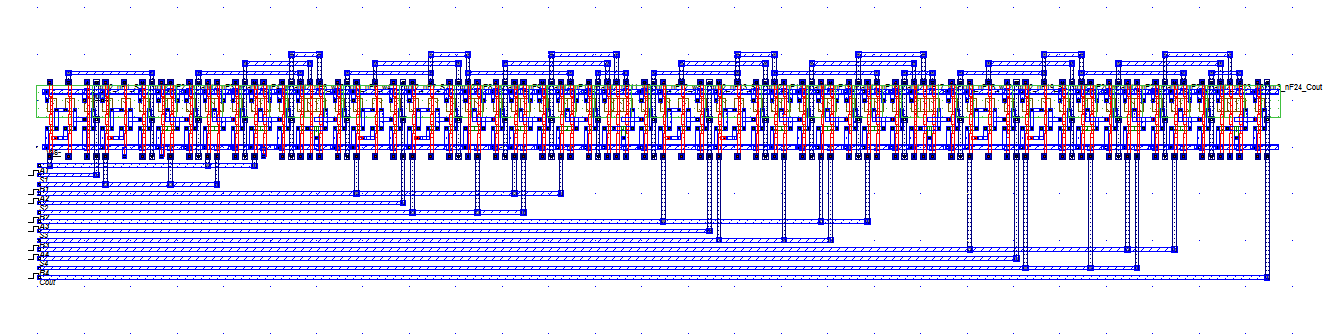
Then we should make Verilog file of the 4-bit Parallel Adder.



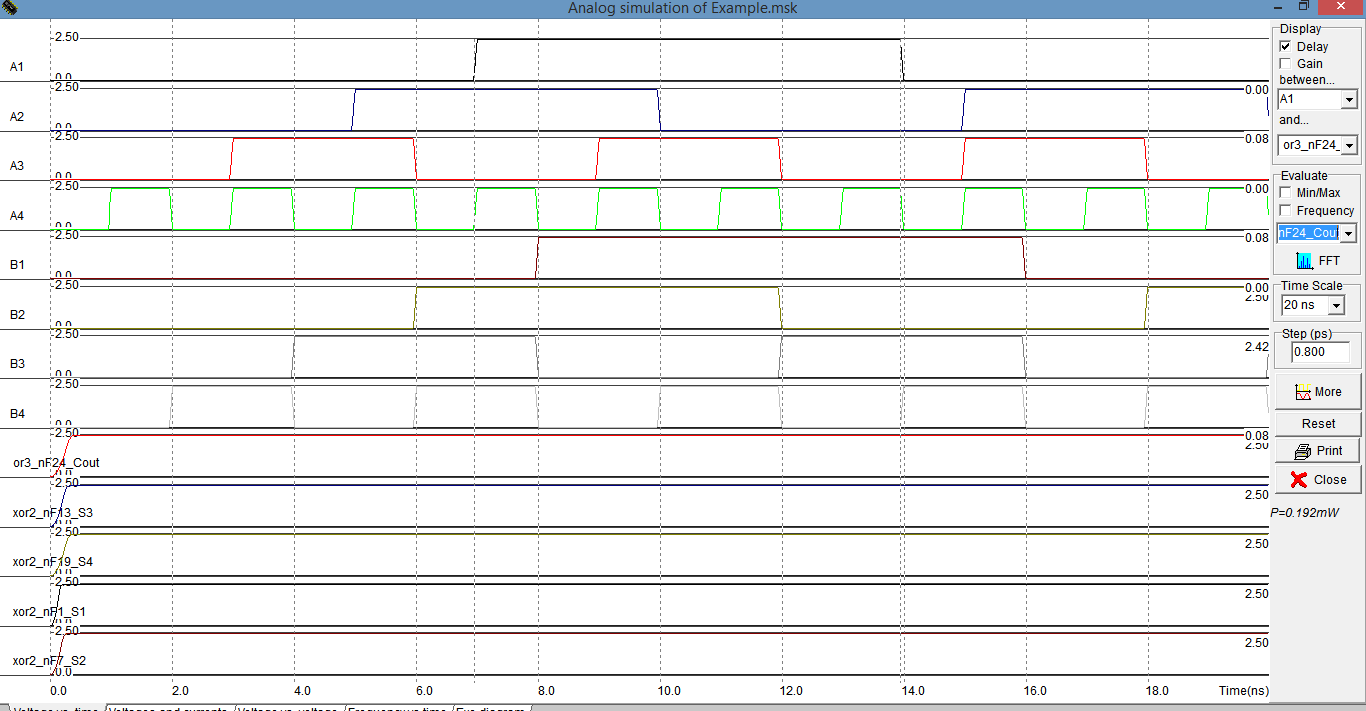
And then should we open the microwind software and compile the Verilog file .



The Layer diagram of the 4bit parallel adder is given below:



The Timing Diagram is given below:



**Result:**

In all the cases the , the Timing Diagrams are checked and verified.