**Experiment No:** 02

**Experiment Name:** Design and Implementation of CMOS NAND gate.

**Objectives:**

(i)Designing and logic verification of CMOS NAND gate using DSCH2.

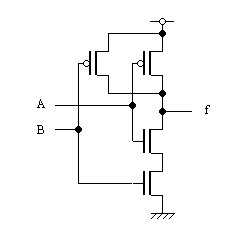
(ii)Designing and logic verification of CMOS NAND gate using Microwind.

(iii)Showing Timing Diagrams.

**Procedure:**

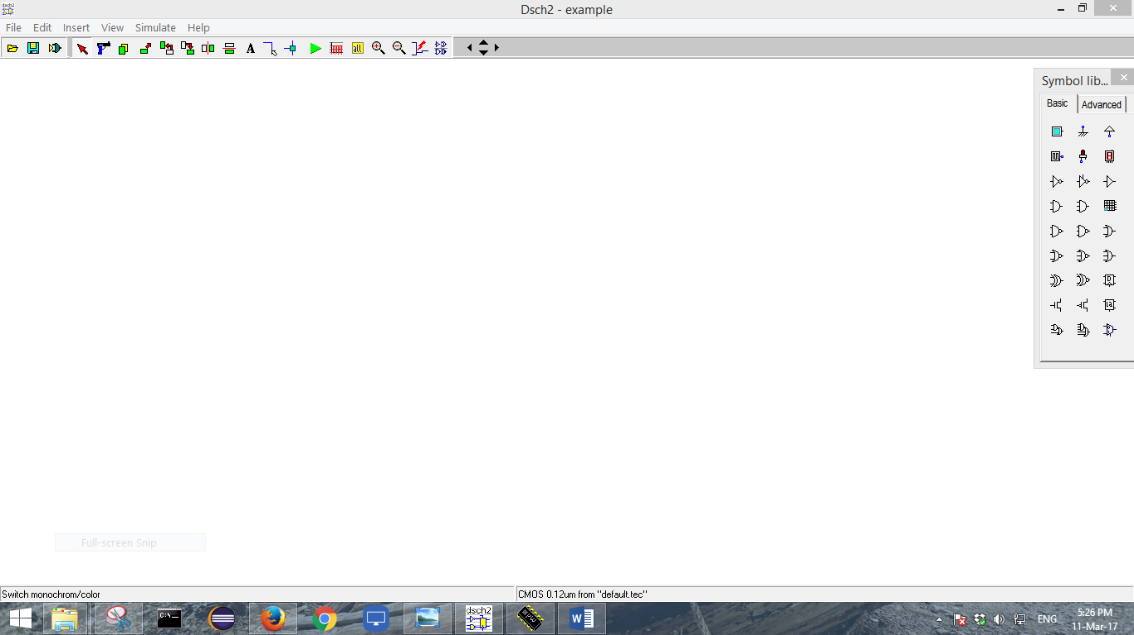
(i)Designing and logic Verification of CMOS NAND gate using DSCH2.

The Schematic Diagram and Truth Table of NAND Gate is given below :



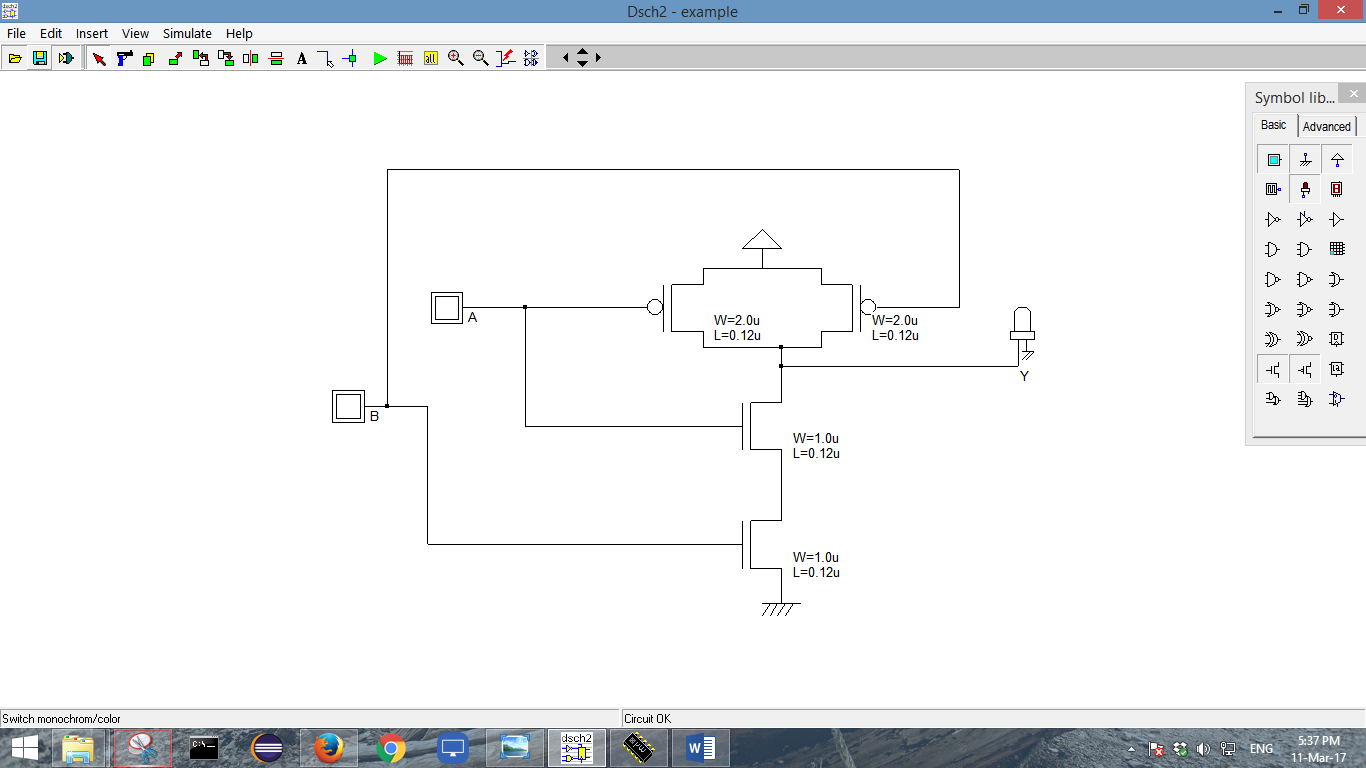
|  |  |  |
| --- | --- | --- |
| A | B | f |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Now we should open the DSCH2 software.

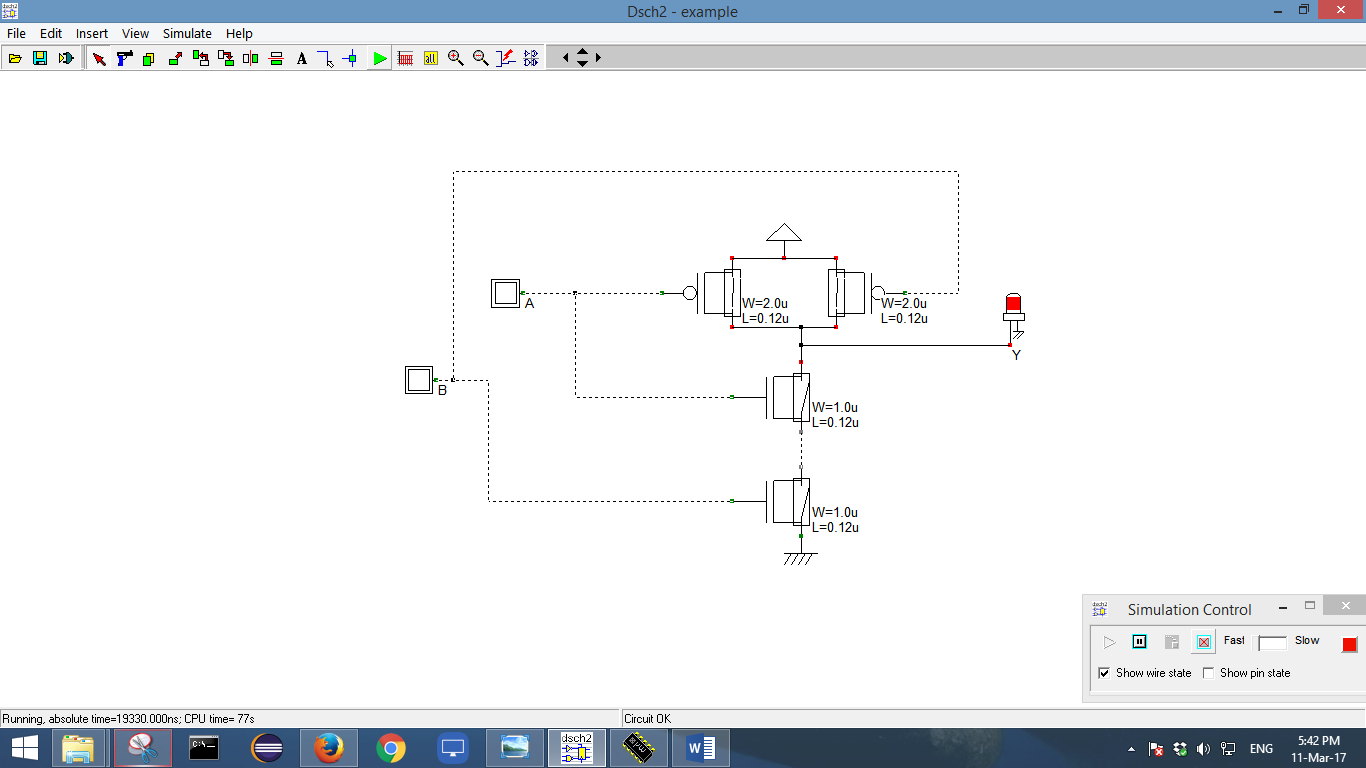


Now we should take the PMOS and NMOS circuits from the option bar of the left side. Then we should draw the circuit diagram of CMOS by drag and dropping.

The circuit should look like this:



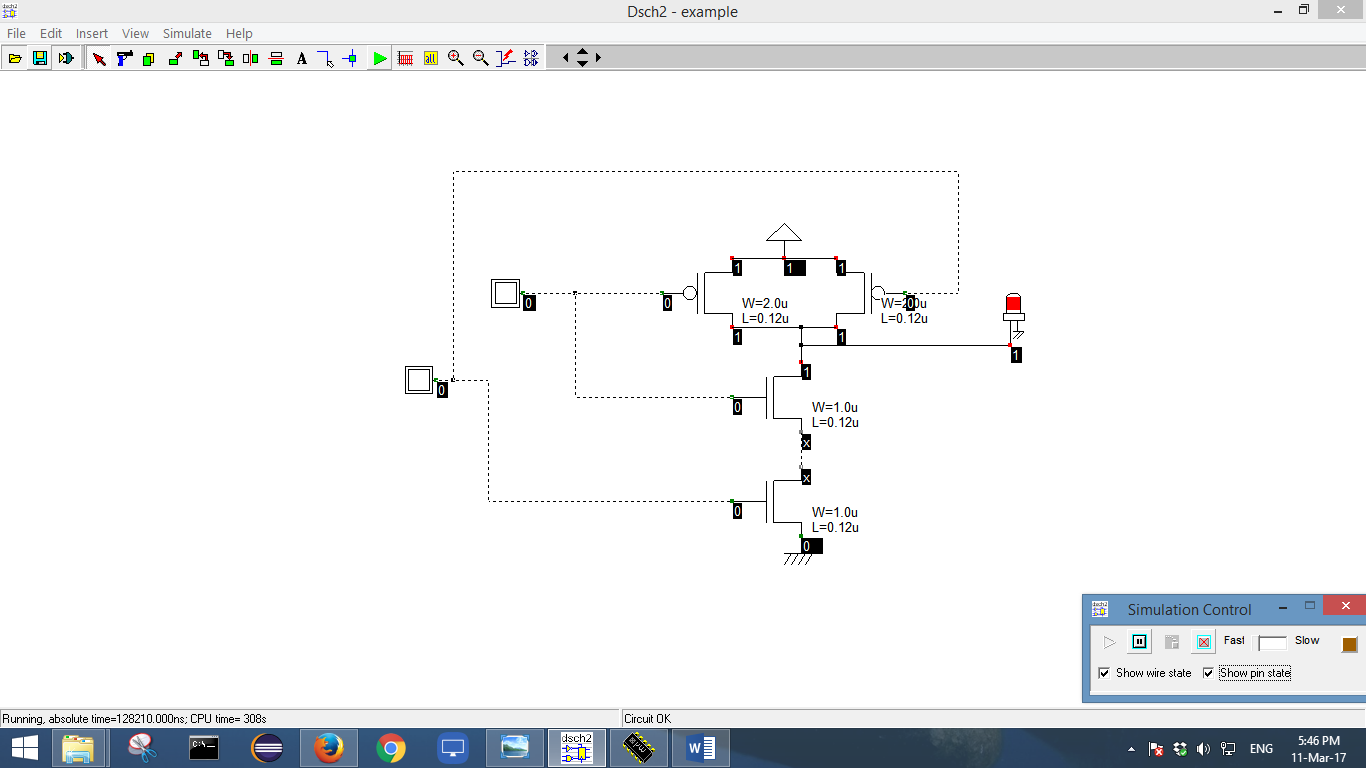
Now we should chck the Floating Lines and then we will start simulation. When we simulate we see a simulation control panel at the right bottom. From the panel we should mark the show pin state option. It will show us the state of each and every pin.



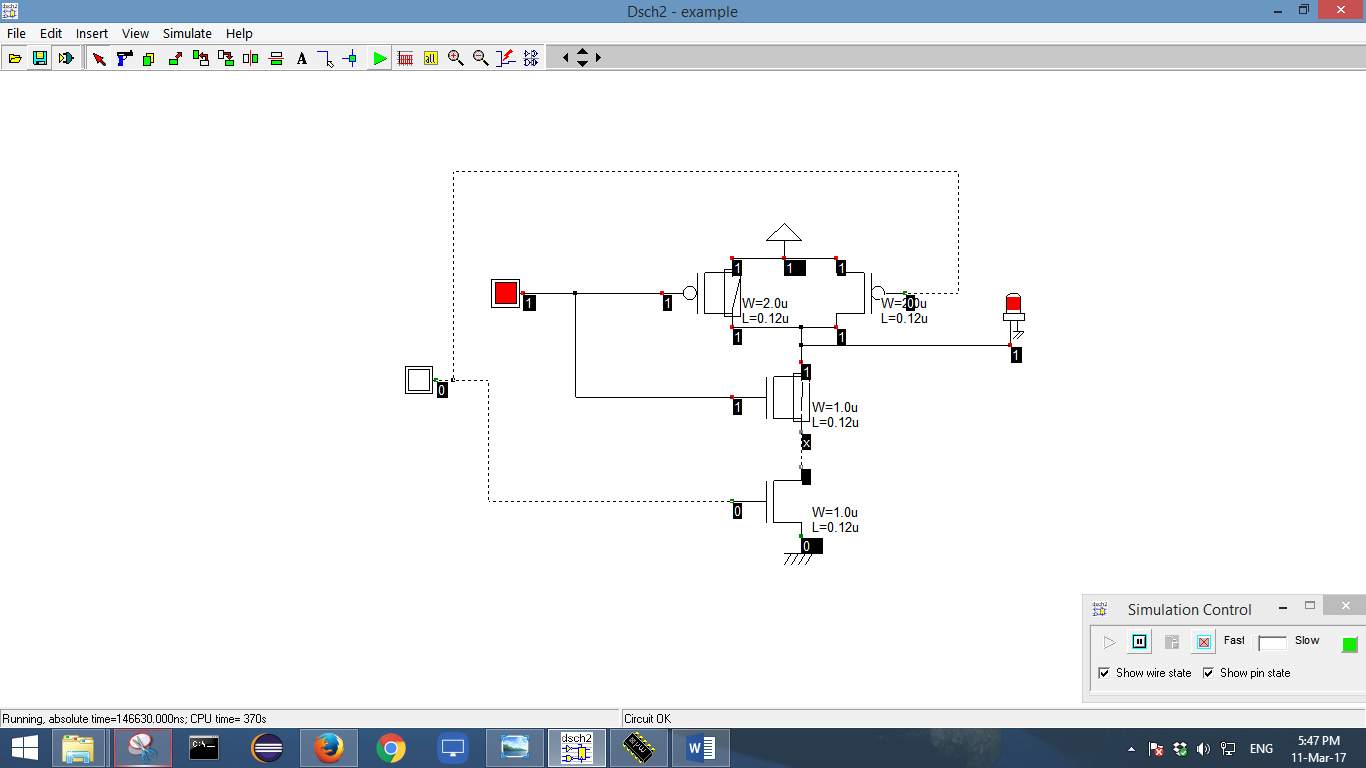
Now we should change the inputs of the circuit by pressing the buttons A and B.

The different outputs are :

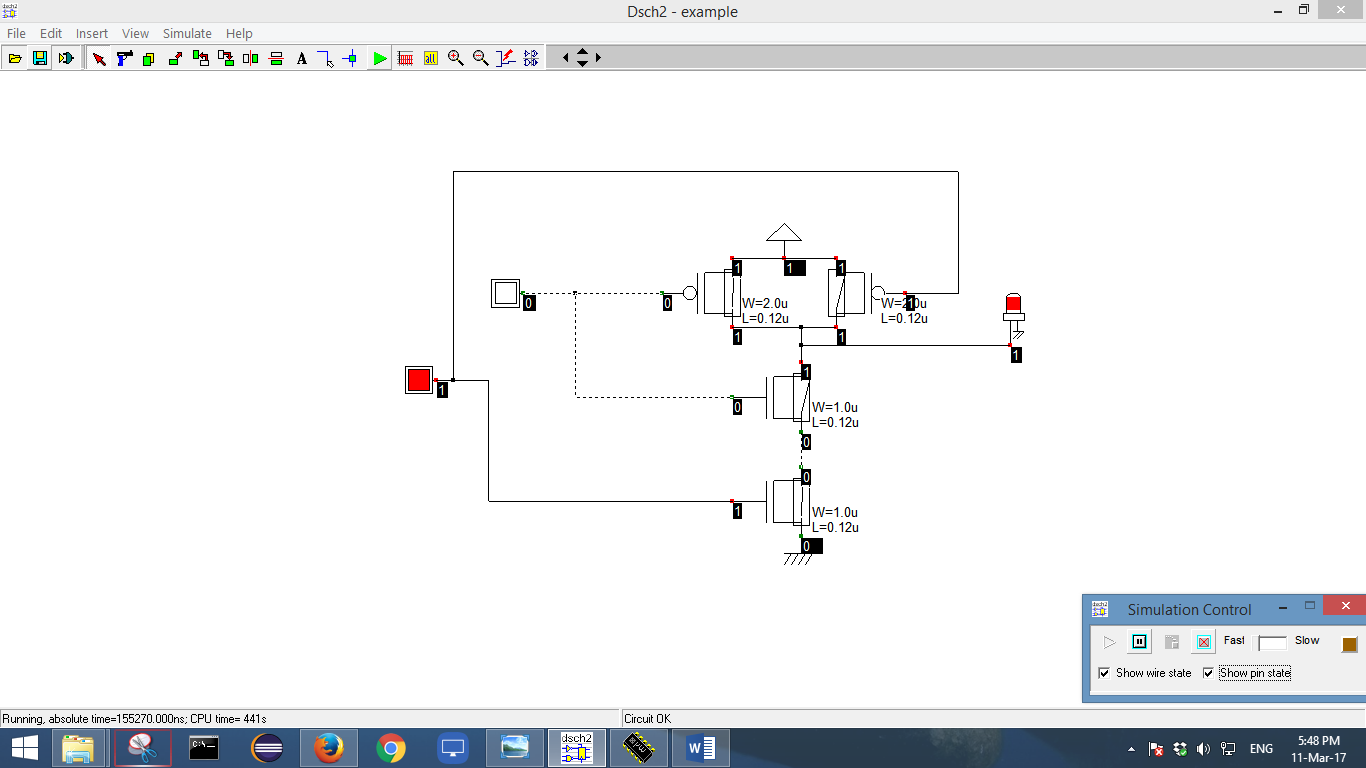
For A=0 and B=0



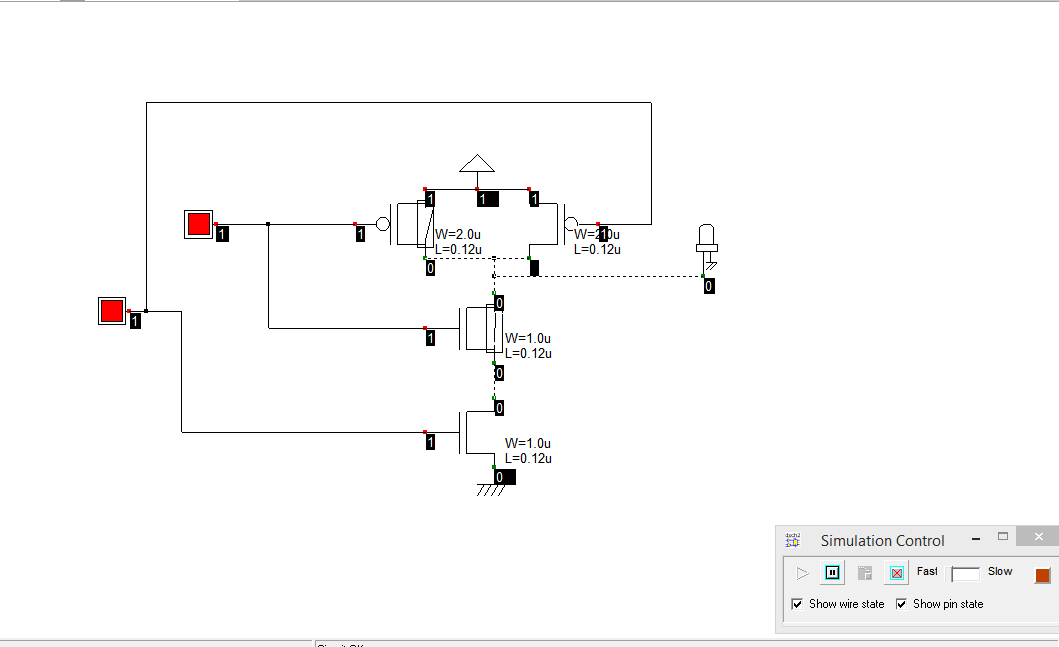
For A=1 and B=0



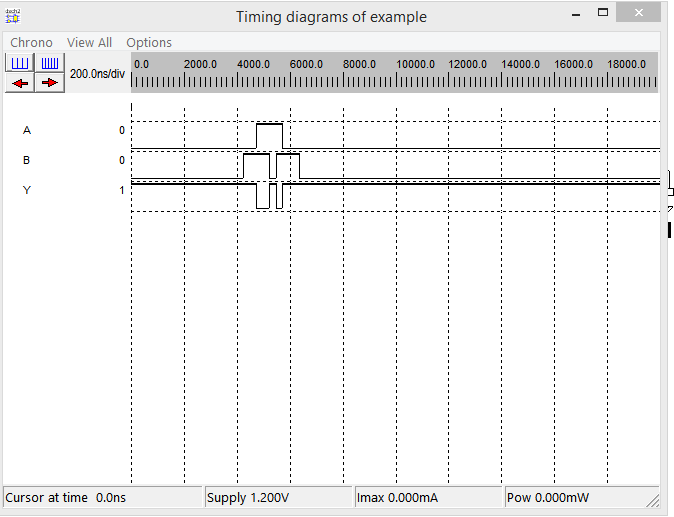
For A=0 and B=1



For A=1 and B=1

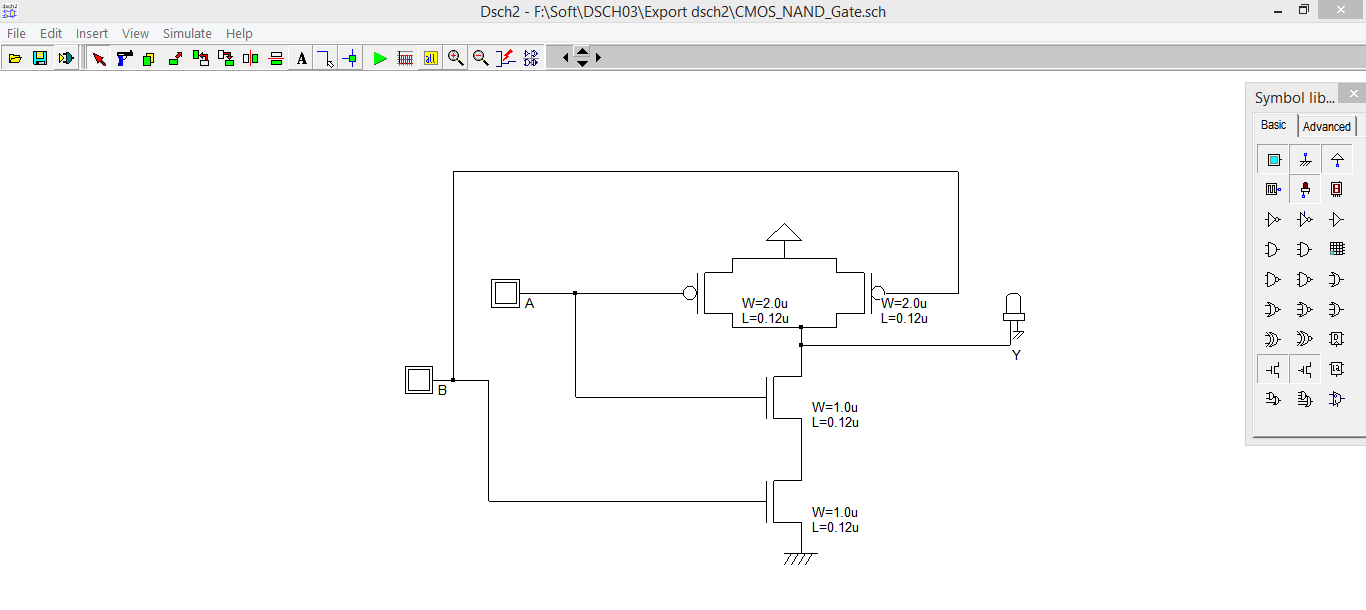


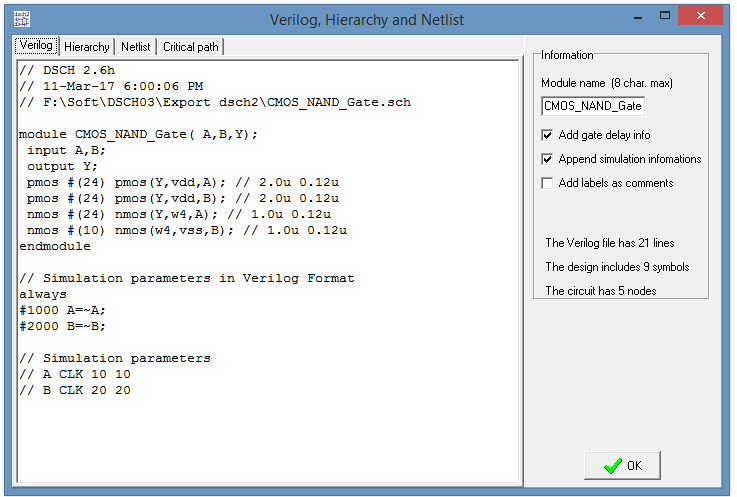
The Timing Diagram of the Simulation is given below:



(ii)Designing and logic Verification of CMOS NAND gatye using Microwind.

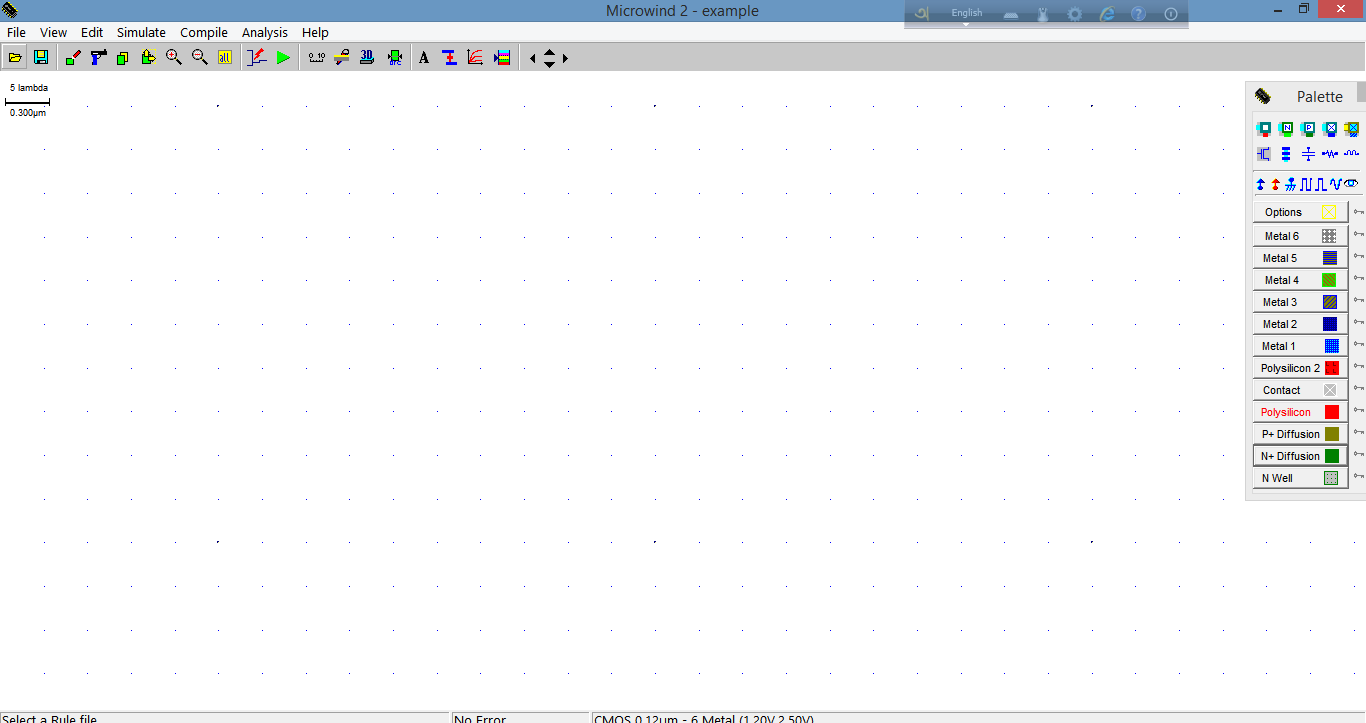
First we should open the DSCH2 software and open the CMOS NAND gate that we have simulated before.



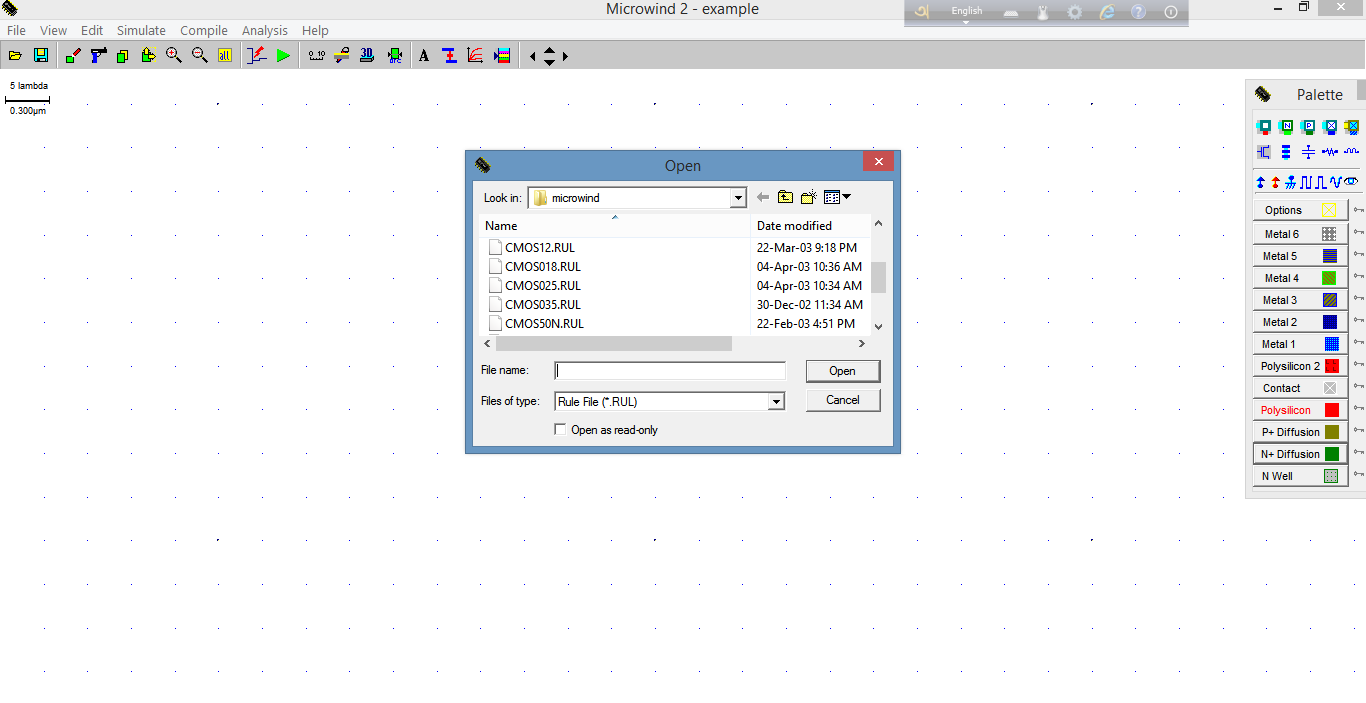
Then we should go to file and select Make Verilog File .

Then we should click OK and it will create a Verilog file with .txt extension in the current location of the previous program.

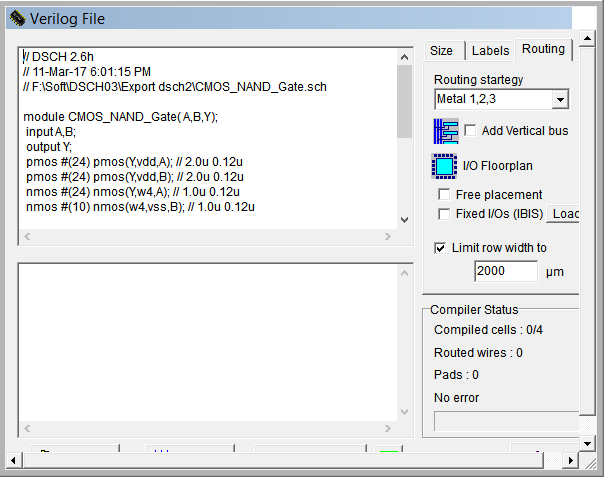
Then we should open the Microwind software.



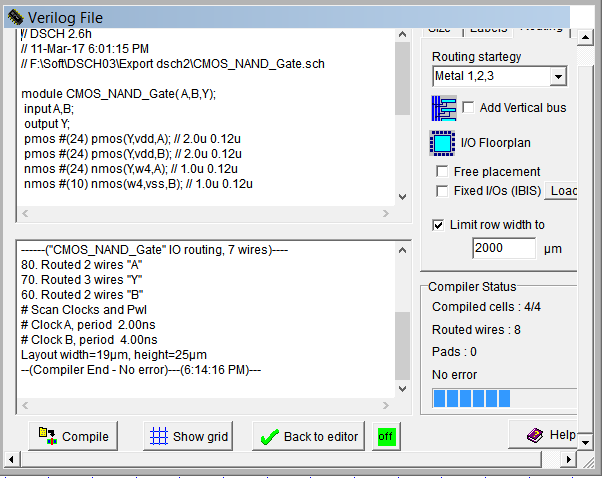
After opening it we should go to file, click the Select Foundary, and select CMOS025.RUL



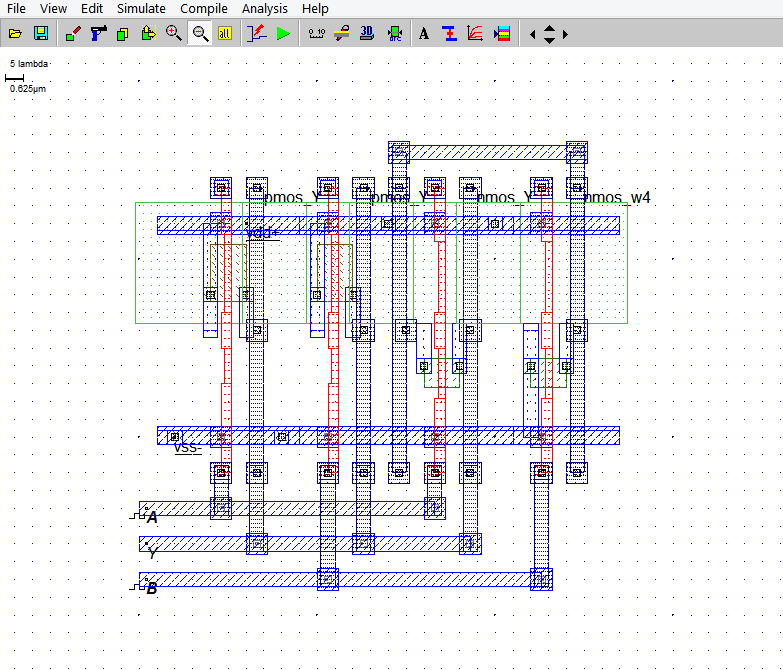
Then we should click on compile and select compile Verilog file, and then click on the file which has been generated before and then we should see the panel below:



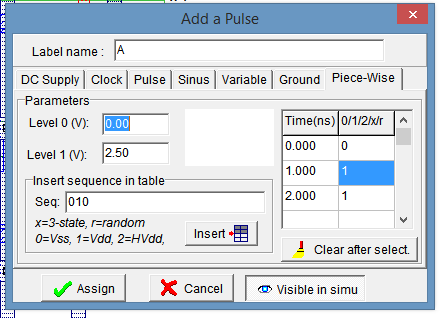
Then we should click the button compile and we should get an message , of successfully compilation.



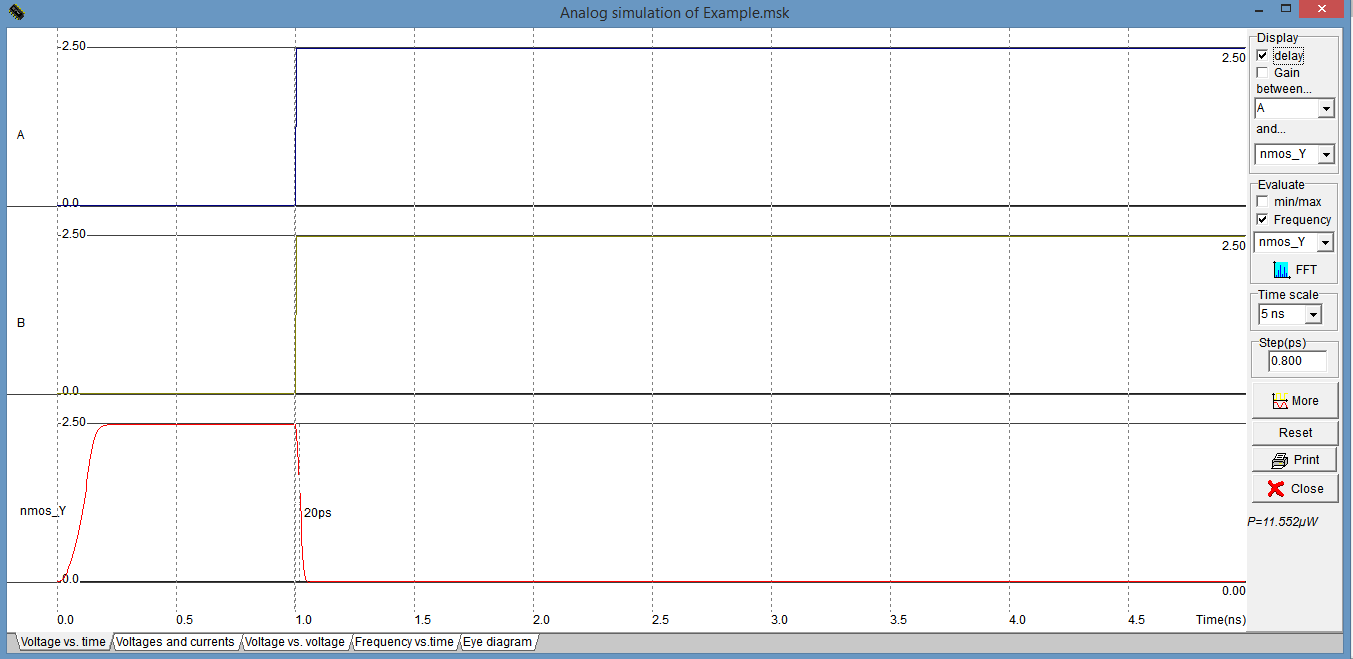
And then we get a layout design of the CMOS NAND.



Now we should click on the input A and assign 01 sequence in piece-wise option. Again we will perform this in the input B.



And finally we should click Run the Simulation and should find the Timing Diagram :



**Result:**

To design the NAND gate we should make sure that the PMOSs are parallely and the NMOSs are serially connected. The Timing Diagram of both DSCH2 and Microwind are also verified.