***Experiment No: 03***

***Experiment Name: (a) Layout design and verification of NAND gate.***

***(b) Layout design and verification of NOR gate.***

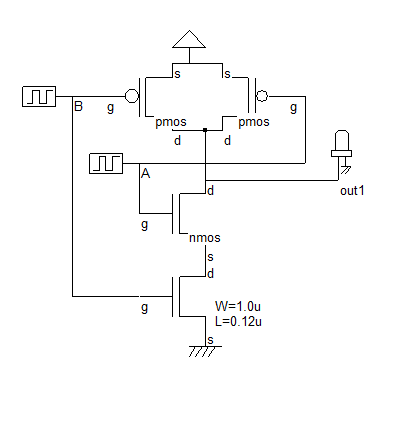
***(a) Layout design and verification of NAND gate.***

# ***State of the Problem***:

*In this experiment work we are going to design the layout of NAND gate. Also we will verify the gates with true table and timing diagram.*

# ***Hypothesis:***

The truth-table and schematic diagram of NAND gate is given below:



|  |  |  |
| --- | --- | --- |
| A | B | OUT |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

*True Table*

*Schematic diagram of NAND*

We will design the layout of NAND gate in ‘MICROWIND2’ software following this diagram.

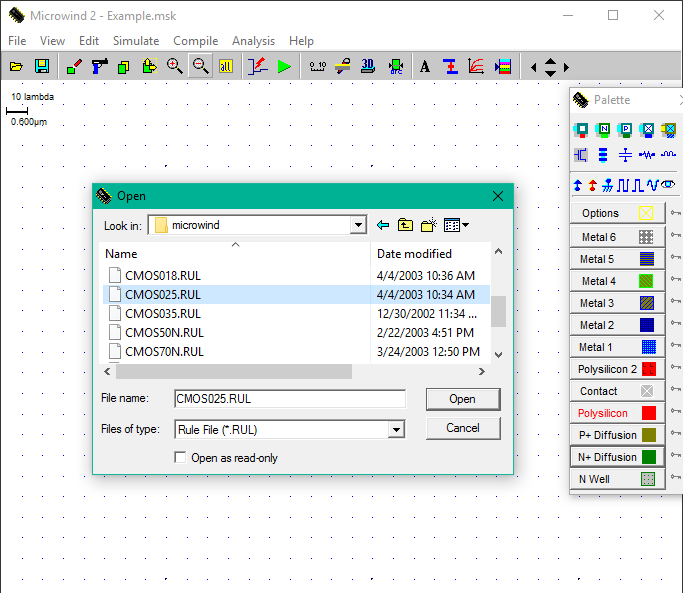
***Materials:***

* MICROWIND2

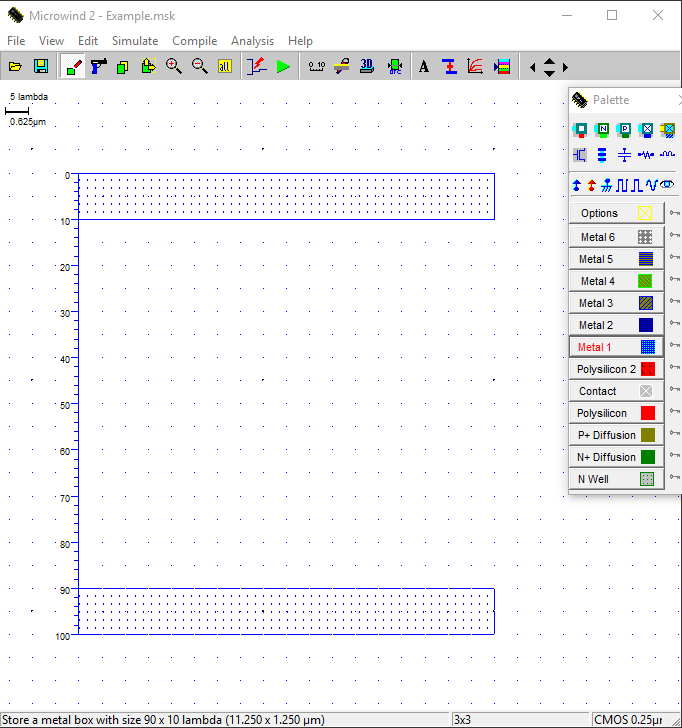
# ***Procedure:***

Here is the working procedure with illustration:

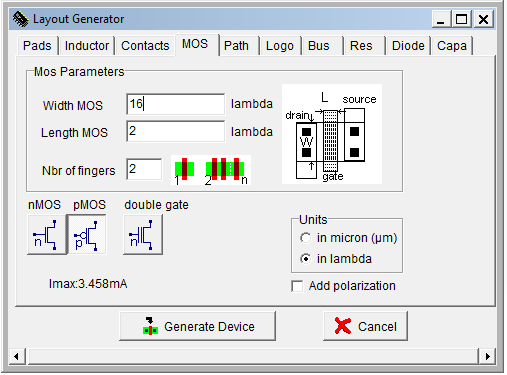
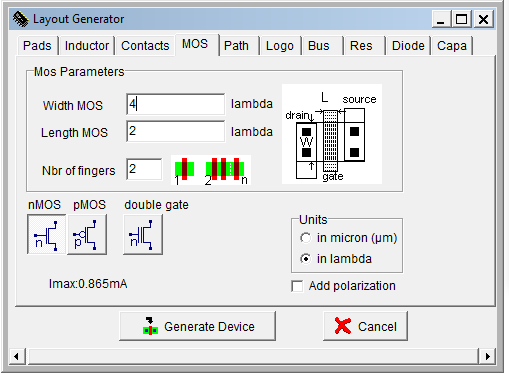
* At first, we open the ‘MICROWIND2’ software and select exact foundry which we needed. Here we use CMOS025.RUL as our foundry. Figure are given below:



* Create Vdd and Vss metal rails as 90\*10 lamda. Top rail as Vdd and bottom as Vss . Figure is given below:

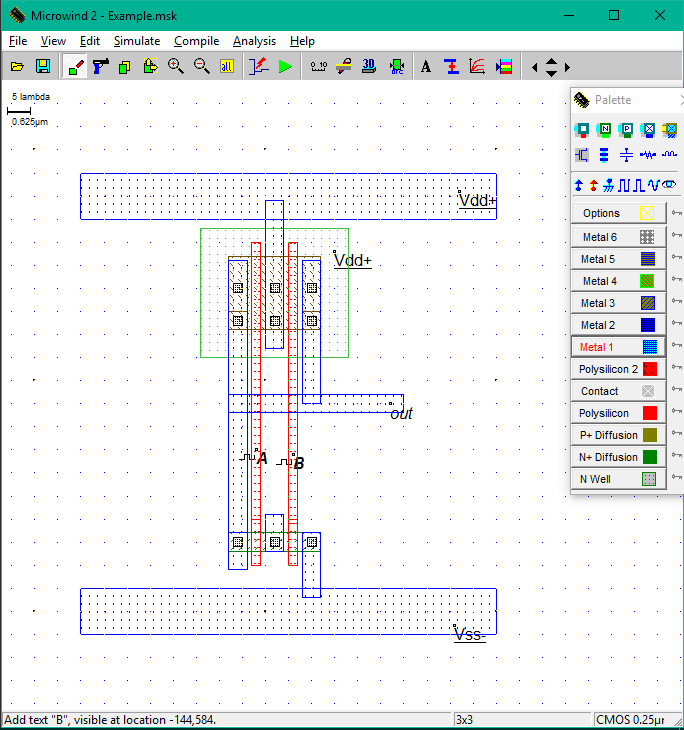


* Generate the nMOS ans pMOS with layout generator. Figures are given bellow:

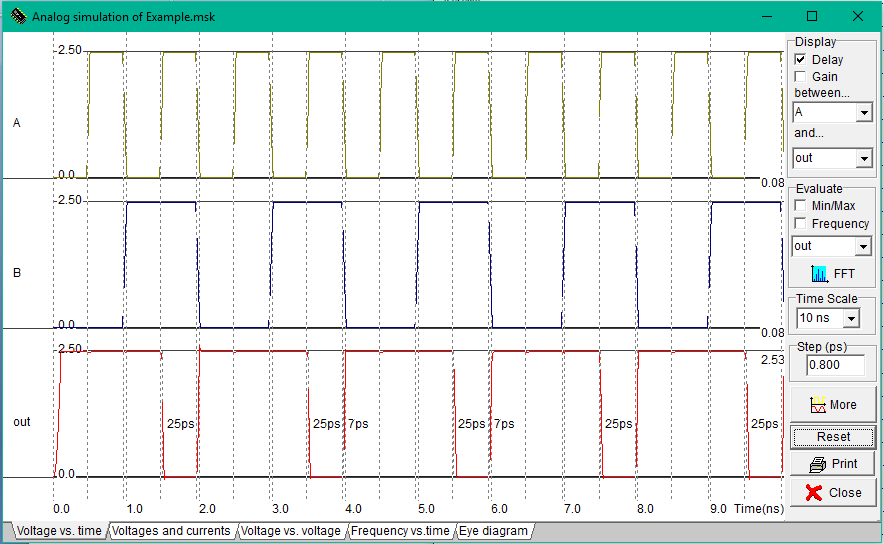


nMOS pMOS

* Now, Place the nMOS and pMOS transistor in our design. Then, connect input, output, metal,poly, Vdd , Vss and other necessary connection according our design. Final figure is given below:



* By simulating the simulation of our design the timing diagram is generated which is given below:



# ***Conclusion:***

The NAND gate is implemented using two pMOS and two nMMOS and the truth table is successfully verified. The required waveforms were obtained, observed and noted down using MICROWIND2.

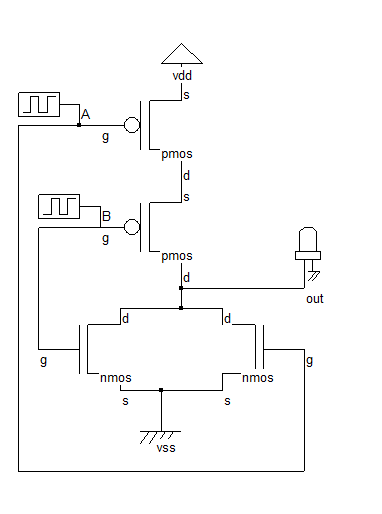
***(b) Layout design and verification of NOR gate.***

# ***State of the Problem***:

*In this experiment work we are going to design the layout of NOR gate. Also we will verify the gates with true table and timing diagram.*

# ***Hypothesis:***

The truth-table and schematic diagram of NOR gate is given below:



|  |  |  |
| --- | --- | --- |
| A | B | OUT |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

*True Table*

*Schematic diagram of NOR*

We will design the layout of NOR gate in ‘MICROWIND2’ software following this diagram.

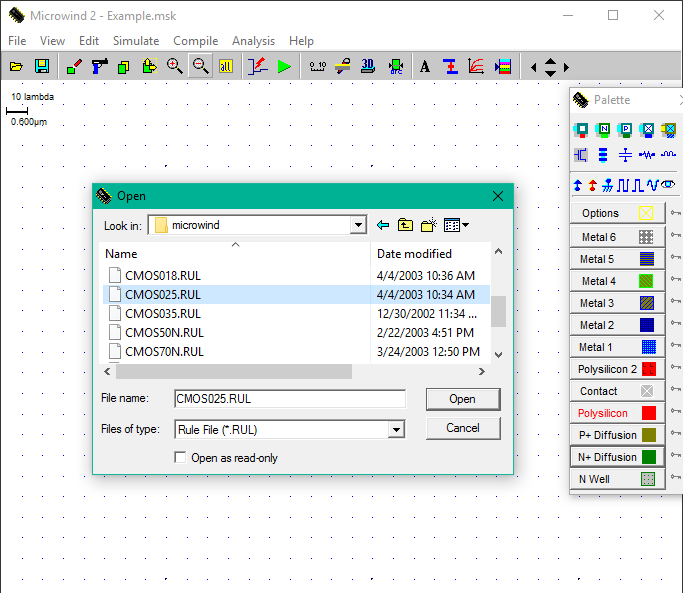
***Materials:***

* MICROWIND2

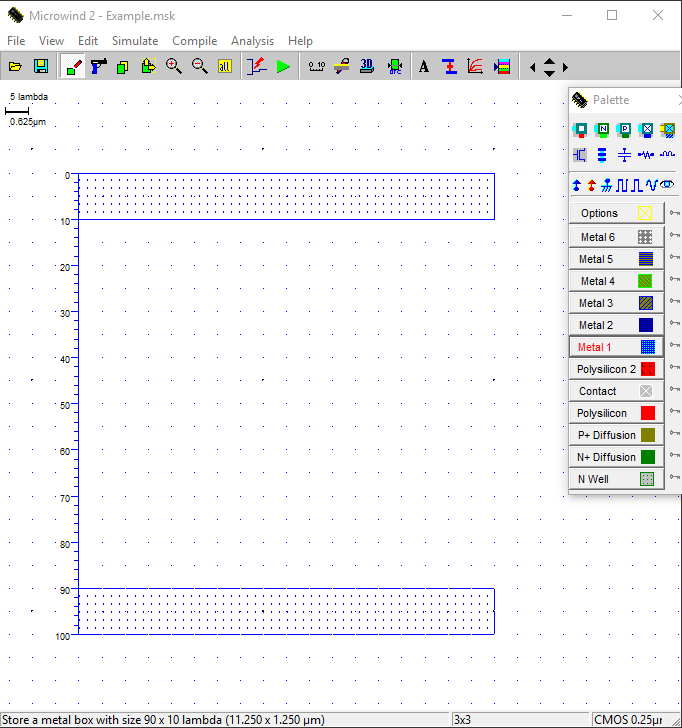
# ***Procedure:***

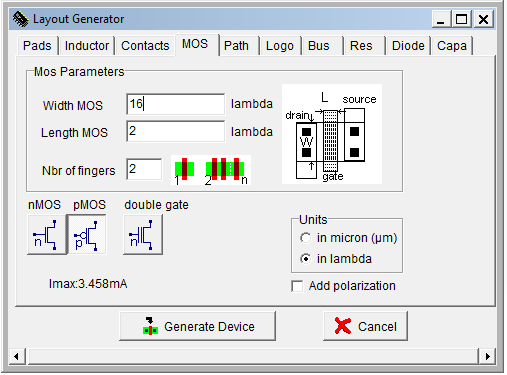
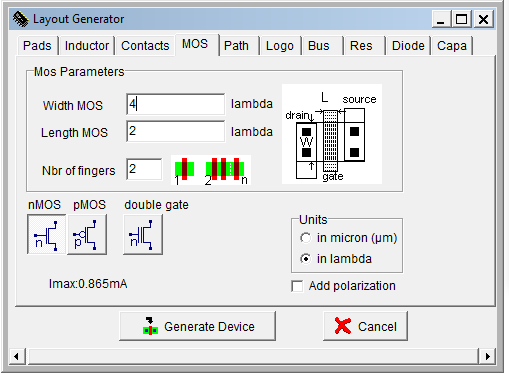
Here is the working procedure with illustration:

* At first, we open the ‘MICROWIND2’ software and select exact foundry which we needed. Here we use CMOS025.RUL as our foundry. Figure are given below:



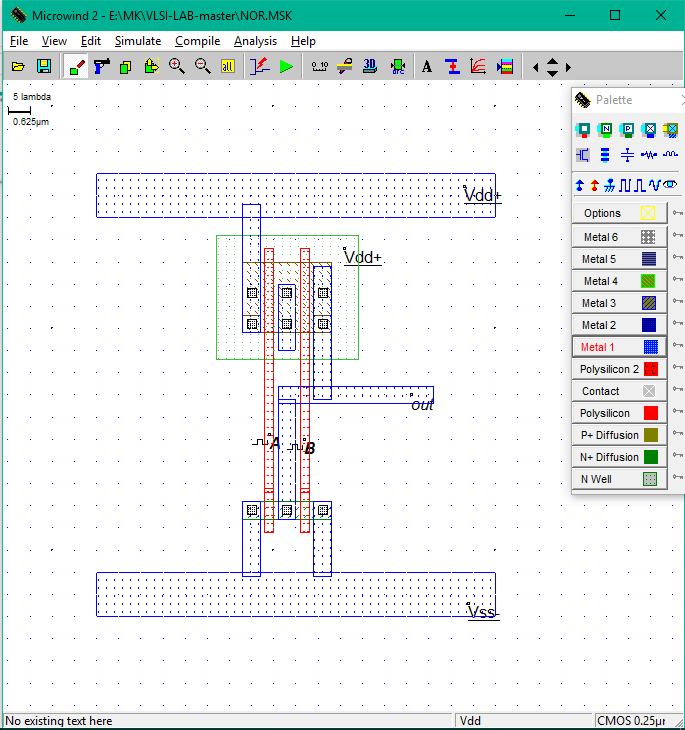
* Create Vdd and Vss metal rails as 90\*10 lamda. Top rail as Vdd and bottom as Vss . Figure is given below:



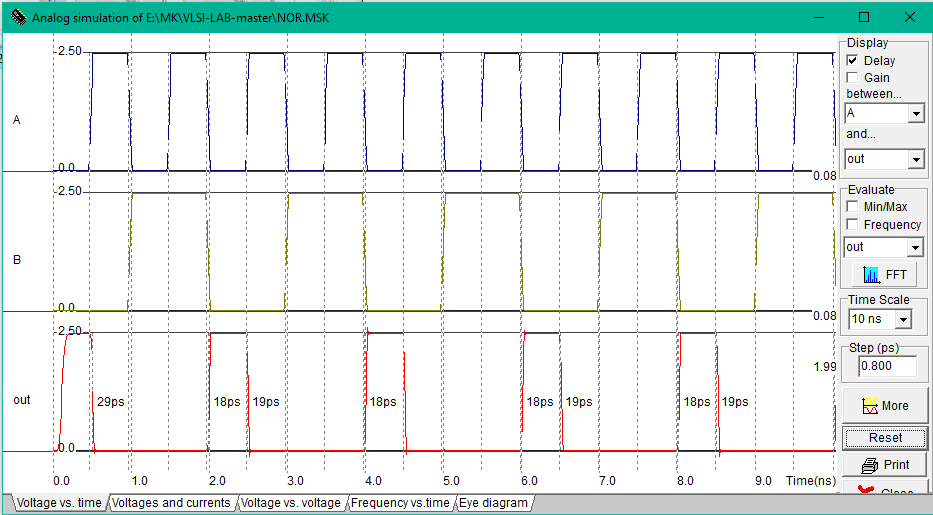
* Generate the nMOS ans pMOS with layout generator. Figures are given bellow:

nMOS pMOS

* Now, place the nMOS and pMOS transistor in our design. Then, connect input, output, metal,poly, Vdd , Vss and other necessary connection according our design. Final figure is given below:



* By simulating the simulation of our design the timing diagram is generated which is given below:



# ***Conclusion:***

The NOR gate is implemented using two pMOS and two nMMOS and the truth table is successfully verified. The required waveforms were obtained, observed and noted down using MICROWIND2.