**Lab Report : 05**

# Title: Implementation and Design of full adder circuit using ASIC design tools. Y=and Carry=AB+BC+CA

# 

# Course title: VLSI Circuits Design Lab.

Course code: CSE-412

4th Year1st Semester

**Date of Submission : 22-12-1015**

**Submitted to-**

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|  | *Class Roll* | *Exam Roll* | *Name* | *Session* | *Signature* |
|  | 407 | 120103 | Aditi Sarker | 2011-12 |  |