Implementation of Dancing LED Pattern on FPGA

This project report is submitted to

Shri Ramdeobaba College of Engineering and Management, Nagpur

(An Autonomous Institution* Permanently *Affiliated to Rashtrasant Tukdoji Maharaj Nagpur University)

in partial fulfillment of the teacher assessment

for the course

ENT308 :Computer Organisation

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NAGPUR – 440013

Session: 2019 - 20

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- # Aim

  Implementation of Dancing led pattern on FPGA board by means of MIPS-16 machine using a hardware description language.

- # Introduction

  ## MIPS

  - MIPS (Microprocessor without Interlocked Pipelined Stages) is a reduced instruction set computer (RISC) instruction set architecture (ISA).
  - MIPS instructions have fixed width. The o MIPS 32 ISA has 32 bits wide instructions. Each instruction in MIPS16 is 16 bits wide.

  ## FPGA

  - Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects.
  - FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing.

  ## VHDL

  - VHDL (VHSIC-HDL, Very High Speed Integrated Circuit Hardware Description Language) is a hardware description language .
  - It is used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits.

- # Software Used and About the software

  ## XILINX ISE

  - Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.
  - Xilinx ISE is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors. The Xilinx ISE is primarily used for circuit synthesis and design, while ISIM or the ModelSim logic simulator is used for system-level testing.

- ## ALP for Problem Statement

We have to glow the led in dancing led pattern .We assumed the dancing led pattern to be alternating, i.e. 1010101010101010 and then 0101010101010101 pattern.

Value given to register:
$s3= FFFF(hexadecimal) $s2=AAAA(hexadecimal)

Instruction(ALP)

```
Here : sub $s1, $s3, $s2
       sub$s1, $s3, $s1
       j  Here
```

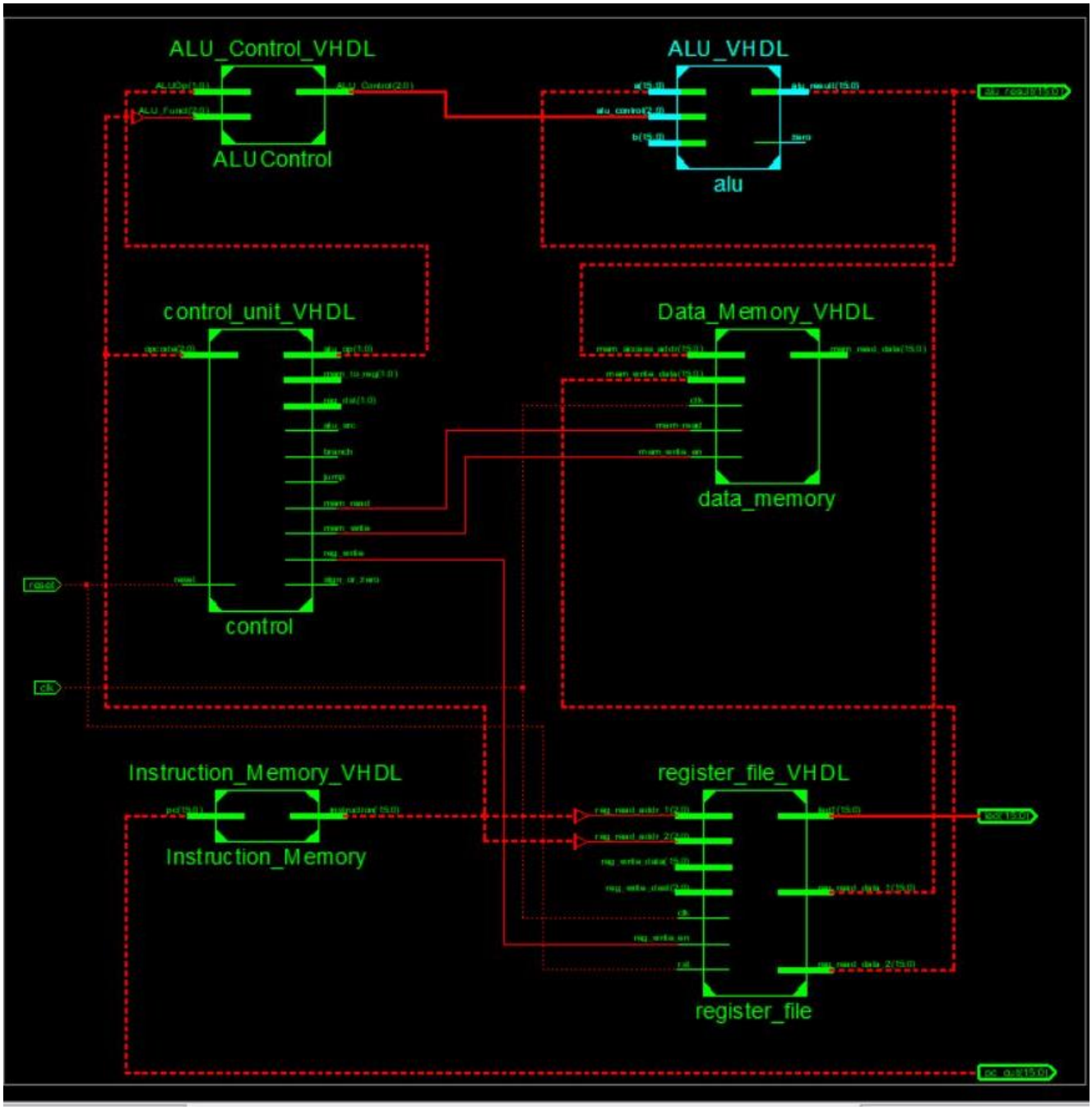
- ## Binary Encoding of Instructions

Instruction(ALP)	BINARY CODE
Here : sub $s1, $s3, $s2	000 011 010 001 0001
sub $s1, $s3, $s1	000 011 001 001 0001
j Here	010 000 000 000 0000

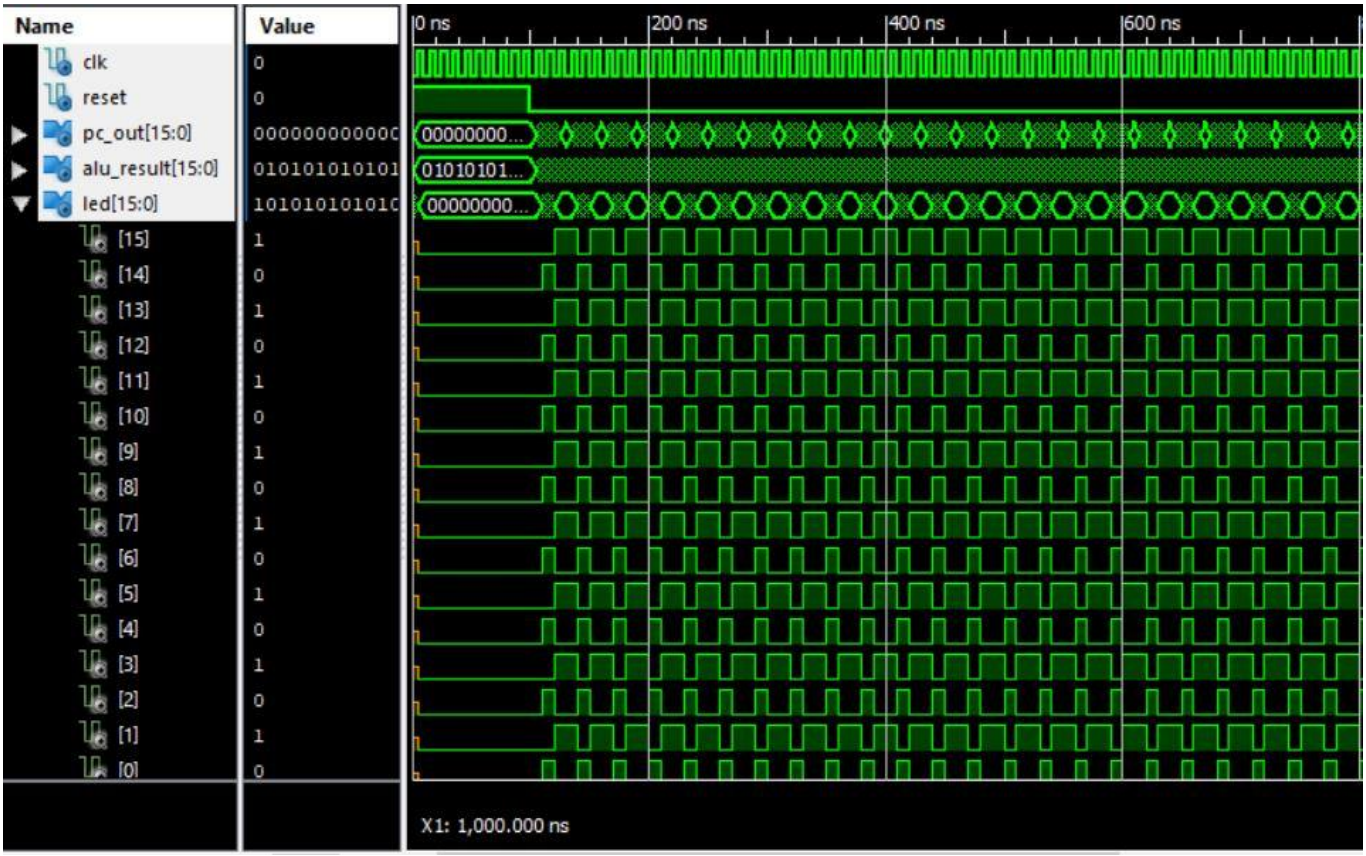
- ## ISim Statistics

ISim Statistics
Xilinx HDL Libraries Used=ieee
Fuse Resource Usage=593 ms, 37376 KB
Total Signals=94
Total Nets=4691
Total Blocks=12
Total Processes=40
Total Simulation Time=1 us
Simulation Resource Usage=0.25 sec, 5334646 KB
Simulation Mode=gui
Hardware CoSim=0

- RTL Schematic



- Simulation Result



- Operating Frequency

Operating Frequency (f) = 1/T

= 1/ 5.442 ns

$\boldsymbol{f}$ **= 183.755 MHz**

- Result

Hence we have implemented dancing led pattern by a MIPS machine using hardware description language.

- References

- Computer Organization and Design (fifth edition) by David Patterson and John Hennessy
- http://www.ijsrp.org/research-paper-0413/ijsrp-p16126.pdf
- https://www.fpga4student.com