EEDG 6375 DESIGN AUTOMATION OF VLSI SYSTEMS

Fiduccia Mattheyses Heuristic

PROJECT REPORT

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Who have !-

EXECUTION PROCEDURE: (DETAILS ABOUT RANDOM CUTSET GENERATION): We executed the fiduccia Mattheyses algorithm, to reduce the cuteet for partitioning the given netlists. We implemented the algorithm to run 8 passes. For each run me implemented a new random cut set: : we read the modefile sequentially 1. Random Cutset 1 file (V 1.0) and assign each node to an attende Partition. 2. Random Cutset 2: We read the nets sequentially and assign each node in one net to a file (V1.1) partition and the alternate net's nodes to the other partition. If a node is repeated, the latist assignment is considered. we assign the first n nodes in 3. Random cutset 3: the nodes file to one partition file (v1.2) such that (wgt of part 1)/Gotal weight) is less than 0.5. After this we have the other nodes assigned to The other partition. 4. Random cutset 4: we assigned the first quarter of the nodes (by weight) to part A and file (v1.3)second quarter in parts, third

quarter in part A and rest in part B

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least outset for each bunchmark is placed in a red square. If written in red.

	Partitioning	Results Rep	orting She	et	
Benchmark Name	Run #	Execution Time	Starting Cut	Ending Cut	ercentage Change
Example 1:	1	5	2365	676	71.41649049
FPGA-Example 1:	2	4.57	2000	629	68.55
Time in Seconds)	3	7.02	2541	509	79.96851633
,	4	5.64	2220	483	78.24324324
	5	8.38	1897	566	70.16341592
	Average	6.104			73.6683332
Example 2:	1	247	438715	89886	79.51152799
Time in Minutes)	2	235	329166	88162	73.21655335
,	3	288	9077	3417	62.35540377
	4	227	14674	7674	47.70342102
	5	303	276096	89260	67.67066528
	Average	260			66.09151428
Example 3:	1	179	355654	85554	75.94459784
(Time in Minutes)	2	194	292082	80062	72.5892044
(1	3	201	15558	12912	17.00732742
	4	183	40043	33015 ←	17.55113253
	5	212	266574	84854	68.16868862
	Average	193.8	200371	0 103 1	50.25219016
Example 4:	1	608	728801	131583	81.94527724
(Time in Minutes)	2	631	604579	122807	79.68718728
(Tillie III Williates)	3	601	13222	10586	19.93646952
	4	589	23599	20103	14.81418704
	5	612	503407	132190	73.74092931
	Average	608.2	303407	132190	54.02481008
*Minimum cutset attained		008.2			34.02481008
	e and is in Seconds. Actual T	ime of Execution for	8 Passes ner Run i	s shown Below	
Benchmark	Time				
FPGA-Example1	6.1 Seconds	Value, of	final o	rutect i	n the 4th Lander
FPGA-Example2	260 Minutes	000000	Cha and	1 5 4 4	n the 4th randor , 5 runs, for
FPGA-Example3	193.8 Minutes	courses,	Stagnau	3 aprice	, o ruivo, for
FPGA-Example4	608.2 Minutes	IDGA 2	.4		
		119/13	/기 •		
Additional Simulations	(30 Passes per Run)				
Benchmark Name	Run #	Execution Time	Starting Cut	Ending Cut	ercentage Change
Example 1:	1	22	2365	676 <	71.41649049
PGA-Example 1:	2	19.91	2000	629 ←	68.55
Time in Seconds	3	21.54	2541	485	80.91302637
	4	21.49	2220	369	83.37837838
	5	17.25	1897	563 <	70.32156036
	Average	20.372			74.91589112

the absolute minimum ending out for fpgal is achieved often using random out #4 and running the huristic for 30 passes.

Random cuts #1, #2 q #5 stagnate after 8-10 passes of FM.

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