

EE517 LAB Course Project

**Design and analysis of a 2-stage op-amp using
gm/id method.**



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1 Aim :

Design and analysis of a 2-stage op-amp using gm/id methodology.

2 Objective :

1. Design a 2-stage Op-amp with gm/Id methodology in 65 nm technology for given specifications.
2. Be familiar with the design steps of gm/Id methodology and mention the plots related to that in detail.

3 Specifications and library :

1. Slew rate = $12V/\mu s$
2. Phase margin $\geq 60^\circ$
3. DC gain $\geq 70dB$
4. Unity Gain Bandwidth = 20MHz
5. ICMR = 0.6-0.9V
6. Load Capacitance (CL) = 10pF
7. Reference current source (Iref) = 50 μA

4 Tools used :

1. Cadence Virtuoso

5 Theory :

An operational transconductance amplifier is a differential to single ended amplifier. The structure is a bit different compared to a differential structure since it uses a current mirror in above. This is done to increase the transconductance which in turn increases the Gain of the single ended output. Here we have shown a single stage OTA however multistage OTAs are also used.

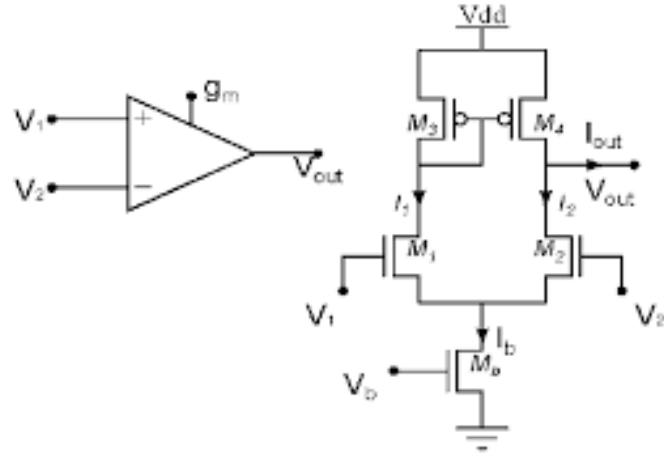


Figure 1: Basic CMOS Transconductance Amplifier

Two stage OTAs give advantages in two aspects. This can be used to get higher gain compared to single stage and the output swing is also higher than single stage.

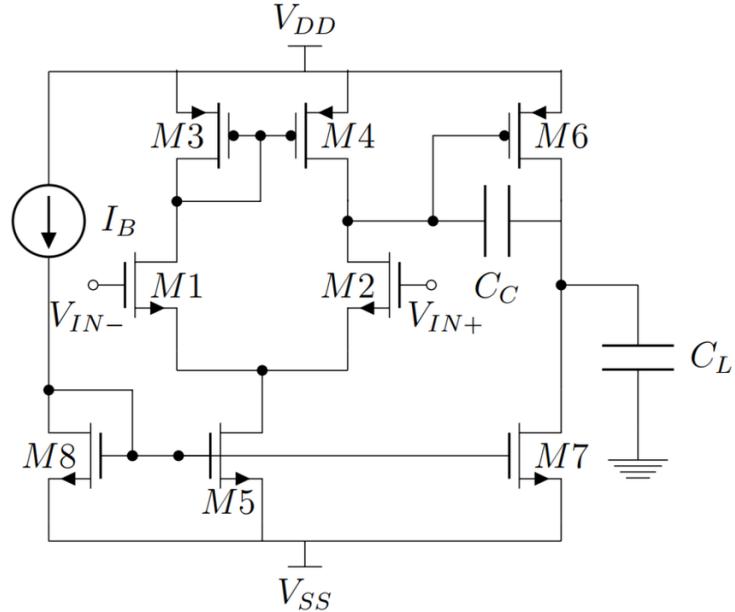


Figure 2: 2-stage OP-Amp

6 Procedure :

- For both NMOS and PMOS we need the plots of gm/gds vs gm/id, id/w vs gm/id and vgs vs gm/id.
- These plots have been generated for individual NMOS and PMOS separately.
- Initial calculations are started from the specifications and rest follow from the graphs. The calculations have been shown in calculations section.

7 Plots of various parameters

7.1 Design of M1, M2 :

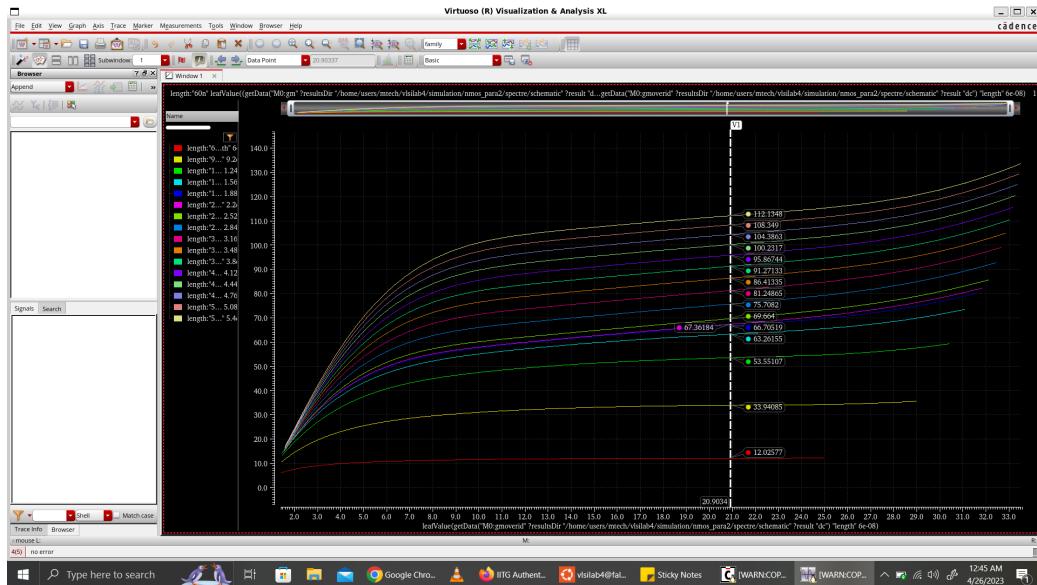


Figure 3: Plot of gm/gds vs gm/id for nmos

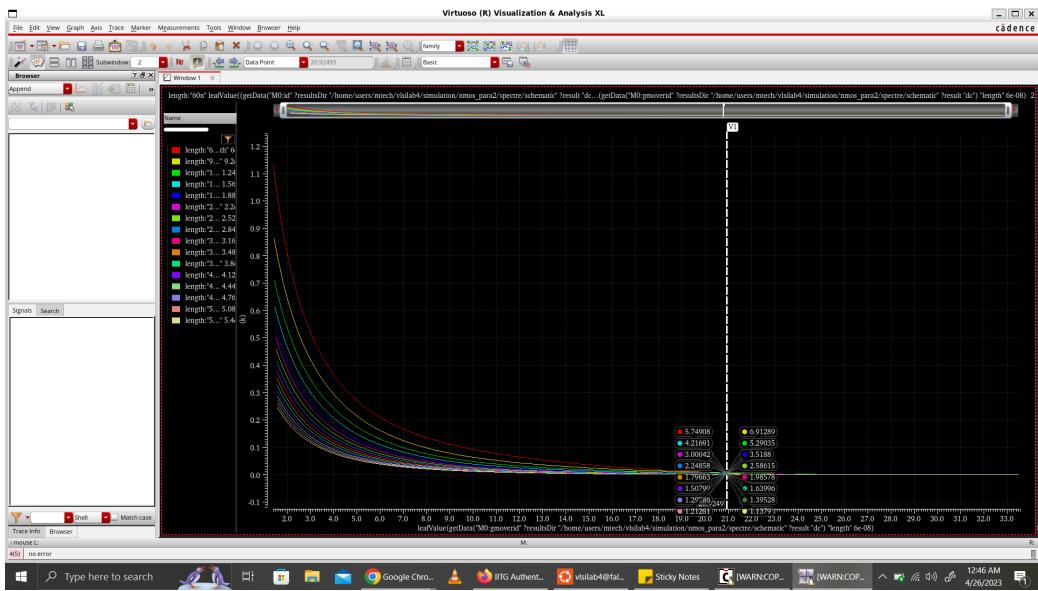


Figure 4: Plot of id/w vs gm/id for nmos

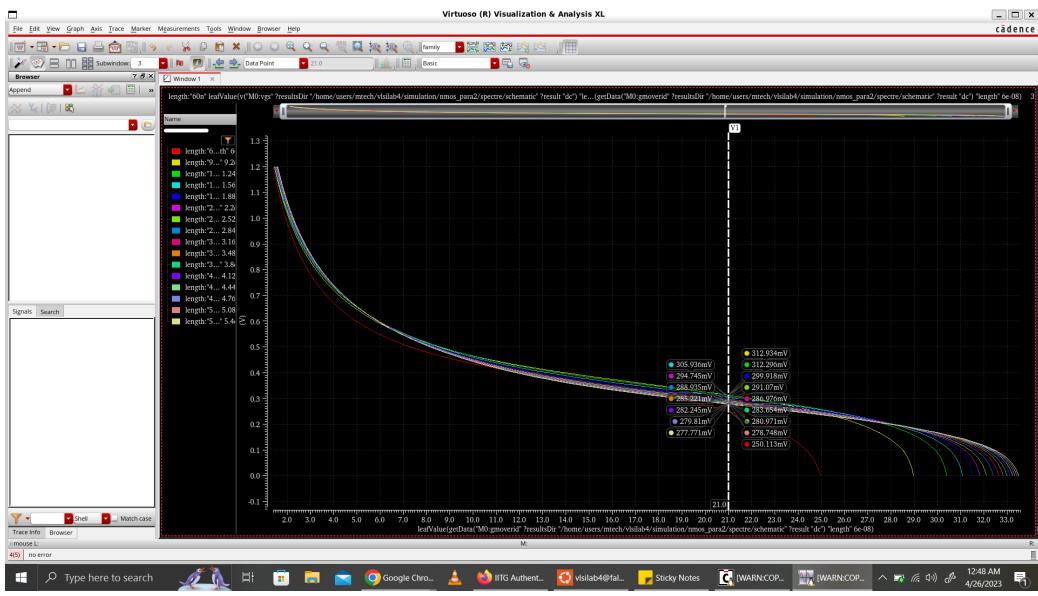


Figure 5: Plot of vgs vs gm/id for nmos

7.2 Design of M3, M4 :

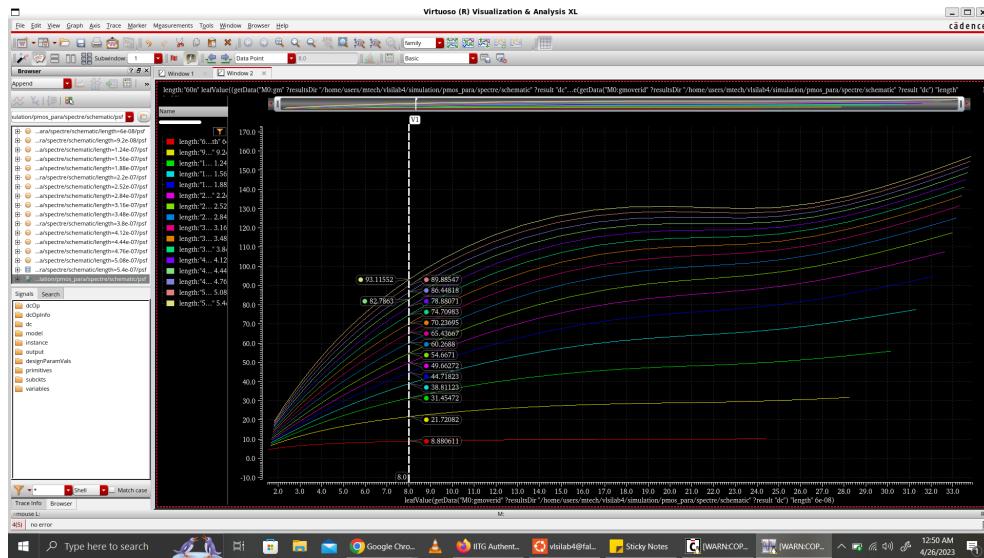


Figure 6: Plot of gm/gds vs gm/id for pmos

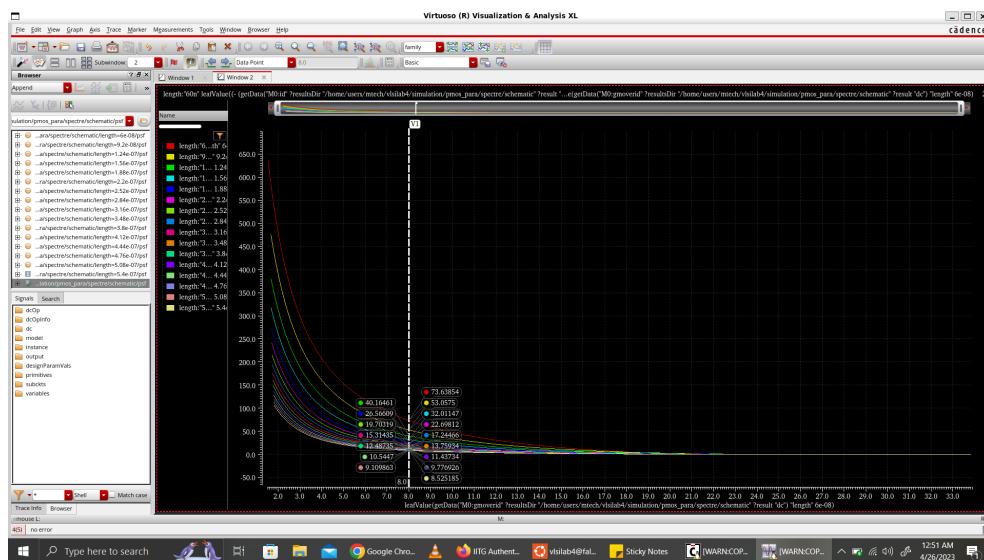


Figure 7: Plot of id/w vs gm/id for pmos

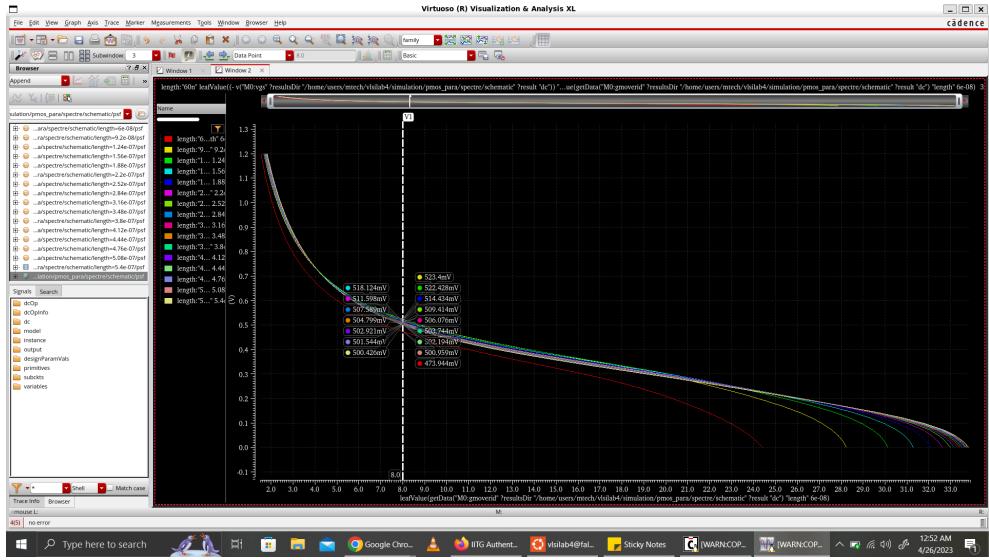


Figure 8: Plot of vgs vs gm/id for pmos

7.3 Design of M6 :

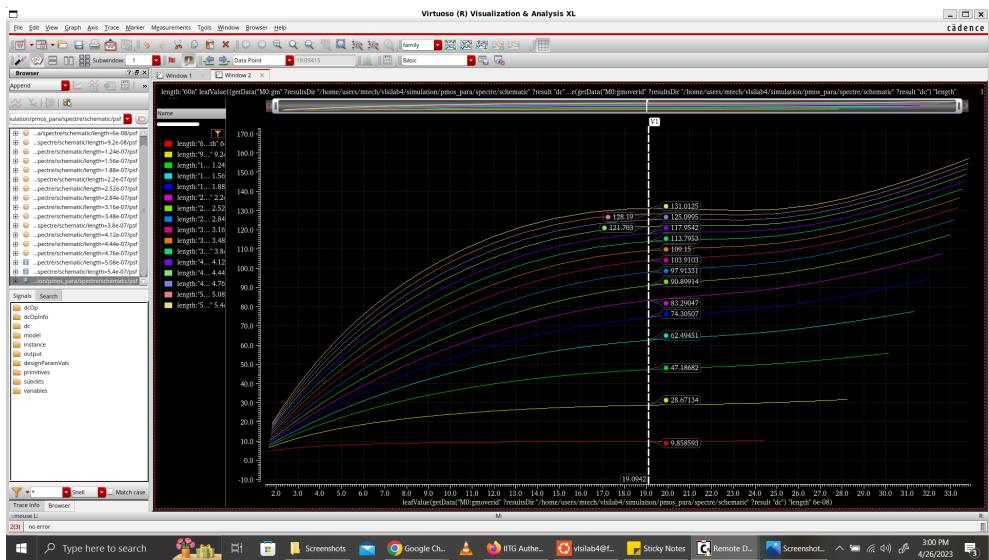


Figure 9: Plot of gm/gds vs gm/id for pmos

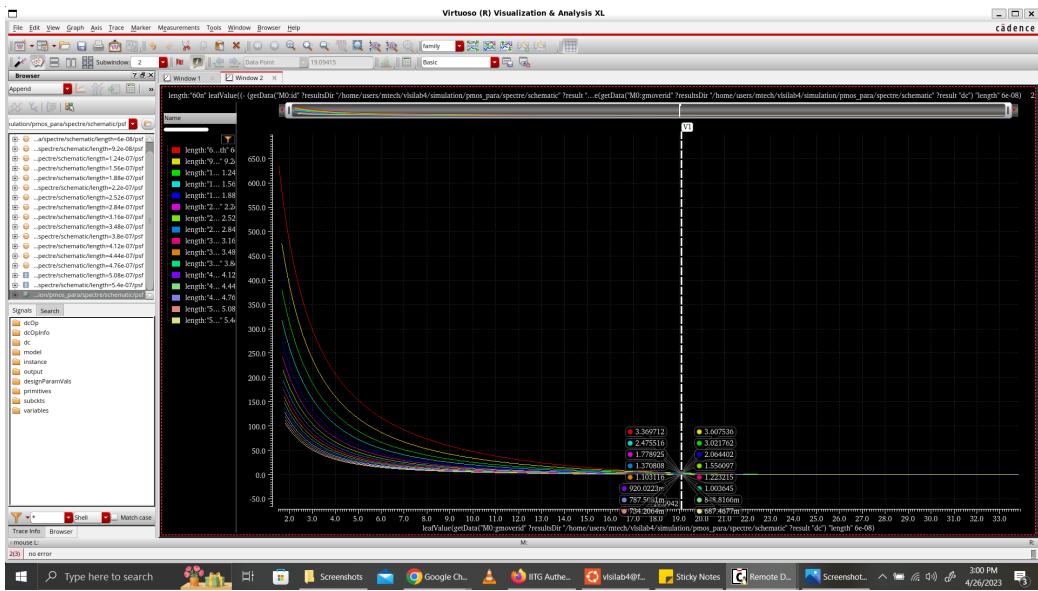


Figure 10: Plot of $\frac{I}{W}$ vs $\frac{Gm}{Id}$ for pmos

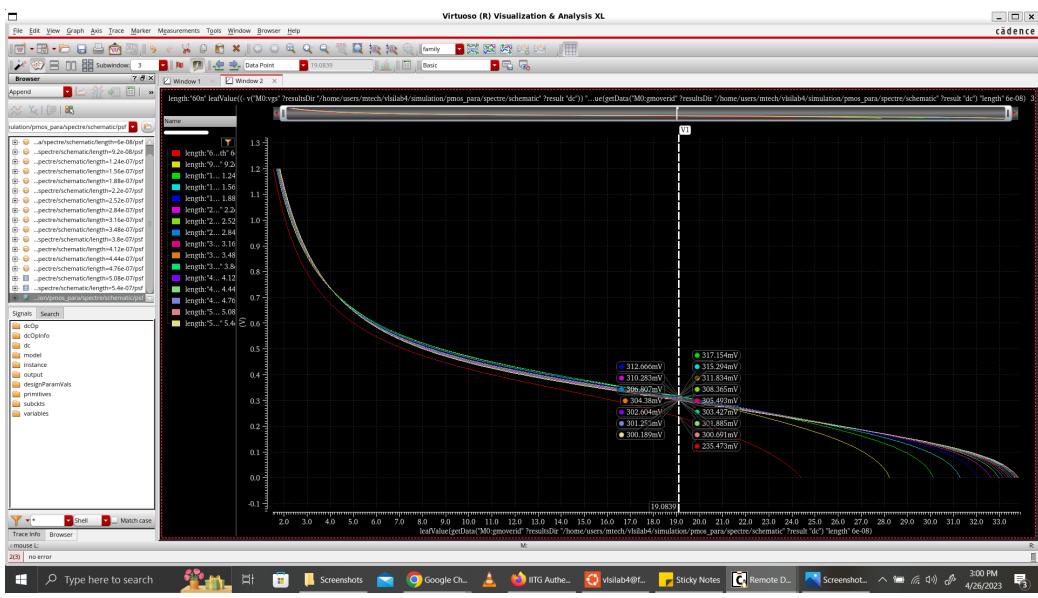


Figure 11: Plot of V_{GS} vs $\frac{Gm}{Id}$ for pmos

7.4 Design of M7 :

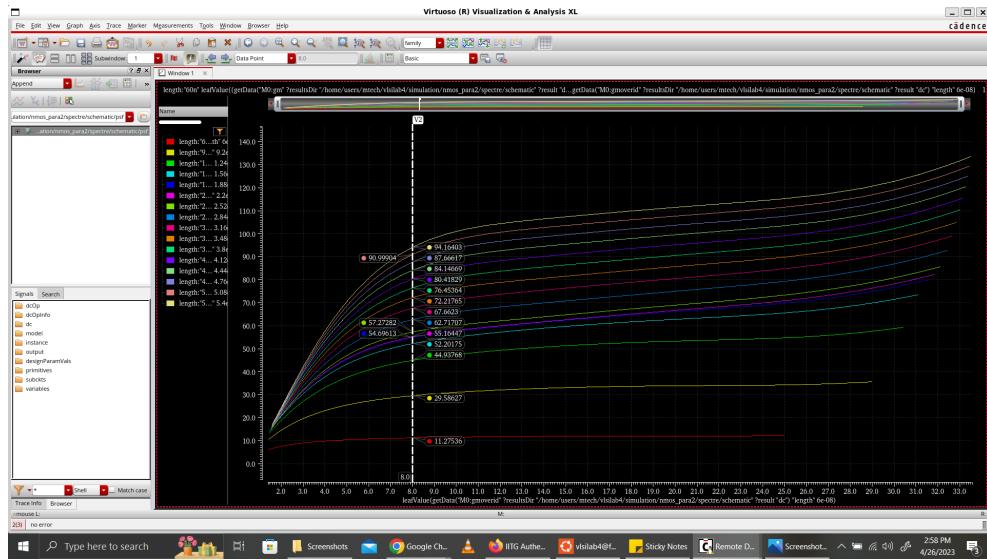


Figure 12: Plot of gm/gds vs gm/id for nmos

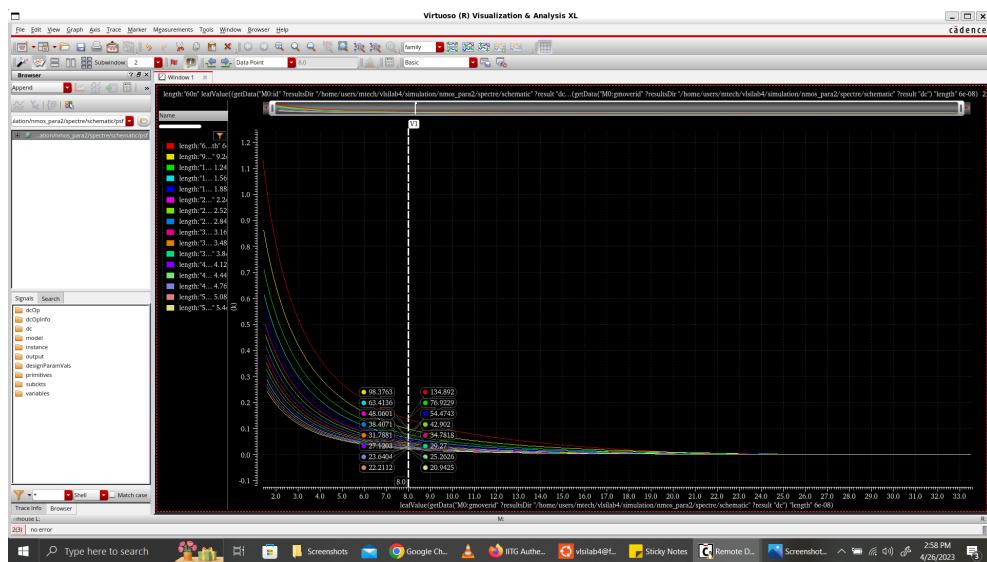


Figure 13: Plot of id/w vs gm/id for nmos

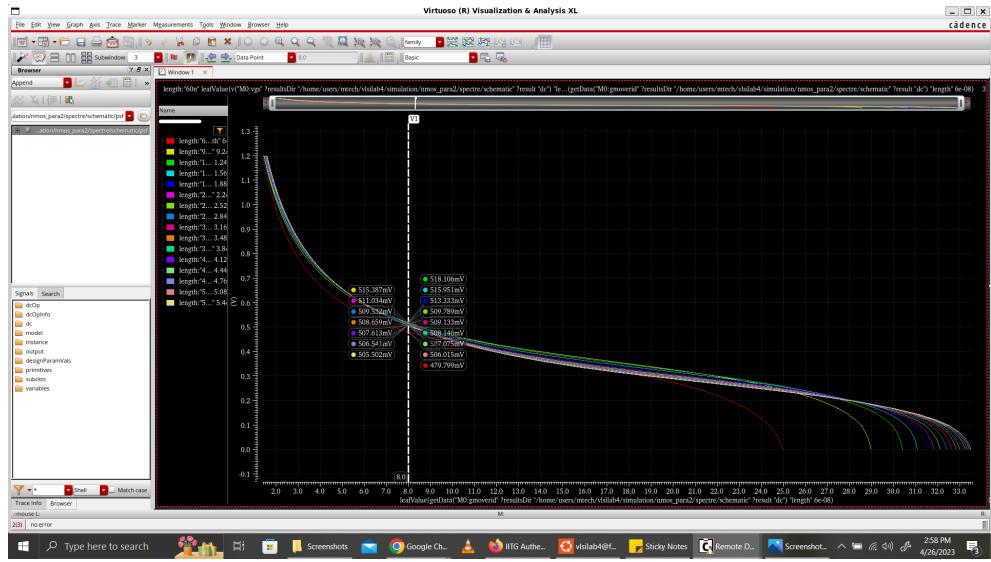


Figure 14: Plot of vgs vs gm/id for nmos

8 Schematics:

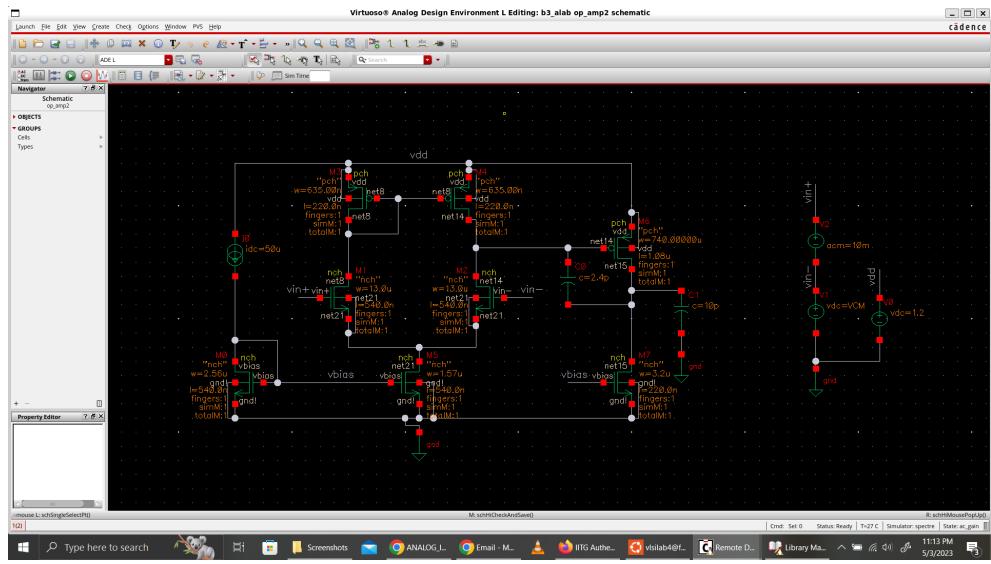


Figure 15: Circuit Diagram

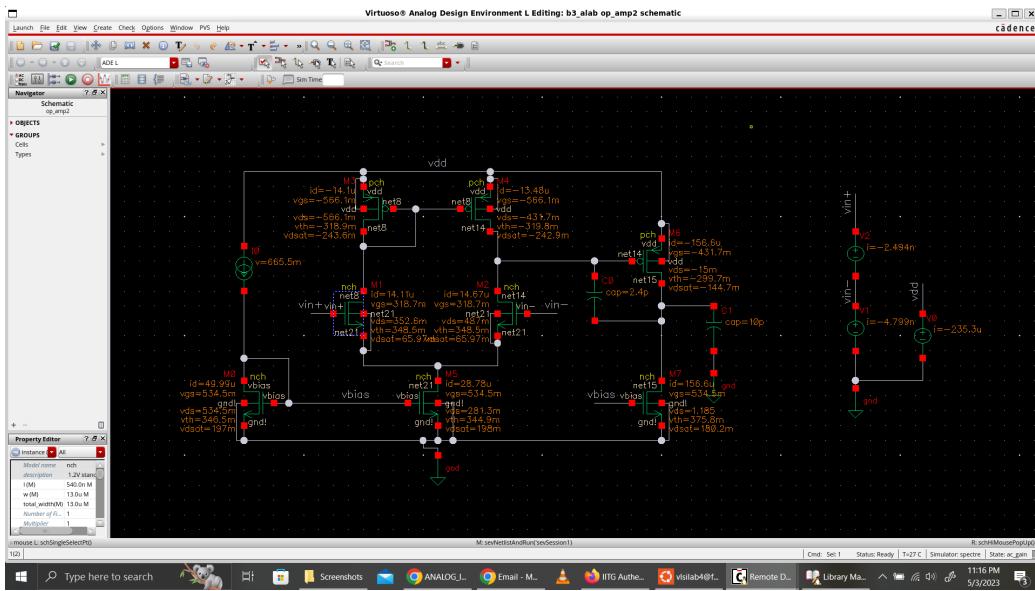


Figure 16: Circuit with dc operating point



Figure 17: Gain and Phase Margin

9 Calculations:

1. From the desired phase margin, choose the minimum value for C_c , i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10\text{GB}$.

$$C_c = 0.24 * C_L \quad (1)$$

The C_c is chosen as 2.4pF .

2. Determine the minimum value for the “tail current” (I_5) from

$$I_5 = SR * C_c \quad (2)$$

Given $SR = 12 \text{ V/us}$. So $I_5 = 28.8 \text{ uA}$ and $I_1 = 14.4 \text{ uA}$.

3. Design for $(W/L)_1$ and $((W/L)_2)$ to achieve the desired GB.

$$g_{m1} = GBC_c \quad (3)$$

The g_{m1} comes to be around $301.44\mu\text{S}$.

9.1 Design of M1, M2:

1. For M1 and M2, gm/id comes to be around 21.
2. From the plot the maximum gm/gds possible for this value is 112.135 for length of $L = 540\text{nm}$. The gds value we get is 2.697.
3. For the same L and gm/id using the graph of id/w vs gm/id we get the width of M1 and M2 as $W = 13\text{um}$.

9.2 Design of M3, M4:

1. For M3 and M4, we assume gm/id to be around 8. This is to keep them in saturation for proper functioning of current mirror.
2. We are keeping the gds of M3 same as M1, $gds = 2.697$.
3. As we know id and gm/id we can calculate the gm and hence the gm/gds . gm comes to be around 115.2 and gm/gds around 42.7.
4. From the graphs of gm/gds and id/w we get the L and W to be $L=220\text{nm}$ and $W=634\text{nm}$.

9.3 Design of M6:

1. For M6, id is calculated from the formula.

$$\frac{I_{d1}}{I_{d6}} \leq \frac{C_c}{2(C_L + C_c)} \quad (4)$$

id6 comes around 148.8. 2. The gm is calculated from phase margin formula, we get gm = 2840.6. Hence gm/id = 19.09. 3. From the plot the maximum gm/gds possible for this value is 131 for length of L = 540nm. The gds value we get is 21.7.

3. For the same L and gm/id using the graph of id/w vs gm/id we get the width of M6 as W = 216.5um.

9.4 Design of M7:

1. For M7, we assume gm/id to be around 8. This is to keep them in saturation for proper functioning of current mirror.
2. We are keeping the gds of M7 same as M6, gds = 21.7.
3. As we know id and gm/id we can calculate the gm and hence the gm/gds. gm comes to be around 1190.4 and gm/gds around 54.86.
4. From the graphs of gm/gds and id/w we get the L and W to be L=220nm and W=3.1um.

10 Design Summary :

MOSFET	Width	Length	gm/id	id
M1, M2	13um	540nm	21	14.4uA
M3, M4	635nm	220nm	8	14.4uA
M6	740um	1.08um	19.09	148.8uA
M7	3.2um	220nm	8	148.8uA
M5	1.57u	540n	8	28.8uA
M0	2.56u	540n	8	50uA

Table 1: Design Summary

11 Observations:

- As the (W/L)₆ was changed the gain was varying. So it is adjusted to have higher gain.
- For C_c=2.4pF we are getting higher gain compared to C_c=3pF hence it is kept as 2.4pF.
- We got a gain of approx. 60db , Phase Margin of 40 deg and Bandwidth of 12MHz.

12 Conclusion :

All the results have been obtained practically and matching with the theoretical justification. The theoretical calculations have been done.

13 References :

- B. Hesham, E. -S. Hasaneen and H. F. A. Hamed, "Design Procedure for Two-Stage CMOS Opamp using gm/ID design Methodology in 16 nm FinFET Technology," 2019 31st International Conference on Microelectronics (ICM), Cairo, Egypt, 2019, pp. 325-329, doi: 10.1109/ICM48031.2019.9021511.
- Hafeez K T lectures on gm/Id method
- Behzad Razavi, "Design of Analog CMOS Integrated Circuit