POWER OPTIMIZATION USING FIR FILTER IN FPGA

CONTENTS

INTRODUCTION

- Finite Impulse Response (FIR) filters are commonly used in digital signal processing for applications like audio processing, image enhancement, and communication systems.
- Power optimization is important to make filters more efficient and suitable for modern low-power applications.
- Techniques such as reducing the number of filter coefficients, using hardware-friendly structures, or eliminating multipliers can help reduce power usage.
- This project focuses on how FIR filters can be designed in a way that reduces power consumption while still maintaining their accuracy and performance.

LITERATURE SURVEY

Sl. No	Author	Methodology	Technique	Power	Limitation
[1]	A. Momeniet al	Approximate Multipliers	Simplify multiplier logic using LSB truncation (or) partial computations	40%-60% multiplier power saving	Large filters may accumulate error significantly
[2]	R. Venkataramani A.Ranjan	Hybrid Approximations [Add+Mult]	Combine multiple approximate units (e.g.adders+ multipliers)	Overall power saving of 40%-60%	Complexity in balancing error and power trade-off
[3]	A. Kumar, I. Sharma, L.K. Balyan	Multiplier-less FIR filter design	Directed Minimal Spanning Tree (DMST), Canonical Signed Digit (CSD), Common Subexpression Elimination (CSE), Shift Inclusive Differential Coefficient (SIDC)	Significant reduction in hardware complexity and power consumption due to elimination of multipliers	Significant reduction in hardware complexity and power consumption due to elimination of multipliers

[4]	Kamal Hossainetal	Order to achieve desired frequency response	Windowing frequency sampling and optimization	40%-60%	It impact on audio quality
[5]	Siliveri swetha, N. Siva Sankara Reddy	Low power and high speed carry select Adder (CSLA)	CSLA using D. latch and multipliers for FIR filter design	22%-56% power reduction compared to existing architectures	Increased area in same design
[6]	J.Han,ln.orshansky	Approximate Adders	Replace accurate adders with LOA,ETA or other Low-power design	30%-50% power saving in adders	Error included in sum,not suitable for critical applications

[7]	Amrita Rai	Fully adiabatic PAL FIR filter	Reversible logic, logarithmic multiplier	~75% reduction compared to CMOS FIR	Complexity in reversible logic design
[8]	Anand R., Sathishkumar Samiappan, M. Prabukumar	FIR filter design optimizatio n	Gray wolf optimization, cuckoo search, particle swarm optimization, genetic algorithm	Enhanced design precision, decreased execution time	Computational complexity of algorithms
[9]	Maliha Tasnim, Sachin Sachdeva, Yibo Liu, Sheldon X.-D. Tan	Hybrid Temporal Computing (HTC)	Temporal and pulse rate data encoding	36.61% power and 45.85% area reduction compared to CBSC	Novelty may require specialized hardware support
[10]	Govindaraj V., Ezhilazhagan Chenguttuvan, Dhanasekar Subramaniyam	Power and area efficient FIR filter design	Carry skip adder implementation	Reduced power and area	Limited to specific adder architectures

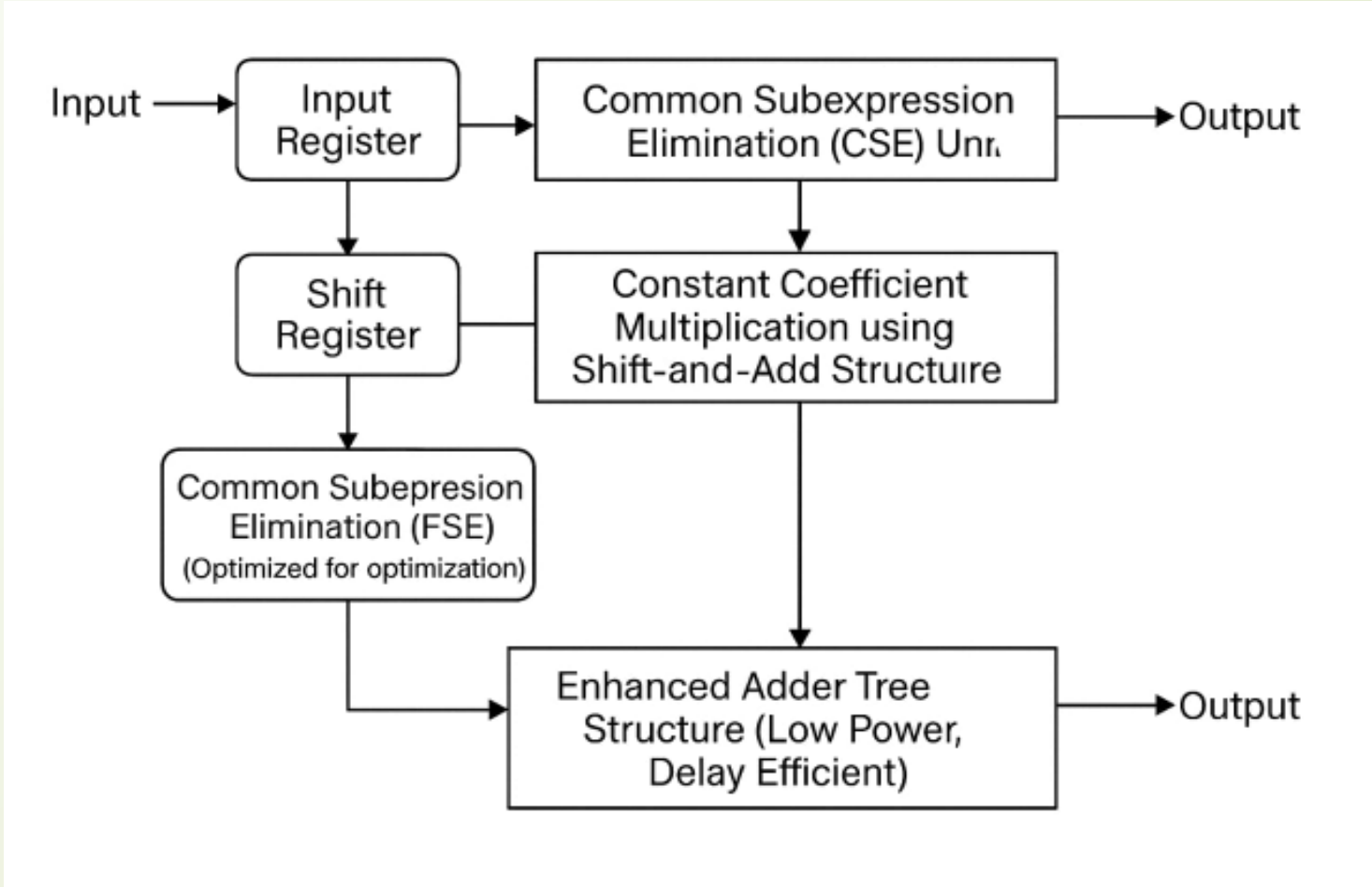
OBJECTIVES

- Improve adder efficiency for faster processing.
- Apply Flower Pollination Optimization (FPO) for best filter coefficients.
- Reduce power and delay.
- Maintain good signal quality.
- Test and compare performance using simulations.

PROBLEM STATEMENT

- Applying metaheuristic algorithms such as Flower Pollination Optimization (FPO) to find optimal filter coefficients and hardware configurations.
- Eliminating multipliers through shift and add techniques

BLOCK DIAGRAM



HARDWARE and SOFTWARE REQUIREMENTS

HARDWARE:

- FPGA Development Board
- PC / Laptop with minimum 8 GB RAM

SOFTWARE:

- Xilinx Vivado / ISE Design Suite
- HDL Coding Tools (Verilog/VHD)

EXPECTED RESULT

- **Power** : Expecting to reduce power by 40% to 60% using efficient techniques.
- **Latency** : Stays about the same (~5 ns) or slightly better.
- **Security** : May need extra care to avoid power-based attacks ideally no big impact.

REFERANCES

[1] A. Kumar, I. Sharma, L.K. Balyan, "Design of Low Power Multiplier less FIR Filter with Enhanced Adder Efficiency Using Flower Pollination Optimization," *Applied Acoustics*, 2020. https://doi.org/10.1016/j.apacoust.2020.107793

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