Monish Nene

ESD LAB2 Report

**Things Learnt in Lab1**

RS 232

Interrupts in MSP432 and 89C51

External and internal address Program memory access for 89C51

MAX232

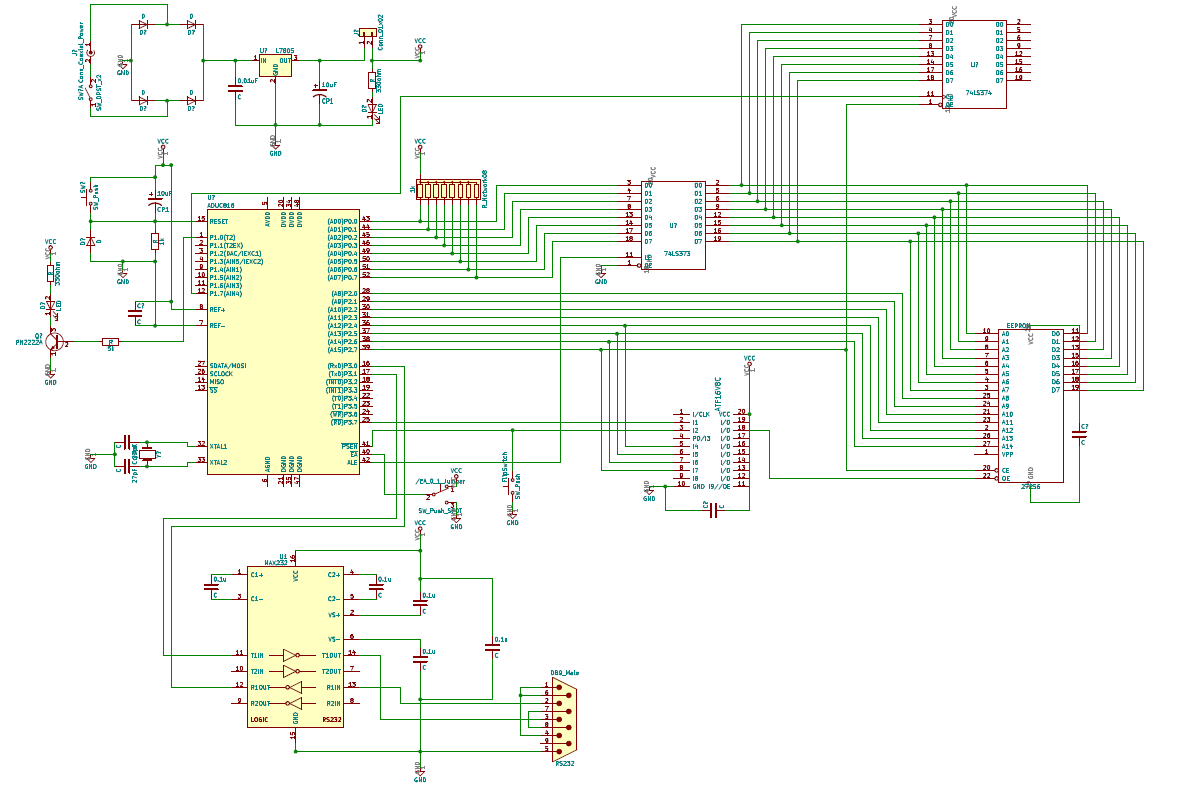
LOGIC Analysis

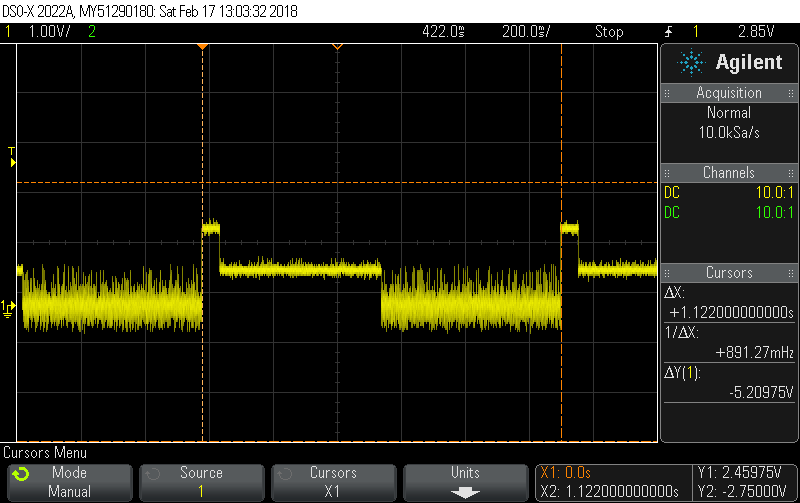
**Toughest Thing to do**

Interfacing 89C51 with EEPROM

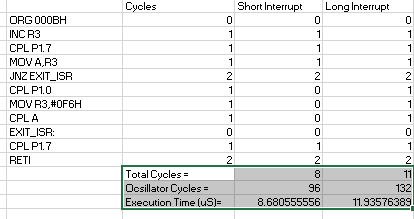
Debugging Hardware

**Schematic**

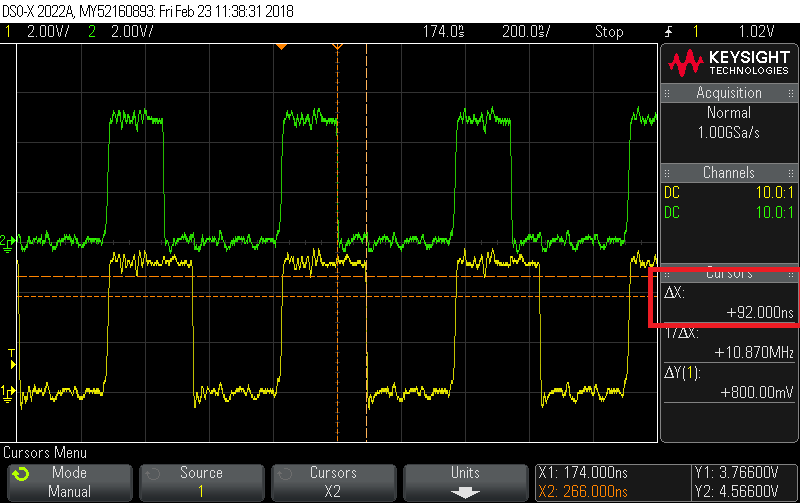


LED Waveform (period 1.122 S)

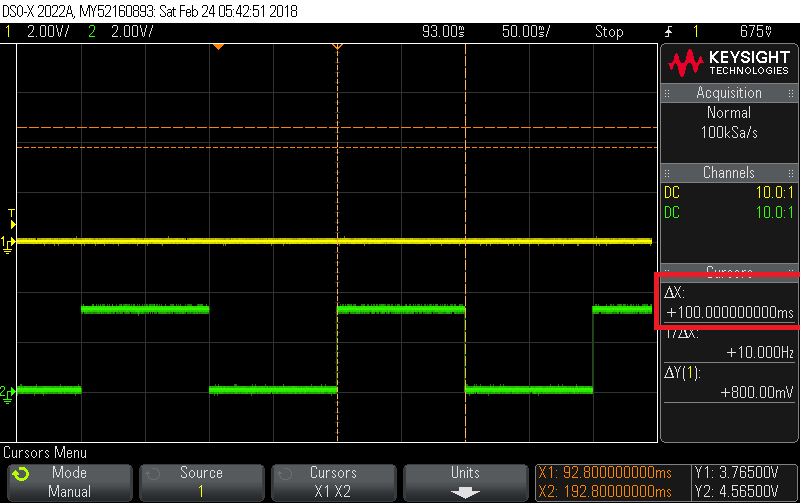
ISR Routine Cycles

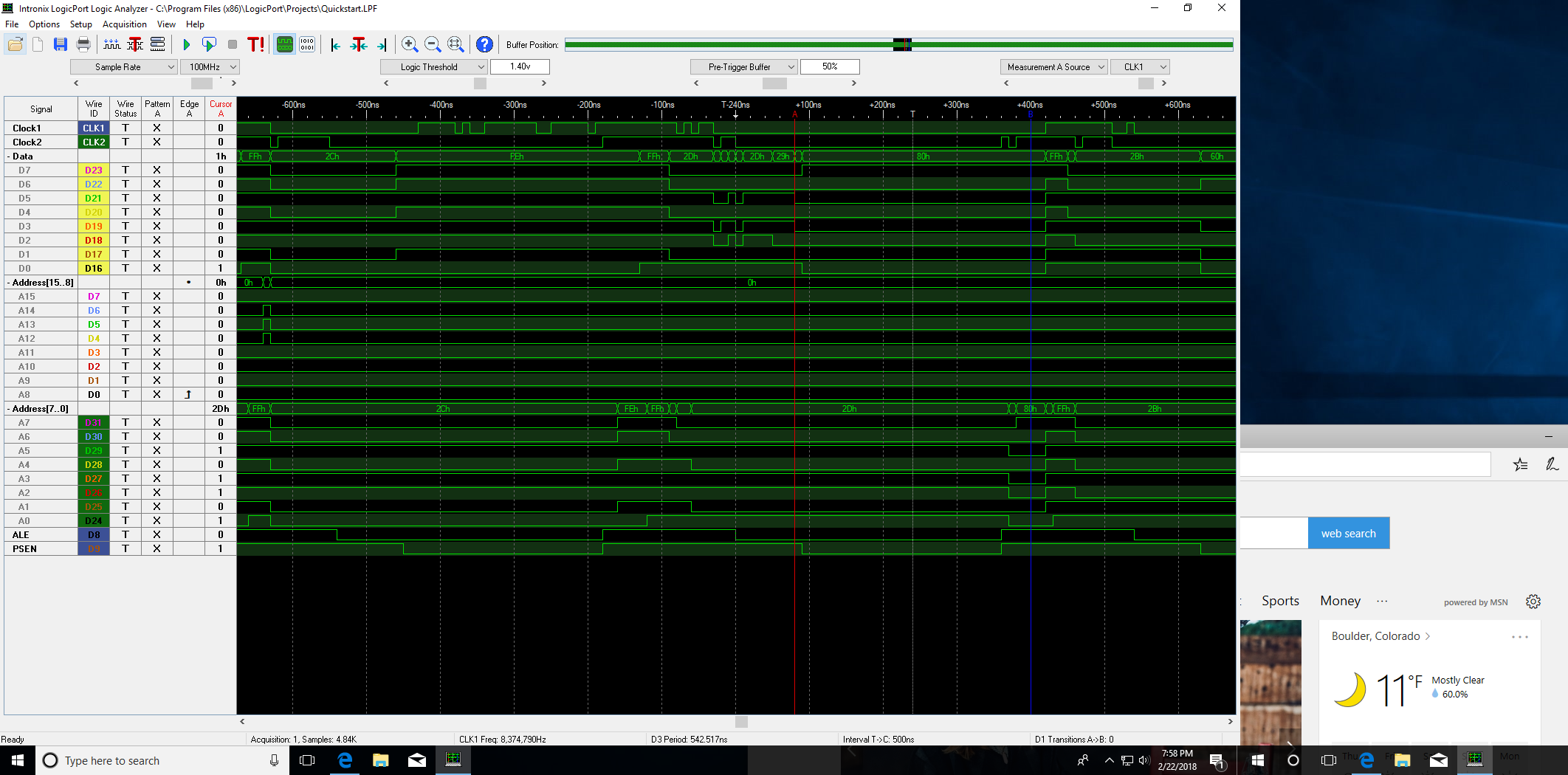


ALE\_PSEN\_TLL\_PL 92ns

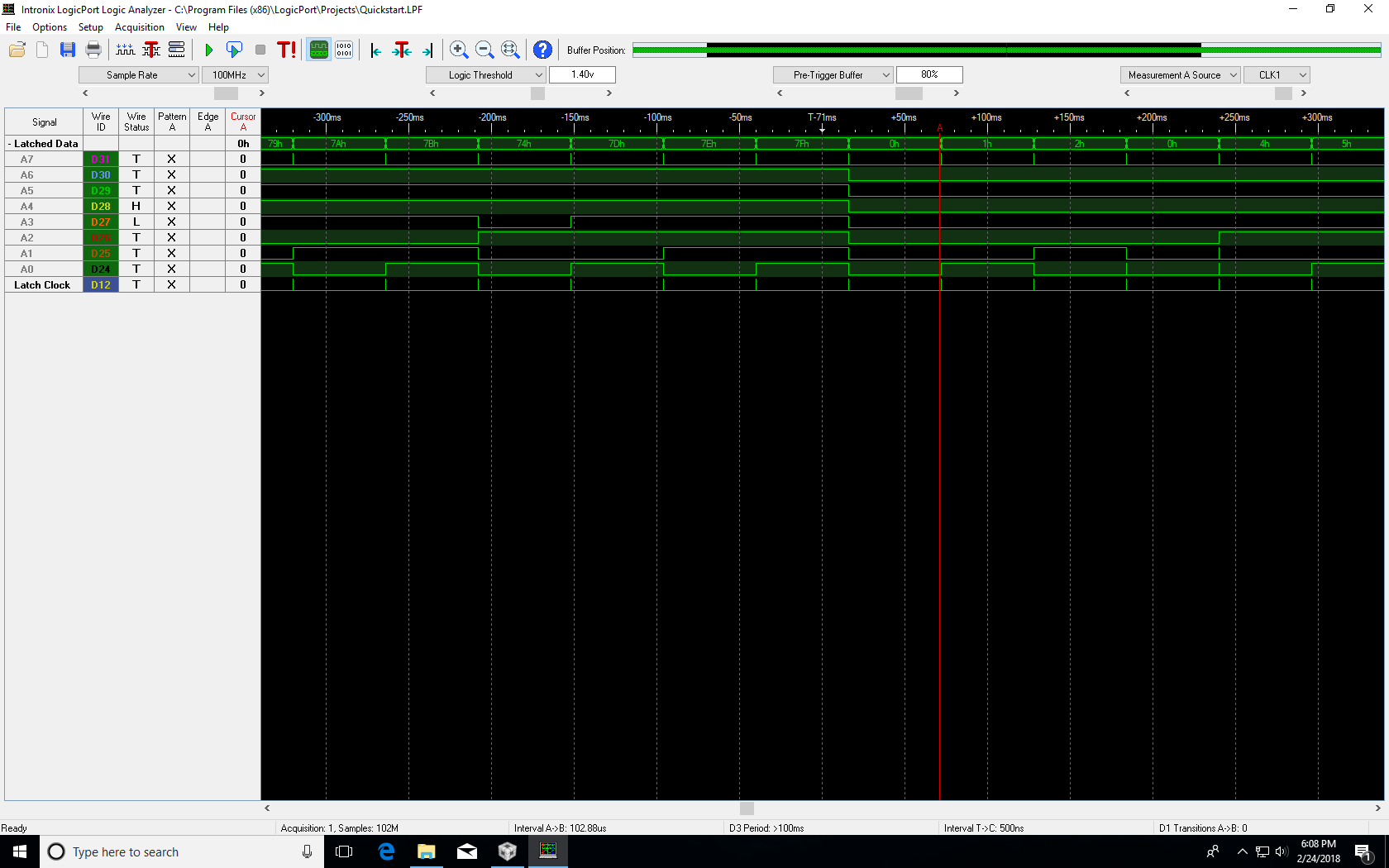


MSP\_CODE\_LED\_INTERRUPT

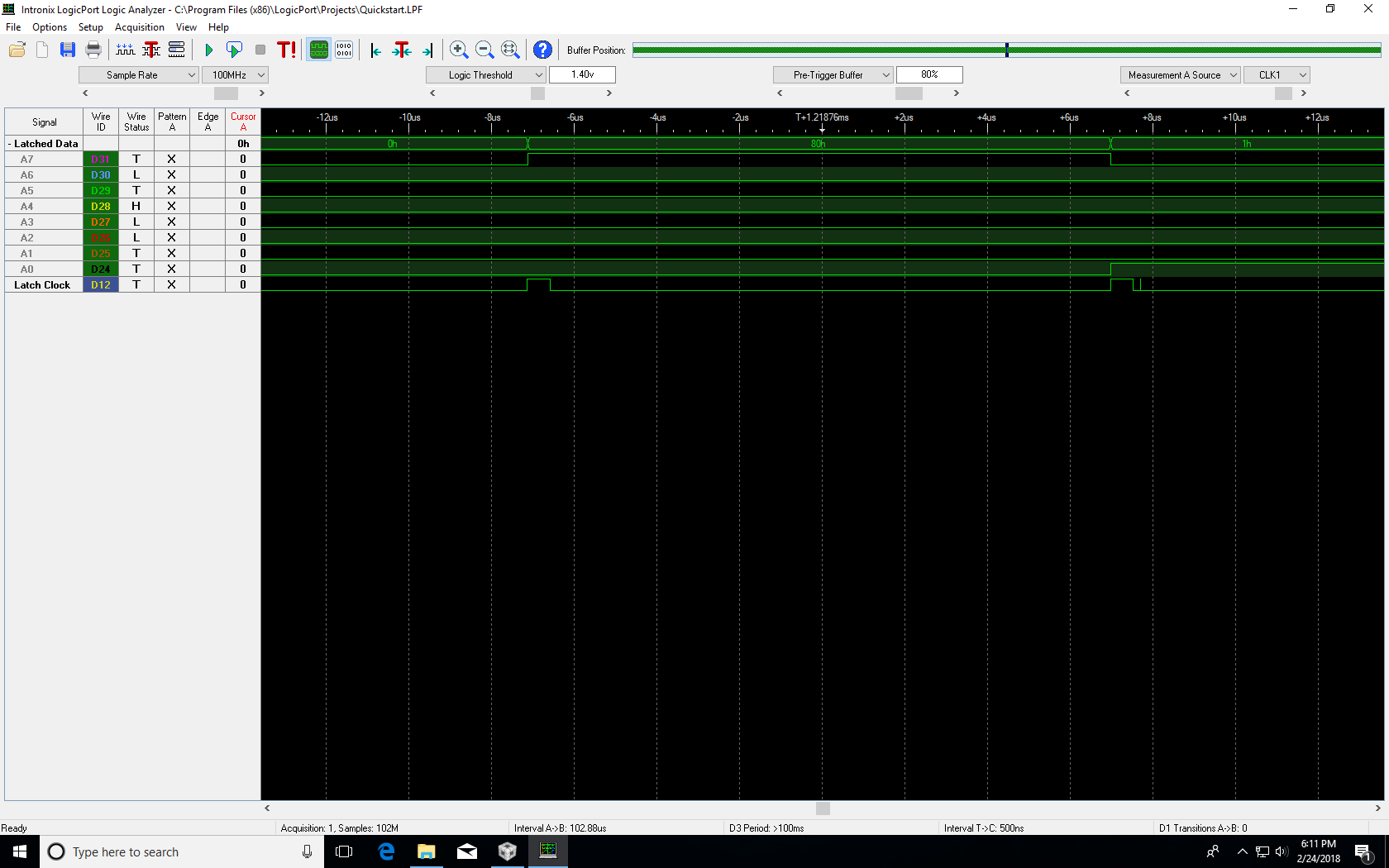


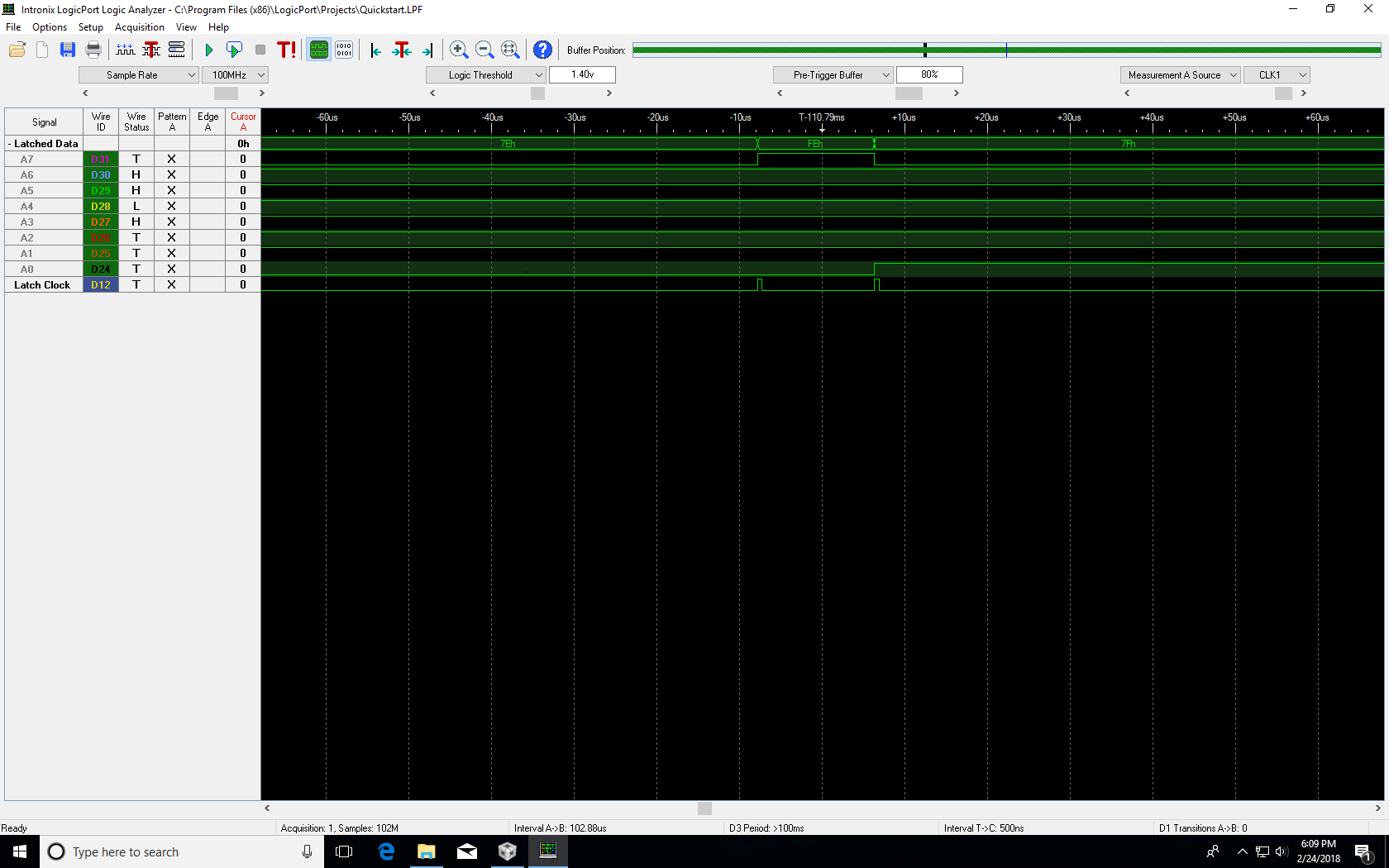
TLL-PL time 90ns

Data Latched (Supplemental)



Data Latched 80h (Supplemental)



Data Latched FEh (Supplemental)

DATA Latched in ISR FF (Supplemental)