Can a Self-Driving Car's Architecture Power a Home Robot?

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1 Introduction

A robotics company wants to recycle the computer module from a self-driving vehicle and use it in household cleaning robots. The compute module for the self-driving vehicle has an octa-core CPU, 16 GB LPDDR5 RAM, a 1.2 TOPS AI accelerator, dual 4K cameras and LIDAR, and a peak power draw of 100 W. This compute module is useful for illustrating computer architecture because it shows the process of using high-performance computing in a different domain, and implies different levels of power, cost, and performance. This analysis will compare what modifications would need to be made to the architecture of the self-driving car compute module in order to develop a resource-efficient household robot capable of performing important features for home robotics, such as 2D SLAM, person tracking, a battery life of 10 hours, and an average consumption of less than 10 W.

2 Background

Computer architecture principles focus on organizing computation resources with workload characteristics: the evolution of memory hierarchy and the maximization of parallelism of computation to achieve performance potential [Patterson & Hennessy, 2019]. Architectures for autonomous vehicles have used heterogeneous computing environments where general-purpose processing is integrated with special-purpose processing. This exists to achieve SLAM, path planning, and object detection fast enough to function at highway speeds, which could include vision processing. Performance on dedicated systems in the automobile sector, like NVIDIA Drive and Intel Mobileye, is focused on worst-case performance. As such, both of these currently operate on the principle of redundant processing, within one computer vision framework, that must reach a level of functional safety in an avoidance of a road collision.

Adaptive computing research indicates that robotic systems could alter their computational characteristics in part or whole; e.g., based on operational characteristics [Yadav et al., 2021]. Power optimization studies on mobile robotics show great power saving possibilities if done in a cooperative hardware/software manner; nonetheless, they typically process information in proprietary low-power architectures rather than using reuse of a generic high-performance framework. Literature shows perceivable gaps in cross-domain hardware reuse strategies with one of the key limitations found in automotive-to-consumer systems requiring 10x reduction in power.

3 Methodology

The strategy involves selective architectural downsizing through a more power-first optimization. The octa-core CPU required will be reduced to a quad-core CPU at 1.5 GHz (vs. 2.5 GHz for automotive applications) with an L2 cache hierarchy suitable for efficient indoor navigation algorithms. The memory subsystem will be a 4 GB LPDDR4 with aggressive power gating from a 16 GB LPDDR5 memory subsystem which is fine for both 2D occupancy maps and person detection models. The AI accelerator will go down to 0.5 TOPS with performance scaling. The use of structured light sensors in place of LIDAR will reduce power consumption by 60–80%.

3.1 Architectural Transformation

Component	Original	Power	Optimized	Power
CPU Cores	8-core	40 W	4-core	12 W
Memory	16 GB LPDDR5	15 W	4 GB LPDDR4	3 W
AI Accelerator	1.2 TOPS	20 W	0.5 TOPS	8 W
Sensors	LIDAR+4K	15 W	Structured	3 W
Storage	1 TB NVMe	5 W	128 GB eMMC	1 W
Total Power	100 W		8 W	92% reduction

Table 1: Architectural transformation with power savings.

Assumptions are that indoor navigation needs 90% less parallel processing than highway autonomy, that the 2D SLAM memory requires 15 times less than 3D mapping, and that the response latency has a raised tolerance of about 10 ms to about 200 ms. The approach optimizes those many layers of performance improvement by taking advantage of specialized sensor integration, improving energy costs via DVFS and power gating, reducing hardware costs via consumer grade components while maximizing effective navigation accuracy.

4 Discussion

This adaptation achieves a power reduction of 92% (from 100 W to 8 W) while maintaining a core capability for computation in indoor navigation. The performance summary indicates that 2D SLAM uses 2–4 GB memory compared to the original 16 GB, and has an 80% decrease in computational complexity as a function of travel through simpler environments. Moreover, this route allows a minimum of 10-hours run time from battery operation while accommodating additional obstacle avoidance through sound automotive sensor fusion algorithms. The major trade-offs were increased first bill of materials (BOM) costs from automotive-grade costing, but this is cancelable through faster development speeds and verified reliability. Factors that constrained the research were, first, an inability to scale because further reduction of power would have required a redesign on the silicon level for further power reductions. Moreover, errant candid insights include that limited architectural preservation (retaining the cache hierarchy and reducing the number of cores) is more effective than proportionally scaling. Lastly, substitution of sensors allowed greater power savings than optimization of computation only.

The ecological contribution of reusing car hardware is diverse. Positively, hardware reuse lengthens component life, lessens redundant R&D expenditure, and saves electronic waste while accelerating technology transfer from high-end automotive to consumer robotics markets. On the negative side, the incompatibility of power-unbounded automotive systems and battery-limited devices highlight the environmental cost of excessive engineering, where wasted computation is wasted energy and other resources. Thus, the future architecture revolves around flexibility and power-scaling through design operations related to reduced environmental footprints in ways that enable efficient cross-domain reuse.

5 Conclusion

Successful cross-domain hardware adaptation necessitates a complete redesign rather than simply a scaling of parameters. Reducing power consumption by 10x will ultimately require the careful selection of hardware components and optimum domain-specific adaptation. The main point of the architecture insight is that if we can retain high reusability features (i.e., cache hierarchies, sensor fusion) and modify domain-specific features (i.e., core count, memory capacity) aggressively, we increase the likelihood of attaining functional outputs. This approach helps design systems faster, sustain them longer via hardware reuse through lifecycle extension, and improve user experience by producing better navigable outcomes. Future work should establish formalized cross-domain assessment strategies, as well as investigate modular hardware designs that support efficient repurposing across applications.

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