

Reference Design for Automotive 8-Ch Class-D Amplifier With 2.1-MHz Switching Power Supply



TEXAS INSTRUMENTS

Description

This reference design shows how to implement an eight-channel, Class-D amplifier that is capable of driving 2- Ω loads and an off-battery step-down power supply with 5-V and 3.3-V outputs. The amplifier design provides audio inputs for each audio channel. A high-performance audio analog-to-digital converter (ADC) creates the digital data stream from the audio inputs and creates the digital timing for the system.

Resources

TIDA-00733	Design Folder
TAS6424-Q1	Product Folder
LM53635-Q1	Product Folder
PCM1865-Q1	Product Folder
LP5907-Q1	Product Folder
LP5912-Q1	Product Folder
LM74610-Q1	Product Folder



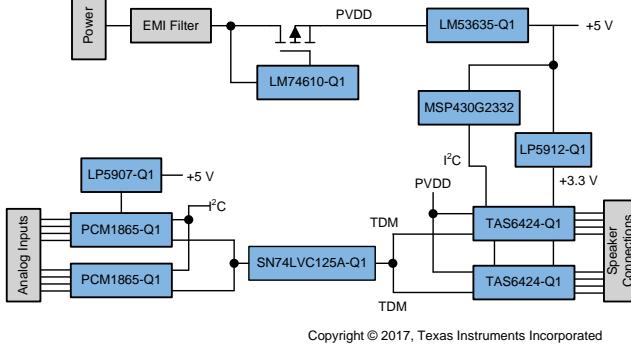
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Features

- Audio Output Power: 45 W per Channel at 10% THD + N
- Wide Power Supply Voltage Range of 4.5 V to 18 V
- 40-V Load Dump Protection
- Passes CISPR 25 Class 5 Radiated Emissions

Applications

- Head Unit
- Premium Amplifier



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1 System Description

The TIDA-00733 is an eight-channel, 2.1-MHz, automotive class-D, 45-W audio amplifier reference design that combines two four-channel class-D amplifiers with two four-channel audio analog-to-digital converters (ADCs) and a wide V_{IN} buck regulator to provide power for the system. The two TAS6424-Q1 class-D amplifier stages are designed to provide 2- Ω output capability. The design uses two PCM1865-Q1 audio ADCs. One PCM1865-Q1 ADC provides the digital audio timing reference required by the TAS6424s and the other PCM1865-Q1. Each PCM1865-Q1 digitizes four channels of analog audio and provides an output in eight-channel time-division multiplex (TDM) mode. The design includes an MSP430™ microcontroller (MCU) to initialize the PCM1865-Q1 and TAS6424-Q1 devices. The MCU provides the system configuration and control typically provided by an application processor or digital signal processor (DSP) in a typical automotive head unit or premium amplifier.

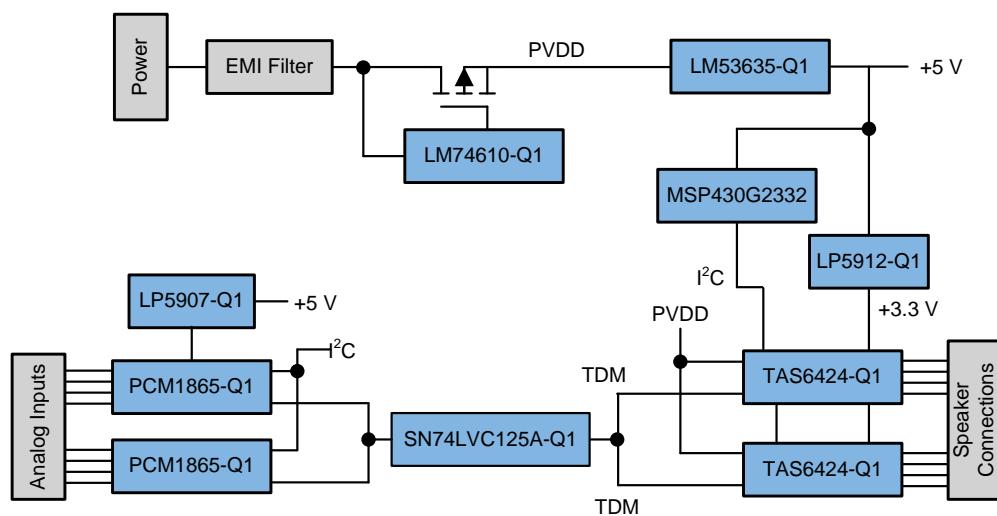
1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input power source	Automobile battery 4.5 V to 18 V with transients to 40 V
Operating temperature	-40°C to 125°C
Total harmonic distortion plus noise (THD + N)	0.013% typical at 1-W output with a 1-kHz signal
Signal input	Analog, 2.1 V _{RMS} max
Audio power output	36 W into 2 Ω with 1% THD + N
	45 W into 2 Ω with 10% THD + N
	22 W into 4 Ω with 1% THD + N
	27 W into 4 Ω with 10% THD + N
Form factor	145-mm × 114.5-mm rectangular PCB

2 System Overview

2.1 Block Diagram



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Figure 1. TIDA-00733 Block Diagram

2.2 Design Considerations

This design has several requirements beyond the primary specifications listed in the previous [Table 1](#).

The design must have a 3.3-V power supply on the board to power the digital portions of the circuit. The board must also have a way to configure itself so that it does not require external software to test the board.

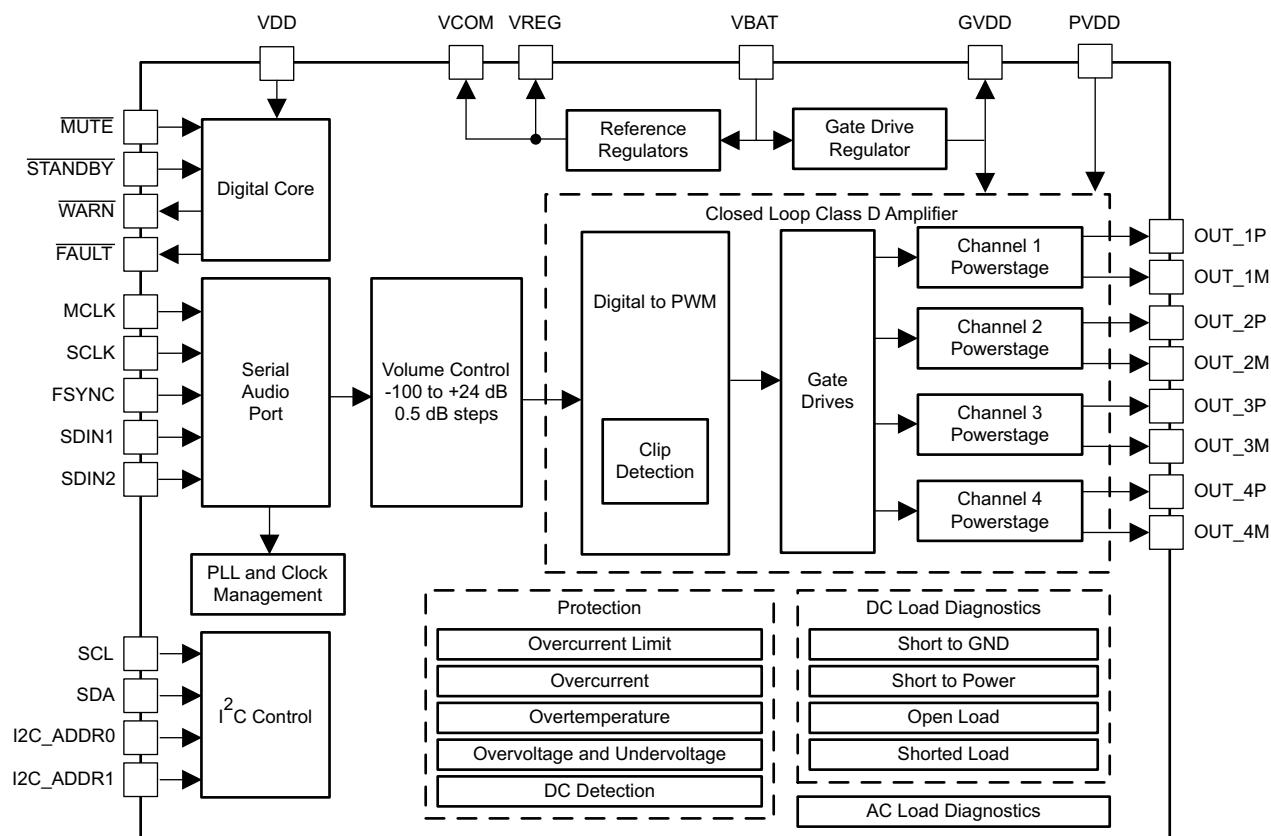
2.3 Highlighted Products

2.3.1 TAS6424-Q1

The TAS6424-Q1 device is a four-channel digital input Class-D audio amplifier that implements a 2.1-MHz PWM switching frequency, which, in turn, enables a cost-optimized solution in a very-small PCB size, full operation down to 4.5 V for start and stop events, and exceptional sound quality with up to 40-kHz audio bandwidth.

The TAS6424-Q1 Class-D audio amplifier is designed for use in automotive head units and external amplifier modules. The device provides four channels (see Figure 2) at 27 W into 4 Ω at 10% THD+N, 45 W into 2 Ω at 10% THD+N from a 14.4-V supply, and 75 W into 4 Ω at 10% THD+N from a 25-V supply. The Class-D topology dramatically improves efficiency over traditional linear amplifier solutions. The designer can set the output switching frequency either above the AM band, which eliminates the AM-band interference and reduces output filter size and cost, or below the AM band to optimize efficiency.

For a pin-compatible two-channel amplifier, see the TAS6422-Q1. The device is offered in a 56-pin HSSOP PowerPAD™ package with the exposed thermal pad up.

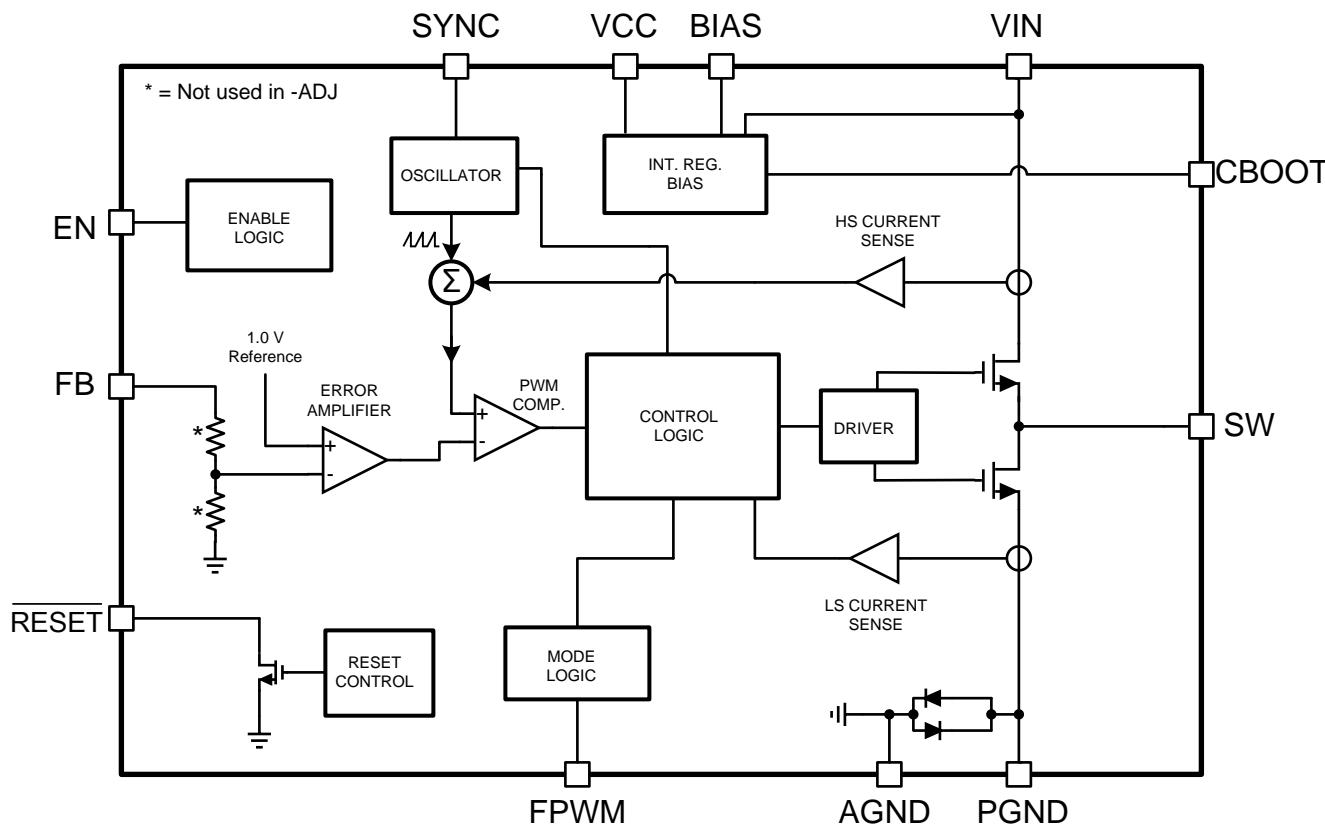


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Figure 2. TAS6424-Q1 Functional Block Diagram

2.3.2 LM53635-Q1

The LM53625-Q1/LM53635-Q1 synchronous buck regulator is optimized for automotive applications, providing an output voltage of 5 V, 3.3 V, or an adjustable output (see Figure 3). Advanced high-speed circuitry allows the LM53625-Q1/LM53635-Q1 to regulate from an input of 18 V to an output of 3.3 V at a fixed frequency of 2.1 MHz. Innovative architecture allows this device to regulate a 3.3-V output from an input voltage of only 3.55 V. All aspects of the LM53625-Q1/LM53635-Q1 are optimized for automotive and performance-driven industrial customers. An input voltage range up to 36 V, with transient tolerance up to 42 V, eases input surge protection design. The automotive-qualified HotRod™ QFN package with wettable flanks reduces parasitic inductance and resistance while increasing efficiency, minimizing switch node ringing, and dramatically lowering electromagnetic interference (EMI). An open-drain reset output, with built-in filtering and delay, provides a true indication of system status. This feature negates the requirement for an additional supervisory component, which saves on cost and board space. The seamless transition between pulse-width modulation (PWM) and pulse-frequency modulation (PFM) modes and low quiescent current (only 15 μ A for the 3.3-V option) ensure high efficiency and superior transient responses at all loads.



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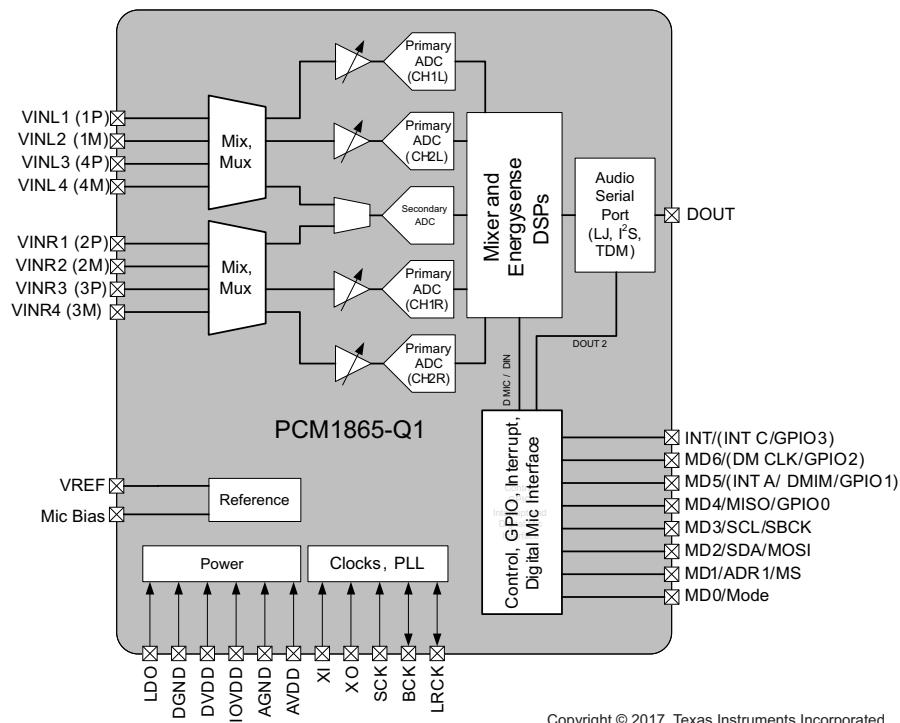
Figure 3. LM53635-Q1 Functional Block Diagram

2.3.3 PCM1865-Q1

The PCM1865-Q1 audio front-end device takes a new approach to audio-function integration to ease compliance with European Ecodesign legislation while enabling high-performance end products (see Figure 4). Smaller, smarter products are becoming increasingly feasible at reduced costs without the requirement for a 5-V supply or an external programmable-gain amplifier.

The highly-flexible audio front end of the PCM1865-Q1 supports input levels from small-mV microphone inputs to 2.1-V_{RMS} line inputs without external resistor dividers. The PCM1865-Q1 integrates many system-level functions that assist or replace some digital signal processing (DPS) functions.

All of these features are available using a single 3.3-V power supply. An integrated band-gap voltage reference provides excellent power supply rejection ratio (PSRR) such that a dedicated analog 3.3-V rail may not be required.



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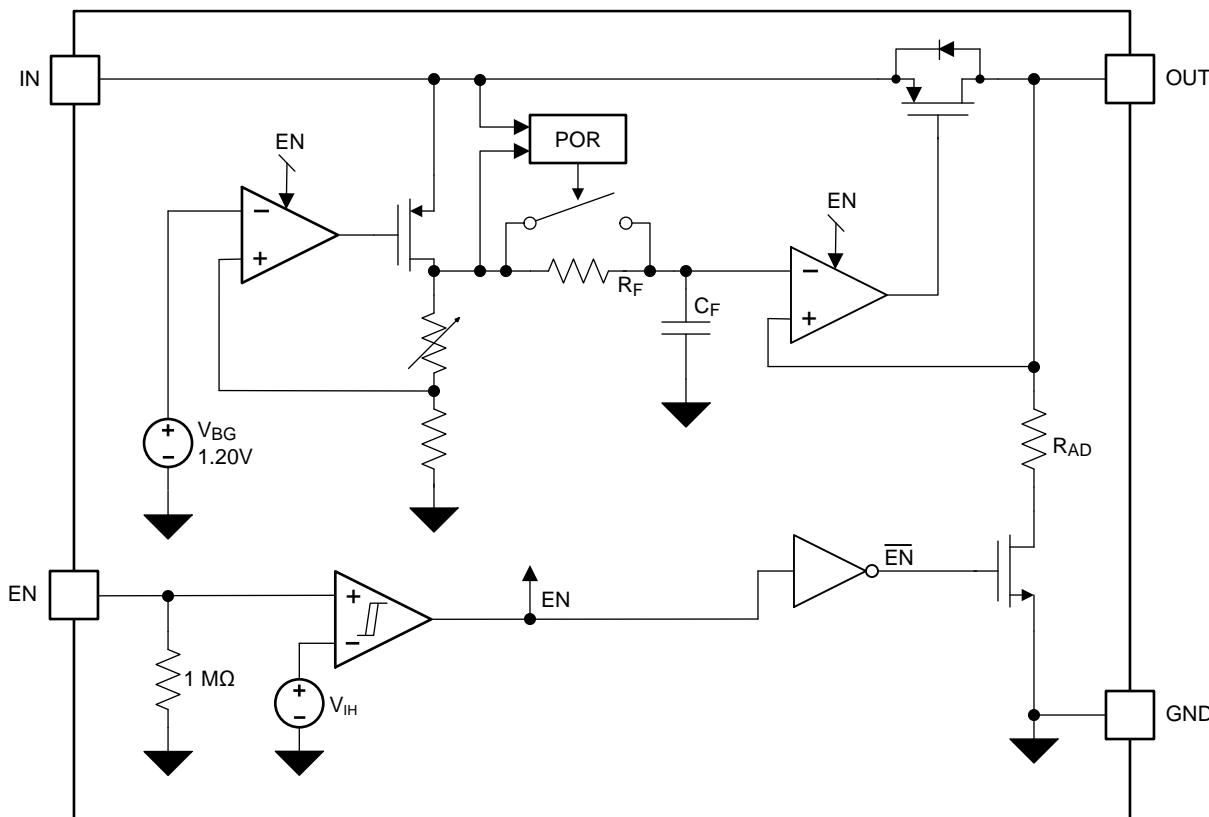
Figure 4. PCM1865-Q1 Simplified Block Diagram

2.3.4 LP5907-Q1

The LP5907-Q1 is a low-noise low-dropout linear regulator (LDO) that can supply 250 mA of output current (see [Figure 5](#)). Designed to meet the requirements of RF and analog circuits, the LP5907-Q1 device provides low noise, high PSRR, low quiescent current, and low line- or load-transient response figures. Using new innovative design techniques, the LP5907-Q1 offers class-leading noise performance without a noise bypass capacitor and the ability for remote output capacitor placement.

The device is designed to work with a 1- μ F input and a 1- μ F output ceramic capacitor (and does not require a separate noise bypass capacitor).

This device is available with fixed output voltages from 1.2 V to 4.5 V in 25-mV steps. Contact Texas Instruments Sales for specific voltage option requirements.



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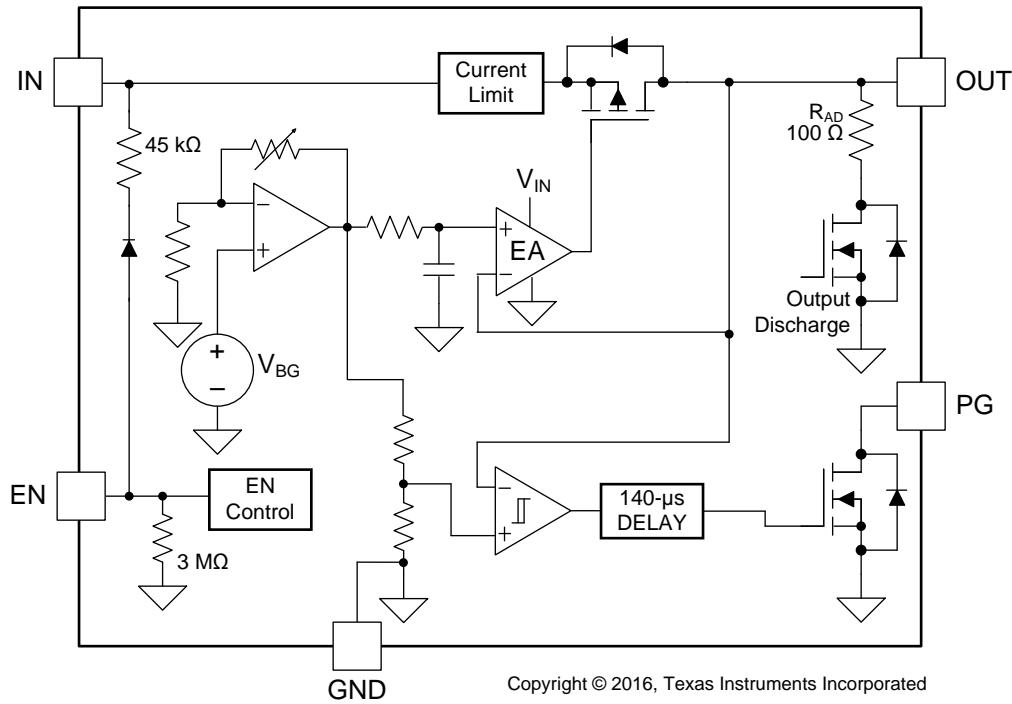
Figure 5. LP5907-Q1 Functional Block Diagram

2.3.5 LP5912-Q1

The LP5912-Q1 is a low-noise LDO that can supply up to 500 mA of output current (see [Figure 6](#)). Designed to meet the requirements of RF and analog circuits, the LP5912-Q1 device provides low noise, high PSRR, low quiescent current, and low line- and load-transient response. The LP5912-Q1 offers class-leading noise performance without a noise bypass capacitor and with the ability for remote output capacitance placement.

The device is designed to work with a 1- μ F input and a 1- μ F output ceramic capacitor (and does not require a separate noise bypass capacitor).

This device is available with fixed output voltages from 0.8 V to 5.5 V in 25-mV steps. Contact Texas Instruments Sales for specific voltage option requirements.



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Figure 6. LP5912-Q1 Functional Block Diagram

2.3.6 LM74610-Q1

The LM74610-Q1 is a controller device which is specified for use with an N-Channel MOSFET in a reverse polarity protection circuitry (see [Figure 7](#)). The device is designed to drive an external MOSFET to emulate an ideal diode rectifier when connected in series with a power source. A unique advantage of this scheme is that it is not referenced to ground and thus has zero I_Q .

The LM74610-Q1 controller provides a gate drive for an external N-Channel MOSFET and a fast-response internal comparator to discharge the MOSFET gate in the event of reverse polarity. This fast pulldown feature limits the amount and duration of reverse current flow if opposite polarity is sensed. The device design also meets CISPR25 Class-5 EMI specifications and automotive ISO7637 transient requirements with a suitable transient voltage suppression (TVS) diode.

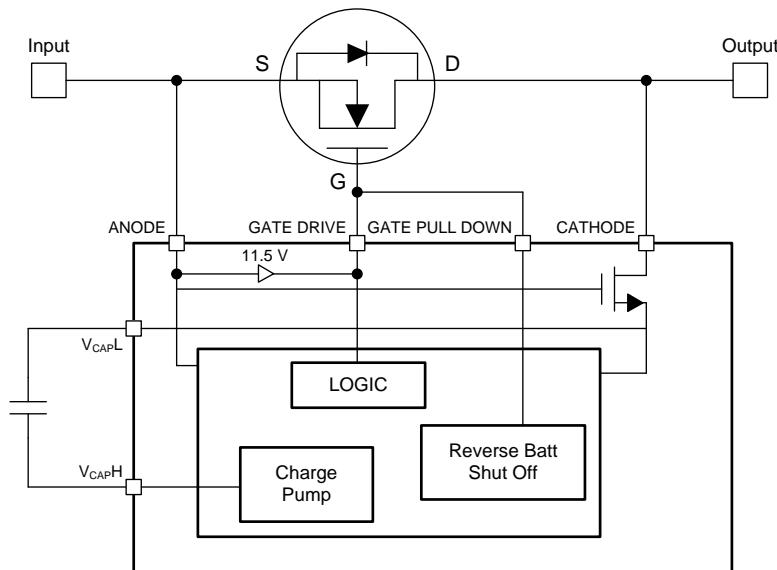


Figure 7. LM74610-Q1 Functional Block Diagram

2.3.7 SN74LVC125A-Q1

The SN74LVC125A-Q1 quadruple-bus buffer gate is designed for 1.65-V to 3.6-V V_{CC} operation (see [Figure 8](#)).

The SN74LVC125A-Q1 features independent line drivers with three-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} must be tied to V_{CC} through a pullup resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

Drive the inputs from either 3.3-V or 5-V devices, for which they are specified. This feature allows the use of this device as a translator in a mixed 3.3-V or 5-V system environment.

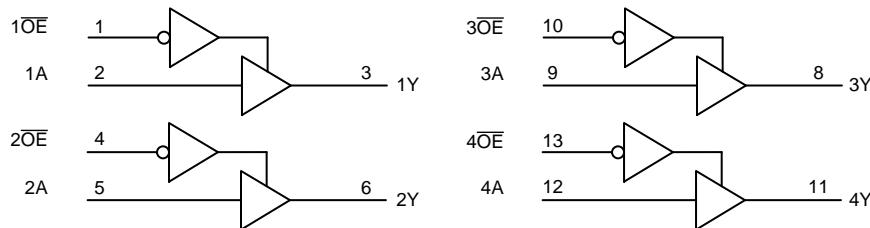


Figure 8. SN74LVC125A-Q1 Logic Diagram (Positive Logic)

2.3.8 TLV2462A-Q1

The devices in the TLV246x-Q1 family of low-power rail-to-rail input and output operational amplifiers are well suited for battery management systems in electric vehicles (EVs), hybrid electric vehicles (HEVs), and powertrain as well as lighting and roof module systems in body and lighting applications. The input common-mode voltage range extends beyond the supply rails for maximum dynamic range in low-voltage systems. The amplifier output has rail-to-rail performance with high-output-drive capability, solving one of the limitations of older rail-to-rail input and output operational amplifiers. This rail-to-rail dynamic range and high output drive make the TLV246x-Q1 ideal for buffering ADCs.

The operational amplifier has a 6.4-MHz bandwidth and a 1.6-V/ μ s slew rate with only 500- μ A supply current, which provides good AC performance with low-power consumption. Devices are available with an optional shutdown terminal, which places the amplifier in an ultra-low supply current mode ($I_{DD} = 0.3 \mu A$ per channel). While in shutdown, the operational amplifier output enters a high-impedance state. DC applications are also well served with an input noise voltage of 11 nV/ \sqrt{Hz} and input offset voltage of 100 μV .

[Figure 9](#) shows the TLV2462A-Q1 functional block diagram.

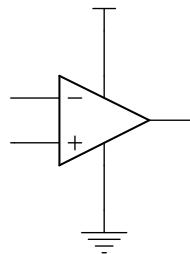


Figure 9. TLV2462A-Q1 Functional Block Diagram

2.3.9 MSP430G2332

The Texas Instruments MSP430™ family of ultra-low-power MCUs consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μ s.

The MSP430G2332 series of MCUs are ultra-low-power, mixed-signal microcontrollers with built-in 16-bit timers and up to 16 I/O touch-sense enabled pins and built-in communication capability using the universal serial communication interface (see Figure 10). The MSP430G2332 series have a 10-bit ADC. For configuration details, see the *Available Options* table in the [MSP430G2xx2](#) data sheet. Typical applications include low-cost sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system.

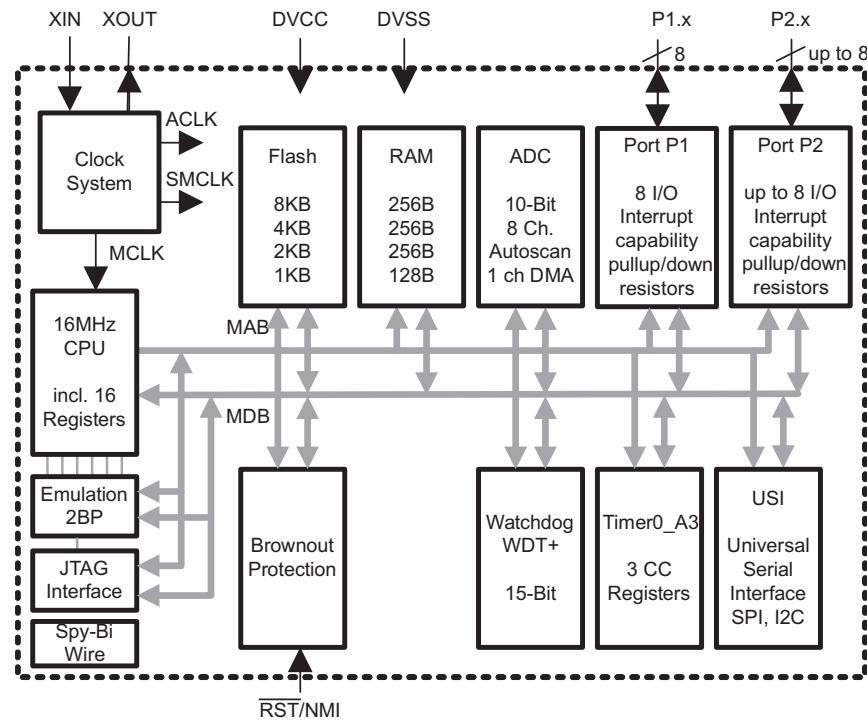


Figure 10. MSP430G2332 Functional Block Diagram

2.4 System Design Theory

2.4.1 Hardware Overview

This user's guide instructs how to evaluate several different functions of components used in the design. The PCM1865-Q1 is shown as both the timing master and slave in this configuration and the two PCM1865-Q1 digital outputs are tied together to provide eight-channel digital audio. The TDM timing and data signals are buffered using an SN74LVC125A-Q1 quad buffer. The TDM input provides timing for the TAS6424-Q1 amplifiers. The TAS6424-Q1 provides audio outputs capable of driving 2- Ω - or 4- Ω speaker loads. The LM53635-Q1 buck regulator supplies 5 V, which is used to power the LP5907-Q1 and LP5912-Q1 regulators and also provides enough capacity to power other in-system loads. The LP5907-Q1 and LP5912-Q1 devices each provide 3.3 V to different parts of the circuit. The LM74610-Q1 circuit replaces a rectifier diode to reduce the power loss while still providing reverse voltage protection.

The TIDA-00733 is designed to use an enclosure to simulate the housing used in a typical head unit or premium amplifier. The enclosure, a Hammond 1590J, provides EMI shielding in addition to acting as the system heat sink after installing the TIDA-00733 design within.

[Figure 11](#) and [Figure 12](#) show the complete TIDA-00733 PCB.

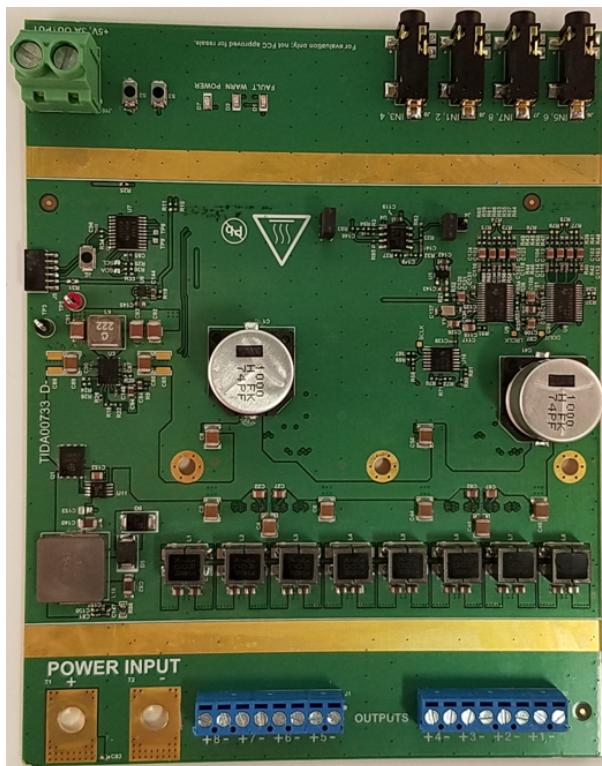


Figure 11. TIDA-00733 PCB—Top

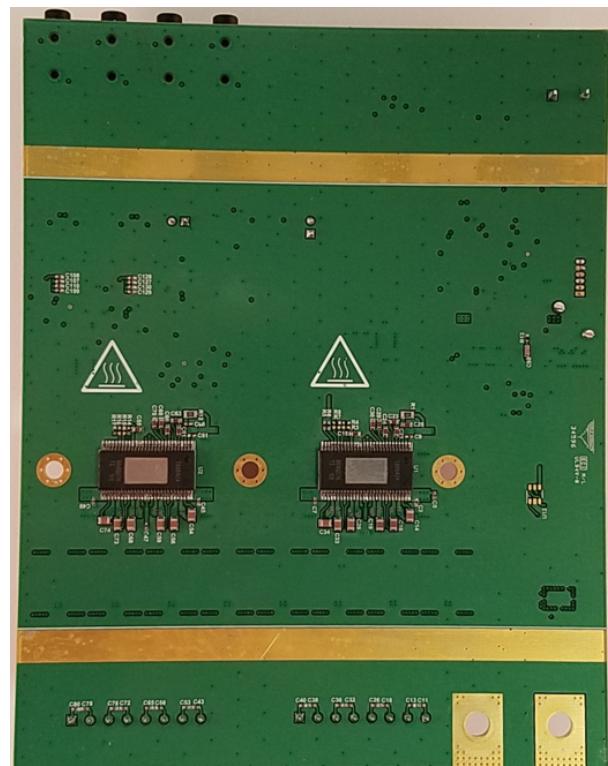


Figure 12. TIDA-00733 PCB—Bottom

2.4.1.1 PCB Outline and Interface

The printed-circuit board (PCB) for the TIDA-00733 is designed to create the shortest path for power to the TAS6424-Q1 class-D amplifiers. The board size is 145 mm × 114.5 mm (5.7 in × 4.5 in). Some of the board area is required for the necessary connectors to bring in external audio signals, the power connectors, and the speaker output connectors. The primary circuitry fits in an area that is 86.9 mm × 114.5 mm (3.4 in × 4.5 in).

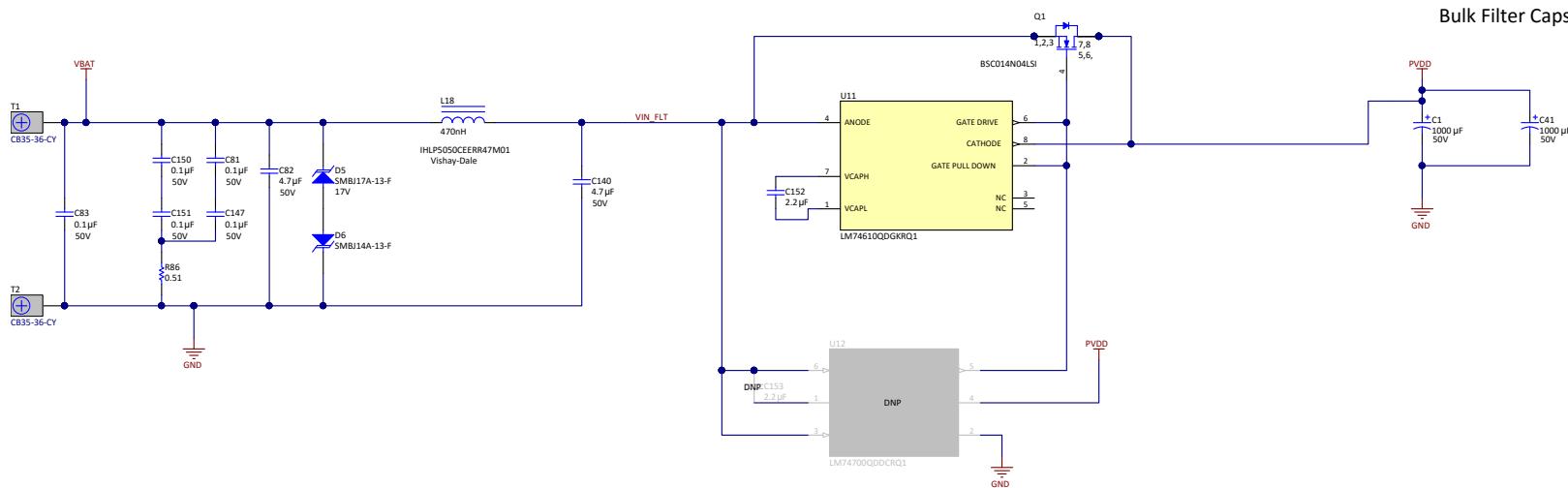
2.4.1.2 Power

The TIDA-00733 is designed to be powered by an automotive 12-V power system. The TAS6424-Q1 device has two power rails which connect directly to a main power input. The V_{BAT} is connected to the TAS6424-Q1 at pin 3. V_{BAT} can be in the range of 4.5 V to 18 V. P_{VDD} must be in the range of 4.5 V to 26.4 V. The V_{BAT} limits the input voltage range of the TIDA-00733 design due to its lower maximum level. The rest of the components in the system operate at 3.3 V; therefore regulators are provided to create 3.3 V from the 5 V that the LM53635L circuit supplies.

The main power input from the battery is filtered with a pi filter to reduce noise entering the system as well as reducing noise conducted out of the system on the power lines. Capacitors C81, C82, C147, C150, and C151 are on the input side and are placed in different places along the power input line to provide filtering where necessary. C81, C147, C150, and C151 along with R86 provide a filter just inside the system enclosure to short any high-frequency noise on the power lines and prevent the noise from entering or exiting the system. C82 is placed between these capacitors and the main filter inductor, L18. C140 is the last section of the pi filter and the LM74610 smart diode circuit. The pi filter further reduces any noise on the power line. The construction of L18 is very important. L18 must be a shielded inductor to reduce EMI emissions. A non-shielded inductor can act as an antenna and receive emissions inside the box and couple them onto the power line. This EMI can then be radiated outside the box.

2.4.1.2.1 LM74610-Q1

The LM74610-Q1 provides reverse battery protection when using it in conjunction with an N-channel MOSFET (see [Figure 13](#)). The MOSFET is connected with the source and drain pins reversed from the normal connection. This configuration allows the body diode to conduct if the MOSFET is off and the input power is connected. A charge pump in the LM74610 charges capacitor C152 and uses the stored voltage to provide the gate drive to MOSFET Q1. The benefit to this circuit is that the amount of power dissipated in the reverse protection circuit is much lower than it would be than when using a typical Schottky rectifier because the voltage drop is much lower with the MOSFET. This observation is very important in designs like the TIDA-00733 where load currents as high as 40 A are possible.



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Figure 13. LM74610-Q1 Smart Diode Circuit and Power Input

2.4.1.2.2 LM53635L-Q1

The LM53635L-Q1 regulator provides a regulated 5-V_{DC} for use by the linear regulators and as a source of power for auxiliary loads (see [Figure 14](#)). The LM53635L-Q1 has been selected because of its input voltage range (4 V to 36 V), efficiency, and electromagnetic interference (EMI) performance. The LM53635L-Q1 is a fixed 5-V output device. The LM53635L-Q1 also has spread-spectrum operation when used without synchronization. Spread-spectrum operation improves EMI performance.

The LM53635L-Q1 circuit follows the recommendations from the data sheet for choosing components. The power input is filtered with two 10-uF capacitors and two 0.1-uF capacitors placed on each side of the part to provide balanced filter paths at the LM53635-Q1 (U3) input.

R24 pulls the U1 pin 16 to the input voltage PVDD. Pin 16, which is called FPWM, controls the operating mode of the LM53635L-Q1 device. Pulling pin 16 low sets U1 for auto light-load mode, which is not employed in this system. Pin 16 is pulled high to force PWM mode all of the time; this configuration limits the efficiency of the LM53635L-Q1 at light loads by forcing the switching frequency to remain the same. This outcome is desirable in an audio system to reduce the possible creation of audible beat frequencies that couple into the audio path due to skipped pulses, which effectively lower the switching frequency. Pin 16 must also be pulled high if using an external synchronization signal with the LM53635L-Q1.

At the output of the LM53635L-Q1 circuit, C84 provides the boost required to drive the N-channel MOSFET switch of the LM53635-Q1 device. R9 is provided to slow any transients (if present). C98 and R13 are a snubber for high-frequency transients. L9, C91, C92, and C93 provide the necessary output filtering for the regulated +5 V. L9 is a shielded inductor to reduce EMI effects. Pin 22 provides an internal bias to the LM53635L-Q1 device and is connected to the output through R22 and C146, which provide a low-pass filter. C146 is tied to pin 20, AGND, before they have both been connected to the main system ground through a net-tie. VCC is also bypassed to AGND through C94. LED D7 is connected to the 5-V output as a power-on indicator. J10 is provided to connect an external load to test the power output capability. D7 and J10 are placed outside the area where the box encloses the main part of the circuit.

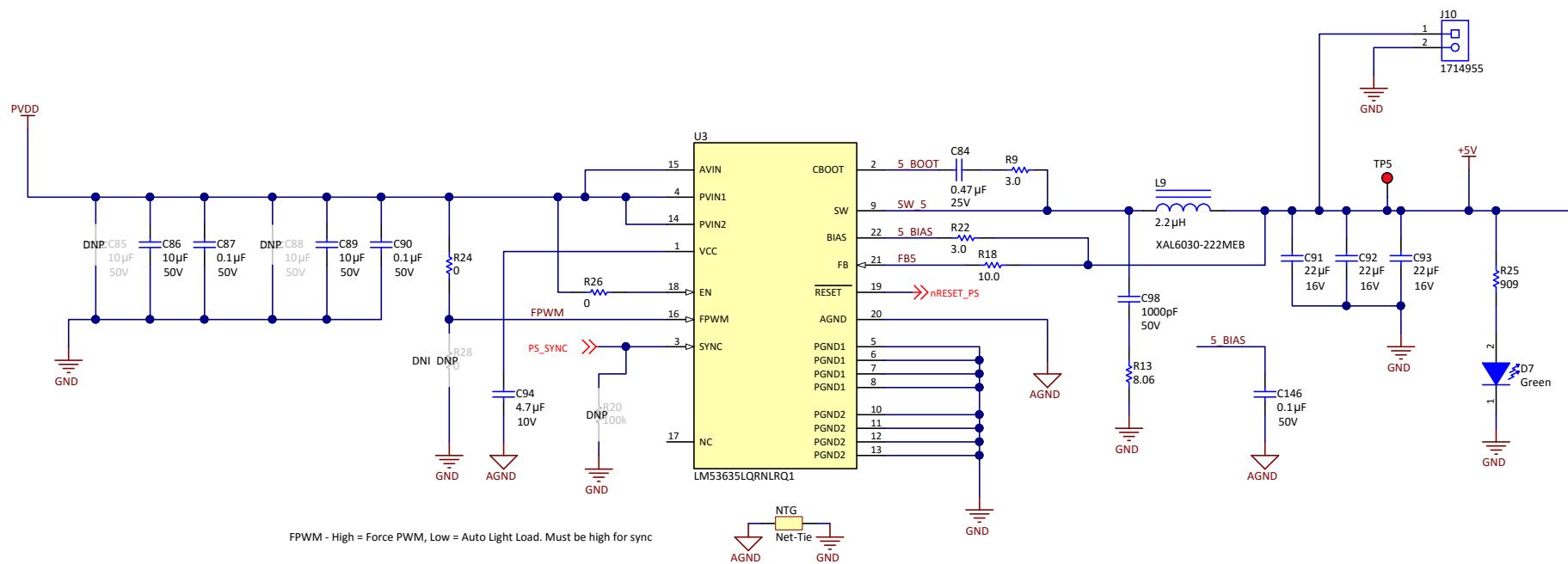
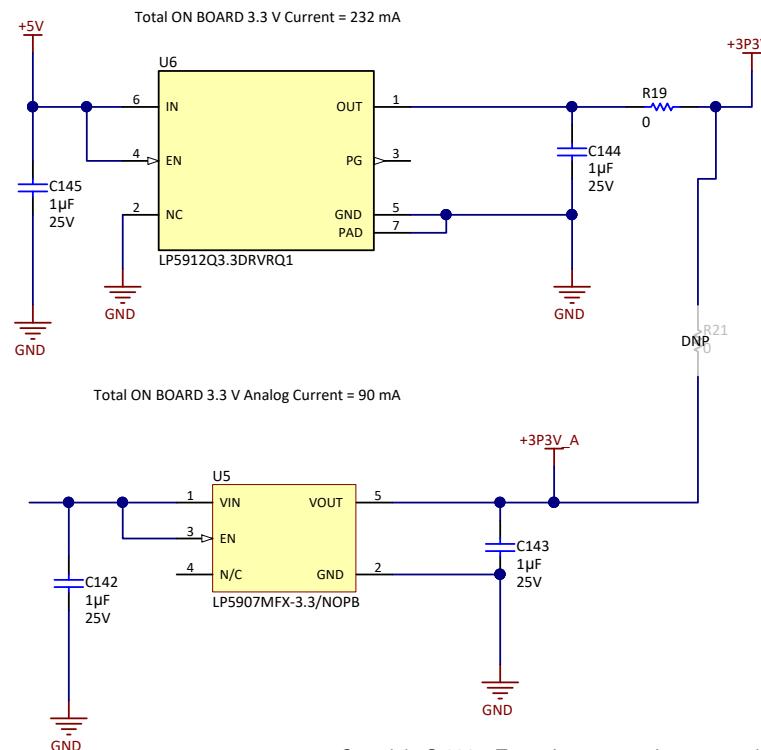


Figure 14. LM53635L-Q1 Regulator Circuit

2.4.1.2.3 LP5907-Q1 and LP5912-Q1

Two linear regulators are provided for +3.3 V. U6, the LP5912-Q1, is used for all digital +3.3-V requirements, which includes the MSP430, the digital part of the PCM8165-Q1 devices, the SN74LVC125A-Q1 logic buffer, and the VDD connections on the TAS6424-Q1 devices. U5, the LP5907-Q1, provides +3.3 V for the analog portions of the PCM1865-Q1 devices to ensure low noise in the ADCs of the two parts. R21 is provided to allow testing with U5 removed.

Figure 15 shows the LP5912-Q1 and LP5907-Q1 circuits.



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Figure 15. LP5912-Q1 and LP5907-Q1 Circuits

2.4.1.3 PCM1865-Q1

The PCM1865-Q1 is ideal for this design (see [Figure 16](#) and [Figure 17](#)). Eight ADC channels are required to provide the eight channels of digital data for the two TAS6424-Q1 devices.

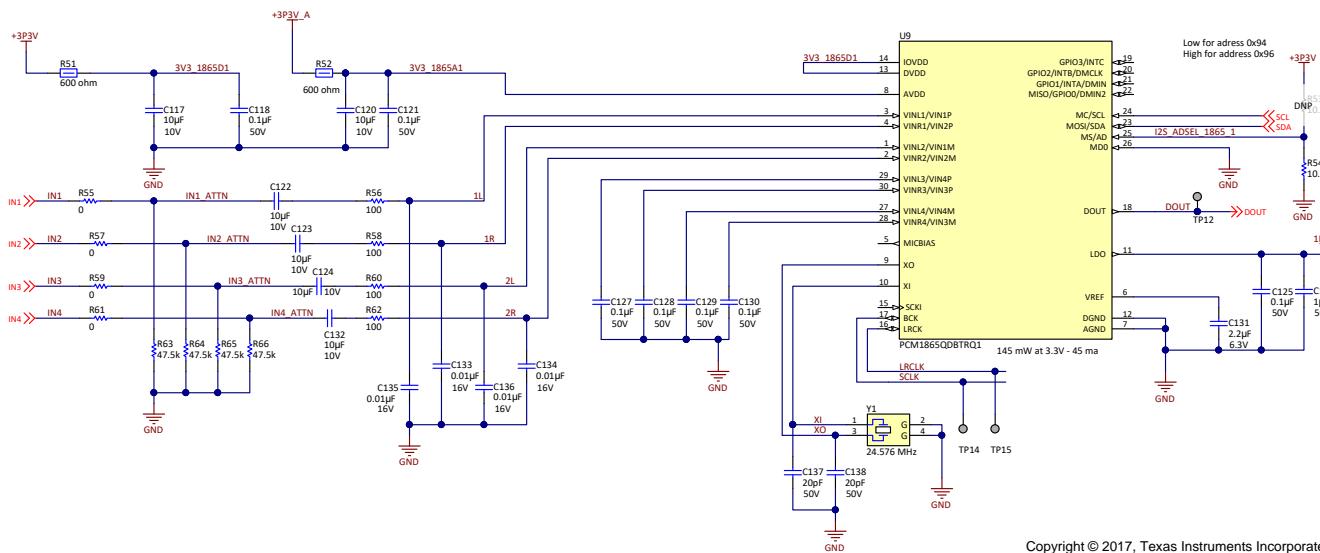
The PCM1865-Q1 has an internal clock generator to create the TDM data stream. U9 is configured as a timing master and provides timing for U1, U2, and U8. A 24.576-MHz crystal, Y1, is the oscillator timing reference.

The power to the PCM1865-Q1 is +3.3 V. The digital I/O and internal digital circuits are supplied through the IOVDD and DVDD pins 14 and 13, which are connected together. The PCM1865-Q1 generates high-frequency digital signals and noise that can couple onto pins 13 and 14. This high-frequency noise can couple to the board power lines and become radiated emissions. R35 and R51, at U8 and U9 respectively, are ferrites that provide high-frequency filtering to reduce the probability of high-frequency emissions.

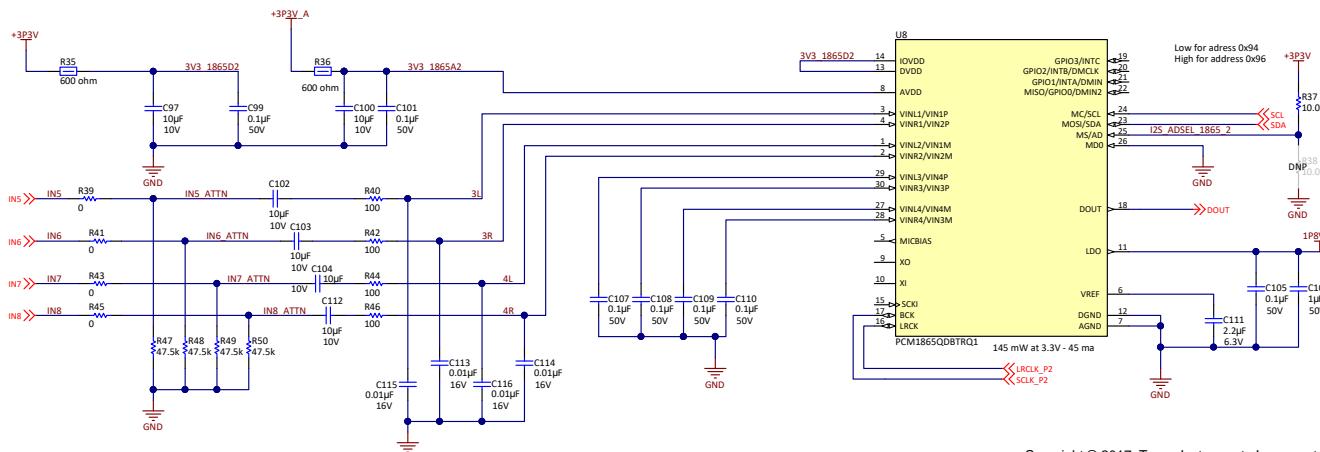
Power supply filtering and bypass capacitors C97, C99, C117, and C118 are placed close to pins 13 and 14 of the two PCM1865-Q1 devices. The +3.3 V for the analog section, AVDD, is filtered by C100, C101, C120, and C121. All of the 0.1- μ F capacitors are placed close to the power pins on the PCM1865-Q1 devices to provide transient filtering. Two ferrites, R36 and R52, provide high-frequency filtering of the +3.3-V power to prevent noise from affecting the sensitive ADC portions of the ICs.

The four analog inputs of each PCM1865-Q1 are configured as single-ended inputs. Several passive components are required to couple the analog signal into each ADC channel of the PCM1865-Q1 device. Each input has a 47.5-k Ω impedance which is set by a resistor to ground. A 0- Ω series resistor is provided to create a resistive divider with the 47.5-k Ω resistor if the input voltage will exceed 2.1 V_{RMS}. Next, a 10- μ F capacitor AC couples the input. This circuit is followed by a 100- Ω resistor and a 0.01- μ F capacitor to provide a low-pass filter with a cutoff frequency of 159 kHz. The high cutoff frequency is chosen to ensure that the signal has only been attenuated by -0.077 dB at 20 kHz and that the signal bandwidth is sufficient for the 96-kHz sampling frequency of the PCM1865s. All eight analog inputs have the same circuit. The designer can also use several unpopulated resistors to connect the different inputs together so that one signal source can drive multiple channels. The eight input channels have a corresponding output channel on a TAS6424-Q1 device.

The digital interface on the PCM1865-Q1 devices include an I²C interface and the digital audio interface. The I²C interface connects to the system MCU and is used to configure the PCM1865-Q1 devices. The digital audio interface consists of three signals: SCLK, LRCLK, and DOUT. SCLK is the serial or BIT clock. In some applications and on the PCM1865-Q1 data sheet, this signal is called BCLK or BCK. The LRCLK signal is the left-right clock, also known as the word clock. This clock indicates the start of a data frame for TDM configured data. The frequency of LRCLK is equal to the sampling clock frequency. DOUT is the data output. The TDM output is configured for eight data words to be compatible with the TDM requirements of the TAS6424-Q1. The DOUT data words are 24 bits each, though the data stream is configured for 32-bit words. For this design, the audio sampling rate is 96 kHz. Consequently, SCLK is 24.576 MHz. The designer can set the audio sampling rate to either 48 kHz or 44.1 kHz if desired. U9 is configured as the timing master and provides the two timing signals as well as filling the first four data time slots for TDM. PCM1865-Q1 U8 receives timing and provides data outputs in the last four TDA time slots. The DOUT pins of the two PCM1865-Q1 devices are tied together. When a PCM1865-Q1 output is idle, it is in a high-impedance state so that the other PCM1865-Q1 device can drive the output. In this way, two PCM1865-Q1 devices provide a single data stream for TDM.



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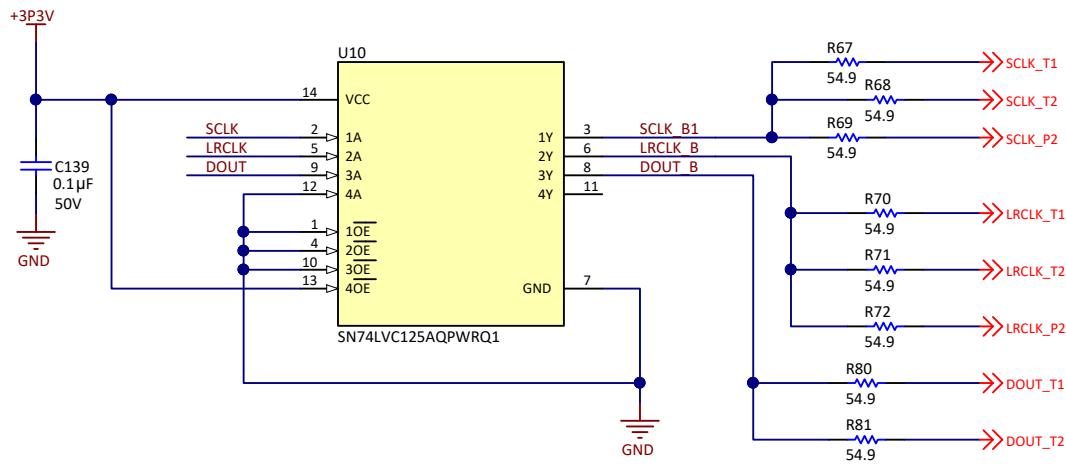
Figure 16. PCM1865-Q1 Circuits—Master PCM1865-Q1


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Figure 17. PCM1865-Q1 Circuits—Slave PCM1865-Q1

2.4.1.4 SN74LVC125A-Q1

An SN74LVC125A-Q1 quad buffer is provided to add drive strength to the TDM signals (see [Figure 18](#)). SCLK and LRCLK both have three loads, while DOUT has two. PCM1865-Q1 U9 drives the clock signals SCLK and LRCLK to the SN74LVC125A-Q1 device and the buffered clock outputs are routed to PCM1865-Q1 U8 and the two TAS6424-Q1 devices through separate PCB traces. The signals are separated with one resistor for each path to isolate the signals and to provide a way to reduce signal overshoot and undershoot at the load ends. The two PCM1865-Q1 DOUT signals are connected together and fed through the SN74LVC125A-Q1 and the two TAS6424-Q1 devices, again through separate resistors and traces. The output series resistors are placed near the SN74LVC125A-Q1 to provide the best signal correction. The value for the resistors was chosen to reduce signal undershoot on the signals while still providing adequate rise and fall time for the TAS6424-Q1 devices and the slave PCM1865-Q1. These resistors help to reduce EMI by reducing the strength of undesired high-frequency signals.



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Figure 18. SN74LVC125A-Q1 Circuit

2.4.1.5 TAS6424-Q1

The TAS6424-Q1 is a 75-W class-D audio power amplifier that operates with a switching frequency of 2.1 MHz (see [Figure 19](#) and [Figure 20](#)). The TAS6424-Q1 has a digital audio input which is compatible with I²S and TDM digital audio data. The digital audio input enables a system designer to eliminate an analog signal chain that connects from an audio digital-to-analog converter (DAC), through the circuit board, and to the power amplifier. Removing this analog signal chain reduces the risk of noise interference in the audio signal. The TAS6424-Q1 has load dump protection, so the designer can connect the power pins for P_{VDD} and P_{VDD} directly to the car battery system. The TIDA-00733 design uses two TAS6424-Q1 devices, U1 and U2.

The TAS6424-Q1 has three voltage inputs. V_{DD} is a logic-level supply connected at U1 pin 19 and must be in the range of 3 V to 3.5 V. V_{BAT} is connected to the TAS6424-Q1 at pin 3. P_{VDD} connects to U1 pins 2, 29, 30, 42, 43, 55, and 56. Other voltages are generated inside the TAS6424-Q1. V_{REG} is an internal regulator, which is bypassed to A_{REF} through a capacitor. V_{COM} is an internal reference, which is also bypassed to A_{REF}. The two voltages G_{VDD} form the gate drive for the output high-side MOSFETs. Pin 9 is the G_{VDD} for outputs 3 and 4 while pin 10 is the G_{VDD} for outputs 1 and 2. Both pins are bypassed to ground with 1- μ F capacitors.

Pins 12 through 16 form the digital audio input to the TAS6424-Q1 device from the PCM1865-Q1 device. Pin 20, MCLK, is tied directly to SCLK because MCLK and SCLK can be the same frequency when using a TDM input. Pins 20 and 21 are the I²C interface. Pins 22 and 23 set the address for the I²C. In this design, U1 and U2 require different addresses so that the designer may configure them differently. Pin 24 is the nSTANDBY function. If the designer sets this signal low, the TAS6424-Q1 device is in a low-power standby state. This function is not for use in TIDA-00733. Pin 25 is the nMUTE function. When this signal is low, the outputs of the TAS6424-Q1 are muted, but the operating state of the device is maintained. Pins 24 and 25 must be pulled up by resistors or a processor for the TAS6424-Q1 device to operate. Pins 26 and 27, /FAULT and /WARN, are open-drain outputs. These pins function as light-emitting diode (LED) drivers, as [Figure 20](#) shows, or as processor interrupts. Pin 26 is asserted low when a defined fault condition exists. Pin 27 is asserted low when clipping occurs or if the TAS6424-Q1 device has passed the overtemperature warning threshold. For further details, see [TAS6424-Q1 75-W, 2-MHz Digital Input 4-Channel Automotive Class-D Audio Amplifier With Load-Dump Protection and I²C Diagnostics](#).

Each output channel is a bridge-tied load (BTL) output. This topology requires a low-pass filter for both the positive- and negative-going outputs of each channel. The output inductors for TIDA-00733 have been chosen to provide enough current capacity to power 2- Ω loads. A dual inductor has been used to save space. The two inductors in each package are *not* magnetically coupled together.

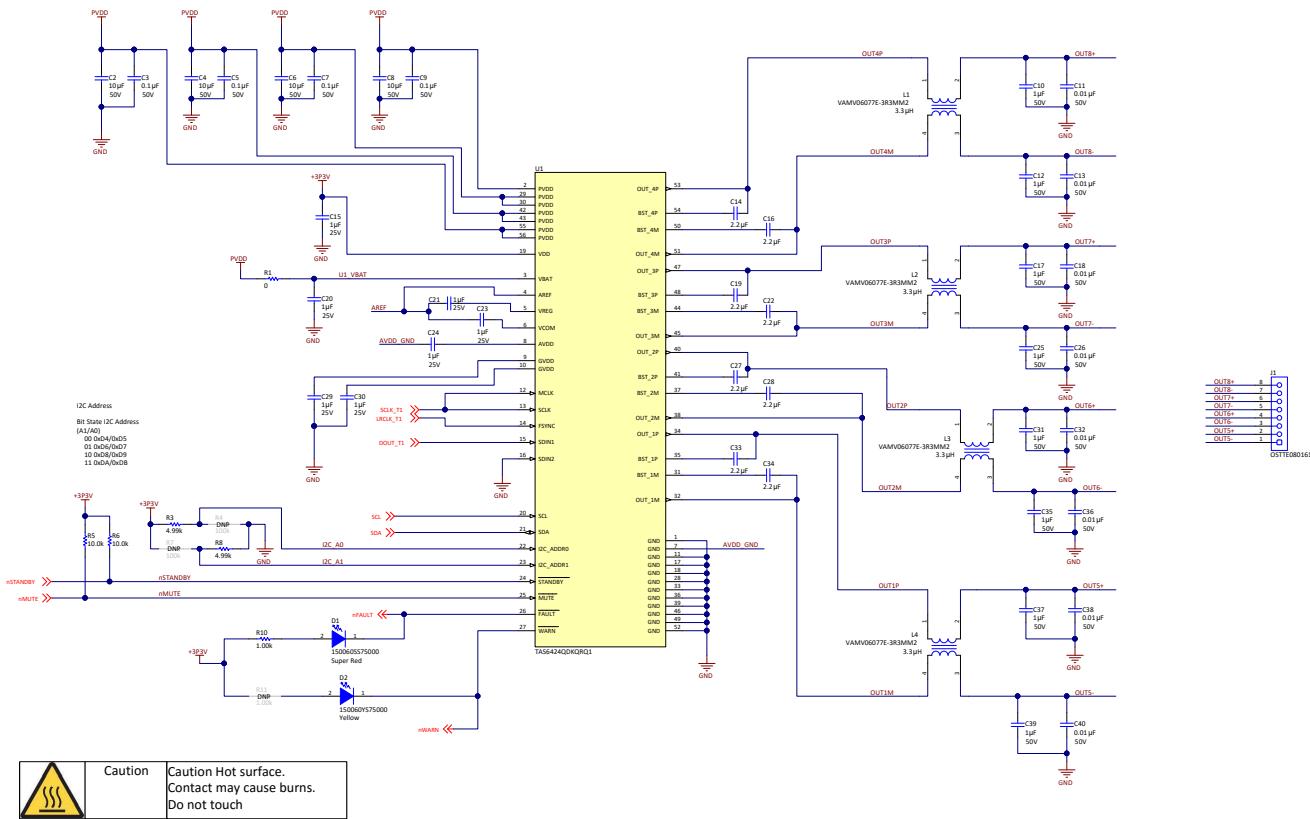
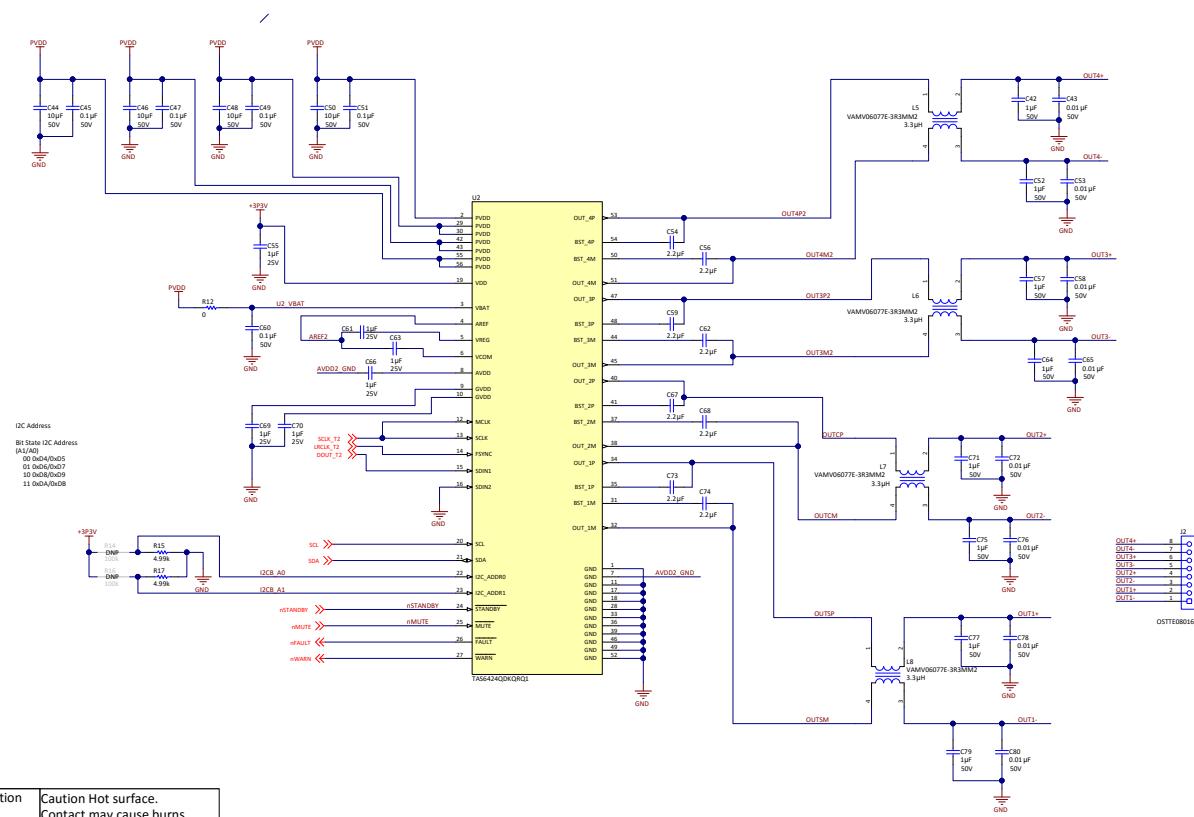


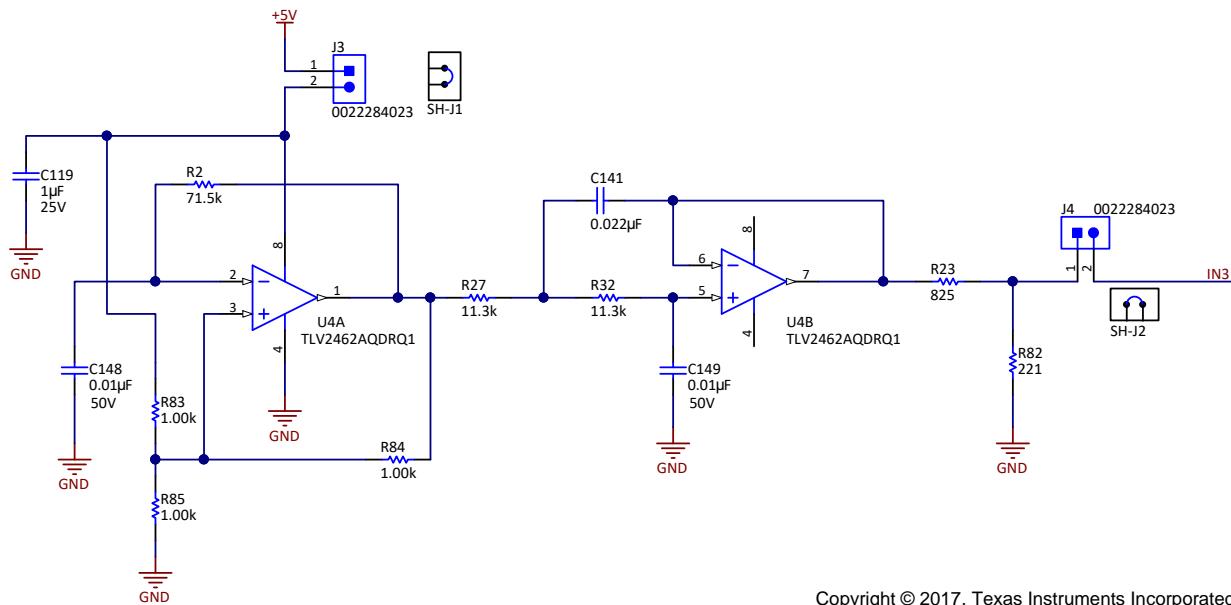
Figure 19. TAS6424-Q1 Class-D Power Audio Amplifier Circuits (Part 1 of 2)


Figure 20. TAS6424-Q1 Class-D Power Audio Amplifier Circuits (Part 2 of 2)

2.4.1.6 Support Circuits

2.4.1.6.1 TLV2462A-Q1 Oscillator Circuit

To run EMI tests, the ideal setup is to have a signal source on the board with the rest of the circuits. A TLV2462-Q1 dual operational amplifier (op amp) is used to provide this function (see Figure 21). One op amp, U4A, is configured as a 1-kHz square-wave oscillator. U4B provides a low-pass filter with a cutoff frequency of approximately 1.4 kHz so that the output approximates a sine wave. J3 connects the op amp to +5-V power, while J4 connects the output to the inputs of the PCM1865-Q1 devices. R23 and R25 are selected to drive the TAS6424-Q1 outputs to 1 W when a 2- Ω load has been connected.

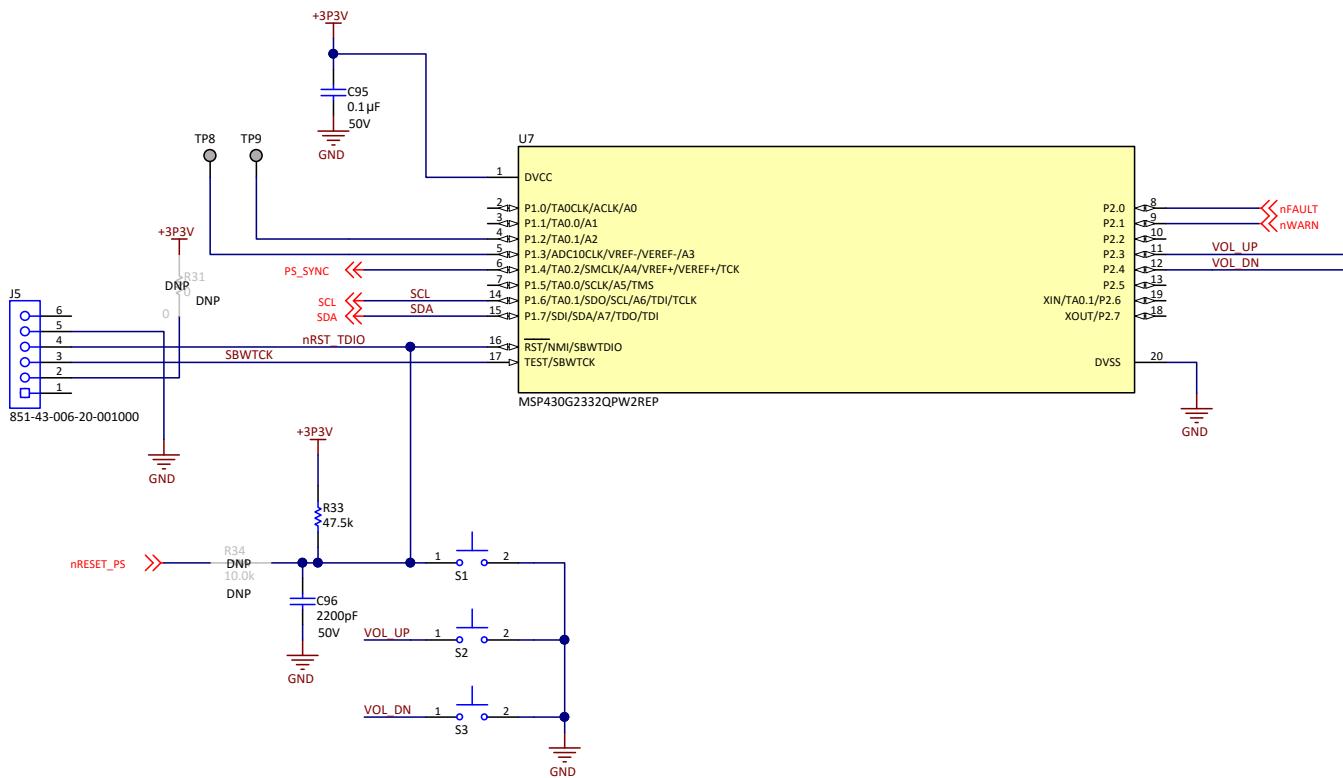


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Figure 21. TLV2462-Q1 Oscillator Circuit

2.4.1.6.2 MSP430G2332-EP

Creating a stand-alone design requires a host processor to configure the PCM1865-Q1 and TAS6424-Q1 devices at power up. The MSP430G2332-EP has been chosen because this board design is intended for an extended temperature range. The I²C interface that connects to the PCM1865-Q1 and the TAS6424-Q1 devices is the primary interface from the MSP430 to the other components on the board (see Figure 22). J5 is the programming interface for the MSP430. R33 and C96 provide a delayed power-up reset function. Switch S1 allows the user to reset the MSP430 without cycling power to the board. The signals nWARN1 and nFAULT1 are routed from the TAS6424-Q1 to the MSP430, but there is no provision in the software to act upon faults or warnings. Switches S2 and S3 are provided for volume up and volume down functions, though this has not been implemented. Pin 6 is an I/O that is routed to the LM53635L-Q1 to provide an optional 2-MHz synchronization signal. The synchronization function is not implemented in this reference design.



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Figure 22. TIDA-00733 Microcontroller

2.4.2 Software

The MSP430 used in the TIDA-00733 circuit board is required to configure the PCM1865-Q1 and TAS6424-Q1 devices at power up. The program to accomplish this configuration is listed in the following configuration code. The configuration program for TIDA-00733 is developed using the Code Composer Studio™ (CCS) integrated development environment (IDE). Some of the software directives in the program are specific to CCS. The software is based on the software in [TIDA-00743](#) and is very similar in operation.

TIDA-00733 configuration code:

```
#include <msp430.h>
#include "USI_I2C.h"

//#define number_of_bytes 5 // How many bytes? MSK: This needs to go

//void Master_Transmit(void);
//void Master_Transmit(char i2cAddress, unsigned char registerAddress, unsigned char writeValue);
//void Master_Recieve(void);

//void Setup_USI_Master_TX(void); //will need to pass parameter to tell what the
master clock is so that the I2C clock sets up correctly
//void Setup_USI_Master_RX(void); // - in both cases

unsigned char SLV_Test_Addr = 0x48;
unsigned char PCM1_Addr = 0x4a; //PCM1865 Address - // 0x4A
unsigned char PCM2_Addr = 0x4b; //PCM1865 Address - // 0x4B
unsigned char TAS1_Addr = 0x6a; //TAS6424 Address // 0x6A
unsigned char TAS2_Addr = 0x6b; //TAS6424 Address // 0x6B
unsigned char Test_Reg = 0x10;
unsigned char Test_Data = 0x2d;
unsigned char Low_Vol = 0x0f;
unsigned char EM_Vol = 0xd1;
unsigned char Ful_Vol = 0xd5;
unsigned char Volume = 0x0f;

//int I2C_State, Bytecount, Transmit = 0; // State variable
//void Data_TX (void);
//void Data_RX (void);
int main(void)
{
    volatile unsigned int i; // Use volatile to prevent removal

    WDTCTL = WDTPW + WDTHOLD; // Stop watchdog
    if (CALBC1_1MHZ==0xFF) // If calibration constant erased
    {
        while(1); // do not load, trap CPU!!
    }
    DCOCTL = 0; // Select lowest DCOx and MODx settings
    BCSCTL1 = CALBC1_1MHZ; // Set DCO
    DCOCTL = CALDCO_1MHZ;

    P1OUT = 0xC0; // P1.6 & P1.7 Pullups, others to 0
    P1REN |= 0xC0; // P1.6 & P1.7 Pullups
    P1DIR = 0xFF; // Unused pins as outputs
    P2OUT = 0x00; //Make Sure FS = P2.2 is LOW so that CDCS503
multiplies by 1
    P2DIR = 0xFE;

    __delay_cycles(10000);

    Set_I2C();
    __delay_cycles(10000);

//PCM1865 Master Section
    I2C_Write (I2C_BYTE, PCM1_Addr, 0x20, 0x91); // Set as timing master on PCM1865
    I2C_Write (I2C_BYTE, PCM1_Addr, 0x26, 0x00); //Set BCLK Divider from SCK to 1 on PCM1865 -
96 kHz for LR CLK
    I2C_Write (I2C_BYTE, PCM1_Addr, 0x27, 0xff); //Sets BCK to LRCLK ratio to 256
    I2C_Write (I2C_BYTE, PCM1_Addr, 0x0b, 0x03); //set for TDM mode with 32 bit data slots
    I2C_Write (I2C_BYTE, PCM1_Addr, 0x0c, 0x01); //Set for 4 channel TDM
    I2C_Write (I2C_BYTE, PCM1_Addr, 0x0d, 0x01); //Data offset from LRCLK rising edge. Set to 0x81
for the second four words 0x01 for the first four
```

```

/* PCM1865 Slave Section - See if this changes input issue
 * should not need to set up master clock derivation
 * If needed, must set both register 0x20 and 0x28 bit 1
 */

I2C_Write (I2C_BYTE, PCM2_Addr, 0x0b, 0x03); //set for TDM mode with 32 bit data slots
I2C_Write (I2C_BYTE, PCM2_Addr, 0x0c, 0x01); //Set for 4 channel TDM
I2C_Write (I2C_BYTE, PCM2_Addr, 0x0d, 0x81); //Data offset from LRCLK rising edge. Set to
0x81 for the second 4 words

//TAS6424 section
I2C_Write (I2C_BYTE, TAS1_Addr, 0x00, 0x80); //Master Reset TAS6424 1.
I2C_Write (I2C_BYTE, TAS2_Addr, 0x00, 0x80); //Master Reset TAS6424 2.

I2C_Write (I2C_BYTE, TAS1_Addr, 0x04, 0x55); // Mute outputs on TAS6424 1
I2C_Write (I2C_BYTE, TAS2_Addr, 0x04, 0x55); // Mute outputs on TAS6424 2
I2C_Write (I2C_BYTE, TAS1_Addr, 0x00, 0x80); //Master Reset TAS6424 1.
I2C_Write (I2C_BYTE, TAS2_Addr, 0x00, 0x80); //Master Reset TAS6424 2.
I2C_Write (I2C_BYTE, TAS1_Addr, 0x21, 0x80); //Clear Clock Fault TAS6424 1
I2C_Write (I2C_BYTE, TAS2_Addr, 0x21, 0x80); //Clear Clock Fault TAS6424 2

I2C_Write (I2C_BYTE, TAS1_Addr, 0x01, 0x31); // Set Gain to Level 2 (15V) on TAS6424 1
I2C_Write (I2C_BYTE, TAS2_Addr, 0x01, 0x31); // Set Gain to Level 2 (15V) on TAS6424 2

I2C_Write (I2C_BYTE, TAS1_Addr, 0x02, 0x62); // Set PWM for 44x FS on TAS6424 1
I2C_Write (I2C_BYTE, TAS2_Addr, 0x02, 0x62); // Set PWM for 44x FS on TAS6424 2

I2C_Write (I2C_BYTE, TAS1_Addr, 0x03, 0x86); // Set Sampling Rate to 96 kHz, 1st 4 TDM slots on
TAS6424 1
I2C_Write (I2C_BYTE, TAS2_Addr, 0x03, 0xA6); // Set Sampling Rate to 96 kHz, last 4 TDM slots
on TAS6424 2
__delay_cycles(1000000);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x05, Low_Vol); // Turn down Channel 1 on TAS6424 1
I2C_Write (I2C_BYTE, TAS1_Addr, 0x06, Low_Vol); // Turn down Channel 2 on TAS6424 1
I2C_Write (I2C_BYTE, TAS1_Addr, 0x07, Low_Vol); // Turn down Channel 3 on TAS6424 1
I2C_Write (I2C_BYTE, TAS1_Addr, 0x08, Low_Vol); // Turn down Channel 4 on TAS6424 1
I2C_Write (I2C_BYTE, TAS2_Addr, 0x05, Low_Vol); // Turn down Channel 1 on TAS6424 2
I2C_Write (I2C_BYTE, TAS2_Addr, 0x06, Low_Vol); // Turn down Channel 2 on TAS6424 2
I2C_Write (I2C_BYTE, TAS2_Addr, 0x07, Low_Vol); // Turn down Channel 3 on TAS6424 2
I2C_Write (I2C_BYTE, TAS2_Addr, 0x08, Low_Vol); // Turn down Channel 4 on TAS6424 2

Volume = EM_Vol;

I2C_Write (I2C_BYTE, TAS1_Addr, 0x04, 0x00); // Un-mute outputs on TAS6424 1
I2C_Write (I2C_BYTE, TAS2_Addr, 0x04, 0x00); // Un-mute outputs on TAS6424 2

I2C_Write (I2C_BYTE, TAS1_Addr, 0x05, Volume); // Turn up Channel 1 on TAS6424 1
I2C_Write (I2C_BYTE, TAS1_Addr, 0x06, Volume); // Turn up Channel 2 on TAS6424 1
I2C_Write (I2C_BYTE, TAS1_Addr, 0x07, Volume); // Turn up Channel 3 on TAS6424 1
I2C_Write (I2C_BYTE, TAS1_Addr, 0x08, Volume); // Turn up Channel 4 on TAS6424 1
I2C_Write (I2C_BYTE, TAS2_Addr, 0x05, Volume); // Turn up Channel 1 on TAS6424 2
I2C_Write (I2C_BYTE, TAS2_Addr, 0x06, Volume); // Turn up Channel 2 on TAS6424 2
I2C_Write (I2C_BYTE, TAS2_Addr, 0x07, Volume); // Turn up Channel 3 on TAS6424 2
I2C_Write (I2C_BYTE, TAS2_Addr, 0x08, Volume); // Turn up Channel 4 on TAS6424 2

// }

LPM0;
}

```

The include file, *msp430.h*, is part of the MSP430Ware™ software library provided by Texas Instruments as an add-on to CCS. The include file *USI_I2C.h* defines the I²C commands used by the universal serial interface (USI) block in the MSP430G2332. Next, variables are declared to represent the I²C addresses of the TAS6424-Q1 and the PCM1865-Q1 and various gain settings used in the program.

The main function starts after the declarations. The first commands are a test to ensure that the calibration for the MSP430 internal clock is valid. If the clock calibration is valid, the clock and the GPIO for banks 1 and 2 are set up. This step is followed by a delay to ensure that the GPIO outputs are settled. The I²C section is then set up.

The next section contains commands to configure the PCM1865-Q1 devices. The first command sets U9 (PCM1) as the timing master:

```
I2C_Write (I2C_BYTE, PCM1_Addr, 0x20, 0x91);
```

The next command sets the master clock-to-BCLK divide ratio. The command shown sets the BCLK to the same value as the 24.576-MHz timing crystal. Note that BCLK, or bit clock, is the signal SCLK in the previous schematic images.

```
I2C_Write (I2C_BYTE, PCM1_Addr, 0x26, 0x00);
```

Following this, the BCLK to LRCLK ratio is set to 256:

```
I2C_Write (I2C_BYTE, PCM1_Addr, 0x27, 0xff);
```

After the clocks have been set up, TDM mode is configured:

```
I2C_Write (I2C_BYTE, PCM1_Addr, 0x0b, 0x03);
I2C_Write (I2C_BYTE, PCM1_Addr, 0x0c, 0x01);
I2C_Write (I2C_BYTE, PCM1_Addr, 0x0d, 0x01);
```

The write to address 0x0b sets the PCM1865-Q1 up for TDM mode with 32-bit time slots. The write to register 0x0c sets the part for four-channel TDM and the write to 0x0d sets the data for a one-bit offset from the rising edge of the LRCLK. This concludes the setup of the master PCM1865-Q1. The rest of the registers are allowed to keep their default settings.

Next, the slave PCM1865-Q1 is configured:

```
I2C_Write (I2C_BYTE, PCM2_Addr, 0x0b, 0x03);
I2C_Write (I2C_BYTE, PCM2_Addr, 0x0c, 0x01);
I2C_Write (I2C_BYTE, PCM2_Addr, 0x0d, 0x81)
```

These commands are the same as the TDM configuration commands for the master PCM1865-Q1 except that the data is set for a 129-bit delay from LRCLK. This includes one bit offset in the first four channels and 128 bits (four 32-bit words) of data delay until the master PCM1865-Q1 is done sending data. The data from U8 is then delivered in the data slots 5 through 8. The rest of the registers are allowed to keep their default settings. At this point, the audio data timing is present and analog signals at the inputs are being converted to digital data.

The TAS6424-Q1 configuration setting is more complicated:

```
I2C_Write (I2C_BYTE, TAS1_Addr, 0x00, 0x80);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x00, 0x80);
```

```
I2C_Write (I2C_BYTE, TAS1_Addr, 0x04, 0x55);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x04, 0x55);
```

```
I2C_Write (I2C_BYTE, TAS1_Addr, 0x21, 0x80);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x21, 0x80);
```

```
I2C_Write (I2C_BYTE, TAS1_Addr, 0x01, 0x31);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x01, 0x31);
```

All of the commands for the TAS6424-Q1 devices are first sent to TAS1 (U2) then to TAS2 (U1). The first two commands in the TAS6424-Q1 configuration is a master reset for the TAS6424-Q1 devices. This command restarts the part. This command ensures the parts are in their default power-up state. The next commands ensure the outputs are muted so that nothing can be heard during configuration. The third pair of commands clears the clock fault register. At power up, a clock fault is registered because there is no clock input to the device until the PCM1865-Q1 master device has been configured. After the PCM1865-Q1 device has been configured, the TAS6424-Q1 operates correctly, but the fault register must be cleared by the host processor. The last two commands set the gain to be appropriate for a 15-V PVDD power rail. This setting ensures that the output reaches its maximum at 15 V. This setting is appropriate for the 14.4-V test level that is used to test the TIDA-00733 design. Register 0x01 also controls other functions: high-pass filter enable, global overtemperature warning control set point, overcurrent level set point, and volume rate. These other functions are maintained at their default values.

The next commands configure the clocking for the TAS6424-Q1:

```
I2C_Write (I2C_BYTE, TAS1_Addr, 0x02, 0x62);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x02, 0x62);
```

The first clock configuration command sets the PWM frequency to 44 times f_s , where frame sync f_s is the frequency of the LRCLK. The *Output Switch Frequency Option* table in [TAS6424-Q1 75-W, 2-MHz Digital Input 4-Channel Automotive Class-D Audio Amplifier With Load-Dump Protection and I^C Diagnostics](#) shows that the PWM settings for either a 48-kHz sample rate or a 96-kHz sample rate results in a PWM frequency of 2.11 MHz when bits 6 through 4 of register 0x02 are set to 110, or 6_h. The other functions in register 0x02 are set for their defaults.

```
I2C_Write (I2C_BYTE, TAS1_Addr, 0x03, 0x86);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x03, 0xA6);
__delay_cycles(100000);
```

The second clock configuration command sets the TAS6424-Q1 sampling rate to 96 kHz. This command also sets each TAS6424-Q1 for the TDM time slot from which to retrieve data. TAS1 retrieves data from the first four TDM time slots and TAS2 retrieves data from the second four TDM time slots.

At this point, the TAS6424-Q1 devices are operating correctly and user must turn up the volume. The gain setting has no effect because the outputs are muted. Before setting the TAS6424-Q1 for a normal output volume, set the four channel gains for a very low value. Each channel has its own register for setting gain, so four register writes are made to each TAS6426 to set all channels for the same gain:

```
I2C_Write (I2C_BYTE, TAS1_Addr, 0x05, Low_Vol);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x06, Low_Vol);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x07, Low_Vol);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x08, Low_Vol);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x05, Low_Vol);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x06, Low_Vol);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x07, Low_Vol);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x08, Low_Vol);

Volume = EM_Vol;

I2C_Write (I2C_BYTE, TAS1_Addr, 0x04, 0x00);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x04, 0x00);

I2C_Write (I2C_BYTE, TAS1_Addr, 0x05, Volume);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x06, Volume);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x07, Volume);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x08, Volume);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x05, Volume);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x06, Volume);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x07, Volume);
I2C_Write (I2C_BYTE, TAS2_Addr, 0x08, Volume);
```

The parameters "Low_Vol" and "EM_Vol" are set in the declarations at the beginning of the program. Low_Vol = 0x0f and EM_Vol = 0xd1. The setting 0x0f corresponds to an output gain of -96 dB. A delay of one second is included to ensure that there is no audible pop on the outputs. The outputs are then unmuted and set for a gain of 0xd1, or +1 dB. This value is chosen to drive the audio output to reach 10% THD + N, when PVDD is 14.4 V and the load is 2 Ω.

A final command, LPM0, sets the MSP430 MCU into a low-power standby state.

3 System Setup and Test

3.1 Hardware Setup

WARNING



Hot surface. Contact may cause burns.
Avoid touching to minimize the risk of burns.

3.1.1 Bench Test Setup

The primary test setup is used to characterize most of the operation parameters of the TIDA-00733 design. The temperature of the TAS6424-Q1 device increases during normal operation, so the designer must provide a heat sink to ensure that the TAS6424-Q1 does not overheat before reaching full output power. [Figure 23](#) shows the TIDA-00733 board with a heat sink, power connections, and speaker output connections.



Figure 23. TIDA-00733 Board With Heat Sink

Figure 24 shows the top of the TIDA-00733 board. The +5-V supply connectors along the top edge (from left to right) are for attaching a load, two push buttons S2 and S3 (see Section 2.4.1.6.2), the indicator LEDs, and the analog audio signal input jacks.



Figure 24. Connectors for TIDA-00733 Assembly

The diagram in [Figure 25](#) shows how to make the electrical connections to the TIDA-00733 design. The power supply used must be capable of a 20-V output at 40 A if the designer wishes to drive all channels to full power. The designer must also turn off the power supply until all connections have been made. The output load resistors must be capable of dissipating the output power of the TAS6424-Q1. Use an Audio Precision SYS-2722 to supply the audio signal input and to measure power output and THD +N. The SYS-2722 outputs are connected to the inputs for the channels under test and the SYS-2722 inputs are connected to the load resistors to measure the power output and THD for the channels of interest. Use a digital multimeter (DMM) to measure the DC current and voltage at the power input.

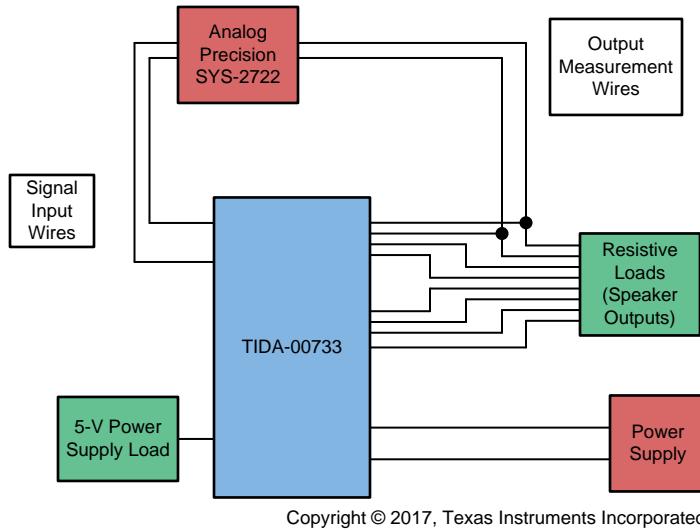


Figure 25. Test Setup Block Diagram for Power Output and THD Tests

[Figure 26](#) shows a photo of the test setup.



Figure 26. Test Setup for Power Output and Total Harmonic Distortion and Noise Tests

3.1.2 EMI Test Setup

For EMI performance testing, the TIDA-00733 design must be enclosed in a Faraday cage to ensure low emissions. [Figure 27](#) shows the TIDA-00733 design in a metal EMI enclosure. The enclosure is a Hammond model 1590J aluminum box. The box is modified with a slot to allow the board to stick out of the long sides after assembling the box. The PCB is mounted to the box lid with the TAS6424-Q1 thermal pads in contact with the lid so that the box forms a heat sink for the TAS6424-Q1 devices. The strips on both sides of the PCB have no solder mask to allow contact with the machined enclosure (see [Figure 24](#)).

For the EMI test, resistors R73 through R79 are populated with $0\text{-}\Omega$ resistors to connect all of the audio inputs together. The addition of these resistors allows driving the board with one input signal. Shunts are placed on J3 and J4 to power the 1-kHz oscillator and connect it to the audio inputs.

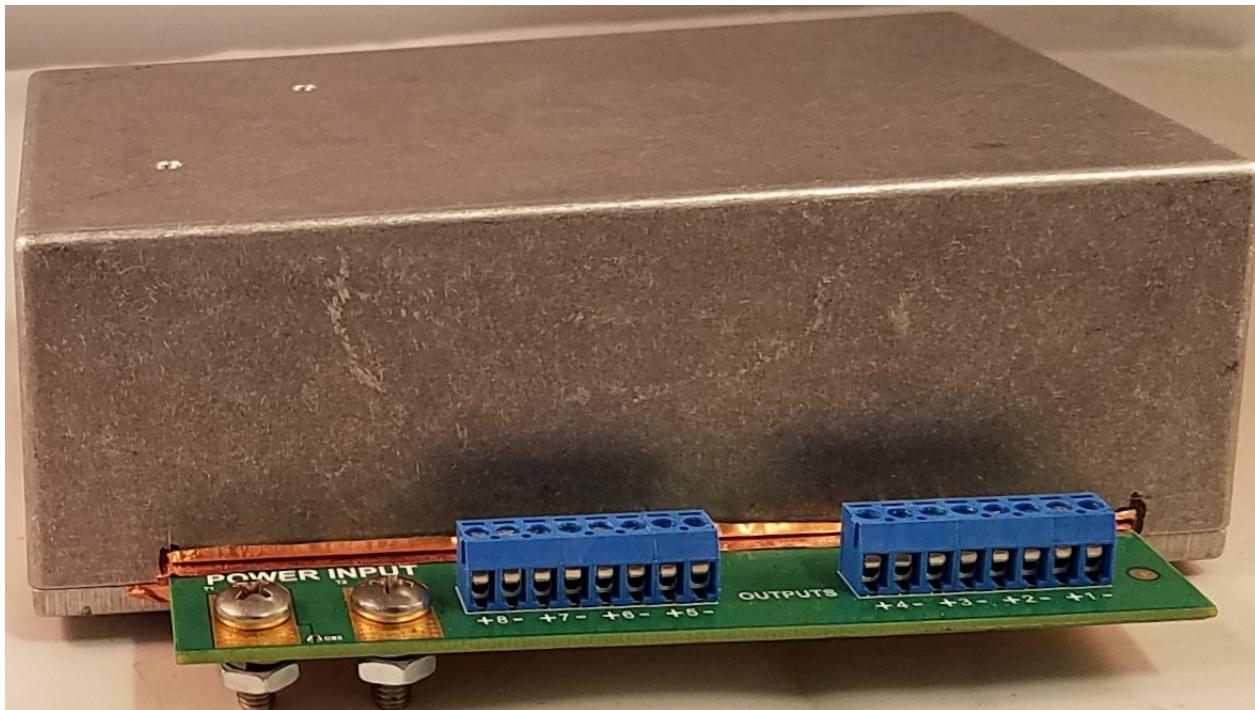
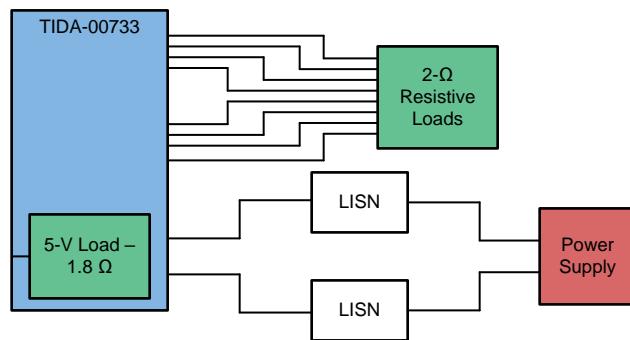


Figure 27. TIDA-00733 in Metal Box for EMI Tests

[Figure 28](#) shows the TIDA-00733 electrical connection diagram. A 12-V car battery provides the power to ensure that the emissions only originate from the unit under test (UUT) and not from noise generated by the power supply. Power is routed through two line impedance stabilization networks (LISN) in accordance with CISPR 25. Eight 2- Ω resistive loads are connected to the amplifier outputs. Connect the battery to the TIDA-00733 system after making all the other connections so that the system is not powered during test setup.



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Figure 28. Test Setup Block Diagram for EMI Tests

CISPR 25 radiated emissions tests have been performed on the TIDA-00733 reference design. For radiated emissions tests, the loads are placed near the LISNs and the UUT is placed 1.5 m from the loads. [Figure 29](#) shows an entire EMI setup for measuring radiated emissions in a test chamber. The EMI test is conducted with the UUT and its loads placed on a 50-mm thick insulator, which is in turn placed on a table with a grounded conductive surface. See the CISPR 25 specification for more setup details.



Figure 29. Radiated Emissions Test Setup

3.2 Testing and Results

3.2.1 Power Output, Total Harmonic Distortion, and Noise (THD + N)

The power output and THD + N were tested with the setup described in [Section 3.1.1](#). The input signal is set for 1 kHz during these tests. [Figure 30](#) shows a plot of the THD + N versus power output in watts with a load of $2\ \Omega$. This plot shows the average value of the curve for eight channels on one board. The power supply is set to ensure that the voltage delivered at the power input to the board is 14.4 V when the outputs are driven to 10% THD. The outputs reach 10% THD + N when supplying 45 W of power to the load. The THD+N reaches 1% when the power output is 36 W.

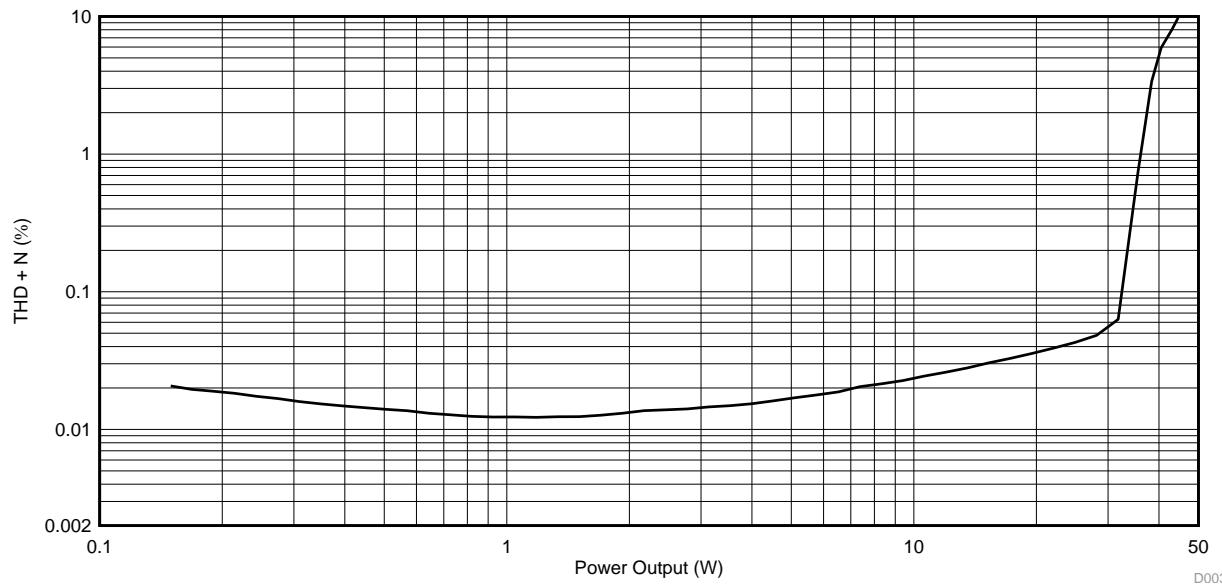


Figure 30. Power Output (W) vs THD + Noise (%) into $2\ \Omega$

[Figure 31](#) shows a plot of THD + N versus power output for $4\text{-}\Omega$ loads. Again, the plot shows the average of eight outputs driving $4\text{-}\Omega$ loads with a 14.4-V power supply and a 1-kHz input signal. The average power output is 27 W per channel. The THD+N reaches 1% when the power output is 22 W.

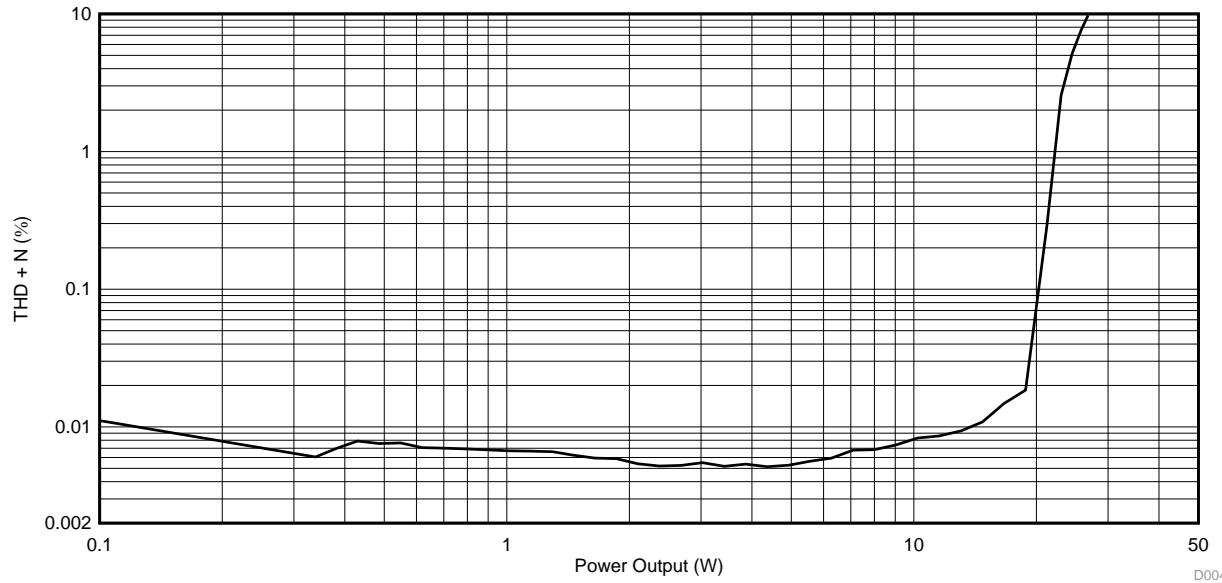


Figure 31. Power Output (W) versus THD + Noise (%) into $4\ \Omega$

3.2.2 EMI—Radiated Emissions Results

3.2.2.1 Radiated Emissions

For the radiated emission (RE) tests, set up the UUT as described in [Section 3.1.2](#). The previous [Figure 29](#) shows an example of the setup for radiated emissions testing. The limits in the graphs represent the levels for CISPR 25 Class 5.

Emissions in the range of 150 kHz to 30 MHz are measured with a monopole antenna. Only one polarization is measured for this antenna. [Figure 32](#) shows the ambient scan of the test setup with the UUT unpowered. [Figure 33](#) shows the test results.

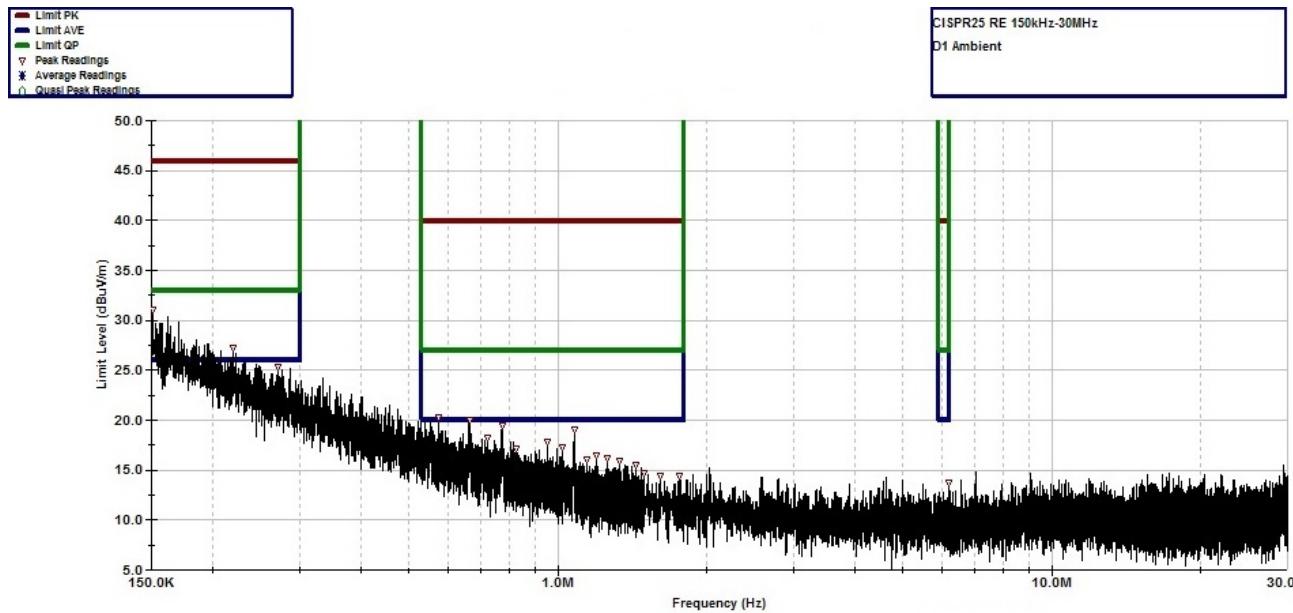


Figure 32. CISPR 25 Radiated Emissions: 150 kHz to 30 MHz, Ambient

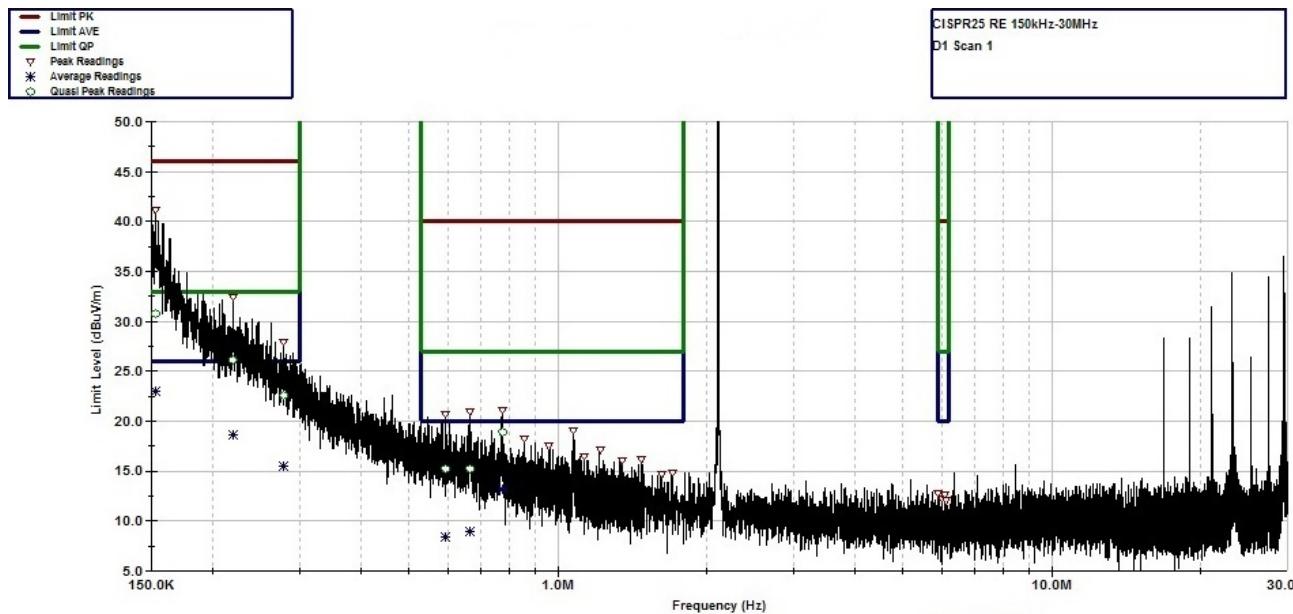


Figure 33. CISPR 25 Radiated Emissions: 150 kHz to 30 MHz

The radiated emissions average reading margin in the 150-kHz to 30-MHz range is greater than 3 dB for the whole range.

Emissions in the range of 30 MHz to 200 MHz are measured with a biconical antenna in both horizontal and vertical polarizations. [Figure 34](#) and [Figure 35](#) show the ambient scans with the UUT power OFF. [Figure 36](#) shows the results with the antenna horizontally polarized and [Figure 37](#) shows the results with the antenna vertically polarized.

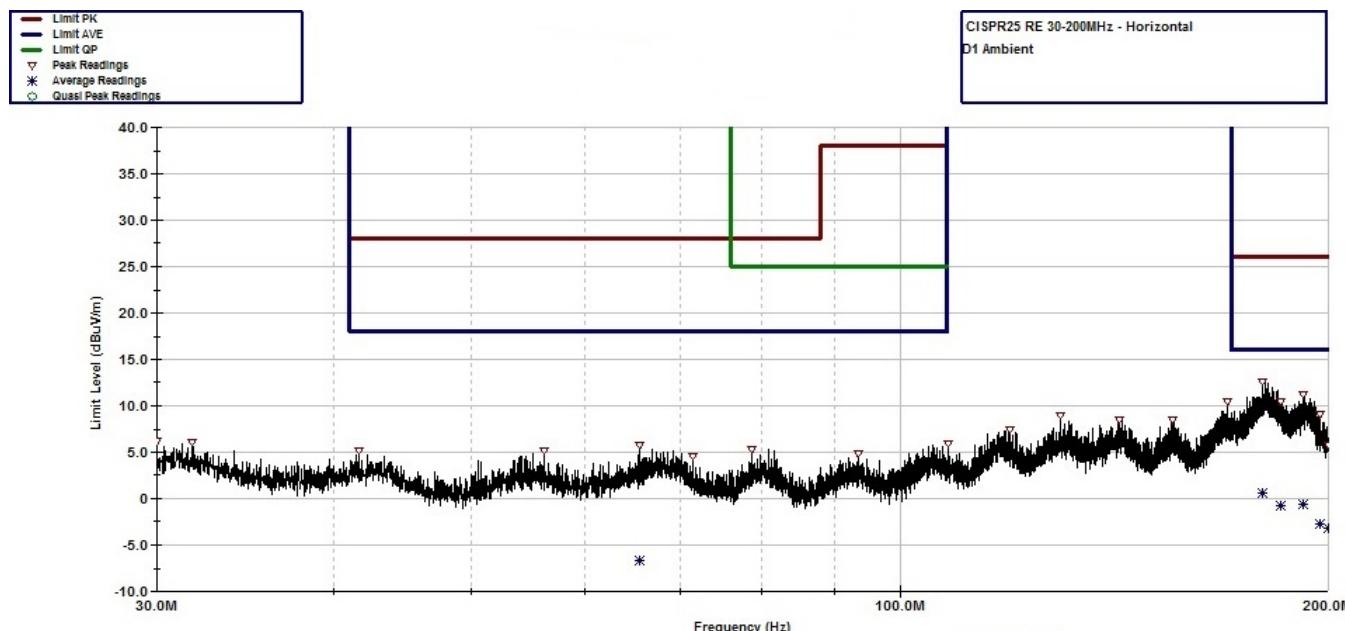


Figure 34. CISPR 25 Radiated Emissions: 30 MHz to 200 MHz, Horizontal Antenna Orientation, Ambient Scan

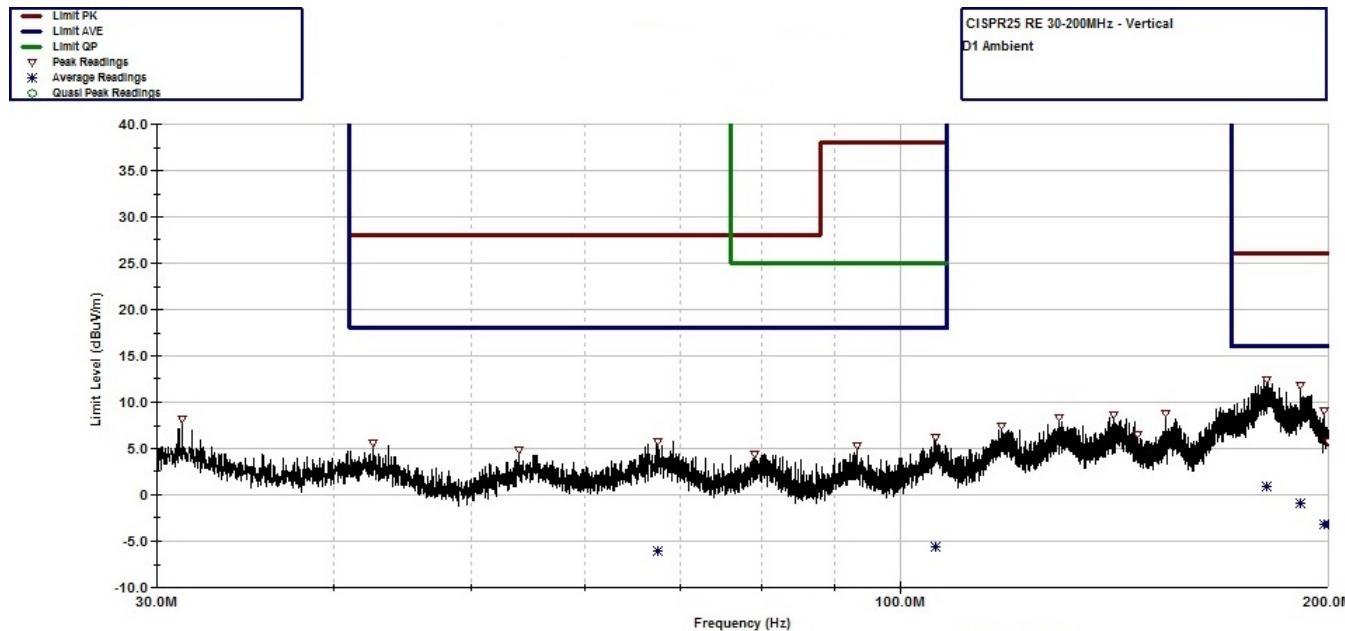


Figure 35. CISPR 25 Radiated Emissions: 30 MHz to 200 MHz, Vertical Antenna Orientation, Ambient Scan

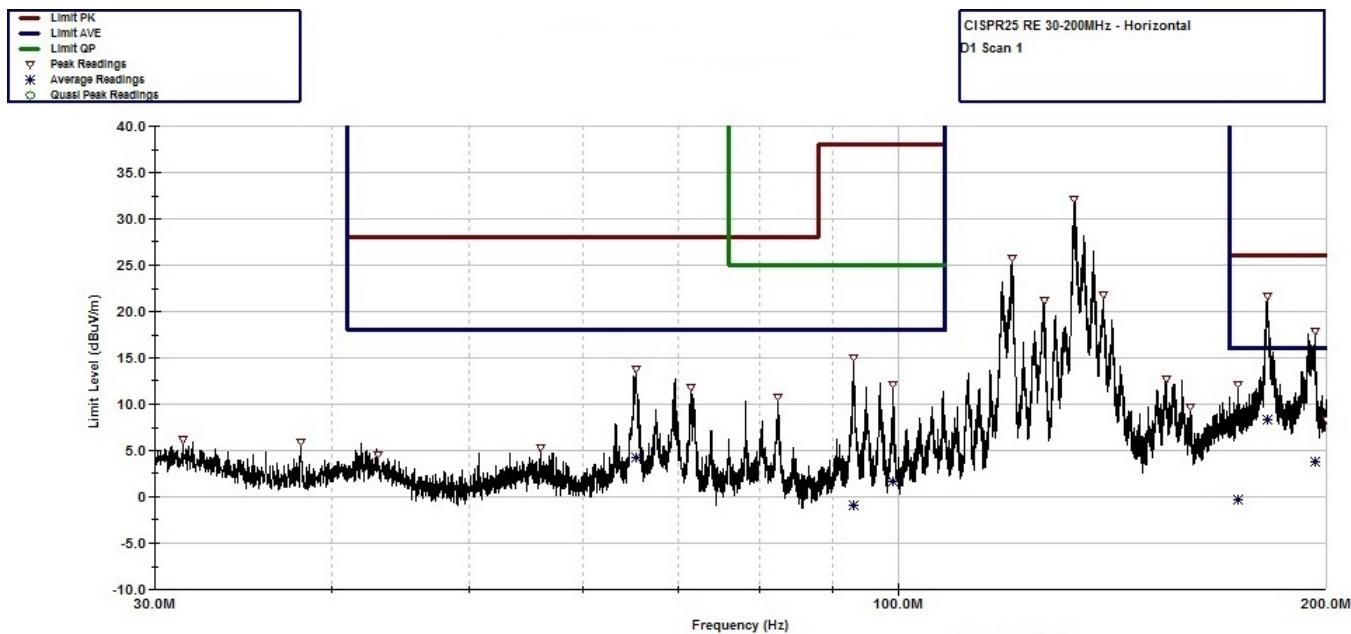


Figure 36. CISPR 25 Radiated Emissions: 30 MHz to 200 MHz, Horizontal Antenna Orientation

The radiated emissions average reading margin for the horizontal polarization test is greater than 13 dB. The peak reading margin is greater than 4 dB.

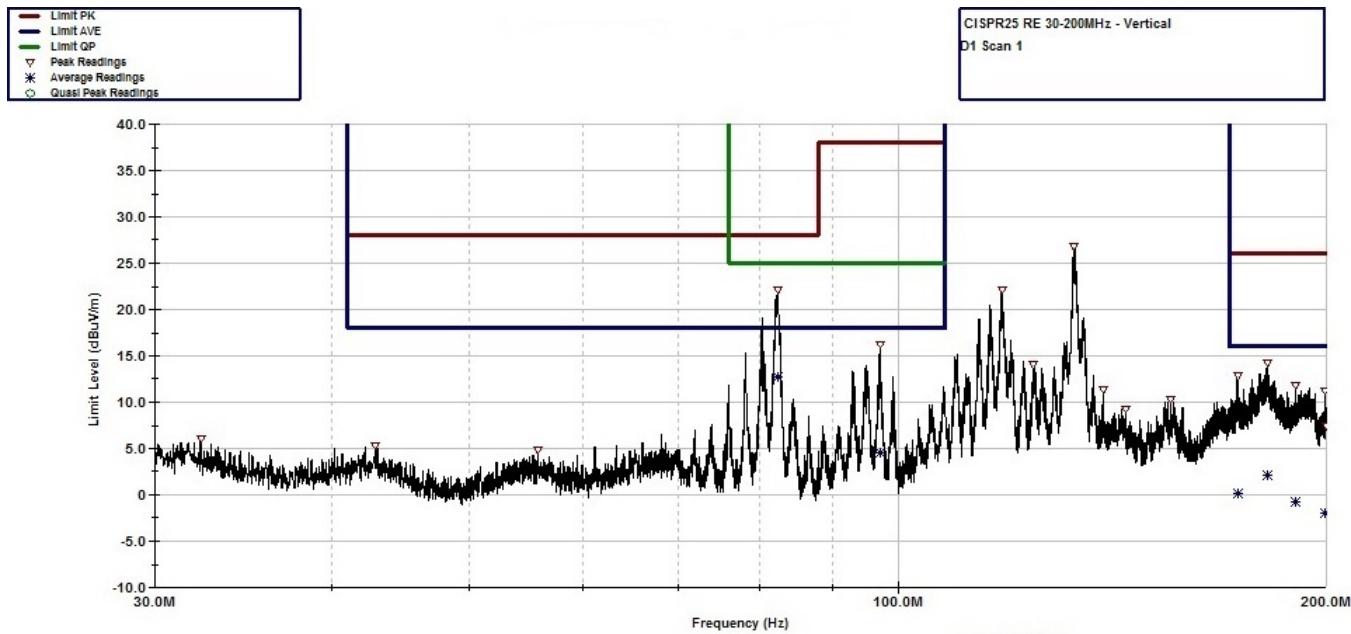


Figure 37. CISPR 25 Radiated Emissions: 30 MHz to 200 MHz, Vertical Antenna Orientation

The RE average reading margin for the vertical polarization test is greater than 5 dB. The peak reading margin is greater than 6 dB.

Emissions in the frequency range from 200 MHz to 1000 MHz are measured with a horn antenna. Both horizontal and vertical polarizations of the antenna are tested. [Figure 38](#) and [Figure 39](#) show the ambient scan when the UUT power is OFF. [Figure 40](#) and [Figure 41](#) show the actual system response.

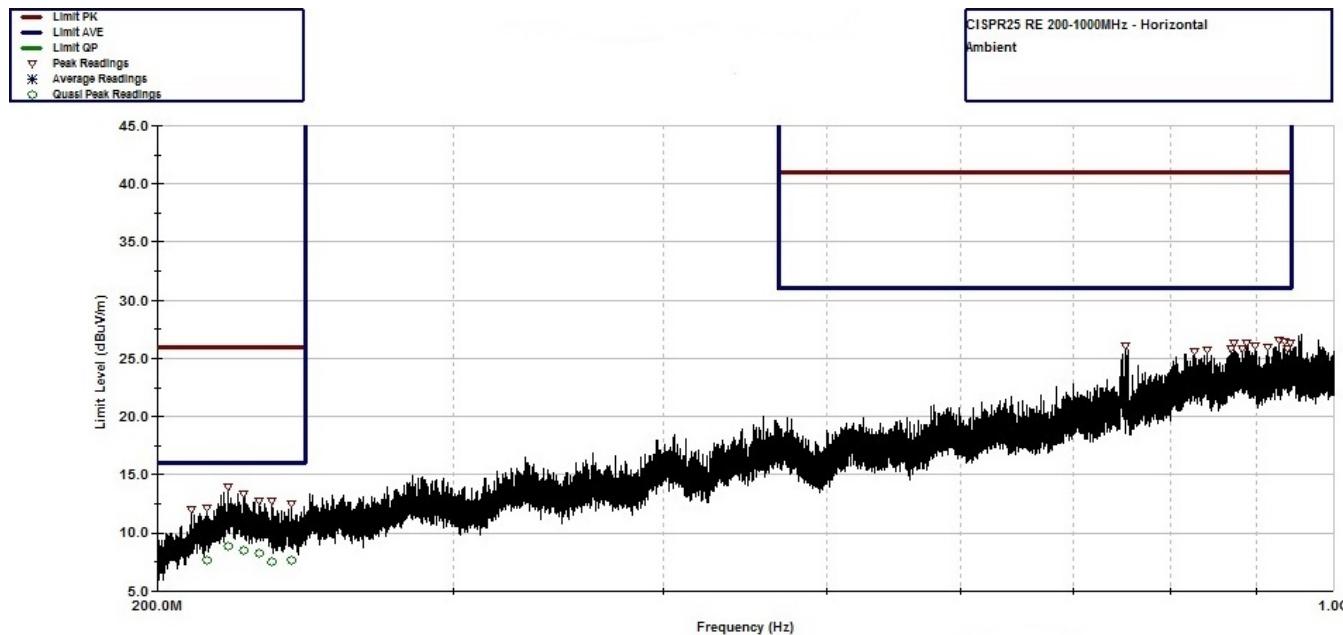


Figure 38. CISPR 25 Radiated Emissions: 200 MHz to 1 GHz, Horizontal Antenna Orientation, Ambient Scan

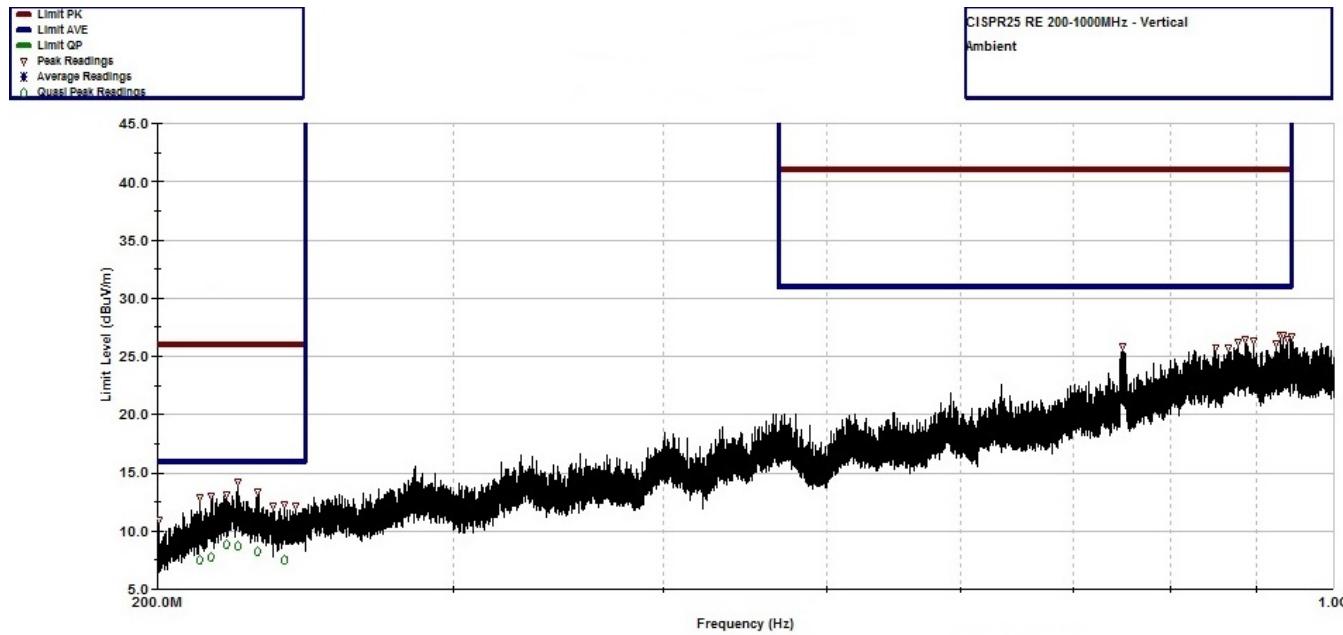


Figure 39. CISPR 25 Radiated Emissions: 200 MHz to 1 GHz, Vertical Antenna Orientation, Ambient Scan

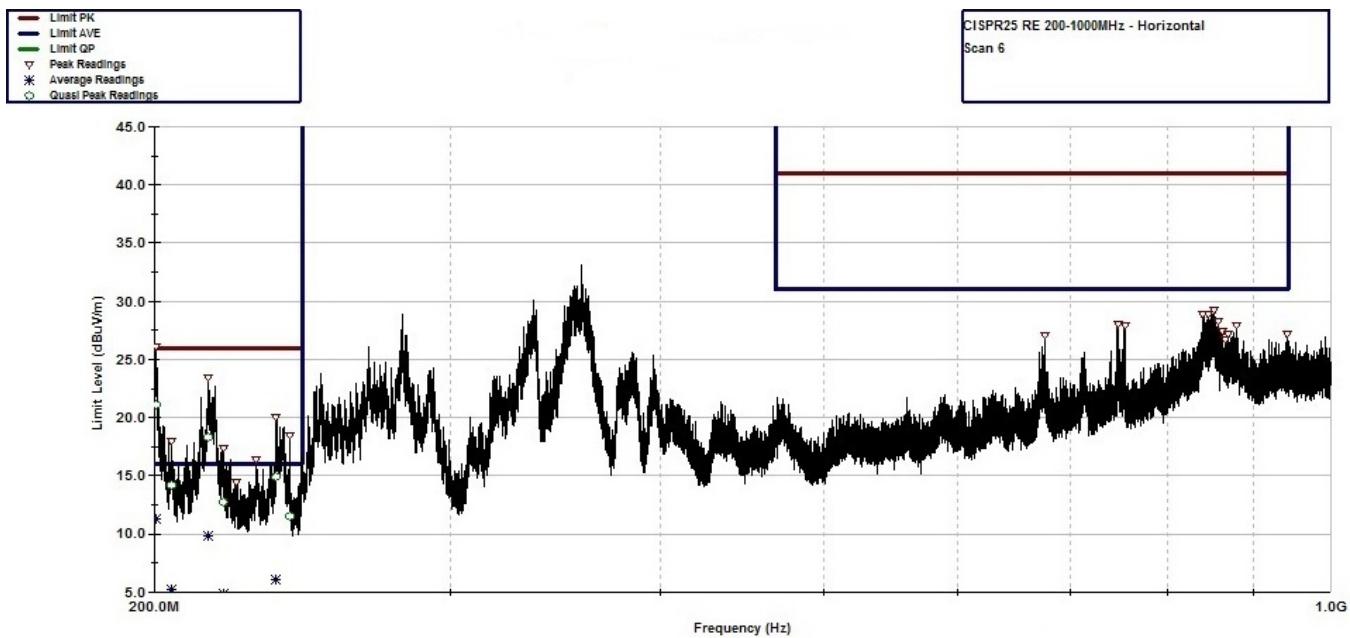


Figure 40. CISPR 25 Radiated Emissions: 200 MHz to 1 GHz, Horizontal Antenna Orientation

The RE average reading margin for the horizontal polarization test is greater than 4 dB (see [Figure 41](#)). The peak reading reaches 26 dB μ V at 200.6 MHz, which means that no margin is present at that frequency.

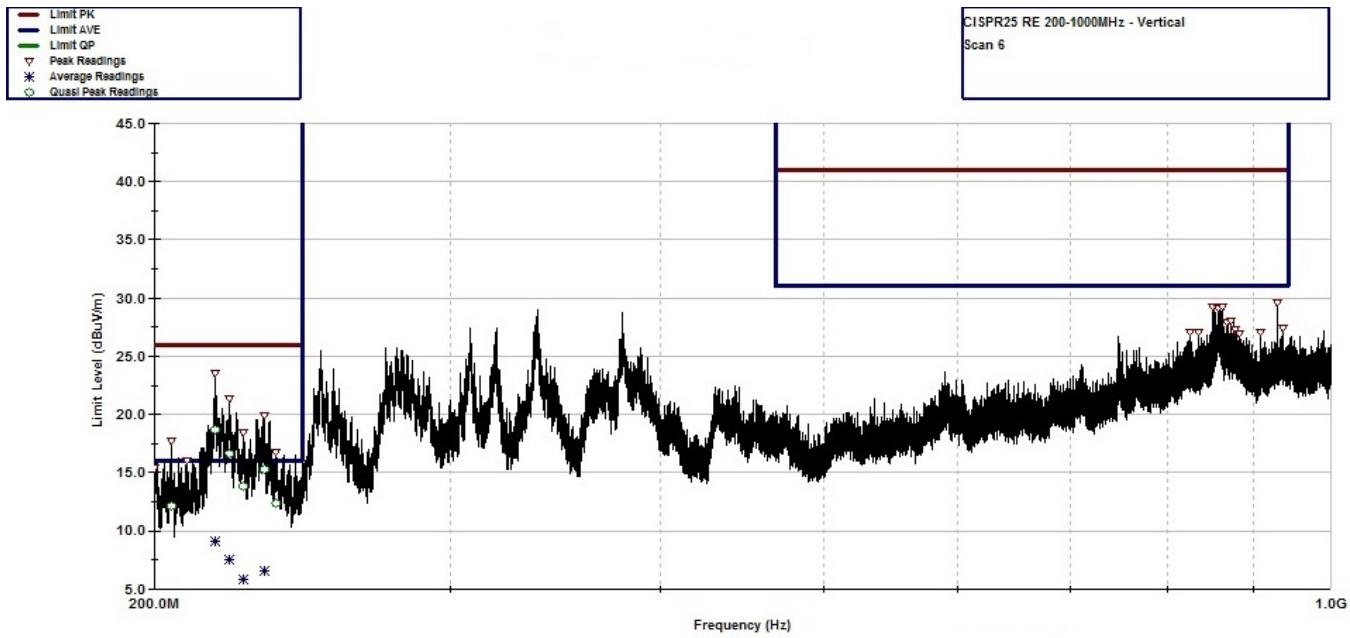


Figure 41. CISPR 25 Radiated Emissions: 200 MHz to 1 GHz, Vertical Antenna Orientation

The RE average reading margin for the vertical polarization test is greater than 6 dB. The peak reading margin is greater than 2 dB.

The results show that the TIDA-00733 reference design can meet CISPR25 Class 5 radiated emissions.

4 Further EMI Design Considerations

EMI testing of the TIDA-00733 design led to several changes. The input filter and layout were changed significantly by shortening the distance from the box edge to the inductor L18. L18 was changed to a fully-shielded device to reduce signal pickup and subsequent radiation from the power lines. The value of L18 was also lowered, which improved radiated emission readings.

Adding the small ferrites (R35, R36, R51, and R52) to the power connections on the PCM1865-Q1 devices significantly reduced radiated emissions above 40 MHz. This reduction may be due to the length of the +3P3V routing. The ferrites reduce the amplitude of the higher frequencies that the PCM1865-Q1 devices put on the +3P3V supply at the source of the noise.

Early tests led to adding C83 at power input T1; however, later testing indicated that this addition no longer improves EMI performance, so it was de-populated.

Further improvements may be possible. Adding ferrites to the +3P3V power connections for U1, U2, and especially U10, may further improve EMI performance. Increasing the value of L18 or C82 improves the low-frequency EMI performance; however, the designer must take care to avoid impacting the higher-frequency EMI performance when making changes to L18 and C82. Creating a smaller board so that the TDM traces are shorter may also improve the EMI performance.

5 Design Files

5.1 Schematics

To download the schematics, see the design files at [TIDA-00733](#).

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00733](#).

5.3 PCB Layout Recommendations

The TIDA-00733 PCB design was created to facilitate EMI testing and to reduce EMI effects. The TIDA-00733 PCB was laid out to fit into a metal box, a Hammond 1590J, which was machined to allow the ends of the board with the connectors to stick out. To fit the box well, the different groups of circuitry have been spread out more than they would be in a size-optimized system. The box is intended to make contact with the top and bottom surfaces of the PCB where the long gold strips are on each side of the board. This configuration creates a Faraday cage that encloses all of the active circuitry in the box while creating connections to the board ground.

The box lid is used as a heat sink for the TAS6424-Q1 components. The shorter support components for the TAS6424-Q1 devices are placed near the TAS6424-Q1 devices on the bottom layer, while the components taller than the TAS6424-Q1 devices are placed on the top of the board to provide clearance for the lid or other heatsink.

[Figure 42](#) shows the top layer of the PCB. Most components are on this layer. The circuits along the upper part of the PCB are the power input filter and smart diode, the LM53635L-Q1 circuit, the LP5912-Q1 circuit, and the MSP430. A connector for a +5-V load is on the right side of the board at the top. The inductors, filter capacitors, and output connectors for the TAS6424-Q1 circuits are along the left side. Power routing for the PVDD connection of the TAS6424-Q1 devices is a wide trace near the center of the board. Three mounting holes have been provided to attach the lid or other heat sink to the board. The holes are spaced to provide even thermal connections across the thermal pad on the two TAS6424-Q1 devices.

The input filter components are placed very close to the edge of the box to minimize the length of the power trace from the power connector to the filter. The LM74610 smart diode circuit is next. The output of the LM74610 connects to a large area that includes the PVDD power connection for the LM53635-Q1 and the two TAS6424-Q1 devices. The LM53635L-Q1 circuit is placed and routed to keep the current loop area small by placing the grounds of the circuit input and output capacitors close together. The routing follows the recommendations specified in the LM53635-Q1 data sheet.

The two PCM1865-Q1 ADCs are in the lower right corner of the board just inside where the metal box connects to the board. The input components are placed very tightly together with the input connectors outside the enclosure area to the right. The test oscillator circuit, the LP5907-Q1 regulator, and the SN74LVC125A-Q1 hex buffer are placed just above the PCM1865-Q1 devices. The digital output connections are kept away from the analog inputs of the ADCs.

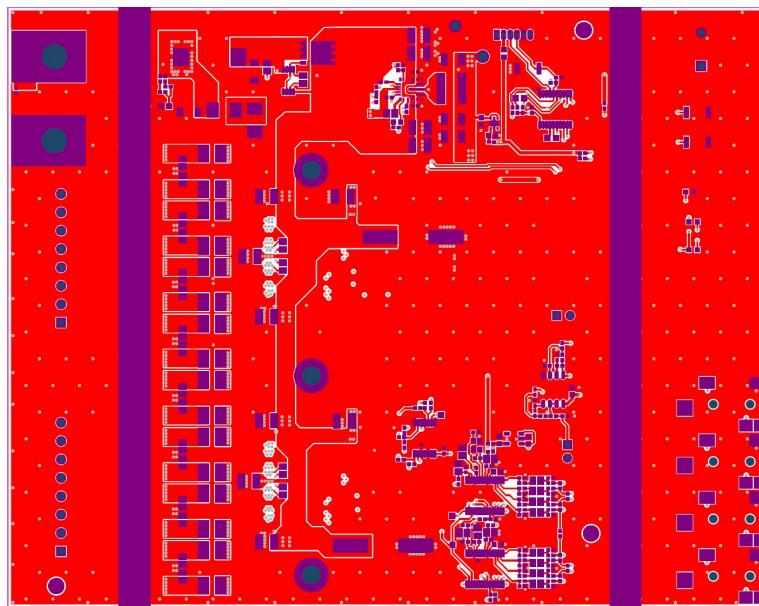


Figure 42. TIDA-00733 Top Circuit Board—Top Layer

Figure 43 shows inner layer 1, which is below the top layer in the board stackup. This layer is primarily a ground layer, though the input power connection and half of each audio output bridge are routed on this layer to eliminate the possibility of a short circuit with the enclosure. These high-current connections all have wide traces to ensure low losses in the board. Where a high current trace changes layers, multiple vias are used to reduce the impedance at the transition.

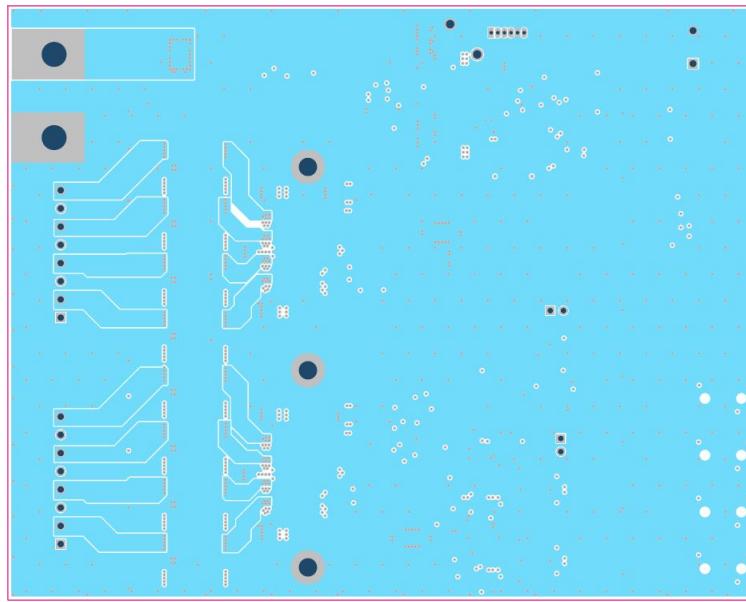


Figure 43. TIDA-00733 Circuit Board—Inner Layer 1

Figure 44 shows inner layer 2. This layer also has the input power connection and half of each audio output bridge are routed on it. This layer has the connection to the +5-V power connector and most of the signal trace routing. The unused areas are covered with more ground.

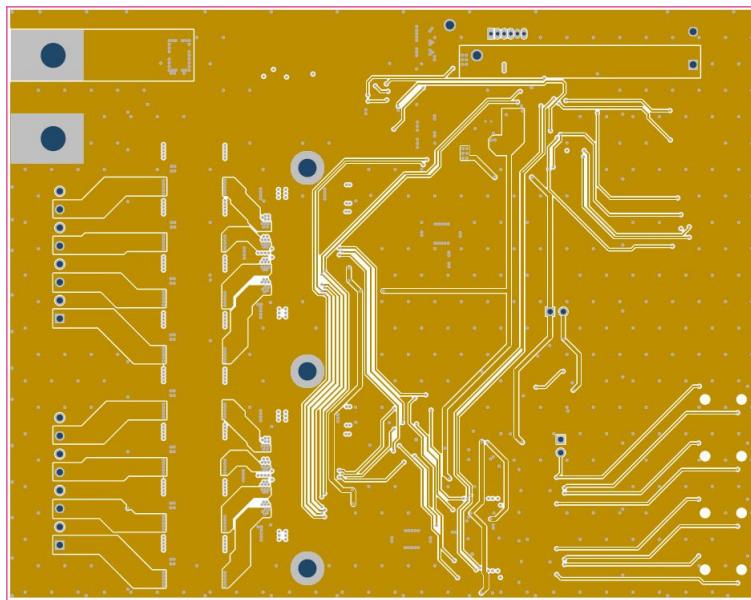


Figure 44. TIDA-00733 Circuit Board—Inner Layer 2

Figure 45 shows the bottom layer of the board. As previously stated, the two TAS6424-Q1 devices are placed on the bottom along with most of the small discrete components that form part of the circuit. The large inductors required for 2- Ω operation make the overall dimensions for each TAS6424-Q1 circuit approximately 34.6 mm \times 42.7 mm.

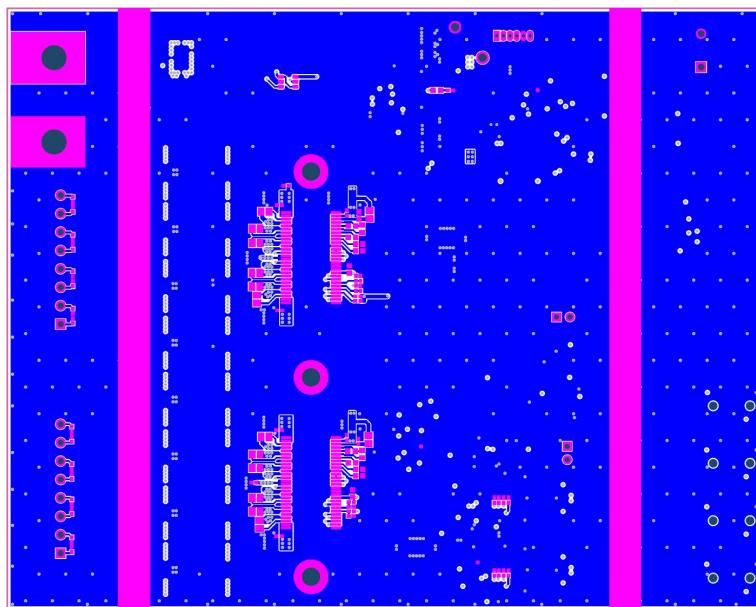


Figure 45. TIDA-00733 Bottom Circuit Board Layer

5.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-00733](#).

5.4 Altium Project

To download the Altium project files, see the design files at [TIDA-00733](#).

5.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-00733](#).

5.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-00733](#).

6 Software Files

To download the software files, see the design files at [TIDA-00733](#).

7 Related Documentation

1. Texas Instruments, [MIXED SIGNAL MICROCONTROLLER](#)
2. Texas Instruments, [TAS6424-Q1 75-W, 2-MHz Digital Input 4-Channel Automotive Class-D Audio Amplifier With Load-Dump Protection and I²C Diagnostics](#)
3. Texas Instruments, [2-MHz Automotive Class-D, 4-Channel, 21-W Audio Amplifier in Class-AB Form-Factor Reference Design](#)

7.1 Trademarks

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8 About the Author

MARK KNAPP is a Systems Architect at Texas Instruments Incorporated who specializes in automotive premium audio systems and instrument clusters. He also has an extensive background in video camera systems and infrared imaging systems for military, automotive, and industrial applications. Mark earned his BSEE at the University of Michigan-Dearborn and his MSEE at the University of Texas at Dallas.

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