General Reading

1. FPGA-based accelerator for convolution operations
   1. <https://ezproxyprod.ucs.louisiana.edu:2373/document/9172934>
   2. Convolutions require 109-1012 operations per second
   3. Maps convolution to matrix convolution for flexibility/continuity, mapping this way allows for the acceleration of the convolution to ignore system design
2. Angel-EyeAngel-Eye: A Complete Design Flow for Mapping CNN Onto Embedded FPGA
   1. <https://ezproxyprod.ucs.louisiana.edu:2373/document/7930521>
3. A FPGA-based Accelerator of Convolutional Neural Network for Face Feature Extraction
   1. <https://ezproxyprod.ucs.louisiana.edu:2373/document/8754067>

Hardware Comparison

1. A software controlled hardware acceleration architecture for image processing using an embedded development board
   1. <https://ezproxyprod.ucs.louisiana.edu:2373/document/7942352>
2. Optimizing the Convolution Operation to Accelerate Deep Neural Networks on FPGA
   1. <https://ezproxyprod.ucs.louisiana.edu:2373/document/8330049>
3. A FPGA-based Hardware Accelerator for Multiple Convolutional Neural Networks
   1. <https://ezproxyprod.ucs.louisiana.edu:2373/document/8565657>
4. A Method for Accelerating Convolutional Neural Networks Based on FPGA
   1. <https://ezproxyprod.ucs.louisiana.edu:2373/document/9151535>
5. Paper