**10/25/2020 –** Looked int AXI DMA accessing. I think this should be the method to input data to a design. Followed this guide: <http://www.fpgadeveloper.com/2014/08/using-the-axi-dma-in-vivado.html>

I was also looking into the guide provided by Kasem: <https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_2/ug1393-vitis-application-acceleration.pdf> (page 518), I believe I need to setup a PetaLinux installation.

Using this guide to setup PetaLinux, got to page 15 and having an error opening settings source <https://www.xilinx.com/support/documentation/sw_manuals/xilinx2020_1/ug1144-petalinux-tools-reference-guide.pdf>

**10/26/2020 –** Continued to look at the guide Kasem sent. Did not spend much time but got petalinux installed. Vivado would not export the xsa file so I went to sleep.

**10/28/2020 –** Found out the ubuntu installation I had was not supported for vitis/petalinux. Changed to Ubuntu 14.04.1 LTS. Installed Vitis, Vivado, PetaLinux. Started a document to cumulate reference papers on accelerated hardware designs. Finally got PetaLinux to open but when I tried to create the project I got a failure. For some reason Vitis does not want to launch due to some ecplipse error. I put a posting to the Zynq forum here <https://discuss.pynq.io/t/image-processing-acceleration/1955>