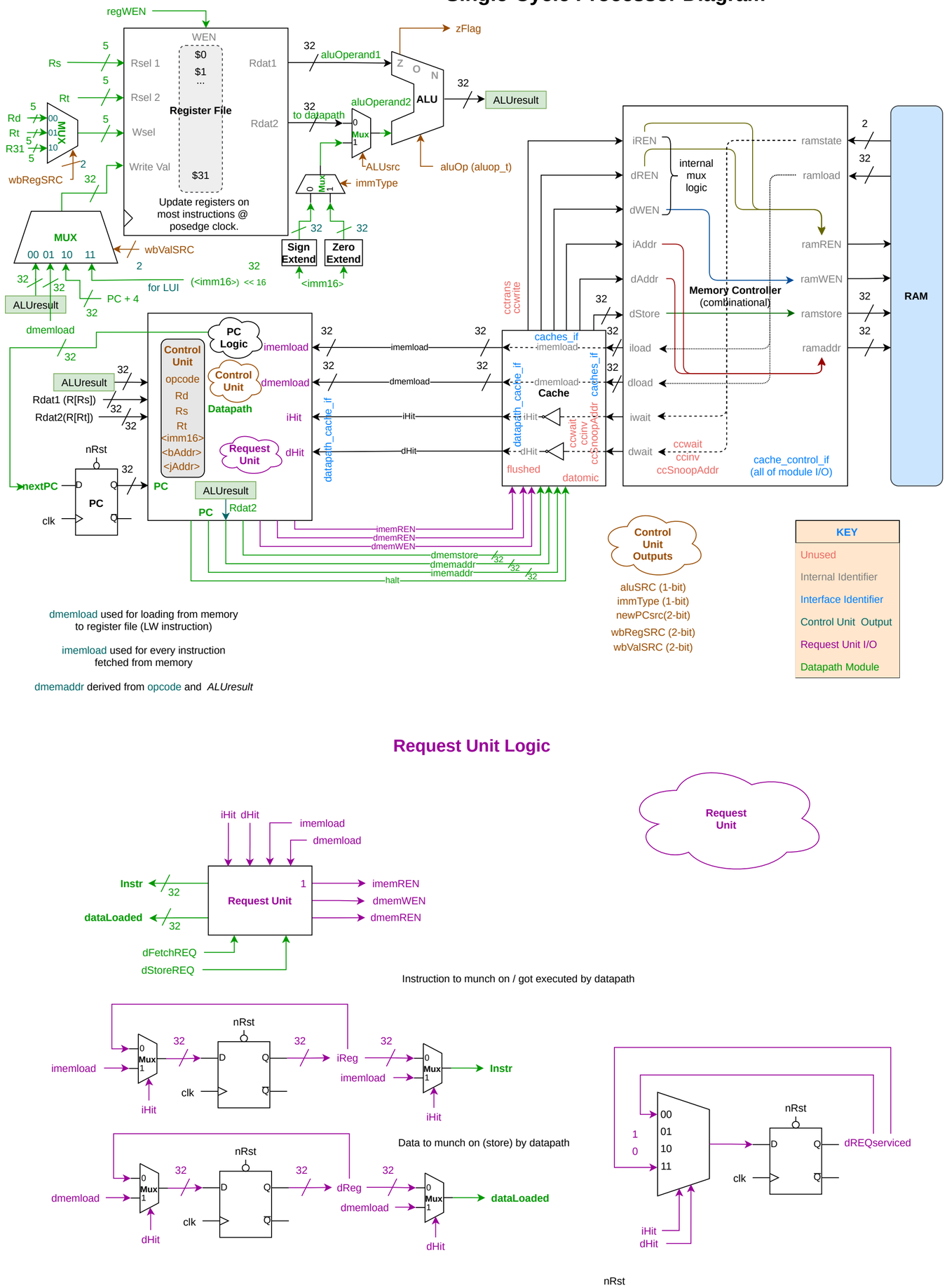
Single-Cycle Processor Diagram



dmemload used for loading from memory to register file (LW instruction)

imemload used for every instruction fetched from memory

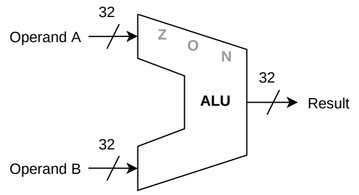
dmemaddr derived from opcode and *ALUresult*

Control Unit Outputs

aluSRC (1-bit)
immType (1-bit)
newPCsrc(2-bit)
wbRegSRC (2-bit)
wbValSRC (2-bit)

KEY
Unused
Internal Identifier
Interface Identifier
Control Unit Output
Request Unit I/O
Datapath Module

Arithmetic Logic Unit Summary



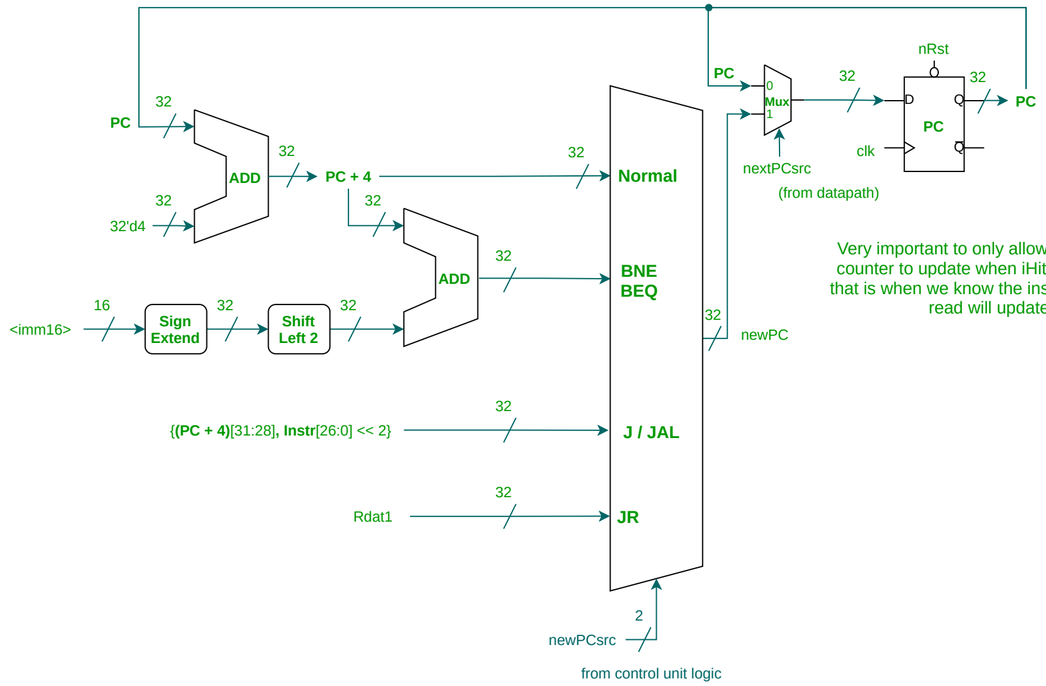
Inputs
Instruction
zFlag

Outputs
Mux: ALU Operand 2 Sel
ALU Operation (aluop_t)
Mux: Sign Extension Type Sel
Mux: newPC Line Sel
Mux: Writeback Destination Sel
Mux: Writeback Value Sel
Mux: Rs <--> Rt switch (SLL/SRL)

ALU Operations	
SLL	B << A[4:0]
SRL	B >> A[4:0]
ADD	A + B
SUB	A - B
AND	A & B
OR	A | B
XOR	A ^ B
NOR	~(A | B)
SLT	(A < B)? 1 : 0, signed
SLTU	(A < $B)? 1 : 0, unsigned

Request Unit Logic

PC Logic



Very important to only allow the program counter to update when iHit is high since that is when we know the instruction being read will update!