Grado en diseño y desarrollo de videojuegos

VJ1214 - Consolas y dispositivos

Bloque 1: Arquitectura de computadores

Puertas lógicas básicas

1. Puertas lógicas

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   – AND, OR, NOT, XOR
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5. Puertas lógicas multibit

1. Puertas lógicas

A	$\overline{A}$
0	1
1	0

$F(A) = \overline{A}$

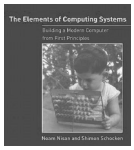
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

F(A,B) = A+B

A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

F(A,B) = AB

Libro de referencia



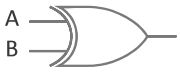
- Capítulo 1

- Capítulos 3 y 5

1. Puertas lógicas

A	B	Xor(A,B)
0	0	0
0	1	1
1	0	1
1	1	0

1. Puertas lógicas

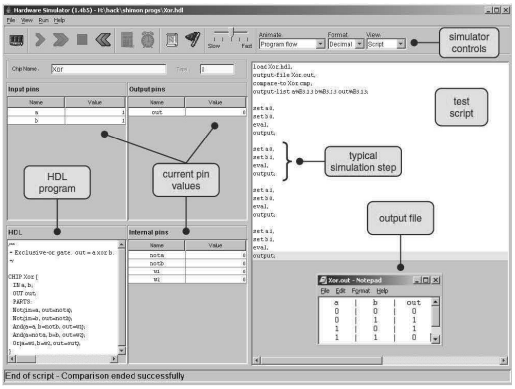


A	B	Xor(A,B)
0	0	0
0	1	1
1	0	1
1	1	0

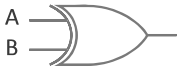
$\overline{A}B$

$A\overline{B}$

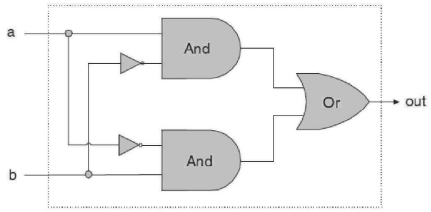
2. HDL



1. Puertas lógicas

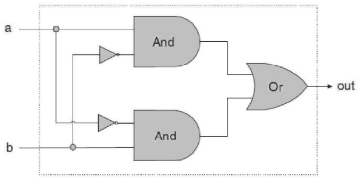


A	B	Xor(A,B)
0	0	0
0	1	1
1	0	1
1	1	0



$F(A,B) = Xor(A,B) = A\overline{B}+\overline{A}B$

2. HDL




```
CHIP Xor
{
   IN    a, b;
      OUT   out;

      PARTS:
      Not (in=a,    out=nota);
      Not (in=b,    out=notb);
      And (a=a,     b=notb, out=w1);
      And (a=nota,  b=b,    out=w2);
      Or  (a=w1,    b=w2,   out=out);
}
```

2. Lenguajes de descripción de hardware (HDL)

2. HDL

Nombre del chip

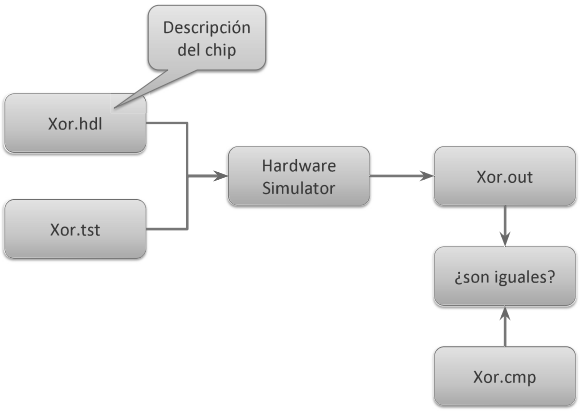
```
CHIP Xor
{
   IN    a, b;
      OUT   out;

      PARTS:
      Not (in=a,    out=nota);
      Not (in=b,    out=notb);
      And (a=a,     b=notb, out=w1);
      And (a=nota,  b=b,    out=w2);
      Or  (a=w1,    b=w2,   out=out);
}
```

2. HDL

Interfaz

```
CHIP Xor
{
   IN    a, b;
   OUT   out;

      PARTS:
      Not (in=a,   out=nota);
      Not (in=b,   out=notb);
      And (a=a,    b=notb, out=w1);
      And (a=nota, b=b,    out=w2);
      Or  (a=w1,   b=w2,   out=out);
}
```

2. HDL

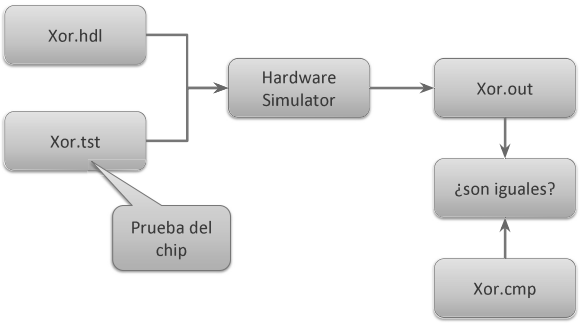


2. HDL

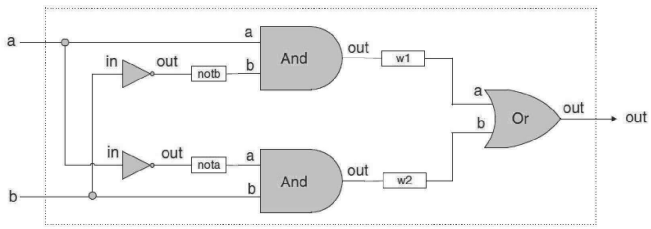
Construcción

```
CHIP Xor
{
   IN    a, b;
   OUT   out;

      PARTS:
      Not (in=a,   out=nota);
      Not (in=b,   out=notb);
      And (a=a,    b=notb, out=w1);
      And (a=nota, b=b,    out=w2);
      Or  (a=w1,   b=w2,   out=out);
}
```

2. HDL



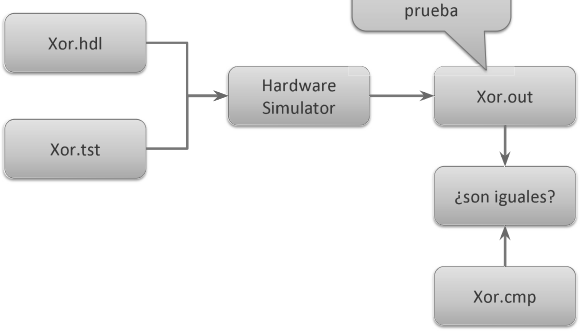
2. HDL



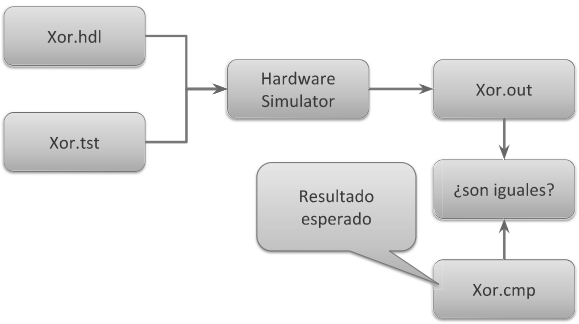

```
      PARTS:
      Not (in=a,   out=nota);
      Not (in=b,   out=notb);
      And (a=a,    b=notb, out=w1);
      And (a=nota, b=b,    out=w2);
      Or  (a=w1,   b=w2,   out=out);
}
```

2. HDL

Resultado de la evaluación de la prueba



2. HDL



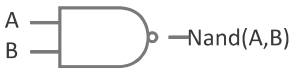
3. La puerta NAND

2. HDL

```
load       Xor.hdl,
output-file Xor.out,
compare-to  Xor.cmp,
output-list a, b, out

set a 0,
set b 0,
eval,
output;

set a 0,
set b 1,
eval,
output;

set a 1,
set b 0,
eval,
output;

set a 1,
set b 1,
eval,
output;
```

Fichero de test

3. NAND



A	B	Nand(A,B)
0	0	1
0	1	1
1	0	1
1	1	0

2. HDL

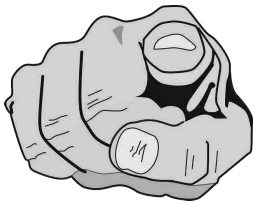
Ficheros: out y cmp

```
|   a   |   b   |  out  |
|   0   |   0   |   0   |
|   0   |   1   |   1   |
|   1   |   0   |   1   |
|   1   |   1   |   0   |
```

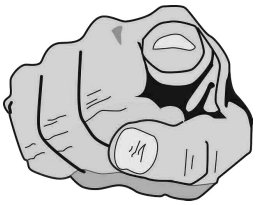
3. Nand

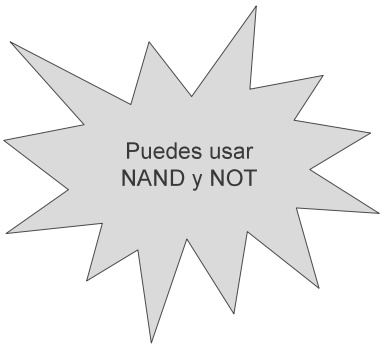
- Es posible construir las puertas lógicas NOT, AND y OR a partir de puertas Nand.

NOT

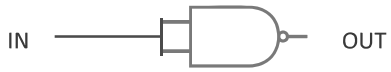


AND



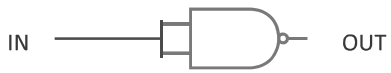


NOT



AND

NOT

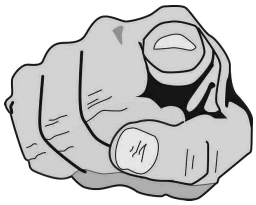



```
CHIP Not
{
      IN    in;
      OUT   out;

      PARTS:
      Nand (a=in,b=in, out=out);
}
```

AND


```
CHIP And
{
      IN    a,b;
      OUT   out;

      PARTS:
      Nand (a=a,b=b, out=temp);
      Not  (in=temp, out=out);
}
```

OR

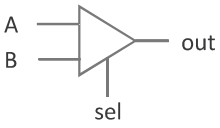


4. Multiplexores y Demultiplexores

5. Propiedades

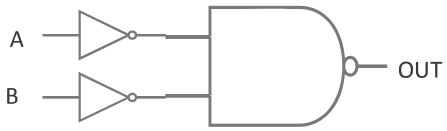
- Teoremas de DeMorgan
  - El complemento de un producto de dos variables es igual a la suma de los complementos de las variables.
    - $\overline{AB} = \bar{A} + \bar{B}$
  - El complemento de una suma de dos variables es igual al producto de los complementos de las variables.
    - $\overline{A + B} = \bar{A}\bar{B}$

4. Multiplexor



A	B	sel	out
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	1

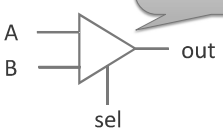
OR




```
CHIP Or
{
      IN    a,b;
      OUT   out;

      PARTS:
      Not   (in=a, out=nota);
      Not   (in=b, out=notb);
      Nand  (a=nota,b=notb, out=out);
}
```

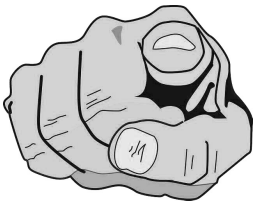
4. Multiplexor

Permite seleccionar unos datos frente a otros, dependiendo de un selector



A	B	sel	out
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	1

MUX

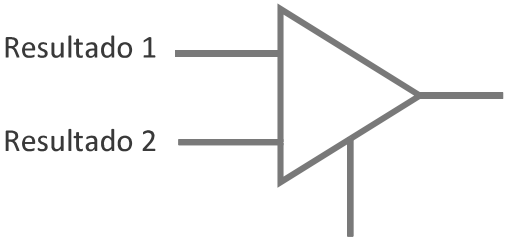


4. Multiplexor

$$F(A,B,S) = A\bar{B}\bar{S} + AB\bar{S} + \bar{A}BS + ABS$$

A	B	sel	out
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	1

4. Multiplexor

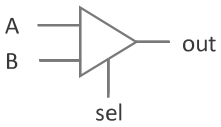


$$F(A,B,S) = A\bar{B}\bar{S} + AB\bar{S} + \bar{A}BS + ABS$$

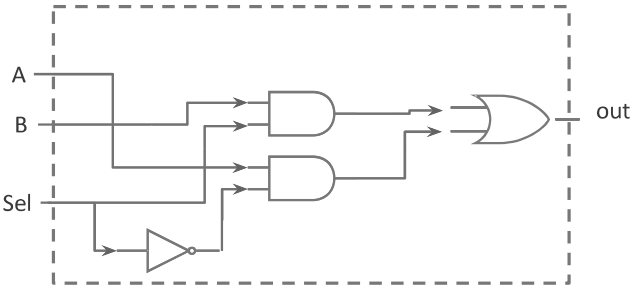
$$F(A,B,S) = BS + A\bar{S}$$

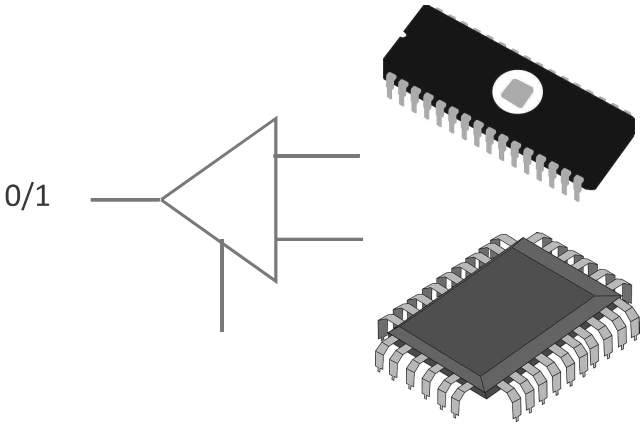
AB\S	0	1
00		
01		1
11	1	1
10	1	

4. Multiplexor

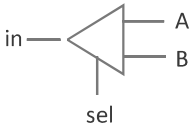


$F(A,B,S) = BS + A\bar{S}$



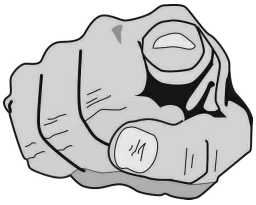


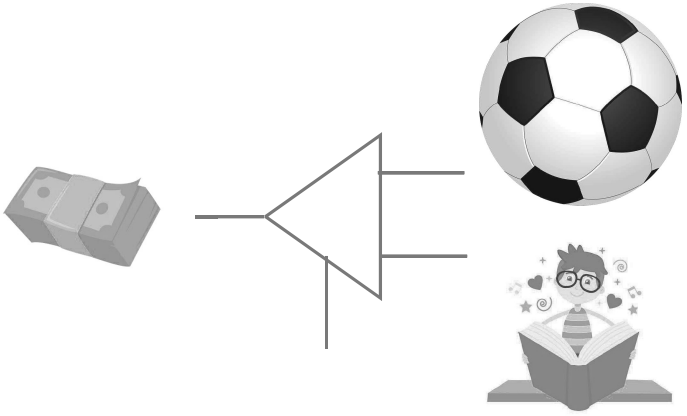
4. Demultiplexor



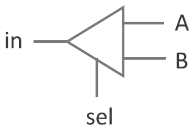
in	sel	A	B
0	0	0	0
0	1	0	0
1	0	1	0
1	1	0	1

DMUX





4. Demultiplexor

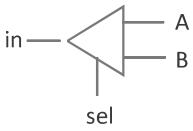


in	sel	A	B
0	0	0	0
0	1	0	0
1	0	1	0
1	1	0	1

$F_A(in,sel) = in\ \overline{sel}$

$F_B(in,sel) = in\ sel$

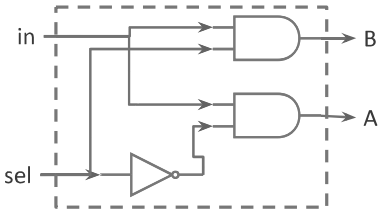
4. Demultiplexor



in	sel	A	B
0	0	0	0
0	1	0	0
1	0	1	0
1	1	0	1

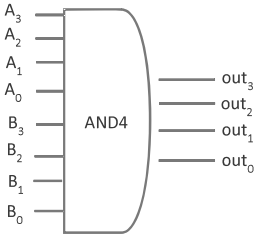
$F_A(in,sel) = in\ \overline{sel}$

$F_B(in,sel) = in\ sel$



5. Puertas multibit

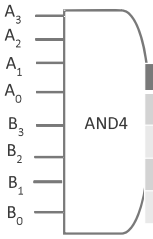
- Con operandos de 4 bits, se pueden ver como una puerta con 8 entradas y 4 salidas



5. Puertas lógicas multibit

5. Puertas multibit

- Con operandos de 4 bits, se pueden ver como una puerta con 8 entradas y 4 salidas



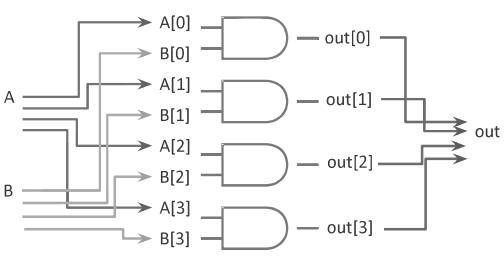
A3	A2	A1	A0	B3	B2	B1	B0	Out3	Out2	Out1	Out0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	1
0	0	1	1	1	1	1	0	0	0	1	0

5. Puertas multibit

- Es necesario construir puertas lógicas que realices operaciones entre dos operandos, los cuales tienen más de un bit.

A	B	out
0000	0000	0000
0000	0001	0000
0000	1111	0000
…	…	…
0001	0000	0000
0001	0001	0001
…	…	…
1111	1111	1111

5. Puertas multibit



A[4]	B[4]	Out[4]
0000	0000	0000
0000	0001	0000
0000	1111	0000
…	…	…
0001	0000	0000
0001	0001	0001
…	…	…
1111	1111	1111

5. Puertas multibit

```
CHIP And4
{
   IN a[4], b[4];
      OUT   out[4];

      PARTS:
      And (a=a[0],b=b[0],out=out[0]);
      And (a=a[1],b=b[1],out=out[1]);
      And (a=a[2],b=b[2],out=out[2]);
      And (a=a[3],b=b[3],out=out[3]);
}
```

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- https://pixabay.com/static/uploads/photo/2015/07/17/22/44/student-849828_640.jpg