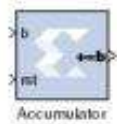# Accumulator

This block is listed in the following Xilinx Blockset libraries: Math and Index and Floating-Point.

The Xilinx Accumulator block implements an adder or subtractor-based scaling accumulator.

The block's current input is accumulated with a scaled current stored value. The scale factor is a block parameter.

Block Interface

The block has an input `b` and an output `q`. The output must have the same width as the input data. The output will have the same arithmetic type and binary point position as the input. The output `q` is calculated as follows:

$$q(n) = \begin{cases} 0 & \text{if } rst = 1 \\ q(n-1) \times FeedbackScaling + b(n-1) & \text{otherwise} \end{cases}$$

A subtractor-based accumulator replaces addition of the current input `b(n)` with subtraction.

Block Parameters

The block parameters dialog box can be invoked by double-clicking the icon in your Simulink model.

Basic tab

Parameters specific to the Basic tab are as follows:

- **Operation**: This determines whether the block is adder- or subtractor-based.

  Fixed-Point Output Precision

  - **Number of bits**: specifies the bit location of the binary point of the output number, where bit zero is the least significant bit.

  Overflow

    Refer to the section Overflow and Quantization.

Feedback scaling: specifies the feedback scale factor to be one of the following:

  1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, or 1/256.

Reinitialize with input 'b' on reset: when selected, the output of the accumulator is reset to the data on input port b. When not selected, the output of the accumulator is reset to

zero. This option is available only when the block has a reset port. Using this option has clock speed implications if the accumulator is in a multirate system. In this case the accumulator is forced to run at the system rate since the clock enable (CE) signal driving the accumulator runs at the system rate and the reset to input operation is a function of the CE signal.

Internal Precision tab

Parameters specific to the Internal Precision tab are as follows:

Floating Point Precision

*   **Input MSB Max**: The Most Significant Bit of the largest number that can be accepted.

*   **Output MSB Max**: The MSB of the largest result. It can be up to 54 bits greater than the Input MSB

*   **Output LSB Min**: The Least Significant Bit of the smallest number that can be accepted. It is also the LSB of the accumulated result.

Implementation tab

Parameters specific to the Implementation tab are as follows:

*   **Use behavioral HDL (otherwise use core)**: The block is implemented using behavioral HDL. This gives the downstream logic synthesis tool maximum freedom to optimize for performance or area.

*   **Implement using**: Core logic can be implemented in **Fabric** or in a **DSP48**, if a DSP48 is available in the target device. The default is **Fabric**.

Other parameters used by this block are explained in the topic Common Options in Block Parameter Dialog Boxes.

The Accumulator block always has a latency of 1.

LogiCORE™ Documentation

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