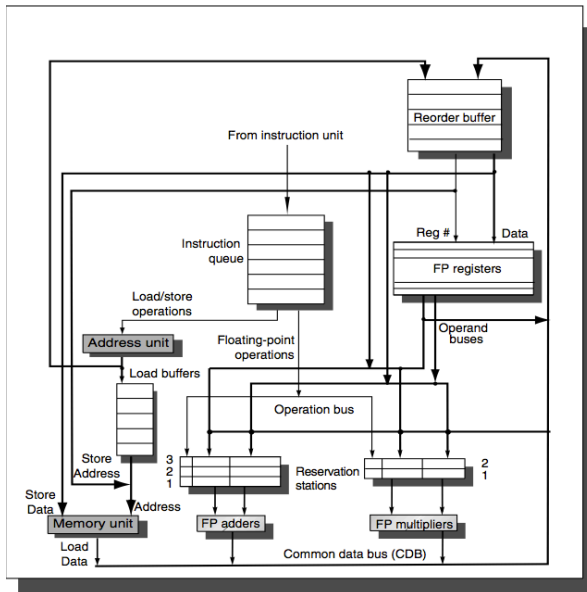# Out-of-Order Speculative Execution with a Retargetable ISA

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Tomasulo with Speculation

Another idea: Retargetable ISA with register load-store architecture

- Generalize instruction translation and dispatch
- Exploration of higher-level instruction abstractions within Bluespec
- Replace execution rule with multiple modules (e.g., floating point, vector ops)
- Investigation tradeoffs between abstraction and hardware performance
- Precedent with microcode and ISA simulators