Out-of-Order SMIPS

6.375 Microarchitecture Design Proposal
6 April 2011

Team: David S. Greenberg and Bhaskar Mookerji

For our 6.375 final project, we are implementing a superscalar processor using Tomasulo's algorithm.

1 Problem

2 High-Level Design

2.1 FPGA Issues

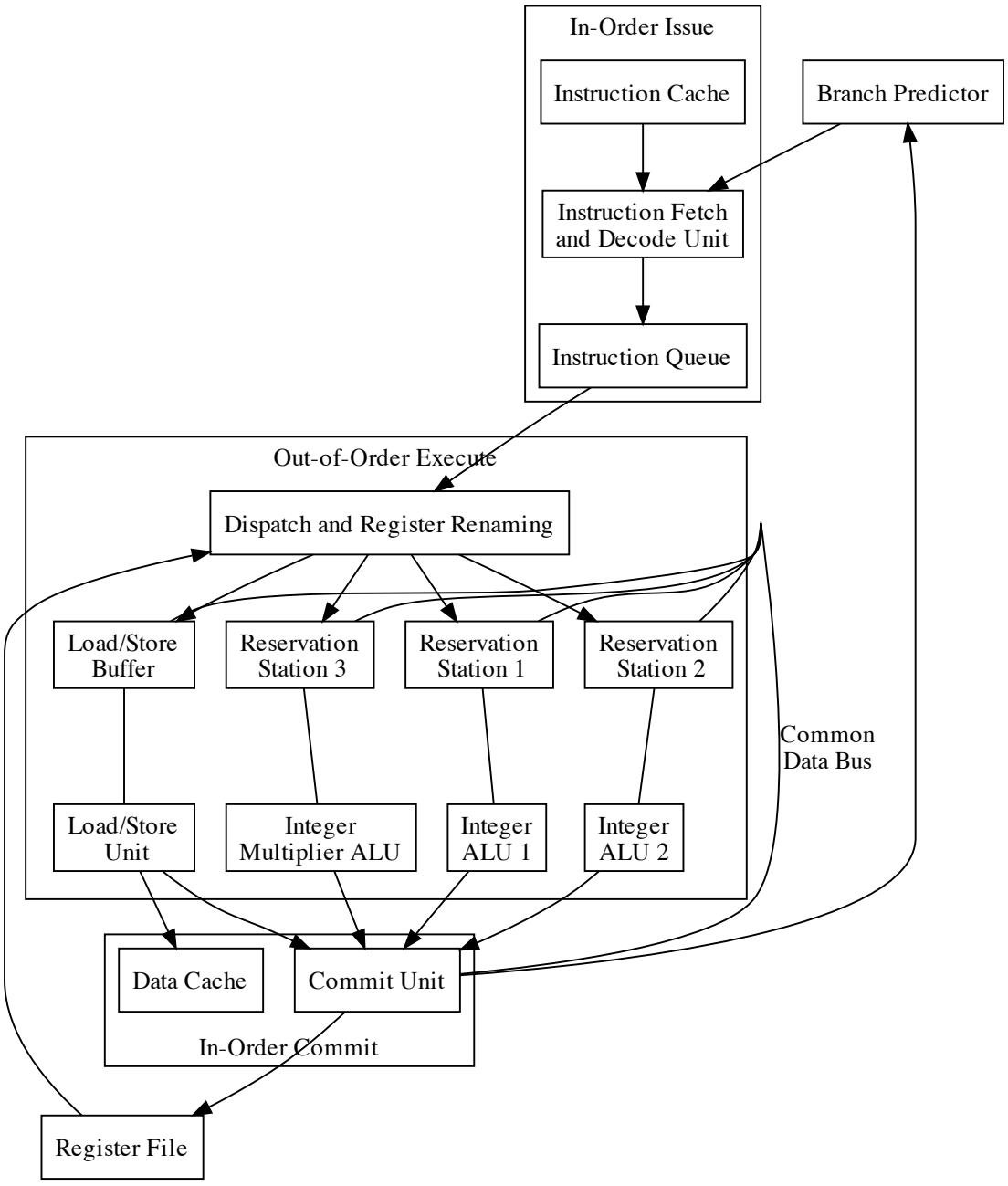

Figure 1: System architecture using out-of-order execution and pipelined integer arthmetic.

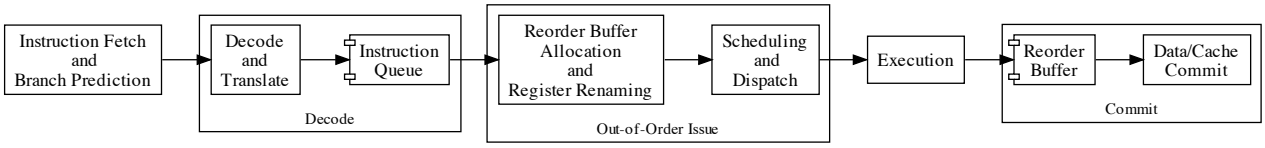

Figure 2: Instruction pipeline. Pipeline stage is labeled in-box, unless superseded by an overbox. A component box indicates component (such as a FIFO) between stages. Not included in this diagram is the reservation stations and load/store buffer in the execution stage.