# Out-of-Order SMIPS

6.375 Microarchitecture Design Proposal
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For our 6.375 final project, we are implementing a superscalar processor using Tomasulo's algorithm.

# 1 Microarchitecture Overview

## 1.1 New System Types

1. **Renamed Register Index**
2. **Reservation Station Entries**
3. **Reorder Buffer Entries**

# 2 Pipeline Stage Interfaces

1. **Pipeline Container: Processor**
2. **Instruction Fetch**
3. **Instruction Decode and Dispatch**
4. **Execute**
5. **Writeback and Commit**

# 3 Architectural Interfaces

1. **Issue and Dispatch Units**
2. **Reservation Stations**
3. **Common Data Bus**
4. **Reorder Buffer**
5. **Branch Predictor**

# 4 Goals and Testing Strategy

## 4.1 Functional Correctness

## 4.2 FPGA Synthesis

## 4.3 Performance

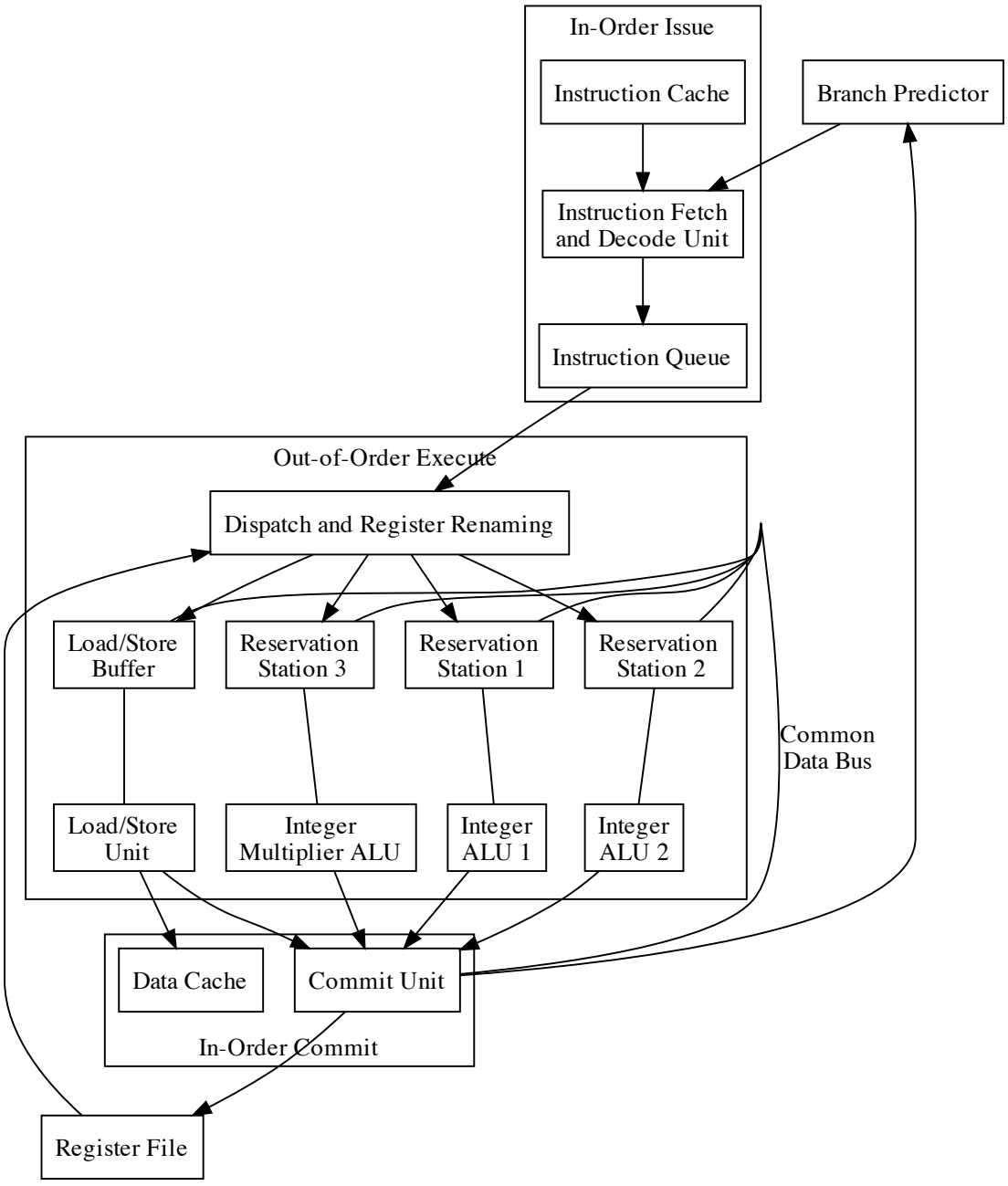


Figure 1: System architecture using out-of-order execution and pipelined integer arthmetic.

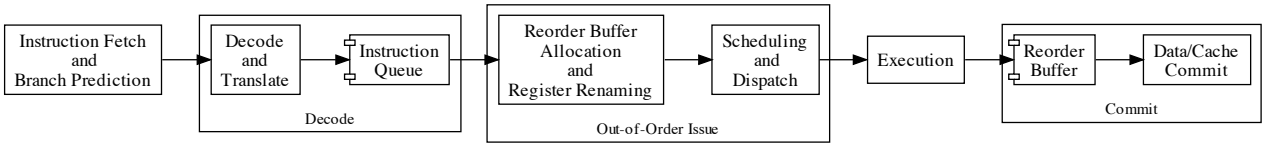


Figure 2: Instruction pipeline. Pipeline stage is labeled in-box, unless superseded by an overbox. A component box indicates component (such as a FIFO) between stages. Not included in this diagram is the reservation stations and load/store buffer in the execution stage.