

# ENG 581: Pipelined ADC Design

## Final Project

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# 1. Introduction

The objective of this project is to design the first stage of a fully differential  $20 \frac{Msamples}{sec}$  1.5b/stage 12-bit pipelined ADC. The primary goal is to design a residue amplifier, 1.5b sub-ADC and switched capacitor MDAC for the first stage to meet the overall ADC specifications in Table ?? with minimum power consumption. To simulate the performance of the overall ADC, the first stage design was instantiated in the ideal ADC model provided by the course, as shown in figure 1.1.

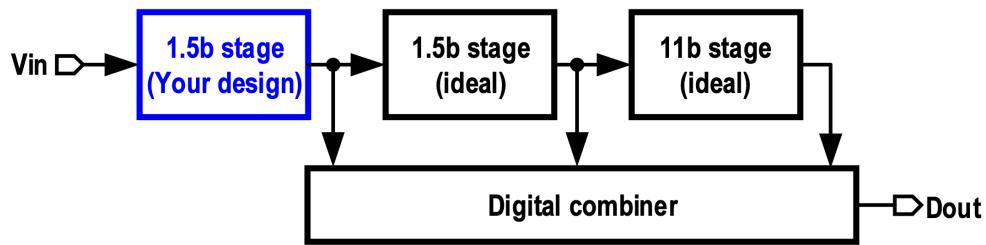


Figure 1.1: Pipelined ADC Block Diagram

## 1.1 First Stage

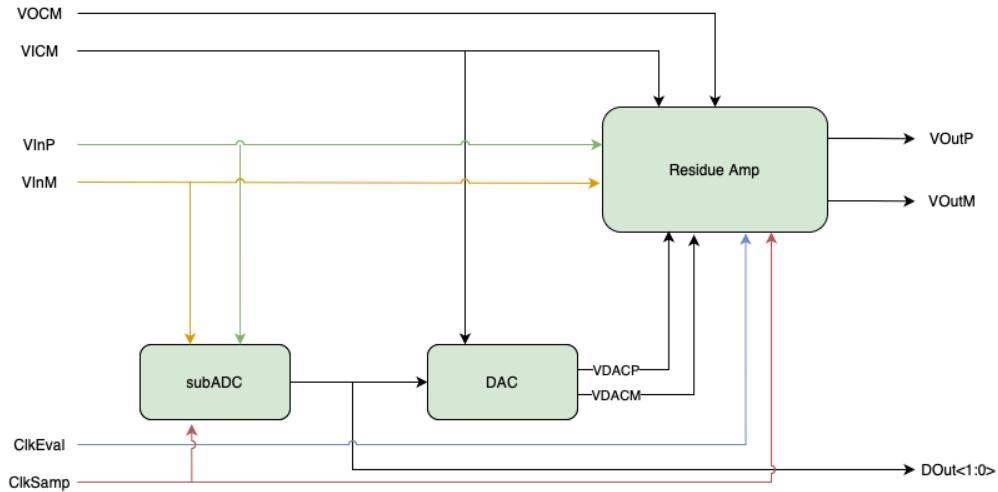


Figure 1.2: 1.5b Stage Block Diagram

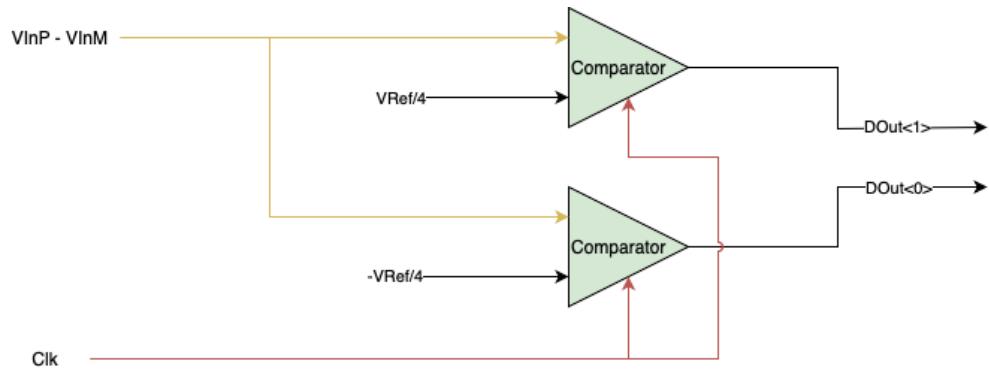


Figure 1.3: Sub ADC Block Diagram

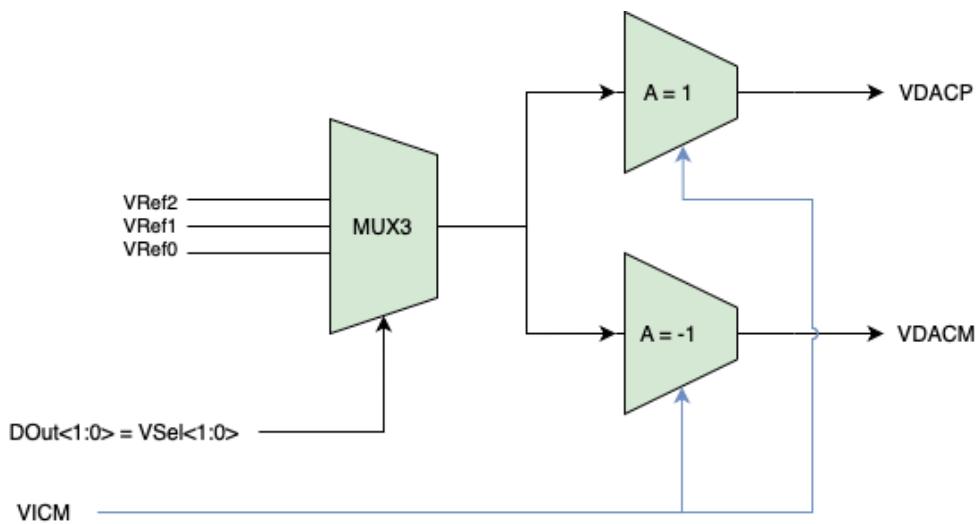


Figure 1.4: DAC Block Diagram

# 2. Residue Amplifier

## 2.1 Design Choices

The first design decision involves selecting between a single-stage or two-stage operational amplifier for the residue amplifier. While additional stages are typically advantageous for increasing the gain of the amplifier (e.g., the standard differential pair followed by a common-source stage), they also introduce additional parasitic effects. These parasitics can degrade the bandwidth, which is critical for the high-speed operation. Furthermore, stabilizing a multi-stage operational amplifier while meeting the required bandwidth and phase margin becomes increasingly challenging. For this application, the amplifier must achieve sufficient gain to minimize errors while ensuring adequate speed to meet the settling time requirements of the pipeline stage.

We chose a single-stage design, specifically a folded-cascode opamp, as it offers several advantages for our residue amplifier. This architecture should provide a bandwidth exceeding our requirements, simplify the compensation process to achieve the desired phase margin, and ensure that noise is primarily determined by the input capacitance, which can be modified. Additionally, the folded-cascode topology gives us the flexibility to implement gain boosting if higher gain is required to meet the gain error specifications.

## 2.2 Simulated Performance Summary

Please refer to table 2.1 for the simulated performance.

Design parameter/variable	Simulated performance
Supply voltage	1.8V
Closed loop gain	48.74 dB
Load capacitance ( $C_L$ )	1 pF
Settling time	250ns
Peak SNR	25 dB
THD ( $F_{in} = 0.5\text{MHz}$ )	6.5 dB
THD ( $F_{in} = 9\text{MHz}$ )	32.7 dB
Total power consumption [mW]	1.209
Differential DC loop gain ( $v_{od} = 0$ ) [dB]	48.74
Differential loop-gain unity gain bandwidth [MHz]	423.2
Differential loop-gain phase margin [deg]	71.59
CMRR [dB]	324 dB

Table 2.1: Amplifier Design Parameters and Specifications

### 2.3 Schematic

FULLY DIFFERENTIAL OP AMP

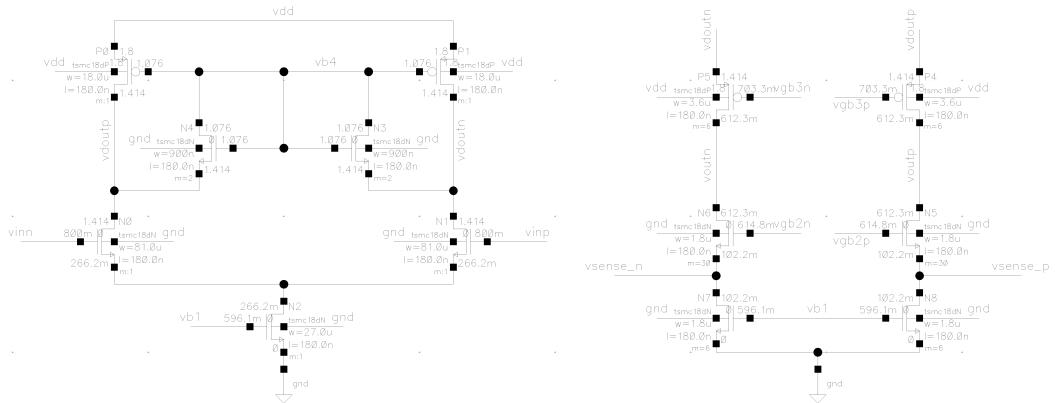


Figure 2.1: Residue Amplifier - Main Schematic

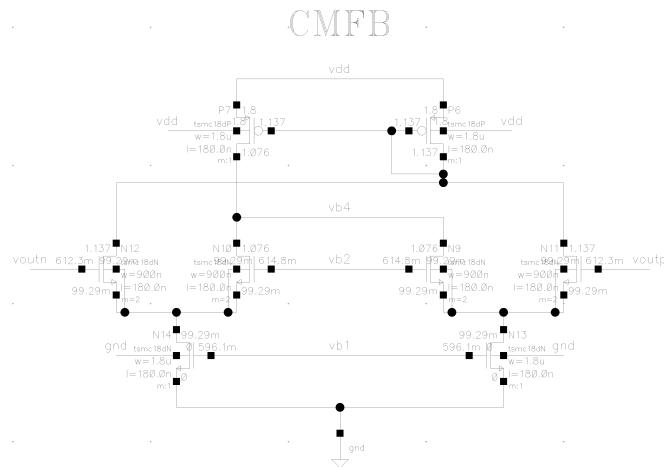


Figure 2.2: Residue Amplifier - CMFB Schematic

## BIASING

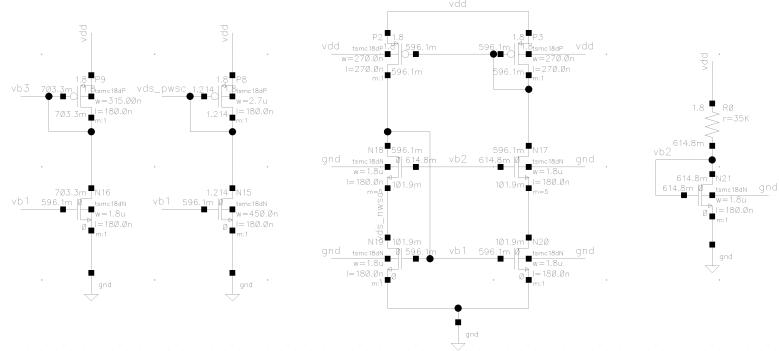


Figure 2.3: Residue Amplifier - Biasing Schematic

## GAIN BOOSTING



Figure 2.4: Residue Amplifier - Gain Boosting Schematic (not implemented in final amp)

<b>Device</b>	<b>Size (W/L)</b>	<b>Bias Current (uA)</b>	$g_m$ (mS)	$V_{ov}$ (mV)	<b>Region of Operation</b>
N0	450	155.1	3.375	54.49	Sub-threshold
N1	450	155.1	3.375	54.49	Sub-threshold
N2	150	310.1	4.444	103.4	Saturation
N3	5	4.62 fA	3.375	43.83	Cutoff
N4	5	4.62 fA	3.375	43.83	Cutoff
N5	10	111.6	2.393	55.44	Saturation
N6	10	111.6	2.393	55.44	Saturation
N7	10	111.6	1.51	100.5	Saturation
N8	10	111.6	1.51	100.5	Saturation
N9	5	9.287	174.7 uS	64.54	Saturation
N10	5	9.287	174.7 uS	21.99	Saturation
N11	5	9.139	172.5 uS	63.78	Saturation
N12	5	9.139	172.5 uS	63.78	Saturation
N13	10	18.43	247.9 uS	100.5	Triode
N14	10	18.43	247.9 uS	100.5	Triode
N15	2.5	10.72	133.2 uS	104.2	Saturation
N16	10	27.51	372.6 uS	103	Saturation
N17	10	18.58	398.5 uS	55.53	Saturation
N18	10	18.58	398.5 uS	55.53	Saturation
N19	10	18.58	251.2 uS	100.5	Saturation
N20	10	18.58	251.2 uS	100.5	Saturation
N21	10	33.86	418.7 uS	113.4	Saturation
P0	100	266.7	1.972	212.3	Saturation
P1	100	266.7	1.972	212.3	Saturation
P2	1	18.58	43.93 uS	557.9	Saturation
P3	1	18.58	43.93 uS	557.9	Saturation
P4	20	111.6	1.416	135.4	Saturation
P5	20	111.6	1.416	135.4	Saturation
P6	10	18.28	169 uS	173.9	Saturation
P7	10	18.57	170.5 uS	174.6	Saturation
P8	15	10.72	150.5 uS	116.4	Saturation
P9	1.785	27.51	72.41 uS	497.4	Saturation

Table 2.2: Device Specifications

# 3. 1.5b Sub-ADC

## 3.1 Design Choices

The design of the 1.5-bit Sub-ADC focuses on optimizing the trade-offs between speed, power, and noise performance. The core of this design lies in the comparators, which are critical for detecting threshold voltages and generating the digital outputs.

During the design process, multiple comparator architectures were evaluated:

- Dynamic latch-only comparators,
- Pre-amplifier-based comparators with clocked latches, and
- StrongARM latch comparators.

After extensive simulation and analysis, a **preamplifier with a clocked latch** was selected as the final design. This architecture provides:

- **High noise immunity:** The preamplifier boosts the input signal, improving the signal-to-noise ratio (SNR).
- **Speed:** The clocked latch ensures fast decision-making.
- **Robust operation:** Handles small signal variations effectively.

Additionally, a **0.75V common-mode offset** was added to the signal and reference voltages. This offset ensures that the comparator operates within the proper input common-mode range of the 180nm CMOS process.

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## 3.2 Schematic

The 1.5b Sub-ADC uses **two comparators**:

1. Comparator 1 compares the input voltage against a **1V threshold**.
2. Comparator 2 compares the input voltage against a **0.5V threshold**.

Each comparator consists of a **preamplifier stage** followed by a **clocked latch**. The complete comparator schematic is shown in Figure 3.1. The preamplifier stage is the same as the OTA used in the residue amplifier, and is not shown in the schematic below.

The transistor sizes and bias currents for the comparator are tabulated in Table 3.1.

Table 3.1: Transistor Sizes and Bias Currents for the Comparator

Transistor	Type	Width ( $\mu m$ )	Length ( $\mu m$ )
M0, M5	PMOS (Input Pair)	2.75 (x5)	0.18
M1, M4	PMOS (Load)	2.75 (x5)	0.18
N5, N7	NMOS (Latch)	0.9	0.18
N1, N6	NMOS (Latch Load)	0.9	0.18

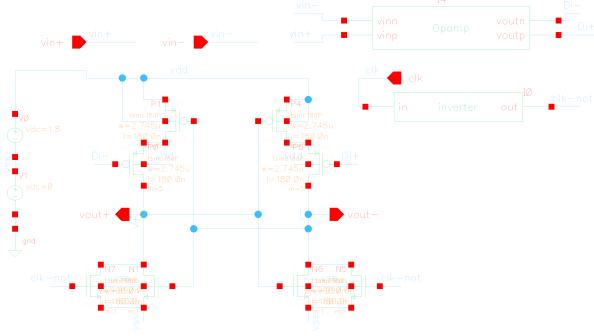


Figure 3.1: Schematic of the preamplifier with clocked latch comparator.

### 3.3 Transient Settling Waveform of the Comparator Output

The transient response of the comparator output is shown in Figure 3.2. The input signal includes a **0.75V common-mode offset**, which ensures the comparators operate within their valid input range.

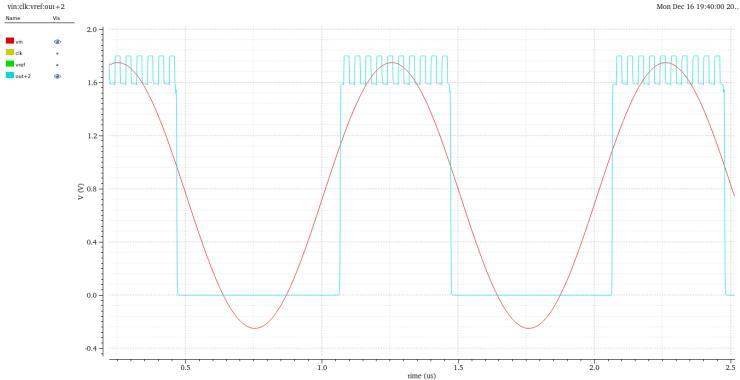


Figure 3.2: Transient response of the comparator output with 0.75V common-mode offset.

The waveform confirms the proper operation of the comparators, with clean transitions observed at the clock edges and minimal settling time. The wiggles on the latched input are due to the clocked latch. In the original design, we used a clocked pre-amplifier and used a switch capacitor circuit to provide signal stability and assist the clock gated latch. However, once we switched to using the high bandwidth OTA as the pre-amplifier, we saw better SNR, better performance, and less oscillations and good rise/fall time.

### 3.4 Simulation Results of the 1.5b Stage

#### 3.4.1 2-Bit Digital Output vs. Input Voltage

Figure 3.3 shows the digital output of the 1.5b Sub-ADC as a function of the input voltage. The two comparators produce the correct outputs for the given thresholds of 1V and 0.5V. These references correspond to the original 0.25 and -0.25 reference voltages. The output closely resembles that of the ideal Sub-ADC block

When the comparators and the multiplexer were tested with an ideal OTA, the system achieved an SNR of 80 dB.

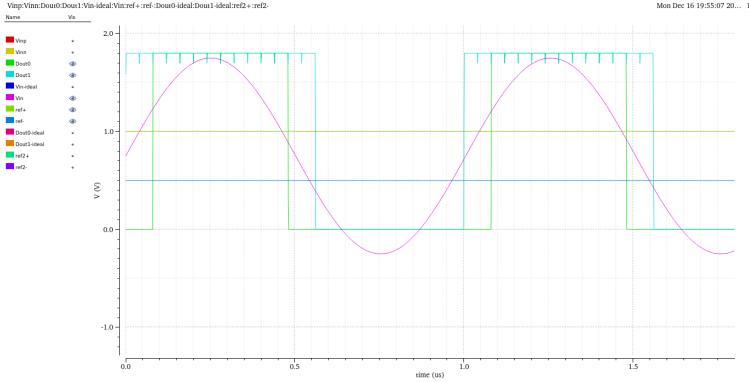


Figure 3.3: 2-bit digital output vs. input voltage for the 1.5b stage.

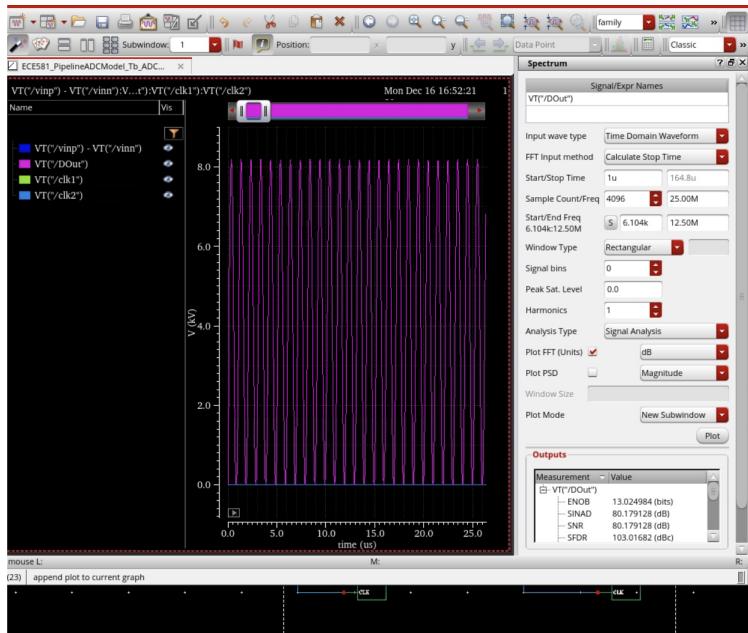


Figure 3.4: SNR of our comparator and mux

### 3.5 Conclusion

The 1.5b Sub-ADC successfully utilizes two preamplifier-based clocked latch comparators with thresholds set at 1V and 0.5V. A 0.75V common-mode offset ensured proper comparator operation. The design achieves:

- High SNR of 80 dB with an ideal OTA,
- Accurate residue voltage generation, and
- Correct digital outputs

This approach demonstrates an effective trade-off between performance, area, and power, making it suitable for pipeline ADC applications.

# 4. MDAC

## 4.1 Design Choices

The design of the Multiplying Digital-to-Analog Converter (MDAC) involves critical decisions regarding speed, power efficiency, and area utilization. A key component of the MDAC is the multiplexer (MUX), which is responsible for selecting the appropriate input signals for further processing. In our design, we implemented the MUX using 6 transmission gates, which serve both as a decoder and as switching lanes.

### Transmission Gate-Based MUX vs. Traditional NAND-Based Encoder

We initially explored a design approach using a NAND-based encoder followed by pass transistors to switch between the input signals. In this approach:

- A 2-to-4 **NAND-based decoder** was used to generate control signals for selecting the appropriate input.
- The decoder required multiple stages of logic gates, leading to increased propagation delay, parasitic capacitance, and higher power consumption.

To address these limitations, we adopted a **transmission gate-based MUX** design, which offers the following advantages:

1. **Speed Improvement:** Transmission gates provide near **rail-to-rail signal switching**, significantly reducing propagation delay compared to logic gates.
2. **Lower Area and Complexity:** By combining the decoder and switching functionality into the same transmission gates, the circuit eliminates the need for additional logic gates, reducing area and parasitic load.
3. **Analog Signal Integrity:** Transmission gates, consisting of both NMOS and PMOS transistors, offer lower **ON-resistance** across the entire input range, ensuring better signal integrity for analog signals.

## 4.2 Schematic

The MUX design consists of **6 transmission gates** configured to switch between three analog inputs ( $+0.5\text{ V}$ ,  $0\text{ V}$ , and  $-0.5\text{ V}$ ). The transmission gates act as both the decoder and the switching elements, simplifying the overall design.

Figure 4.1 shows the complete schematic of the transmission gate-based MUX, including the annotated clock phases used to control the transmission gates.

The transistor sizes for the transmission gates were minimally sized to reduce parasitic capacitance and improve switching speed.

## 4.3 Transient Analysis of the MUX

The transient response of the multiplexer was simulated in Cadence to verify its performance. Figure 4.3 shows the transient waveforms, demonstrating the proper switching behavior of the transmission gates as the select signals cycle through the three input voltages ( $+0.5\text{ V}$ ,  $0\text{ V}$ , and  $-0.5\text{ V}$ ).

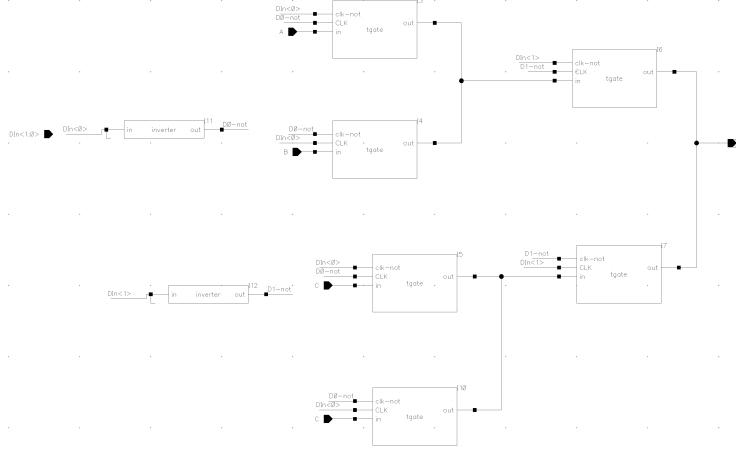


Figure 4.1: Schematic of the transmission gate-based multiplexer (MUX).

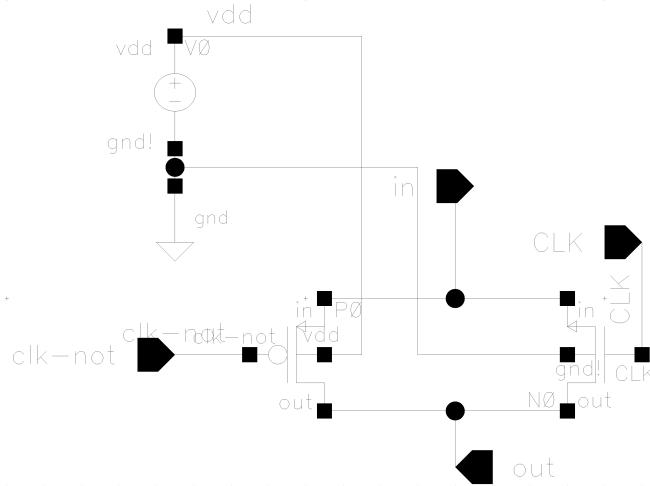


Figure 4.2: Schematic of the transmission gate.

## 4.4 Conclusion

The final MDAC multiplexer design successfully utilizes 6 transmission gates as both the decoder and switching elements. Compared to the traditional NAND-based encoder approach, the transmission gate-based design offers:

- Faster switching speeds due to reduced propagation delays,
- Improved signal integrity with near rail-to-rail switching,
- Reduced circuit complexity and area by combining decoding and switching into a single stage.

The transient simulations confirm the MUX's ability to correctly select and transmit the analog inputs with minimal delay and distortion, making it a suitable choice for the MDAC.

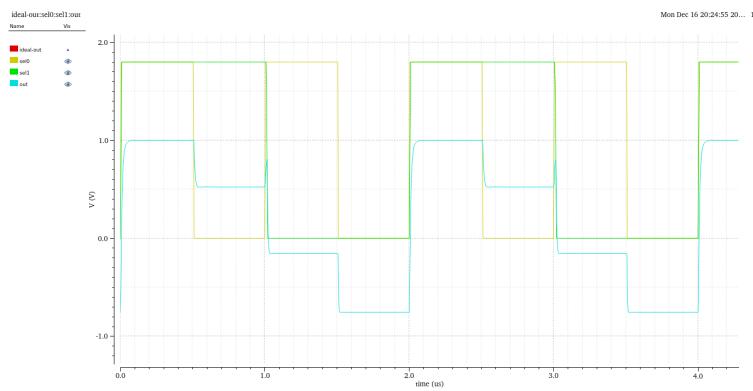


Figure 4.3: Transient analysis of the transmission gate-based MUX.

# 5. Simulation Results

Due to our ideal OTA not meeting all of our requirements, we included some additional data with simulations run with the ideal residue amp to show the performance of the other parts of our ADC see figures 5.6, 5.7 and 5.2.

	Simulated
<b>Supply voltage (<math>V_{DD}</math>)</b>	1.8V
<b>SNDR</b>	28dB
<b>SFDR</b>	27.34dB
<b>DNL</b>	See figures 5.4 and 5.6
<b>INL</b>	See figures 5.5 and 5.7
<b>Power consumption</b>	1.209mW

Table 5.1: Simulated Results

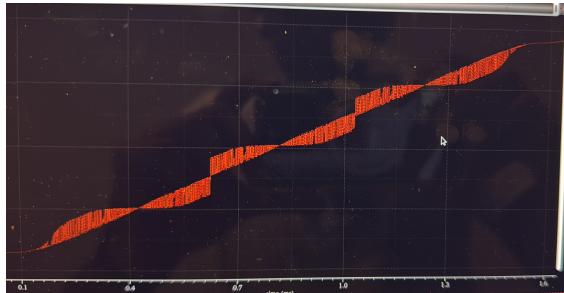


Figure 5.1: Ramp Output

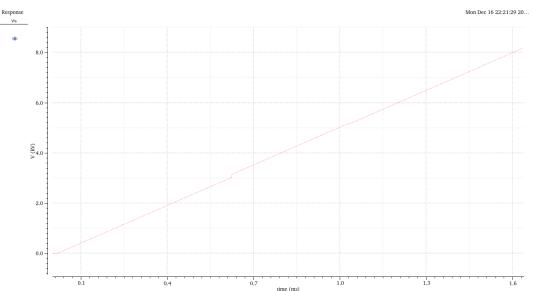


Figure 5.2: Ramp Output with ideal Residue Amp

## 5.0.1 Differential-Mode Loop-Gain AC Response

See figure 5.8.

## 5.0.2 Positive/Negative Step Response

See figures 5.9 and 5.10.

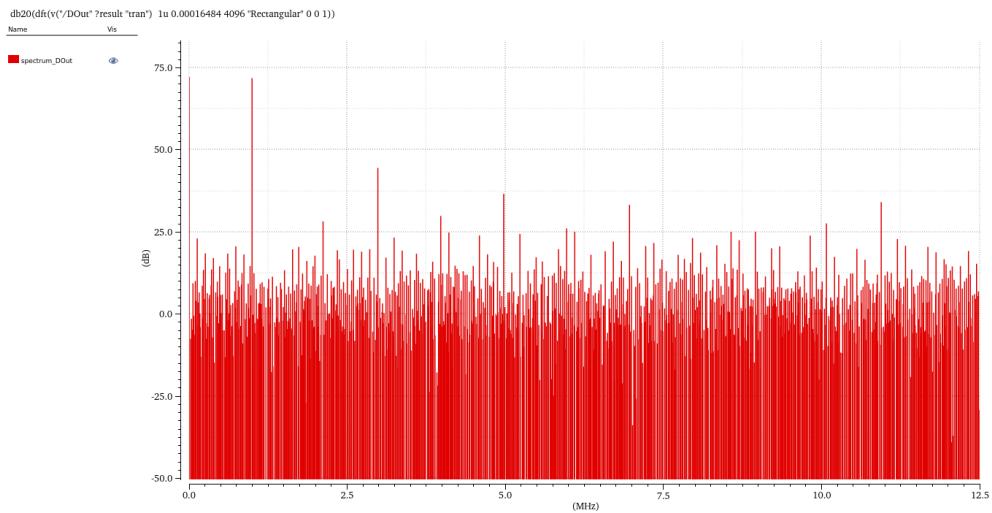


Figure 5.3: Overall ADC Frequency Spectrum - Sine Test

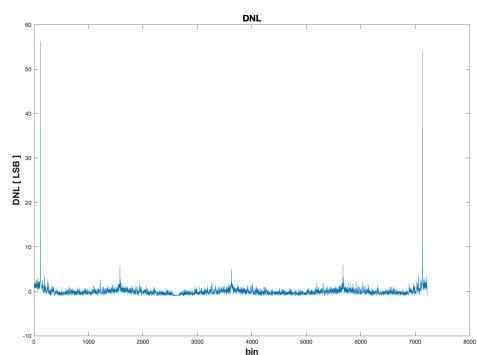


Figure 5.4: Overall ADC DNL

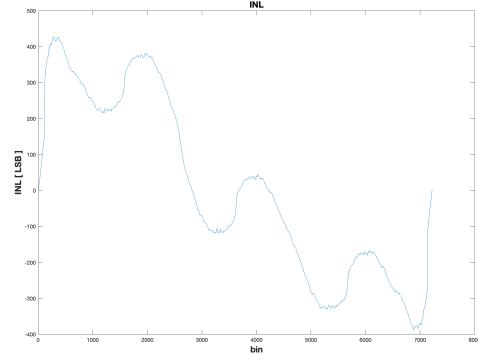


Figure 5.5: Overall ADC INL

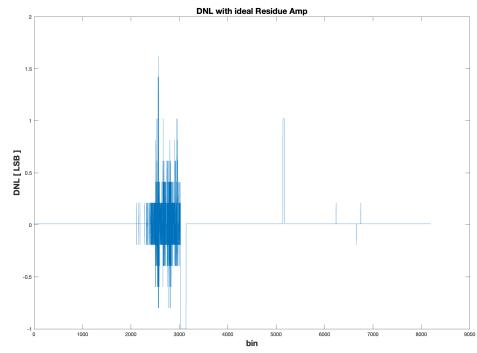


Figure 5.6: Overall ADC DNL with ideal residue amp

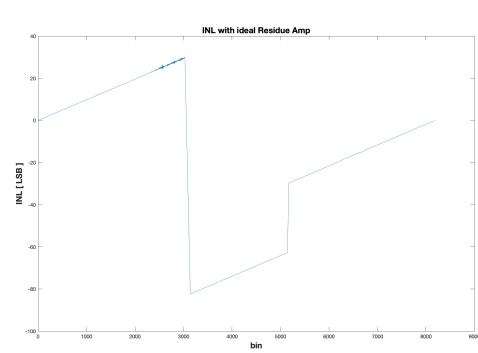


Figure 5.7: Overall ADC INL with ideal residue amp

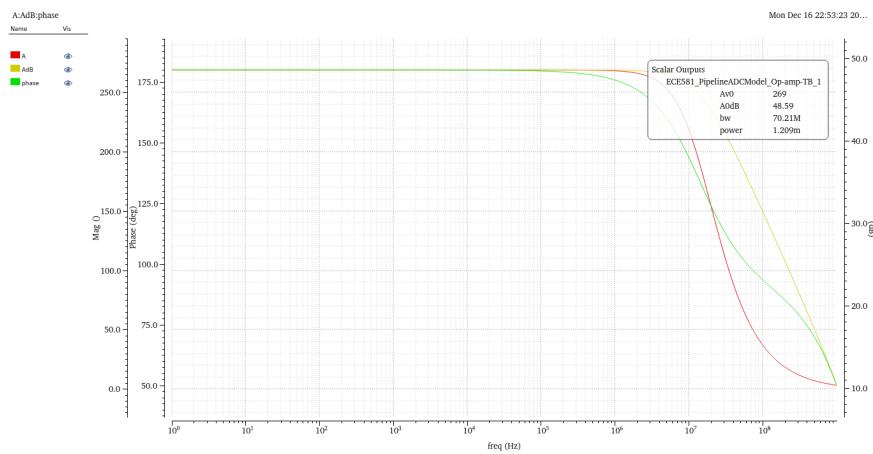


Figure 5.8: DC gain, loop-gain bandwidth, and phase- and gain-margins

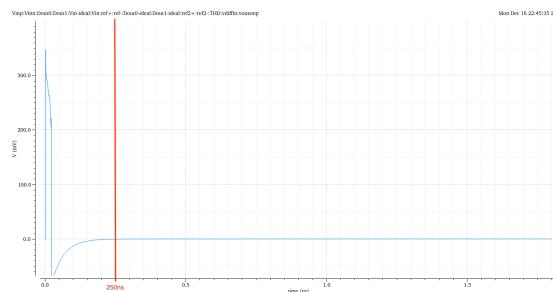


Figure 5.9: Positive Step Response

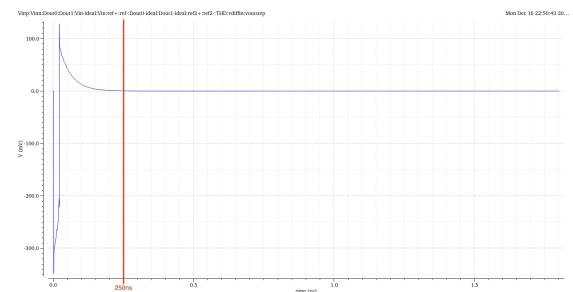


Figure 5.10: Negative Step Response