Dev Patel

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Education

University of Illinois Urbana Champaign Urbana, IL

Masters+BS in Electrical Engineering, Minor in Computer Science, 3.6 GPA *Aug. 2021 – Dec 2025*

- **Notable Courses**: *Digital IC Design, Analog Integrated Circuit Design, Embedded Systems Verification, Machine Learning in VLSI Design, Computer Architecture, Semiconductor Theory* **Masters focus on IC Design**

Experience

Apple May 2025 – August 2025

Silicon (Analog CAD) Engineering Intern *Cupertino, CA*

- Automated supply modeling in alignment with IEEE-1801 using Python,C++, and Perl, improving accuracy across multiple hardware projects

Rivian Jan 2025 – May 2025

Power Electronics Engineering Intern *Champaign, IL*

- Developed power/embedded systems for control and analysis of next generation charging systems

Rocket Lab USA May 2024 – August 2024

Space Systems Intern *Long Beach, CA*

- Designed machine learning models using PyTorch to automate PCBA defect analysis, reducing inspection times by over 2x
- Automated the battery cell screening workflow and enhanced the manufacturability of satellite battery packs by optimizing test procedures and assembly flow

ST Microelectronics June 2023 – December 2023

Embedded Applications Engineer *Chicago, IL*

- Prototyped a 250W grid-connected inverter using GaN MOSFETs and advanced gate drivers, and performed hardware validation with power supplies and oscilloscopes
- Developed firmware for MPPT algorithms and implemented control on STM32 microcontrollers

Projects

DVFS CPU with SDLS Cells (65nm TSMC CMOS) | *Tapeout* August 2025 – December 2025

- Leading tapeout effort for a DVFS-capable CPU using custom SDLS standard cells and Analog Controller
- Designed for ultra-low power and wide voltage swing, with support for RISC-V32 vector extension. Responsible for all AMS IP

Pipelined ADC in 180nm CMOS | *Cadence Virtuoso, SPECTRE* Nov 2024 – Dec 2024

- Designed the first stage (1.5b) of a 12-bit pipelined ADC, focusing on the residue amplifier, sub-ADC, and MDAC to meet high-performance and low-power requirements
- Used folded-cascode topology in the residue amp for high bandwidth and efficiency
- Verilog-A and SPICE modeling for simulation and test

Low Dropout Regulator (LDO) in 180nm CMOS | *Cadence Virtuoso, SPECTRE* April 2024 – May 2024

- Designed an LDO using a telescopic cascode OTA, with optimized biasing and compensation for high output swing and stability
- Achieved DC load regulation of 15.55 µV/mA and worst-case PSR of –1.42 dB through iterative simulation and loop-gain tuning

Leadership

Electronics Lead | *Illinois EV Concept* Aug 2021 – Dec 2024

- Designed power electronics circuits and embedded controllers, including DC-DC converters and BMS, while leading a 14+ member Electronics subteam in developing the EV2 challenger for the Shell Eco-Marathon
- Developed custom SOC Firmware and active balancing style hardware for custom BMS solution

Technical Skills

Design Software: Altium, OrCAD, KiCAD PCB Designer, Cadence Virtuoso
Simulation Software: ROS, CARLA, PSIM, LTSPICE, PSPICE, MATLAB, Simulink
Communications: CAN, SPI, I2C, UART
Languages: C, C++, Python, Java, Verilog, System Verilog
Cloud Frameworks: 3x Amazon Web Services Certified (Architect Associate, Professional, and Security Specialty)