ECE 483: Analog IC Design
Final Report
Low Dropout Regulator

Sayankar, Rutvik
rutviks2@illinois.edu

Patel, Dev
dpatel2@illinois.edu

January 8, 2025

1. Overall Design Approach

1.1 Design choices and System level trade-offs

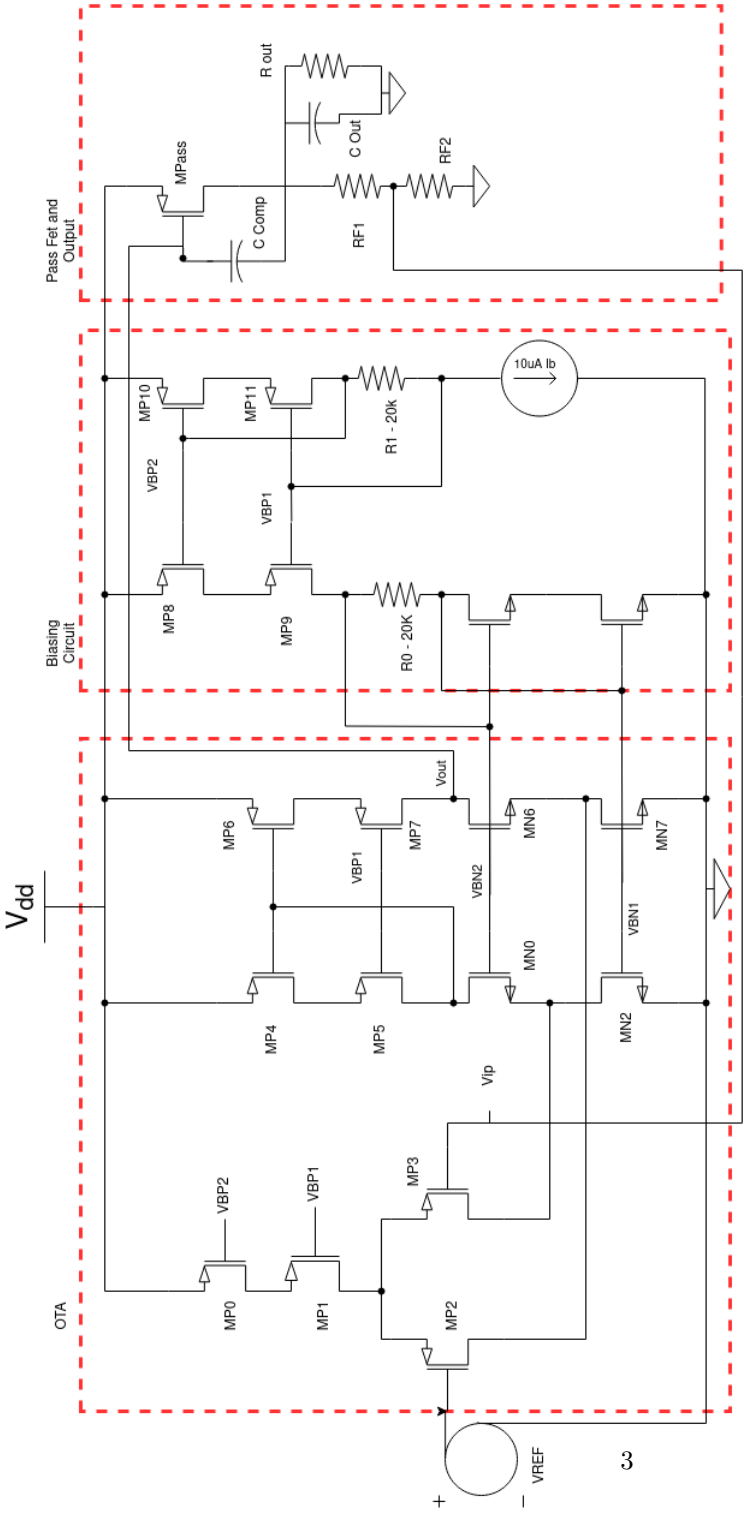
This project entailed the design and simulation of a low dropout regulator (LDO) meeting stringent input/output/load criteria while maintaining precise DC Load and Line Regulation. The initial stage of our design process involved a comprehensive study of the internal schematics and architecture of an LDO. Fundamentally, an LDO comprises an operational amplifier (op-amp) looped with biasing resistors and a pass transistor. Our choice of a PMOS pass transistor stemmed from its ability to generate a positive driving signal at low voltages, albeit with minor compromises in Line Regulation and Power Supply Rejection Ratio (PSSR).

In our analysis, we recognized the pivotal role of the Operational Transconductance Amplifier (OTA) in meeting performance targets. Initially, our 5-pack OTA failed to meet the required line regulation specifications, prompting us to explore a two-stage design. However, this approach introduced complexities such as pole stabilization challenges and increased circuit intricacies.

Subsequently, we narrowed down our design to a single-stage configuration and evaluated two options: the folded cascode and the telescopic cascode OTA. After careful consideration, we opted for the telescopic cascode topology due to its superior output swing, Input Common-Mode Range (ICMR), and compatibility with our PMOS pass device, which exhibits a wide output swing. The Telescopic cascode OTA required an additional biasing circuit. For this circuit, we leveraged the use of resistors and current mirroring to optimally bias the telescopic OTA at four different nodes. Additionally, we introduced a compensation capacitor between the Gate Voltage and Output Voltage of the pass transistor. The inclusion of a compensation capacitor in the LDO design serves a crucial role in enhancing the stability and simplifying the analysis and simulation of the system. Specifically, the compensation capacitor is strategically placed to make the output pole of the error amplifier dominant, thereby transforming the overall system behavior into that of a single pole system. By making the error amplifier output pole dominant, the compensation capacitor effectively adjusts the phase margin and loop gain characteristics of the LDO circuit. This adjustment is pivotal in ensuring stable and predictable performance across various operating conditions, load variations, and input disturbances. Through iterative simulations and parameter optimizations, we determined an optimal capacitance value of 10pF, ensuring stability and performance consistency.

2. Schematic & Parameters

2.1 Schematic



2.2 Device Parameters

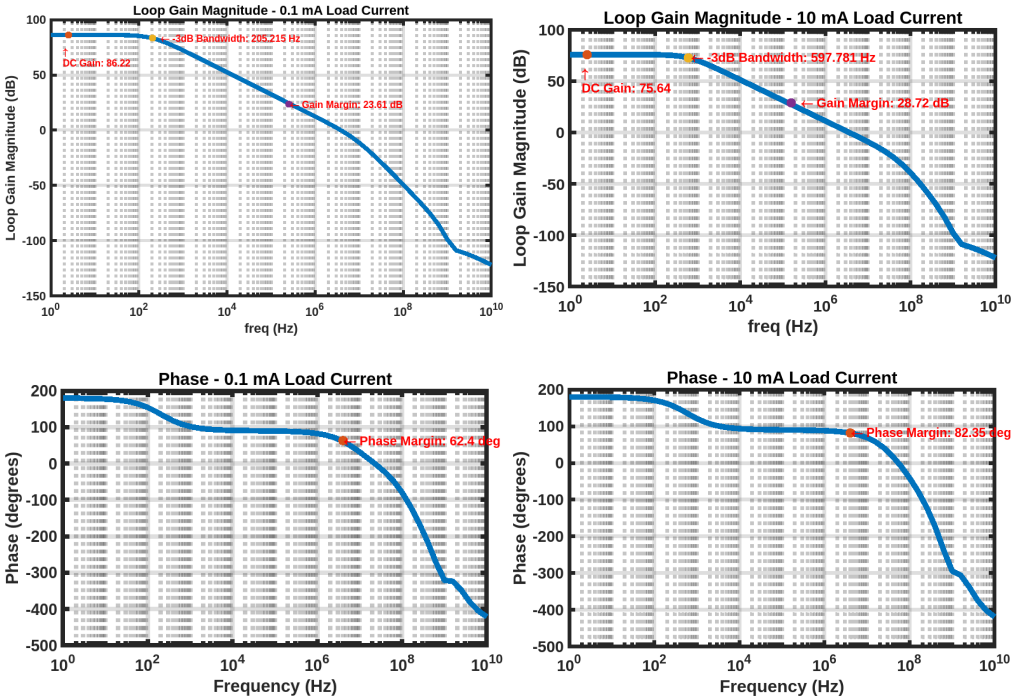
Device	W(μm)	L(nm)	Multiplier	g_m(μS)	r_{ds}(ohms)	Vov(mV)	I_{bias} (μA)
MPass	1.08	270	500	12.41m	5.864k	106.1	800
MP0	1.44	270	24	881.1	23.07k	114.7	60
MP1	1.44	270	24	911.2	770.3k	108.5	59.99
MP2	1.44	270	24	552.5	161.7k	57.96	29.96
Mp3	1.44	270	24	552	161.9k	58.41	29.97
MP4	1.44	270	4	148.7	132.3k	116.1	10.2
MP5	1.44	270	4	154	466.9k	109.5	10.2
MP6	1.44	270	4	148,7	131.9k	116.1	10.19
MP7	1.44	270	4	153.9	459.8k	109.6	10.19
MP8	1.44	270	4	147.6	148.5k	114.7	10.03
MP9	1.44	270	4	153	562.2k	104.2	10.03
MP10	1.44	270	4	147	139k	114.7	10
MP11	1.44	270	4	152	473.1k	108.2	10
MN0	.72	540	6	174.5	596.1k	89.27	10.2
MN2	.72	540	8	444	69.14k	177.1	40.17
MN4	.72	540	6	172	511.6k	90.43	10.03
MN5	.72	540	2	110.7	263.9k	177.1	10.03
MN6	.72	540	6	174.5	596.7k	89.22	10.19
MN7	.72	540	8	444.1	69.22k	177.1	40.17

3. Performance

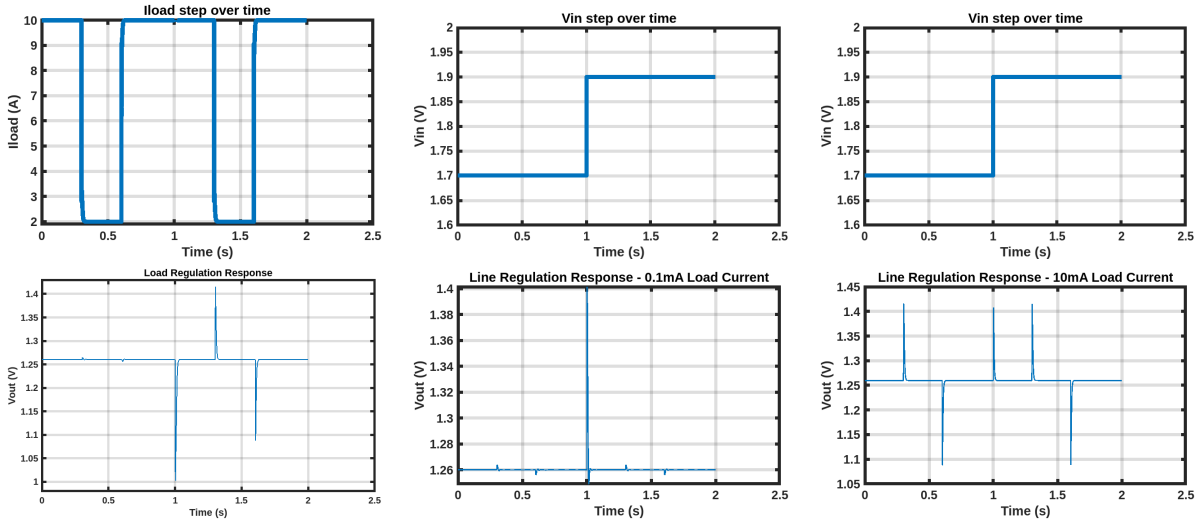
3.1 Simulation Results

Design Parameter/Variable	Specification	Simulated Performance
Input Voltage	1.8V ± 10%	1.8V
Output Voltage	1.0V - 1.4V	1.0V - 1.4V
Load Current	0.1mA - 10mA	0.1mA - 10mA
DC Load Regulation	$\leq 50\mu$V/mA	15.55μV/mA
DC Line Regulation	$\leq 500\mu$V/V	750μV/V
Quiescent Current	Minimum	600μA
PSR (@Fin = 1KHz/Fin = 1MHz)	-	-72.97dB/-12.31dB
Worst-case PSR	-	-1.42dB
DC loop gain (IL=0.1mA/IL=10mA)	-	86.22 dB / 75.64 dB
Loop-gain unity-gain frequency (IL=0.1mA/IL=10mA)	-	3.981 MHz / 3.479 MHz
Loop-gain phase margin(IL=0.1mA/IL=10mA)	-	62.4° / 82.35°
Loop-gain gain margin (IL=0.1mA/IL=10mA)	-	23.61 dB / 28.72 dB
Output noise (IL=0.1mA/IL=10mA)	-	61.3μV / 58.1μV

3.1.1 Loop-gain AC response



3.1.2 DC load and line regulation response



3.1.3 Power supply rejection (PSR)

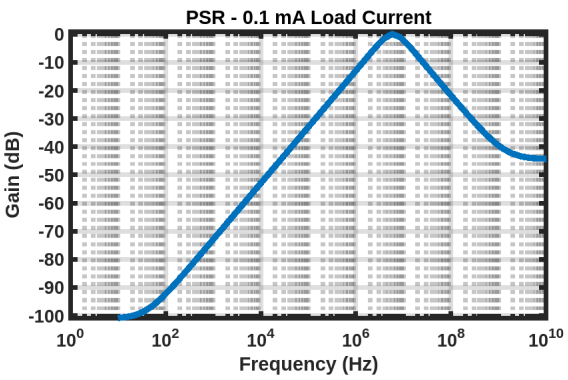


Figure 3.1: PSR with Minimum Load Current

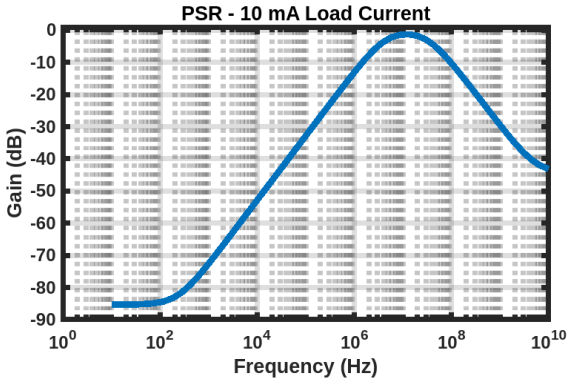


Figure 3.2: PSR with Maximum Load Current