Computer Organization and Architecture Laboratory

Laboratory Test 2

(August 28, 2024)

1. **Answer the following:**

The Fibonacci series is defined as follows:

$$F_0 = 0$$
$$F_1 = 1$$
$$F_i = F_{i-1} + F_{i-2}, \text{ for } i > 1$$

It is required to design a hardware to find out the *k*-th Fibonacci number. Assume that the numbers will be less than 256, i.e., can be stored in an 8-bit register.

[10 + 20 + 10 = 40 marks]

a) Draw the datapath for the hardware, clearly labelling the input and output ports of the various hardware modules. The value of *k* should be provided as an input. The *k*-th Fibonacci number should be generated as the output.

b) Write all the Verilog modules required to model the datapath, using ***structural modelling style***.

c) Write a test bench to feed the value of *k* to the top-level Verilog module realizing the datapath, and print the *k*-th Fibonacci number.