Group 1

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Computer Organization and Architecture Lab

Verilog Assignment 8: Instruction Encoding, Data Path and Control Unit Design

Instruction Encoding:

1. **R- Type:**

31 29	28 24	23 19	18 14	13 4	3 0
Opcode	Rd	Rs	Rt	Sh. Amt	Function
3 bits	5 bits	5 bits	5 bits	10 bits	4bits

Instruction	Opcode	Function
ADD	000	0000
SUB	000	0001
AND	000	0010
OR	000	0011
XOR	000	0100
NOR	000	0101
NOT	000	0110
SL	000	0111
SRL	000	1000
SRA	000	1001
INC	000	1010
DEC	000	1011
SLT	000	1100
SGT	000	1101
HAM	000	1111

2. **I – Type:**

Opcode	Rd	Rs	Immediate	Function
3 bits	5 bits	5 bits	15 bits	4bits

Instruction	Opcode	Function
ADDI	001	0000
SUBI	001	0001
ANDI	001	0010
ORI	001	0011
XORI	001	0100
NORI	001	0101
SLI	001	0111
SRLI	001	1000
SRAI	001	1001
SLTI	001	1100
SGTI	001	1101
LUI	001	1110
HAMI	001	1111

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3. Load Store Instructions:

Opcode	Rs	Rt	Immediate
3 bits	5 bits	5 bits	19 bits

Instruction	Opcode
LD	010
ST	011

4. B – Type:

Opcode	Rd	Rs	Immediate	Function
3 bits	5 bits	5 bits	15 bits	4bits

Instruction	Opcode	Function
BMI	100	0001
BPL	100	0010
BZ	100	0100
BR	100	1000

5. CMOV:

Opcode	Rs	Rt	Rd	Don't Care
3 bits	5 bits	5 bits	5 bits	14 bits

Instruction	Opcode
CMOV	110

6. Program Control:

Opcode	Don't Care	Function
3 bits	25 bits	4 bits

Instruction	Opcode	Function
HALT	111	0001
NOP	111	0010
JAL	111	0100

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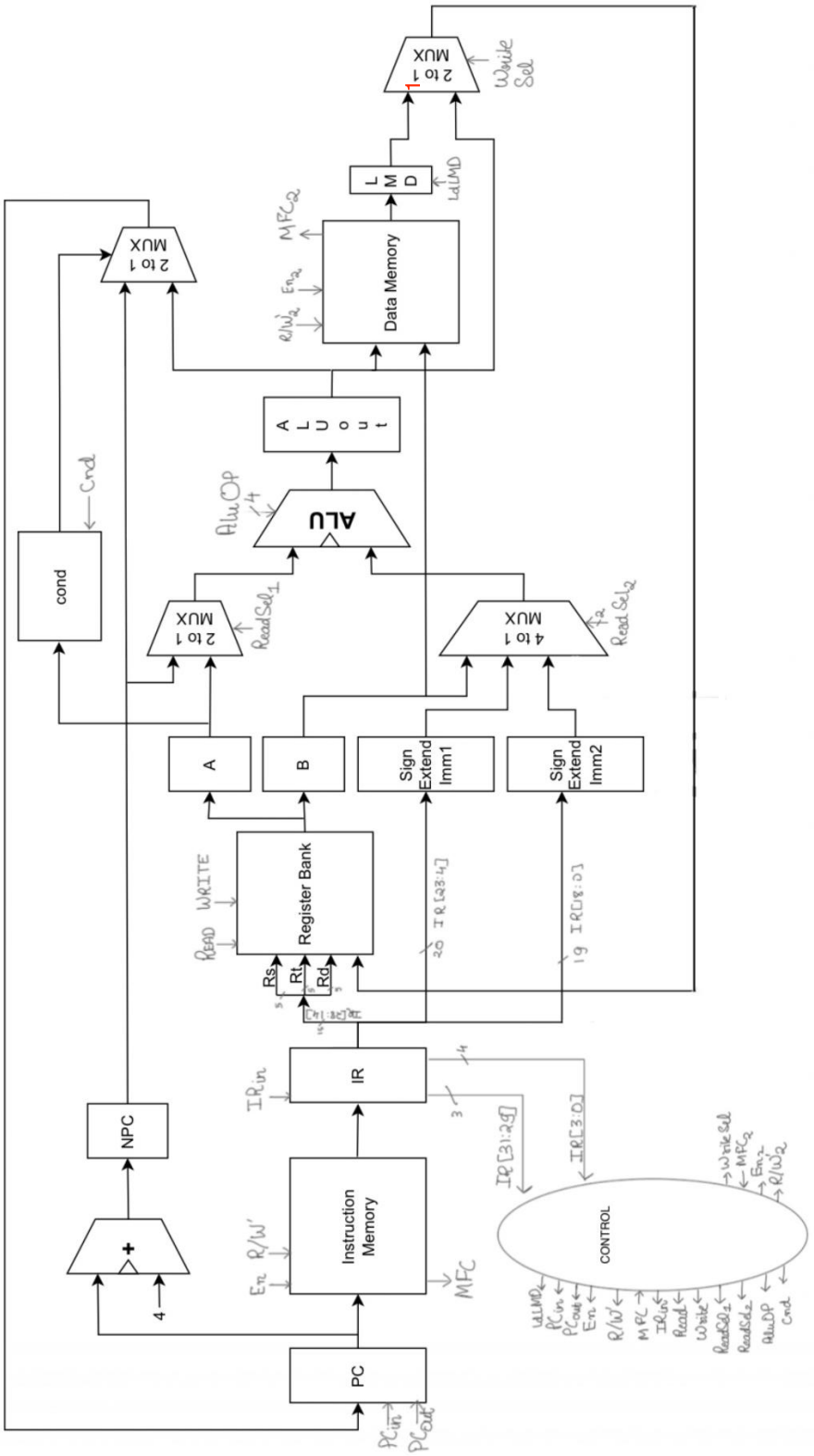
Data Path:



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Control Unit Design:

Instruction Fetch Signals common to all Instructions:

- T1: PCout, En, R/W' = 1
- T2: WMFC
- T3: IRin

1. R Type:

- T4: READ, WRITE, ReadSel1 = 0, ReadSel2 = 0, AluOP = func, WriteSel = 0, PCin
- T5:
- T6: End

2. I Type:

- T4: READ, WRITE, ReadSel1 = 0, ReadSel2 = 1, AluOP = func, WriteSel = 0, PCin
- T5:
- T6: End

3. Load Instruction:

- T4: READ, ReadSel1 = 0, ReadSel2 = 2, AluOP = 0, R/W'2 = 1, En2 = 1, PCin
- T5: WMFC2,
- T6: LdLMD, WriteSel = 1, Write, End

4. Store Instruction:

- T4: READ, ReadSel1 = 0, ReadSel2 = 2, AluOP = 0, R/W'2 = 0, En2 = 1, PCin
- T5: WMFC2
- T6: End

5. B-Type Instruction:

- T4: Read, ReadSel1 = 1, ReadSel2 = 1, AluOP = 0, Cnd = func, PCin
- T5:
- T6: End

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Control Signals:

PCOut : T1

En : T1

R/W' : T1

IRin : T3

READ : T4

PCin : T4

WRITE : T4(I1 + I2) + T6(I3)

ReadSel1 : T4(I5)

ReadSel21 : T4(I2 + I5)

ReadSel22 : T4(I3 + I4)

ALUOp : T4(I1 + I2)Func

WriteSel : T6(I3)

En2 : T4(I3 + I4)

R/W'2 : T4(I3)

LdLMD : T6(I3)

Cnd : T4(I5)Func

Assumptions and Justifications:

To reduce the number of states in finite state machine, all instructions are completed in 6 time steps even though some instructions can be completed in fewer time steps.

MOVE command is not explicitly specified as it is converted to an ADDI Rx, Ry, 0.

The RET register is located in the register bank at R16.

Instructions with same control signals except for the operations were pooled into a single Instruction class (R Type, I type, B type) and the specific operation was passed using function bits.

Add operation has been assigned as ALUOp = 0 to avoid extra signals in Move and Branch.