Wenjing Jin

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Education

2017 – present **Ph.D. in Computer Science and Engineering**
Seoul National University, Korea
Thesis: Software-Transparent DRAM Power Savings and Reliability Enhancement for CXL-enabled Disaggregated Memory

2015 – 2017 **M.S. in Electrical and Computer Engineering**
Sungkyunkwan University, Korea
Thesis: Optimizing Degree of Parallelism for Spark Clusters

2009 – 2013 **B.S. in Electronic Communication Engineering**
Yanbian University, China

Research Area

Memory System — Memory management unit (MMU), Linux kernel memory management, DRAM, CXL disaggregated memory, Power management, RAS features.

Other Technologies — Solid-state drive (SSD), RISC-V, Linux kernel optimization.

Research Publications

2023 **Wenjing Jin**, Wonsuk Jang, Haneul Park, Jongsung Lee, Soosung Kim, and Jae W. Lee, "DRAM Translation Layer: Software-Transparent DRAM Power Savings for Disaggregated Memory", in *Proceedings of the 50th Annual International Symposium on Computer Architecture (ISCA)*, Orlando, Florida, June 2023.

2020 Gyusun Lee*, **Wenjing Jin***, Wonsuk Song, Jeonghun Gong, Jonghyun Bae, Tae Jun Ham, Jae W. Lee, Jinkyu Jeong, "A Case for Hardware-based Demand Paging", in *ACM/IEEE 47th Annual International Symposium on Computer Architecture (ISCA)*, Valencia, Spain, May 2020. (* **co-first author**)

2019 Jonghyun Bae, Hakbeom Jang, Jeonghun Gong, **Wenjing Jin**, Shine Kim, Jaeyoung Jang, Tae Jun Ham, Jinkyu Jeong, Jae W. Lee, "SSDStreamer: Specializing I/O Stack for Large-Scale Machine Learning", in *IEEE Micro*, September/October 2019.

2019 Shine Kim, Jonghyun Bae, Hakbeom Jang, **Wenjing Jin**, Jeonghun Gong, Seungyeon Lee, Tae Jun Ham, and Jae W. Lee, "Practical Erase Suspension for Modern Low-latency SSDs", in *USENIX Annual Technical Conference (ATC)*, Seattle, Washington, July 2019.

2017 Jonghyun Bae, Hakbeom Jang, **Wenjing Jin**, Jun Heo, Jaeyoung Jang, Joo-Young Hwang, Sangyeun Cho, and Lee, Jae W. Lee, "Jointly Optimizing Task Granularity and Concurrency for In-memory Mapreduce Frameworks", in *IEEE International Conference on Big Data (BigData)*, Boston, MA, December 2017.

2016 Jonghyun Bae, Sangoh Jeong, **Wenjing Jin**, and Jae W. Lee, "ggplot2.SparkR: Rebooting ggplot2 for Scalable Big Data Visualization", in *Spark Summit East*, New York City, New York, February, 2016.

Patents

US,EP,CN,KR **Method for processing page fault by processor (US11436150B2, EP3916567B1, CN113742115B, KR102400977B1)**
with Jinkyu Jeong, Jae W. Lee, Gyusun Lee, and Tae Jun Ham.

Patents (continued)

KR **MEMORY SYSTEM AND COMPUTING SYSTEM INCLUDING THE SAME (20230376427)** with Kiseok Oh, Jae W. Lee, Jongsung Lee, and Juyun Jung.

Engineering and Prototyping Projects

2021-2022 **Prototyping hardware-based demand paging.**

- Based on the research paper: [ISCA'20] "A Case for Hardware-based Demand Paging".
- Implemented hardware-based demand paging using FPGA on the RISCV Rocket core.
- TSMC 40nm GP tape-out.

2015 **ggplot2.sparkR package for Apache Spark.**

- ggplot2.SparkR is an R package for scalable visualization of big data represented in Apache Spark DataFrame.
- Web site: `http://papl-skku.github.io/ggplot2.SparkR/`

Talks

2023 "DRAM Translation Layer: Software-Transparent DRAM Power Savings for Disaggregated Memory", in 2023^{2nd} SNU-Samsung CXL/UCIe Workshop. Dec 7.

Honors and Awards

2017-2018 **SNU Global Scholarship**, Seoul National University.
2015-2016 **International Student Scholarship**, Sungkyunkwan University.
2013 **President's Award for Academic Excellence**, Yanbian University.
2011-2013 **Scranton Women's full scholarship**, Scranton Women's Leadership Center, Korea.
2011-2012 **Model Student of Academic Records**, Yanbian University.

Skills

Languages	Reading, writing and speaking competencies for English, Mandarin Chinese, and Korean.
Programming Languages	Java, Scala, C, Verilog, Chisel, R, Shell, LaTeX
Tools and Technologies	Docker, Git, Google Cloud, FPGA, RISC-V, AXI, NVMe, experience in using simulators like Gem5, ZSim, DRAMSim, and Ramulator.