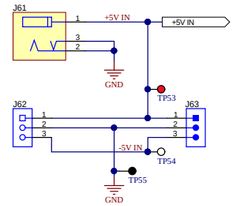
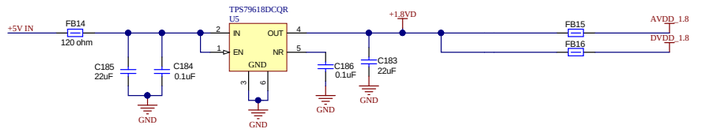
Input Power Connector

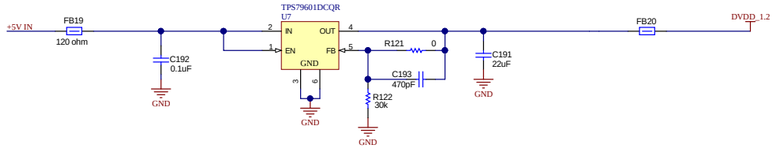


AFE Power Supply

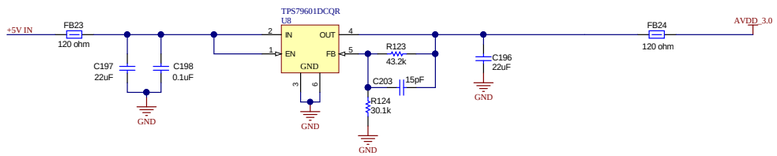
+1.8V



+1.2V

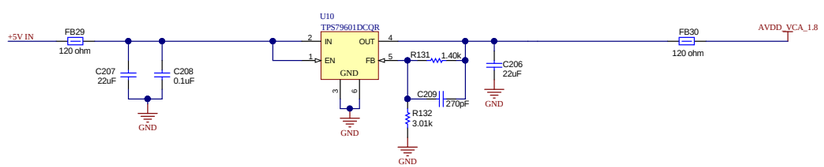


+3.15V



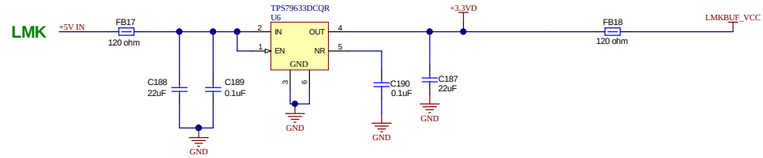
+5VA

+1.8V



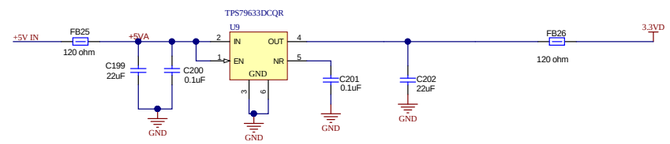
LMK and CW Power Supply

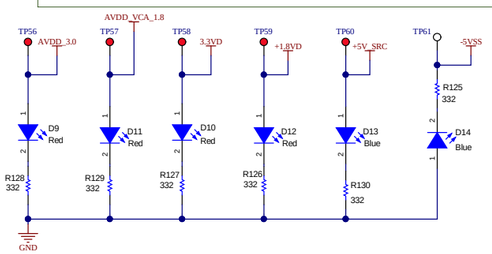
LMK

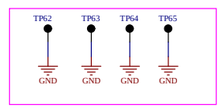


CW -5V

+3.3VD







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SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 1 of 13
Drawn By: Praveen Aroul		File: DC075B_POWER_SUPPLIES.SchDoc	Size: C
Engineer: Praveen Aroul		Contact: http://www.ti.com/support	

TEXAS INSTRUMENTS
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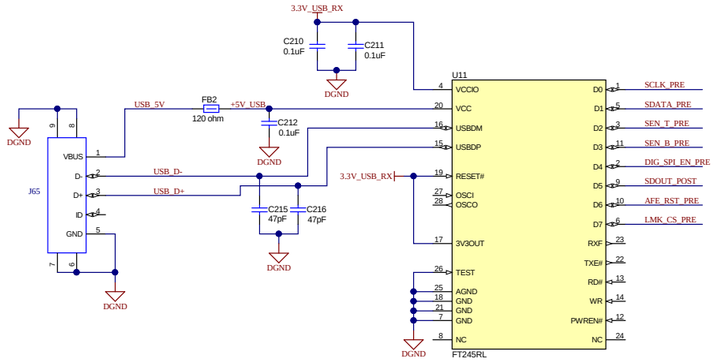
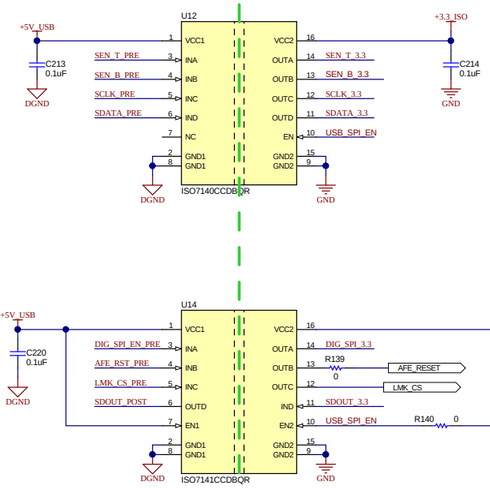
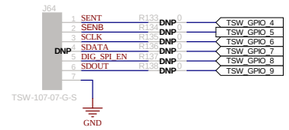
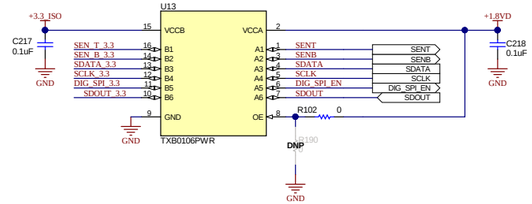
USB<->SPI









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Drawn By: Praveen Aroul		File: DC075B_USB.SchDoc	Size: C
Engineer: Praveen Aroul		Contact: http://www.ti.com/support	

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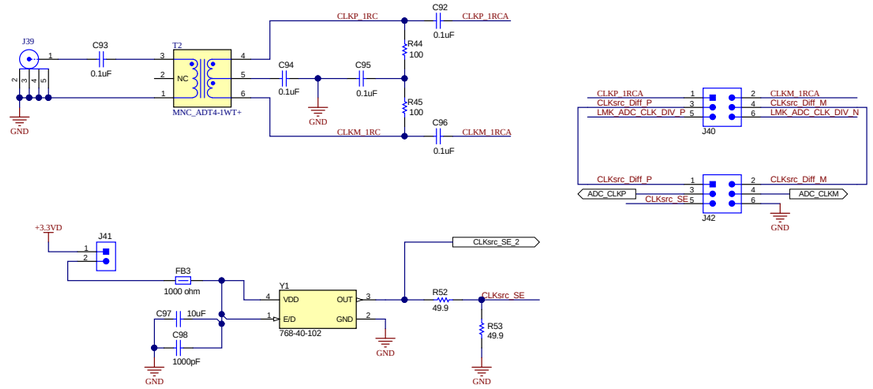
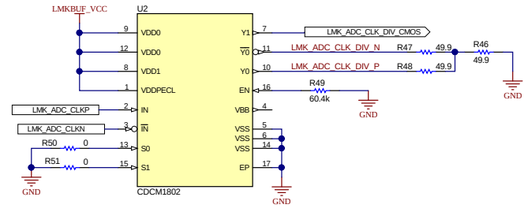
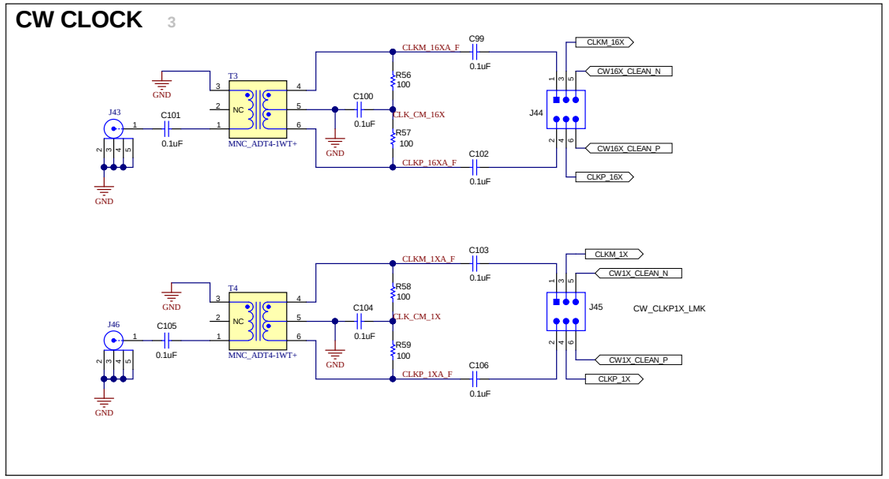
ADC CLOCK





CW CLOCK 3



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Number: DC075	Rev: B	Sheet Title: INPUT CLOCKS	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 3 of 13
Drawn By: Praveen Aroul		File: DC075B_INPUT_CLOCKS.SchDoc	Size: C
Engineer: Praveen Aroul		Contact: http://www.ti.com/support	

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LMK04826

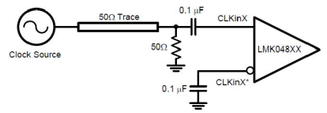


Figure 7-4. CLKinX/X* Single-ended Termination

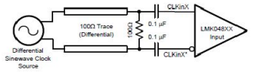
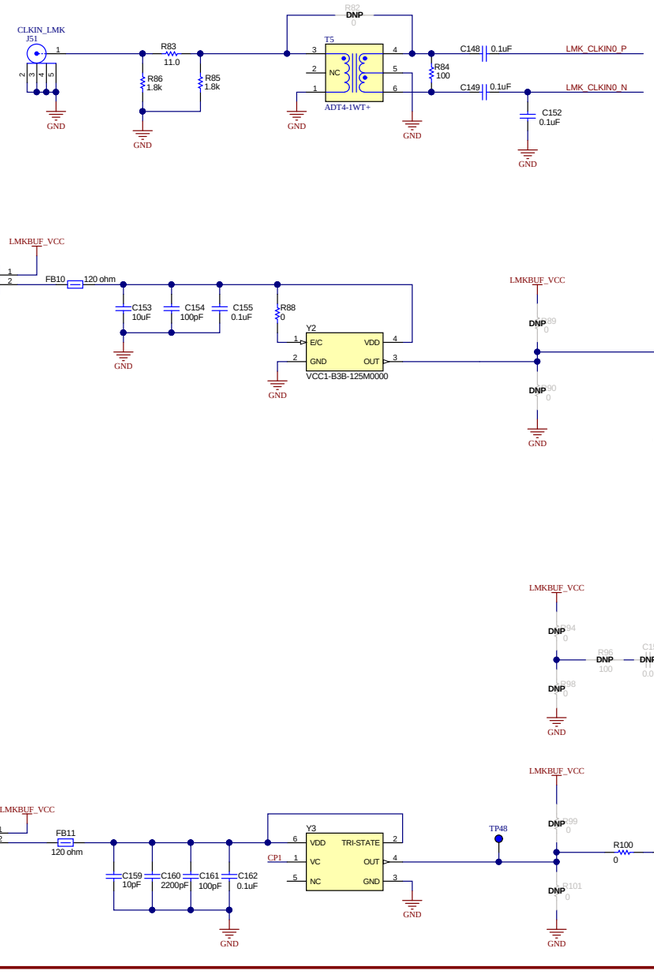
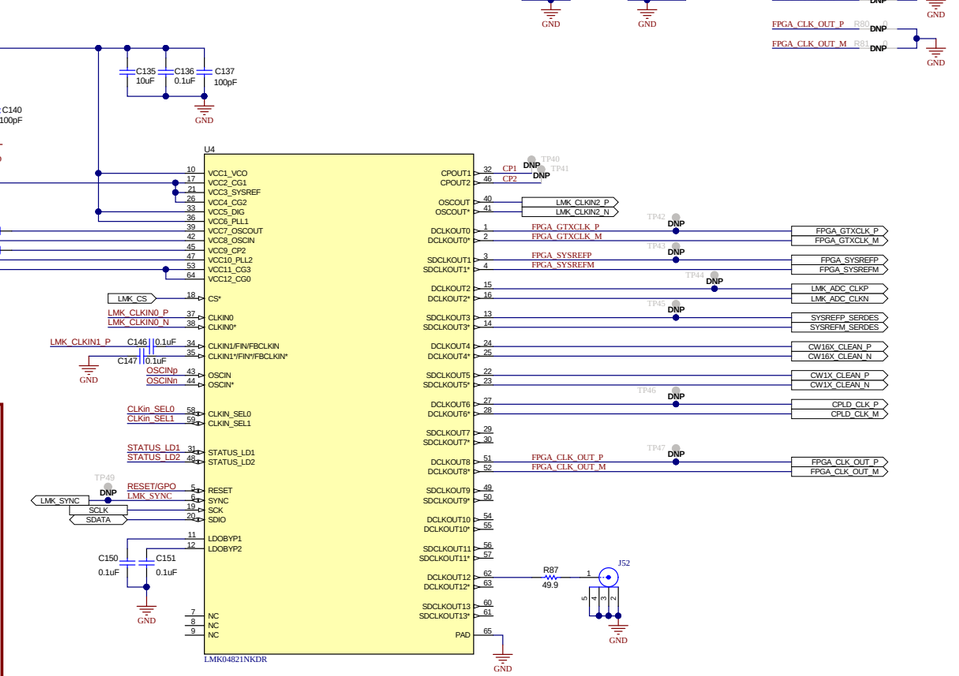
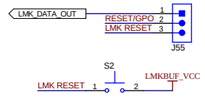


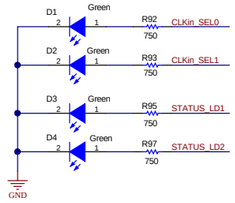
Figure 7-3. CLKinX/X* Termination for a Differential Sinewave Reference Clock Source

LMK Input Clock Sources









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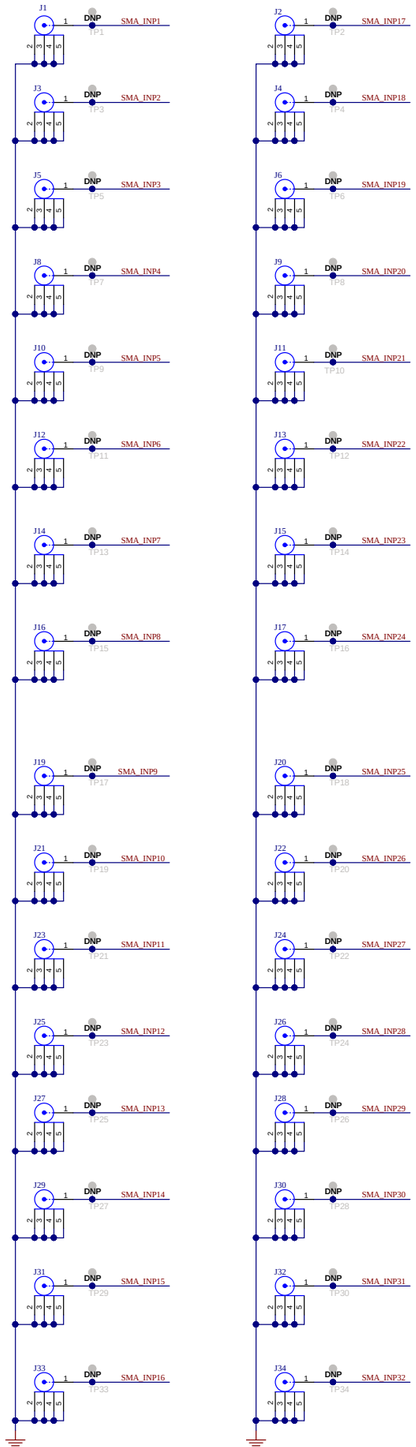
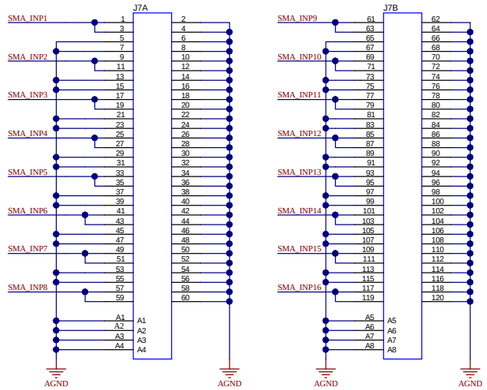
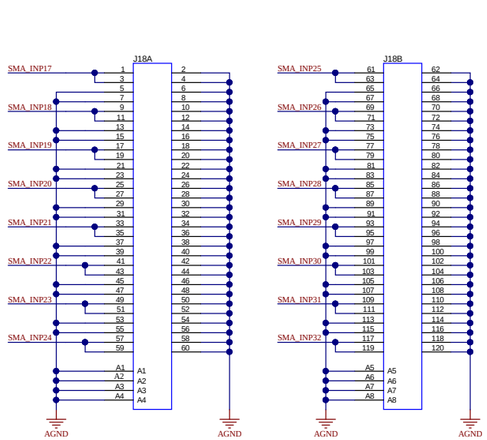
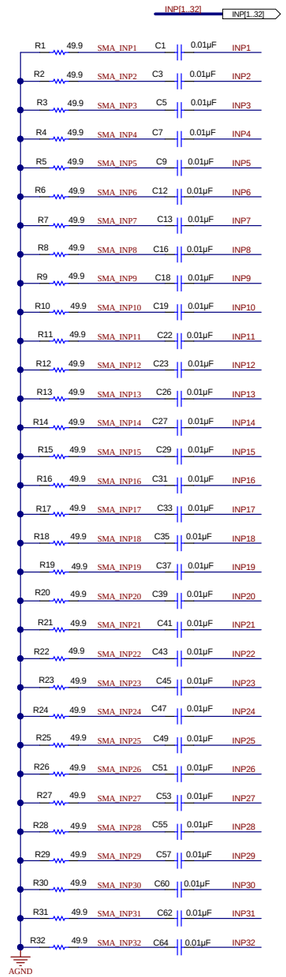
TID #: N/A		Project Title: AFE58JD32LP/AFE5832LP	
Number: DC075	Rev: B	Sheet Title: LMK CLOCK CIRCUIT	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 4 of 13
Drawn By: Praveen Aroul		File: DC075B_LMK_CLOCK_CIRCUIT.SchDoc	Size: C
Engineer: Praveen Aroul		Contact: http://www.ti.com/support	http://www.ti.com

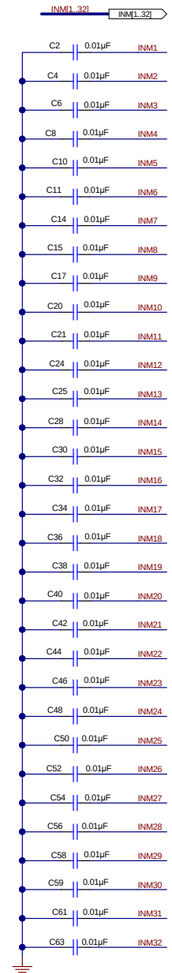
ANALOG INPUTS











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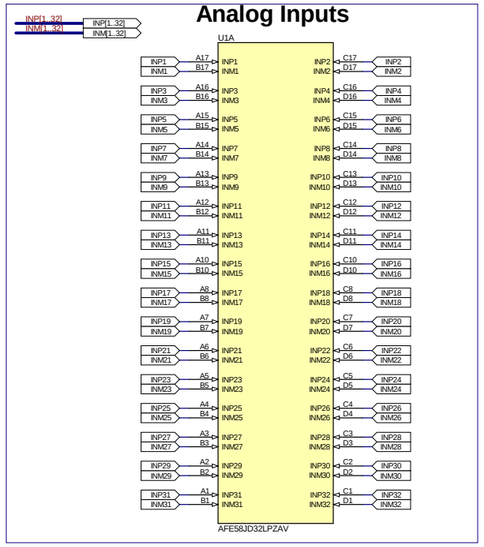
Number: DC075	Rev: B	Sheet Title: ANALOG INPUTS	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 5 of 13
Drawn By: Praveen Aroul		File: DC075B_ANALOG_INPUTS.SchDoc	Size: C
Engineer: Praveen Aroul		Contact: http://www.ti.com/support	http://www.ti.com

Device Pin configuration

Analog Inputs



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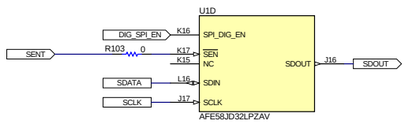
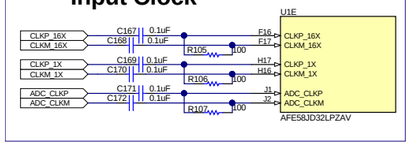
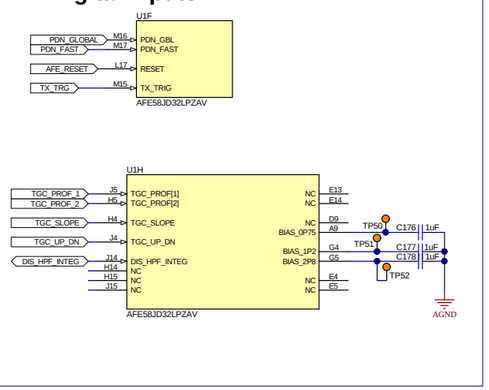


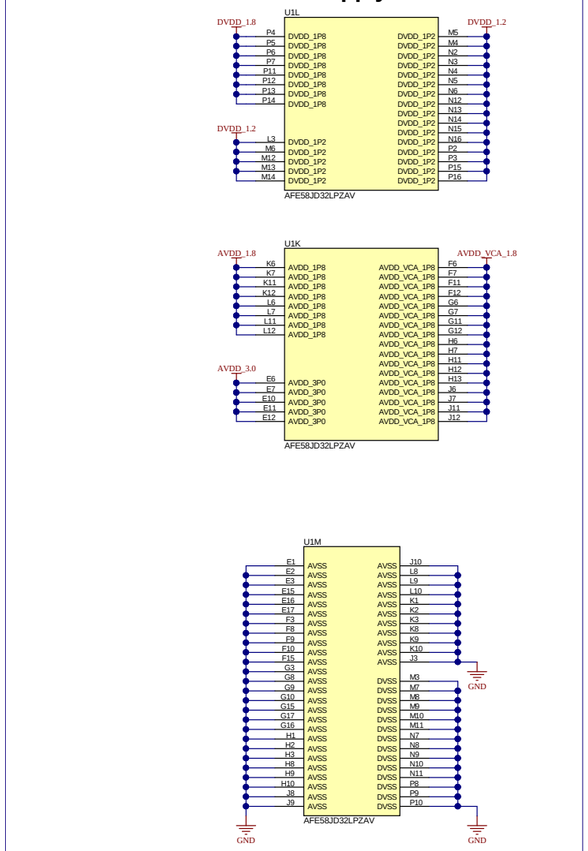
Input Clock



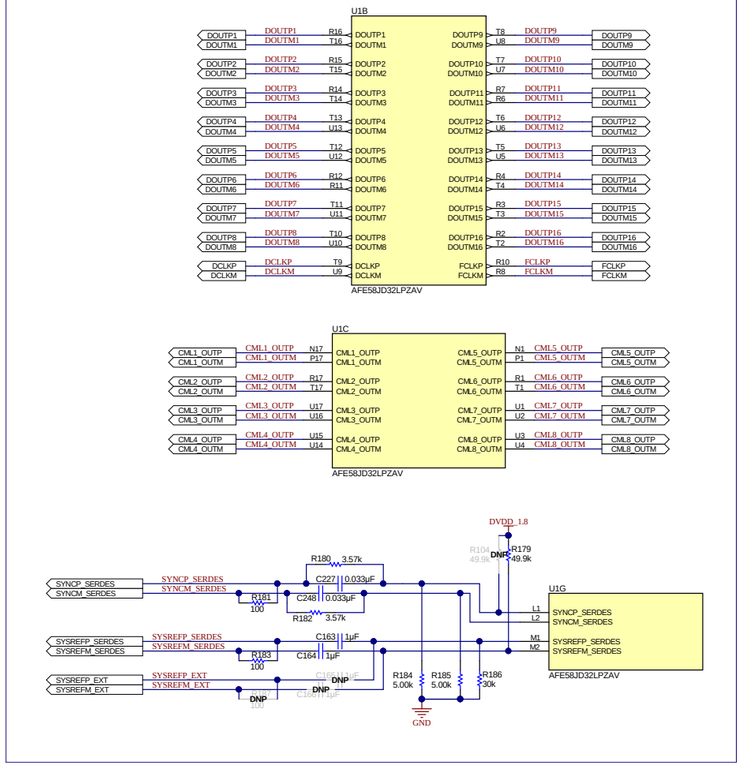
Digital Inputs



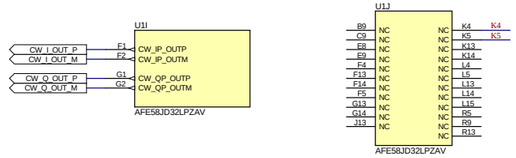
Power Supply



LVDS/JESD Output



CW Output



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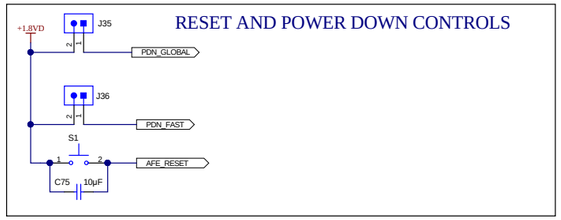
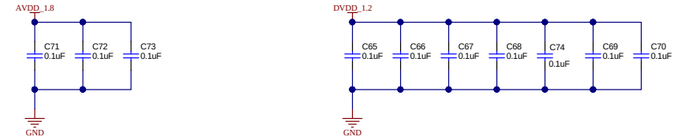
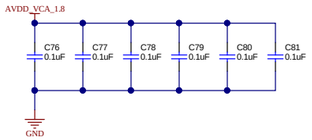
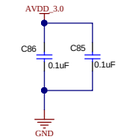
Drawn By: Praveen Aroul		File: DC075B_DEVICE_PINOUT.SchDoc	Size: C
Engineer: Praveen Aroul		Contact: http://www.ti.com/support	http://www.ti.com

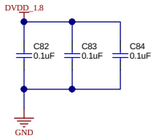
RESET AND POWER DOWN CONTROLS

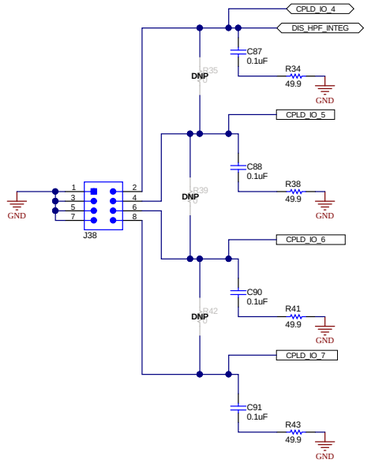












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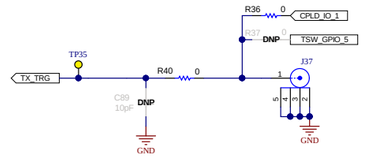

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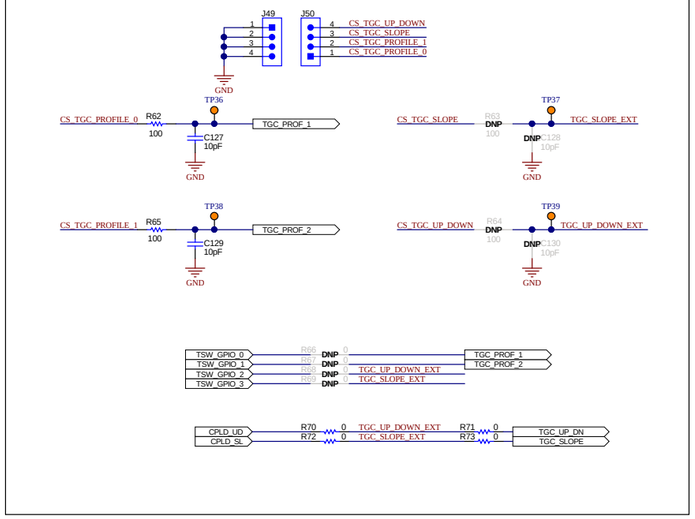
DTGC

DTGC CONTROL SIGNALS



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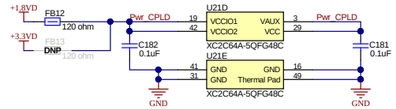
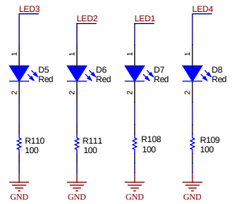
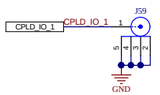
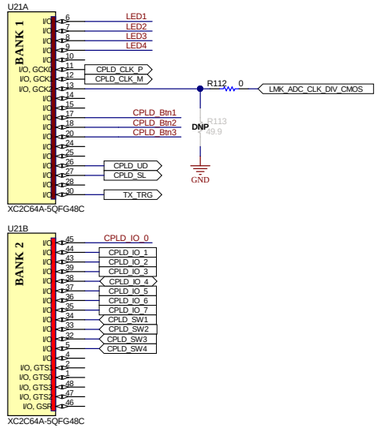
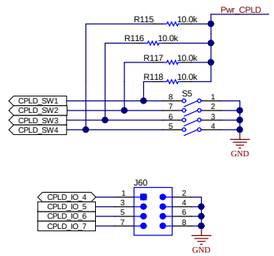
DTGC CPLD

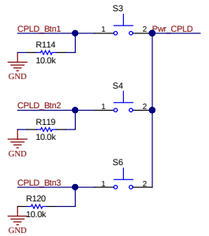












Orderable: AFE58JD32LPEVM		Designed for: Public Release	Mod. Date: 12/15/2018
TID #: N/A		Project Title: AFE58JD32LP/AFE5832LP	
Number: DC075	Rev: B	Sheet Title: DTGC CPLD	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 9 of 13
Drawn By: Praveen Aroul		File: DC075B_DTGC_CPLD.SchDoc	Size: C
Engineer: Praveen Aroul		Contact: http://www.ti.com/support	

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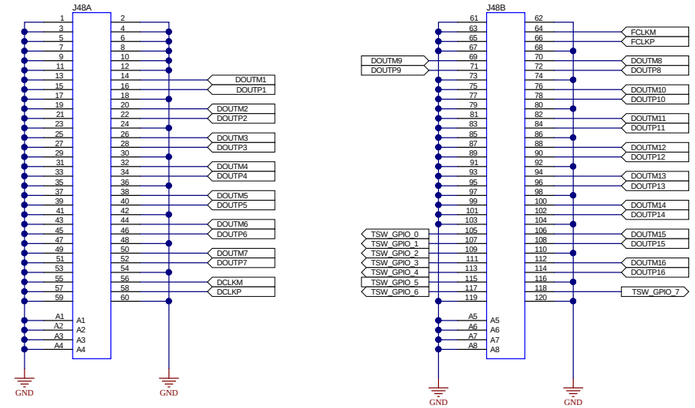
ADC LVDS OUTPUT



Orderable: AFE58JD32LPEVM		Designed for: Public Release	Mod. Date: 11/9/2018
TID #: N/A		Project Title: AFE58JD32LP/AFE5832LP	
Number: DC075	Rev: B	Sheet Title: LVDS OUTPUT	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 10 of 13
Drawn By: Praveen Aroul		File: DC075B_LVDS_OUTPUT.SchDoc	Size: C
Engineer: Praveen Aroul		Contact: http://www.ti.com/support	

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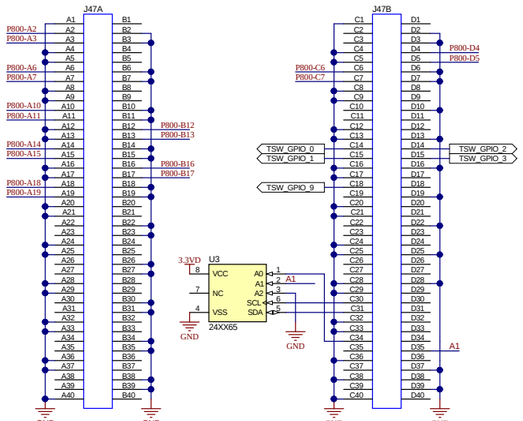
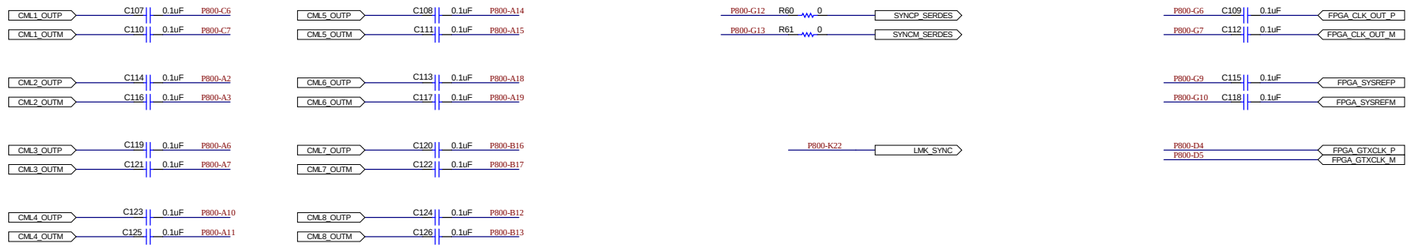
ADC SERDES (JESD204b) Output

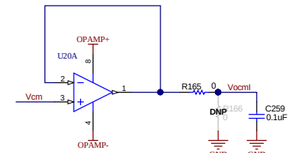


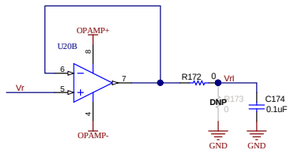


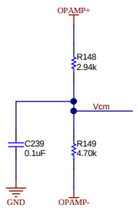
Orderable: AFE58JD32LPEVM		Designed for: Public Release	Mod. Date: 11/9/2018
TID #: N/A		Project Title: AFE58JD32LP/AFE5832LP	
Number: DC075	Rev: B	Sheet Title: JESD OUTPUT	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 11 of 13
Drawn By: Praveen Aroul		File: DC075B_JESD_OUTPUT.SchDoc	Size: C
Engineer: Praveen Aroul		Contact: http://www.ti.com/support	http://www.ti.com

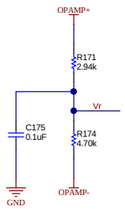
CW I/V OUTPUT

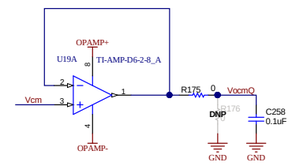
Layout of I/Q channels should be symmetric (mirror matching)
Match tolerance of components in the I/Q path. R=0.1%, C=5%

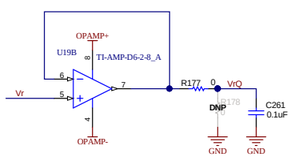


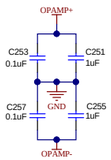


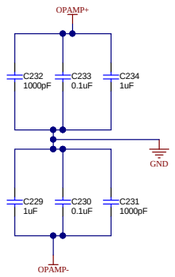


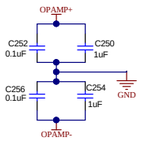


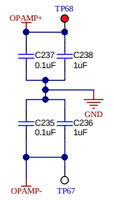


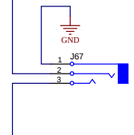


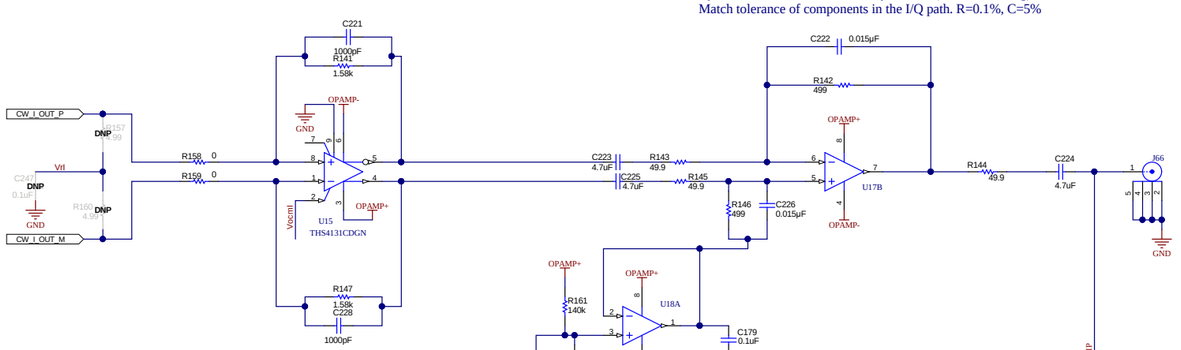


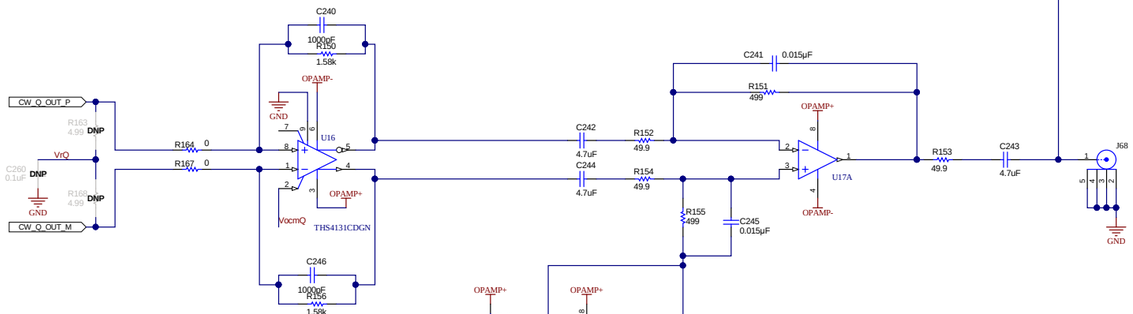












Orderable: AFE58JD32LPEVM		Designed for: Public Release	Mod. Date: 12/15/2018
TID #: N/A		Project Title: AFE58JD32LP/AFE5832LP	
Number: DC075	Rev: B	Sheet Title: CW_OUTPUTS	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 12 of 13
Drawn By: Praveen Aroul		File: DC075B_CW_OUTPUTS.SchDoc	Size: C
Engineer: Praveen Aroul		Contact: http://www.ti.com/support	

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MECHANICAL PARTS

Keystone 2203 for LVDS.

PMSSS 440 0025 PH | Keystone 2203 | Keystone 8402 for JESD Capture Card

PCB Number: DC075
PCB Rev: A
!PCB

H4
MECH
MechPart

CE Mark

LBL1
PCB Label
Label

PCB
LOGO
Texas Instruments

PCB
LOGO
WEEE logo

PCB
LOGO
FCC disclaimer

Label Table	
Variant	Label Text
001	AFE58JD32LPEVM
002	AFE5832LPEVM

H3 H7 H10 H11 H14

H1 H5 H8 H13 H16

H2 H6 H9 H12 H15

DNP FID1 | DNP FID2 | DNP FID3 | DNP FID4 | DNP FID5 | DNP FID6

SH-1 Place SH-1 on J53

SH-2 Place SH-2 on J55 pins 2-3

SH-3 Place SH-3 on J54 pins 1-2

SH-4 Place SH-4 on J57

SH-5 Place SH-5 on J40 pins 3-5

SH-6 Place SH-6 on J40 pins 4-6

SH-7 Place SH-7 on J42 pins 1-3

SH-8 Place SH-8 on J42 pins 2-4

SH-9 Place SH-9 on J44 pins 3-5

SH-10 Place SH-10 on J44 pins 4-6

SH-11 Place SH-11 on J45 pins 3-5

SH-12 Place SH-12 on J45 pins 4-6

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5
Assembly Note
Indication for all LEDs has been marked with their cathode side.

Orderable: AFE58JD32LPEVM		Designed for: Public Release	Mod. Date: 11/9/2018
TID #: N/A		Project Title: AFE58JD32LP/AFE5832LP	
Number: DC075	Rev: B	Sheet Title: HARDWARE	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 13 of 13
Drawn By: Praveen Aroul		File: DC075B_HARDWARE.SchDoc	Size: C
Engineer: Praveen Aroul		Contact: http://www.ti.com/support	

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