TX7364 3-Level, 64-Channel Transmitter with On-Chip Beamformer, T/R Switch

1 Features

- Transmitter supports:
  - 64-channel 3-level pulser and active transmit/receive (T/R) switch
- 3-level pulser:
  - Maximum output voltage: ±100V
  - Minimum output voltage: ±1V
  - Maximum output current: 1A
  - True return to zero to discharge output to ground
  - Second harmonic of –40dBc at 5MHz
  - –3-dB Bandwidth with 400Ω || 125pF load
    - 22MHz for a ±100-V supply
  - Very low receive power: 0.1 mW/ch
- Active transmit/receive (T/R) switch with:
  - Turn on resistance of 26Ω
  - Turn on and Turn off time: 100ns
  - Transient glitch: $10mV_{PP}$
- On-chip beam former with:
  - Channel based T/R switch on and off controls
  - Delay resolution: half beamformer clock period, minimum 2.5ns
  - Maximum delay: 2^{14} beamformer clock period
  - Maximum beamformer clockspeed: 200MHz
  - On-Chip RAM for pattern and delay profile
  - One 512 × 32 memory to store beam-former pattern and delay for a group of 4 channels
  - Global repeat feature present, enabling long duration patterns
- High-speed (400 MHz maximum), 2-lane LVDS serial programming interface.
  - Low programming time: ≈2.5 us for delay profile update
  - 32-bit Checksum to detect wrong SPI writes
- Supports CMOS serial programming interface (50 MHz maximum)
- High reliability features:
  - Internal temperature sensor and automatic thermal shutdown
  - No specific power sequencing requirement
  - Error flag register to detect faulty conditions
  - Integrated passives for the floating supplies and bias voltages
  - Small package: FC-BGA-196 (12 mm × 12 mm) with 0.8-mm pitch

2 Applications

- Ultrasound imaging system
- Piezoelectric driver
- In-probe ultrasound imaging

3 Description

TX7364 is a highly integrated, high-performance transmitter device for ultrasound imaging system. The device has total 64 pulser circuits, 64 transmit/receive switches (referred as T/R or TR switches) and supports on-chip beamformer (TxBF). The device also integrates on-chip floating power supplies that reduce the number of required high voltage power supplies.

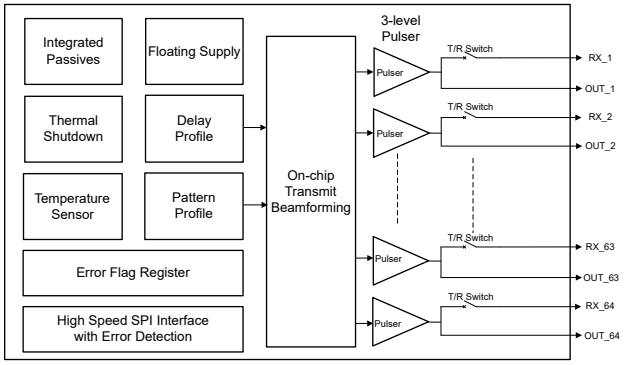
TX7364 has a pulser circuit that generates three-level high voltage pulses (up to ±100 V) that is used to excite multiple channels of an ultrasound transducer. The device supports total 64 outputs. The maximum output current is 1A.

Device can be used as a transmitter solution for many applications like ultrasound imaging, non-destructive testing, SONAR, LIDAR, marine navigation system, brain imaging systems and so on.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TX7364	FC-BGA-196	12.0 mm × 12.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

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4 Device Comparison

Table 4-1. Device Comparison

DEVICE NAME	DESCRIPTION
TX7332	Three-Level, 32-Ch Transmitter w/ Integrated Transmit Beamformer
TX7516	Five-Level, 16-Channel Transmitter with T/R Switch, and On-Chip Beamformer
TX75E16	5-Level, 16-Channel Transmitter with T/R Switch, On-Chip Beamformer, and Enhanced Load Damping Features

5 Pin Configuration and Functions

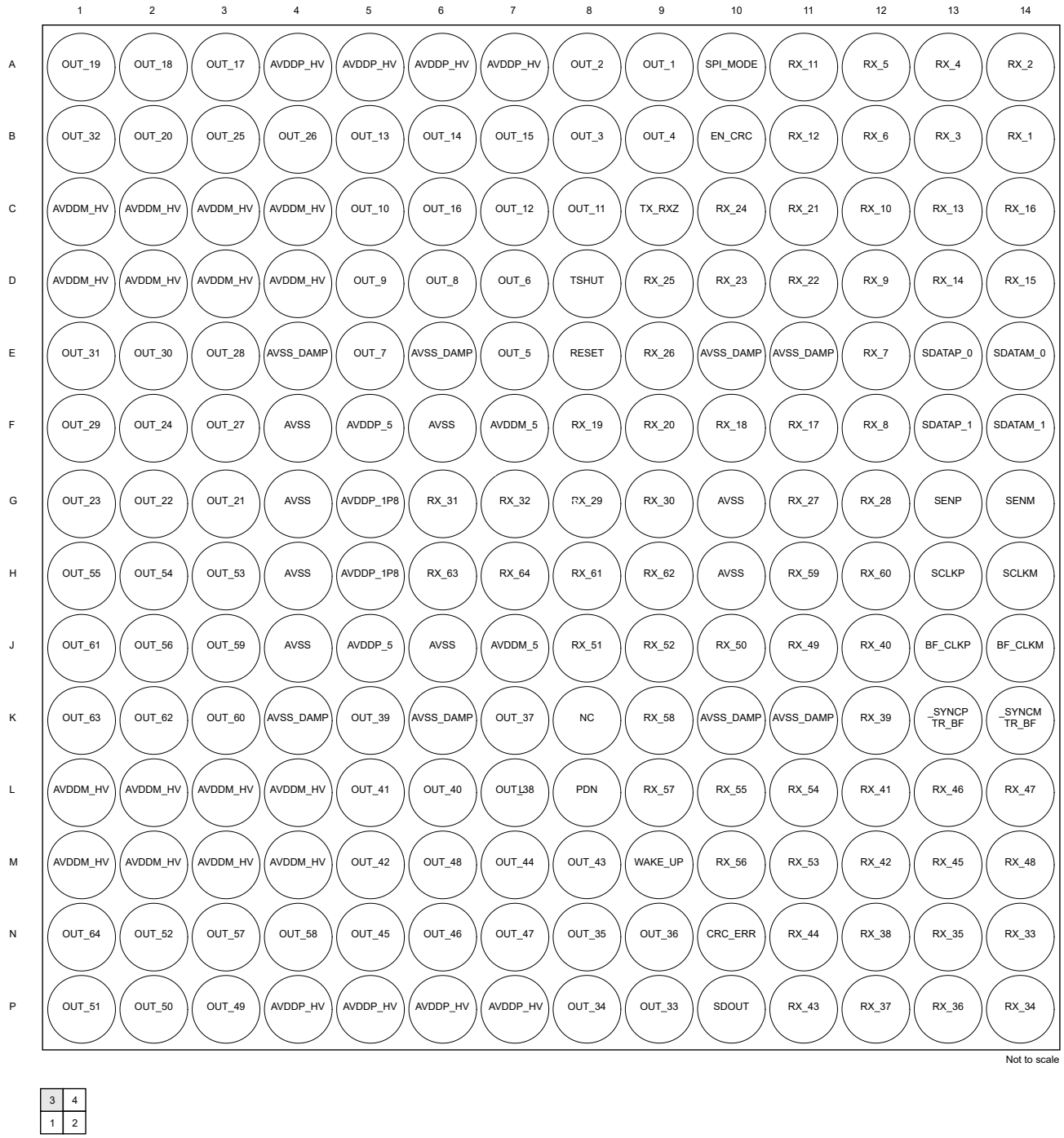


Figure 5-1. ACP Package, 196 Pin FC-BGA (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AVDDM_5	F7, J7	P	Low voltage negative supply pin, -5V

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AVDDM_HV	C1, C2, C3, C4, D1, D2, D3, D4, L1,L2, L3, L4, M1, M2,M3, M4	P	High voltage negative supply pin for pulser, for example -100V
AVDDP_5	F5, J5	P	Low voltage positive supply pin, 5V
AVDDP_1P8	G5, H5	P	Digital supply, 1.8V
AVDDP_HV	A4, A5, A6, A7, P4,P5, P6, P7	P	High voltage positive supply pin for pulser, for example 100V
AVSS	F4, F6, G4,G10, H4, H10, J4, J6	-	Ground pin
AVSS_DAMP	E4, E6, E10, E11, K4, K6, K10, K11	-	Return to zero ground pin. Short AVSS_DAMP to AVSS connection far from device as suggested in the application diagram.
BF_CLKM	J14	I	Differential clock input for the beam former clock, (negative) with internal 100Ω termination to the BF_CLKP pin. Internal termination resistor can be programmed using serial programming interface.
BF_CLKP	J13	I	Differential clock input for the beam former clock, (positive) with internal 100Ω termination to the BF_CLKM pin. Internal termination resistor can be programmed using serial programming interface.
EN_CRC	B10	I	Enable Cyclic Redundancy Check for the SPI. 1.8V logic level supported. Internal 18kΩ resistor to ground.
CRC_ERR	N10	O	Cyclic Redundancy Check error output pin. CRC_ERR pin is set to high-Z state in normal operation. In case of SPI error, CRC ERR pin is pulled high. 1.8V logic level supported. CRC_ERR output pin of multiple TX7364 devices can be shorted together. Connect common 1kΩ resistor and 1nF capacitor in parallel to ground.
NC	K8	-	No connection
OUT_1	A9	I/O	Transmitter output for channel 1
OUT_2	A8	I/O	Transmitter output for channel 2
OUT_3	B8	I/O	Transmitter output for channel 3
OUT_4	B9	I/O	Transmitter output for channel 4
OUT_5	E7	I/O	Transmitter output for channel 5
OUT_6	D7	I/O	Transmitter output for channel 6
OUT_7	E5	I/O	Transmitter output for channel 7
OUT_8	D6	I/O	Transmitter output for channel 8
OUT_9	D5	I/O	Transmitter output for channel 9
OUT_10	C5	I/O	Transmitter output for channel 10
OUT_11	C8	I/O	Transmitter output for channel 11
OUT_12	C7	I/O	Transmitter output for channel 12
OUT_13	B5	I/O	Transmitter output for channel 13
OUT_14	B6	I/O	Transmitter output for channel 14
OUT_15	B7	I/O	Transmitter output for channel 15

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
OUT_16	C6	I/O	Transmitter output for channel 16
OUT_17	A3	I/O	Transmitter output for channel 17
OUT_18	A2	I/O	Transmitter output for channel 18
OUT_19	A1	I/O	Transmitter output for channel 19
OUT_20	B2	I/O	Transmitter output for channel 20
OUT_21	G3	I/O	Transmitter output for channel 21
OUT_22	G2	I/O	Transmitter output for channel 22
OUT_23	G1	I/O	Transmitter output for channel 23
OUT_24	F2	I/O	Transmitter output for channel 24
OUT_25	B3	I/O	Transmitter output for channel 25
OUT_26	B4	I/O	Transmitter output for channel 26
OUT_27	F3	I/O	Transmitter output for channel 27
OUT_28	E3	I/O	Transmitter output for channel 28
OUT_29	F1	I/O	Transmitter output for channel 29
OUT_30	E2	I/O	Transmitter output for channel 30
OUT_31	E1	I/O	Transmitter output for channel 31
OUT_32	B1	I/O	Transmitter output for channel 32
OUT_33	P9	I/O	Transmitter output for channel 33
OUT_34	P8	I/O	Transmitter output for channel 34
OUT_35	N8	I/O	Transmitter output for channel 35
OUT_36	N9	I/O	Transmitter output for channel 36
OUT_37	K7	I/O	Transmitter output for channel 37
OUT_38	L7	I/O	Transmitter output for channel 38
OUT_39	K5	I/O	Transmitter output for channel 39
OUT_40	L6	I/O	Transmitter output for channel 40
OUT_41	L5	I/O	Transmitter output for channel 41
OUT_42	M5	I/O	Transmitter output for channel 42
OUT_43	M8	I/O	Transmitter output for channel 43
OUT_44	M7	I/O	Transmitter output for channel 44
OUT_45	N5	I/O	Transmitter output for channel 45
OUT_46	N6	I/O	Transmitter output for channel 46
OUT_47	N7	I/O	Transmitter output for channel 47
OUT_48	M6	I/O	Transmitter output for channel 48
OUT_49	P3	I/O	Transmitter output for channel 49
OUT_50	P2	I/O	Transmitter output for channel 50
OUT_51	P1	I/O	Transmitter output for channel 51
OUT_52	N2	I/O	Transmitter output for channel 52
OUT_53	H3	I/O	Transmitter output for channel 53
OUT_54	H2	I/O	Transmitter output for channel 54
OUT_55	H1	I/O	Transmitter output for channel 55
OUT_56	J2	I/O	Transmitter output for channel 56
OUT_57	N3	I/O	Transmitter output for channel 57
OUT_58	N4	I/O	Transmitter output for channel 58
OUT_59	J3	I/O	Transmitter output for channel 59

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
OUT_60	K3	I/O	Transmitter output for channel 60
OUT_61	J1	I/O	Transmitter output for channel 61
OUT_62	K2	I/O	Transmitter output for channel 62
OUT_63	K1	I/O	Transmitter output for channel 63
OUT_64	N1	I/O	Transmitter output for channel 64
RESET	E8	I	Hardware reset (Active high logic). 1.8V logic level supported. Internal 18kΩ resistor to ground.
RX1	B14	O	Channel 1 T/R switch low voltage side output, connect to input of receiver
RX2	A14	O	Channel 2 T/R switch low voltage side output, connect to input of receiver
RX3	B13	O	Channel 3 T/R switch low voltage side output, connect to input of receiver
RX4	A13	O	Channel 4 T/R switch low voltage side output, connect to input of receiver
RX5	A12	O	Channel 5 T/R switch low voltage side output, connect to input of receiver
RX6	B12	O	Channel 6 T/R switch low voltage side output, connect to input of receiver
RX7	E12	O	Channel 7 T/R switch low voltage side output, connect to input of receiver
RX8	F12	O	Channel 8 T/R switch low voltage side output, connect to input of receiver
RX9	D12	O	Channel 9 T/R switch low voltage side output, connect to input of receiver
RX10	C12	O	Channel 10 T/R switch low voltage side output, connect to input of receiver
RX11	A11	O	Channel 11 T/R switch low voltage side output, connect to input of receiver
RX12	B11	O	Channel 12 T/R switch low voltage side output, connect to input of receiver
RX13	C13	O	Channel 13 T/R switch low voltage side output, connect to input of receiver
RX14	D13	O	Channel 14 T/R switch low voltage side output, connect to input of receiver
RX15	D14	O	Channel 15 T/R switch low voltage side output, connect to input of receiver
RX16	C14	O	Channel 16 T/R switch low voltage side output, connect to input of receiver
RX17	F11	O	Channel 17 T/R switch low voltage side output, connect to input of receiver
RX18	F10	O	Channel 18 T/R switch low voltage side output, connect to input of receiver
RX19	F8	O	Channel 19 T/R switch low voltage side output, connect to input of receiver
RX20	F9	O	Channel 20 T/R switch low voltage side output, connect to input of receiver
RX21	C11	O	Channel 21 T/R switch low voltage side output, connect to input of receiver
RX22	D11	O	Channel 22 T/R switch low voltage side output, connect to input of receiver
RX23	D10	O	Channel 23 T/R switch low voltage side output, connect to input of receiver
RX24	C10	O	Channel 24 T/R switch low voltage side output, connect to input of receiver
RX25	D9	O	Channel 25 T/R switch low voltage side output, connect to input of receiver
RX26	E9	O	Channel 26 T/R switch low voltage side output, connect to input of receiver
RX27	G11	O	Channel 27 T/R switch low voltage side output, connect to input of receiver
RX28	G12	O	Channel 28 T/R switch low voltage side output, connect to input of receiver
RX29	G8	O	Channel 29 T/R switch low voltage side output, connect to input of receiver
RX30	G9	O	Channel 30 T/R switch low voltage side output, connect to input of receiver
RX31	G6	O	Channel 31 T/R switch low voltage side output, connect to input of receiver
RX32	G7	O	Channel 32 T/R switch low voltage side output, connect to input of receiver
RX33	N14	O	Channel 33 T/R switch low voltage side output, connect to input of receiver
RX34	P14	O	Channel 34 T/R switch low voltage side output, connect to input of receiver
RX35	N13	O	Channel 35 T/R switch low voltage side output, connect to input of receiver
RX36	P13	O	Channel 36 T/R switch low voltage side output, connect to input of receiver
RX37	P12	O	Channel 37 T/R switch low voltage side output, connect to input of receiver

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
RX38	N12	O	Channel 38 T/R switch low voltage side output, connect to input of receiver
RX39	K12	O	Channel 39 T/R switch low voltage side output, connect to input of receiver
RX40	J12	O	Channel 40 T/R switch low voltage side output, connect to input of receiver
RX41	L12	O	Channel 41 T/R switch low voltage side output, connect to input of receiver
RX42	M12	O	Channel 42 T/R switch low voltage side output, connect to input of receiver
RX43	P11	O	Channel 43 T/R switch low voltage side output, connect to input of receiver
RX44	N11	O	Channel 44 T/R switch low voltage side output, connect to input of receiver
RX45	M13	O	Channel 45 T/R switch low voltage side output, connect to input of receiver
RX46	L13	O	Channel 46 T/R switch low voltage side output, connect to input of receiver
RX47	L14	O	Channel 47 T/R switch low voltage side output, connect to input of receiver
RX48	M14	O	Channel 48 T/R switch low voltage side output, connect to input of receiver
RX49	J11	O	Channel 49 T/R switch low voltage side output, connect to input of receiver
RX50	J10	O	Channel 50 T/R switch low voltage side output, connect to input of receiver
RX51	J8	O	Channel 51 T/R switch low voltage side output, connect to input of receiver
RX52	J9	O	Channel 52 T/R switch low voltage side output, connect to input of receiver
RX53	M11	O	Channel 53 T/R switch low voltage side output, connect to input of receiver
RX54	L11	O	Channel 54 T/R switch low voltage side output, connect to input of receiver
RX55	L10	O	Channel 55 T/R switch low voltage side output, connect to input of receiver
RX56	M10	O	Channel 56 T/R switch low voltage side output, connect to input of receiver
RX57	L9	O	Channel 57 T/R switch low voltage side output, connect to input of receiver
RX58	K9	O	Channel 58 T/R switch low voltage side output, connect to input of receiver
RX59	H11	O	Channel 59 T/R switch low voltage side output, connect to input of receiver
RX60	H12	O	Channel 60 T/R switch low voltage side output, connect to input of receiver
RX61	H8	O	Channel 61 T/R switch low voltage side output, connect to input of receiver
RX62	H9	O	Channel 62 T/R switch low voltage side output, connect to input of receiver
RX63	H6	O	Channel 63 T/R switch low voltage side output, connect to input of receiver
RX64	H7	O	Channel 64 T/R switch low voltage side output, connect to input of receiver
SCLKM	H14	I	For LVDS SPI mode, differential high-speed clock input for the SPI, (negative) with internal 400Ω termination to the SCLKP pin. For CMOS SPI mode, connect SCLKM pin to ground.
SCLKP	H13	I	ForLVDS SPI mode, differential high-speed clock input for the SPI, (positive) with internal 400Ω termination to the SCLKM pin. For CMOS SPI mode, high speed clock input for SPI. 1.8V logic level supported. It has internal 10kΩ pull down resistor.
SDATAM_0	E14	I	For LVDS SPI mode, differential high-speed data input pair 0 for the SPI, (negative) with internal 400Ω termination to the SDATAP_0 pin. In CMOS SPI mode, connect SDATAM_0 pin to ground.
SDATAM_1	F14	I	For LVDS SPI mode, differential high-speed data input pair 1 for the SPI, (negative) with internal 400Ω termination to the SDATAP_1 pin. When SDATAM_1 is not used, connect 10kΩ resistor to AVDDP_1P8 supply. For CMOS SPI mode, connect SDATAM_1 pin to ground.
SDATAP_0	E13	I	For LVDS SPI mode, differential high-speed data input pair 0 for the SPI, (positive) with internal 400Ω termination to the SDATAM_0 pin. For CMOS SPI mode, data input 0 for SPI. 1.8V logic level supported. It has internal 10kΩ pull down resistor.
SDATAP_1	F13	I	For LVDS SPI mode, differential high-speed data input pair 1 for the SPI, (positive) with internal 400Ω termination to the SDATAM_1 pin. For CMOS SPI mode, datainput 1 for SPI. 1.8V logic level supported. It has internal 10kΩ pull down resistor. When not in use, connect 10kΩ resistor to ground.

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
SDOUT	P10	O	SPI data output pin. This has a 100kΩ pull down resistor. 1.8V logic level supported.SDOUT is in high-z state when not active hence SDOUT pin of multiple devices can be shorted together.
SENM	G14	I	For LVDS SPI mode, differential high speed enable input pair for the SPI, (negative)with internal 400Ω termination to the SENP pin. For CMOS SPI mode, connect SENM pin to ground.
SENP	G13	I	For LVDS SPI mode, differential high speed enable input pair for the SPI, (positive) with internal 400Ω termination to the SENM pin. For CMOS SPI mode, enable inputfor SPI. It has internal 10kΩ pull down resistor. 1.8V logic level supported.
TSHUT	D8	O	This pin functions as thermal shutdown flag active high output. In normal operation TSHUT pin is high-Z state. When this pin is set to high, it indicates that the device is in power down mode because of some error in device operation. Read error flag register to identify the reason behind the device shutdown. 1.8V logic is supported. Connect 1kΩ resistor and 1nF capacitor in parallel to ground. TSHUT pin of multiple devices can be shorted together.
SPI_MODE	A10	I	SPI mode selection pin. Connect to logic level '1' for CMOS mode and to '0' for LVDS mode. This pin has internal 18kΩ pull down resistor. 1.8V logic is supported.
TR_BF_SYNCM	K14	I	Differential input (negative) for the synchronization of the on-chip beamformer operation, with internal 100Ω termination to the TR_BF_SYNCP pin. Internal termination resistor can be programmed using serial programming interface.
TR_BF_SYNCP	K13	I	Differential input (positive) for the synchronization of the on-chip beamformer operation, with internal 100Ω termination to the TR_BF_SYNCM pin. Internal termination resistor can be programmed using serial programming interface.
TX_RXZ	C9	O	Specifies whether the device is in transmit mode (Even if one channel is transmitting) or in receive mode (All channels are in receive mode that is T/R switch of all the channels are ON). Output of this pin can be used to disable the HPF in ultrasound receiver front end. When device is in transmit mode, TX_RXZ is pulled high and when device is in receive mode,TX_RXZ pin is set to high-Z state. In CW mode, TX_RXZ pin is permanently pulled to high. 1.8V logic supported. Connect 1kΩ resistor and 1-nFcapacitor in parallel to ground. TX_RXZ pin of multiple devices can be shorted together.
WAKE_UP	M9	I	Active high wake up signal to power up the floating LDOs in the device. This pin has internal 18kΩ pull down resistor. 1.8V logic is supported.
PDN	L8	I	Active high signal to place the device in a PDN Mode. This pin has internal 18kΩ pull down resistor. 1.8V logic is supported.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

Table 5-2. Pin Name to Signal Name Map

SIGNAL NUMBER	PIN NAME	SIGNAL NAME
1	AVDDP_1P8	Digitaland I/O Supply
2	AVDDP_HV, AVDDM_HV	HV Supply
4	BF_CLKP –BF_CLKM	BF_CLK
5	TR_BF_SYNCP - TR_BF_SYNCM	TR_BF_SYNC
6	SCLKP - SCLKM	SCLK
7	SENP - SENM	SEN
8	SDATAP_0 - SDATAM_0	SDATA_0
9	SDATAP_1 - SDATAM_1	SDATA_1

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	AVDDP_1P8	-0.3	2	V
	AVDDM_5	-5.5	0.3	V
	AVDDP_5	-0.3	5.5	V
	AVDDM_HV	-105	0.3	V
	AVDDP_HV	-0.3	105	V
Voltage at low voltage pins	All the pins except supply and OUT* pins.	-0.3	2	V
Storage temperature, T_{stg}	Maximum junction temperature (T_J), any condition		125	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		TX7364 ACP (FC-BGA) 196	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	18.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.95	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.13	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report..

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
SUPPLIES						
V_{P_1P8}	AVDDP_1P8		1.7	1.8	1.9	V
V_{M_5}	AVDDM_5		-5.25	-5	-4.75	V
V_{P_5}	AVDDP_5		4.9	5	5.4	V
V_{MHV}	AVDDM_HV		-100		-1.5	V
V_{PHV}	AVDDP_HV		1.5		100	V
TEMPERATURE						
T_A	Ambient temperature		0		70	°C
BIAS VOLTAGES (1)						
	Common-mode voltage	BF_CLKM, BF_CLKP		1.2		V

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
BF_CLK INPUT						
f_{BF_CLK}	BF_CLK frequency	Minimum BF_CLK frequency		10		MHz
		Maximum BF_CLK frequency		200		MHz
V_{DE_BF}	Differential clock amplitude	Sine-wave, ac-coupled	0.7			V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
D_{BF}	Minimum BF_CLK duty cycle			45		%
	Maximum BF_CLK duty cycle			55		%
R_{CLK_TERM}	BF_CLK buffer termination	Minimum value		85		Ω
		Maximum value		115		Ω
TR_BF_SYNC INPUT						
f_{SYNC}	Maximum TR_BF_SYNC frequency (2)			1		MHz
V_{CM_SYNC}	Input common mode		1.125		1.375	V
V_{DE_SYNC}	Differential amplitude	LVPECL, dc-coupled		1.6		V_{PP}
		LVDS, dc-coupled		0.7		V_{PP}
w_{SYNC}	Minimum TR_BF_SYNC pulse width			16		DIG_CLK (3) clock cycles
	Maximum TR_BF_SYNC pulse width (4)			30		DIG_CLK (3) clock cycles
R_{SYNC_TERM}	TR_BF_SYNC buffer termination	Minimum value		85		Ω
		Maximum value		115		Ω

(1) Internally set by the device.
(2) For high voltage and high power scenario the device can enter thermal shutdown before reaching to maximum TR_BF_SYNC frequency. For normal operation, apply next TR_BF_SYNC pulse after all the channels completes the transmit and enters in the receive mode.
(3) DIG_CLK signal is derived from BF_CLK clock signal. The frequency of DIG_CLK clock is given by BF_CLK frequency divide by 2^(BF_CLK_DIV), where BF_CLK_DIV is a two bit register which can be programmed from 0 to 3. To enable the clock division feature, set BF_CLK_DIV_EN bit to '1'
(4) If TR_BF_SYNC is kept high continuously then device internal blocks doesn't shutdown during receive mode. To avoid such scenario the maximum pulse width of TR_BF_SYNC signal is limited to 30 DIG_CLK clock cycles

6.5 Electrical Characteristics

Typical/Min/Max values are at 25°C. **Device supplies:** AVDDP_1P8 = 1.8 V, AVDDP_5 = 5 V, AVDDM_5V = -5 V, AVDDP_HV = 100 V, AVDDM_HV = –100 V. **Device input:** BF_CLK = 200MHz, TR_BF_SYNC = 5kHz applied with differential mode. **Load:** Connected to the pulser output is 400Ω||125pF, and to T/R switch low voltage output is 100Ω||20pF, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PULSER							
R_H	Output transistor ON resistance (1)				18		Ω
R_G	Clamp transistor ON resistance (1)				18		Ω
R_{INT}	Damp transistor ON resistance (1)				1200		Ω
C_{PAR}	Pulsar Output Parasitic Capacitance	When T/R switch is OFF	AVDDP_HV = 5V, AVDDM_HV = -5V		42		pF
			AVDDP_HV = 100V, AVDDM_HV = -100V		21.5		pF
		When T/R switch is ON			21		pF
V_{DIODE}	Knee voltage of diode used in pulser (1)	For 1mA current			0.75		V
I_{OSAT}	Output transistor saturation current				1		A
I_{CSAT}	Clamp transistor saturation current				0.75		A
t_{R_GP}	Pulser output rise time, ground to positive high	See Pulser Output Waveform			10.5		ns
t_{F_GM}	Pulser output fall time, ground to minus high	See Pulser Output Waveform			10.5		ns
t_{R_MP}	Pulser output rise time, minus high to positive high	See Pulser Output Waveform			23.7		ns
		At temperature 70C			26.7		ns
t_{F_PM}	Pulser output fall time, positive high to minus high.	See Pulser Output Waveform			23.7		ns
		At temperature 70C			26.7		ns
t_{R_MG}	Pulser output rise time, minus high to ground.	See Pulser Output Waveform			12		ns
t_{F_PG}	Pulser output fall time, positive high to ground.	See Pulser Output Waveform			12		ns
BW	Maximum Pulser BW Frequency at which output peak to peak amplitude reduces by 3dB	+/-100V supply, 1A mode			22		MHz
		+/-80V supply, 1A mode			25		
F_{CW}	Maximum CW signal frequency				7		MHz
$HD2_{PUL}$	Second harmonic distortion	At 5MHz, 5 cycles, measured using pulse inversion technique (2)			40		dBc
CT_{PUL}	Cross talk	With only single channel pulser excited with signal frequency = 5MHz			60		dBc
T/R SWITCH							
R_{ON}	On DC resistance	See Simplified Schematic of T/R Switch			26		Ω
R_{OFF}	Impedance at DC and at 1MHz	See Simplified Schematic of T/R Switch			1		MΩ
R_{SHORT}	Off short resistance	See Simplified Schematic of T/R Switch			50		Ω
C_{PDIS}	T/R switch disabled parasitic capacitance	Measure on the RX_n node			3.5		pF
T_{TON}	Turn -on time				100		ns
T_{TOFF}	Turn -off time				100		ns
V_{GON}	Turn -on, -off glitch voltage	**Normal Mode**; Without transmit or with return to zero duration after transmit set to minimum of 500 ns (Duration to stay in return to zero required to get mentioned performance is load and supply dependent)			10		mV_{PP}
		Low Glitch Mode; Without transmit or with return to zero duration after transmit set to minimum of 500 ns (Duration to stay in return to zero required to get mentioned performance is load and supply dependent)			4		mV_{PP}
V_{MAXRX}	Maximum linear signal amplitude	Measured at at Rx_n node			1		V_{PP}
BW_{TR}	Bandwidth	Measured by feeding the signal at the pulser output with 50Ω source impedance and measuring the voltage at RX_n node			>50		MHz

Typical/Min/Max values are at 25°C. **Device supplies:** AVDDP_1P8 = 1.8 V, AVDDP_5 = 5 V, AVDDM_5V = -5 V, AVDDP_HV = 100 V, AVDDM_HV = –100 V. **Device input:** BF_CLK = 200MHz, TR_BF_SYNC = 5kHz applied with differential mode. **Load:** Connected to the pulser output is 400Ω||125pF, and to T/R switch low voltage output is 100Ω||20pF, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$HD2_{TR}$	Second harmonic distortion	Till frequency <20 MHz, Signal is applied with source impedance of 50Ω at TX output OUT_n node and amplitude of 1Vpp is ensured at RX_n node			50		dBc
CT_{TR}	Cross talk	With only single channel T/R switch is excited with signal frequency = 5MHz			70		dBc
THERMAL SHUTDOWN							
T_{SHUT}	Shutdown Temperature	When TSHUT_TEMP is set to '0'			105		°C
		When TSHUT_TEMP is set to '1'			125		°C
T_{SHUT_DEL}	Shutdown Temperature Threshold Variation.	Shutdown threshold can vary by +/-T_{SHUT_DEL} .For both TSHUT_TEMP is set to '0' or '1'			10		°C
POWER SUPPLY REJECTION							
$PSRR_{PHV}$	AVDDP_HV power supply rejection	When T/R switch is On at 100kHz			83		dBc
$PSRR_{MHV}$	AVDDM_HV power supply rejection	When T/R switch is On at 100kHz			86		dBc
$PSRR_{LV5}$	AVDDP_5 or AVDDM_5 power supply rejection	When T/R switch is On at 100kHz			75		dBc
$PSRR_{LV}$	AVDDP_1P8 power supply rejection	When T/R switch is On at 100kHz			90		dBc
POWER DISSIPATION IN 3-LEVEL, TRANSMIT RECEIVE MODE[3]							
I_{PH}	AVDDP_HV supply current				13.1		mA
I_{MH}	AVDDM_HV supply current				10.8		mA
I_{ML_TR}	AVDDM_5 supply current				0.4		mA
I_{PL_TR}	AVDDP_5 supply current				0.63		mA
I_{1P8_B}	AVDDP_1P8 supply current				34		mA
P_{D_TR}	Total power dissipation				38.3		mW/ch
POWER DISSIPATION IN 3-LEVEL, CW-MODE[4]							
I_{PHV_CW}	AVDDP_HV supply current	HV supply = +/-5V	Pattern used is Return to Zero waveform		260		mA
			Pattern used is Non-Return to Zero waveform		396		mA
I_{PHV_CW}	AVDDP_HV supply current	HV supply = +/-4V	Pattern used is Return to Zero waveform		210		mA
			Pattern used is Non-Return to Zero waveform		316		mA
I_{MHV_CW}	AVDDM_HV supply current	HV supply = +/-5V	Pattern used is Return to Zero waveform		259		mA
			Pattern used is Non-Return to Zero waveform		394		mA
I_{MHV_CW}	AVDDM_HV supply current	HV supply = +/-4V	Pattern used is Return to Zero waveform		209		mA
			Pattern used is Non-Return to Zero waveform		314		mA
I_{ML_CW}	AVDDM_5 supply current	HV supply = +/-5V or +/-4V	Pattern used is Return to Zero waveform		92		mA
			Pattern used is Non-Return to Zero waveform		52		mA
I_{PL_CW}	AVDDP_5 supply current	HV supply = +/-5V or +/-4V	Pattern used is Return to Zero waveform		110		mA
			Pattern used is Non-Return to Zero waveform		50		mA
I_{1P8_CW}	AVDDP_1P8 supply current	HV supply = +/-5V or +/-4V	Pattern used is Return to Zero waveform		77		mA
			Pattern used is Non-Return to Zero waveform		90		mA

Typical/Min/Max values are at 25°C. **Device supplies:** AVDDP_1P8 = 1.8 V, AVDDP_5 = 5 V, AVDDM_5V = -5 V, AVDDP_HV = 100 V, AVDDM_HV = –100 V. **Device input:** BF_CLK = 200MHz, TR_BF_SYNC = 5kHz applied with differential mode. **Load:** Connected to the pulser output is 400Ω||125pF, and to T/R switch low voltage output is 100Ω||20pF, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_{D_CW}	Total power dissipation	HV supply = +/-5V	Pattern used is Return to Zero waveform		117		mW/ch
			Pattern used is Non-Return to Zero waveform		145		mW/ch
P_{D_CW}	Total power dissipation	HV supply = +/-4V	Pattern used is Return to Zero waveform		89		mW/ch
			Pattern used is Non-Return to Zero waveform		101		mW/ch
POWER DISSIPATION IN OTHER MODES							
P_{D_R}	Total power dissipation in receive only(5) or Global powerdown mode	PDN_GBL = 1			23.4		mW
P_{PDN}	Total power dissipation in receive only with SPI buffer powered down	PDN_GBL = 1 and EN_DYN_PDN_SPIBUF = 1			11		mW
Pfpd	Total power dissipation with TX, BF Clock & SPI buffers powered down	EN_CLK_GATE = 1 EN_DYN_PDN_CLKBUF = 1 PDN_GBL = 1 and EN_DYN_PDN_SPIBUF = 1			7.2		mW
t_{WUP_GBL}	Wake-up time	Global Power Down mode			200		µs

(1) Refer Pulser Block Diagram
(2) In pulse inversion technique, HD2 power (F2) is measured by looking at the FFT of sum of positive and negative polairty signal, fundamental power (F1) is measured by looking at the FFT of positive polarity signal. Then HD2 in dBc is given by = F1 - F2 + 6 (6dB is adjusted as in sum HD2 power gets doubled)
(3) Different supply voltages used to measure power are: AVDDP_5 = 5 V, AVDDM_5 = –5 V, AVDDP_HV = 100 V, AVDDM_HV = –100 V. To measure power, device is configured to generate patterns shown in Transmit receive mode output pattern on all the channels with 0 transmit delay beam forming.
(4) For CW-mode, value of all the supplies used to measure power are AVDDP_5 = +5V, AVDDM_5 = -5V, AVDDP_HV = +5V and AVDDM_HV = -5V.
All pulsers (32 channels) generate CW waveform. A Non-Return to Zero (NRZ) pattern refers to a +5V -> -5V -> +5V kind of wave and a Return to Zero (RZ) pattern refers to +5->0->-5->0 at a frequency of 5MHz. In RZ pattern, the 0V level is kept to 20 ns each for +5->0 and -5->0 transition.
(5) "Receive-only Mode": It means that in device T/R switches of all the channels are always On and none of the pulser transmit the high voltage pulses.

6.6 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. Typical values are at T_A = 25°C, minimum and maximum values are across the full temperature range. Supplies: AVDDP_1P8 = 1.8 V, AVDDP_5 = 5 V, AVDDM_5 V = –5 V, AVDDP_HV = 100 V, AVDDM_HV = –100 V (unless otherwise noted)

			MIN	TYP	MAX	UNIT
DIGITAL INPUTS (PDN, EN_CRC, RESET, {SCLKP, SDATAP_0/1, SENP in CMOS SPI mode}, SPI_MODE, WAKE_UP)(1)						
V_{IH1}	High-level input voltage		1.35			V
V_{IL1}	Low-level input voltage				0.45	V
I_{IH1}	High-level input current			100		µA
I_{IL1}	Low-level input current			100		µA
C_{i1}	Input capacitance			6		pF
DIGITAL INPUTS (SCLKP, SCLKM, SDATAM_0/1, SDATAP_0/1, SENP, SENM for SPI configured in LVDS mode)(1)						
V_{CM_SPI}	Input common mode		1		1.4	V
V_{DE_SPI}	Differential amplitude	LVDS, dc-coupled		0.7		V_{PP}
R_{SPI_TERM}	Differential termination	Minimum value		90		Ω
		Maximum value		130		Ω
DIGITAL OUTPUTS (CRC_ERR, SDOUT, TSHUT, TX_RXZ) (1)						
V_{OH}	High-level output voltage		1.44	1.8		V
V_{OL}	Low-level output voltage	Only applicable for SDOUT signal. For other pins CRC_ERR, TSHUT, and TX_RXZ active low state doesnt exist.		0	0.2	V
I_{OH}	High-level output current	Only applicable for pins CRC_ERR, TSHUT, and TX_RXZ.	20			mA
z_o	Output impedance for CRC_ERR, SDOUT, TX_RXZ, and TSHUT	When high		50		Ω
z_o	Output impedance for CRC_ERR, TX_RXZ, and TSHUT	When low		50		Ω
		When high Z state		50		kΩ

(1) All digital specifications are characterized across operating temperature range but are not tested at production.

6.7 Timing Requirements

Typical values are at T_A = 25°C, AVDDP_1P8 = 1.8= V, AVDDP_5 = 5 V, AVDDM_5V = –5 V, AVDDP_HV = 100 V, AVDDM_HV = –100 V (unless otherwise noted); minimum and maximum values are across the full temperature range. All timing specifications are characterized but are not tested at production.

			MIN	TYP	MAX	UNIT
SERIAL INTERFACE TIMING (LVDS MODE)						
t_{SCLK} (1)	SCLK period in write mode		2.5			ns
t_{SCLK_H} (1)	SCLK high time in write mode		1			ns
t_{SCLK_L} (1)	SCLK low time in write mode		1			ns
t_{DSU} (1)	Data setup time in write mode		0.75			ns
t_{DH} (1)	Data hold time in write mode		0.75			ns
t_{SEN_SU} (1)	SEN falling edge to SCLK rising edge in write mode		0.75			ns
t_{SEN_HO} (1)	Time between last SCLK rising edge to SEN rising edge in write mode		0.75			ns
t_{SCLK_RD} (2)	SCLK period in read mode		50			ns
$t_{SCLK\_H\_RD}$ (2)	SCLK high time in read mode		19			ns
$t_{SCLK\_L\_RD}$ (2)	SCLK low time in read mode		19			ns
t_{DSU_RD} (2)	Data setup time in read mode		4			ns
t_{DH_RD} (2)	Data hold time in read mode		4			ns
$t_{SEN\_SU\_RD}$ (2)	SEN falling edge to SCLK rising edge in read mode		4			ns
$t_{SEN\_HO\_RD}$ (2)	Time between last SCLK rising edge to SEN rising edge in read mode		4			ns
t_{OUT_DV} (2)	SDOUT delay in read mode		10			ns
SERIAL INTERFACE TIMING (CMOS MODE)						
t_{SCLK}	SCLK period in write mode		20			ns
t_{SCLK_H}	SCLK high time in write mode		9			ns
t_{SCLK_L}	SCLK low time in write mode		9			ns
t_{DSU}	Data setup time in write mode		2			ns
t_{DH}	Data hold time in write mode		2			ns
t_{SEN_SU}	SEN falling edge to SCLK rising edge in write mode		2			ns
t_{SEN_HO}	Time between last SCLK rising edge to SEN rising edge in write mode		2			ns
t_{SCLK_RD}	SCLK period in read mode		50			ns
$t_{SCLK\_H\_RD}$	SCLK high time in read mode		19			ns
$t_{SCLK\_L\_RD}$	SCLK low time in read mode		19			ns
t_{DSU_RD}	Data setup time in read mode		4			ns
t_{DH_RD}			4			ns
$t_{SEN\_SU\_RD}$	SEN falling edge to SCLK rising edge in read mode		4			ns
$t_{SEN\_HO\_RD}$	Time between last SCLK rising edge to SEN rising edge in read mode		4			ns
t_{OUT_DV}	SDOUT delay in read mode		8			ns
TIMING REQUIREMENT FOR TR_BF_SYNC and WAKE_UP SIGNALS						
t_{WUP} (3)	Minimum time to apply WAKE_UP signal before applying TR_BF_SYNC signal		2			µs
t_{SU_SYNC} (3)	Setup time related to TR_BF_SYNC (Differential) relative to the rising edge of the BF_CLK (Differential) clock		0.8			ns
t_{H_SYNC} (3)			0.8			ns
t_{PROP_VAR}	Minimum	Typical Skew variation across devices. Skew is defined as variation in time instant across channel to channel and device to device when high voltage output start making transition		-1		ns
	Maximum			1		ns
t_{PROP_INT}	Across device From a 50% transition point of BF_CLK rising edge on which TR_BF_SYNC is latched to 1-V deviation at output; see			15		ns

(1) See Serial Interface Timing for more details.
(2) See Serial Interface Register Read Operation for more details.
(3) See TR_BF_SYNC and WAKE_UP Timing requirement for more details.

6.8 Typical Characteristics

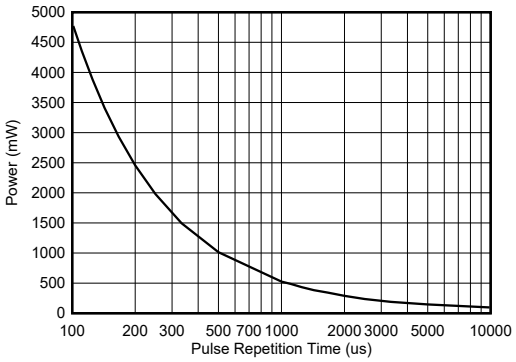


Figure 6-1. Power versus Pulse Repetition Time (PRT)

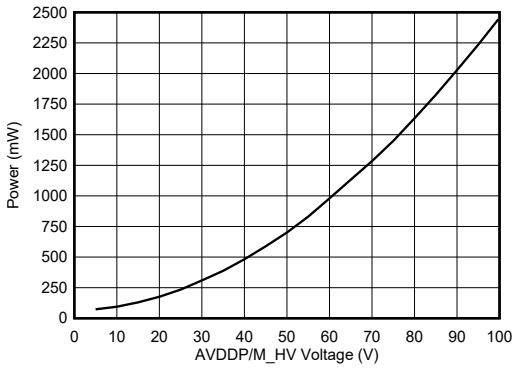


Figure 6-2. Power versus High Voltage Supply

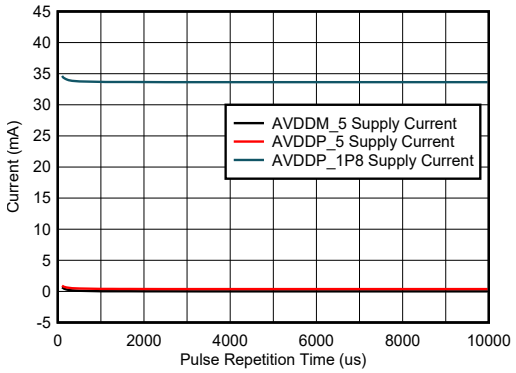


Figure 6-3. Low Voltage Supplies Current versus PRT

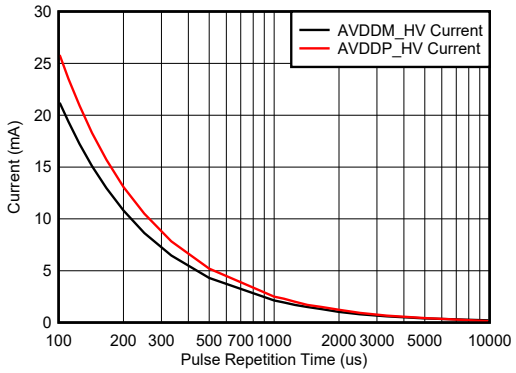


Figure 6-4. High Voltage Supplies Current versus PRT

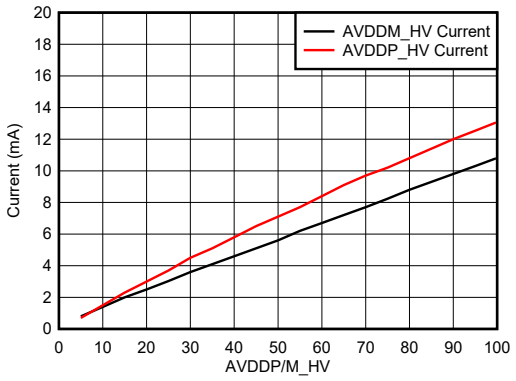


Figure 6-5. High Voltage Supplies Current versus High Voltage Supply

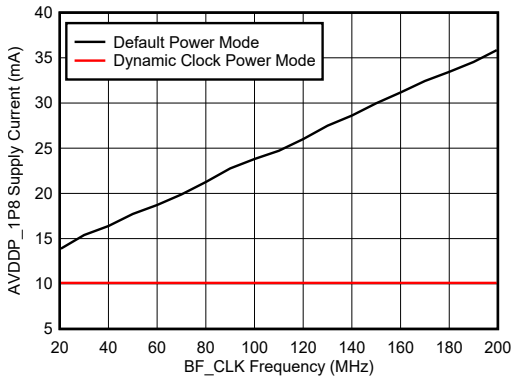


Figure 6-6. AVDD_1P8 Supply Current across Power Modes and PRF

6.8 Typical Characteristics (continued)

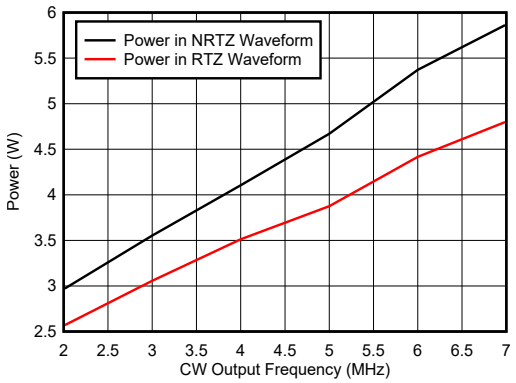


Figure 6-7. Power versus Output Frequency in CW mode

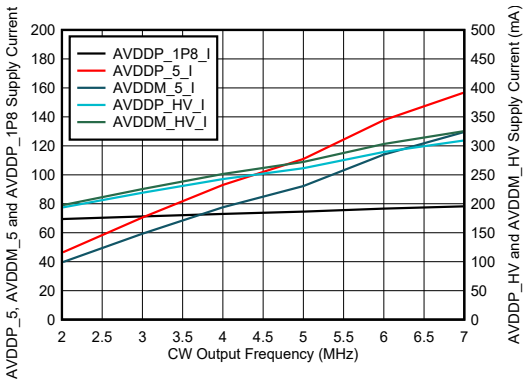


Figure 6-8. Supply Current versus Output Frequency in CW Mode (Return to Zero Waveform)

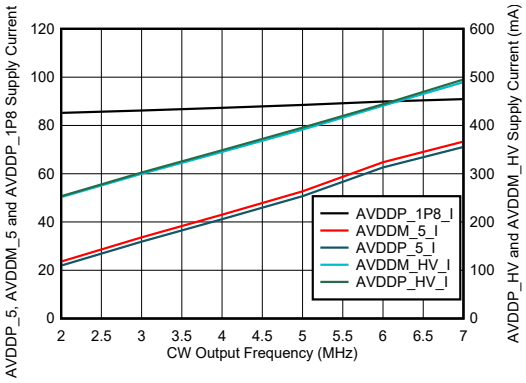


Figure 6-9. Supply Current versus Output Frequency in CW mode (Non Return to Zero Waveform)

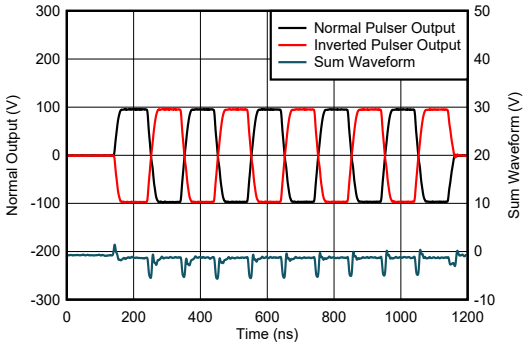


Figure 6-10. 3-Level Pulse Inversion Waveform

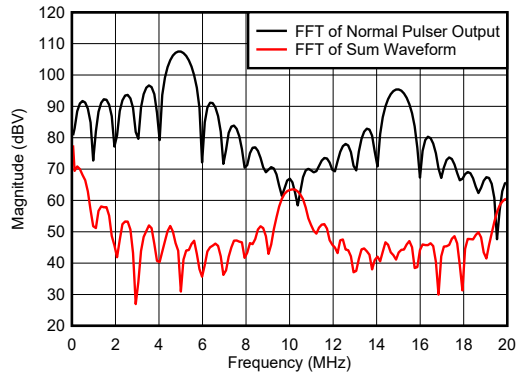


Figure 6-11. FFT of 3-Level Pulse Inversion Waveform

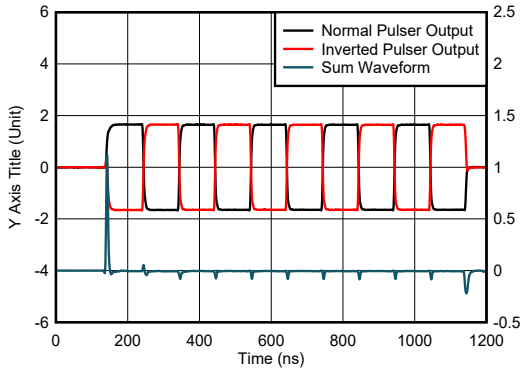


Figure 6-12. 3-Level Pulser Inversion Wavefrom at AVDDP/ M_HV Supply at ±2.5V

6.8 Typical Characteristics (continued)

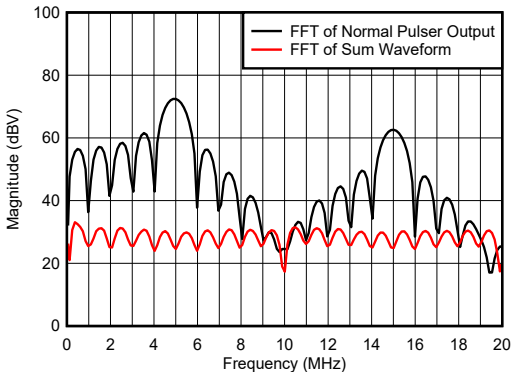


Figure 6-13. FFT of 3-Level Pulser Inversion Wavefrom at AVDDP/M_HV Supply at ±2.5V

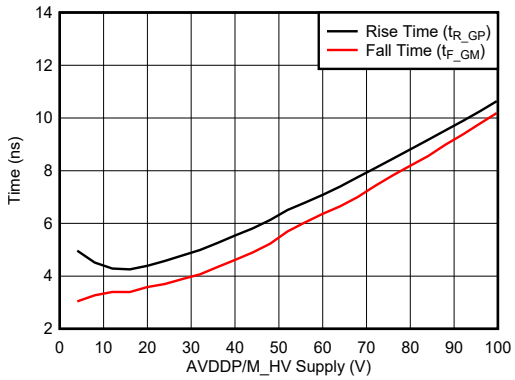


Figure 6-14. Pulser Output Rise Time (t_{R_GP}) and Fall Time (t_{F_GM}) versus AVDDP/M_HV Supply

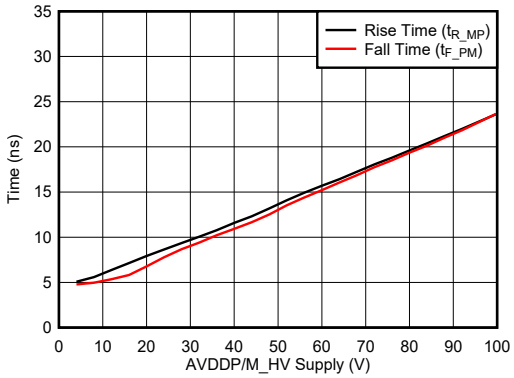


Figure 6-15. Pulser Output Rise Time (t_{R_MP}) and Fall Time (t_{F_PM}) versus AVDDP/M_HV Supply

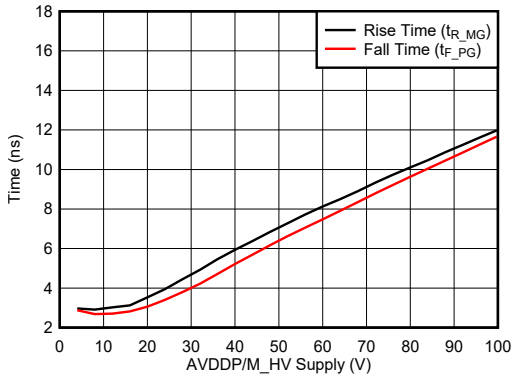


Figure 6-16. Pulser Output Rise Time (t_{R_MG}) and Fall Time (t_{F_PG}) versus AVDDP/M_HV Supply

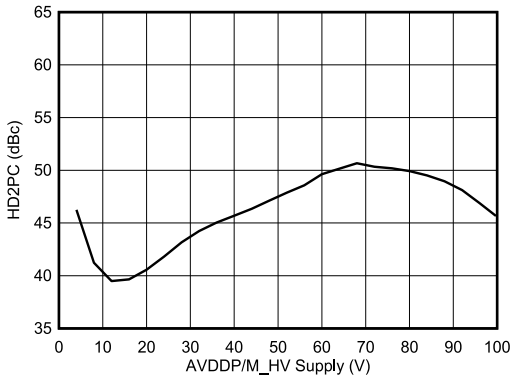


Figure 6-17. Pulser HD2 versus AVDDP/M_HV Supply Voltage

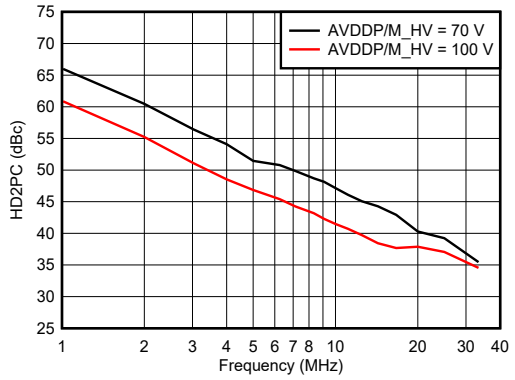


Figure 6-18. Pulser HD2 versus Frequency

6.8 Typical Characteristics (continued)

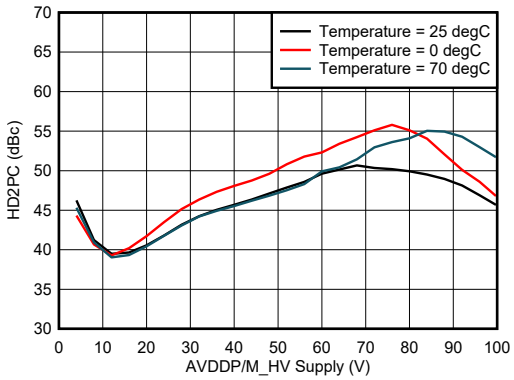


Figure 6-19. Pulser HD2 versus AVDDP/M_HV Supply and Temperature

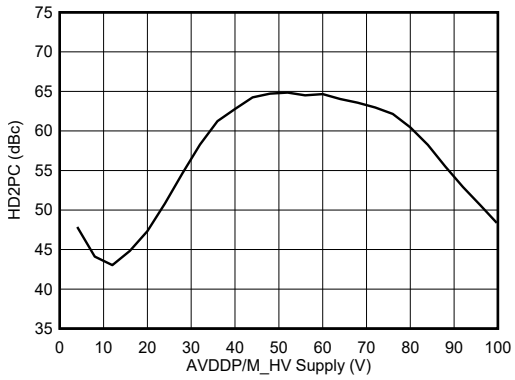


Figure 6-20. Pulser HD2 versus AVDDP/M_HV Supply for No Load Condition

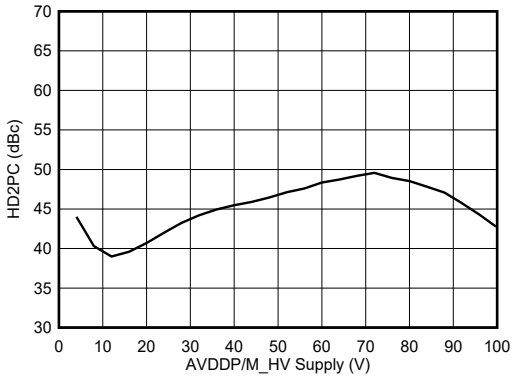


Figure 6-21. Pulser HD2 versus AVDDP/M_HV Supply for 2kΩ || 125pF Load

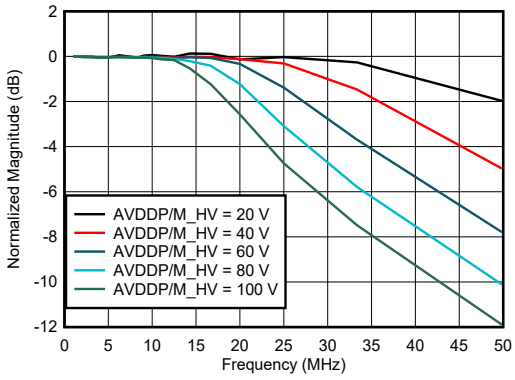


Figure 6-22. Pulser Bandwidth across AVDDP/M_HV Supply

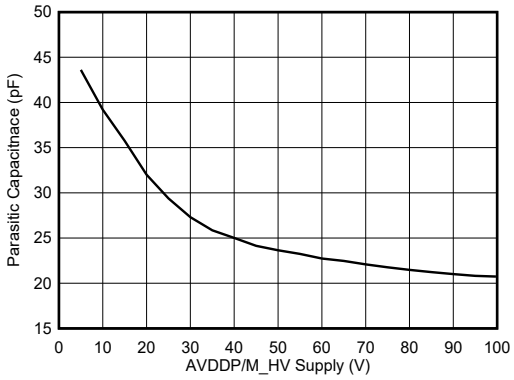


Figure 6-23. Pulser Output Parasitic versus AVDDP/M_HV Supply

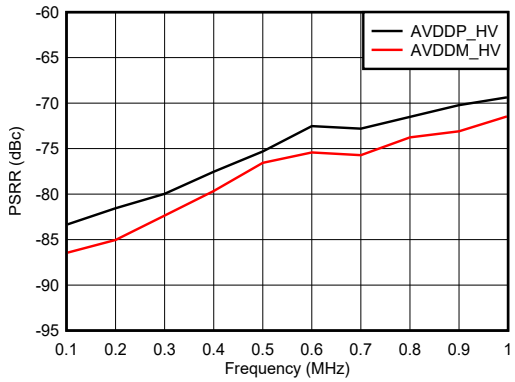


Figure 6-24. High Voltage Supplies PSRR in Receive Mode versus Supply Tone Frequency

6.8 Typical Characteristics (continued)

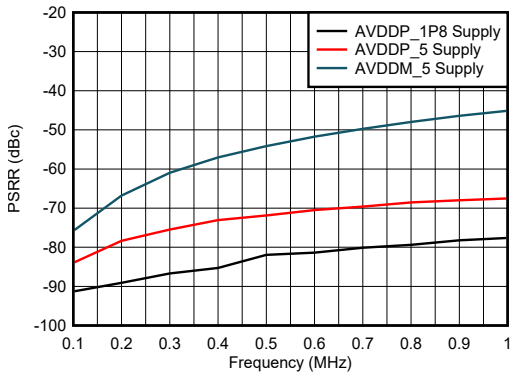


Figure 6-25. Low Voltage Supplies PSRR in Receive Mode versus Supply Tone Frequency

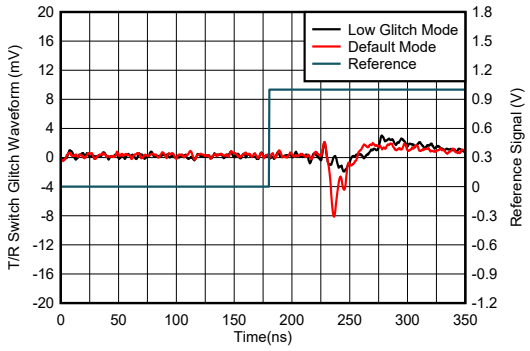


Figure 6-26. T/R Switch Turn ON Glitch

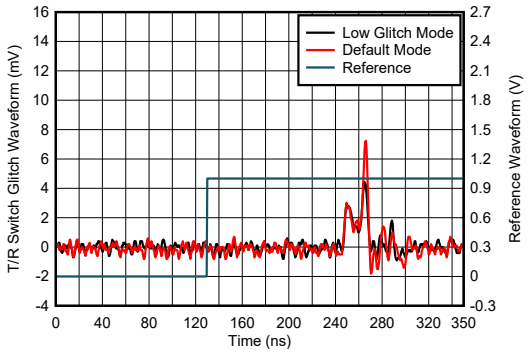


Figure 6-27. T/R Switch Turn OFF Glitch

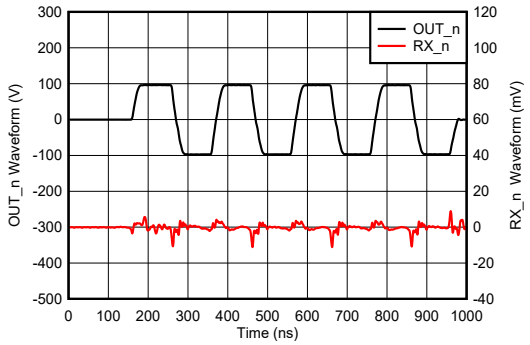


Figure 6-28. T/R Switch Isolation

7 Detailed Description

TX7364 (referred as device in this data sheet) is highly integrated transmitter solution targeted for exciting ultrasound transducers. Device integrates 64 pulsers, 64 T/R switches. on-chip beamformer and pattern generator.

Pulser circuit generates three-level high voltage pulses (up to ±100 V) with maximum output current of 1A. When pulser transmits the high voltage pulses, T/R switch turns OFF and protects the low voltage receiver circuit from damage.When the transducer is receiving echo signals, the T/R switch turns ON and connects the transducer to the receiver. The ON/OFF operation of the T/R switch is controlled by on-chip beamforming engine in the device. The T/R switch offers 26-Ω impedance in the ON state.

Ultrasound transmission relies on excitation of multiple transducer elements, with different delay values defining the direction of the transmission. Such an operation is referred to as transmit beamforming. TX7364 supports staggered pulsing of the different channels, allowing for transmit beamforming.

In the on-chip beamformer mode, delay profile for pulsing of different channels is stored within the device. The device supports a transmit beamformer delay resolution of half beamformer clock period and a maximum delay of 2^{14} beamformer clock periods. An internal pattern generator generates the output pulse patterns based on pattern profiles stored in a profile RAM. A group of 4 channels has its own RAM, which is 512 words long. The patterns have global repeat feature. This capability can be used to generate long patterns.

These pattern profiles and delay profiles are written using a high speed (400 MHz) serial peripheral interface. The high-speed writes could be prone to errors. Hence, the device has a checksum feature to detect errors in SPI writes.

To protect the device from getting damaged because of improper configuration, an internal error flag register can detect faulty condition and configure the device in shutdown mode automatically.

The device integrates all the decoupling capacitors required for the floating supplies and internal bias voltages. This significantly reduces the required number of external capacitors. TX7364 is available in a 12-mm × 12-mm 196-pin FC-BGA package (ACP package) and is specified for operation from 0°C to 70°C.

7.1 Overview

The full functional diagram of the device is shown in Functional Block Diagram.

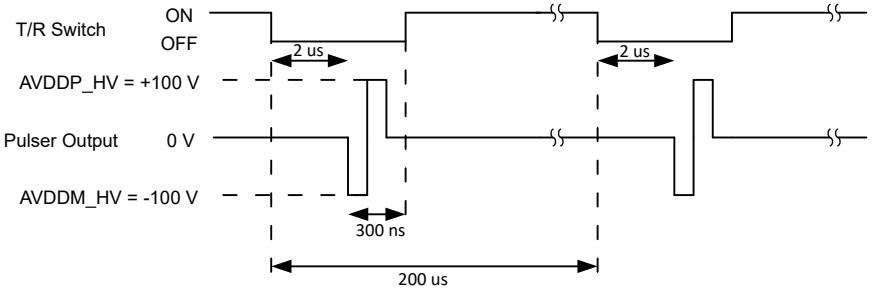


Figure 7-1. Transmit Receive Mode Output Pattern

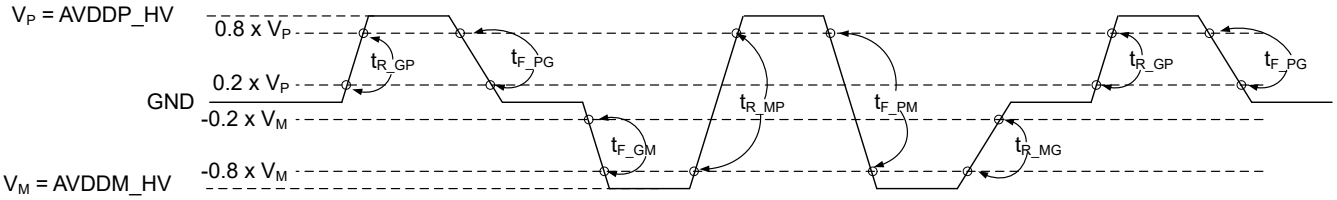
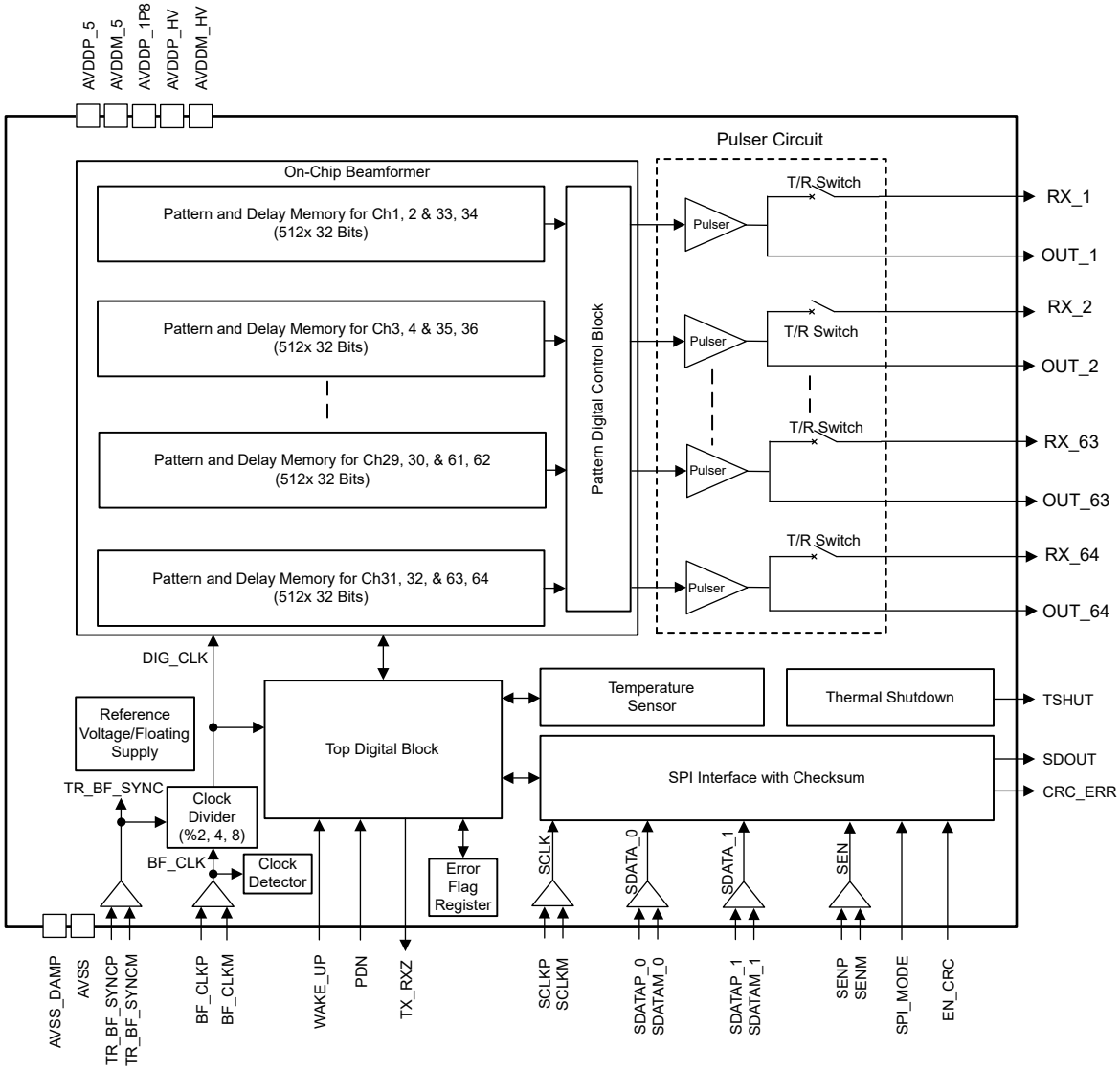


Figure 7-2. Pulser Output Waveform

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 BF_CLK Clock and TR_BF_SYNC Input

BF_CLK clock and TR_BF_SYNC input signals are used by the device to perform on-chip beamforming operation.This BF_CLK clock and TR_BF_SYNC support only differential mode input (sine wave, LVPECL, or LVDS).

7.3.1.1 Differential Input Mode

The equivalent circuit of BF_CLK and TR_BF_SYNC input buffer in differential mode is shown in Figure 7-3. Both BF_CLK and TR_BF_SYNC buffers support programmable internal termination. See the Recommended Operating Conditions for supported variation in R_{CLK_TERM} and R_{SYNC_TERM} resistance values. Table 7-1 and Table 7-2 list the typical resistance values of R_{CLK_TERM} and R_{SYNC_TERM} for different combination of register bits. The BF_CLK input is meant to be a high-speed free-running clock and can be either AC or DC coupled to the clock input pins. The TR_BF_SYNC input however is not a free-running clock and would require to be DC coupled to the device.

Table 7-1. BF_CLK Input Termination Programmability

CLK_TERM	R_{CLK_TERM} value in ohms
00	100
01	200
10	400
11	High Z

Table 7-2. TR_BF_SYNC Input Termination Programmability

SYNC_TERM	R_{SYNC_TERM} value in ohms
00	100
01	200
10	400
11	High Z

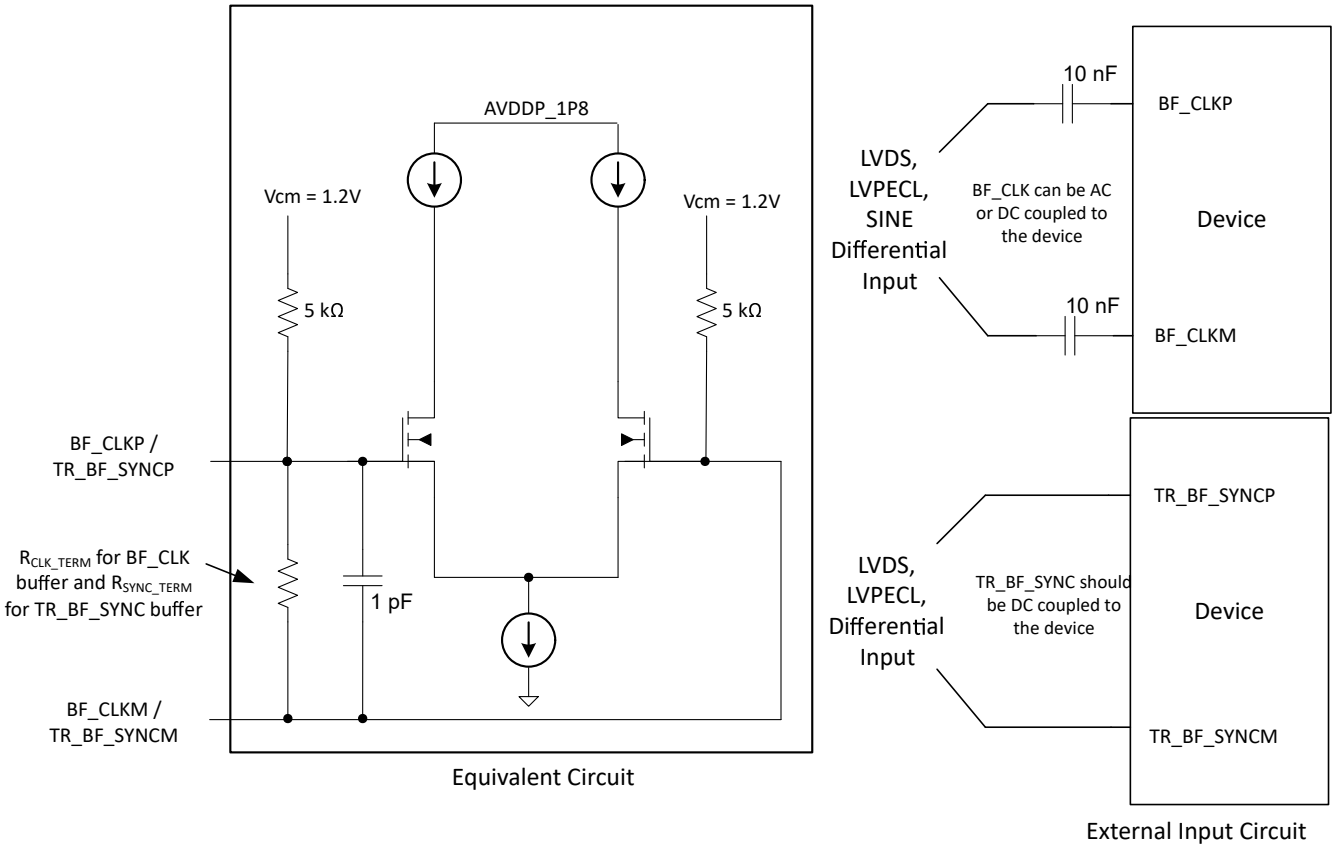


Figure 7-3. Internal Clock Buffer for Differential Clock Mode

7.3.2 Digital Clock (DIG_CLK)

The digital block of the device runs on digital clock (DIG_CLK) which is generated by dividing the BF_CLK signal. Figure 7-4 shows DIG_CLK generation scheme from BF_CLK signal. The frequency of DIG_CLK clock is given by BF_CLK divide by 2^(BF_CLK_DIV), where BF_CLK_DIV is a two bit register which can be programmed from 0 to 3. To enable the clock division feature, set BF_CLK_DIV_EN bit to '1' . The DIG_CLK gets enabled after 3 BF_CLK cycle of applying TR_BF_SYNC signal. DIG_CLK signal gets disabled when the device enters receive mode.

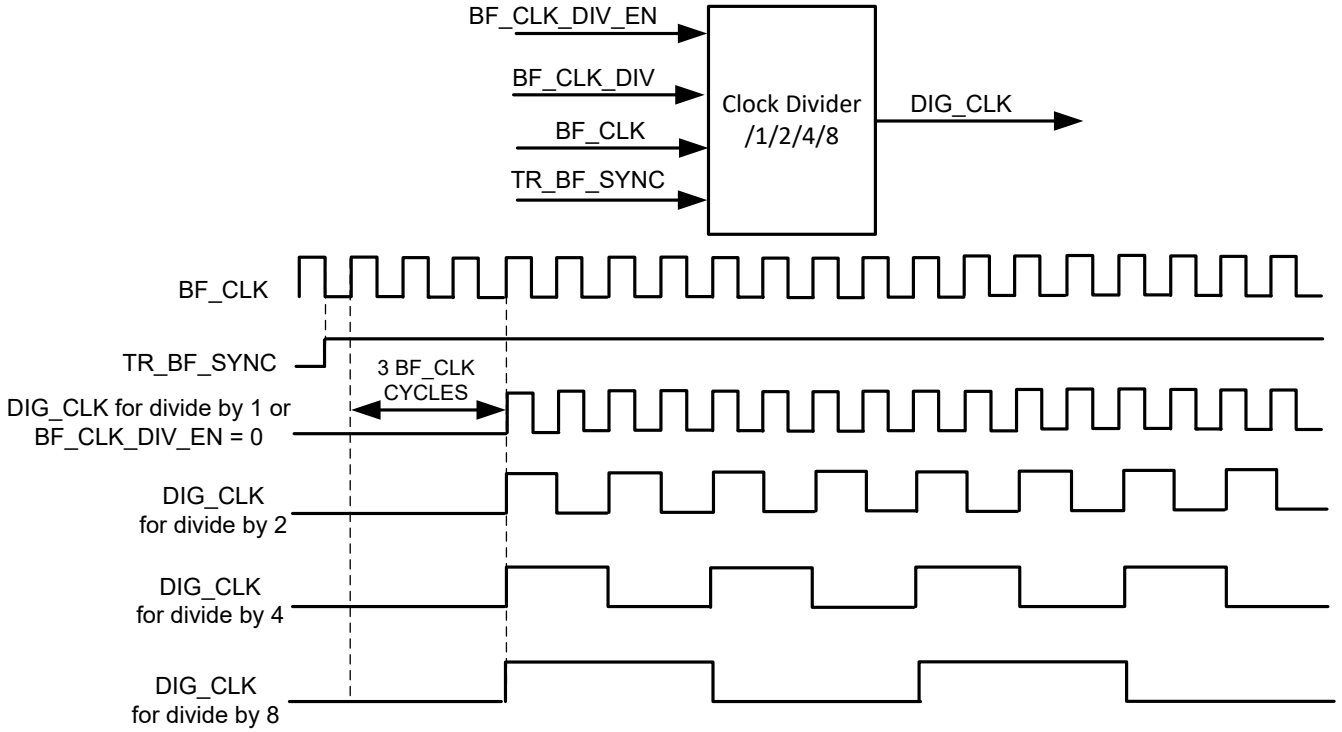


Figure 7-4. Digital Clock Generation Scheme

7.3.3 Pulser

Figure 7-5 shows a simplified block diagram of a pulser. In the device, there are total 64 pulsers. A pulser gets all the input signals from the pattern generator block. The below list describes the pulser block diagram.

- A pulser operates on high voltage supplies AVDDP_HV, AVDDM_HV.
- Level shifter blocks shift the logic level from the low voltage signals coming from the pattern generator block to the high voltage domain.
- The pulser block consists of four types of switches:
  1. Output switch: Switches SW_{PHV} and SW_{MHV} which connects the output to the high voltage supplies.
  2. Return to zero switch: Switch SW_G which connects the output to ground.
  3. Initialize switch: Switch SW_{INT} which connects the internal node to ground through initialization resistor R_{INT} when device is in the receive mode.
  4. T/R switch: T/R switch disconnects or connects the receiver side to the transducer connected on OUT_n node.
- All the transistors and T/R switches turns on when corresponding control signal goes to logic level ‘1’.
- Return to zero switch supports true discharge of output to ground without any diode drop.
- Figure 7-6 shows a simplified schematic of the T/R switch. T/R switch turns on when EN_TR is set to logic level '1', and turns off when EN_TR is set to logic level '0'. It consists of a series transistor which remains off when T/R switch is off and protects the low voltage Rx from high voltage pulses. This series transistor turns on when the T/R switch is on and connects the Rx input to the ultrasound transducer. On the low voltage Rx input side, there is a transistor between AVSS and low voltage rx node, which turns ON when the T/R switch is OFF. It helps in reducing a T/R switch leakage in transmission phase. T/R switch equivalent diagram in ON and OFF state is shown in Figure 7-6.

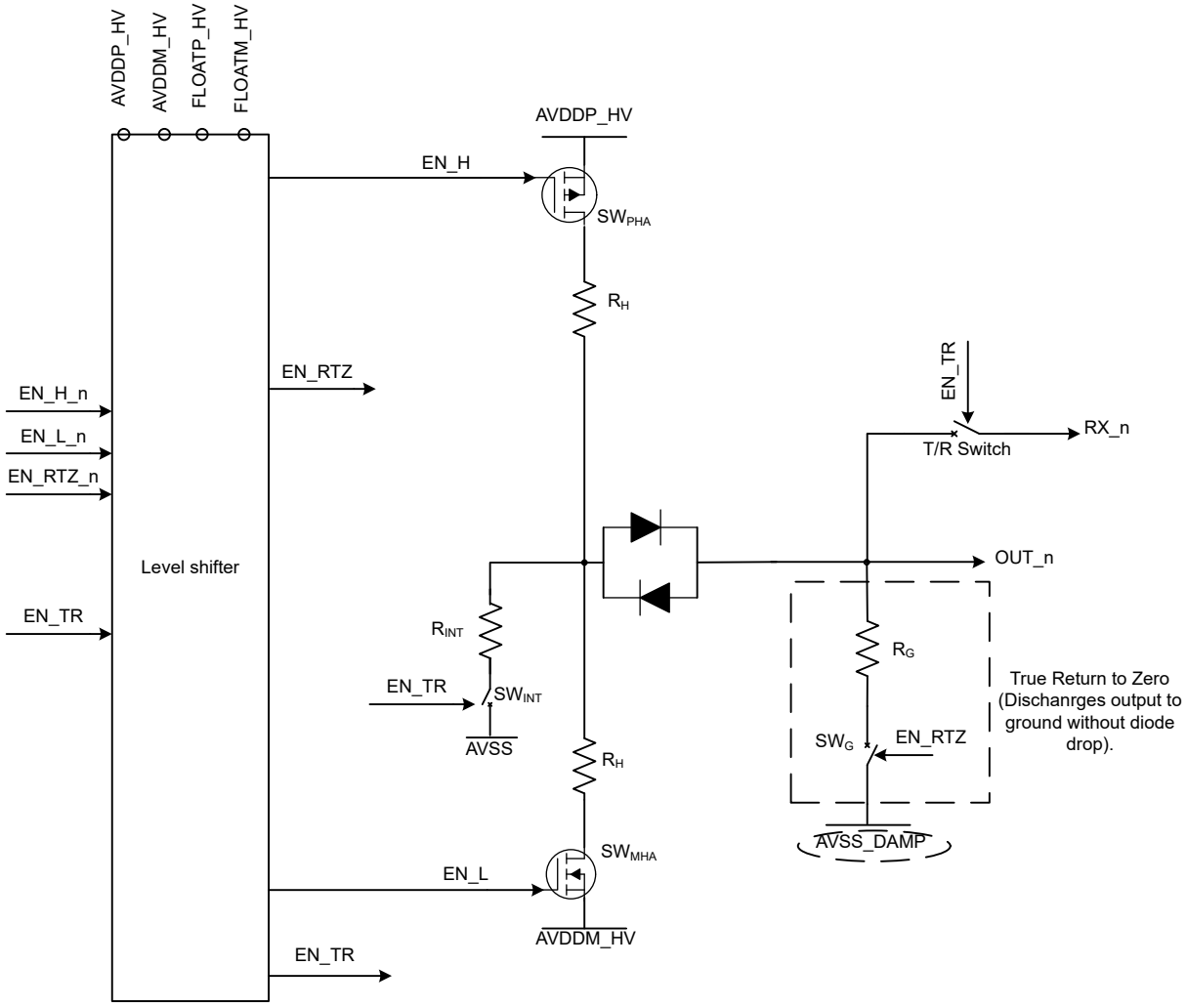


Figure 7-5. Pulser Block Diagram

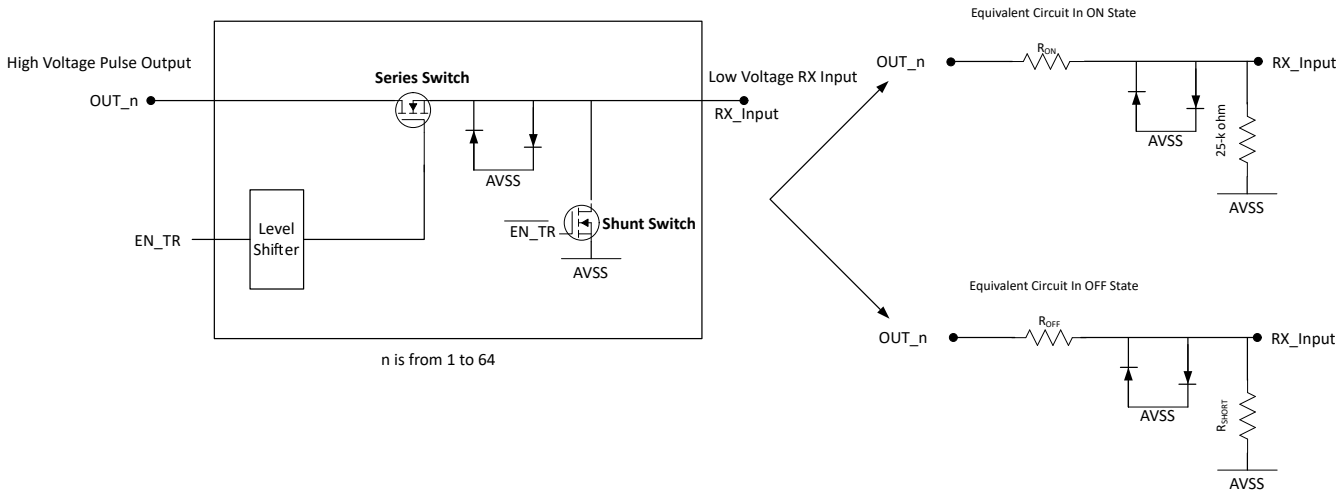


Figure 7-6. Simplified Schematic of T/R Switch

7.3.4 Output Level Modes

The device has 64 pulsers. These pulsers can be configured to generate 3-level waveforms. Typical output waveform for 3-level mode is shown in Figure 7-7.

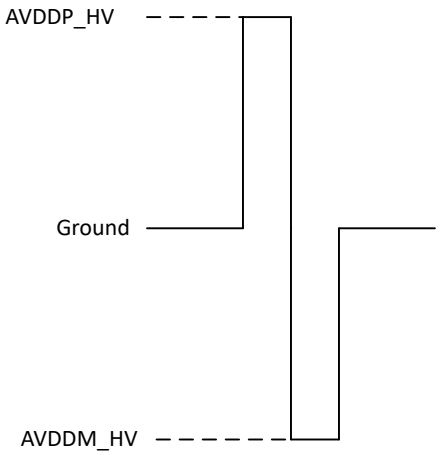


Figure 7-7. Typical 3-level Output Waveform

7.3.5 Floating LDOs

To turn ON the high voltage PMOS and NMOS transistors, a gate voltage is applied which is generated using integrated floating LDOs. In the device there are total four floating LDO for this purpose. In default mode of operation, to reduce the device power consumption, floating LDOs gets powered down automatically whenever device enters in receive mode. If receive duration of the device is less than 100 ms then applying WAKE_UP signal before 2us of applying TR_BF_SYNC is enough to power up the floating LDO. In below cases the floating LDOs takes longer time to power up.

1. On powering up the device.
2. When device is configured in global power down mode for greater than 100 ms.
3. When device enters in thermal shutdown mode for greater than 100 ms.
4. When device remains in receive mode (for eg, T/R switch of all channels are ON) for more than 100 ms).

In each of the above case, to use the device in transmit mode it is required to power up the floating LDOs.Follow any one of the below steps to power up the floating LDOs:

1. Keep WAKE_UP signal high for 200-µs duration.
2. Set the register bit DIS_DYN_PDN_LDO to '1', wait for 200 µs and set the bit DIS_DYN_PDN_LDO to '0'.

Whenever floating LDOs are powered up, there will be a surge current of ~350mA to 400mA on ±5 V and high voltage supplies. So, for the system with 4 TX7364 devices on board, surge current can go as high as 1.6 A. If ±5 V supplies are not designed to handle this high current then supply can dip which will RESET the device. To avoid this issue any of the below solutions can be adopted:

1. Apply WAKE_UP signal across devices in sequential order. For ex, if a system has 4 devices, then apply WAKE_UP signal to devices 1 and 2 for the first 200 us, then to 3 and 4 for next 200 us.
2. In case all the devices share the same WAKE_UP signal then using PDN_FLOAT* bits, floating LDOs can bepowered up in sequential order. First set the PDN_FLOAT* bits to "1" in all the devices, apply WAKE_UP signal and set PDN_FLOAT* bits back to 0 device by device using SPI signal.
   - Since 1.6-A current flows only for a short duration of 200 us, so supply dip can be reduced by using higher decap on the ±5-V supplies.
   - Surge current can be reduced by programming register bits RED_MAX_CUR_P1, RED_MAX_CUR_P2, RED_MAX_CUR_M1, and RED_MAX_CUR_M2. Reducing the surge current increases the LDO power up time by same factor multiplied by 200 us.

To enable the floating LDOs permanently, set register bit DIS_DYN_PDN_LDO bit to '1'. When this bit is set to'1' then it is not required to apply WAKE_UP signal to power up the floating LDO. Each floating LDO consumes typically 400 uA current through high voltage supply and independent of supply level. For AVDDP/M_HV = ±100 V, device will consume extra power of 160 mW (400 uA x 4 x 100 = 160 mW). When device is configured in CW mode then also LDOs gets powered up permanently. The four floating LDOs can be powered down individually using register bits PDN_FLOAT_PHV1, PDN_FLOAT_PHV2, PDN_FLOAT_MHV1, and PDN_FLOAT_MHV2 register bits.

7.3.6 Memory Block Organization

In the device, there are a total of 16 memory blocks. As mentioned before, a group of 4 channels share the same memory block for pattern, delay & T/R Switch OFF & ON delay information. The memory is organized as a 512-word deep block (each word is 32 bit long). The below figure shows the contents of the memory and how it is supposed to be programmed for Transmit Beamforming & Pattern Generation.

Table 7-3. Memory Block N (N can have any value from 1 to 16)

Address <8:0>	Data[31:24]	Data[23:16]	Data[15:8]	Data[7:0]	Remarks
0	TR_SW_ON_DEL of Channel 2*N + 31	0	TR_SW_ON_DEL of Channel 2*N - 1	0	The first address of the memory should always have the T/R Switch ON delay information of channels 2 × N - 1 and 2 × N + 31. This address is hard-coded and so does not have any memory pointer associated with it
1	TR_SW_ON_DEL of Channel 2*N + 32	0	TR_SW_ON_DEL of Channel 2*N	0	The second address of the memory should always have the T/R Switch ON delay information of channels 2 × N and 2 × N + 32. This address is hard-coded and so does not have any memory pointer associated with it
Address <8:0>	**Data <31:16>**		**Data<15:0>**		**Remarks**
…					
K	Channel Delay of Channel 2 × N + 31		Channel Delay of Channel 2 × N - 1		Delay Profile 0. (Program BF_PROF_SEL_n to K to use this delay information. K can be from 2 to 510 and should be an even number)
K+1	Channel Delay of Channel 2 × N + 32		Channel Delay of Channel 2 × N		
K+2	Channel Delay of Channel 2 × N + 31		Channel Delay of Channel 2 × N - 1		Delay Profile 1. (Program BF_PROF_SEL_n to K to use this delay information. K can be from 2 to 510 and should be an even number)
K+3	Channel Delay of Channel 2 × N + 32		Channel Delay of Channel 2 × N		
…					
Pattern Start Address (M0)	Pattern profile 0 starts here				Pattern Profile 0 (Denoted by 9-bit number programmed in register MEM_START_WORD with the constraint that it should be a odd number)
M0+1					
…					
Pattern End Address (M0+L0)	Pattern profile 0 ends here				
…					
Pattern Start Address (M1)	Pattern profile 1 starts here				Pattern Profile 1 (Denoted by 9-bit number programmed in register MEM_START_WORD with the constraint that it should be a odd number)
M1+1					
…					
PatternEnd Address (M1+L1)	Patternprofile 1 ends here				

Table 7-3. Memory Block N (N can have any value from 1 to 16) (continued)

Address <8:0>	Data[31:24]	Data[23:16]	Data[15:8]	Data[7:0]	Remarks
…					
511					

As shown in Table 7-3:

1. The memory block is organized as a 512 × 32-bit space. There is a total of 512 words in each memory block with each word being 32 bits wide.
2. There are 16 memory blocks present in the device. Each memory block provides Transmit Beamforming and Pattern Generation information for 4 channels. A memory block N (N = 1 to 16) provides information on the channels 2 × N - 1, 2 × N, 2 × N + 31 & 2 × N + 32.
3. The first register in the memory block is reserved for T/R Switch ON delays. As shown in Table 7-3, the bits [15:8] correspond to T/R Switch ON delay of channel 2*N-1 and the bits [31:24] correspond to T/R Switch ON delay of channel 2*N+31'. The unused bits in this register must be initialized and set to 0 to avoid improper functioning of the device.
4. The second register in the memory block is also reserved for T/R Switch ON delays. As shown in Table 7-3, the bits [15:8] correspond to T/R Switch ON delay of channel 2*N and the bits [31:24] correspond to T/R Switch ON delay of channel 2*N+32'. The unused bits in this register must be initialized and set to 0 to avoid improper functioning of the device.
5. The channel delays for channels 2 × N - 1, 2 × N, 2 × N + 31 & 2 × N + 32 can be stored anywhere in the memory (except for the first two locations) with the constraint that the starting location should be even. Multiple delay profiles can be stored and a Delay Pointer is used to point to the required delay profile. A maximum of 250 delay profiles can be stored (assuming 10 words are required for the pattern stored in the memory). Memory location K holds the delay information of channels 2 × N - 1 & 2 × N and location K+1 holds the delay information of channels 2 × N + 31 & 2 × N + 32 where K is the value programmed as the BF_PROF_SEL_n and should be even.
   a. As shown in Table 7-3, the delay for a channel is a 16 bit field. Let us us call it Delay[15:0].
   b. Out of the 16 bits, the LSB 14 bits are used to program the actual delay information, that is, Delay[13:0] is used to store the channel delay.
   c. The 15th bit, Delay[14], is used to store the fractional delay for the channel. This feild is called FRAC_DEL_n where 'n' corresponds to the channel number. Setting FRAC_DEL_n to '1' will delay the pattern by a further half beamformer clock period.
   d. The MSB bit, Delay[15], is unused and can be set to 0.
6. The pattern information for channels 2 × N-1, 2 × N, 2 × N + 31 & 2 × N + 32 can be stored anywhere in the memory except for the first and second location and pattern should start from odd word address in memory. A pattern pointer MEM_START_WORD points to the pattern profile for all the 64 channels in the memory.

7.3.7 On-Chip Beam-Forming Mode

The device supports On-chip beam forming mode which is used to generate pulser output waveform and control T/R switch ON/OFF operation. Figure 7-8 shows a simplified block diagram of on-chip beam forming mode operation. Sequence of operation performed by the On-chip beamformer is as below:

1. An input pulse is applied at WAKE_UP pins. This input pulse wakes up floating LDO in default mode and also BF_CLK and TR_BF_SYNC buffer in dynamic clock power mode. WAKE_UP signal is not needed if DIS_DYN_PDN_LDO bit is set to '1' and device is not configured in dynamic clock power mode.
2. An input pulse is applied at TR_BF_SYNC pin. On receiving this pulse signal the transmit beamformer block of the device starts generating the clocks (CLK_1, CLK_2...CLK_64) for pattern-generator block after counting certain number of BF_CLK period as per the content of delay profile.
3. After the pattern-generator block receives the clock, it starts generating control signal for the pulser as per the values programmed in the pattern profile.
4. The pulser then generates high voltage output pulse signal as per the control signals generated by the pattern-generator block.
5. After pattern gets over, the T/R switch is turned ON to connect receiver AFE to the transducer.

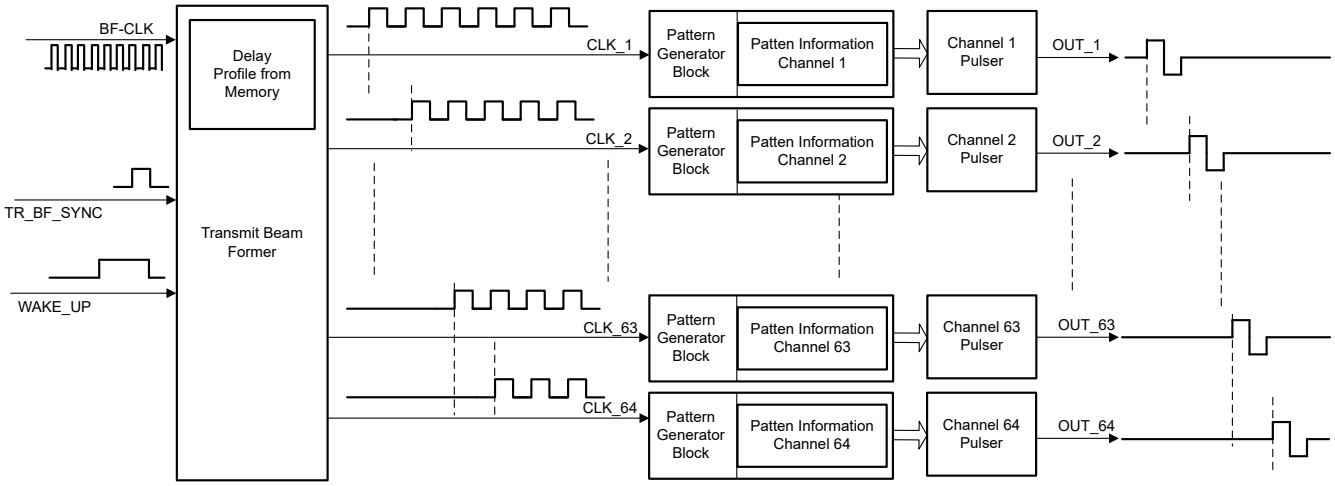


Figure 7-8. On-chip Beamforming Mode

The on-chip beamforming mode greatly simplifies controlling the beamforming operation. Unlike the off-chip beamforming mode, it does not require additional input control signals to define the instantaneous pulse transitions.Instead, delay and pattern (shape) of each channel is stored in delay and pattern profiles. There are many such profile sets that can be programmed at start through the SPI interface. Each transmit window is defined by a TR_BF_SYNC pulse, and the required profile to be used for a transmit window can be loaded through a single register control. Additionally, a new profile (for example, a delay profile required for a certain focusing depth) can also be programmed prior to the start of the transmit window.

7.3.8 Trigger Signal in On-chip Beamforming

Applying trigger signal to device is the first step to start on-chip beamforming operation. By default,TR_BF_SYNC detection is disabled, allowing the user to first to program the device and then enable SYNC detection. To enable TR_BF_SYNC detection, set the register bit EN_SYNC_DET to '1'. Further to achieve low power from the device the internal high voltage floating LDO references are powered down during the receive mode. In order to apply trigger signal to the device, the internal floating supply blocks must be powered up. WAKE_UP pin is made high to power up these blocks. After floating LDOs are powered up, a pulse on TR_BF_SYNC pin is used to trigger the device. See Figure 7-9 and Section 6.7 for timing requirement with respect to BF_CLK. Figure 7-9 is applicable when device is not configured in receive mode or in global power down mode for more than 100 ms. In such cases WAKE_UP signal has to be applied for 200 µs duration as explained in Section 7.3.4.

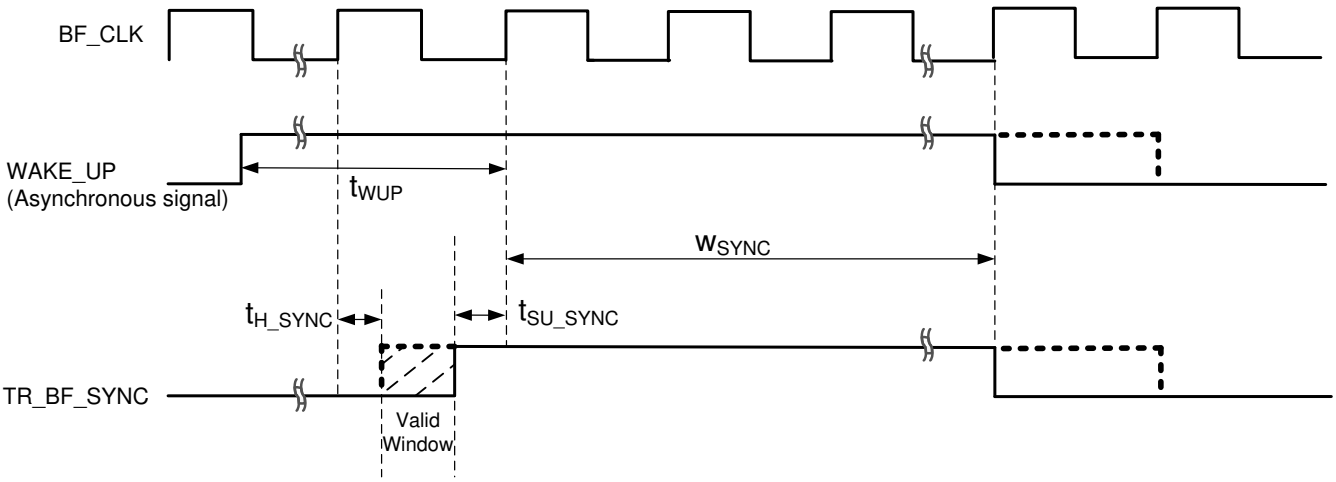


Figure 7-9. TR_BF_SYNC and WAKE_UP Timing Requirement

Note

For simplicity in explanation, only TR_BF_SYNC pulse is shown as trigger signal in this document. It is assumed that WAKE_UP signals is applied to the device as per the given suggestion.

7.3.8.1 TR_BF_SYNC and SPI Timing Requirement

Below points explain timing requirement between SEN and TR_BF_SYNC signal:

1. When CRC mode is enabled: In CRC mode, after completing SPI writes operation, the user needs to send 32 CRC bits after making SEN high. So, users should wait for 32 SPI clocks for CRC to complete and then applythe TR_BF_SYNC signal. TR_BF_SYNC signal can be applied immediately after sending the last CRC bit.
2. When CRC mode is disabled: TR_BF_SYNC signal should be applied after 100 ns of SEN signal goes high. If this requirement is not met, then device can transmit unexpected signal.

7.3.8.2 Transmit Beamformer (TxBF)

The functional block diagram of TxBF block in on-chip beamforming mode is shown in Figure 7-10. TxBF block takes its input from the delay and pattern information in memory, and register settings. Based on these input signals, the TxBF block generates a clock signal for the pattern generator block. The TxBF block consist of total 64 counters (C_1 to C_64) and 64 clock dividers (D_1 to D_64).

Note that on receiving the TR_BF_SYNC pulse, T/R switch starts to turn OFF and takes T_{TOFF} time to fully turn off.

Until T/R switch is not completely turned OFF, pulser will not generate high voltage pulses. For this reason,a channel delay should be programmed such that pulser starts transmitting the high voltage pulses after T/R switch is in OFF state.

Figure 7-11 and the following steps describe the sequence of operations performed by the TxBF block:

- When device is in receive mode, the output of all the counters are set to zero and each counter waits for an enable pulse. Similarly, all the clock dividers get reset and disabled in receive mode and wait for the enable signal from the corresponding counter.
- The enable signal (EN_COUNT) for the counter is generated by counting 292 number of DIG_CLK clock periods. DIG_CLK clock is generated by the device after 3 BF_CLK clock cycles of applying TR_BF_SYNC pulse.
- On receiving the enable pulse, each counter {C_1, ... to C_64} starts counting and generates the enable signal for the clock divider (EN_DIV_n signals) after DEL_n number of DIG_CLK clock cycles. The DEL_n control comes from the chosen delay profile. The device supports maximum integer delay (DEL_n) value of $(2^{14} - 1)$ DIG_CLK clock periods and minimum delay of 1 DIG_CLK clock period.
- After receiving EN_DIV_n enable signal, the clock divider generates output clock signals CLK_1, CLK_2… CLK_64 by dividing DIG_CLK clock signal by factor N. Here N represents the value programmed using CLK_DIV register control as listed in Table 7-4. An internal propagation delay t_{PROP_INT} from BF_CLK to divided clock is also involved in the generation of the output clock. The parameter value of t_{PROP_INT} is listed in Section 6.7.
- The pattern generator output can be delayed further by half of DIG_CLK period before applying to the pulser. This feature is termed as fractional delay feature. When FRA_DEL_n bit is set to '1' then the final pattern generated by the pulser of channel n gets delayed by half DIG_CLK period. Hence the minimum resolution that can be achieved is half the DIG_CLK period.

Table 7-4. Pattern Generator Clock Programmability

CLK_DIV Register Value (Decimal)	Division Factor N
0	1
1	2
2	3
3	4
4	5

Table 7-4. Pattern Generator Clock Programmability (continued)

CLK_DIV Register Value (Decimal)	Division Factor N
5	6
6	7
7	8
8	16
Others	32

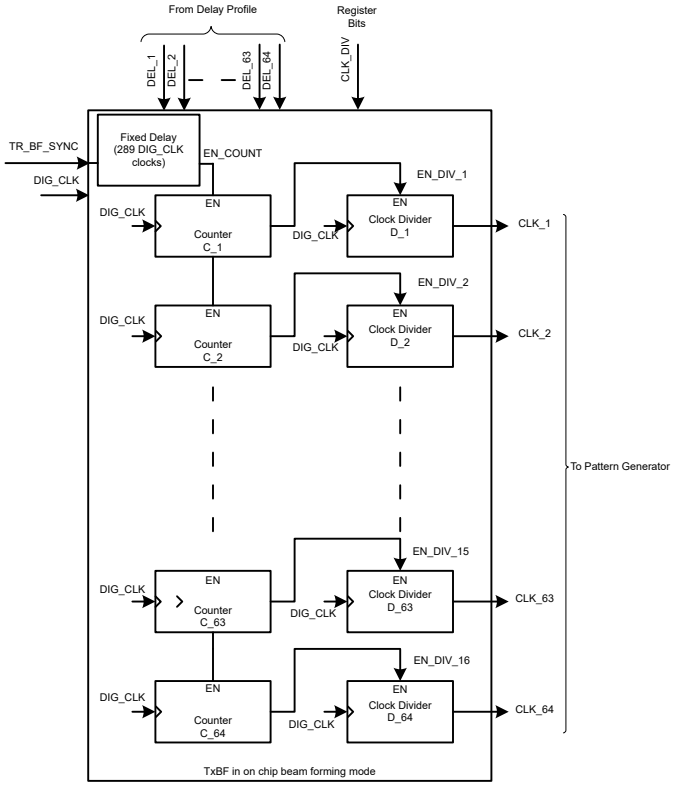


Figure 7-10. TxBF Block Diagram

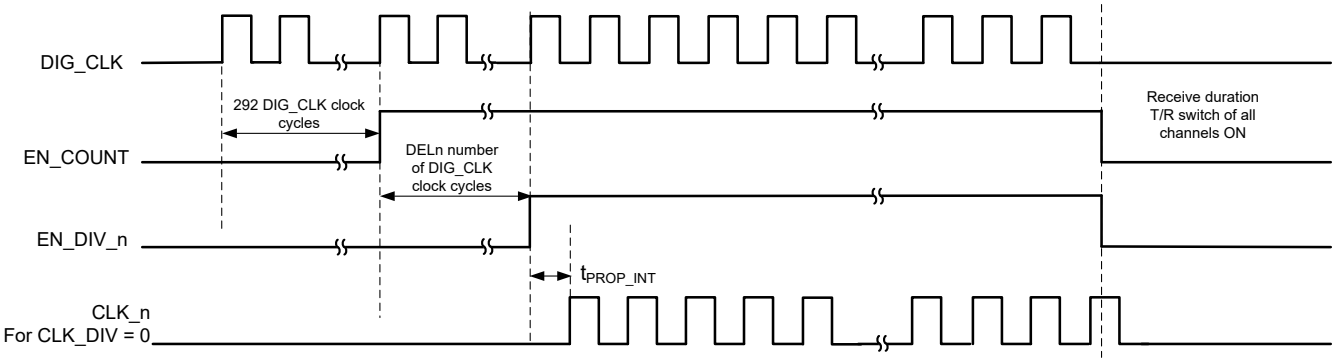


Figure 7-11. Timing Diagram of TxBF Block

7.3.8.2.1 Delay Profile Selection

The device supports multiple delay profiles to configure the delay for transmit beam-former block.

Note

The content of both delay and pattern memory are undefined on power up and applying a reset. A user should configure it as per the requirement. Also applying reset to the device does not modify the content of delay and pattern memory.

Multiple delay profiles can be programmed and stored within the device. Each delay profile contains integer delay and fractional delay for all the 64 channels as explained in Section 7.3.6. A user can switch between delay profiles by choosing the new profile through the register control bits BF_PROF_SEL_n (n = 1 to 16). Programming avalue of N (N can be any value from 2 to 510) in BF_PROF_SEL_n field, enables the delay profile present at location N in memory.

- These control bits are present for every memory block, that is, for every set of 4 channels.
- In each memory block, delay information of 4 channels are present. Memory block M (M ranges from 1 to 16) provides delay information of channels 2 × M-1, 2 × M, 2 × M + 31 & 2 × M + 32.
- By programming a value of N in the BF_PROF_SEL_n, the device takes the register information of word N & N+1 in memory and interpret to be the channel delay information, that is, the LSB 16 bits of word N provide delay information of channel 2 × M–1, MSB 16 bits of word N provide delay information of channel 2 × M+31, LSB 16 bits of word N+1 provide delay information of channel 2 × M, MSB 16 bits of word N+1 provide delay information of channel 2 × M+32. This includes the fractional delay information as well.

Changing BF_PROF_SEL_n does not change the profile instantaneously. The change in the profile is reflected in next profile read window as explained in Section 7.3.8.3.4.

7.3.8.2.2 Delay Update Time

Below section gives an estimate of the total time taken to program the delays to all 64 channels of the device for a single PRT. As mentioned earlier, the delay information of a group of 4 channels is present in 2 registers of a memory block. There are 2 ways we can update the delay values for all 64 channels in the device.

1. The delay values can be individually programmed line to line, just before the start of transmit or in the previous TR_BF_SYNC.
2. The delay values can be loaded into the memory (the memory can hold roughly 250 delay profiles) at the start of imaging. The user can just change the delay pointer from line to line.

For the first approach, to update the delay profile for a group of 4 channels, a total of three registers have to be written as follows:

1. Page Select Register
2. First Register for delays of two channels
3. Second Register for delays of the other two channels

Each register write consists of a packet length of 44 bits. To update 1 delay profile, the total number of bits sent is 44×3 = 132 bits.

To update the delays of all 64 channels of the device, the total number of bits are 132×16 = 2112 bits.

The TX7364 has two high speed LVDS SPI lanes capable of a maximum speed of 400Mbps. Therefore, the effective data rate is 800Mbps, or 1.25ns/bit.

Thus, total time take to send the entire delay information to the device is 2112×1.25 = 2.64us.

The time taken (in us) to update the delay profile in this approach is given by MEM_NUM×132×(1/(SPI_Rate×NUM_LANES), where MEM_NUM is the number of memory blocks that has to be updated, SPI_RATE is the speed of SPI operation (in MHz), and NUM_LANES is the number of SDATA lanes used for programming.

For the second approach, to update the delay pointers for the memory blocks, a total of eight registers have to be written (Each register holds the pointer for two memory blocks).

The packet length for each register is 44 bits.

Hence a total of 8×44 = 352 bits have to be sent to the device.

With an effective data rate of 1.25ns/bit, the total time taken to update the delay pointers is 352×1.25 = 440ns.

The time taken (in us) to update the delay profile in this approach is given by (NUM_PTR/2)×44×(1/(SPI_Rate×NUM_LANES), where NUM_PTR is the number of delay pointers that has to be updated, SPI_RATE is the speed of SPI operation (in MHz), and NUM_LANES is the number of SDATA lanes used for programming.

The above time can be reduced further using burst mode where the packet length will be 32bits (address is auto-incremented in burst mode).

7.3.8.3 Pattern Generator

Pattern Generator in the device generates control signals for pulser based on the multiple input signals as shown in Figure 7-13. Pattern-generator block supports two modes of operation; B-mode and CW mode.

7.3.8.3.1 B-Mode

Figure 7-12 shows functional block diagram of pattern generator in B-mode operation. Pattern generator block generates control signal for the pulser whenever it receives the clock (CLK_n) from TxBF block after getting TR_BF_SYNC pulse. Pattern generator reads the value stored in pattern memory and based on that it generates the control signal for the pulser. A group of 4 channels share a common pattern memory and hence, will transmit the same pattern.

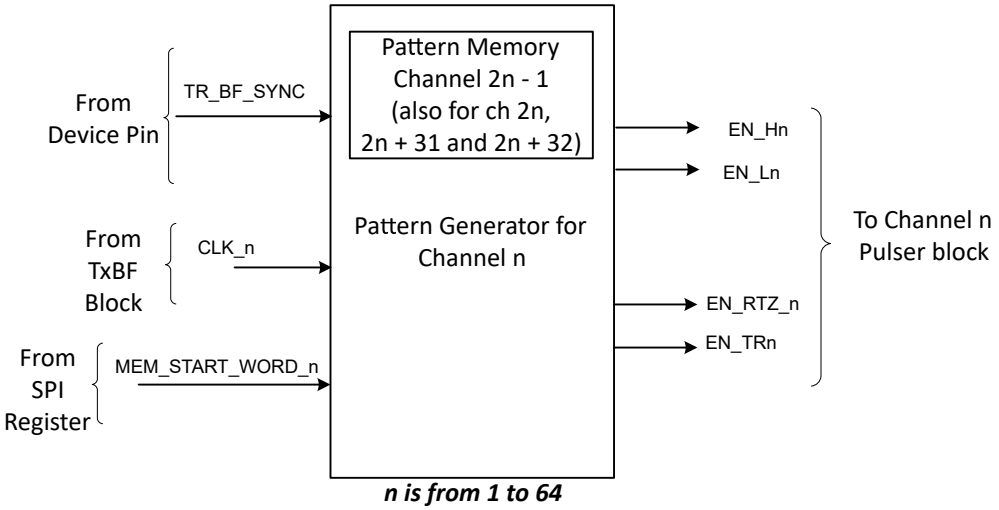


Figure 7-12. Pattern generator in B-mode

7.3.8.3.1.1 Pattern Memory

Figure 7-13 shows the pattern memory arrangement.

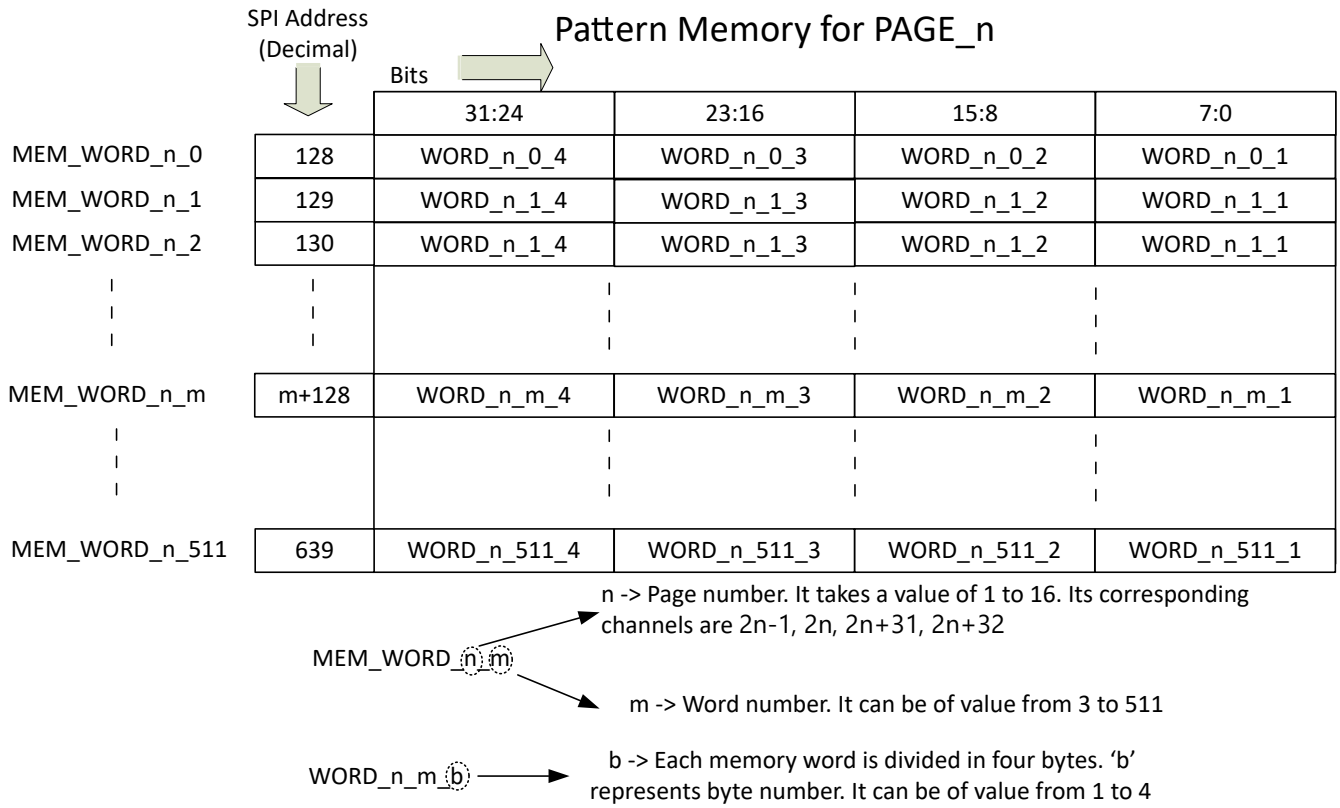


Figure 7-13. Pattern Memory Map

- In device there are total 16 memories. Each memory provides information for 4 channels such as the T/R Switch ON delay, channel delay and pattern.
- Each memory has total 512 words; word 0 to word 511. Each word is of length 32 bits.
- The word m (m can be from 0 to 511) of page n (n from 1 to 16) can be programmed by writing in register address of m + 128 in register page n.
- Each word is further divided in four bytes (WORD_n_m_b). Based on content of byte the pattern generator block decides the pulser control signal output.
- The first & second word, MEM_WORD_n_0 & MEM_WORD_n_1, is reserved for the T/R Switch ON delay. This word cannot be used for storing the delay or pattern information of the channel.
- Apart from the first & second word, the content and the location of byte in the memory word decide its interpretation by the pattern generator block.The interpretation of byte is divided into three categories as below. Table 7-5 lists the range of value that can be programmed in different types of bytes.
  - Global repeat number (GBL_REP_NUM)
  - Pattern Length (PAT_LEN)
  - Level-periodparameter (LVL_PER)

Table 7-5. Byte Category and Allowed Values

Byte Type	Allowed Values (Hexadecimal)
GBL_REP_NUM	0x00 to 0xFF
PAT_LEN	0x0000 to 0x3FFF
LVL_PER	0x00 to 0xFF

7.3.8.3.1.2 Pattern Generator Operation in B-mode

Below steps explain the operation of pattern generator. In below description suffix "n" represent the page number (1 to 16).

- **Step1**:On receiving TR_BF_SYNC pulse pattern generator block starts to turn OFF T/R switch as per logic explained in T/R Switch Control Signal.
- **Step2**:After T/R switch is turned OFF, the pattern generator makes EN_RTZ_n signal high (Pulser output goes to return to zero state) and waits for CLK_n clock signal from transmit beamformer block. Transmit beam former block activates the CLK_n signal after counting for delay value; more detail given in Transmit Beamformer (TxBF).
- **Step 3**: On receiving CLK_n clock, pattern generator reads the first byte (WORD_n_m_1) of word MEM_WORD_n_m.Where m represents the address programmed in register MEM_START_WORD. The MEM_START_WORD' is common to all the memory blocks. m can take any value between 3 to 511 (The 0^{th} & 1^{st} word is reserved for T/R Switch delays of the channels and even though the 2^{nd} word is free, it does not satisfy the constraint that the address of the starting word should be 1 and hence cannot be used for storing the pattern). This byte is always treated as GBL_REP_NUM (Global repeat number). The number of transitions in the pattern, defined by PAT_LEN can be repeated G number of times, where G is value programmedin byte GBL_REP_NUM. GBL_REP_NUM byte can be programmed from 0 to 255; 0 means no repeat.
- **Step 4**: The 2^{nd} byte in this word is reserved. Pattern generator block reads the third- and fourth-byte WORD_n_m_3 and WORD_n_m_4. In this 16-bit number, the MSB 2 bits are always 0 and ignored. The rest 14 bits are use to define the length of the pattern and is subsequently referred to as PAT_LEN. This defines the total number of states or transitions for this particular pattern. There are a total of K states/transitions in the pattern where K is the value programmed in PAT_LEN. These whole set of K transitions will be repeated G number of times where G is the GBL_REP_NUM. The PAT_LEN takes a value of 0-2032 (the first and second word is for T/R Switch, third word cannot be used as explained in Step 3 and one more word is used for storing the PAT_LEN & GBL_REP_NUM, so effectively, the rest 508 words can be used for actually defining the transitions. As explained below, each word can store 4 transitions so we can have a total of 508*4 = 2032 transitions).
- **Step 5**: Each byte from the next register word onwards is treated as type LVL_PER. The 5 MSB bitsin LVL_PER byte is treated as PERIOD and 3 LSBs as LEVEL. Allowed value for PERIOD is 0 to 31 and for LEVEL it is 0 to 7. Pattern generator reads these and generates the control signal for the pulser based on LEVEL as shown in Table 7-6. This control signal is kept in the same state for (PERIOD + 1) number of DIG_CLK cycles.

Note

Two consecutive periods should not be programmed as 0, that is, Two consecutive levels cannot have a period of 1 DIG_CLK cycle. If programmed in that way, the Pulser can transmit an unexpected pattern which can possible draw very high current. If a particular period corresponding to its level is programmed as 0, the minimum value for the next period is 1.

Table 7-6. LEVEL Definition

LEVEL (Bits)	EN_Hn	EN_Ln	EN_RTZ_n	Pulser Output
000	0	0	0	HiZ
001	1	0	0	AVDDP_HV
100	0	0	1	Ground
101	0	1	0	AVDDM_HV
Others	X	X	X	DO NOT USE

- Step 5 continues till the number of transitions read by the pattern generator is equal to the PAT_LEN programmed. After that, based on the GBL_REP_NUM programmed, the pattern generator either stops reading the memory or again starts reading from the first transition till the number of repetitions of the pattern is equal to the GBL_REP_NUM programmed.
- **Table 7-7. LEVEL Definition for Opposite Polarity**

LEVEL (Bits)	EN_Hn	EN_Ln	EN_RTZ_n	Pulser Output
000	0	0	0	HiZ

Table 7-7. LEVEL Definition for Opposite Polarity (continued)

LEVEL (Bits)	EN_Hn	EN_Ln	EN_RTZ_n	Pulser Output
001	0	1	0	AVDDM_HV
100	0	0	1	Ground
101	1	0	0	AVDDP_HV
Others	X	X	X	DO NOT USE

The operation of pattern generator is also explained using a flow chart as shown in Figure 7-14.

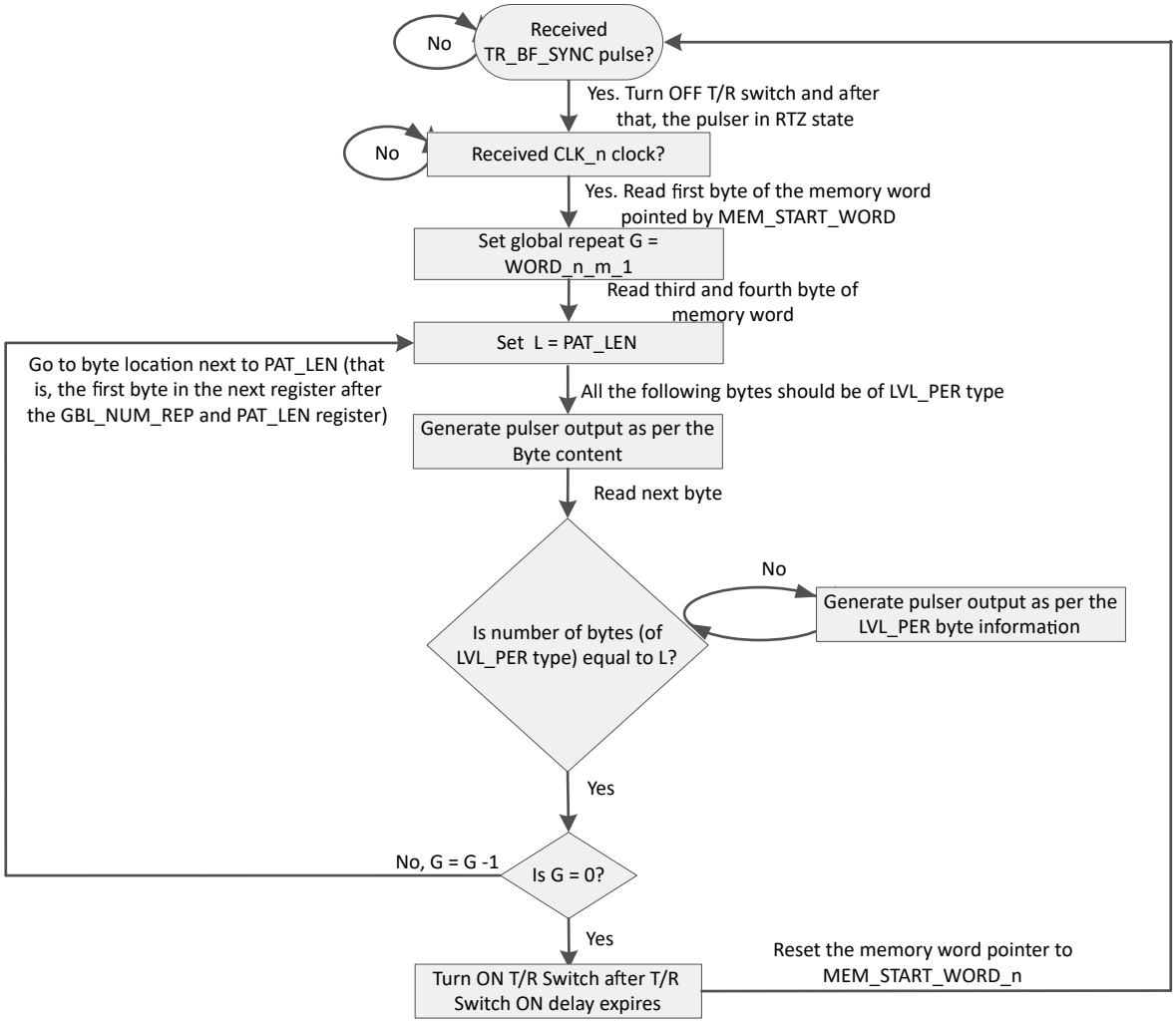


Figure 7-14. Pattern Generator Flow Chart

7.3.8.3.1.3 B-Mode Example Pattern

The expected pattern from pattern generator when pattern memory is programmed as per Table 7-8 and MEM_START_WORD_n = 31 is shown in Figure 7-15.

Table 7-8. Pattern Memory Content

SPI Address	Memory Word	Byte 4	Byte 3	Byte 2	Byte 1
159	31	PATTERN_LENGTH = 0x000E		XX	GBL_REP_NUM= 0x01

Table 7-8. Pattern Memory Content (continued)

SPI Address	Memory Word	Byte 4	Byte 3	Byte 2	Byte 1
160	32	LVL_PER= 0x19 Level = 001 (AVDDP_HV) Period = 3	LVL_PER= 0x0C Level = 100 (Ground) Period = 1	LVL_PER= 0x09 Level =001 (AVDDP_HV) Period = 1	LVL_PER= 0x0C Level= 100 (Ground) Period = 1
161	33	LVL_PER= 0x0C Level = 100 (Ground)Period = 1	LVL_PER = 0x0C Level = 100 (Ground) Period = 1	LVL_PER= 0x09 Level =001 (AVDDP_HV) Period = 1	LVL_PER= 0x0C Level= 100 (Ground) Period = 1
162	34	LVL_PER= 0x0C Level = 100 (Ground)Period = 1	LVL_PER= 0x1D Level = 101 (AVDDM_HV) Period = 3	LVL_PER= 0x0C Level =100 (Ground) Period = 1	LVL_PER= 0x0D Level= 101 (AVDDM_HV) Period = 1
163	35	XX	XX	LVL_PER= 0x0C Level =100 (Ground) Period = 1	LVL_PER= 0x0D Level= 101 (AVDDM_HV) Period = 1

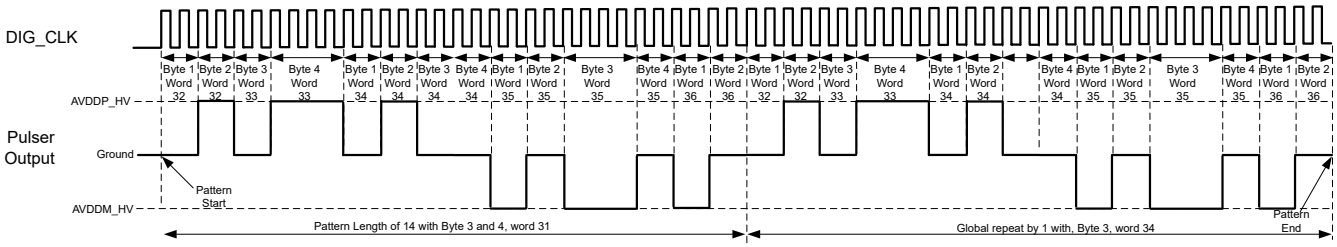


Figure 7-15. Example Pulser Output in B-mode

7.3.8.3.2 Pattern Generator Operation in Continuous Wave (CW) Mode

The block diagram of pattern generator in CW mode is shown in Figure 7-16. To enable CW mode in the device set register bit CW_EN = 1 and apply TR_BF_SYNC pulse.

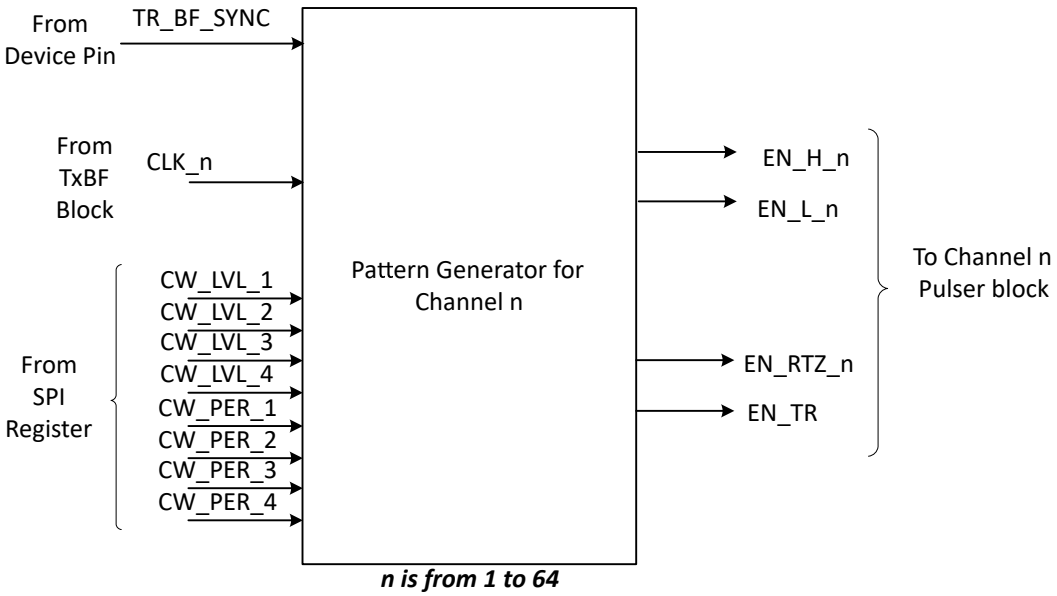


Figure 7-16. Pattern Generator in CW-mode

In CW mode, device generates a fixed output waveform independent of the value programmed in the pattern memory.By default, the T/R switch of all the channels are ON when CW mode is enabled and all the

channels get configured in receive mode. To configure any channel in transmit mode, disable the T/R switch of corresponding channel using register bit TR_SW_DIS_n. In CW mode:

- The transmit beamforming operation functionality does not change. It operates in same way for both B- and CW-mode.
- On receiving TR_BF_SYNC output goes to ground state after T/R switch is turned OFF and pattern generator wait for CLK_n clock signal.
- Once pattern generator block receives clock CLK_n from transmit beamformer block it starts transmitting the continuous waveform.
- The continuous waveform consists of total four programmable levels and period which shall be programmed using register bits CW_LVL_x and CW_PER_x (x -> 1 to 4); see Figure 7-17.
- The mapping of CW_LVL_x to pulser output is listed in Table 7-9.The output waveform stays in programmed level for CW_PER_x number of DIG_CLK_n clock periods. Here CW_PER_x can be programmed from 0 to 31.
- **Step to enable CW mode**:Set the register bit CW_EN to '1' and apply TR_BF_SYNC pulse. Device will start transmitting CW pattern on receiving TR_BF_SYNC trigger.
- **Step to disable CW mode**: Set the register bit CW_EN to '0' (When device is operating in CW mode, SPI operation is allowed when device is generating CW pulses) and apply TR_BF_SYNC pulse. Device will stop transmitting CW pattern on receiving TR_BF_SYNC trigger.

Table 7-9. CW_LVL_xmapping to Pulser Output

CW_LVL_x (Binary)	Pulser Output
000	Hi-Z
001	AVDDP_HV
100	Ground
101	AVDDM_HV
Others	DO NOT USE

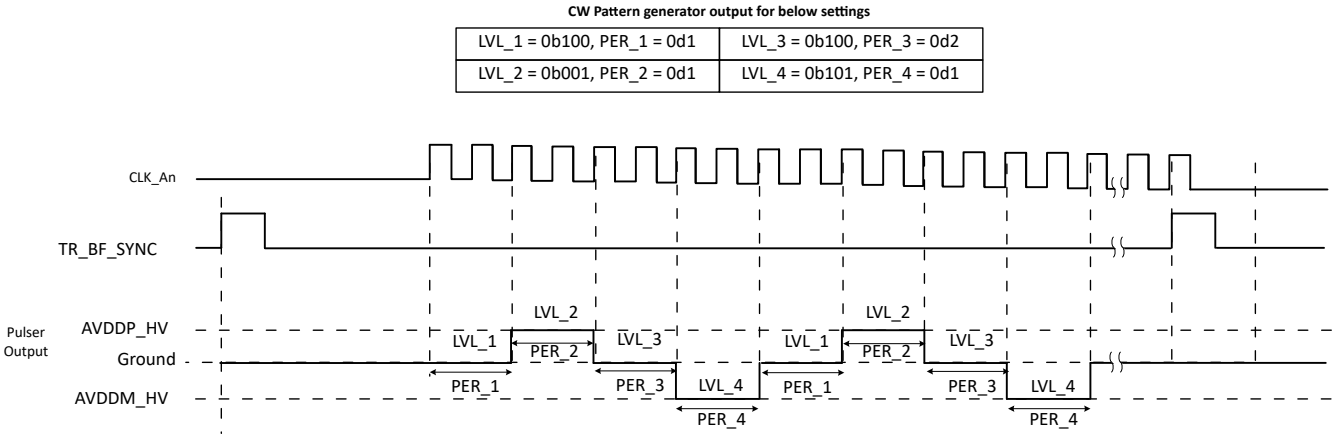


Figure 7-17. Example Pulser Output in CW-mode

7.3.8.3.3 T/R Switch Control Signal

Turning ON and OFF of T/R switch is associated with receive and transmit phases respectively. As mentioned before, the T/R Switch ON delays for a group of four channels in the memory is stored in the first two locations. See Section 7.3.6 for more details. In on-chip beamforming mode, control signals EN_TR_n (n from 1 to 64) controls the T/R switches for channels 1 to 64. These control signals are generated by the device per the following logic:

- **T/R switch turn OFF operation:** T/R switch of all the active channels starts to turn OFF as soon as TR_BF_SYNC pulse is applied. T/R switch starts to turn OFF whenever signal EN_TR_n goes low. EN_TR_n signals go to low after 30 DIG_CLK clock cycles after TR_BF_SYNC pulse is applied; see Figure 7-18.

- **T/R switch turn ON operation with respect to the end of its own pattern (TR_SW_GBL_MODE set to '0'):**Signals EN_TR_n for active channel n goes high after(4 × TR_SW_ON_DEL_n + 6) number of DIG_CLK clock cycles after end of corresponding channel n pattern.
- **T/R switch turn ON operation with respect to the end of pattern of all the channels (TR_SW_GBL_MODE set to '1'):** Signals EN_TR_n for active channel n goes high after (4 × TR_SW_ON_DEL_n+6)number of DIG_CLK clock cycles after end of pattern of all the 64 channels.
- **When device is programmed in CW mode:** Signals EN_TR_n is set to 1 always and enables the T/R switch of all the active channels. To disable the T/R switch of any channel permanently use the register bits TR_SW_DIS_n.

Note

Whenever T/R switch of any channel is in ON state, pulser of corresponding channel gets disabled automatically.

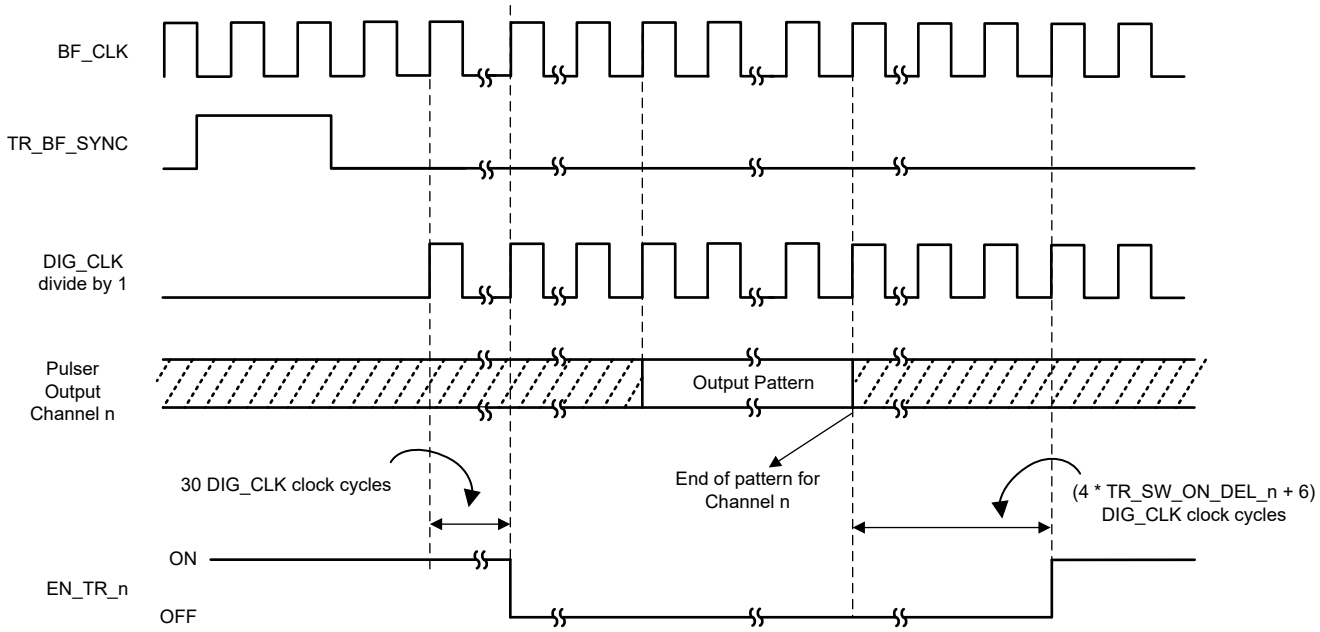


Figure 7-18. T/R Switch Control Signal for TR_SW_GBL_MODE = 0

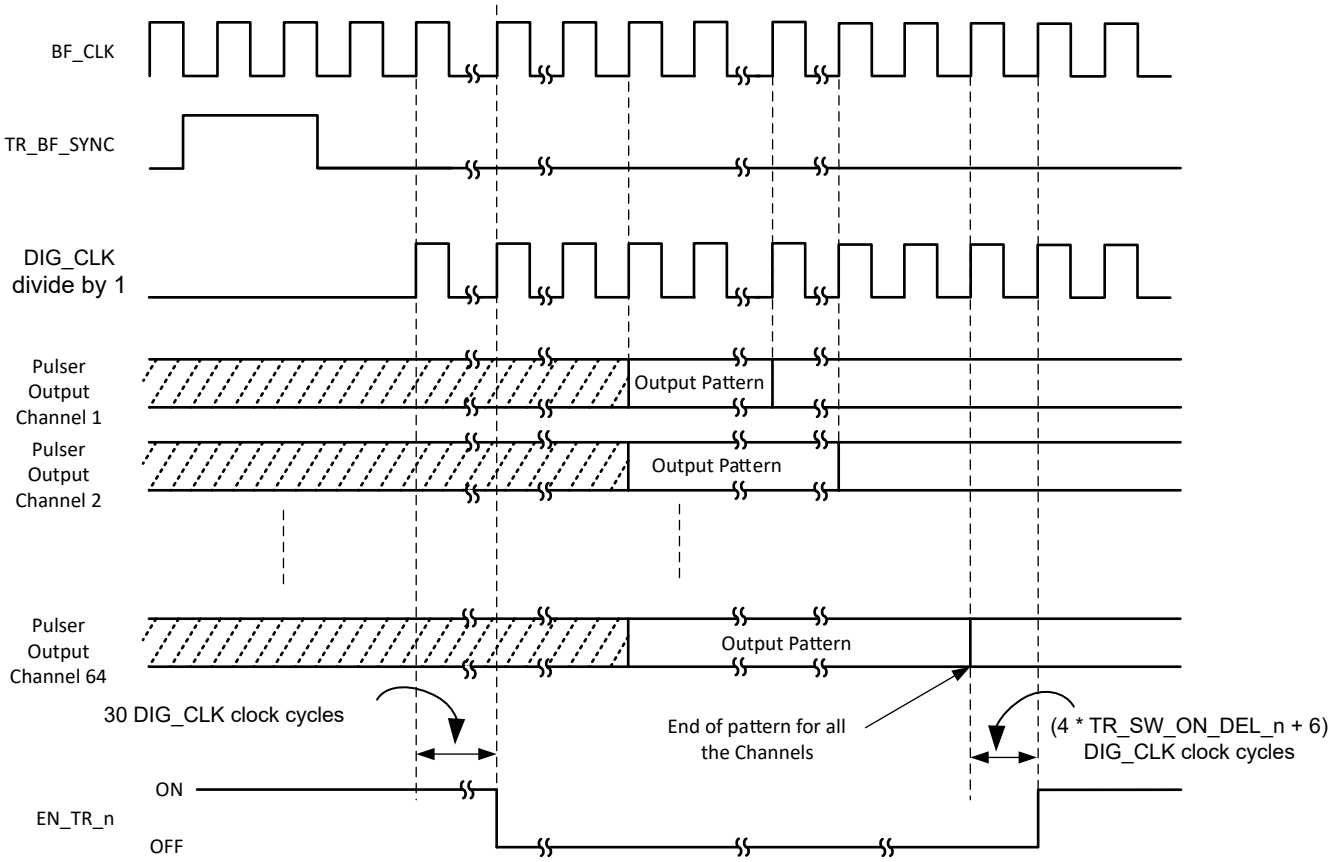


Figure 7-19. T/R Switch Control Signal for TR_SW_GBL_MODE = 1

7.3.8.3.3.1 Enabling and Disabling T/R Switch Permanently

Any of the 64 T/R switch can be turned ON or OFF permanently using the register bits TR_SW_EN_n and TR_SW_DIS_n (n is from 1 to 64).

Table 7-10. T/R Switch Control Logic

TR_SW_EN_n	TR_SW_DIS_ n	Series Switch	Shunt Switch	T/R Switch Status
0	0	Dynamic ON/OFF	Dynamic ON/OFF	T/R switch control signal generated as per the logic in pattern generator block.
0	1	OFF	OFF	T/R switch is disabled. Both the series and shunt switch are permanently OFF. Effect of TR_SW_DIS_n takes place on following TR_BF_SYNC pulse after enabling the TR_SW_DIS_n bit.
1	0	ON	OFF	T/R switch is enabled. Series switch is programmed in ON and shunt switch in OFF state permanently.
1	1	ON	OFF	T/R switch is enabled. Series switch is programmed in ON and shunt switch in OFF state permanently.

7.3.8.3.4 Read and Write of Channel Memory

The read and the write window timing of delay and pattern memory is shown in Figure 7-20. ‘Write’ refers to SPI write to either modifying the delay or pattern memory or changing the delay profile or start pointer of pattern memory, to be used for the next transmission window. ‘Read’ refers to the loading of selected profile from delay

memory into the TxBF and pattern memory in pattern generator blocks. It is important to take note of following points related to write and read operation of profile.

- Write operation of memory is not allowed when any channel of the device is transmitting except when device is operating in CW mode.
- Once profile content, BF_PROF_SEL_n, and pattern memory start pointer is programmed, the effect of it is reflected only in the next read window. For example, in Figure 7-20 if BF_PROF_SEL_n is changed in write window 1 then the new delay profile is loaded in read window 1 and used for the subsequent transmit cycle.

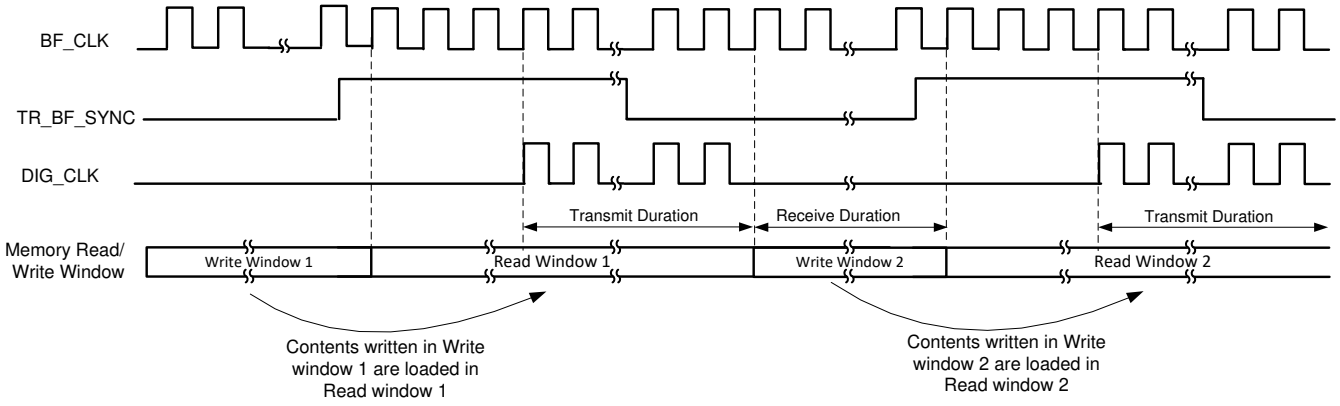


Figure 7-20. Read and Write Timing Window of Delay and Pattern Profile

7.3.9 Full Timing Diagram for On-chip Beamforming Mode

For quick reference different operations performed in the on-chip beamforming mode are summarized in Figure 7-21.

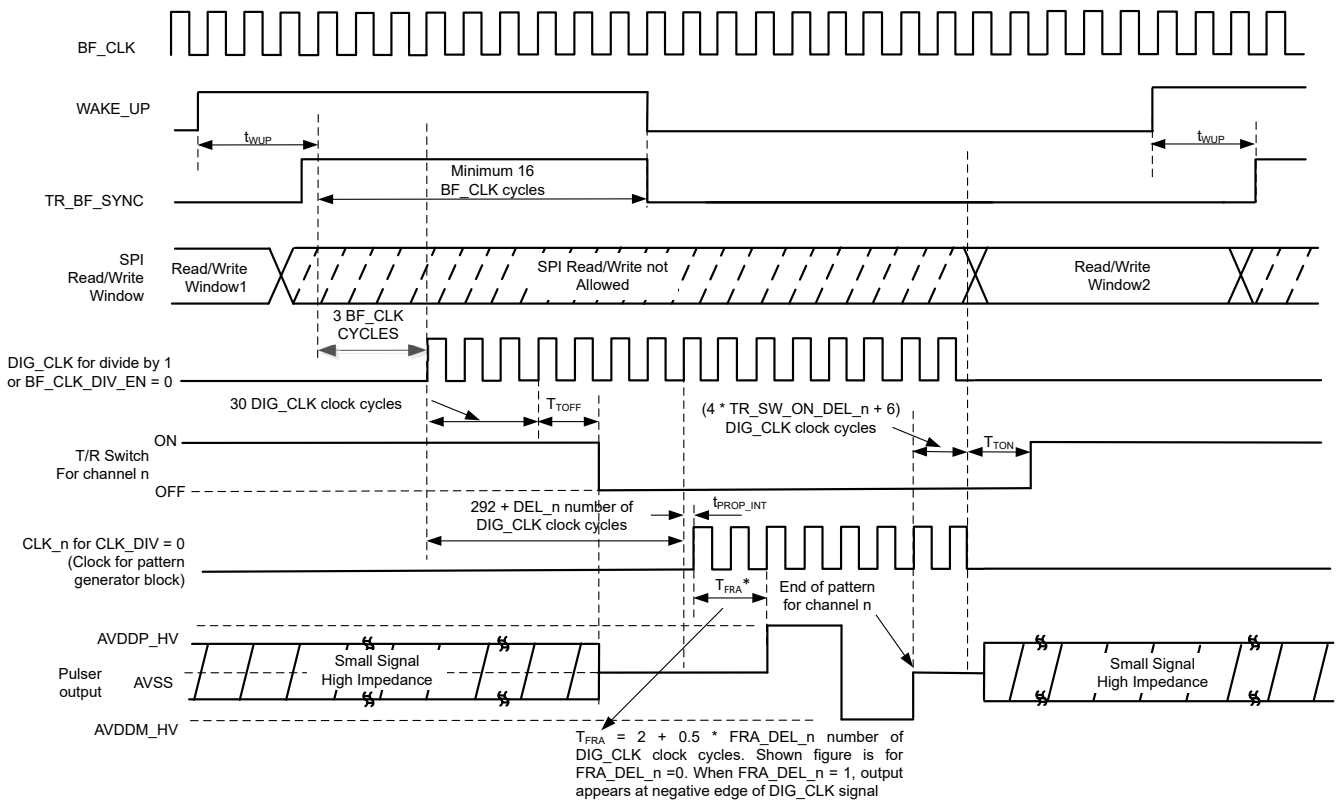


Figure 7-21. On-Chip Beamforming Operation

7.3.10 Temperature Sensor

Device has an integrated internal temperature sensor to facilitate the measurement of internal junction temperature.Temperature sensors works on clock driven from DIG_CLK clock signal. The clock frequency of temperature sensor is given by DIG_CLK/(4×N), where value of N can be programmed using register bit CLK_DIV_TSENSE; see Table 7-11. By adjusting CLK_DIV_TSENSE, make sure that the clock of temperature sensor is in range of 500 kHz to 3 MHz. Temperature sensor operation is independent of TR_BF_SYNC signal.

Table 7-11. Temperature Sensor Clock Division Factor

CLK_DIV_TSENSE	Value of Factor N
000	32
001	64
010	8
011	16
1XX	4

Follow below steps to read temperature from temperature sensor block:

1. Make sure that EN_DYN_PDN_CLKBUF and EN_CLK_GATE bits are set to 0.
2. Enable the temperature sensor reset by setting the TEMP_SENSE_EN bit to ‘1’. If it is already set to 1 then set it to 0 and back to 1.
3. After enabling, temperature sensor block takes 2048 clock cycles to measure the device temperature. Once temperature sensor finishes the temperature measurement, it sets the register bit READ_TEMP_VALID to ‘1’.
4. Read the READ_TEMP_VALID register bit. If it is set to '1' then temperature code T can be read using register READ_TEMP. READ_TEMP is 9-bit 2s complement code with value in range of -246 to 246.
5. For value of T read from READ_TEMP register, device temperature can be calculated using below formula:
   - Device temperature = -60.0 + (0.97 × T + 255)/2.45
6. To read the next temperature valueset the TEMP_SENSE_EN bit to ‘0’ and follow above steps again.

Temperature sensor supports continuous operation too. To read temperature in continuous mode, follow below steps:

1. Make sure that EN_DYN_PDN_CLKBUF and EN_CLK_GATE bits are set to 0.
2. Set CONT_TEMP_SENSE and TEMP_SENSE_EN bits to '1'.
3. After enabling the above bits, the temperature sensor block takes 2048 clock cycles to measure the device temperature. In continuous mode, TEMP_VALID is set to "1" by the device after the first temperature value isready to read. After that TEMP_VALID bit always remains "1" until the temperature sensor is disabled and enabled again.
4. Temperature code T can be read using register READ_TEMP. READ_TEMP is 9-bit 2s complement code with value in range of -246 to 246.
5. For value of T read from READ_TEMP register, device temperature can be calculated using below formula:
   - Device temperature = -60.0 + (0.97 × T + 255)/2.45
6. To read the next temperature value, repeat steps 4 and 5. Device will continuously update the temperature value after every 2048 DIG_CLK clocks.

In continuous mode operation, there is a small probability of the temperature value being incorrect. It can happen when the temperature sensor is updating the temperature value and at the same time the user tries to read the temperature. In that case there can be a clash in write and read operation and temperature value can come out incorrect. So, in case the temperature value comes out to be unexpected, it is recommended to read the value again to confirm.

7.3.11 Temperature Shut Down

The internal junction temperature of the device can be measured by using the temperature sensor block. However, to protect the device from thermal run away, 12 additional temperature shut down blocks areintegrated in the device and are active all of the time. The position of 12 thermal shut down blocks with respect to 64

channels are shown in Figure 7-22. Whenever the temperature of any thermal shutdown block crosses the threshold defined by the register bit TSHUT_TEMP (= 0 -> 105ºC, = 1 -> 125ºC), device enters to thermal shutdown. To determine which block out of the 12 thermal shutdown blocks triggered the device in thermal shutdown mode, read the error flag register bits TEMP_SHUT_ERR [11:0] post shutdown. To bring out the device from thermal shutdown mode, either set the register bit ERROR_RST to '1' or apply a hardware reset to the device. When device enters in thermal shutdown mode, floating LDOs are powered down, pulser is configured in return to zero state and T/R switch keeps operating as per user defined scenario.

Note

It is strongly recommended to use thermal shutdown threshold of 105ºC in elastography mode.

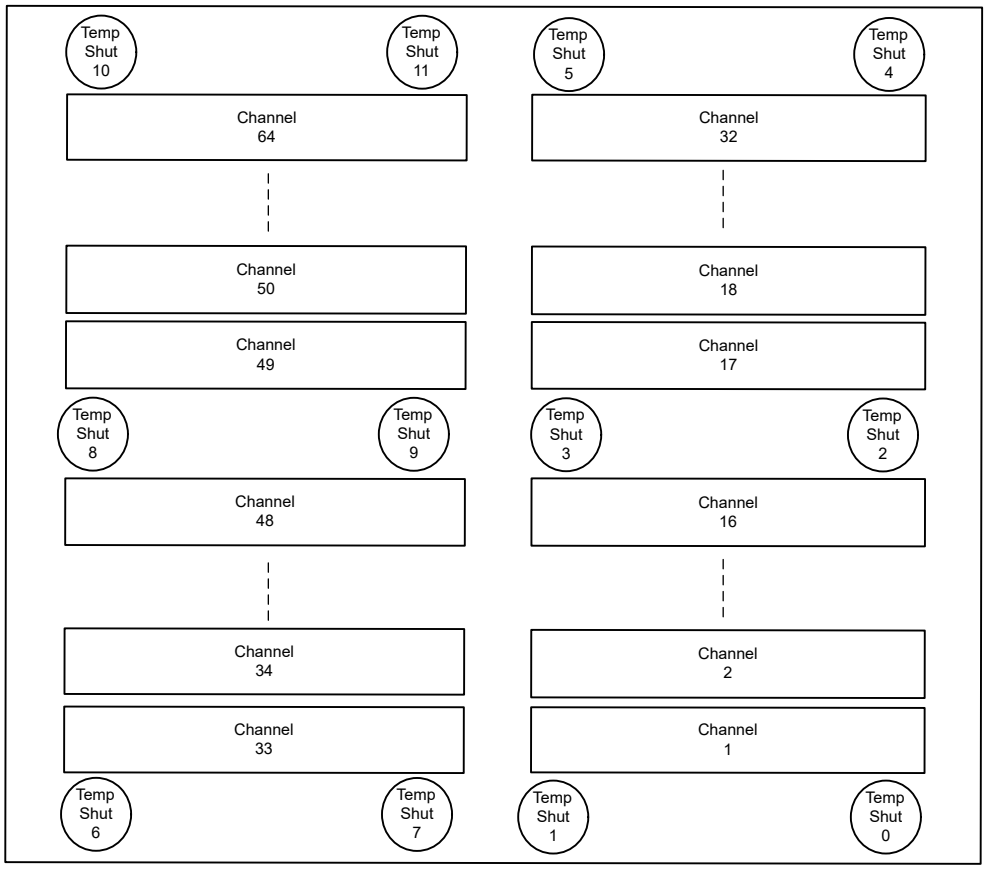


Figure 7-22. Temperature Shut Down Block Position in the Device

7.3.12 Error Flag Register

The device has capability to detect multiple abnormal situations, and to prevent the device damage, it automatically powers down the device and sets the TSHUT pin to high. Since there are multiple possible reasons for device going to shut down mode, user can read the error flag register to understand the exact reason of shut down. Description in following subsections explains the different and abnormal condition which can be detected by the device and the meaning of different register bit in error flag register. All the register bits get reset on hardware reset. Software reset does not clear any of the error register bit. Additionally, some of the bits can be reset by setting register bit ERROR _RST to ‘1’. Set the ERROR _RST bit to ‘1’ and back to ‘0’ to reset the error bits in errorflag register. Once all the error flag registers are reset, device starts working normally. Different error check condition can be enabled or disabled using specified register. On disabling the feature, error flag is still set by the device but device does not enter in shut down mode and does not set the TSHUT pin to high. When device enters in thermal shutdown mode, high voltage floating LDOs are powered down, pulser is configured in return to zero state and T/R switch is disabled. Once device is programmed to come out of thermal

shutdown mode, floating LDOs output voltage would have discharged. To charge it back, follow the LDO power up sequence explained in Section 7.3.5.

7.3.12.1 High Temperature Error (TEMP_SHUT_ERR [11:0])

Description: Device has total 12 thermal shut down blocks. Out of these 12 blocks, which block has triggered the thermal shut down can be identified by reading TEMP_SHUT_ERR [11:0] register bit, where n represents the thermal shut down block as shown in Figure 7-25.

Reset process: TEMP_SHUT_ERR [11:0] can be reset using both hardware reset and ERROR_RST bit.

Enable/Disable process: By default, device shut down due to high temperature is enabled. This feature can not be disabled.

7.3.12.2 No BF_CLK Clock Detect Error (NO_CLK_ERR)

Description: In default power mode if BF_CLK clock is not applied to the device when it is active or when the device is in dynamic clock power mode and BF_CLK clock is not applied for > 6µs when the device is in transmit mode, device enters to thermal shut down mode and the NO_CLK_ERR bit goes low. After device powers up or applies hardware reset, one TR_BF_SYNC pulse is needed to enable the clock detect feature.

Reset process: NO_CLK_ERR bit can be reset to 1 only using hardware reset.

Enable/Disable process: By default, no clock detect feature is enabled. This feature cannot be disabled.

7.3.12.3 Single Level for High Duration Error (SINGLE_LVL_ERR)

Description: If the pulser output remains in PHV or MHV level for N number of BF_CLK clock cycles then device enters to thermal shut down mode and the SINGLE_LVL_ERR bit goes high. Here N is decimal value of register LVL_DURATION.

Reset process: SINGLE_LVL_ERR bit can be reset using both hardware reset and ERROR_RST bit.

Enable/Disable process: By default, single level detect feature is enabled with LVL_DURATION set to maximum value. To disable this feature, set the register bit DIS_SINGLE_LVL_ERR to ‘1’.

7.3.12.4 Long Pattern Error (LONG_PAT_ERR)

Description: In pulser output if any of the channel makes more than (64 × N – 1) transition then device enters to thermal shut down mode and LONG_TRAN_ERR bit goes high. Here N is decimal value of register TRAN_COUNT and by transition it means to change the output from one level to another level. The long transition error detect feature is disabled in CW mode.

Reset process: LONG_TRAN_ERR bit can be reset using both hardware reset and ERROR_RST bit.

Enable/Disable process: By default, long transition detect feature is enabled with TRAN_COUNT set to value 1 that is 64 transitions. To disable this feature set the register bit DIS_LONG_TRAN_ERR to ‘1’.

7.3.12.5 AVDDP_5 Supply Error (P5V_SUP_ERR)

Description: If AVDDP_5 supply voltage magnitude goes lower than 4.5 V then device enters to thermal shut downmode and P5V_SUP_ERR bit goes high. All the registers in the global register map, except the error flag register, reset after AVDDP_5 supply drops below 4.5 V. So, after the device enters in AVDDP_5 supply error, registers in the global register map required to be re-configured after AVDDP_5 supply is back in standard operating range. Above is true even if, this error mode is disabled using DIS_P5V_SUP_ERR.

Reset process: P5V_SUP_ERR bit can be reset using both hardware reset and ERROR_RST bit.

Enable/Disable process: By default, AVDDP_5 supply detect feature is enabled. To disable this feature set the register bit DIS_ P5V_SUP_ERR to ‘1’.

7.3.12.6 AVDDP_HV Supply Range Error (PHV_RANGE_ERR)

Description: If AVDDP_HV supply level goes out of voltage range defined using register PHV_L and PHV_H then device enters to thermal shut down mode and PHV_ RANGE bit goes high.

Reset process: After the device goes to shut down because of supply range error then either apply hardwarereset or follow below steps:

1. Set PHV_L to 0 and PHV_H to 15.
2. Bring the device out of thermal shut down by setting ERROR_RST to ‘1’ and back to ‘0’.
3. Set the supply range to desired value using PHV_L and PHV_H bits.
4. If AVDDP_HV supply value is out of the intended supply range then device will again enter to thermal shutdown.

Enable/Disable process: By default, AVDDP_HV supply range detect feature is disabled. To enable this feature follow below steps:

1. Set PHV_L to 0 and PHV_H to 15.
2. Enable the supply range detect feature by setting register bit EN_PHV_RANGE_ERR to ‘1’.
3. Set the supply range to the desired values using PHV_L and PHV_H bits.
4. If AVDDP_HV supply value is out of the intended supply range then device will enter to thermal shutdown.

Table 7-12. PHV_L Register Value to Supply Level Mapping

PHV_L	AVDDP_HV Supply level (in V) below which device will go to thermal shutdown
0	Noshutdown based on supply range
1	6.25
2	12.5
3	18.75
4	25
5	31.25
6	37.5
7	43.75
8	50
9	56.25
10	62.5
11	68.75
12	75
13	81.25
14	87.5
15	93.75

Table 7-13. PHV_H Register Value to Supply Level Mapping

PHV_H	AVDDP_HV Supply level (in V) above which device will go to thermal shutdown
0	0
1	12.5
2	18.75
3	25
4	31.25
5	37.5
6	43.75
7	50
8	56.25
9	62.5
10	68.75
11	75
12	81.25

Table 7-13. PHV_H Register Value to Supply Level Mapping (continued)

PHV_H	AVDDP_HV Supply level (in V) above which device will go to thermal shutdown
13	87.5
14	93.75
15	No shutdown based on supply range

7.3.12.7 TR_BF_SYNC Error (TRIG_ERR)

Description: If TR_BF_SYNC trigger is accidentally applied when the device is still in transmit duration then device enters in shut down mode and set the register bit TRIG_ERR to ‘1’.

Reset process: TRIG_ERRbit can be reset using both hardware reset and by applying TR_BF_SYNC pulse.

Enable/Disable process: Trigger error feature is enabled by default. To disable the feature set the register bit DIS_TRIG_ERR to ‘1’.

7.3.12.8 Error Flag Read Error (VALID_FLAG)

In case the supply AVDDP_5 and AVDDM_5 is not within the allowed range, SDOUT read itself will fail. To check if SDOUT is working correctly or not, first read the VALID_FLAG_n (n = 1 to 5) bits. If the read value matches with the value provided in the reg map section, then SDOUT data is valid otherwise either AVDDP_5 or AVDDM_5 supply is not up.

7.3.12.9 STANDBY Flag (STDBY_FLAG)

Description: If the external PDN input to the device is set to logic ‘1’, the device will be in a PDN Mode and will not be transmitting or receiving and will set the STDBY_FLAG bit to ‘1’. However, this will not set the TSHUT pin high as it is based on the user input on the STDBY pin.

Reset process: De-assert the PDN input to the device (pull it to logic ‘0’) in order to clear the STDBY_FLAG bit.

Enable/Disable process: The Standby flag error is enabled by default. This feature cannot be disabled.

7.3.12.10 Flag Register Summary and Precautions

All the error flag register bits are summarized in Table 7-14.

Table 7-14. Error Flag Register Summary

S. No.	Error Register Bit	Description	Reset using ERROR_RST bit?	Disabled/Enabled bit
1	TEMP_SHUT_ERR [11:0]	High Temperature Error	Yes	Always enabled
2	NO_CLK_ERR	No BF_CLK Clock Detect Error	No	Always enabled
3	SINGLE_LVL_ERR	Single Level for High Duration Error	Yes	DIS_SINGLE_LVL_ERR
4	LONG_TRAN_ERR	Long Transition Error	Yes	DIS_LONG_TRAN_ERR
5	P5V_SUP_ERR	AVDDP_5 Supply Error	Yes	DIS_P5V_SUP_ERR
6	M5V_SUP_ERR	AVDDM_5 Supply Error	Yes	DIS_M5V_SUP_ERR
7	PHV_RANGE_ERR	AVDDP_HV Supply Range Error	Yes	EN_PHV_RANGE_ERR
8	TRIG_ERR	TR_BF_SYNC Error	No. However it can be reset by applying TR_BF_SYNC pulse.	DIS_TRIG_ERR
9	VALID_FLAG	Check register read validity	NA	NA
10	STDBY_FLAG	PDN Pin status of device	No	Always enabled

Note

Post hardware reset, if there are no error flags raised, the following values can be read from the registers as below:

1. Register 29 (in decimal) should read 0x4FFC00.
2. Register 77(in decimal) should read 0xA8000000.
3. Register 98(in decimal) should read 0x58000000.
4. Register 108(in decimal) should read 0xB0010000.
5. Register 120(in decimal) should read 0xC8000000.
6. Register 78(in decimal) should read 0x50000000.

Whenever user observes TSHUT pin going high, follow steps given in Table 7-15 to narrow down the possible issue.

Table 7-15. Steps to Locate the Error

Step	Step Description	Possible Error
1	TheAVDDP_1P8 supply voltage has to be within the specified limits for error register bits to be valid. If AVDD_1P8 supply dips more than the allowed range then error flag register information can corrupt.	Device cannot detect if AVDD_1P8 supply is not correct. It has to be ensured by the system.
2	Read the VALID_FLAG_n bits.	If the readout matches with the values provided in the reg map section, then go to next step. If it shows any other value then either AVDDP_5 supply or AVDDM_5 supply is less than |4.5|V.
3	Check P5V_SUP_ERR bit	If P5V_SUP_ERR error bit is '1' then first fix the AVDDP_5 supply. The rest of flag bits won't be valid if P5V_SUP_ERR bit goes '1'. If P5V_SUP_ERR error bit is '0' then go to next step.
4	Check M5V_SUP_ERR bit	If M5V_SUP_ERR error bit is '1' then first fix the AVDDM_5 supply. The rest of flag bits are not valid if M5V_SUP_ERR bit goes '1'. If P5V_SUP_ERR error bit is '0' then go to next step.
5	Read other error bits	Debug the system based on which error flag bit goes to '1'

7.3.12.11 HD2 System Level Optimization

The HD2 performance of the pulser output is optimized during the device production. However, the HD2 performance is function of the load connected to the pulser output therefore in the system with real probe,device can give different HD2 performance. To optimize the HD2 performance further with real probe, device offers two trim registers using which slope and duty cycle can be adjusted. All the trim bits are common for all the 64 channels.

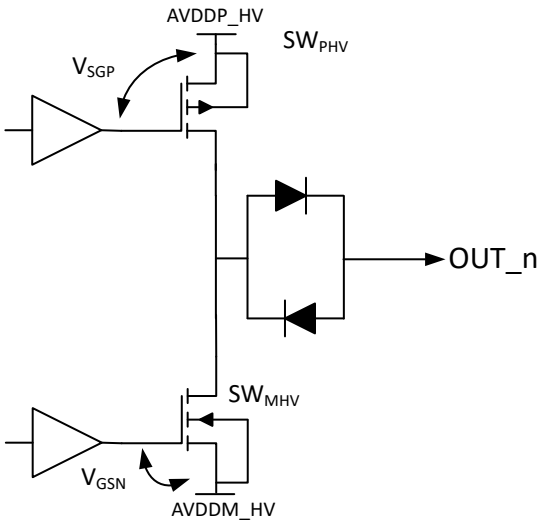


Figure 7-23. Pulser Output Stage

7.3.12.11.1 Vgs Trim

Vgs of output transistors SW_{PHV} and SW_{MHV} are trimmed in production and can be adjusted further using PHV1_FL, PHV2_FL, MHV1_FL, and MHV2_FL register bits; see Table 7-16. The effect of Vgs trim is shown in Figure 7-24. Increasing the Vgs of transistor increases its current drive and reducing Vgs reduces the current drive. This trim helps in increasing the slope for HV supply greater than 30 V. Table 7-16 lists the change in Vgs and corresponding increasing current drive.

Table 7-16. Vgs Trim Registers Mapping

PHV1_FL, PHV2_FL, MHV1_FL, and MHV2_FL register bits	Typical change in current drive of SW_{PHV}, SW_{MHV}switches.(1)
000	Default
001	-2%
010	-4%
011	-6%
100	-8%
101	-10%
110	-12%
111	-14%

(1) Data represents typical change in Vgs and current drive. The change in Vgs and current drive can vary from device to device.

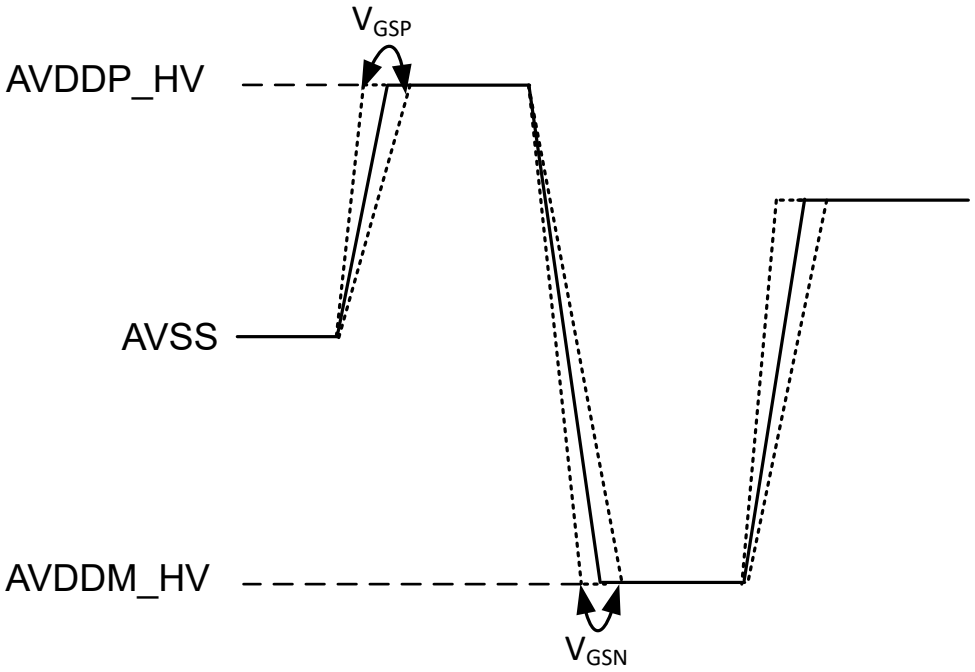


Figure 7-24. Vgs Trim

7.3.12.11.2 Transistor ON Delay Trim

Inthe pulser output waveform,different turn ON instant T_{PHV_ON}, T_{MHV_ON}, T_{PRTZ_ON}, and T_{NRTZ_ON} as shown in Figure 7-25 can be adjusted independently using register bit T_PHV_ON, T_MHV_ON, T_PRTZ_ON, and T_NRTZ_ON registers respectively. Table 7-17 shows

Table 7-17. Two-trim Registers Mapping

Delay Trim Registers	Delay Value
00	Default
01	+350 ps
10	+700 ps
11	1 ns

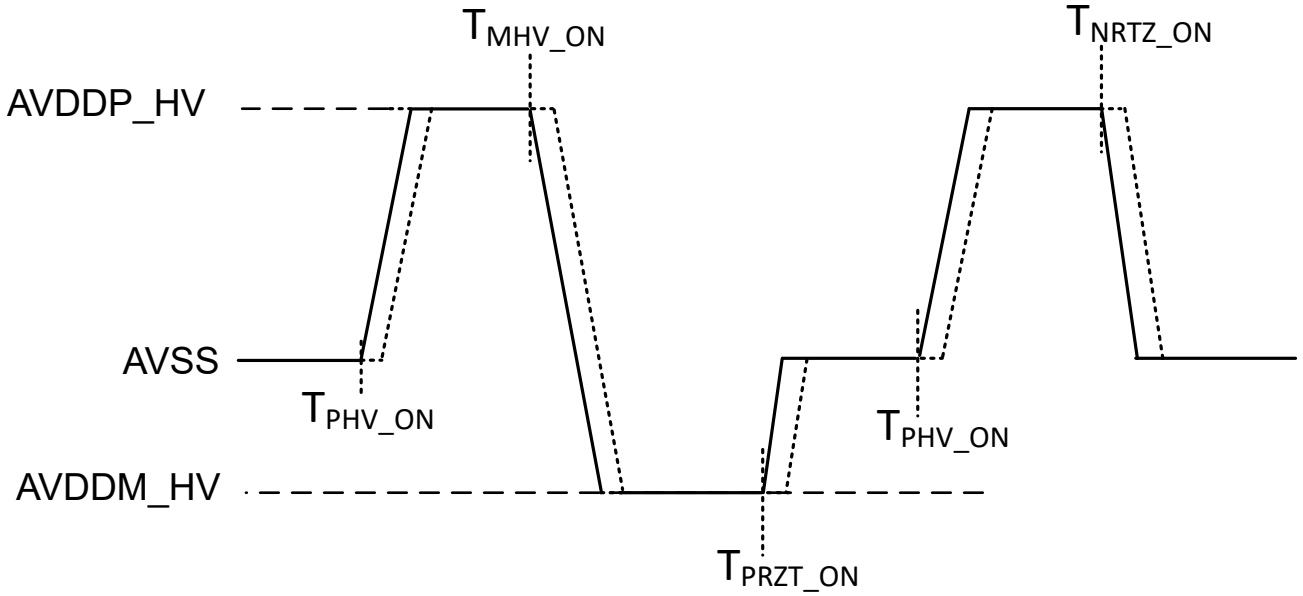


Figure 7-25. ON Delay Trim

7.3.12.11.3 Transistor OFF Delay Trim

In the pulser output waveform, before turning ON the transistor of next transition, the transistor of previous transition is turned OFF to avoid any through current. Adjusting the turn ON delay trim can increase non-overlap time. To compensate it turn OFF delay trim can be used to adjust the non-overlap time. Different turn OFFinstant T_PHV_OFF, T_MHV_OFF, T_PRTZ_OFF, and T_NRTZ_OFF as shown in Table 7-18 can be adjusted independently using register bit T_PHV_OFF, T_MHV_OFF, T_PRTZ_OFF, and T_NRTZ_OFF registers respectively. Figure 7-26 shows delay trim register bit combination to delay value mapping.

Table 7-18. Two-trim Registers Mapping

Delay Trim Registers	Delay Value
00	Default
01	+350 ps
10	+700 ps
11	1 ns

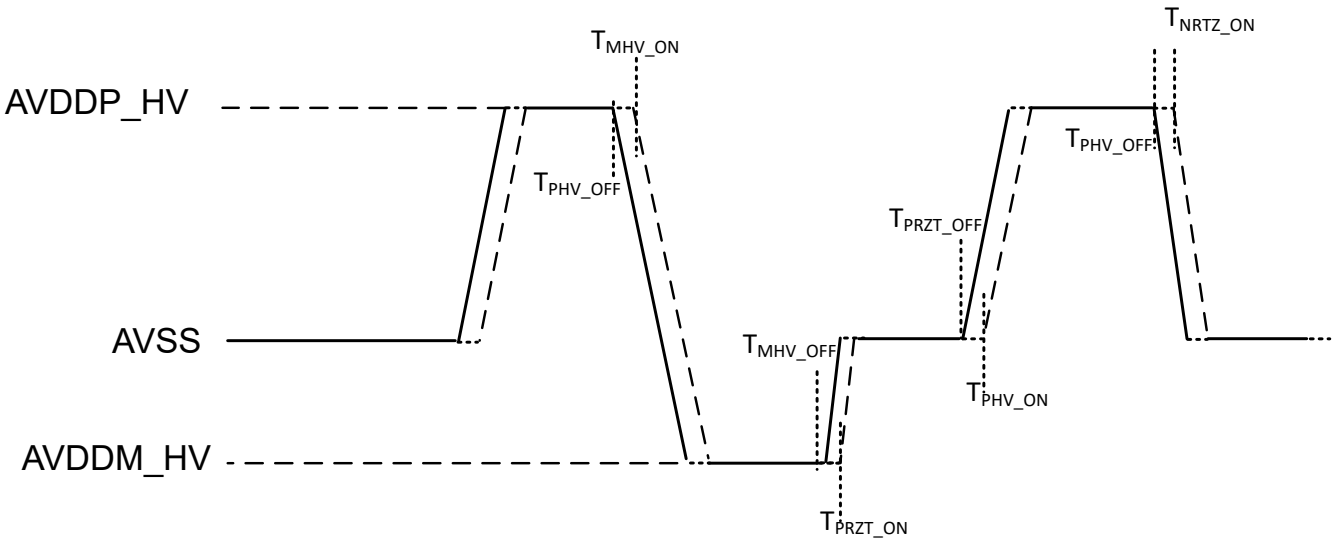


Figure 7-26. OFF Delay Trim

7.4 Device Functional Modes

7.4.1 Dynamic SPI Mode

To reduce the device power in receive mode and when SPI operation is not being performed, LVDS buffer for SPI signals can be powered down. To enable this mode set EN_DYN_PDN_SPIBUF to ‘1’. Enabling this bit will reduce1.8-V supply current, when WAKE_UP signal is ‘0’, by around 6mA giving power saving of 1.8 × 6 mA = 10.8 mW per device. When dynamic SPI mode is enabled, SPI buffers get power up when WAKE_UP signal is set to logic level ‘1’ and powers down when WAKE_UP signal is set to ‘0’. After setting WAKE_UP signal to ‘1’, wait for 1 µs before starting SPI write or read operation.

7.4.2 Dynamic Clock Power Mode

To reduce digital power of the device in B-mode operation, the BF_CLK buffer, TR_BF_SYNC buffer and clock going to digital can be switched off during receive duration. For example, when T/R switch is ON. To enable dynamic clock power mode set the register bit EN_CLK_GATE and EN_DYN_PDN_CLKBUF to '1'. After setting these bits to '1', device automatically powers down the BF_CLK and TR_BF_SYNC buffer when T/R switch of all the channels in the device turn ON and powers it back on receiving WAKE_UP signal. Other than the lower power (Only AVDD_1P8 supply current reduces on programming the device from default power to dynamic clock power mode), there is no change in the device operation between default power mode and dynamic clock power mode.

7.4.3 Pulser Power Down

In on-chip beam forming mode device support a feature to power down the individual pulser using a register bit. To power down any pulser, use register bit PDN_PUL_n (n-> 1 to 64). On enabling the pulser power down bit, the pulser output goes to return to zero state on next TR_BF_SYNC pulse while T/R switch of corresponding channel remains active.

7.4.4 Invert Pattern

In on-chip beam forming mode, output signal level of any pulser shall be inverted by just enabling a bit PAT_INV_CH_n (n -> 1 to 64). Table 7-19 lists down pulser output level with and without invert pattern mode. This bit eases the use of the device in harmonic imaging where inverted pulse is required.

7.4.5 Global Power Down

To global power down the device set register bit PDN_GBL to '1'. During global power down mode all thepulsers, floating LDOs, BF_CLK buffer and TR_BF_SYNC buffers are powered down. The T/R switch remains in the state as per the user programmed configuration. Since in global power down floating LDOs are powered down hence after disabling global power down mode, floating LDOs also needs to be powered up if global power down duration was more than 100 ms using suggestion given in Section 7.3.4.

7.4.6 STANDBY Mode

In addition to the Global Power down, the device also has a PDN pin which functions as an input. By making this pin logic ‘1’, the device is placed in a PDN Mode where all the pulsers, floating LDOs are powered down. No SPI operation is needed for this as this a pin-based control. Since floating LDOs are powered downhence after disabling global power down mode, floating LDOs also needs to be powered up if global power down duration was more than 100 ms using suggestion given in Section 7.3.4.

Table 7-19. Invert Pattern

PULSER OUTPUT WITH PAT_INV_n = 0	PULSER OUTPUT WITH PAT_INV_n = 1
AVDDP_HV	AVDDM_HV
AVDDM_HV	AVDDP_HV
AVSS	AVSS

7.5 Programming

The Serial Programming Interface (SPI) block supports LVDS mode of operation with write speeds up to 400 Mbps per lane in differential input mode and 50 Mbps in single ended mode to program the device. This interface consists of input/output pins named as SCLK, SDATA_0, SDATA_1, SEN, SDOUT, EN_CRC and CRC_ERR. The interface supports:

1. Single and dual lane mode: In single lane mode SDATA_0 is used to send register data to program all the internalregisters. In dual lane mode both SDATA_0 and SDATA_1 are used to send register data to program internal register. Dual lane mode reduces the programming time of the device to half.
2. Register readout: Read out of internal register is done through the output data pin SDOUT.
3. SPI programming error check: The interface also supports a 32-bit CRC to detect bit errors while programming the device. To enable this feature set EN_CRC to logic level ‘1’. CRC_ERR pin is used to flag the error in programming. After toggling EN_CRC pin, that is, going from 0 to 1 or 1 to 0, it is required to apply hardware reset to the device before proceeding with SPI operation.

7.5.1 SPI Signal Input Buffer

SPI input signals SCLK, SDATA_0/1 and SEN are used to program the device. These signal support both differential input (sine wave, LVPECL, or LVDS) and CMOS mode.

7.5.1.1 Differential Input Mode

To configure the SPI buffer in differential input mode set SPI_MODE pin to '0'. The equivalent circuit of SPI signals input buffer in differential mode is shown in Figure 7-27. SPI input buffers support programmable internal termination. Refer to Recommended Operating Conditions for supported variation in R_{SPI_TERM} resistance value. In case resistance variation leads to signal integrity issues in the system then one can use external termination and internal termination can be disabled by programming SPI_TERM to "01". Table 7-20 lists the typical resistance values of R_{SPI_TERM} for different combination of register bits. The input signal to SPI buffers should be DC coupled. SCLK, SDATA and SEN buffer input termination value can be programmed independently using SPI registers SCLK_TERM, SEN_TERM and SDATA_TERM. Default termination value of all the buffers are kept as 400 Ω.

Table 7-20. SPI Buffer Input Termination Programmability

SCLK_TERM/SEN_TERM/ SDATA_TERM	R_{SPI_TERM} Value in ohms
00	400
01	HighZ
10	100
11	200

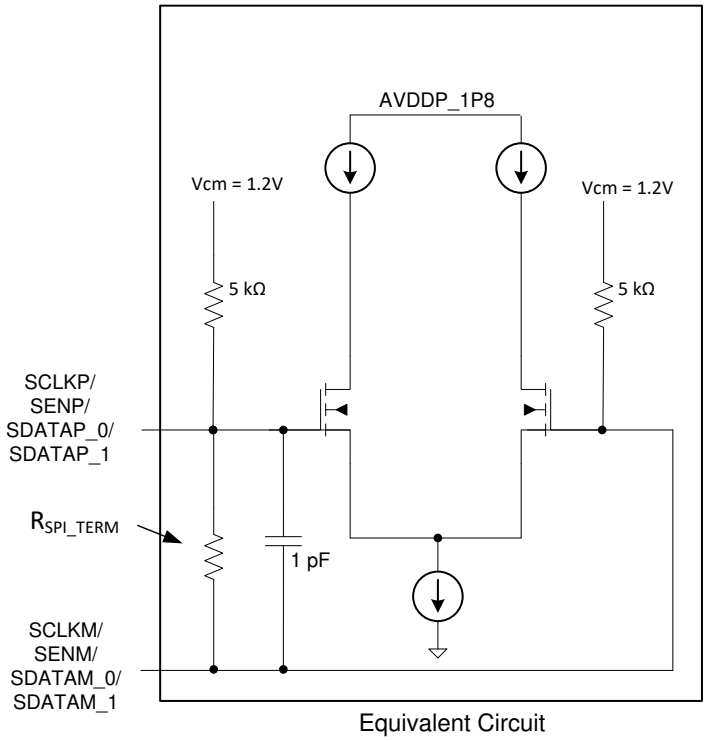


Figure 7-27. SPI Buffer for Differential Input Mode

7.5.1.2 Single Ended Input Mode

To configure the SPI buffer in single ended input mode set SPI_MODE pin to logic level '1'. The equivalent circuit of SPI signals input buffer in single ended mode is shown in Figure 7-28. Connect negative input pin to AVSS.

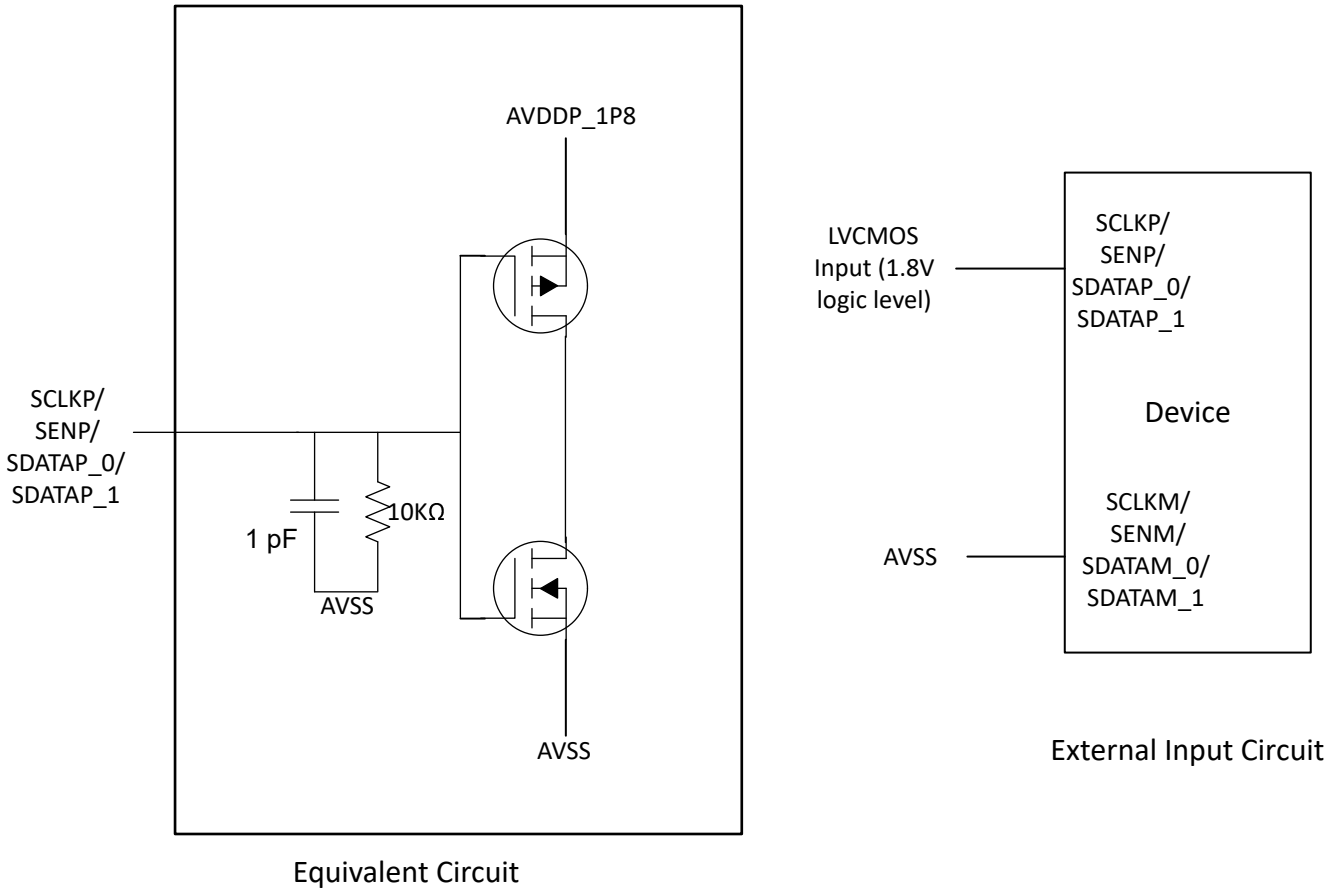


Figure 7-28. SPI Buffer for Single Ended Input Mode

7.6 SPI Write Operation

This interface is formed by the SEN, SCLK, SDATA_0, and SDATA_1 pins. Serially incoming bits on pin SDATA_0 and SDATA_1 are latched by the device on every SCLK rising edge when SEN is low. SDATA_0 and SDATA_1 serial data are loaded into the register for total 44 SCLK rising edge when SEN is low. If the word length exceeds a multiple of 44 bits, the excess bits are ignored. Data can be loaded in multiples of 44-bit words within a single active SEN pulse (an internal counter counts the number of 44 clock groups after the SEN falling edge). Data are divided into three portions: dummy bits (2 bits, need to be kept to 0), the address bits (10 bits) and data (32 bits). The timingdiagram for serial interface write operation is shown below. Figure 7-29 shows the timing diagram for serial interface write operation.

Note

It is recommended to avoid SPI read and write operation while transmitting high voltage pulses.

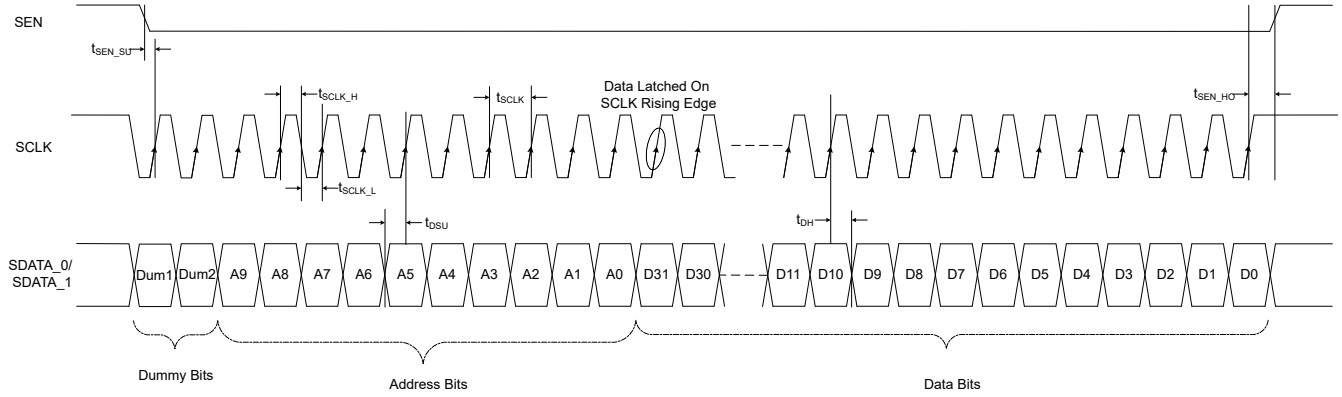


Figure 7-29. Serial Interface Timing

SPI write operation can be carried out in two possible ways as described below:

1. Single lane mode: Only single serial data line is used to program the device. Use SDATA_0 pin to send serial data and connect SDATA_1 to logic level '0'.
2. Double lane mode: Both the serial data lanes SDATA_0 and SDATA_1 are used to program the device. Internal to the device, data from 2 SPI lanes will be written sequentially into the register space. That is, if SDATA_0 has been used to program address 128 and SDATA_1 to program 256, then address 128 in register space is updated first followed by address 256. If both SDATA_0 and SDATA_1 are used to program the same address location, then data from SDATA_1 will overwrite the targeted address in the register space.

Note

Register 0 can only be programmed via SDATA_0 lane and any data on SDATA_1 while programming register 0 is ignored. It is advised to keep SDATA_1 to ‘0’ while programming register 0 via SDATA_0. If only SDATA_0 is used for programming the device then it is recommended to power down the SDATA_1 buffer using register bit PDN_SDATA_1 bit.

7.7 Burst Write Mode

To reduce total device programming time, device supports an extra write mode referred to as burst write mode. To enable burst write mode set register bit BURST_WR_EN to '1'. When burst write mode is enabled, it is required to send the register address only once after the SEN goes low. After the SEN goes low, keep SEN continually low and send only data bits. Device automatically increments the address by one after receiving each set of 32 bits and write the next 32 register bit on incremented register address; see Figure 7-30. In the burst write mode, once the auto incremented address reaches the maximum address (639) then SEN needs to be pulledhigh and start the SPI write operation again. In double lane mode the burst write length must be same for both the lanes. Burst mode is supported only for page register map. Global register map does not support burst-write mode.

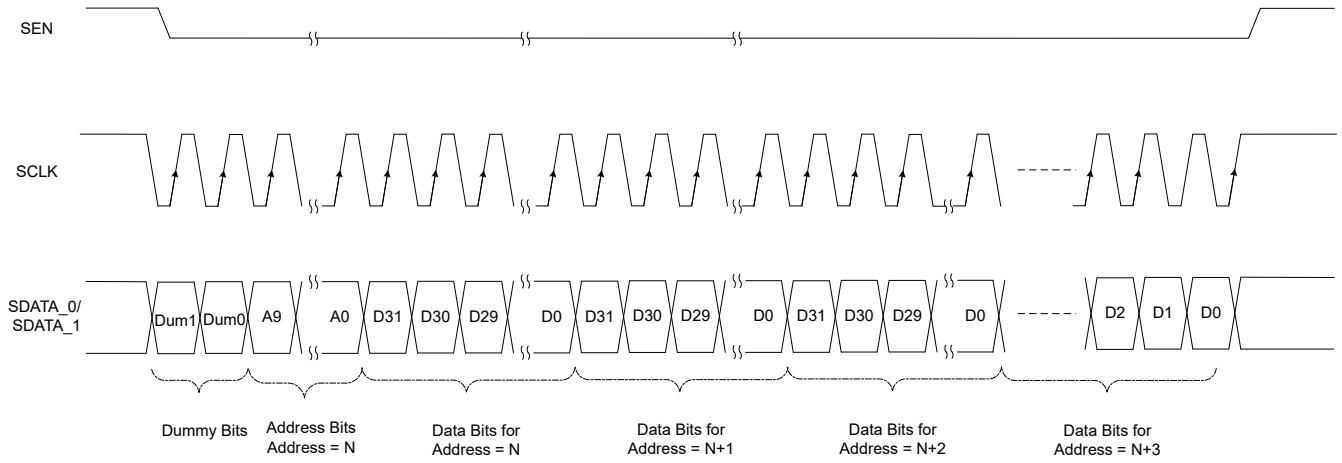


Figure 7-30. Burst Write Mode

7.8 Register Readout

The device includes an option where contents of the internal registers can be read back. This read back feature can be useful as a diagnostic test to verify the serial interface communication between the external controller and thedevice. To read the register, set READ_EN bit to '1'. To read the content of any address user need to provide the register data with same address two times by keeping SEN low. Say, to read the data corresponding to any address X, the device expects the 2-bit dummy data (need to be kept to 0), 10-bit address X, followed by 32-bit dummy data, followed by 2-bit dummy data (need to be kept to 0) & 10-bit address X again on SDATA_0. After this the device gives out the data on SDOUT serially on every fall edge of SCLK for next 32 SCLKs. Read operation timing diagram is shown in Figure 7-31. SDOUT has a delay of t_{OUT_DV} from the SCLK falling edge. To enable serial register, write again, set the READ_EN bit back to "0". Device SDOUT buffer gets enabled only during the time when register data is being send out by the device. SDOUT pins from multiple devices can be tied together without any pull-up resistors.

Device also supports burst read mode where addresses need to be repeated. In burst read mode keep the SEN pin always low. First send the address of first register followed by the address of second register and so on. Many register addresses can be given in sequence except last register address has to be repeated. Device will send out the register data of first register in next SPI data packet followed by second register data and so on. See Figure 7-32. The register content of global register map except address 0 and all the 17 SPI pages can be read through register read out feature. Register content of only one page can be read at a time.

In normal read mode

- Sayserial data applied on SDATA pin is Dummy (keep to 0) + Address 1 (12 bits) -> Data1 (32 bits) -> Dummy (keep to 0) +Address 1 (12 bits) -> Data2 (32 bits). Here Address 1 is the address of the register, data of which has to be read and Data1, Data2 is dummy data.
- Dataon SDOUT -> Duration when Data2 is fed in on SDATA pin, SDOUT gives out data corresponds to Address 1.

In burst read mode

- Say serial data applied on SDATA pin is in below sequence. Here Address*n* represents the position of data that has to be read and Data*n* are dummy data. Here Address 1 to Address 5 can be any addresses (Need to be continuous) in a given page.
  - Dummy (keep to 0) + Address 1(12 bits)
  - Data1(32 bits)
  - Dummy (keep to 0) + Address 2(12 bits)
  - Data2(32 bits)
  - Dummy (keep to 0) + Address 3(12 bits)
  - Data3(32 bits)
  - Dummy (keep to 0) + Address 4(12 bits)

  - Data4(32 bits)
  - Dummy (keep to 0)+ Address 5(12 bits)
  - Data5 (32 bits)
  - Dummy (keep to 0)+ Address5 (12 bits) (Repeated two times as this is the last address in the burst mode)
  - Data6 (32 bits)
- Dataon SDOUT ->
  - Duration when Data2 is fed in on SDATA pin, SDOUT gives out data corresponds to Address 1.
  - Duration when Data3 is fed in on SDATA pin, SDOUT gives out data corresponds to Address 2.
  - Duration when Data4 is fed in on SDATA pin, SDOUT gives out data corresponds to Address 3.
  - Duration when Data5 is fed in on SDATA pin, SDOUT gives out data corresponds to Address 4.
  - Duration when Data6 is fed in on SDATA pin, SDOUT gives out data corresponds to Address 5.

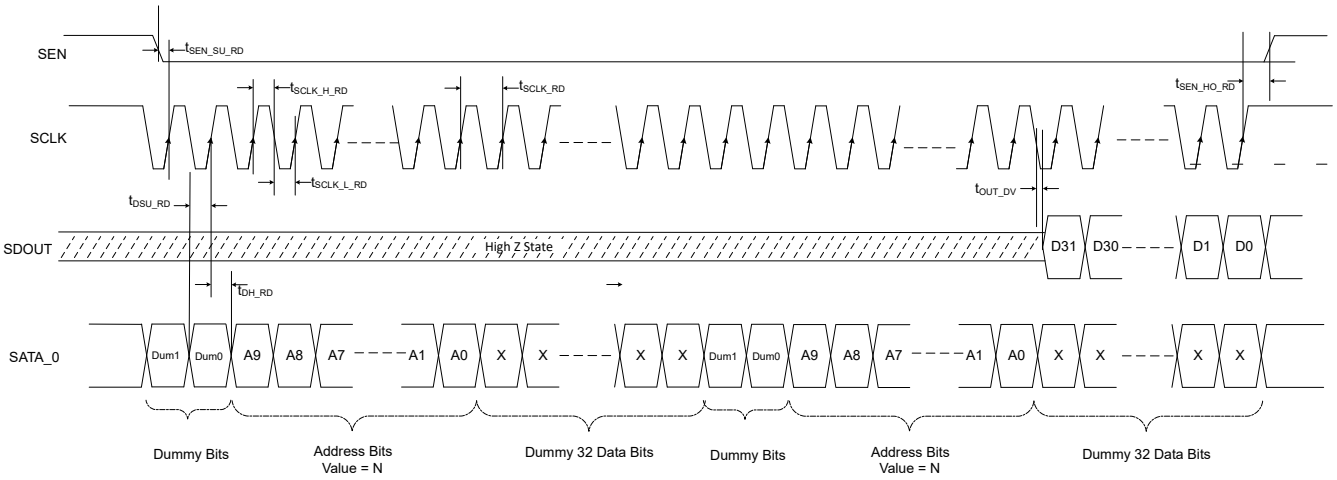


Figure 7-31. Serial Interface Register, Read Operation

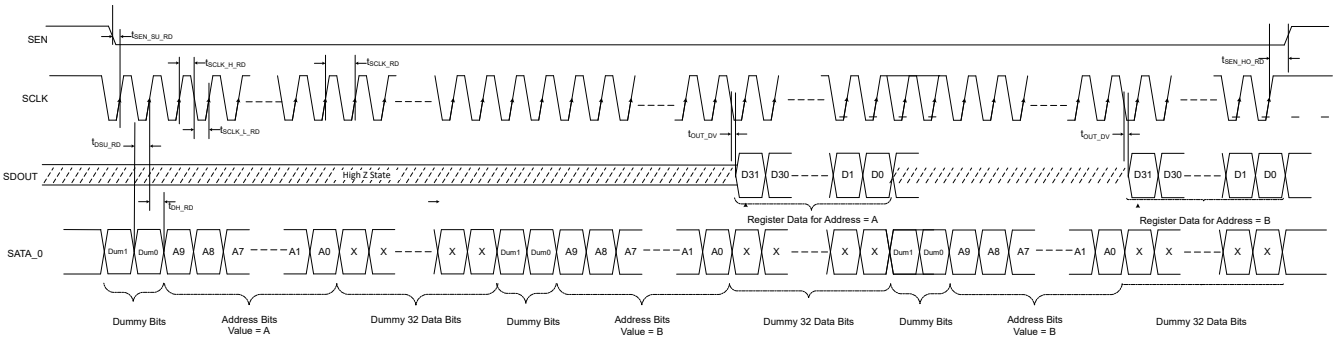


Figure 7-32. Serial Interface Register, Burst Read Operation

7.9 SPI Programming Window

The SPI programming is not allowed until all channels go into receive mode after applying the TR_BF_SYNC pulse; see Figure 7-33. Not complying to this requirement will lead to abnormal behavior from device. In CW mode SPI operation is allowed while device is transmitting CW signals.

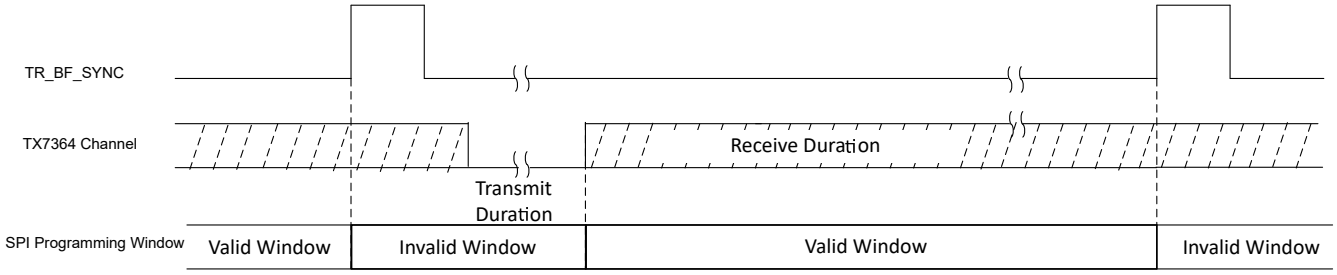


Figure 7-33. SPI Programming Valid Window

7.10 Register Programming Error Check

Serial programming can be prone to bit errors at very high transfer rates because of signal integrity or jitter and maylead to unwanted transmit patterns. A 32-bit cyclic redundancy check (CRC) is computed in the device on the serial data applied for both the data lanes individually (SDATA_0 and SDATA_1) and is compared with CRC code provided by the user on corresponding lane to detect such bit errors. To enable the CRC check feature in the device set EN_CRC pin to '1'. After toggling EN_CRC pin, that is, going from 0 to 1 or 1 to 0, it is required to apply hardware reset to the device before proceeding with SPI operation. Device calculates the 32-bit CRC code for comparison at the end of every SPI transaction, for example. after every rise edge of ‘SEN’. The internal calculated CRC code is compared with the code provided by the user on next 32 SCLK edges after SEN signal goes high. When the received code from the user matches with the device computed CRC, the output pin CRC_ERR remains in high-z state. When computed CRC code does not match the receive CRC code, the CRC_ERR pin and TSHUT pin goes high and device enters into shut down mode. To bring out device from shut down state apply RESET and start the programming of device again.

7.11 CRC Code Calculation

The device computes the CRC code via polynomial division (modulo 2). The polynomial division (modulo 2) is similarto the arithmetic division except that subtraction is replaced by ‘xor’ operation. The 33-bit polynomial used is as per ieee 802.3 crc32 polynomial standard as follows:

x32+ x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x1+ x0

In normal SPI write mode one SPI packet includes chip select, address and data bits (Total 44 bits). The 44 bit data is appended with 32 0s and then divided by 33-bit polynomial and the resultant CRC code is the 32-bit remainder generated from the polynomial division. Example CRC computation:

If the below address and data are transmitted into the device

- A0:12’h 000
- D0: 32’h 0000 4010

The serial bit stream corresponding to the above address and data would be 76‘h000_00004010_00000000

Dividing the above bit stream with 33-bit polynomial would result in 32’h 0D57B73C as the resultant CRC code

In case user writes multiple registers by keeping SEN signal low then CRC is computed on serial bit stream formed by cascading all the address and data bits and appending 32 0s in last. The resultant stream is then divided by 33-bit polynomial. The resultant CRC code is the 32-bit remainder generated from the polynomial division. Example CRC computation:

If the following two addresses and data are transmitted by keeping SEN low:

- A0:12’h 000
- D0: 32’h 0000 4010
- A1: 12’h036
- D1: 32’h 804A 1E68

The serial bit stream corresponding to the above address and data would be 120‘h000_00004010_036_804A1E68_00000000

Dividing the above bit stream with 33-bit polynomial would result in 32'h3F932897 as the resultant CRC code.

In case user writes registers in burst mode then CRC is computed on serial bit stream formed by cascading first address bits and all the data bits and appending 32 0s in last. The resultant stream is then divided by 33-bit polynomial. The resultant CRC code is the 32-bit remainder generated from the polynomial division. Example CRC computation:

If the following two addresses and data are transmitted by keeping SEN low:

- A0:12'h 000
- D0: 32'h 0000 4010
- D1: 32'h 804A 1E68
- D2: 32'h A0FF 1E6F

The serial bit stream corresponding to the above address and data would be 140'h000_00004010_804A1E68_A0FF1E6F_00000000

Dividing the above bit stream with 33-bit polynomial would result in 32'h C5E046AF as the resultant CRC code.

During SPI read operation with CRC mode enabled, CRC code is calculated in same as write mode. CRC code is calculated from all the address and dummy data bits applied on SDATA line.

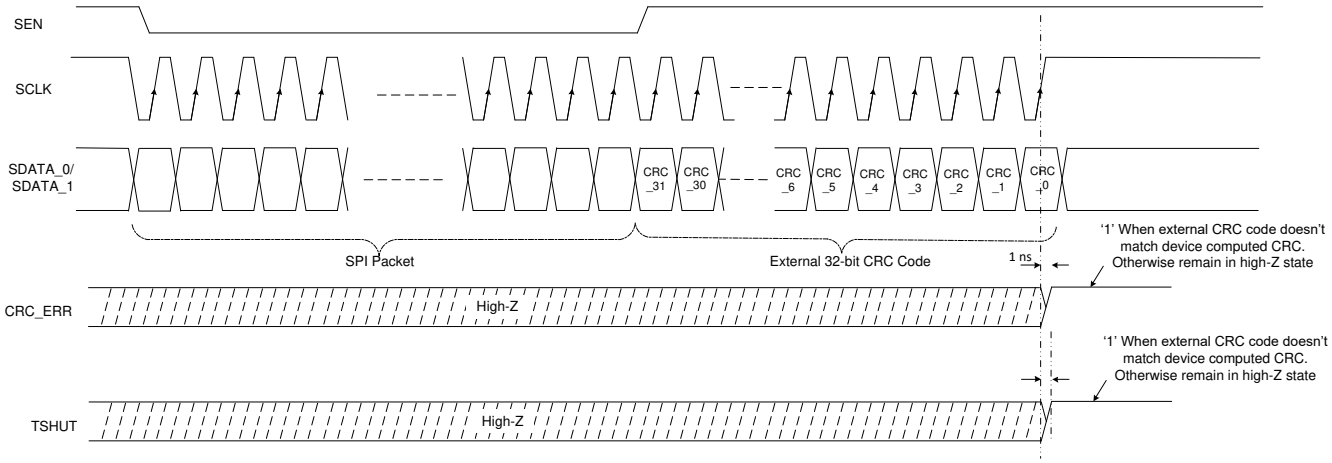


Figure 7-34. Register Programming Error Check Timing Diagram

8 Register Map

The register map of the device is divided into two categories as below. Also see Figure 8-1:

1. Global register map: Register addresses between 0 to 127 correspond to the global register. These registers define the global setting of the device.
2. Page register map: Pattern memory of channels 1 to 64 are part of page register map. There are total 16 different pages with address range between 128 to 639 for pattern memory (one for set of 4 channels). There are 16 different pages named as PAGE_1 to PAGE_16. During SPI write, the page that gets programmed is controlled by page select register in global register map. There are two page select registers for data lane SDATA_0 and SDATA_1.

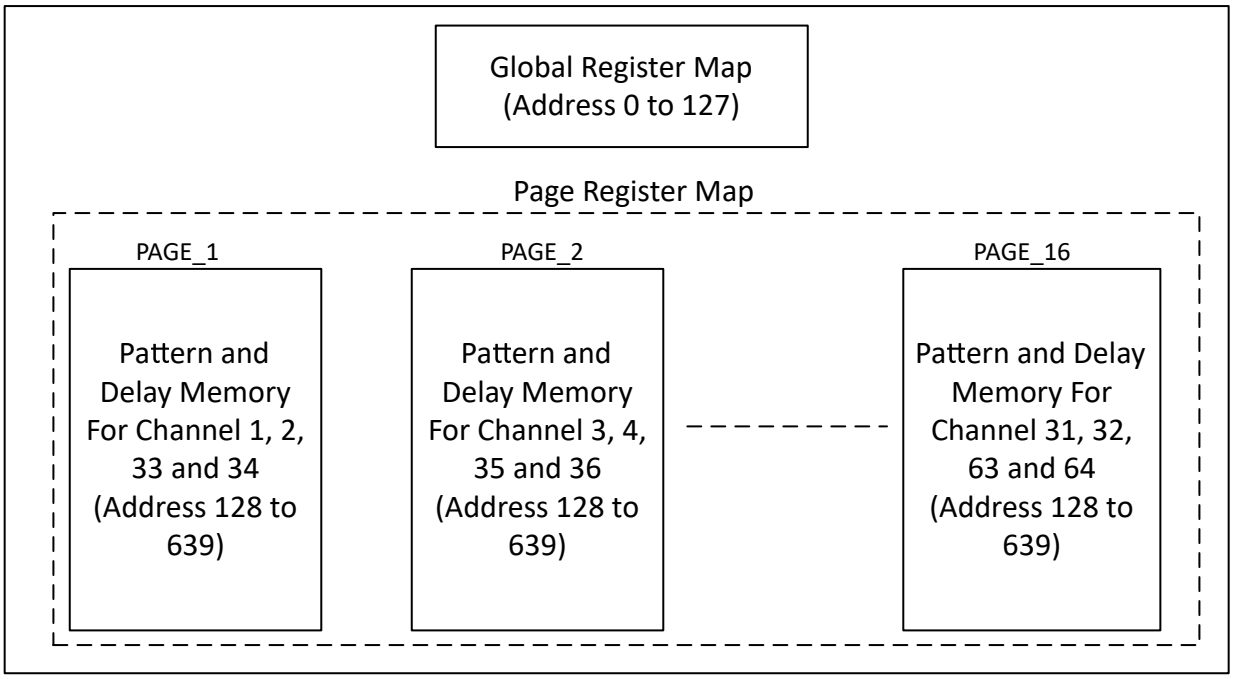


Figure 8-1. Register Map Diagram

8.1 Serial Interface Register Map

Figure 8-2. GBL_PAGE Register Map

ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
00h	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	0							BURST_WR_EN	0						READ_EN	RESET
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
02h	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
02h	PAGE_16_EN_0	PAGE_15_EN_0	PAGE_14_EN_0	PAGE_13_EN_0	PAGE_12_EN_0	PAGE_11_EN_0	PAGE_10_EN_0	PAGE_9_EN_0	PAGE_8_EN_0	PAGE_7_EN_0	PAGE_6_EN_0	PAGE_5_EN_0	PAGE_4_EN_0	PAGE_3_EN_0	PAGE_2_EN_0	PAGE_1_EN_0
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
03h	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
03h	PAGE_16_EN_1	PAGE_15_EN_1	PAGE_14_EN_1	PAGE_13_EN_1	PAGE_12_EN_1	PAGE_11_EN_1	PAGE_10_EN_1	PAGE_9_EN_1	PAGE_8_EN_1	PAGE_7_EN_1	PAGE_6_EN_1	PAGE_5_EN_1	PAGE_4_EN_1	PAGE_3_EN_1	PAGE_2_EN_1	PAGE_1_EN_1
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
09h	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
09h	0															PDN_GBL
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0Bh	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0Bh	CLK_DIV				0										EN_SYNC_DET	CW_EN
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0Ch	CW_PER_4					CW_LVL_4			CW_PER_3						CW_LVL_3	
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	CW_PER_2					CW_LVL_2			CW_PER_1						CW_LVL_1	
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0Dh	0							BF_PROF_SEL_2								
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	0							BF_PROF_SEL_1								
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0Eh	0							BF_PROF_SEL_4								
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0Eh	0							BF_PROF_SEL_3								
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0Fh	0							BF_PROF_SEL_6								
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0Fh	0							BF_PROF_SEL_5								
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
10h	0							BF_PROF_SEL_8								
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
10h	0							BF_PROF_SEL_7								
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
11h	0							BF_PROF_SEL_10								
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
11h	0							BF_PROF_SEL_9								
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
12h	0							BF_PROF_SEL_12								
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
12h	0							BF_PROF_SEL_11								
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
13h	0							BF_PROF_SEL_14								
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 8-2. GBL_PAGE Register Map (continued)

13h	0							BF_PROF_SEL_13								
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
14h	0							BF_PROF_SEL_16								
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
14h	0							BF_PROF_SEL_15								
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
16h	TR_SW_EN_64	TR_SW_EN_62	TR_SW_EN_60	TR_SW_EN_58	TR_SW_EN_56	TR_SW_EN_54	TR_SW_EN_52	TR_SW_EN_50	TR_SW_EN_48	TR_SW_EN_46	TR_SW_EN_44	TR_SW_EN_42	TR_SW_EN_40	TR_SW_EN_38	TR_SW_EN_36	TR_SW_EN_34
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16h	TR_SW_EN_32	TR_SW_EN_30	TR_SW_EN_28	TR_SW_EN_26	TR_SW_EN_24	TR_SW_EN_22	TR_SW_EN_20	TR_SW_EN_18	TR_SW_EN_16	TR_SW_EN_14	TR_SW_EN_12	TR_SW_EN_10	TR_SW_EN_8	TR_SW_EN_6	TR_SW_EN_4	TR_SW_EN_2
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
17h	TR_SW_EN_63	TR_SW_EN_61	TR_SW_EN_59	TR_SW_EN_57	TR_SW_EN_55	TR_SW_EN_53	TR_SW_EN_51	TR_SW_EN_49	TR_SW_EN_47	TR_SW_EN_45	TR_SW_EN_43	TR_SW_EN_41	TR_SW_EN_39	TR_SW_EN_37	TR_SW_EN_35	TR_SW_EN_33
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
17h	TR_SW_EN_31	TR_SW_EN_29	TR_SW_EN_27	TR_SW_EN_25	TR_SW_EN_23	TR_SW_EN_21	TR_SW_EN_19	TR_SW_EN_17	TR_SW_EN_15	TR_SW_EN_13	TR_SW_EN_11	TR_SW_EN_9	TR_SW_EN_7	TR_SW_EN_5	TR_SW_EN_3	TR_SW_EN_1
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
18h	TR_SW_DIS_64	TR_SW_DIS_62	TR_SW_DIS_60	TR_SW_DIS_58	TR_SW_DIS_56	TR_SW_DIS_54	TR_SW_DIS_52	TR_SW_DIS_50	TR_SW_DIS_48	TR_SW_DIS_46	TR_SW_DIS_44	TR_SW_DIS_42	TR_SW_DIS_40	TR_SW_DIS_38	TR_SW_DIS_36	TR_SW_DIS_34
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18h	TR_SW_DIS_32	TR_SW_DIS_30	TR_SW_DIS_28	TR_SW_DIS_26	TR_SW_DIS_24	TR_SW_DIS_22	TR_SW_DIS_20	TR_SW_DIS_18	TR_SW_DIS_16	TR_SW_DIS_14	TR_SW_DIS_12	TR_SW_DIS_10	TR_SW_DIS_8	TR_SW_DIS_6	TR_SW_DIS_4	TR_SW_DIS_2
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
19h	TR_SW_DIS_63	TR_SW_DIS_61	TR_SW_DIS_59	TR_SW_DIS_57	TR_SW_DIS_55	TR_SW_DIS_53	TR_SW_DIS_51	TR_SW_DIS_49	TR_SW_DIS_47	TR_SW_DIS_45	TR_SW_DIS_43	TR_SW_DIS_41	TR_SW_DIS_39	TR_SW_DIS_37	TR_SW_DIS_35	TR_SW_DIS_33
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
19h	TR_SW_DIS_31	TR_SW_DIS_29	TR_SW_DIS_27	TR_SW_DIS_25	TR_SW_DIS_23	TR_SW_DIS_21	TR_SW_DIS_19	TR_SW_DIS_17	TR_SW_DIS_15	TR_SW_DIS_13	TR_SW_DIS_11	TR_SW_DIS_9	TR_SW_DIS_7	TR_SW_DIS_5	TR_SW_DIS_3	TR_SW_DIS_1
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
1Bh	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1Bh	0															TR_SW_GBL_MODE
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
1Dh	TRAN_COUNT										0		LVL_DURATION			
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1Dh	LVL_DURATION						DIS_LONG_TRAN_ERR	DIS_SINGLE_LVL_ERR	0					LONG_TRAN_ERR	0	SINGLE_LVL_ERR
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
1Fh	0					TSHUT_TEMP	0									
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1Fh	0															
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
2Dh	PDN_PUL_64	PDN_PUL_62	PDN_PUL_60	PDN_PUL_58	PDN_PUL_56	PDN_PUL_54	PDN_PUL_52	PDN_PUL_50	PDN_PUL_48	PDN_PUL_46	PDN_PUL_44	PDN_PUL_42	PDN_PUL_40	PDN_PUL_38	PDN_PUL_36	PDN_PUL_34
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2Dh	PDN_PUL_32	PDN_PUL_30	PDN_PUL_28	PDN_PUL_26	PDN_PUL_24	PDN_PUL_22	PDN_PUL_20	PDN_PUL_18	PDN_PUL_16	PDN_PUL_14	PDN_PUL_12	PDN_PUL_10	PDN_PUL_8	PDN_PUL_6	PDN_PUL_4	PDN_PUL_2
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
2Eh	PDN_PUL_63	PDN_PUL_61	PDN_PUL_59	PDN_PUL_57	PDN_PUL_55	PDN_PUL_53	PDN_PUL_51	PDN_PUL_49	PDN_PUL_47	PDN_PUL_45	PDN_PUL_43	PDN_PUL_41	PDN_PUL_39	PDN_PUL_37	PDN_PUL_35	PDN_PUL_33
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2Eh	PDN_PUL_31	PDN_PUL_29	PDN_PUL_27	PDN_PUL_25	PDN_PUL_23	PDN_PUL_21	PDN_PUL_19	PDN_PUL_17	PDN_PUL_15	PDN_PUL_13	PDN_PUL_11	PDN_PUL_9	PDN_PUL_7	PDN_PUL_5	PDN_PUL_3	PDN_PUL_1
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
2Fh	PAT_INV_CH_64	PAT_INV_CH_62	PAT_INV_CH_60	PAT_INV_CH_58	PAT_INV_CH_56	PAT_INV_CH_54	PAT_INV_CH_52	PAT_INV_CH_50	PAT_INV_CH_48	PAT_INV_CH_46	PAT_INV_CH_44	PAT_INV_CH_42	PAT_INV_CH_40	PAT_INV_CH_38	PAT_INV_CH_36	PAT_INV_CH_34
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 8-2. GBL_PAGE Register Map (continued)

2Fh	PAT_INV_CH_32	PAT_INV_CH_30	PAT_INV_CH_28	PAT_INV_CH_26	PAT_INV_CH_24	PAT_INV_CH_22	PAT_INV_CH_20	PAT_INV_CH_18	PAT_INV_CH_16	PAT_INV_CH_14	PAT_INV_CH_12	PAT_INV_CH_10	PAT_INV_CH_8	PAT_INV_CH_6	PAT_INV_CH_4	PAT_INV_CH_2
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
30h	PAT_INV_CH_63	PAT_INV_CH_61	PAT_INV_CH_59	PAT_INV_CH_57	PAT_INV_CH_55	PAT_INV_CH_53	PAT_INV_CH_51	PAT_INV_CH_49	PAT_INV_CH_47	PAT_INV_CH_45	PAT_INV_CH_43	PAT_INV_CH_41	PAT_INV_CH_39	PAT_INV_CH_37	PAT_INV_CH_35	PAT_INV_CH_33
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
30h	PAT_INV_CH_31	PAT_INV_CH_29	PAT_INV_CH_27	PAT_INV_CH_25	PAT_INV_CH_23	PAT_INV_CH_21	PAT_INV_CH_19	PAT_INV_CH_17	PAT_INV_CH_15	PAT_INV_CH_13	PAT_INV_CH_11	PAT_INV_CH_9	PAT_INV_CH_7	PAT_INV_CH_5	PAT_INV_CH_3	PAT_INV_CH_1
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
33h	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
33h	0							MEM_START_WORD								
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
44h	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
44h	0		RED_MAX_CUR_M2		0									RED_MAX_CUR_P1		
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
4Dh	VALID_FLAG_1					0										ERROR_RST
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
4Dh	0										TEMP_SHUT_ERR[11:6]					
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
4Eh	VALID_FLAG_2					0	ARB2	0	ARB1	0						
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
4Eh	PHV_RANGE_ERR	0									M5V_SUP_ERR	P5V_SUP_ERR	0			
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
4Fh	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
4Fh	0								PHV_L				PHV_H			
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
51h	0										DIS_M5V_SUP_ERR	DIS_P5V_SUP_ERR	0	CONST_2	0	CONST_1
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
51h	0			EN_PHV_RANGE_ERR	0											
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
56h	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
56h	0												PDN_FLOAT_PHV_2	PDN_FLOAT_PHV_1	PDN_FLOAT_MHV_2	PDN_FLOAT_MHV_1
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
57h	0				T_NRTZ_ON		T_PRTZ_ON		T_MHV2_ON		T_MHV1_ON		T_PHV2_ON		T_PHV1_ON	
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
57h	0				MHV_2_FL			MHV_1_FL			PHV_2_FL			PHV_1_FL		
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
58h	0				T_NRTZ_OFF		T_PRTZ_OFF		T_MHV2_OFF		T_MHV1_OFF		T_PHV2_OFF		T_PHV1_OFF	
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
58h	0															
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
5Ch	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
5Ch	0			DIS_DYN_PDN_LDO	0											
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
5Fh	0															

Figure 8-2. GBL_PAGE Register Map (continued)

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
5Fh	0													RTZ_DRIVE	0	LOW_GLITCH_MODE
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
62h	VALID_FLAG_3					0										
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
62h	0										TEMP_SHUT_ERR[5:0]					
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
64h	0												CONT_TEMP_SENSE	CLK_DIV_TSENSE		
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
64h	0		READ_TEMP_VALID	READ_TEMP									0		TEMP_SENSE_RESET	TEMP_SENSE_EN
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
66h	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
66h	0			RED_MAX_CUR_P2			0									
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
67h	0													RED_MAX_CUR_M1		
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
67h	0															
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
6Ch	VALID_FLAG_4					0										NO_CLK_ERR
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
6Ch	0												PDN_SDATA_1	0		
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
6Eh	0													EN_DYN_PDN_SPIBUF	EN_DYN_PDN_CLKBUF	EN_CLK_GATE
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
6Eh	0						CLK_TERM		0		SYNC_TERM		BF_CLK_DIV_EN	0	BF_CLK_DIV	
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
6Fh	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
6Fh	SDATA_TERM		SEN_TERM		SCLK_TERM		0									
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
78h	VALID_FLAG_5					0										
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
78h	0											DIS_TRIG_ERR	0	TRIG_ERR	0	STDBY_FLAG
ADD	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
7Bh	0															
ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
7Bh	0							DIS_STDBY	0							

8.1.1 Register 0h (offset = 0h) [reset = 0h]

Figure 8-3. Register 0h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Figure 8-3. Register 0h (continued)

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	BURST_WR_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	READ_EN	RESET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-4. Register 00 Field Descriptions

Bit	Field	Type	Reset	Description
31-9	0	R/W	0h	Must read or write 0
8-8	BURST_WR_EN	R/W	0h	0 = Normal register write mode 1 = Burst register write mode
7-2	0	R/W	0h	Must read or write 0
1-1	READ_EN	R/W	0h	0 = Register write enable 1 = Register read enable
0-0	RESET	R/W	0h	0 = Normal operation 1 = Software reset

8.1.2 Register 2h (offset = 2h) [reset = 0h]

Figure 8-5. Register 2h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PAGE_16_EN_0	PAGE_15_EN_0	PAGE_14_EN_0	PAGE_13_EN_0	PAGE_12_EN_0	PAGE_11_EN_0	PAGE_10_EN_0	PAGE_9_EN_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PAGE_8_EN_0	PAGE_7_EN_0	PAGE_6_EN_0	PAGE_5_EN_0	PAGE_4_EN_0	PAGE_3_EN_0	PAGE_2_EN_0	PAGE_1_EN_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-6. Register 02 Field Descriptions

Bit	Field	Type	Reset	Description
31-16	0	R/W	0h	Must read or write 0
15-15	PAGE_16_EN_0	R/W	0h	0 = Page 16 write disable via lane SDATA_0 1 = Page 16 write enable via lane SDATA_0

Figure 8-6. Register 02 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-14	PAGE_15_EN_0	R/W	0h	0 = Page 15 write disable via lane SDATA_0 1 = Page 15 write enable via lane SDATA_0
13-13	PAGE_14_EN_0	R/W	0h	0 = Page 14 write disable via lane SDATA_0 1 = Page 14 write enable via lane SDATA_0
12-12	PAGE_13_EN_0	R/W	0h	0 = Page 13 write disable via lane SDATA_0 1 = Page 13 write enable via lane SDATA_0
11-11	PAGE_12_EN_0	R/W	0h	0 = Page 12 write disable via lane SDATA_0 1 = Page 12 write enable via lane SDATA_0
10-10	PAGE_11_EN_0	R/W	0h	0 = Page 11 write disable via lane SDATA_0 1 = Page 11 write enable via lane SDATA_0
9-9	PAGE_10_EN_0	R/W	0h	0 = Page 10 write disable via lane SDATA_0 1 = Page 10 write enable via lane SDATA_0
8-8	PAGE_9_EN_0	R/W	0h	0 = Page 9 write disable via lane SDATA_0 1 = Page 9 write enable via lane SDATA_0
7-7	PAGE_8_EN_0	R/W	0h	0 = Page 8 write disable via lane SDATA_0 1 = Page 8 write enable via lane SDATA_0
6-6	PAGE_7_EN_0	R/W	0h	0 = Page 7 write disable via lane SDATA_0 1 = Page 7 write enable via lane SDATA_0
5-5	PAGE_6_EN_0	R/W	0h	0 = Page 6 write disable via lane SDATA_0 1 = Page 6 write enable via lane SDATA_0
4-4	PAGE_5_EN_0	R/W	0h	0 = Page 5 write disable via lane SDATA_0 1 = Page 5 write enable via lane SDATA_0
3-3	PAGE_4_EN_0	R/W	0h	0 = Page 4 write disable via lane SDATA_0 1 = Page 4 write enable via lane SDATA_0
2-2	PAGE_3_EN_0	R/W	0h	0 = Page 3 write disable via lane SDATA_0 1 = Page 3 write enable via lane SDATA_0
1-1	PAGE_2_EN_0	R/W	0h	0 = Page 2 write disable via lane SDATA_0 1 = Page 2 write enable via lane SDATA_0
0-0	PAGE_1_EN_0	R/W	0h	0 = Page 1 write disable via lane SDATA_0 1 = Page 1 write enable via lane SDATA_0

8.1.3 Register 3h (offset = 3h) [reset = 0h]

Figure 8-7. Register 3h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PAGE_16_EN_1	PAGE_15_EN_1	PAGE_14_EN_1	PAGE_13_EN_1	PAGE_12_EN_1	PAGE_11_EN_1	PAGE_10_EN_1	PAGE_9_EN_1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PAGE_8_EN_1	PAGE_7_EN_1	PAGE_6_EN_1	PAGE_5_EN_1	PAGE_4_EN_1	PAGE_3_EN_1	PAGE_2_EN_1	PAGE_1_EN_1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-8. Register 03 Field Descriptions

Bit	Field	Type	Reset	Description
31-16	0	R/W	0h	Must read or write 0
15-15	PAGE_16_EN_1	R/W	0h	0 = Page 16 write disable via lane SDATA_1 1 = Page 16 write enable via lane SDATA_1
14-14	PAGE_15_EN_1	R/W	0h	0 = Page 15 write disable via lane SDATA_1 1 = Page 15 write enable via lane SDATA_1
13-13	PAGE_14_EN_1	R/W	0h	0 = Page 14 write disable via lane SDATA_1 1 = Page 14 write enable via lane SDATA_1
12-12	PAGE_13_EN_1	R/W	0h	0 = Page 13 write disable via lane SDATA_1 1 = Page 13 write enable via lane SDATA_1
11-11	PAGE_12_EN_1	R/W	0h	0 = Page 12 write disable via lane SDATA_1 1 = Page 12 write enable via lane SDATA_1
10-10	PAGE_11_EN_1	R/W	0h	0 = Page 11 write disable via lane SDATA_1 1 = Page 11 write enable via lane SDATA_1
9-9	PAGE_10_EN_1	R/W	0h	0 = Page 10 write disable via lane SDATA_1 1 = Page 10 write enable via lane SDATA_1
8-8	PAGE_9_EN_1	R/W	0h	0 = Page 9 write disable via lane SDATA_1 1 = Page 9 write enable via lane SDATA_1
7-7	PAGE_8_EN_1	R/W	0h	0 = Page 8 write disable via lane SDATA_1 1 = Page 8 write enable via lane SDATA_1
6-6	PAGE_7_EN_1	R/W	0h	0 = Page 7 write disable via lane SDATA_1 1 = Page 7 write enable via lane SDATA_1
5-5	PAGE_6_EN_1	R/W	0h	0 = Page 6 write disable via lane SDATA_1 1 = Page 6 write enable via lane SDATA_1
4-4	PAGE_5_EN_1	R/W	0h	0 = Page 5 write disable via lane SDATA_1 1 = Page 5 write enable via lane SDATA_1
3-3	PAGE_4_EN_1	R/W	0h	0 = Page 4 write disable via lane SDATA_1 1 = Page 4 write enable via lane SDATA_1
2-2	PAGE_3_EN_1	R/W	0h	0 = Page 3 write disable via lane SDATA_1 1 = Page 3 write enable via lane SDATA_1
1-1	PAGE_2_EN_1	R/W	0h	0 = Page 2 write disable via lane SDATA_1 1 = Page 2 write enable via lane SDATA_1
0-0	PAGE_1_EN_1	R/W	0h	0 = Page 1 write disable via lane SDATA_1 1 = Page 1 write enable via lane SDATA_1

8.1.4 Register 9h (offset = 9h) [reset = 0h]

Figure 8-9. Register 9h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PDN_GBL

Figure 8-9. Register 9h (continued)

R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-10. Register 09 Field Descriptions

Bit	Field	Type	Reset	Description
31-1	0	R/W	0h	Must read or write 0
0-0	PDN_GBL	R/W	0h	0 = Normal operation 1 = Global power down

8.1.5 Register Bh (offset = Bh) [reset = 0h]

Figure 8-11. Register Bh

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CLK_DIV				0	0	0	0
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	EN_SYNC_DET	CW_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-12. Register 0B Field Descriptions

Bit	Field	Type	Reset	Description
31-16	0	R/W	0h	Must read or write 0
15-12	CLK_DIV	R/W	0h	Clock division for pattern generator clock 0000 = Division factor 1 0001 = Division factor 2 0010 = Division factor 3 0011 = Division factor 4 0100 = Division factor 5 0101 = Division factor 6 0110 = Division factor 7 0111 = Division factor 8 1000 = Division factor 16 Others = Division factor 32
11-2	0	R/W	0h	Must read or write 0
1-1	EN_SYNC_DET	R/W	0h	0 = TR_BF_SYNC detect is disabled 1 = TR_BF_SYNC detect is enabled
0-0	CW_EN	R/W	0h	0 = CW mode disabled 1 = CW mode enabled

8.1.6 Register Ch (offset = Ch) [reset = 0h]

Figure 8-13. Register Ch

31	30	29	28	27	26	25	24
CW_PER_4					CW_LVL_4		
R/W-0h					R/W-0h		
23	22	21	20	19	18	17	16
CW_PER_3					CW_LVL_3		
R/W-0h					R/W-0h		
15	14	13	12	11	10	9	8
CW_PER_2					CW_LVL_2		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
CW_PER_1					CW_LVL_1		
R/W-0h					R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-14. Register 0C Field Descriptions

Bit	Field	Type	Reset	Description
31-27	CW_PER_4	R/W	0h	CW period 4
26-24	CW_LVL_4	R/W	0h	CW level 4
23-19	CW_PER_3	R/W	0h	CW period 3
18-16	CW_LVL_3	R/W	0h	CW level 3
15-11	CW_PER_2	R/W	0h	CW period 2
10-8	CW_LVL_2	R/W	0h	CW level 2
7-3	CW_PER_1	R/W	0h	CW period 1
2-0	CW_LVL_1	R/W	0h	CW level 1

8.1.7 Register Dh (offset = Dh) [reset = 0h]

Figure 8-15. Register Dh

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	BF_PROF_SEL_2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
BF_PROF_SEL_2							
R/W-0h							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	BF_PROF_SEL_1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
BF_PROF_SEL_1							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-16. Register 0D Field Descriptions

Bit	Field	Type	Reset	Description
31-25	0	R/W	0h	Must read or write 0
24-16	BF_PROF_SEL_2	R/W	0h	Select delay value stored in locations N and N+1 of memory block 2. Where N is the decimal value programmed in register BF_PROF_SEL_2
15-9	0	R/W	0h	Must read or write 0
8-0	BF_PROF_SEL_1	R/W	0h	Select delay value stored in locations N and N+1 of memory block 1. Where N is the decimal value programmed in register BF_PROF_SEL_1

8.1.8 Register Eh (offset = Eh) [reset = 0h]

Figure 8-17. Register Eh

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	BF_PROF_SEL_4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
BF_PROF_SEL_4							
R/W-0h							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	BF_PROF_SEL_3
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
BF_PROF_SEL_3							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-18. Register 0E Field Descriptions

Bit	Field	Type	Reset	Description
31-25	0	R/W	0h	Must read or write 0
24-16	BF_PROF_SEL_4	R/W	0h	Select delay value stored in locations N and N+1 of memory block 4. Where N is the decimal value programmed in register BF_PROF_SEL_4
15-9	0	R/W	0h	Must read or write 0
8-0	BF_PROF_SEL_3	R/W	0h	Select delay value stored in locations N and N+1 of memory block 3. Where N is the decimal value programmed in register BF_PROF_SEL_3

8.1.9 Register Fh (offset = Fh) [reset = 0h]

Figure 8-19. Register Fh

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	BF_PROF_SEL_6
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16

Figure 8-19. Register Fh (continued)

BF_PROF_SEL_6							
R/W-0h							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	BF_PROF_SEL_5
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
BF_PROF_SEL_5							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-20. Register 0F Field Descriptions

Bit	Field	Type	Reset	Description
31-25	0	R/W	0h	Must read or write 0
24-16	BF_PROF_SEL_6	R/W	0h	Select delay value stored in locations N and N+1 of memory block 6. Where N is the decimal value programmed in register BF_PROF_SEL_6
15-9	0	R/W	0h	Must read or write 0
8-0	BF_PROF_SEL_5	R/W	0h	Select delay value stored in locations N and N+1 of memory block 5. Where N is the decimal value programmed in register BF_PROF_SEL_5

8.1.10 Register 10h (offset = 10h) [reset = 0h]

Figure 8-21. Register 10h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	BF_PROF_SEL_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
BF_PROF_SEL_8							
R/W-0h							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	BF_PROF_SEL_7
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
BF_PROF_SEL_7							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-22. Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
31-25	0	R/W	0h	Must read or write 0
24-16	BF_PROF_SEL_8	R/W	0h	Select delay value stored in locations N and N+1 of memory block 8. Where N is the decimal value programmed in register BF_PROF_SEL_8

Figure 8-22. Register 10 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-9	0	R/W	0h	Must read or write 0
8-0	BF_PROF_SEL_7	R/W	0h	Select delay value stored in locations N and N+1 of memory block 7. Where N is the decimal value programmed in register BF_PROF_SEL_7

8.1.11 Register 11h (offset = 11h) [reset = 0h]

Figure 8-23. Register 11h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	BF_PROF_SEL_10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
BF_PROF_SEL_10							
R/W-0h							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	BF_PROF_SEL_9
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
BF_PROF_SEL_9							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-24. Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
31-25	0	R/W	0h	Must read or write 0
24-16	BF_PROF_SEL_10	R/W	0h	Select delay value stored in locations N and N+1 of memory block 10. Where N is the decimal value programmed in register BF_PROF_SEL_10
15-9	0	R/W	0h	Must read or write 0
8-0	BF_PROF_SEL_9	R/W	0h	Select delay value stored in locations N and N+1 of memory block 9. Where N is the decimal value programmed in register BF_PROF_SEL_9 max : 119

8.1.12 Register 12h (offset = 12h) [reset = 0h]

Figure 8-25. Register 12h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	BF_PROF_SEL_12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
BF_PROF_SEL_12							
R/W-0h							

Figure 8-25. Register 12h (continued)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	BF_PROF_SEL_11
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
BF_PROF_SEL_11							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-26. Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
31-25	0	R/W	0h	Must read or write 0
24-16	BF_PROF_SEL_12	R/W	0h	Select delay value stored in locations N and N+1 of memory block 12. Where N is the decimal value programmed in register BF_PROF_SEL_12
15-9	0	R/W	0h	Must read or write 0
8-0	BF_PROF_SEL_11	R/W	0h	Select delay value stored in locations N and N+1 of memory block 11. Where N is the decimal value programmed in register BF_PROF_SEL_11

8.1.13 Register 13h (offset = 13h) [reset = 0h]

Figure 8-27. Register 13h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	BF_PROF_SEL_14
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
BF_PROF_SEL_14							
R/W-0h							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	BF_PROF_SEL_13
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
BF_PROF_SEL_13							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-28. Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
31-25	0	R/W	0h	Must read or write 0
24-16	BF_PROF_SEL_14	R/W	0h	Select delay value stored in locations N and N+1 of memory block 14. Where N is the decimal value programmed in register BF_PROF_SEL_14
15-9	0	R/W	0h	Must read or write 0

Figure 8-28. Register 13 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-0	BF_PROF_SEL_13	R/W	0h	Select delay value stored in locations N and N+1 of memory block 13. Where N is the decimal value programmed in register BF_PROF_SEL_13

8.1.14 Register 14h (offset = 14h) [reset = 0h]

Figure 8-29. Register 14h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	BF_PROF_SEL_16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
BF_PROF_SEL_16							
R/W-0h							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	BF_PROF_SEL_15
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
BF_PROF_SEL_15							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-30. Register 14 Field Descriptions

Bit	Field	Type	Reset	Description
31-25	0	R/W	0h	Must read or write 0
24-16	BF_PROF_SEL_16	R/W	0h	Select delay value stored in locations N and N+1 of memory block 16. Where N is the decimal value programmed in register BF_PROF_SEL_16
15-9	0	R/W	0h	Must read or write 0
8-0	BF_PROF_SEL_15	R/W	0h	Select delay value stored in locations N and N+1 of memory block 15. Where N is the decimal value programmed in register BF_PROF_SEL_15

8.1.15 Register 16h (offset = 16h) [reset = 0h]

Figure 8-31. Register 16h

31	30	29	28	27	26	25	24
TR_SW_EN_64	TR_SW_EN_62	TR_SW_EN_60	TR_SW_EN_58	TR_SW_EN_56	TR_SW_EN_54	TR_SW_EN_52	TR_SW_EN_50
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TR_SW_EN_48	TR_SW_EN_46	TR_SW_EN_44	TR_SW_EN_42	TR_SW_EN_40	TR_SW_EN_38	TR_SW_EN_36	TR_SW_EN_34
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TR_SW_EN_32	TR_SW_EN_30	TR_SW_EN_28	TR_SW_EN_26	TR_SW_EN_24	TR_SW_EN_22	TR_SW_EN_20	TR_SW_EN_18

Figure 8-31. Register 16h (continued)

R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TR_SW_EN_16	TR_SW_EN_14	TR_SW_EN_12	TR_SW_EN_10	TR_SW_EN_8	TR_SW_EN_6	TR_SW_EN_4	TR_SW_EN_2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-32. Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
31-31	TR_SW_EN_64	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 64
30-30	TR_SW_EN_62	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 62
29-29	TR_SW_EN_60	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 60
28-28	TR_SW_EN_58	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 58
27-27	TR_SW_EN_56	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 56
26-26	TR_SW_EN_54	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 54
25-25	TR_SW_EN_52	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 52
24-24	TR_SW_EN_50	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 50
23-23	TR_SW_EN_48	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 48
22-22	TR_SW_EN_46	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 46
21-21	TR_SW_EN_44	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 44
20-20	TR_SW_EN_42	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 42
19-19	TR_SW_EN_40	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 40
18-18	TR_SW_EN_38	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 38
17-17	TR_SW_EN_36	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 36
16-16	TR_SW_EN_34	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 34
15-15	TR_SW_EN_32	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 32
14-14	TR_SW_EN_30	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 30
13-13	TR_SW_EN_28	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 28
12-12	TR_SW_EN_26	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 26
11-11	TR_SW_EN_24	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 24
10-10	TR_SW_EN_22	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 22

Figure 8-32. Register 16 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-9	TR_SW_EN_20	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 20
8-8	TR_SW_EN_18	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 18
7-7	TR_SW_EN_16	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 16
6-6	TR_SW_EN_14	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 14
5-5	TR_SW_EN_12	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 12
4-4	TR_SW_EN_10	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 10
3-3	TR_SW_EN_8	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 8
2-2	TR_SW_EN_6	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 6
1-1	TR_SW_EN_4	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 4
0-0	TR_SW_EN_2	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 2

8.1.16 Register 17h (offset = 17h) [reset = 0h]

Figure 8-33. Register 17h

31	30	29	28	27	26	25	24
TR_SW_EN_63	TR_SW_EN_61	TR_SW_EN_59	TR_SW_EN_57	TR_SW_EN_55	TR_SW_EN_53	TR_SW_EN_51	TR_SW_EN_49
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TR_SW_EN_47	TR_SW_EN_45	TR_SW_EN_43	TR_SW_EN_41	TR_SW_EN_39	TR_SW_EN_37	TR_SW_EN_35	TR_SW_EN_33
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TR_SW_EN_31	TR_SW_EN_29	TR_SW_EN_27	TR_SW_EN_25	TR_SW_EN_23	TR_SW_EN_21	TR_SW_EN_19	TR_SW_EN_17
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TR_SW_EN_15	TR_SW_EN_13	TR_SW_EN_11	TR_SW_EN_9	TR_SW_EN_7	TR_SW_EN_5	TR_SW_EN_3	TR_SW_EN_1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-34. Register 17 Field Descriptions

Bit	Field	Type	Reset	Description
31-31	TR_SW_EN_63	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 63
30-30	TR_SW_EN_61	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 61
29-29	TR_SW_EN_59	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 59
28-28	TR_SW_EN_57	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 57

Figure 8-34. Register 17 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-27	TR_SW_EN_55	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 55
26-26	TR_SW_EN_53	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 53
25-25	TR_SW_EN_51	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 51
24-24	TR_SW_EN_49	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 49
23-23	TR_SW_EN_47	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 47
22-22	TR_SW_EN_45	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 45
21-21	TR_SW_EN_43	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 43
20-20	TR_SW_EN_41	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 41
19-19	TR_SW_EN_39	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 39
18-18	TR_SW_EN_37	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 37
17-17	TR_SW_EN_35	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 35
16-16	TR_SW_EN_33	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 33
15-15	TR_SW_EN_31	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 31
14-14	TR_SW_EN_29	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 29
13-13	TR_SW_EN_27	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 27
12-12	TR_SW_EN_25	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 25
11-11	TR_SW_EN_23	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 23
10-10	TR_SW_EN_21	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 21
9-9	TR_SW_EN_19	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 19
8-8	TR_SW_EN_17	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 17
7-7	TR_SW_EN_15	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 15
6-6	TR_SW_EN_13	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 13
5-5	TR_SW_EN_11	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 11
4-4	TR_SW_EN_9	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 9
3-3	TR_SW_EN_7	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 7
2-2	TR_SW_EN_5	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 5
1-1	TR_SW_EN_3	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 3

Figure 8-34. Register 17 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0-0	TR_SW_EN_1	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch permanently ON for channel 1

8.1.17 Register 18h (offset = 18h) [reset = 0h]

Figure 8-35. Register 18h

31	30	29	28	27	26	25	24
TR_SW_DIS_64	TR_SW_DIS_62	TR_SW_DIS_60	TR_SW_DIS_58	TR_SW_DIS_56	TR_SW_DIS_54	TR_SW_DIS_52	TR_SW_DIS_50
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TR_SW_DIS_48	TR_SW_DIS_46	TR_SW_DIS_44	TR_SW_DIS_42	TR_SW_DIS_40	TR_SW_DIS_38	TR_SW_DIS_36	TR_SW_DIS_34
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TR_SW_DIS_32	TR_SW_DIS_30	TR_SW_DIS_28	TR_SW_DIS_26	TR_SW_DIS_24	TR_SW_DIS_22	TR_SW_DIS_20	TR_SW_DIS_18
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TR_SW_DIS_16	TR_SW_DIS_14	TR_SW_DIS_12	TR_SW_DIS_10	TR_SW_DIS_8	TR_SW_DIS_6	TR_SW_DIS_4	TR_SW_DIS_2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-36. Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
31-31	TR_SW_DIS_64	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 64
30-30	TR_SW_DIS_62	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 62
29-29	TR_SW_DIS_60	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 60
28-28	TR_SW_DIS_58	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 58
27-27	TR_SW_DIS_56	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 56
26-26	TR_SW_DIS_54	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 54
25-25	TR_SW_DIS_52	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 52
24-24	TR_SW_DIS_50	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 50
23-23	TR_SW_DIS_48	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 48
22-22	TR_SW_DIS_46	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 46
21-21	TR_SW_DIS_44	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 44

Figure 8-36. Register 18 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-20	TR_SW_DIS_42	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 42
19-19	TR_SW_DIS_40	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 40
18-18	TR_SW_DIS_38	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 38
17-17	TR_SW_DIS_36	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 36
16-16	TR_SW_DIS_34	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 34
15-15	TR_SW_DIS_32	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 32
14-14	TR_SW_DIS_30	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 30
13-13	TR_SW_DIS_28	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 28
12-12	TR_SW_DIS_26	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 26
11-11	TR_SW_DIS_24	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 24
10-10	TR_SW_DIS_22	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 22
9-9	TR_SW_DIS_20	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 20
8-8	TR_SW_DIS_18	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 18
7-7	TR_SW_DIS_16	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 16
6-6	TR_SW_DIS_14	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 14
5-5	TR_SW_DIS_12	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 12
4-4	TR_SW_DIS_10	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 10
3-3	TR_SW_DIS_8	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 8
2-2	TR_SW_DIS_6	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 6
1-1	TR_SW_DIS_4	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 4
0-0	TR_SW_DIS_2	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 2

8.1.18 Register 19h (offset = 19h) [reset = 0h]

Figure 8-37. Register 19h

31	30	29	28	27	26	25	24
TR_SW_DIS_63	TR_SW_DIS_61	TR_SW_DIS_59	TR_SW_DIS_57	TR_SW_DIS_55	TR_SW_DIS_53	TR_SW_DIS_51	TR_SW_DIS_49
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16

Figure 8-37. Register 19h (continued)

TR_SW_DIS_47	TR_SW_DIS_45	TR_SW_DIS_43	TR_SW_DIS_41	TR_SW_DIS_39	TR_SW_DIS_37	TR_SW_DIS_35	TR_SW_DIS_33
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TR_SW_DIS_31	TR_SW_DIS_29	TR_SW_DIS_27	TR_SW_DIS_25	TR_SW_DIS_23	TR_SW_DIS_21	TR_SW_DIS_19	TR_SW_DIS_17
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TR_SW_DIS_15	TR_SW_DIS_13	TR_SW_DIS_11	TR_SW_DIS_9	TR_SW_DIS_7	TR_SW_DIS_5	TR_SW_DIS_3	TR_SW_DIS_1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-38. Register 19 Field Descriptions

Bit	Field	Type	Reset	Description
31-31	TR_SW_DIS_63	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 63
30-30	TR_SW_DIS_61	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 61
29-29	TR_SW_DIS_59	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 59
28-28	TR_SW_DIS_57	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 57
27-27	TR_SW_DIS_55	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 55
26-26	TR_SW_DIS_53	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 53
25-25	TR_SW_DIS_51	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 51
24-24	TR_SW_DIS_49	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 49
23-23	TR_SW_DIS_47	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 47
22-22	TR_SW_DIS_45	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 45
21-21	TR_SW_DIS_43	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 43
20-20	TR_SW_DIS_41	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 41
19-19	TR_SW_DIS_39	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 39
18-18	TR_SW_DIS_37	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 37
17-17	TR_SW_DIS_35	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 35
16-16	TR_SW_DIS_33	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 33
15-15	TR_SW_DIS_31	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 31
14-14	TR_SW_DIS_29	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 29

Figure 8-38. Register 19 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-13	TR_SW_DIS_27	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 27
12-12	TR_SW_DIS_25	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 25
11-11	TR_SW_DIS_23	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 23
10-10	TR_SW_DIS_21	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 21
9-9	TR_SW_DIS_19	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 19
8-8	TR_SW_DIS_17	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 17
7-7	TR_SW_DIS_15	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 15
6-6	TR_SW_DIS_13	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 13
5-5	TR_SW_DIS_11	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 11
4-4	TR_SW_DIS_9	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 9
3-3	TR_SW_DIS_7	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 7
2-2	TR_SW_DIS_5	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 5
1-1	TR_SW_DIS_3	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 3
0-0	TR_SW_DIS_1	R/W	0h	0 = T_R switch Normal operation 1 = T_R switch disable for channel 1

8.1.19 Register 1Bh (offset = 1Bh) [reset = 0h]

Figure 8-39. Register 1Bh

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	TR_SW_GBL_MODE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-40. Register 1B Field Descriptions

Bit	Field	Type	Reset	Description
31-1	0	R/W	0h	Must read or write 0
0-0	TR_SW_GBL_MODE	R/W	0h	0 = Normal operation 1 = Enable T_R switch turn ON operation with respect to end of pattern of all the channels

8.1.20 Register 1Dh (offset = 1Dh) [reset = 4FFC00h]

Figure 8-41. Register 1Dh

31	30	29	28	27	26	25	24
TRAN_COUNT							
R/W-0h							
23	22	21	20	19	18	17	16
TRAN_COUNT		0	0	LVL_DURATION			
R/W-1h		R/W-0h	R/W-0h	R/W-Fh			
15	14	13	12	11	10	9	8
LVL_DURATION						DIS_LONG_TRAN_ERR	DIS_SINGLE_LVL_ERR
R/W-3Fh						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	LONG_TRAN_ERR	0	SINGLE_LVL_ERR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-42. Register 1D Field Descriptions

Bit	Field	Type	Reset	Description
31-22	TRAN_COUNT	R/W	1h	Sets the maximum transition count limit for the pattern
21-20	0	R/W	0h	Must read or write 0
19-10	LVL_DURATION	R/W	3FFh	Sets the maximum duration of single level.
9-9	DIS_LONG_TRAN_ERR	R/W	0h	0 = Long transition error detect is enabled 1 = Long transition error detect is disabled
8-8	DIS_SINGLE_LVL_ERR	R/W	0h	0 = Long single level error detect is enabled 1 = Long single level error detect is disabled
7-3	0	R/W	0h	Must read or write 0
2-2	LONG_TRAN_ERR	R	0h	0 = Normal operaion 1 = Long Transition Error
1-1	0	R/W	0h	Must read or write 0
0-0	SINGLE_LVL_ERR	R	0h	0 = Normal operaion 1 = Single Level for High Duration Error

8.1.21 Register 1Fh (offset = 1Fh) [reset = 0h]

Figure 8-43. Register 1Fh

31	30	29	28	27	26	25	24
0	0	0	0	0	TSHUT_TEMP	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Figure 8-43. Register 1Fh (continued)

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-44. Register 1F Field Descriptions

Bit	Field	Type	Reset	Description
31-27	0	R/W	0h	Must read or write 0
26-26	TSHUT_TEMP	R/W	0h	Sets the Thermal Shutdown temperature for the device 0 = Shutdown temperature is set to 105 C 1 = Shutdown temperature is set to 125 C
25-0	0	R/W	0h	Must read or write 0

8.1.22 Register 2Dh (offset = 2Dh) [reset = 0h]

Figure 8-45. Register 2Dh

31	30	29	28	27	26	25	24
PDN_PUL_64	PDN_PUL_62	PDN_PUL_60	PDN_PUL_58	PDN_PUL_56	PDN_PUL_54	PDN_PUL_52	PDN_PUL_50
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
PDN_PUL_48	PDN_PUL_46	PDN_PUL_44	PDN_PUL_42	PDN_PUL_40	PDN_PUL_38	PDN_PUL_36	PDN_PUL_34
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PDN_PUL_32	PDN_PUL_30	PDN_PUL_28	PDN_PUL_26	PDN_PUL_24	PDN_PUL_22	PDN_PUL_20	PDN_PUL_18
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDN_PUL_16	PDN_PUL_14	PDN_PUL_12	PDN_PUL_10	PDN_PUL_8	PDN_PUL_6	PDN_PUL_4	PDN_PUL_2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-46. Register 2D Field Descriptions

Bit	Field	Type	Reset	Description
31-31	PDN_PUL_64	R/W	0h	0 = Normal operation 1 = Power down channel 64 pulser
30-30	PDN_PUL_62	R/W	0h	0 = Normal operation 1 = Power down channel 62 pulser
29-29	PDN_PUL_60	R/W	0h	0 = Normal operation 1 = Power down channel 60 pulser
28-28	PDN_PUL_58	R/W	0h	0 = Normal operation 1 = Power down channel 58 pulser

Figure 8-46. Register 2D Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-27	PDN_PUL_56	R/W	0h	0 = Normal operation 1 = Power down channel 56 pulser
26-26	PDN_PUL_54	R/W	0h	0 = Normal operation 1 = Power down channel 54 pulser
25-25	PDN_PUL_52	R/W	0h	0 = Normal operation 1 = Power down channel 52 pulser
24-24	PDN_PUL_50	R/W	0h	0 = Normal operation 1 = Power down channel 50 pulser
23-23	PDN_PUL_48	R/W	0h	0 = Normal operation 1 = Power down channel 48 pulser
22-22	PDN_PUL_46	R/W	0h	0 = Normal operation 1 = Power down channel 46 pulser
21-21	PDN_PUL_44	R/W	0h	0 = Normal operation 1 = Power down channel 44 pulser
20-20	PDN_PUL_42	R/W	0h	0 = Normal operation 1 = Power down channel 42 pulser
19-19	PDN_PUL_40	R/W	0h	0 = Normal operation 1 = Power down channel 40 pulser
18-18	PDN_PUL_38	R/W	0h	0 = Normal operation 1 = Power down channel 38 pulser
17-17	PDN_PUL_36	R/W	0h	0 = Normal operation 1 = Power down channel 36 pulser
16-16	PDN_PUL_34	R/W	0h	0 = Normal operation 1 = Power down channel 34 pulser
15-15	PDN_PUL_32	R/W	0h	0 = Normal operation 1 = Power down channel 32 pulser
14-14	PDN_PUL_30	R/W	0h	0 = Normal operation 1 = Power down channel 30 pulser
13-13	PDN_PUL_28	R/W	0h	0 = Normal operation 1 = Power down channel 28 pulser
12-12	PDN_PUL_26	R/W	0h	0 = Normal operation 1 = Power down channel 26 pulser
11-11	PDN_PUL_24	R/W	0h	0 = Normal operation 1 = Power down channel 24 pulser
10-10	PDN_PUL_22	R/W	0h	0 = Normal operation 1 = Power down channel 22 pulser
9-9	PDN_PUL_20	R/W	0h	0 = Normal operation 1 = Power down channel 20 pulser
8-8	PDN_PUL_18	R/W	0h	0 = Normal operation 1 = Power down channel 18 pulser
7-7	PDN_PUL_16	R/W	0h	0 = Normal operation 1 = Power down channel 16 pulser
6-6	PDN_PUL_14	R/W	0h	0 = Normal operation 1 = Power down channel 14 pulser
5-5	PDN_PUL_12	R/W	0h	0 = Normal operation 1 = Power down channel 12 pulser
4-4	PDN_PUL_10	R/W	0h	0 = Normal operation 1 = Power down channel 10 pulser
3-3	PDN_PUL_8	R/W	0h	0 = Normal operation 1 = Power down channel 8 pulser
2-2	PDN_PUL_6	R/W	0h	0 = Normal operation 1 = Power down channel 6 pulser
1-1	PDN_PUL_4	R/W	0h	0 = Normal operation 1 = Power down channel 4 pulser

Figure 8-46. Register 2D Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0-0	PDN_PUL_2	R/W	0h	0 = Normal operation 1 = Power down channel 2 pulser

8.1.23 Register 2Eh (offset = 2Eh) [reset = 0h]

Figure 8-47. Register 2Eh

31	30	29	28	27	26	25	24
PDN_PUL_63	PDN_PUL_61	PDN_PUL_59	PDN_PUL_57	PDN_PUL_55	PDN_PUL_53	PDN_PUL_51	PDN_PUL_49
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
PDN_PUL_47	PDN_PUL_45	PDN_PUL_43	PDN_PUL_41	PDN_PUL_39	PDN_PUL_37	PDN_PUL_35	PDN_PUL_33
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PDN_PUL_31	PDN_PUL_29	PDN_PUL_27	PDN_PUL_25	PDN_PUL_23	PDN_PUL_21	PDN_PUL_19	PDN_PUL_17
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDN_PUL_15	PDN_PUL_13	PDN_PUL_11	PDN_PUL_9	PDN_PUL_7	PDN_PUL_5	PDN_PUL_3	PDN_PUL_1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-48. Register 2E Field Descriptions

Bit	Field	Type	Reset	Description
31-31	PDN_PUL_63	R/W	0h	0 = Normal operation 1 = Power down channel 63 pulser
30-30	PDN_PUL_61	R/W	0h	0 = Normal operation 1 = Power down channel 61 pulser
29-29	PDN_PUL_59	R/W	0h	0 = Normal operation 1 = Power down channel 59 pulser
28-28	PDN_PUL_57	R/W	0h	0 = Normal operation 1 = Power down channel 57 pulser
27-27	PDN_PUL_55	R/W	0h	0 = Normal operation 1 = Power down channel 55 pulser
26-26	PDN_PUL_53	R/W	0h	0 = Normal operation 1 = Power down channel 53 pulser
25-25	PDN_PUL_51	R/W	0h	0 = Normal operation 1 = Power down channel 51 pulser
24-24	PDN_PUL_49	R/W	0h	0 = Normal operation 1 = Power down channel 49 pulser
23-23	PDN_PUL_47	R/W	0h	0 = Normal operation 1 = Power down channel 47 pulser
22-22	PDN_PUL_45	R/W	0h	0 = Normal operation 1 = Power down channel 45 pulser
21-21	PDN_PUL_43	R/W	0h	0 = Normal operation 1 = Power down channel 43 pulser
20-20	PDN_PUL_41	R/W	0h	0 = Normal operation 1 = Power down channel 41 pulser
19-19	PDN_PUL_39	R/W	0h	0 = Normal operation 1 = Power down channel 39 pulser

Figure 8-48. Register 2E Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-18	PDN_PUL_37	R/W	0h	0 = Normal operation 1 = Power down channel 37 pulser
17-17	PDN_PUL_35	R/W	0h	0 = Normal operation 1 = Power down channel 35 pulser
16-16	PDN_PUL_33	R/W	0h	0 = Normal operation 1 = Power down channel 33 pulser
15-15	PDN_PUL_31	R/W	0h	0 = Normal operation 1 = Power down channel 31 pulser
14-14	PDN_PUL_29	R/W	0h	0 = Normal operation 1 = Power down channel 29 pulser
13-13	PDN_PUL_27	R/W	0h	0 = Normal operation 1 = Power down channel 27 pulser
12-12	PDN_PUL_25	R/W	0h	0 = Normal operation 1 = Power down channel 25 pulser
11-11	PDN_PUL_23	R/W	0h	0 = Normal operation 1 = Power down channel 23 pulser
10-10	PDN_PUL_21	R/W	0h	0 = Normal operation 1 = Power down channel 21 pulser
9-9	PDN_PUL_19	R/W	0h	0 = Normal operation 1 = Power down channel 19 pulser
8-8	PDN_PUL_17	R/W	0h	0 = Normal operation 1 = Power down channel 17 pulser
7-7	PDN_PUL_15	R/W	0h	0 = Normal operation 1 = Power down channel 15 pulser
6-6	PDN_PUL_13	R/W	0h	0 = Normal operation 1 = Power down channel 13 pulser
5-5	PDN_PUL_11	R/W	0h	0 = Normal operation 1 = Power down channel 11 pulser
4-4	PDN_PUL_9	R/W	0h	0 = Normal operation 1 = Power down channel 9 pulser
3-3	PDN_PUL_7	R/W	0h	0 = Normal operation 1 = Power down channel 7 pulser
2-2	PDN_PUL_5	R/W	0h	0 = Normal operation 1 = Power down channel 5 pulser
1-1	PDN_PUL_3	R/W	0h	0 = Normal operation 1 = Power down channel 3 pulser
0-0	PDN_PUL_1	R/W	0h	0 = Normal operation 1 = Power down channel 1 pulser

8.1.24 Register 2Fh (offset = 2Fh) [reset = 0h]

Figure 8-49. Register 2Fh

31	30	29	28	27	26	25	24
PAT_INV_CH_64	PAT_INV_CH_62	PAT_INV_CH_60	PAT_INV_CH_58	PAT_INV_CH_56	PAT_INV_CH_54	PAT_INV_CH_52	PAT_INV_CH_50
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
PAT_INV_CH_48	PAT_INV_CH_46	PAT_INV_CH_44	PAT_INV_CH_42	PAT_INV_CH_40	PAT_INV_CH_38	PAT_INV_CH_36	PAT_INV_CH_34
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8

Figure 8-49. Register 2Fh (continued)

PAT_INV_CH_32	PAT_INV_CH_30	PAT_INV_CH_28	PAT_INV_CH_26	PAT_INV_CH_24	PAT_INV_CH_22	PAT_INV_CH_20	PAT_INV_CH_18
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PAT_INV_CH_16	PAT_INV_CH_14	PAT_INV_CH_12	PAT_INV_CH_10	PAT_INV_CH_8	PAT_INV_CH_6	PAT_INV_CH_4	PAT_INV_CH_2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-50. Register 2F Field Descriptions

Bit	Field	Type	Reset	Description
31-31	PAT_INV_CH_64	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 64
30-30	PAT_INV_CH_62	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 62
29-29	PAT_INV_CH_60	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 60
28-28	PAT_INV_CH_58	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 58
27-27	PAT_INV_CH_56	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 56
26-26	PAT_INV_CH_54	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 54
25-25	PAT_INV_CH_52	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 52
24-24	PAT_INV_CH_50	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 50
23-23	PAT_INV_CH_48	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 48
22-22	PAT_INV_CH_46	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 46
21-21	PAT_INV_CH_44	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 44
20-20	PAT_INV_CH_42	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 42
19-19	PAT_INV_CH_40	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 40
18-18	PAT_INV_CH_38	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 38
17-17	PAT_INV_CH_36	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 36
16-16	PAT_INV_CH_34	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 34
15-15	PAT_INV_CH_32	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 32
14-14	PAT_INV_CH_30	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 30
13-13	PAT_INV_CH_28	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 28
12-12	PAT_INV_CH_26	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 26
11-11	PAT_INV_CH_24	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 24

Figure 8-50. Register 2F Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-10	PAT_INV_CH_22	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 22
9-9	PAT_INV_CH_20	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 20
8-8	PAT_INV_CH_18	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 18
7-7	PAT_INV_CH_16	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 16
6-6	PAT_INV_CH_14	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 14
5-5	PAT_INV_CH_12	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 12
4-4	PAT_INV_CH_10	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 10
3-3	PAT_INV_CH_8	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 8
2-2	PAT_INV_CH_6	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 6
1-1	PAT_INV_CH_4	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 4
0-0	PAT_INV_CH_2	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 2

8.1.25 Register 30h (offset = 30h) [reset = 0h]

Figure 8-51. Register 30h

31	30	29	28	27	26	25	24
PAT_INV_CH_63	PAT_INV_CH_61	PAT_INV_CH_59	PAT_INV_CH_57	PAT_INV_CH_55	PAT_INV_CH_53	PAT_INV_CH_51	PAT_INV_CH_49
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
PAT_INV_CH_47	PAT_INV_CH_45	PAT_INV_CH_43	PAT_INV_CH_41	PAT_INV_CH_39	PAT_INV_CH_37	PAT_INV_CH_35	PAT_INV_CH_33
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PAT_INV_CH_31	PAT_INV_CH_29	PAT_INV_CH_27	PAT_INV_CH_25	PAT_INV_CH_23	PAT_INV_CH_21	PAT_INV_CH_19	PAT_INV_CH_17
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PAT_INV_CH_15	PAT_INV_CH_13	PAT_INV_CH_11	PAT_INV_CH_9	PAT_INV_CH_7	PAT_INV_CH_5	PAT_INV_CH_3	PAT_INV_CH_1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-52. Register 30 Field Descriptions

Bit	Field	Type	Reset	Description
31-31	PAT_INV_CH_63	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 63

Figure 8-52. Register 30 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30-30	PAT_INV_CH_61	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 61
29-29	PAT_INV_CH_59	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 59
28-28	PAT_INV_CH_57	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 57
27-27	PAT_INV_CH_55	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 55
26-26	PAT_INV_CH_53	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 53
25-25	PAT_INV_CH_51	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 51
24-24	PAT_INV_CH_49	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 49
23-23	PAT_INV_CH_47	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 47
22-22	PAT_INV_CH_45	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 45
21-21	PAT_INV_CH_43	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 43
20-20	PAT_INV_CH_41	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 41
19-19	PAT_INV_CH_39	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 39
18-18	PAT_INV_CH_37	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 37
17-17	PAT_INV_CH_35	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 35
16-16	PAT_INV_CH_33	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 33
15-15	PAT_INV_CH_31	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 31
14-14	PAT_INV_CH_29	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 29
13-13	PAT_INV_CH_27	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 27
12-12	PAT_INV_CH_25	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 25
11-11	PAT_INV_CH_23	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 23
10-10	PAT_INV_CH_21	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 21
9-9	PAT_INV_CH_19	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 19
8-8	PAT_INV_CH_17	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 17
7-7	PAT_INV_CH_15	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 15
6-6	PAT_INV_CH_13	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 13
5-5	PAT_INV_CH_11	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 11
4-4	PAT_INV_CH_9	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 9

Figure 8-52. Register 30 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-3	PAT_INV_CH_7	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 7
2-2	PAT_INV_CH_5	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 5
1-1	PAT_INV_CH_3	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 3
0-0	PAT_INV_CH_1	R/W	0h	0 = Normal operation 1 = Invert pattern for channel 1

8.1.26 Register 33h (offset = 33h) [reset = 0h]

Figure 8-53. Register 33h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	MEM_START_WORD
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
MEM_START_WORD							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-54. Register 33 Field Descriptions

Bit	Field	Type	Reset	Description
31-9	0	R/W	0h	Must read or write 0
8-0	MEM_START_WORD	R/W	0h	Pattern Start word for all channels

8.1.27 Register 44h (offset = 44h) [reset = 0h]

Figure 8-55. Register 44h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	RED_MAX_CUR_M2			0	0	0
R/W-0h	R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h

Figure 8-55. Register 44h (continued)

7	6	5	4	3	2	1	0
0	0	0	0	0	RED_MAX_CUR_P1		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-56. Register 44 Field Descriptions

Bit	Field	Type	Reset	Description
31-14	0	R/W	0h	Must read or write 0
13-11	RED_MAX_CUR_M2	R/W	0h	Selects the current drive for the MHV2 Floating supply 000 = 133 mA 001 = 165 mA 010 = 197 mA 011 = 202 mA 100 = 22 mA 101 = 47 mA 110 = 74 mA 111 = 103 mA
10-3	0	R/W	0h	Must read or write 0
2-0	RED_MAX_CUR_P1	R/W	0h	Selects the current drive for the PHV1 Floating supply 000 = 164 mA 001 = 139 mA 010 = 115 mA 011 = 92 mA 100 = 70 mA 101 = 50 mA 110 = 31 mA 111 = 14 mA

8.1.28 Register 4Dh (offset = 4Dh) [reset = A8000000h]

Figure 8-57. Register 4Dh

31	30	29	28	27	26	25	24
VALID_FLAG_1					0	0	0
R-15h					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	ERROR_RST
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	TEMP_SHUT_ERR[11:6]					
R/W-0h	R/W-0h	R-0h					

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-58. Register 4D Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VALID_FLAG_1	R	15h	21 = Flag value is valid. For all other values the read flag is not valid
26-17	0	R/W	0h	Must read or write 0
16-16	ERROR_RST	R/W	0h	0 = Normal operation 1 = Reset error flag and bring out device from thermal shutdown. See Section 3.3.11 for more details
15-6	0	R/W	0h	Must read or write 0
5-0	TEMP_SHUT_ERR[11:6]	R	0h	0 = Normal operation Other values = High Temperature Error in the Bottom Half of the device. The index of the bit gives information about which thermal shutdown block is triggered.

8.1.29 Register 4Eh (offset = 4Eh) [reset = 50000000h]

Figure 8-59. Register 4Eh

31	30	29	28	27	26	25	24
VALID_FLAG_2					0	ARB2	0
R-Ah					R/W-0h	R-0h	R/W-0h
23	22	21	20	19	18	17	16
ARB1	0	0	0	0	0	0	0
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PHV_RANGE_ERR	0	0	0	0	0	0	0
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	M5V_SUP_ERR	P5V_SUP_ERR	0	0	0	0
R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-60. Register 4E Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VALID_FLAG_2	R	Ah	10 = Flag value is valid. For all other values the read flag is not valid
26-26	0	R/W	0h	Must read or write 0
25-25	ARB2	R	0h	Read Only bit. Can read 0 or 1. Both are okay.
24-24	0	R/W	0h	Must read or write 0
23-23	ARB1	R	0h	Read Only bit. Can read 0 or 1. Both are okay.
22-16	0	R/W	0h	Must read or write 0
15-15	PHV_RANGE_ERR	R	0h	0 = Normal operation 1 = AVDDP_HV Supply Range Error
14-6	0	R/W	0h	Must read or write 0
5-5	M5V_SUP_ERR	R	0h	0 = Normal operation 1 = AVDDM_5 Supply Error
4-4	P5V_SUP_ERR	R	0h	0 = Normal operation 1 = AVDDP_5 Supply Error
3-0	0	R/W	0h	Must read or write 0

8.1.30 Register 4Fh (offset = 4Fh) [reset = Fh]

Figure 8-61. Register 4Fh

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8

Figure 8-61. Register 4Fh (continued)

0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PHV_L				PHV_H			
R/W-0h				R/W-Fh			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-62. Register 4F Field Descriptions

Bit	Field	Type	Reset	Description
31-8	0	R/W	0h	Must read or write 0
7-4	PHV_L	R/W	0h	Set the AVDDP_HV supply lower limit.
3-0	PHV_H	R/W	Fh	Set the AVDDP_HV supply upper limit.

8.1.31 Register 51h (offset = 51h) [reset = 0h]

Figure 8-63. Register 51h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	DIS_M5V_SUP_ERR	DIS_P5V_SUP_ERR	0	CONST_2	0	CONST_1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	EN_PHV_RANGE_ERR	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-64. Register 51 Field Descriptions

Bit	Field	Type	Reset	Description
31-22	0	R/W	0h	Must read or write 0
21-21	DIS_M5V_SUP_ERR	R/W	0h	0 = AVDDM_5 supply error detect is enabled 1 = AVDDM_5 supply error detect is disabled
20-20	DIS_P5V_SUP_ERR	R/W	0h	0 = AVDDP_5 supply error detect is enabled 1 = AVDDP_5 supply error detect is disabled
19-19	0	R/W	0h	Must read or write 0
18-18	CONST_2	R/W	0h	Must write 1 during device initialization
17-17	0	R/W	0h	Must read or write 0
16-16	CONST_1	R/W	0h	Must write 1 during device initialization
15-13	0	R/W	0h	Must read or write 0
12-12	EN_PHV_RANGE_ERR	R/W	0h	0 = AVDDP_HV supply range error detect is disabled 1 = AVDDP_HV supply range error detect is enabled

Figure 8-64. Register 51 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	0	R/W	0h	Must read or write 0

8.1.32 Register 56h (offset = 56h) [reset = 0h]

Figure 8-65. Register 56h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	PDN_FLOAT_PHV_2	PDN_FLOAT_PHV_1	PDN_FLOAT_MHV_2	PDN_FLOAT_MHV_1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-66. Register 56 Field Descriptions

Bit	Field	Type	Reset	Description
31-4	0	R/W	0h	Must read or write 0
3-3	PDN_FLOAT_PHV_2	R/W	0h	0 = FLOAT_PHV_2 floating LDOs is enabled 1 = FLOAT_PHV_2 floating LDOs is powered down
2-2	PDN_FLOAT_PHV_1	R/W	0h	0 = FLOAT_PHV_1 floating LDOs is enabled 1 = FLOAT_PHV_1 floating LDOs is powered down
1-1	PDN_FLOAT_MHV_2	R/W	0h	0 = FLOAT_MHV_2 floating LDOs is enabled 1 = FLOAT_MHV_2 floating LDOs is powered down
0-0	PDN_FLOAT_MHV_1	R/W	0h	0 = FLOAT_MHV_1 floating LDOs is enabled 1 = FLOAT_MHV_1 floating LDOs is powered down

8.1.33 Register 57h (offset = 57h) [reset = 0h]

Figure 8-67. Register 57h

31	30	29	28	27	26	25	24
0	0	0	0	T_NRTZ_ON		T_PRTZ_ON	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
T_MHV2_ON		T_MHV1_ON		T_PHV2_ON		T_PHV1_ON	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
0	0	0	0	MHV_2_FL			MHV_1_FL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h

Figure 8-67. Register 57h (continued)

7	6	5	4	3	2	1	0
MHV_1_FL		PHV_2_FL			PHV_1_FL		
R/W-0h		R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-68. Register 57 Field Descriptions

Bit	Field	Type	Reset	Description
31-28	0	R/W	0h	Must read or write 0
27-26	T_NRTZ_ON	R/W	0h	Turn ON delay trim for NRTZ output transition 0: Default 1: 0.35 ns 2: 0.7 ns 3: 1.0 ns
25-24	T_PRTZ_ON	R/W	0h	Turn ON delay trim for PRTZ output transition 0: Default 1: 0.35 ns 2: 0.7 ns 3: 1.0 ns
23-22	T_MHV2_ON	R/W	0h	Turn ON delay trim for SW MHV transistor. Same value should be assigned for T_MHV1_ON and T_MHV2_ON 0: Default 1: 0.35 ns 2: 0.7 ns 3: 1.0 ns
21-20	T_MHV1_ON	R/W	0h	Turn ON delay trim for SW MHV transistor. Same value should be assigned for T_MHV1_ON and T_MHV2_ON 0: Default 1: 0.35 ns 2: 0.7 ns 3: 1.0 ns
19-18	T_PHV2_ON	R/W	0h	Turn ON delay trim for SW PHV transistor. Same value should be assigned for T_PHV1_ON and T_PHV2_ON 0: Default 1: 0.35 ns 2: 0.7 ns 3: 1.0 ns
17-16	T_PHV1_ON	R/W	0h	Turn ON delay trim for SW PHV transistor. Same value should be assigned for T_PHV1_ON and T_PHV2_ON 0: Default 1: 0.35 ns 2: 0.7 ns 3: 1.0 ns
15-12	0	R/W	0h	Must read or write 0
11-9	MHV_2_FL	R/W	0h	Vgs trim for SW MHV transistor. Same value should be assigned for MHV_1_FL and MHV_2_FL
8-6	MHV_1_FL	R/W	0h	Vgs trim for SW MHV transistor. Same value should be assigned for MHV_1_FL and MHV_2_FL
5-3	PHV_2_FL	R/W	0h	Vgs trim for SW PHV transistor. Same value should be assigned for PHV_1_FL and PHV_2_FL
2-0	PHV_1_FL	R/W	0h	Vgs trim for SW PHV transistor. Same value should be assigned for PHV_1_FL and PHV_2_FL

8.1.34 Register 58h (offset = 58h) [reset = 0h]

Figure 8-69. Register 58h

31	30	29	28	27	26	25	24

Figure 8-69. Register 58h (continued)

0	0	0	0	T_NRTZ_OFF		T_PRTZ_OFF	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
T_MHV2_OFF		T_MHV1_OFF		T_PHV2_OFF		T_PHV1_OFF	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-70. Register 58 Field Descriptions

Bit	Field	Type	Reset	Description
31-28	0	R/W	0h	Must read or write 0
27-26	T_NRTZ_OFF	R/W	0h	Turn OFF delay trim for NRTZ output transition 0: Default 1: 0.35 ns 2: 0.7 ns 3: 1.0 ns
25-24	T_PRTZ_OFF	R/W	0h	Turn OFF delay trim for PRTZ output transition 0: Default 1: 0.35 ns 2: 0.7 ns 3: 1.0 ns
23-22	T_MHV2_OFF	R/W	0h	Turn OFF delay trim for SW MHV transistor. Same value should be assigned for T_MHV1_OFF and T_MHV2_OFF 0: Default 1: 0.35 ns 2: 0.7 ns 3: 1.0 ns
21-20	T_MHV1_OFF	R/W	0h	Turn OFF delay trim for SW MHV transistor. Same value should be assigned for T_MHV1_OFF and T_MHV2_OFF 0: Default 1: 0.35 ns 2: 0.7 ns 3: 1.0 ns
19-18	T_PHV2_OFF	R/W	0h	Turn OFF delay trim for SW PHV transistor. Same value should be assigned for T_PHV1_OFF and T_PHV2_OFF 0: Default 1: 0.35 ns 2: 0.7 ns 3: 1.0 ns
17-16	T_PHV1_OFF	R/W	0h	Turn OFF delay trim for SW PHV transistor. Same value should be assigned for T_PHV1_OFF and T_PHV2_OFF 0: Default 1: 0.35 ns 2: 0.7 ns 3: 1.0 ns
15-0	0	R/W	0h	Must read or write 0

8.1.35 Register 5Ch (offset = 5Ch) [reset = 0h]

Figure 8-71. Register 5Ch

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	DIS_DYN_PDN_LDO	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-72. Register 5C Field Descriptions

Bit	Field	Type	Reset	Description
31-13	0	R/W	0h	Must read or write 0
12-12	DIS_DYN_PDN_LDO	R/W	0h	0 = Dynamic power down of floating LDOs is enabled 1 = Dynamic power down of floating LDOs is disabled
11-0	0	R/W	0h	Must read or write 0

8.1.36 Register 5Fh (offset = 5Fh) [reset = 0h]

Figure 8-73. Register 5Fh

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	RTZ_DRIVE	0	LOW_GLITCH_MODE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-74. Register 5F Field Descriptions

Bit	Field	Type	Reset	Description
31-3	0	R/W	0h	Must read or write 0

Figure 8-74. Register 5F Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-2	RTZ_DRIVE	R/W	0h	0 = Configures RTZ drive of the Pulser to 0.7A. 1 = Configures RTZ drive of the Pulser to 0.47A.
1-1	0	R/W	0h	Must read or write 0
0-0	LOW_GLITCH_MODE	R/W	0h	0 = Normal mode 1 = T_R switch configured in low glitch mode

8.1.37 Register 62h (offset = 62h) [reset = 58000000h]

Figure 8-75. Register 62h

31	30	29	28	27	26	25	24
VALID_FLAG_3					0	0	0
R-Bh					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	TEMP_SHUT_ERR[5:0]					
R/W-0h	R/W-0h	R-0h					

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-76. Register 62 Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VALID_FLAG_3	R	Bh	11 = Flag value is valid. For all other values the read flag is not valid
26-6	0	R/W	0h	Must read or write 0
5-0	TEMP_SHUT_ERR[5:0]	R	0h	0 = Normal operation Other values = High Temperature Error in the Top Half of the device. The index of the bit gives information about which thermal shutdown block is triggered.

8.1.38 Register 64h (offset = 64h) [reset = 0h]

Figure 8-77. Register 64h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	CONT_TEMP_SENSE	CLK_DIV_TSENSE		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		
15	14	13	12	11	10	9	8

Figure 8-77. Register 64h (continued)

0	0	READ_TEMP_VALID	READ_TEMP
R/W-0h	R/W-0h	R-0h	R-0h

7	6	5	4	3	2	1	0
READ_TEMP				0	0	TEMP_SENSE_RESET	TEMP_SENSE_EN
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-78. Register 64 Field Descriptions

Bit	Field	Type	Reset	Description
31-20	0	R/W	0h	Must read or write 0
19-19	CONT_TEMP_SENSE	R/W	0h	0 = Continuous temperature sense mode disabled. 1 = Continuous temperature sense mode enabled.
18-16	CLK_DIV_TSENSE	R/W	0h	Clock division for temperature sensor block 000 = Divide by 32 001 = Divide by 64 010 = Divide by 8 011 = Divide by 16 1XX = Divide by 4
15-14	0	R/W	0h	Must read or write 0
13-13	READ_TEMP_VALID	R	0h	Read only register 0 = Temperature read is not ready 1 = Temperature read is ready
12-4	READ_TEMP	R	0h	Read only register. It reads the temperature of the device. Read the register when READ_TEMP_VALID is '1'.
3-2	0	R/W	0h	Must read or write 0
1-1	TEMP_SENSE_RESET	R/W	0h	0 = Normal operation 1 = Resets the temperature sensor.
0-0	TEMP_SENSE_EN	R/W	0h	0 = Temperature sensor disabled 1 = Temperature sensor enabled

8.1.39 Register 66h (offset = 66h) [reset = 0h]

Figure 8-79. Register 66h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	RED_MAX_CUR_P2			0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-80. Register 66 Field Descriptions

Bit	Field	Type	Reset	Description
31-13	0	R/W	0h	Must read or write 0
12-10	RED_MAX_CUR_P2	R/W	0h	Selects the current drive for the PHV2 Floating supply 000 = 164 mA 001 = 139 mA 010 = 115 mA 011 = 92 mA 100 = 70 mA 101 = 50 mA 110 = 31 mA 111 = 14 mA
9-0	0	R/W	0h	Must read or write 0

8.1.40 Register 67h (offset = 67h) [reset = 0h]

Figure 8-81. Register 67h

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	RED_MAX_CUR_M1		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-82. Register 67 Field Descriptions

Bit	Field	Type	Reset	Description
31-19	0	R/W	0h	Must read or write 0
18-16	RED_MAX_CUR_M1	R/W	0h	Selects the current drive for the MHV1 Floating supply 000 = 133 mA 001 = 165 mA 010 = 197 mA 011 = 202 mA 100 = 22 mA 101 = 47 mA 110 = 74 mA 111 = 103 mA
15-0	0	R/W	0h	Must read or write 0

8.1.41 Register 6Ch (offset = 6Ch) [reset = B0000000h]

Figure 8-83. Register 6Ch

31	30	29	28	27	26	25	24
VALID_FLAG_4					0	0	0
R-16h					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	NO_CLK_ERR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Figure 8-83. Register 6Ch (continued)

7	6	5	4	3	2	1	0
0	0	0	0	PDN_SDATA_1	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-84. Register 6C Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VALID_FLAG_4	R	16h	22 = Flag value is valid. For all other values the read flag is not valid
26-17	0	R/W	0h	Must read or write 0
16-16	NO_CLK_ERR	R	0h	0 = No BF_CLK Clock Detect Error 1 = Normal operation. BF_CLK clock is detected by the device.
15-4	0	R/W	0h	Must read or write 0
3-3	PDN_SDATA_1	R/W	0h	0 = SDATA_1 buffer is enabled 1 = SDATA_1 buffer is powered down
2-0	0	R/W	0h	Must read or write 0

8.1.42 Register 6Eh (offset = 6Eh) [reset = 0h]

Figure 8-85. Register 6Eh

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	EN_DYN_PDN_SPIBUF	EN_DYN_PDN_CLKBUF	EN_CLK_GATE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	CLK_TERM	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
0	0	SYNC_TERM		BF_CLK_DIV_EN	0	BF_CLK_DIV	
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-86. Register 6E Field Descriptions

Bit	Field	Type	Reset	Description
31-19	0	R/W	0h	Must read or write 0
18-18	EN_DYN_PDN_SPIBUF	R/W	0h	0 = Dynamic power down of SPI buffer is disabled 1 = Dynamic power down of SPI buffer is enabled
17-17	EN_DYN_PDN_CLKBUF	R/W	0h	0 = Dynamic power down of BF_CLK and TR_BF_SYNC buffer is disabled 1 = Dynamic power down of BF_CLK and TR_BF_SYNC buffer is enabled

Figure 8-86. Register 6E Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-16	EN_CLK_GATE	R/W	0h	0 = Disable dynamic control feature of TR_BF_SYNC, TR_BF_CLK and SPI buffer 1 = Enable dynamic control feature of TR_BF_SYNC, TR_BF_CLK and SPI buffer
15-10	0	R/W	0h	Must read or write 0
9-8	CLK_TERM	R/W	0h	00 = TR_BF_CLK buffer internal termination is set to 100 ohms 01 = TR_BF_CLK buffer internal termination is set to 200 ohms 10 = TR_BF_CLK buffer internal termination is set to 400 ohms 11 = TR_BF_CLK buffer internal termination is set to high impedance
7-6	0	R/W	0h	Must read or write 0
5-4	SYNC_TERM	R/W	0h	00 = TR_BF_SYNC buffer internal termination is set to 100 ohms 01 = TR_BF_SYNC buffer internal termination is set to 200 ohms 10 = TR_BF_SYNC buffer internal termination is set to 400 ohms 11 = TR_BF_SYNC buffer internal termination is set to high impedance
3-3	BF_CLK_DIV_EN	R/W	0h	0 = Beamformer clock divider is disabled 1 = Beamformer clock divider is enabled. Division factor is decided by register bit BF_CLK_DIV
2-2	0	R/W	0h	Must read or write 0
1-0	BF_CLK_DIV	R/W	0h	Valid when BF_CLK_DIV_EN is set to '1' 00 = Divide BF_CLK by 1 01 = Divide BF_CLK by 2 10 = Divide BF_CLK by 4 11 = Divide BF_CLK by 8

8.1.43 Register 6Fh (offset = 6Fh) [reset = 0h]

Figure 8-87. Register 6Fh

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
SDATA_TERM		SEN_TERM		SCLK_TERM		0	0
R/W-0h		R/W-0h		R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-88. Register 6F Field Descriptions

Bit	Field	Type	Reset	Description
31-16	0	R/W	0h	Must read or write 0
15-14	SDATA_TERM	R/W	0h	LVDS SPI SDATA buffer termination programming 00 = Internal termination is set to 400 ohms 01 = Internal termination is set to high impedance 10 = Internal termination is set to 100 ohms 11 = Internal termination is set to 200 ohms
13-12	SEN_TERM	R/W	0h	LVDS SPI SEN buffer termination programming 00 = Internal termination is set to 400 ohms 01 = Internal termination is set to high impedance 10 = Internal termination is set to 100 ohms 11 = Internal termination is set to 200 ohms
11-10	SCLK_TERM	R/W	0h	LVDS SPI SCLK buffer termination programming 00 = Internal termination is set to 400 ohms 01 = Internal termination is set to high impedance 10 = Internal termination is set to 100 ohms 11 = Internal termination is set to 200 ohms
9-0	0	R/W	0h	Must read or write 0

8.1.44 Register 78h (offset = 78h) [reset = C8000000h]

Figure 8-89. Register 78h

31	30	29	28	27	26	25	24
VALID_FLAG_5					0	0	0
R-19h					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	DIS_TRIG_ERR	0	TRIG_ERR	0	STDBY_FLAG
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-90. Register 78 Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VALID_FLAG_5	R	19h	25 = Flag value is valid. For all other values the read flag is not valid
26-5	0	R/W	0h	Must read or write 0
4-4	DIS_TRIG_ERR	R/W	0h	0 = TR_BF_SYNC error detect is enabled 1 = TR_BF_SYNC error detect is disabled
3-3	0	R/W	0h	Must read or write 0
2-2	TRIG_ERR	R	0h	0 = Normal operation 1 = TR_BF_SYNC Error
1-1	0	R/W	0h	Must read or write 0
0-0	STDBY_FLAG	R	0h	0 = Normal operation 1 = STANDBY Error. Indicates STDBY pin is high.

8.1.45 Register 7Bh (offset = 7Bh) [reset = 0h]

Figure 8-91. Register 7Bh

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	DIS_STDBY
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 8-92. Register 7B Field Descriptions

Bit	Field	Type	Reset	Description
31-9	0	R/W	0h	Must read or write 0
8-8	DIS_STDBY	R/W	0h	0 = Normal operation 1 = Ignores the STDBY input and doesn't place the device in STANDBY when the STDBY pin is pulled high.
7-0	0	R/W	0h	Must read or write 0

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Register Configuration Example

Refer to different register configuration example given below to configure device in different modes:

9.1.1.1 B Mode

Register setting given in Table 9-1 configures device to transmit the same B-mode pulses on all the 64 channels.

Table 9-1. B-Mode Register Configuration Example

Address (Hex)	Register Value (Hex)	Comment
0x0	0x00000001	Software reset the device
0x51	0x00050000	Setting CONST_1 and CONST_2 bits to '1'.
0x2	0x0000FFFF	Pattern page select for all 64 channels. Register 0x3 needs to be written if SDATA_1 line is used
Program 0x80 to 0x27F	Xxxx	User can program pattern definition here. Below example setting generates pattern AVDDM_HV => AVDDP_HV => Ground with each of 26 BF_CLK clock duration. 0x87 = 0x30000 (Global repeat = 0, Pattern Length is 3, because there are 3 transitions happening. This is stored in location '7' in the memory) 0x88 = 0xCCC9CD (MHV for 26 clocks, PHV for 26 clocks & RZ for 26 clocks)
Program 0x80 to 0x27F	Xxxx	User can program the delay profile here. Below example setting set the delay of all channels to 10 BF_CLK clock. The information is stored in Register 130 which corresponds to location '2' in the memory. 0x82= 0xA000A, 0x83 = 0xA000A
0x80	0	Setting the T/R Switch ON delays of channels 1,3,5…63 to 0.
0x81	0	Setting the T/R Switch ON delays of channels 2,4,6…64 to 0.
0x2	0x00000000	Deselect all the pages.
0x33	0x7	Setting the Pattern Pointer to 7 which is where the pattern is written above.
0xD	0x20002	Setting delay pointer of Memory Block 1 & 2 to 2.
0xE	0x20002	Setting delay pointer of Memory Block 3 & 4 to 2.
0xF	0x20002	Setting delay pointer of Memory Block 5 & 6 to 2.
0x10	0x20002	Setting delay pointer of Memory Block 7 & 8 to 2.
0x11	0x20002	Setting delay pointer of Memory Block 9 & 10 to 2.
0x12	0x20002	Setting delay pointer of Memory Block 11 & 12 to 2.
0x13	0x20002	Setting delay pointer of Memory Block 13 & 14 to 2.
0x14	0x20002	Setting delay pointer of Memory Block 15 & 16 to 2.
0xB	0x00000002	Enable TR_BF_SYNC

9.1.1.2 CW Mode

Below configuration configures all the 64 channels in continuous CW transmit mode. To configure any channel in receive mode, enable the T/R switch of that particular channel.

Table 9-2. CW Mode Register Configuration Example

Address (Hex)	RegisterValue (Hex)	Comment
0x0	0x00000001	Software reset the device
0x51	0x00050000	Setting CONST_1 and CONST_2 bits to '1'.
0x19	0xFFFFFFFF	Disabling all the T/R Switches of Channels 1,3,5…63.
0x18	0xFFFFFFFF	Disabling all the T/R Switches of Channels 2,4,6…64.
0xC	Xxxx	Program user defined CW pattern. Below example setting configure the CW pattern Definition with AVDDP_HV (26 clocks) => AVDDM_HV (26 clocks) = AVDDP_HV (26 clocks) => AVDDM_HV (26 clocks). 0xC = 0xCFCBCFCB
Program 0x80 to 0x27F	Xxxx	User can program the delay profile here. Below example setting set the delay of all channels to 10 BF_CLK clock. The information is stored in Register 130 which corresponds to location ‘2’ in the memory. 0x82= 0xA000A, 0x83 = 0xA000A
0x2	0x00000000	Deselect all the pages.
0x2E	0xFFFFFFFE	Powering down all channels except Channel 1 to prevent High Power dissipation
0x2D	0xFFFFFFFF	Powering down all channels except Channel 1 to prevent High Power dissipation
0xD	0x20002	Setting delay pointer of Memory Block 1 & 2 to 2.
0xE	0x20002	Setting delay pointer of Memory Block 3 & 4 to 2.
0xF	0x20002	Setting delay pointer of Memory Block 5 & 6 to 2.
0x10	0x20002	Setting delay pointer of Memory Block 7 & 8 to 2.
0x11	0x20002	Setting delay pointer of Memory Block 9 & 10 to 2.
0x12	0x20002	Setting delay pointer of Memory Block 11 & 12 to 2.
0x13	0x20002	Setting delay pointer of Memory Block 13 & 14 to 2.
0x14	0x20002	Setting delay pointer of Memory Block 15 & 16 to 2.
0xB	0x00000003	Enable TR_BF_SYNC & CW_Mode

9.2 Typical Application

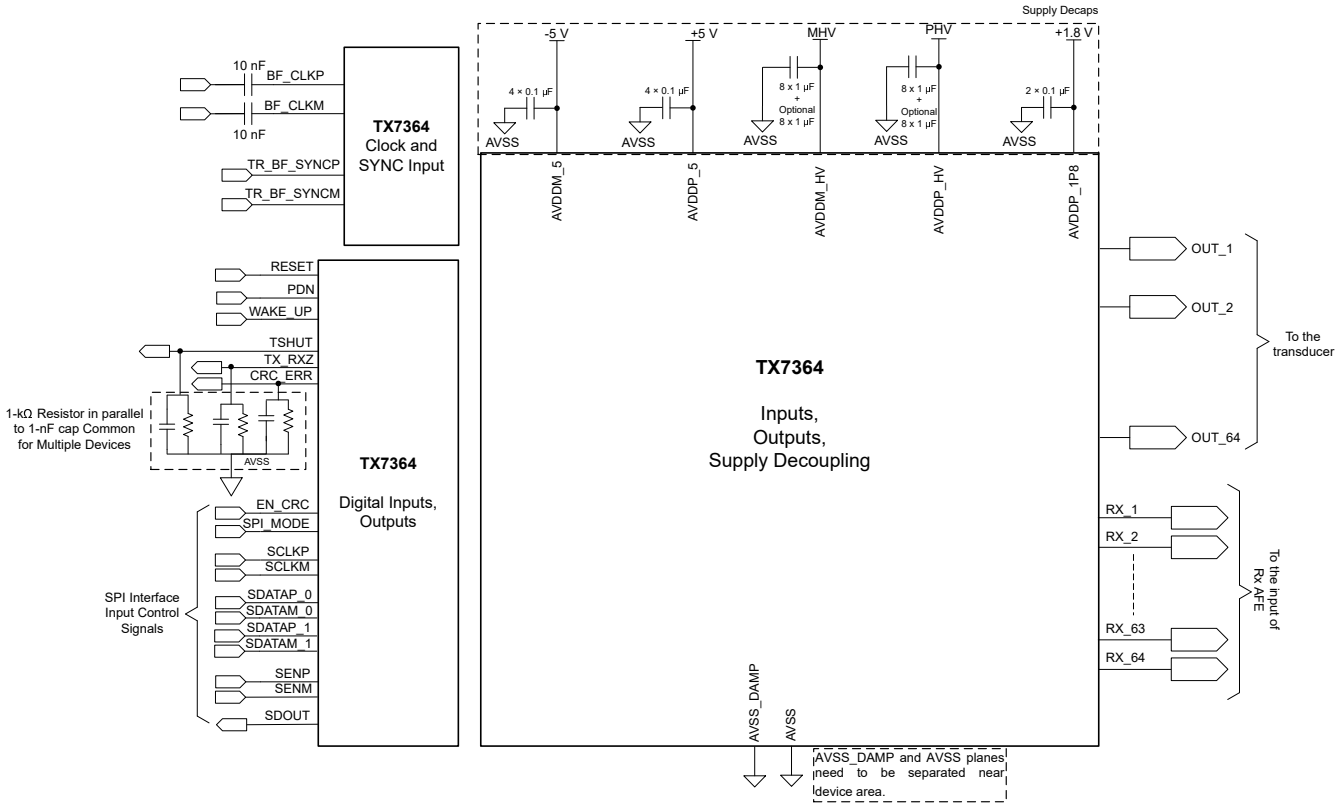


Figure 9-1. Application Circuit

9.2.1 Design Requirements

Table 9-3 lists down the different capacitor specifications connected to different pins of the device.

Table 9-3. Capacitor Specifications

DEVICE PIN	CAPACITOR VALUE IN (µF)	SIZE	VOLTAGE RATING (V)	TOLERANCE	Quantity	Comment (See Section11 for more details)It is assumed that device is placed in the top layer of PCB.
AVDDP_HV, AVDDM_HV.	1	0805	100	10 %	8+ 8 optional	Eight capacitors on thetop layer. It is optional to place anotherfour capacitors in the bottom layer if area is available.
AVDDP_5	0.1	0201	6.3	10%	4	Two capacitors on the top layer and two capacitorsin the bottom layer near to the device pin.
AVDDM_5	0.1	0201	6.3	10%	4	Two capacitors on the top layer and two capacitors on the bottom layer near to the device pin.
AVDDP_1P8	0.1	0201	6.3	10%	2	Two capacitors on the bottom layer near to the device pin.

9.2.2 FPGA Control Signal

To minimize the number of IOs needed from FPGA to control multiple TX7364 devices, scheme described below can be adopted:

- Consider a system with N number of TX7364 devices (64 × N channels system).

- To reduce the number of IOs from FPGA, multiple signals can be shared across TX7364 devices. Table 9-4 lists the signals which can be shared and which one has to be separate across devices.
- Total number of pins from FPGA = 13 + 2N. For 256 channels: 13 + 2 × 4 = 21 pins. TX_RXZ can be taken to FPGA if it is required to know when all the devices are in receive mode.
- Figure 9-2 shows example connection to control 2 devices.

Table 9-4. Control Signal Sharing Scheme

Pin Name	Shared	Comment	Number of pins required from FPGA
SCLK	Yes	SCLK can be fanned directly from FPGA. In the layout, it has to be routed in a daisy chain manner from the first TX7364 device, then to the next TX7364 device and so on. This is to minimize stubs in the trace and minimize reflection and improve signal integrity.	2
SDATA_0/1	No	Keep it separate across devices. By default use SDATA_0 only. In case need to reduce programming time by 2x, SDATA_1 also can be used. In that case number of pins will become 4N instead of 2N. The length matching of SDATA lanes for each device has to be done with respect to the length of the SEN and SCLK trace for that particular device as the SEN and SCLK are routed in a daisy chained manner.	2N
SEN	Yes	SEN can be fanned directly from FPGA. In the layout, it has to be routed in a daisy chain manner from the first TX7364 device, then to the next TX7364 device and so on. This is to minimize stubs in the trace and minimize reflection and improve signal integrity.	2
SDOUT	Yes	Short this pin across devices	1
TR_BF_SYNC	Yes	Use same buffer as BF_CLK signal to fan out to multiple devices example LMK00308. Same type of buffer will be helpful in meeting timing.	2
EN_CRC	Yes	Short this pin across devices	1
TSHUT	Yes	Short this pin across devices and place 1-kΩ resistor and 1-nF capacitor in parallel to ground.	1
CRC_ERR	Yes	Short this pin across devices and place 1-kΩ resistor and 1-nF capacitor in parallel to ground.	1
WAKE_UP	Yes	Short this pin across devices.	1
RESET	Yes	Short this pin across devices.	1
TX_RXZ	Yes	Short this pin across devices and place 1-kΩ resistor and 1-nF capacitor in parallel to ground.	1(Optional)
PDN	Yes	Short this pin across devices	1

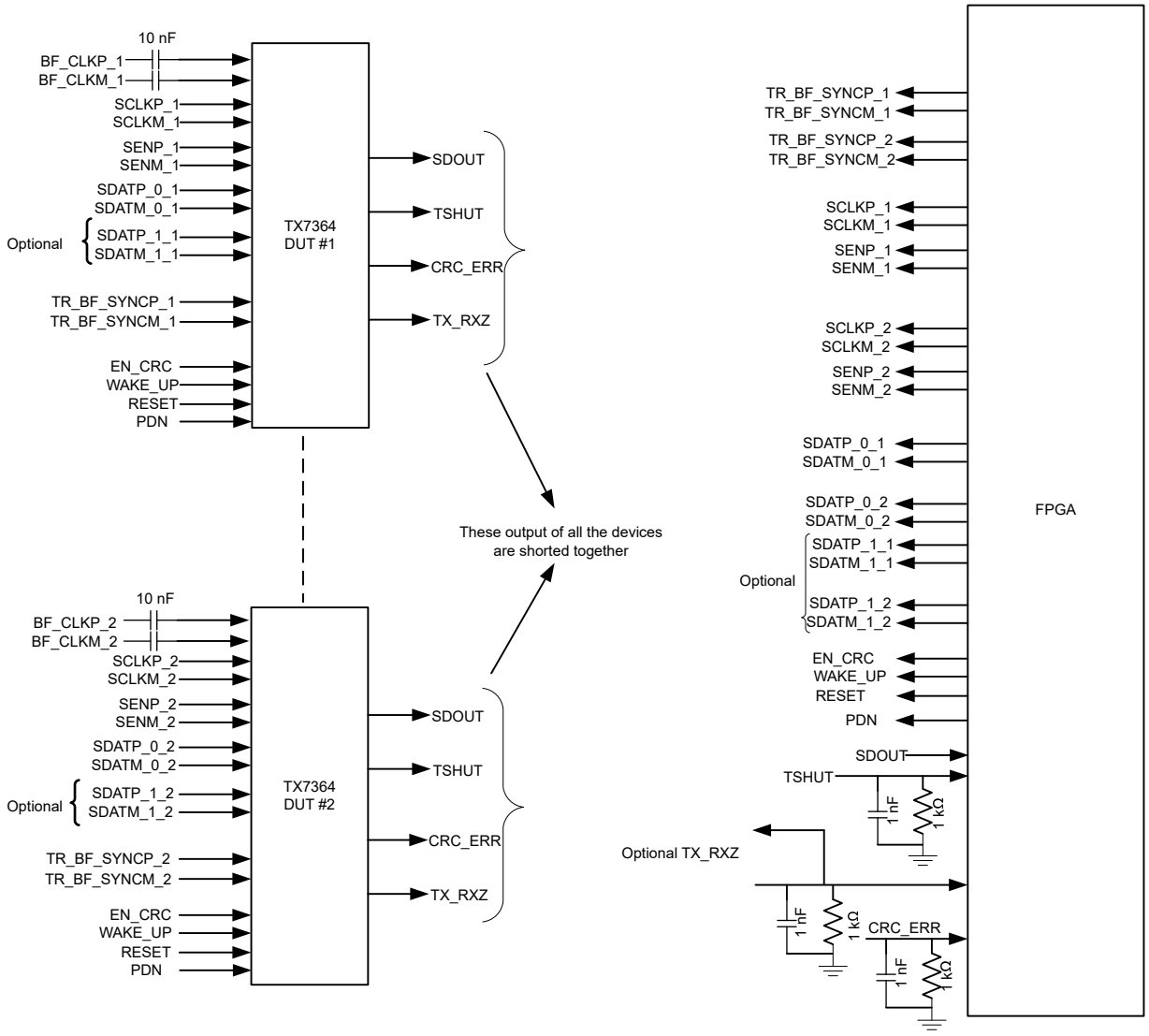


Figure 9-2. TX7364 Control Signal

9.2.3 Detailed Design Procedure

Table 9-5 lists the schematic check list. Review the system schematic using Table 9-5.

Table 9-5. Schematic Checklist

PIN NAME	TI RECOMMENDATION FOR ON-CHIP BEAMFORMING MODE	VERIFIED YES/NO
BF_CLKP, BF_CLKM	Supports only differential input mode: - AC couple BF_CLKP and BF_CLKM signal - Internal 100Ω differential termination is available - Maximum frequency supported 320MHz. For multiple devices in system, the pins need to be separate for each separate device.	
TR_BF_SYNCP, TR_BF_SYNCM	Supports only differential input mode: - DC couple TR_BF_SYNCP and TR_BF_SYNCM signal - Internal 100Ω differential termination is available. For multiple devices in system, the pins need to be separate for each separate device.	
RESET	Connect to FPGA to reset the device	

Table 9-5. Schematic Checklist (continued)

PIN NAME	TI RECOMMENDATION FOR ON-CHIP BEAMFORMING MODE	VERIFIED YES/NO
SPI signals	For differential input mode: - DC couple SCLKP/M, SENP/M, SDATAP/M_0, and SDATAP/M_1 signals. - If do not want to use SDATAP/M_1 pins for SPI communication then connect SDATAP_1 to ground with 10kΩ resistor and connect SDATAM_1 to AVDDP_1P8 with 10kΩ resistor. - Connect SPI_MODE pin to ground -Internal termination of 100Ω is available. - Maximum frequency supported for SPI write is 400MHz and for SPI read is 10MHz.	
	For single ended input mode: - Connect SCLKM, SENM, SDATAM_0 and SDATAM_1 to ground. - Apply SCLKP, SENP, SDATAP_0 and SDATAP_1 with AVDDP_1P8 logic level - If do not want to use SDATAP_1 for SPI communication then connect SDATAP_1 directly to ground. - Connect SPI_MODE pin to AVDDP_1P8 supply. - Maximum frequency supported for SPI write is 50MHz and for SPI read is 10MHz.	
EN_CRC	Connect EN_CRC to FPGA if the user wants to use SPI CRC check feature of the device. Otherwise connect the pin to ground.	
TSHUT	Output of multiple devices can be shorted together. Place external pull down 1kΩ and 1nF capacitor resistor to ground.	
CRC_ERR	Output of multiple devices can be shorted together. Place external pull down 1kΩ and 1nF capacitor resistor to ground.	
PDN	Connect to FPGA to power down the device using pin control.	
TX_RXZ	Output of multiple devices can be shorted together. Place external pull down 1kΩ and 1nF capacitor resistor to ground. .	
WAKE_UP	WAKE_UP must be connected to FPGA. Input of multiple devices can be shorted together.	
AVDDM_5	Voltage level has to be –5V. Connect minimum of 4 × 0.1µF capacitors of 0201 size.	
AVDDM_HV	If supply absolute voltage is > 90V, then use minimum of 4 × 1µF cap of > 100V rating with 0805 size. If supply voltage is < 90V, then use minimum of 4 × 1µF cap of 100V rating with 0805 size. If area is available, then another 4 × 1µF capacitors can be placed in opposite PCB layer of the device.	
AVDDP_5	Voltage level must be 5V. Connect minimum of 4 × 1µF capacitors of 0201 size.	
AVDDP_HV	If supply voltage is > 90V then use minimum of 4 × 1µF cap of > 100V rating with 0805 size. If supply voltage is < 90V then use minimum of 4 × 1µF cap of 100V rating with 0805 size. If area is available then another 4 × 1µF capacitors can be placed in opposite PCB layer of the device.	
AVDD_IP8	Voltage level has to be 1.8V. Connect minimum of 2 × 1µF cap.	

9.2.3.1 Reference Design for Power Supply

Block	TI Recommended Parts	Specifications
HV Power Supply	LM5158(85V/3A): SEPIC+CUK converter DAC53401: DAC to adjust output voltage LM5155 and CSD19537Q3 (MOSFET)	The LM5158 and DAC53401 can together give a maximum output voltage and current of ±2.5V≈±75V/±50mA Maximum input voltage: 5V The LM5155 and CSD19537Q3 can together give a maximum output voltage and current of ±2.5V≈±75V/±100mA Maximum input voltage: 10V
Clocking Scheme	System oscillator: LMK6D Clock Buffer: LMK1D1204	The oscillator supports LVDS output, multiple frequencies in a 3.2mmx2.5mm package. The clock buffer supports a 1:4 fanout. Input voltage range is from 1.7-3.4V. Maximum frequency supported is 2GHz.

Block	TI Recommended Parts	Specifications
Charger (Battery System)	BQ25790, BQ25638	BQ25790 supports 1 to 4 cells batter with a maximum of 5A charger current. Small package. BQ25638 supports 1 cell batter with a maximum of 5A charger current. Comes in 2.6mm × 2.1mm package.

Refer to TIDA-010057 reference design for ultrasound smart probe power supply reference design (https://www.ti.com/tool/TIDA-010057).

Maximum current consumed by low voltage (AVDDP_1P8, AVDDP_5 and AVDDM_5) and high voltage power supplies (AVDDP_HV and AVDDM_HV) in the device is decided by CW mode. In Figure 6-8 CW mode typical supply current plots are given. Check the supply current based on use condition and keep 30% to 50% margin to decide maximum current consumed by the supply.

9.2.4 Application Curves

Figure 6-1 illustrates the total power in mW versus pulse repetition time (PRT). To measure the power, device is configured to generate patterns shown in Figure 7-1 on all the 64 channels with 0 transmit delay beamforming in default power mode. The PRT is same as TR_BF_SYNC signal period. When PRT reduces, the high voltage pulses are fired more often therefore the device power increases.

Figure 6-2 illustrates the total power in mW v/s high voltage supply. The |AVDDP/M_HV| supplies are swept from 5V to 100V. The device is configured to generate patterns shown in Figure 7-1 on all the 64 channels with 0 transmit delay beam forming. As the power supply magnitude increases, the load current increases which results in increase of the device power.

Figure 6-3 shows low voltage supplies current across PRT. It is clear from the figure that low voltage supplies current does not depend on PRT. Also low voltage supplies current does not depend upon the high supply voltage level.

Figure 6-4 shows high voltage supplies current across PRT. As PRT reduces, the high voltage pulses are transmitted more often, hence current increases.

Figure 6-5 shows high voltage supplies current across high voltage supply. As supply voltage increases, the load current increases which is delivered by high voltage supplies.

Figure 6-6 shows AVDD_1P8 supply current across BF_CLK clock frequency. Using dynamic clock power mode the AVDDP_1P8 supply current can be reduced. Between default and dynamic clock power mode none of the other supplies current changes. Also other than AVDDP_1P8 supply, none of other supplies current changes with BF_CLK clock frequency.

Figure 6-7 illustrates the total power in mW vs Output frequency when the device is operated in CW mode. The |AVDDP/M_HV| supplies are kept at 5V. A periodic square wave pattern is generated by toggling the output between AVDDP_HV and AVDDM_HV using the CW pattern generator. The frequency of the pattern is varied by changing the number of clocks in each CW level and/or by using Pattern clock divider. The power shown in the graph is for 32 channel excitation.

Figure 6-8 illustrates the currents drawn from mentioned supplies for the same conditions as explained for Figure 6-7. The currents shown in the graph is for 32 channel excitation with Return to Zero waveform.

Figure 6-9 illustrates the currents drawn from mentioned supplies for the same conditions as explained for Figure 6-7. The currents shown in the graph is for 32 channel excitation with Non-return to Zero waveform.

Figure 6-10 illustrates the time domain result of pulse inversion test. A single channel pulser of the device is first excited with the positive polarity waveform followed by negative polarity waveform of frequency 5MHz. Both the waveforms are captured on scope and summed to get the second harmonic component in the waveform. This test estimates the quality of second harmonic imaging used in ultrasound system.

Figure 6-11 illustrates the FFT of signals shown in Figure 6-9. The fundamental power cancels out on summing positive and inverted waveforms but second harmonic adds up and increases the HD2 power by 6dB. The device achieves fundamental cancellation and HD2 > 40dBc.

Figure 6-12 illustrates the time domain result of pulse inversion test at lower value of High Voltage Supply. The |AVDDP/M_HV| supplies are kept at 2.5V. A single channel pulser of the device is first excited with the positive polarity waveform followed by negative polarity waveform of frequency 5MHz. Both the waveforms are captured on scope and summed to get the second harmonic component in the waveform. This test estimates the quality of second harmonic imaging used in ultrasound system.

Figure 6-13 illustrates the FFT of signals shown in Figure 6-11. The fundamental power cancels out on summing normal and inverted waveforms but second harmonic adds up and increases the HD2 power by 6dB. The device achieves fundamental cancellation and HD2 > 40dBc.

Figure 6-14 illustrates the rise time for ground to AVDDP_HV transition and fall time for ground to AVDDM_HV transition across AVDDP/M_HV supplies. The plot shows that the rise and fall are matched within 1ns across high voltage supply range. This matching is critical to meet the HD2 performance across supply.

Figure 6-15 illustrates the rise time for AVDDM_HV to AVDDP_HV transition and fall time for AVDDP_HV to AVDDM_HV transition across AVDDP/M_HV supplies. The plot shows that the rise and fall are matched within 1ns across high voltage supply range. This matching is critical to meet the HD2 performance across supply.

Figure 6-16 illustrates the rise time for AVDDM_HV to ground transition and fall time for AVDDP_HV to ground transition across AVDDP/M_HV supplies. The plot shows that the rise and fall are matched within 1ns across high voltage supply range. This matching is critical to meet the HD2 performance across supply.

Figure 6-17 illustrates the HD2 performance of pulser output at 5MHz across AVDDP/M_HV supplies for different AVDDP/M_HV supplies. The pattern used for measuring HD2 is a 3-Level waveform pulsing between AVDDP_HV and AVDDM_HV of the pulser. 5MHz, 5-cycles waveform is used for HD2 measure with single channel excited at a time. Good HD2 across supply is required in ultrasound system to get good harmonic imaging.

Figure 6-18 illustrates the HD2 performance of pulser output for AVDDP/M_HV at ±100/70 V across frequency. The pattern used is 3-Level waveform pulsing between AVDDP/M_HV. To measure HD2, single channel is excited at a time.

Figure 6-19 illustrates the HD2 performance of pulser output at 5MHz across high voltage supply for different temperature condition. The pattern used for measuring HD2 is a 3-level waveform pulsing between AVDDP_HV and AVDDM_HV of the pulser. 5MHz, 5-cycles waveform is used for HD2 measure with single channel is excited at a time. Good HD2 across supply and temperature is required in ultrasound system to get good harmonic imaging.

Figure 6-20 illustrates the HD2 performance of pulser output at 5MHz across high voltage supply without any load connected to the pulser output . To measure HD2, single channel is excited at a time. Without load performance is shown to demonstrate the device inherent HD2 performance. Good HD2 across supply is required in ultrasound system to get good harmonic imaging. The three plots represent the typical, minimum, and maximum HD2 observed after characterizing the performance on three devices.

Figure 6-21 illustrates the HD2 performance of pulser output at 5MHz across high voltage supply for 2KΩ||125pF load . To measure HD2, single channel is excited at a time. Good HD2 across supply is required in ultrasound system to get good harmonic imaging. The three plots represent the typical, minimum, and maximum HD2 observed after characterizing the performance on three devices.

Figure 6-22 illustrates the pulser normalized amplitude across frequency for different AVDDP/M_HV supplies. To perform this measurement the peak to peak amplitude of pulser output is measured across frequency and normalized it with respect to peak to peak amplitude at 1MHz for different high voltage supply values. As the high voltage supply value reduces, the pulser peak to peak swing also reduces that helps in getting the higher bandwidth for lower supply voltage.

Figure 6-23 shows pulser output parasitic capacitor across high voltage supplies.

Figure 6-24 illustrates the AVDDP_HV and AVDDM_HV power supply rejection ratio (PSRR) across frequency. The PSRR of the device is measured by applying a known amplitude signal at high voltage supply across frequency and measuring the same frequency component amplitude at RX_n node. The device is programmed in receive mode with T/R switch ON while performing PSRR measurement. For measuring PSRR, RX_n node is connected to 100 Ω resistance in parallel with 20-pF capacitance and OUT_n node connected to 220-Ω resistance in parallel with 220-pF capacitance. The PSRR scales directly with the total load connected at OUT_n and RX_n node. At system level the RX_n node gets connected to the input of very high gain ultrasound analog front end. So total channel gain and PSRR of the device should be considered while deciding the power supply noise level.

Figure 6-25 illustrates the AVDDP_5, AVDDM_5, and AVDDP_1P8 power supply rejection ratio (PSRR) across frequency. The PSRR of the device is measured by applying a known amplitude signal at corresponding supply across frequency and measuring the same frequency component amplitude at RX_A/Bn node. The pulser is programmed in high impedance mode and T/R switch is kept ON while performing PSRR measurement. For measuring PSRR, RX_n node is connected to 100-Ω resistance in parallel with 20-pF capacitance and OUT_n node connected to 400-Ω resistance in parallel with 110-pF capacitance. The PSRR of AVDDP_5 supply scales directly with the total load connected at OUT_n and RX_n node. At system level the RX_n node gets connected to the input of very high gain ultrasound analog front end. So total channel gain and PSRR of the device should be considered while deciding the power supply noise level.

Figure 6-26 illustrates the time domain waveform at pulser output node (OUT_n) when T/R switch turns ON.

Figure 6-27 illustrates the time domain waveform at pulser output node (OUT_n) when T/R switch turns OFF.

Figure 6-28 illustrates the time domain waveform measured at RX_n node when pulser generates the large voltage output. This data shows the good isolation performance from T/R switch.

9.3 Best Design Practices

Take care of following points while working with the TX7364 device:

1. The content of delay and pattern profile register maps are undefined on power up and after applying a reset. Users must configure delay and pattern profile register maps as per requirements.
2. While probing the device supply or any node take extra precaution. Shorting any node to any other node while probing shall damage the device.
3. The maximum speed supported for SPI write and read operation is different. For SPI write, the maximum speed is 400MHz while SPI read can operate at maximum speed of 10MHz.
4. If the device is kept in receive mode for greater than 100ms, then need to power up the floating LDO using steps explained in Section 7.3.5.
5. If temperature shutdown threshold is increased to 125ºC, then take extra precaution and avoid consuming very high instantaneous power.
6. Make sure that the schematic and layout recommendations given in this document are followed for system board design.

9.4 Initialization Setup

To initialize device, follow these steps:

1. Bring up all the power supplies. Any power up sequencing is okay. For AVDDDP/M_HV supplies the maximumslew rate allowed is 200 V/ms. Keep TR_BF_SYNC, RESET and WAKE_UP signal to low while powering up the device. The status of other pins is ‘don't care’.
2. After all the supplies are up wait for 100µs.
3. Apply a pulse on the RESET pin with minimum pulse duration of 1µs.
4. Wait for 1ms.
5. Set CONST_1 and CONST_2 bits in Register 81 (decimal) to '1'.
6. Write user defined register settings.
7. Apply WAKE_UP signal for 200µs to power up the floating LDOs.
8. Apply TR_BF_SYNC pulse signal. Device operates as per the user-defined settings.

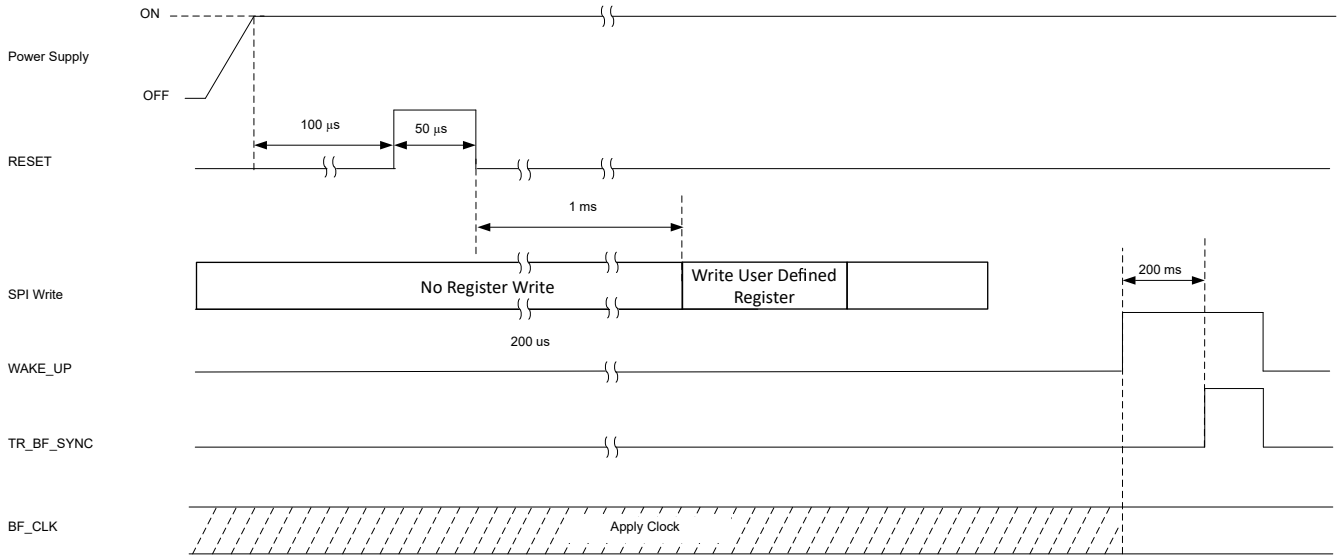


Figure 9-3. Initialization Sequence in On-chip Beamforming Mode

9.5 Power Supply Recommendations

No specific power sequencing is required. Device shall be powered-up and powered-down in any sequence. For AVDDDP/M_HV supplies the maximum slew rate allowed is 200 V/ms.

9.6 Layout

9.6.1 Layout Guidelines

In high-voltage, high-speed devices, most of the switching currents are provided by external decoupling capacitors. Hence, any inductance on the supply path can affect the device performance. For the device, care must be taken to ensure that the supply decoupling capacitors are as close to the device as possible. Also, the current return path must be short as possible. Place multiple vias on the supply path whenever possible.

TX7364 EVM layout can be used as a reference.

Table 9-6 lists the TI recommended placement and routing strategy. It is assumed that the device is placed on the top layer.

Some important points to remember during laying out the board are:

1. Supply decoupling capacitors:
   a. At least one decoupling capacitor for each HV supply pin must be on the same layer as that of the device.
   b. The HV pulses signal current flows through the capacitance connected on HV supplies to ground. In the system, the supply planes can be couple of layers apart from the external layers, and the via inductance can be significant. Hence, there must be a HV supply patch just below the device plane so that the return current has the lowest inductance path. See Figure 9-5 for reference.
   c. AVDDP_5 and AVDDM_5 must have at least two set of decoupling capacitors in the same layer as that of the device.
   d. Place multiple vias for all the supplies to reduce the path inductance.
2. Length matching (tolerance of 100 mils when not specified):
   a. The BF_CLKP and BF_CLKM must be routed as differential pair of 100 Ω (length matched to 5 mils).
   b. TR_BF_SYNCP and TR_BF_SYNCM must be routed as differential pair of 100 Ω (length matched to 5 mils). They must be length matched to BF_CLK as the device latches TR_BF_SYNC on BF_CLK.
   c. SPI data, enable and clock signals must be routed as differential pair of 100 Ω (length matched to 5 mils)when SPI mode is configured in LVDS mode and as 50 Ω trace when SPI mode is CMOS mode. The device supports high-speed SPI (400 MHz in LVDS mode). Hence, the SPI lines must be length matched.

3. Crosstalk and reflection reduction:
   a. To minimize cross-talk between the channels, OUTs must not be routed parallel to each other in adjacent layers as it leads to parasitic capacitors between channels.
   b. RX lines must be impendence controlled to reduce reflection artifacts.
   c. AVSS and AVSS_DAMP ground should be separated to avoid high current carrying ground bounce coupling to clean ground AVSS which is used by low voltage circuit in the device.

Table 9-6. Placement and Routing Checklist

PIN NAME	TI RECOMMENDED PLACEMENT AND ROUTING STRATEGY	VERIFIED YES/NO
AVDDP/M_HV	Place as many as possible HV decoupling capacitors on the top layer. In the system, the supply planescan be couple of layers apart from the external layers and the via inductance can be significant. Hence, there should be a HV supply patch just below the device plane. This ensures that HV supply return current has the lowest inductance path. See Figure 9-5 for reference.	
AVDDP/M_5	Placethe decoupling capacitor as close to the device as possible, either in the top layer or the bottom layer.	
BF_CLK and TR_BF_SYNCpins	Routethe pair as differential 100-Ω trace (length matched to 5 mils). Length match the TR_BF_SYNC signal routing to BF_CLK signal routing.	
OUT pins	Avoid routing two OUT signals parallel to each other in adjacent layers. This is to limit the parasitic capacitor between different OUT signals to get good cross talk performance. For 220-pFload capacitance a small parasitic capacitance of 1 pF between the two OUT signals can degrade cross talk to -47 dBc.	
SPI control pins	Needto take care of signal integrity to ensure SPI works till 400-MHz frequency. Length match the SCLK and SDATA* signals to meet timing.	
RX pins	Take care of signal integrity to avoid reflection because of echo signal coming from the transducer.TI recommends to terminate the RX* signal near to RX device with source (and trace) matching impedance.	
AVSS and AVSS_DAMP	AVSS_DAMPcarries very high current. It has to be separated from AVSS on all the PCB layers as per suggestion given in Figure 9-7.	

9.6.2 Layout Example

Figure 9-4 to Figure 9-9 show the example layout for different layers of the PCB.

1. **Top layer**: Figure 9-4 and Figure 9-5 show the placement and layout recommendations of the PCB layer where device is mounted. All the high voltage supplies have four decoupling capacitors placed in top layer to get lowest parasitic inductance. High voltage supplies carry very large switching current and low parasitic inductance on supply capacitor is needed to achieve the good performance from the device hence it has been placed in the same layer as of device. Similarly, two AVDDP_5 supply decoupling capacitors, two AVDDM_5 supply decoupling capacitors, are placed in top layer as shown in Figure 9-5.
2. **Layer two**: Figure 9-6 shows second layer layout recommendation which is the next layer of the layer where device is mounted. High voltage and low voltage supplies patches are added and connected in parallel to the top layer to further reduce the supply inductance by introducing current parallel path.
3. **Ground plane**: AVSS_DAMP ground carries very large current when pulser output goes to return to zero state. Largecurrent in AVSS_DAMP shall lead to transient voltage glitch in AVSS_DAMP plane. To avoid this glitch to couple to AVSS, AVSS and AVSS_DAMP planes are separated as shown in Figure 9-7.The same separation scheme should be used for all the layers in PCB.
4. **Bottom layer**: Place two decap to AVSS for AVDDM_5, AVDDP_5 and AVDDP_1P8 near the device pins as shown in Figure 9-8.These decaps should not be referred to AVSS_DAMP. Layout example of bottom layer is shown in Figure 9-9.

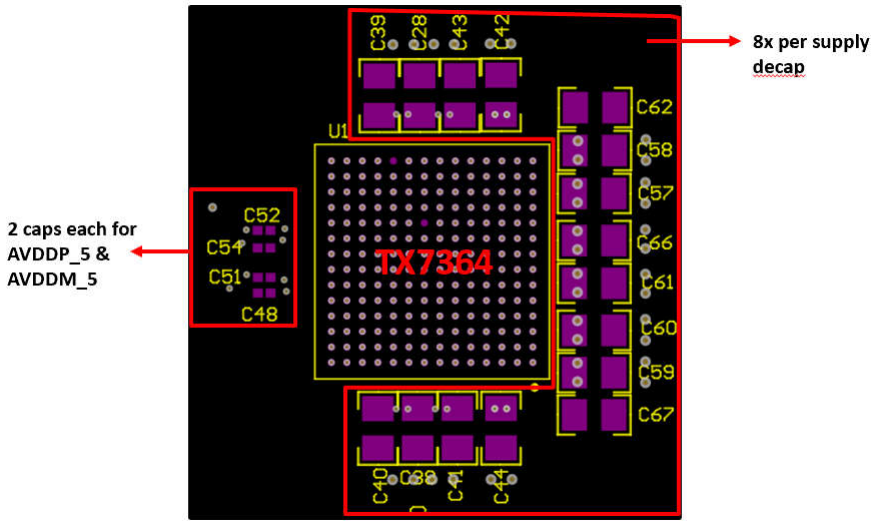


Figure 9-4. Top Layer Placement

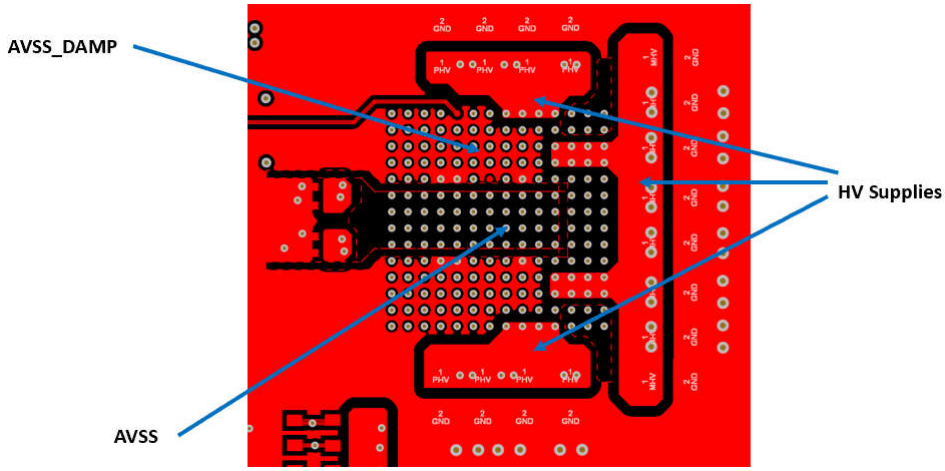


Figure 9-5. Top Layer Layout

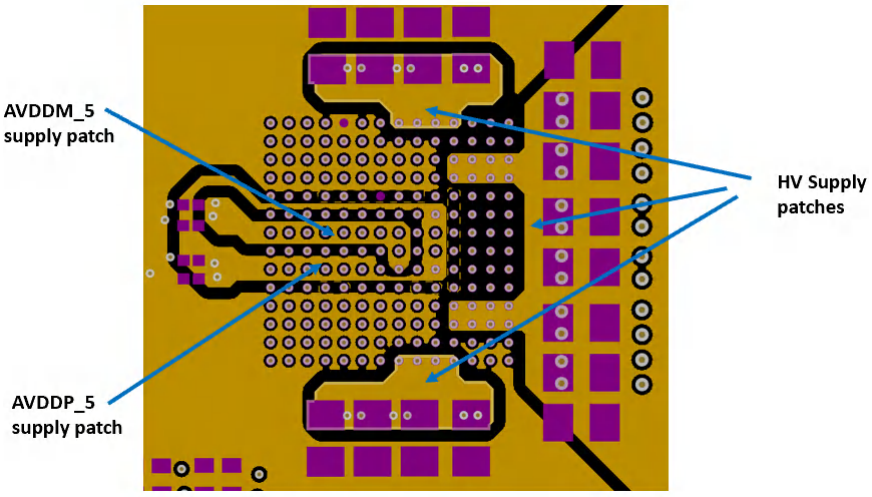


Figure 9-6. Layer Two Layout

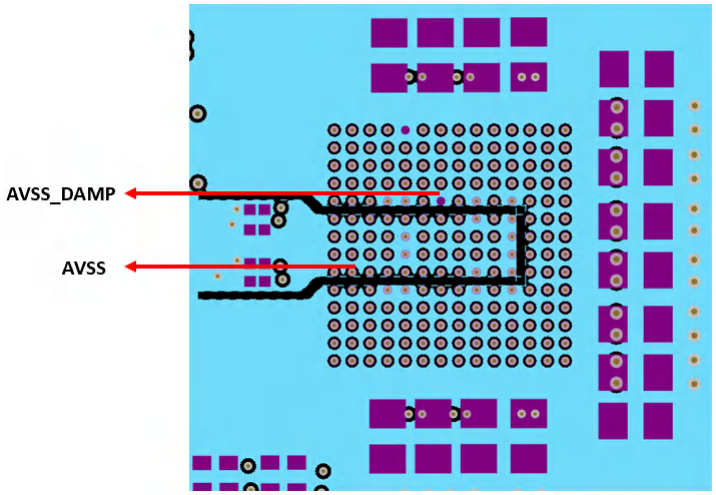


Figure 9-7. Ground Plane

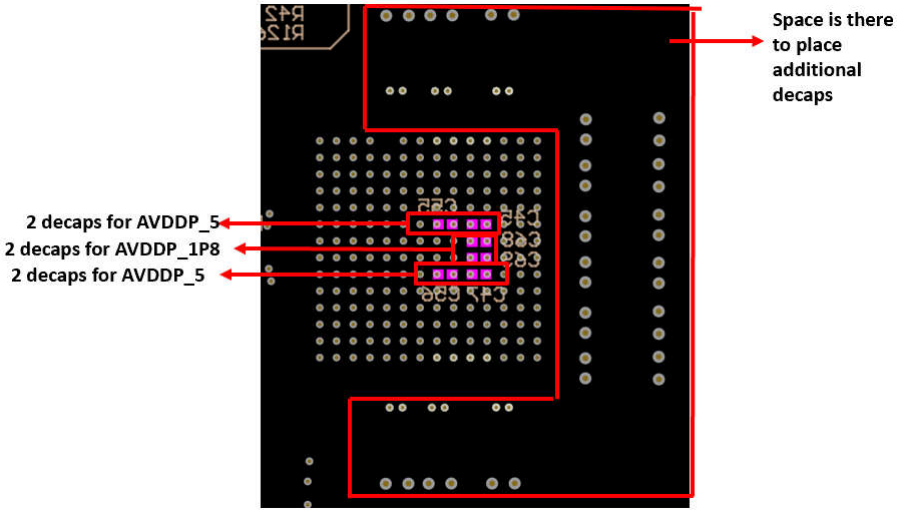


Figure 9-8. Bottom Layer Placement

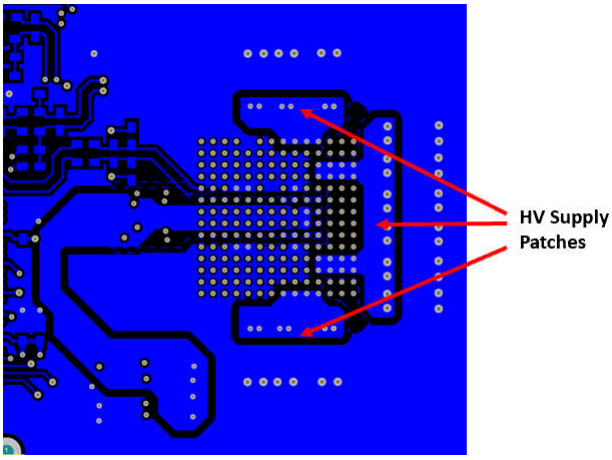


Figure 9-9. Bottom Layer Layout

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

Abbreviation	Comment
PRT	Pulse Repetition Time. Represent TR_BF_SYNC period
PRF	Pulse Repetition Frequency. Represent TR_BF_SYNC frequency
Receive Mode	Duration in which T/R switch of all the channels are in ON state
High Voltage Supplies	AVDDP_HV and AVDDM_HV are collectively referred as high voltage supplies
Low Voltage Supplies	AVDDP_5, AVDDM_5, and AVDDP_1P8 supplies are collectively referred as low voltage supplies
SPI	Serial program interface

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

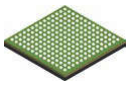
DATE	REVISION	NOTES
April 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

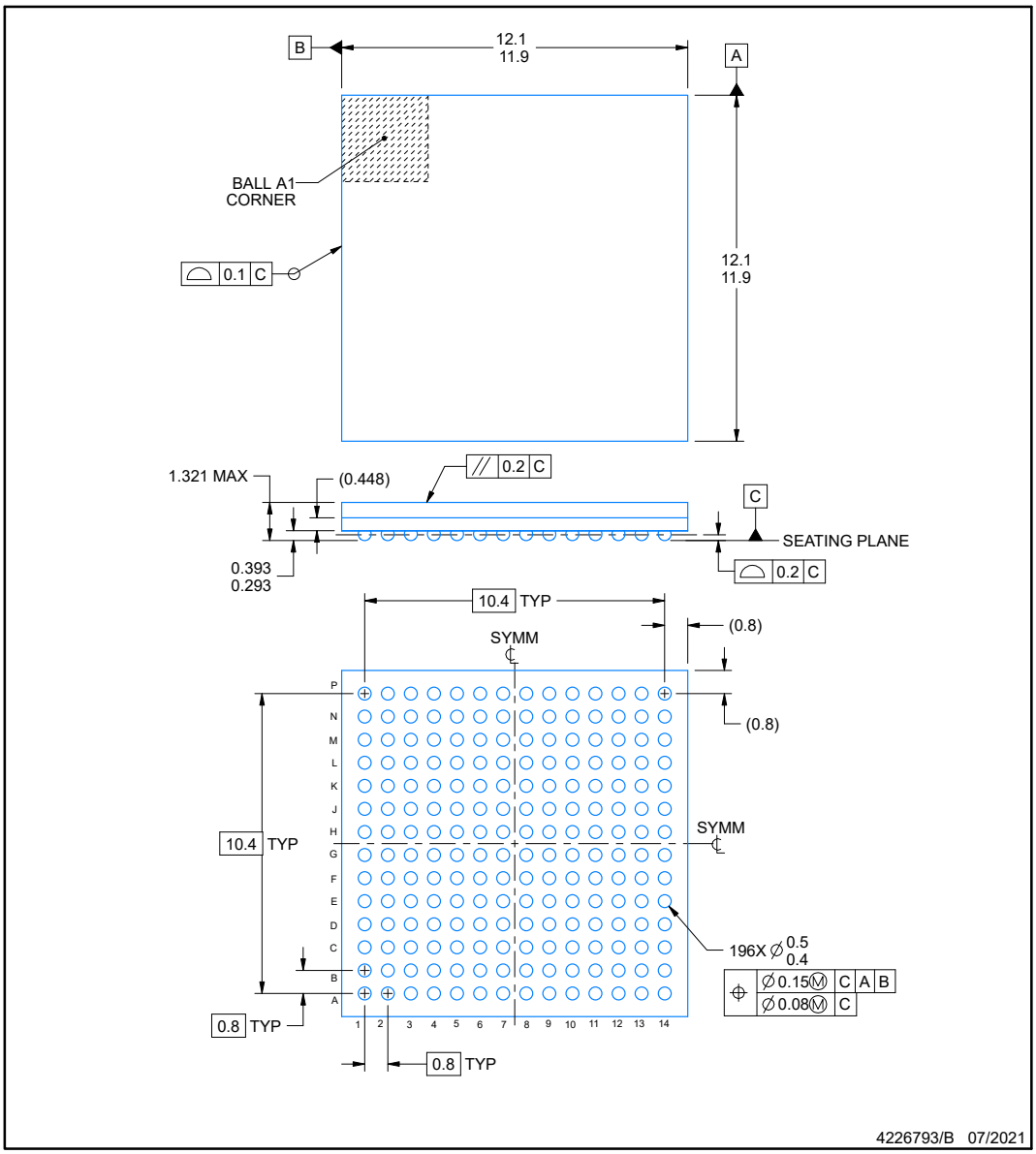
PACKAGE OUTLINE

ACP0196A



FCBGA - 1.321 mm max height

BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

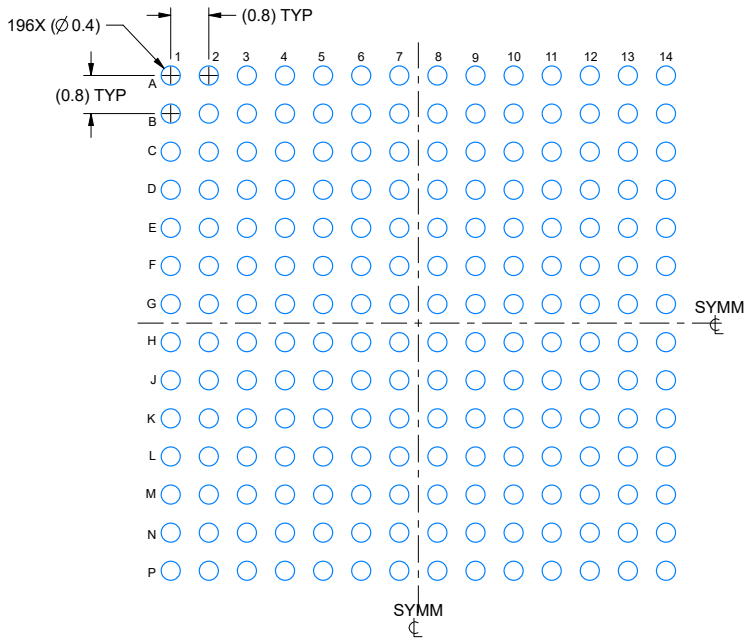
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

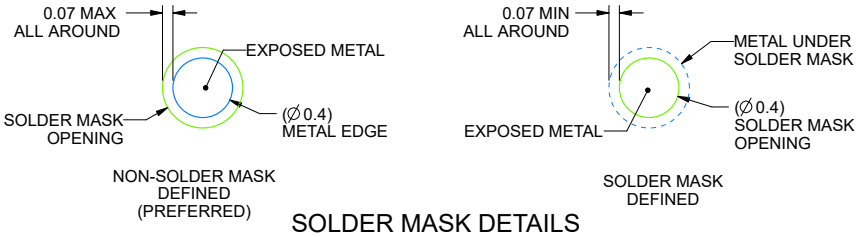
ACP0196A

FCBGA - 1.321 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS
NOT TO SCALE

4226793/B 07/2021

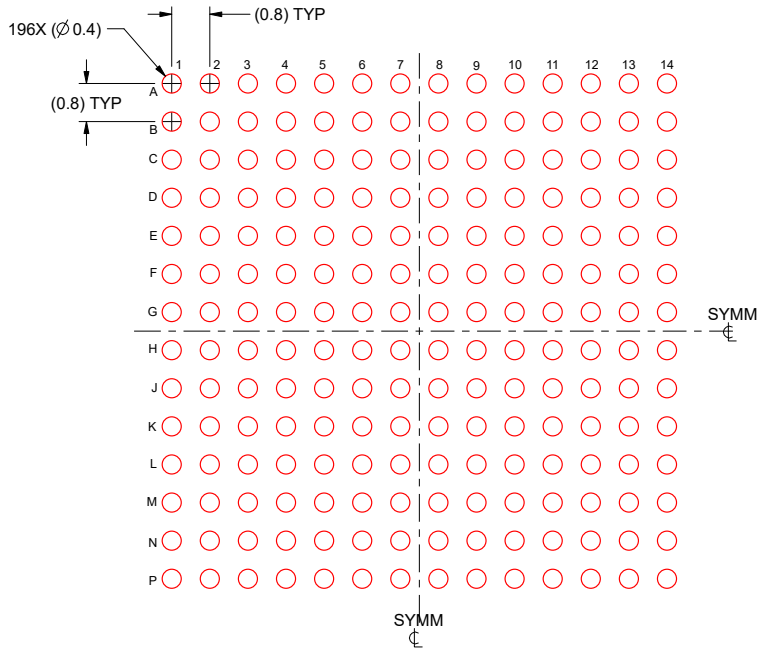
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ACP0196A — **FCBGA - 1.321 mm max height**

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4226793/B 07/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

12.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
TX7364ACP	ACTIVE	FCCSP	ACP	196	189	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0°C to 70°C	TX7364

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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