

MIXED SIGNAL MICROCONTROLLER

FEATURES

- **Low Supply-Voltage Range:** 1.8 V to 3.6 V
- **Ultra-Low Power Consumption**
 - **Active Mode:** 230 μ A at 1 MHz, 2.2 V
 - **Standby Mode:** 0.5 μ A
 - **Off Mode (RAM Retention):** 0.1 μ A
- **Five Power-Saving Modes**
- **Ultra-Fast Wake-Up From Standby Mode in Less Than 1 μ s**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Basic Clock Module Configurations**
 - **Internal Frequencies up to 16 MHz With Four Calibrated Frequency**
 - **Internal Very-Low-Power Low-Frequency (LF) Oscillator**
 - **32-kHz Crystal**
 - **External Digital Clock Source**
- **Two 16-Bit Timer_A With Three Capture/Compare Registers**
- **Up to 24 Touch-Sense-Enabled I/O Pins**
- **Universal Serial Communication Interface (USCI)**
 - **Enhanced UART Supporting Auto Baudrate Detection (LIN)**
 - **IrDA Encoder and Decoder**
 - **Synchronous SPI**
 - **I²C™**
- **On-Chip Comparator for Analog Signal Compare Function or Slope Analog-to-Digital (A/D) Conversion**
- **10-Bit 200-kSPS Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan (See Table 1)**
- **Brownout Detector**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **On-Chip Emulation Logic With Spy-Bi-Wire Interface**
- **Family Members are Summarized in Table 1**
- **Package Options**
 - **TSSOP: 20 Pin, 28 Pin**
 - **PDIP: 20 Pin**
 - **QFN: 32 Pin**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide (SLAU144)***

DESCRIPTION

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μ s.

The MSP430G2x13 and MSP430G2x53 series are ultra-low-power mixed signal microcontrollers with built-in 16-bit timers, up to 24 I/O touch-sense-enabled pins, a versatile analog comparator, and built-in communication capability using the universal serial communication interface. In addition the MSP430G2x53 family members have a 10-bit analog-to-digital (A/D) converter. For configuration details see Table 1.

Typical applications include low-cost sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system.



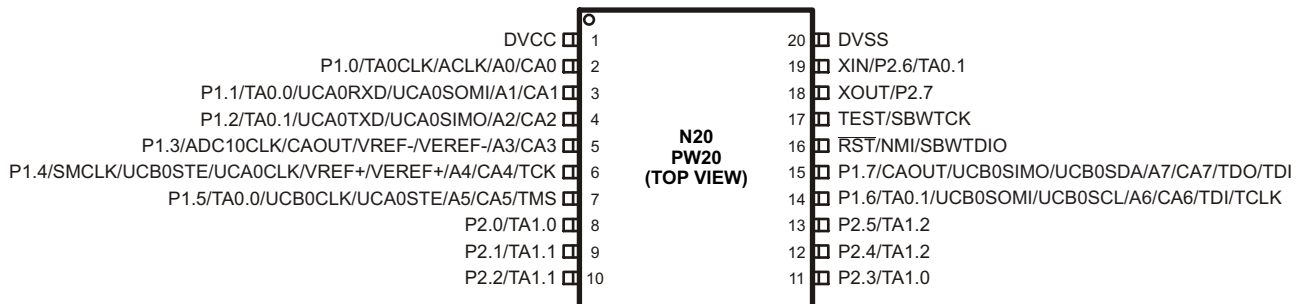
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Table 1. Available Options⁽¹⁾⁽²⁾

| Device | BSL | EEM | Flash (KB) | RAM (B) | Timer_A | COMP_A+ Channel | ADC10 Channel | USCI_A0, USCI_B0 | Clock | I/O | Package Type |
|-------------------|-----|-----|------------|---------|---------|-----------------|---------------|------------------|--------------|-----|--------------|
| MSP430G2553IRHB32 | 1 | 1 | 16 | 512 | 2x TA3 | 8 | 8 | 1 | LF, DCO, VLO | 24 | 32-QFN |
| MSP430G2553IPW28 | | | | | | | | | | 24 | 28-TSSOP |
| MSP430G2553IPW20 | | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2553IN20 | | | | | | | | | | 16 | 20-PDIP |
| MSP430G2453IRHB32 | 1 | 1 | 8 | 512 | 2x TA3 | 8 | 8 | 1 | LF, DCO, VLO | 24 | 32-QFN |
| MSP430G2453IPW28 | | | | | | | | | | 24 | 28-TSSOP |
| MSP430G2453IPW20 | | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2453IN20 | | | | | | | | | | 16 | 20-PDIP |
| MSP430G2353IRHB32 | 1 | 1 | 4 | 256 | 2x TA3 | 8 | 8 | 1 | LF, DCO, VLO | 24 | 32-QFN |
| MSP430G2353IPW28 | | | | | | | | | | 24 | 28-TSSOP |
| MSP430G2353IPW20 | | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2353IN20 | | | | | | | | | | 16 | 20-PDIP |
| MSP430G2253IRHB32 | 1 | 1 | 2 | 256 | 2x TA3 | 8 | 8 | 1 | LF, DCO, VLO | 24 | 32-QFN |
| MSP430G2253IPW28 | | | | | | | | | | 24 | 28-TSSOP |
| MSP430G2253IPW20 | | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2253IN20 | | | | | | | | | | 16 | 20-PDIP |
| MSP430G2153IRHB32 | 1 | 1 | 1 | 256 | 2x TA3 | 8 | 8 | 1 | LF, DCO, VLO | 24 | 32-QFN |
| MSP430G2153IPW28 | | | | | | | | | | 24 | 28-TSSOP |
| MSP430G2153IPW20 | | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2153IN20 | | | | | | | | | | 16 | 20-PDIP |
| MSP430G2513IRHB32 | 1 | 1 | 16 | 512 | 2x TA3 | 8 | - | 1 | LF, DCO, VLO | 24 | 32-QFN |
| MSP430G2513IPW28 | | | | | | | | | | 24 | 28-TSSOP |
| MSP430G2513IPW20 | | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2513IN20 | | | | | | | | | | 16 | 20-PDIP |
| MSP430G2413IRHB32 | 1 | 1 | 8 | 512 | 2x TA3 | 8 | - | 1 | LF, DCO, VLO | 24 | 32-QFN |
| MSP430G2413IPW28 | | | | | | | | | | 24 | 28-TSSOP |
| MSP430G2413IPW20 | | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2413IN20 | | | | | | | | | | 16 | 20-PDIP |
| MSP430G2313IRHB32 | 1 | 1 | 4 | 256 | 2x TA3 | 8 | - | 1 | LF, DCO, VLO | 24 | 32-QFN |
| MSP430G2313IPW28 | | | | | | | | | | 24 | 28-TSSOP |
| MSP430G2313IPW20 | | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2313IN20 | | | | | | | | | | 16 | 20-PDIP |
| MSP430G2213IRHB32 | 1 | 1 | 2 | 256 | 2x TA3 | 8 | - | 1 | LF, DCO, VLO | 24 | 32-QFN |
| MSP430G2213IPW28 | | | | | | | | | | 24 | 28-TSSOP |
| MSP430G2213IPW20 | | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2213IN20 | | | | | | | | | | 16 | 20-PDIP |
| MSP430G2113IRHB32 | 1 | 1 | 1 | 256 | 2x TA3 | 8 | - | 1 | LF, DCO, VLO | 24 | 32-QFN |
| MSP430G2113IPW28 | | | | | | | | | | 24 | 28-TSSOP |
| MSP430G2113IPW20 | | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2113IN20 | | | | | | | | | | 16 | 20-PDIP |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

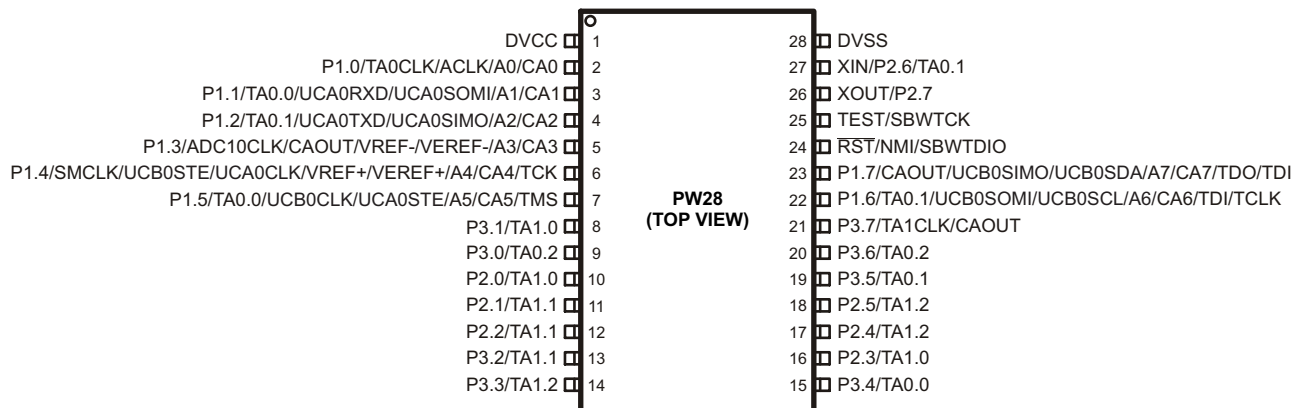
Device Pinout, MSP430G2x13 and MSP430G2x53, 20-Pin Devices, TSSOP and PDIP



NOTE: ADC10 is available on MSP430G2x53 devices only.

NOTE: The pulldown resistors of port P3 should be enabled by setting P3REN.x = 1.

Device Pinout, MSP430G2x13 and MSP430G2x53, 28-Pin Devices, TSSOP



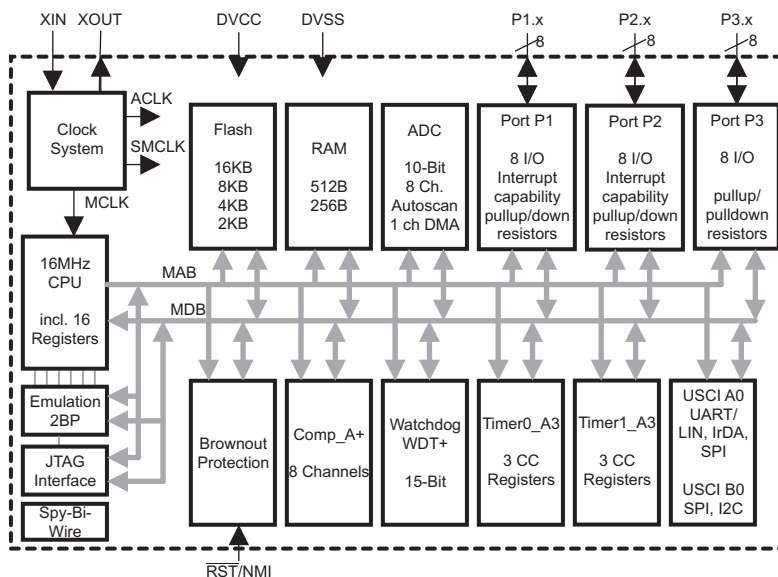
NOTE: ADC10 is available on MSP430G2x53 devices only.

Device Pinout, MSP430G2x13 and MSP430G2x53, 32-Pin Devices, QFN



NOTE: ADC10 is available on MSP430G2x53 devices only.

Functional Block Diagram, MSP430G2x53



NOTE: Port P3 is available on 28-pin and 32-pin devices only.

Functional Block Diagram, MSP430G2x13



NOTE: Port P3 is available on 28-pin and 32-pin devices only.

Table 2. Terminal Functions

| NAME | TERMINAL NO. | | | I/O | DESCRIPTION |
|--|--------------|------|-------|-----|---|
| | PW20, N20 | PW28 | RHB32 | | |
| P1.0/ TA0CLK/ ACLK/ A0 CA0 | 2 | 2 | 31 | I/O | General-purpose digital I/O pin Timer0_A, clock signal TACLK input ACLK signal output ADC10 analog input A0 ⁽¹⁾ Comparator_A+, CA0 input |
| P1.1/ TA0.0/ UCA0RXD/ UCA0SOMI/ A1/ CA1 | 3 | 3 | 1 | I/O | General-purpose digital I/O pin Timer0_A, capture: CCI0A input, compare: Out0 output / BSL transmit USCI_A0 UART mode: receive data input USCI_A0 SPI mode: slave data out/master in ADC10 analog input A1 ⁽¹⁾ Comparator_A+, CA1 input |
| P1.2/ TA0.1/ UCA0TXD/ UCA0SIMO/ A2/ CA2 | 4 | 4 | 2 | I/O | General-purpose digital I/O pin Timer0_A, capture: CCI1A input, compare: Out1 output USCI_A0 UART mode: transmit data output USCI_A0 SPI mode: slave data in/master out ADC10 analog input A2 ⁽¹⁾ Comparator_A+, CA2 input |
| P1.3/ ADC10CLK/ A3/ VREF-/VEREF-/ CA3/ CAOUT | 5 | 5 | 3 | I/O | General-purpose digital I/O pin ADC10, conversion clock output ⁽¹⁾ ADC10 analog input A3 ⁽¹⁾ ADC10 negative reference voltage ⁽¹⁾ Comparator_A+, CA3 input Comparator_A+, output |
| P1.4/ SMCLK/ UCB0STE/ UCA0CLK/ A4/ VREF+/VEREF+/ CA4/ TCK | 6 | 6 | 4 | I/O | General-purpose digital I/O pin SMCLK signal output USCI_B0 slave transmit enable USCI_A0 clock input/output ADC10 analog input A4 ⁽¹⁾ ADC10 positive reference voltage ⁽¹⁾ Comparator_A+, CA4 input JTAG test clock, input terminal for device programming and test |
| P1.5/ TA0.0/ UCB0CLK/ UCA0STE/ A5/ CA5/ TMS | 7 | 7 | 5 | I/O | General-purpose digital I/O pin Timer0_A, compare: Out0 output / BSL receive USCI_B0 clock input/output USCI_A0 slave transmit enable ADC10 analog input A5 ⁽¹⁾ Comparator_A+, CA5 input JTAG test mode select, input terminal for device programming and test |

(1) MSP430G2x53 devices only

Table 2. Terminal Functions (continued)

| TERMINAL | | | | I/O | DESCRIPTION |
|---|--------------|------|-------|-----|---|
| NAME | NO. | | | | |
| | PW20, N20 | PW28 | RHB32 | | |
| P1.6/ TA0.1/ A6/ CA6/ UCB0SOMI/ UCB0SCL/ TDI/TCLK | 14 | 22 | 21 | I/O | General-purpose digital I/O pin Timer0_A, compare: Out1 output ADC10 analog input A6 ⁽¹⁾ Comparator_A+, CA6 input USCI_B0 SPI mode: slave out master in USCI_B0 I2C mode: SCL I2C clock JTAG test data input or test clock input during programming and test |
| P1.7/ A7/ CA7/ CAOUT/ UCB0SIMO/ UCB0SDA/ TDO/TDI | 15 | 23 | 22 | I/O | General-purpose digital I/O pin ADC10 analog input A7 ⁽¹⁾ Comparator_A+, CA7 input Comparator_A+, output USCI_B0 SPI mode: slave in master out USCI_B0 I2C mode: SDA I2C data JTAG test data output terminal or test data input during programming and test ⁽²⁾ |
| P2.0/ TA1.0 | 8 | 10 | 9 | I/O | General-purpose digital I/O pin Timer1_A, capture: CCI0A input, compare: Out0 output |
| P2.1/ TA1.1 | 9 | 11 | 10 | I/O | General-purpose digital I/O pin Timer1_A, capture: CCI1A input, compare: Out1 output |
| P2.2/ TA1.1 | 10 | 12 | 11 | I/O | General-purpose digital I/O pin Timer1_A, capture: CCI1B input, compare: Out1 output |
| P2.3/ TA1.0 | 11 | 16 | 15 | I/O | General-purpose digital I/O pin Timer1_A, capture: CCI0B input, compare: Out0 output |
| P2.4/ TA1.2 | 12 | 17 | 16 | I/O | General-purpose digital I/O pin Timer1_A, capture: CCI2A input, compare: Out2 output |
| P2.5/ TA1.2 | 13 | 18 | 17 | I/O | General-purpose digital I/O pin Timer1_A, capture: CCI2B input, compare: Out2 output |
| XIN/ P2.6/ TA0.1 | 19 | 27 | 26 | I/O | Input terminal of crystal oscillator General-purpose digital I/O pin Timer0_A, compare: Out1 output |
| XOUT/ P2.7 | 18 | 26 | 25 | I/O | Output terminal of crystal oscillator ⁽³⁾ General-purpose digital I/O pin |
| P3.0/ TA0.2 | - | 9 | 7 | I/O | General-purpose digital I/O pin Timer0_A, capture: CCI2A input, compare: Out2 output |
| P3.1/ TA1.0 | - | 8 | 6 | I/O | General-purpose digital I/O pin Timer1_A, compare: Out0 output |
| P3.2/ TA1.1 | - | 13 | 12 | I/O | General-purpose digital I/O pin Timer1_A, compare: Out1 output |
| P3.3/ TA1.2 | - | 14 | 13 | I/O | General-purpose digital I/O Timer1_A, compare: Out2 output |
| P3.4/ TA0.0 | - | 15 | 14 | I/O | General-purpose digital I/O Timer0_A, compare: Out0 output |

(2) TDO or TDI is selected via JTAG instruction.

(3) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

Table 2. Terminal Functions (continued)

| TERMINAL | | | | I/O | DESCRIPTION |
|---------------------------|--------------|------|--------|-----|---|
| NAME | NO. | | | | |
| | PW20, N20 | PW28 | RHB32 | | |
| P3.5/ TA0.1 | - | 19 | 18 | I/O | General-purpose digital I/O Timer0_A, compare: Out1 output |
| P3.6/ TA0.2 | - | 20 | 19 | I/O | General-purpose digital I/O Timer0_A, compare: Out2 output |
| P3.7/ TA1CLK/ CAOUT | - | 21 | 20 | I/O | General-purpose digital I/O Timer1_A, clock signal TACLK input Comparator_A+, output |
| RST/ NMI/ SBWTDIO | 16 | 24 | 23 | I | Reset Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test |
| TEST/ SBWTCK | 17 | 25 | 24 | I | Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test |
| AVCC | NA | NA | 29 | NA | Analog supply voltage |
| DVCC | 1 | 1 | 30 | NA | Digital supply voltage |
| DVSS | 20 | 28 | 27, 28 | NA | Ground reference |
| NC | NA | NA | 8, 32 | NA | Not connected |
| QFN Pad | NA | NA | Pad | NA | QFN package pad. Connection to VSS is recommended. |

SHORT-FORM DESCRIPTION

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. [Table 3](#) shows examples of the three types of instruction formats; [Table 4](#) shows the address modes.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

Table 3. Instruction Word Formats

| INSTRUCTION FORMAT | EXAMPLE | OPERATION |
|-----------------------------------|-----------|-----------------------|
| Dual operands, source-destination | ADD R4,R5 | R4 + R5 --> R5 |
| Single operands, destination only | CALL R8 | PC -->(TOS), R8--> PC |
| Relative jump, un/conditional | JNE | Jump-on-equal bit = 0 |

Table 4. Address Mode Descriptions⁽¹⁾

| ADDRESS MODE | S | D | SYNTAX | EXAMPLE | OPERATION |
|------------------------|---|---|-----------------|------------------|--|
| Register | ✓ | ✓ | MOV Rs,Rd | MOV R10,R11 | R10 -- --> R11 |
| Indexed | ✓ | ✓ | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5) -- --> M(6+R6) |
| Symbolic (PC relative) | ✓ | ✓ | MOV EDE,TONI | | M(EDE) -- --> M(TONI) |
| Absolute | ✓ | ✓ | MOV &MEM,&TCDAT | | M(MEM) -- --> M(TCDAT) |
| Indirect | ✓ | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) -- --> M(Tab+R6) |
| Indirect autoincrement | ✓ | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) -- --> R11 R10 + 2-- --> R10 |
| Immediate | ✓ | | MOV #X,TONI | MOV #45,TONI | #45 -- --> M(TONI) |

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
 - DCO's dc generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc generator remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc generator is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc generator is disabled
 - Crystal oscillator is stopped

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed), the CPU goes into LPM4 immediately after power-up.

Table 5. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|---|--|---------------------|-----------------|
| Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range ⁽¹⁾ | PORIFG RSTIFG WDTIFG KEYV ⁽²⁾ | Reset | 0FFFEh | 31, highest |
| NMI Oscillator fault Flash memory access violation | NMIIFG OFIFG ACCVIFG ⁽²⁾⁽³⁾ | (non)-maskable (non)-maskable (non)-maskable | 0FFFCCh | 30 |
| Timer1_A3 | TA1CCR0 CCIFG ⁽⁴⁾ | maskable | 0FFFAh | 29 |
| Timer1_A3 | TA1CCR2 TA1CCR1 CCIFG, TAIFG ⁽²⁾⁽⁴⁾ | maskable | 0FFF8h | 28 |
| Comparator_A+ | CAIFG ⁽⁴⁾ | maskable | 0FFF6h | 27 |
| Watchdog Timer+ | WDTIFG | maskable | 0FFF4h | 26 |
| Timer0_A3 | TA0CCR0 CCIFG ⁽⁴⁾ | maskable | 0FFF2h | 25 |
| Timer0_A3 | TA0CCR2 TA0CCR1 CCIFG, TAIFG ⁽⁵⁾⁽⁴⁾ | maskable | 0FFF0h | 24 |
| USCI_A0/USCI_B0 receive USCI_B0 I2C status | UCA0RXIFG, UCB0RXIFG ⁽²⁾⁽⁵⁾ | maskable | 0FFEEh | 23 |
| USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit | UCA0TXIFG, UCB0TXIFG ⁽²⁾⁽⁶⁾ | maskable | 0FFECCh | 22 |
| ADC10 (MSP430G2x53 only) | ADC10IFG ⁽⁴⁾ | maskable | 0FFEAh | 21 |
| | | | 0FFE8h | 20 |
| I/O Port P2 (up to eight flags) | P2IFG.0 to P2IFG.7 ⁽²⁾⁽⁴⁾ | maskable | 0FFE6h | 19 |
| I/O Port P1 (up to eight flags) | P1IFG.0 to P1IFG.7 ⁽²⁾⁽⁴⁾ | maskable | 0FFE4h | 18 |
| | | | 0FFE2h | 17 |
| | | | 0FFE0h | 16 |
| See ⁽⁷⁾ | | | 0FFDEh | 15 |
| See ⁽⁸⁾ | | | 0FFDEh to 0FFC0h | 14 to 0, lowest |

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.

(2) Multiple source flags

(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.

(4) Interrupt flags are located in the module.

(5) In SPI mode: UCB0RXIFG. In I2C mode: UCA1IFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.

(6) In UART or SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.

(7) This location is used as bootstrap loader security key (BSLSKEY). A 0xAA55 at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.

(8) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Special Function Registers (SFRs)

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.










| | | |
|---------------|---|---|
| Legend | rw: | Bit can be read and written. |
| | rw-0,1: | Bit can be read and written. It is reset or set by PUC. |
| | rw-(0,1): | Bit can be read and written. It is reset or set by POR. |
| |  | SFR bit is not present in device. |

Table 6. Interrupt Enable Register 1 and 2




| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|--------|-------|--|---|------|-------|
| 00h |  |  | ACCVIE | NMIIE |  |  | OFIE | WDTIE |
| | | | rw-0 | rw-0 | | | rw-0 | rw-0 |

| | |
|---------------|--|
| WDTIE | Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode. |
| OFIE | Oscillator fault interrupt enable |
| NMIIE | (Non)maskable interrupt enable |
| ACCVIE | Flash access violation interrupt enable |





| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|----------|----------|----------|----------|
| 01h |  |  |  |  | UCB0TXIE | UCB0RXIE | UCA0TXIE | UCA0RXIE |
| | | | | | rw-0 | rw-0 | rw-0 | rw-0 |

| | |
|-----------------|-----------------------------------|
| UCA0RXIE | USCI_A0 receive interrupt enable |
| UCA0TXIE | USCI_A0 transmit interrupt enable |
| UCB0RXIE | USCI_B0 receive interrupt enable |
| UCB0TXIE | USCI_B0 transmit interrupt enable |

Table 7. Interrupt Flag Register 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|--------|--------|--------|-------|--------|
| 02h |  |  |  | NMIIFG | RSTIFG | PORIFG | OFIFG | WDTIFG |
| | | | | rw-0 | rw-(0) | rw-(1) | rw-1 | rw-(0) |

| | |
|---------------|---|
| WDTIFG | Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V _{CC} power-on or a reset condition at the $\overline{\text{RST}}$ /NMI pin in reset mode. |
| OFIFG | Flag set on oscillator fault. |
| PORIFG | Power-On Reset interrupt flag. Set on V _{CC} power-up. |
| RSTIFG | External reset interrupt flag. Set on a reset condition at $\overline{\text{RST}}$ /NMI pin in reset mode. Reset on V _{CC} power-up. |
| NMIIFG | Set via $\overline{\text{RST}}$ /NMI pin |

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|-----------|-----------|-----------|-----------|
| 03h |  |  |  |  | UCB0TXIFG | UCB0RXIFG | UCA0TXIFG | UCA0RXIFG |
| | | | | | rw-1 | rw-0 | rw-1 | rw-0 |

| | |
|------------------|---------------------------------|
| UCA0RXIFG | USCI_A0 receive interrupt flag |
| UCA0TXIFG | USCI_A0 transmit interrupt flag |
| UCB0RXIFG | USCI_B0 receive interrupt flag |
| UCB0TXIFG | USCI_B0 transmit interrupt flag |

Memory Organization

Table 8. Memory Organization

| | | MSP430G2153 MSP430G2113 | MSP430G2253 MSP430G2213 | MSP430G2353 MSP430G2313 | MSP430G2453 MSP430G2413 | MSP430G2553 MSP430G2513 |
|------------------------|-----------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|
| Memory | Size | 1kB | 2kB | 4kB | 8kB | 16kB |
| Main: interrupt vector | Flash | 0xFFFF to 0xFFC0 | 0xFFFF to 0xFFC0 | 0xFFFF to 0xFFC0 | 0xFFFF to 0xFFC0 | 0xFFFF to 0xFFC0 |
| Main: code memory | Flash | 0xFFFF to 0xFC00 | 0xFFFF to 0xF800 | 0xFFFF to 0xF000 | 0xFFFF to 0xE000 | 0xFFFF to 0xC000 |
| Information memory | Size | 256 Byte | 256 Byte | 256 Byte | 256 Byte | 256 Byte |
| | Flash | 010FFh to 01000h | 010FFh to 01000h | 010FFh to 01000h | 010FFh to 01000h | 010FFh to 01000h |
| RAM | Size | 256 Byte | 256 Byte | 256 Byte | 512 Byte | 512 Byte |
| | | 0x02FF to 0x0200 | 0x02FF to 0x0200 | 0x02FF to 0x0200 | 0x03FF to 0x0200 | 0x03FF to 0x0200 |
| Peripherals | 16-bit | 01FFh to 0100h | 01FFh to 0100h | 01FFh to 0100h | 01FFh to 0100h | 01FFh to 0100h |
| | 8-bit | 0FFh to 010h | 0FFh to 010h | 0FFh to 010h | 0FFh to 010h | 0FFh to 010h |
| | 8-bit SFR | 0Fh to 00h | 0Fh to 00h | 0Fh to 00h | 0Fh to 00h | 0Fh to 00h |

Bootstrap Loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

Table 9. BSL Function Pins

| BSL FUNCTION | 20-PIN PW PACKAGE 20-PIN N PACKAGE | 28-PIN PACKAGE PW | 32-PIN PACKAGE RHB |
|---------------------|---|--------------------------|---------------------------|
| Data transmit | 3 - P1.1 | 3 - P1.1 | 1 - P1.1 |
| Data receive | 7 - P1.5 | 7 - P1.5 | 5 - P1.5 |

Flash Memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO} .
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

Calibration Data Stored in Information Memory Segment A

Calibration data is stored for both the DCO and for ADC10 organized in a tag-length-value structure.

Table 10. Tags Used by the ADC Calibration Tags

| NAME | ADDRESS | VALUE | DESCRIPTION |
|-------------|---------|-------|--|
| TAG_DCO_30 | 0x10F6 | 0x01 | DCO frequency calibration at $V_{CC} = 3\text{ V}$ and $T_A = 30^\circ\text{C}$ at calibration |
| TAG_ADC10_1 | 0x10DA | 0x10 | ADC10_1 calibration tag |
| TAG_EMPTY | - | 0xFE | Identifier for empty memory areas |

Table 11. Labels Used by the ADC Calibration Tags

| LABEL | ADDRESS OFFSET | SIZE | CONDITION AT CALIBRATION / DESCRIPTION |
|-----------------------|----------------|------|--|
| CAL_ADC_25T85 | 0x0010 | word | INCHx = 0x1010, REF2_5 = 1, $T_A = 85^\circ\text{C}$ |
| CAL_ADC_25T30 | 0x000E | word | INCHx = 0x1010, REF2_5 = 1, $T_A = 30^\circ\text{C}$ |
| CAL_ADC_25VREF_FACTOR | 0x000C | word | REF2_5 = 1, $T_A = 30^\circ\text{C}$, $I_{VREF+} = 1\text{ mA}$ |
| CAL_ADC_15T85 | 0x000A | word | INCHx = 0x1010, REF2_5 = 0, $T_A = 85^\circ\text{C}$ |
| CAL_ADC_15T30 | 0x0008 | word | INCHx = 0x1010, REF2_5 = 0, $T_A = 30^\circ\text{C}$ |
| CAL_ADC_15VREF_FACTOR | 0x0006 | word | REF2_5 = 0, $T_A = 30^\circ\text{C}$, $I_{VREF+} = 0.5\text{ mA}$ |
| CAL_ADC_OFFSET | 0x0004 | word | External VREF = 1.5 V, $f_{ADC10CLK} = 5\text{ MHz}$ |
| CAL_ADC_GAIN_FACTOR | 0x0002 | word | External VREF = 1.5 V, $f_{ADC10CLK} = 5\text{ MHz}$ |
| CAL_BC1_1MHZ | 0x0009 | byte | - |
| CAL_DCO_1MHZ | 0x0008 | byte | - |
| CAL_BC1_8MHZ | 0x0007 | byte | - |
| CAL_DCO_8MHZ | 0x0006 | byte | - |
| CAL_BC1_12MHZ | 0x0005 | byte | - |
| CAL_DCO_12MHZ | 0x0004 | byte | - |
| CAL_BC1_16MHZ | 0x0003 | byte | - |
| CAL_DCO_16MHZ | 0x0002 | byte | - |

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

Up to three 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition (port P1 and port P2 only) is possible.
- Edge-selectable interrupt input capability for all bits of port P1 and port P2 (if available).
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup or pulldown resistor.
- Each I/O has an individually programmable pin oscillator enable bit to enable low-cost touch sensing.

WDT+ Watchdog Timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A3 (TA0, TA1)

Timer0/1_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 12. Timer0_A3 Signal Connections

| INPUT PIN NUMBER | | | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | |
|------------------|--------|---------|---------------------------|-------------------------|-----------------|----------------------------|-------------------|---------|---------|
| PW20, N20 | PW28 | RHB32 | | | | | PW20, N20 | PW28 | RHB32 |
| P1.0-2 | P1.0-2 | P1.0-31 | TACLK | TACLK | Timer | NA | | | |
| | | | ACLK | ACLK | | | | | |
| | | | SMCLK | SMCLK | | | | | |
| PinOsc | PinOsc | PinOsc | TACLK | INCLK | | | | | |
| P1.1-3 | P1.1-3 | P1.1-1 | TA0.0 | CCI0A | CCR0 | TA0 | P1.1-3 | P1.1-3 | P1.1-1 |
| | | | ACLK | CCI0B | | | P1.5-7 | P1.5-7 | P1.5-5 |
| | | | V _{SS} | GND | | | | P3.4-15 | P3.4-14 |
| | | | V _{CC} | V _{CC} | | | | | |
| P1.2-4 | P1.2-4 | P1.2-2 | TA0.1 | CCI1A | CCR1 | TA1 | P1.2-4 | P1.2-4 | P1.2-2 |
| | | | CAOUT | CCI1B | | | P1.6-14 | P1.6-22 | P1.6-21 |
| | | | V _{SS} | GND | | | P2.6-19 | P2.6-27 | P2.6-26 |
| | | | V _{CC} | V _{CC} | | | | P3.5-19 | P3.5-18 |
| | P3.0-9 | P3.0-7 | TA0.2 | CCI2A | CCR2 | TA2 | | P3.0-9 | P3.0-7 |
| PinOsc | PinOsc | PinOsc | TA0.2 | CCI2B | | | | P3.6-20 | P3.6-19 |
| | | | V _{SS} | GND | | | | | |
| | | | V _{CC} | V _{CC} | | | | | |

Table 13. Timer1_A3 Signal Connections

| INPUT PIN NUMBER | | | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | |
|------------------|---------|---------|---------------------------|-------------------------|-----------------|----------------------------|-------------------|---------|---------|
| PW20, N20 | PW28 | RHB32 | | | | | PW20, N20 | PW28 | RHB32 |
| - | P3.7-21 | P3.7-20 | TACLK | TACLK | Timer | NA | | | |
| | | | ACLK | ACLK | | | | | |
| | | | SMCLK | SMCLK | | | | | |
| - | P3.7-21 | P3.7-20 | TACLK | INCLK | | | | | |
| P2.0-8 | P2.0-10 | P2.0-9 | TA1.0 | CCI0A | CCR0 | TA0 | P2.0-8 | P2.0-10 | P2.0-9 |
| P2.3-11 | P2.3-16 | P2.3-12 | TA1.0 | CCI0B | | | P2.3-11 | P2.3-16 | P2.3-15 |
| | | | V _{SS} | GND | | | | P3.1-8 | P3.1-6 |
| | | | V _{CC} | V _{CC} | | | | | |
| P2.1-9 | P2.1-11 | P2.1-10 | TA1.1 | CCI1A | CCR1 | TA1 | P2.1-9 | P2.1-11 | P2.1-10 |
| P2.2-10 | P2.2-12 | P2.2-11 | TA1.1 | CCI1B | | | P2.2-10 | P2.2-12 | P2.2-11 |
| | | | V _{SS} | GND | | | | P3.2-13 | P3.2-12 |
| | | | V _{CC} | V _{CC} | | | | | |
| P2.4-12 | P2.4-17 | P2.4-16 | TA1.2 | CCI2A | CCR2 | TA2 | P2.4-12 | P2.4-17 | P2.4-16 |
| P2.5-13 | P2.5-18 | P2.5-17 | TA1.2 | CCI2B | | | P2.5-13 | P2.5-18 | P2.5-17 |
| | | | V _{SS} | GND | | | | P3.3-14 | P3.3-13 |
| | | | V _{CC} | V _{CC} | | | | | |

Universal Serial Communications Interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA. Not all packages support the USCI functionality.

USCI_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

USCI_B0 provides support for SPI (3 or 4 pin) and I2C.

Comparator_A+

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC10 (MSP430G2x53 Only)

The ADC10 module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and data transfer controller (DTC) for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

Peripheral File Map

Table 14. Peripherals With Word Access

| MODULE | REGISTER DESCRIPTION | REGISTER NAME | OFFSET |
|-------------------------------------|---------------------------------|---------------|--------|
| ADC10 (MSP430G2x53 devices only) | ADC data transfer start address | ADC10SA | 1BCh |
| | ADC memory | ADC10MEM | 1B4h |
| | ADC control register 1 | ADC10CTL1 | 1B2h |
| | ADC control register 0 | ADC10CTL0 | 1B0h |
| Timer1_A3 | Capture/compare register | TA1CCR2 | 0196h |
| | Capture/compare register | TA1CCR1 | 0194h |
| | Capture/compare register | TA1CCR0 | 0192h |
| | Timer_A register | TA1R | 0190h |
| | Capture/compare control | TA1CCTL2 | 0186h |
| | Capture/compare control | TA1CCTL1 | 0184h |
| | Capture/compare control | TA1CCTL0 | 0182h |
| | Timer_A control | TA1CTL | 0180h |
| | Timer_A interrupt vector | TA1IV | 011Eh |
| | | | |
| Timer0_A3 | Capture/compare register | TA0CCR2 | 0176h |
| | Capture/compare register | TA0CCR1 | 0174h |
| | Capture/compare register | TA0CCR0 | 0172h |
| | Timer_A register | TA0R | 0170h |
| | Capture/compare control | TA0CCTL2 | 0166h |
| | Capture/compare control | TA0CCTL1 | 0164h |
| | Capture/compare control | TA0CCTL0 | 0162h |
| | Timer_A control | TA0CTL | 0160h |
| | Timer_A interrupt vector | TA0IV | 012Eh |
| | | | |
| Flash Memory | Flash control 3 | FCTL3 | 012Ch |
| | Flash control 2 | FCTL2 | 012Ah |
| | Flash control 1 | FCTL1 | 0128h |
| Watchdog Timer+ | Watchdog/timer control | WDTCCTL | 0120h |

Table 15. Peripherals With Byte Access

| MODULE | REGISTER DESCRIPTION | REGISTER NAME | OFFSET |
|--|--------------------------------------|---------------|--------|
| USCI_B0 | USCI_B0 transmit buffer | UCB0TXBUF | 06Fh |
| | USCI_B0 receive buffer | UCB0RXBUF | 06Eh |
| | USCI_B0 status | UCB0STAT | 06Dh |
| | USCI_B0 I2C Interrupt enable | UCB0CIE | 06Ch |
| | USCI_B0 bit rate control 1 | UCB0BR1 | 06Bh |
| | USCI_B0 bit rate control 0 | UCB0BR0 | 06Ah |
| | USCI_B0 control 1 | UCB0CTL1 | 069h |
| | USCI_B0 control 0 | UCB0CTL0 | 068h |
| | USCI_B0 I2C slave address | UCB0SA | 011Ah |
| | USCI_B0 I2C own address | UCB0OA | 0118h |
| USCI_A0 | USCI_A0 transmit buffer | UCA0TXBUF | 067h |
| | USCI_A0 receive buffer | UCA0RXBUF | 066h |
| | USCI_A0 status | UCA0STAT | 065h |
| | USCI_A0 modulation control | UCA0MCTL | 064h |
| | USCI_A0 baud rate control 1 | UCA0BR1 | 063h |
| | USCI_A0 baud rate control 0 | UCA0BR0 | 062h |
| | USCI_A0 control 1 | UCA0CTL1 | 061h |
| | USCI_A0 control 0 | UCA0CTL0 | 060h |
| | USCI_A0 IrDA receive control | UCA0IRRCTL | 05Fh |
| | USCI_A0 IrDA transmit control | UCA0IRTCTL | 05Eh |
| | USCI_A0 auto baud rate control | UCA0ABCTL | 05Dh |
| ADC10 (MSP430G2x53 devices only) | ADC analog enable 0 | ADC10AE0 | 04Ah |
| | ADC analog enable 1 | ADC10AE1 | 04Bh |
| | ADC data transfer control register 1 | ADC10DTC1 | 049h |
| | ADC data transfer control register 0 | ADC10DTC0 | 048h |
| Comparator_A+ | Comparator_A+ port disable | CAPD | 05Bh |
| | Comparator_A+ control 2 | CACTL2 | 05Ah |
| | Comparator_A+ control 1 | CACTL1 | 059h |
| Basic Clock System+ | Basic clock system control 3 | BCSCTL3 | 053h |
| | Basic clock system control 2 | BCSCTL2 | 058h |
| | Basic clock system control 1 | BCSCTL1 | 057h |
| | DCO clock frequency control | DCOCTL | 056h |
| Port P3 (28-pin PW and 32-pin RHB only) | Port P3 selection 2. pin | P3SEL2 | 043h |
| | Port P3 resistor enable | P3REN | 010h |
| | Port P3 selection | P3SEL | 01Bh |
| | Port P3 direction | P3DIR | 01Ah |
| | Port P3 output | P3OUT | 019h |
| | Port P3 input | P3IN | 018h |
| | | | |
| Port P2 | Port P2 selection 2 | P2SEL2 | 042h |
| | Port P2 resistor enable | P2REN | 02Fh |
| | Port P2 selection | P2SEL | 02Eh |
| | Port P2 interrupt enable | P2IE | 02Dh |
| | Port P2 interrupt edge select | P2IES | 02Ch |
| | Port P2 interrupt flag | P2IFG | 02Bh |
| | Port P2 direction | P2DIR | 02Ah |
| | Port P2 output | P2OUT | 029h |
| | Port P2 input | P2IN | 028h |

Table 15. Peripherals With Byte Access (continued)

| MODULE | REGISTER DESCRIPTION | REGISTER NAME | OFFSET |
|------------------|-------------------------------|---------------|--------|
| Port P1 | Port P1 selection 2 | P1SEL2 | 041h |
| | Port P1 resistor enable | P1REN | 027h |
| | Port P1 selection | P1SEL | 026h |
| | Port P1 interrupt enable | P1IE | 025h |
| | Port P1 interrupt edge select | P1IES | 024h |
| | Port P1 interrupt flag | P1IFG | 023h |
| | Port P1 direction | P1DIR | 022h |
| | Port P1 output | P1OUT | 021h |
| | Port P1 input | P1IN | 020h |
| Special Function | SFR interrupt flag 2 | IFG2 | 003h |
| | SFR interrupt flag 1 | IFG1 | 002h |
| | SFR interrupt enable 2 | IE2 | 001h |
| | SFR interrupt enable 1 | IE1 | 000h |

Absolute Maximum Ratings⁽¹⁾

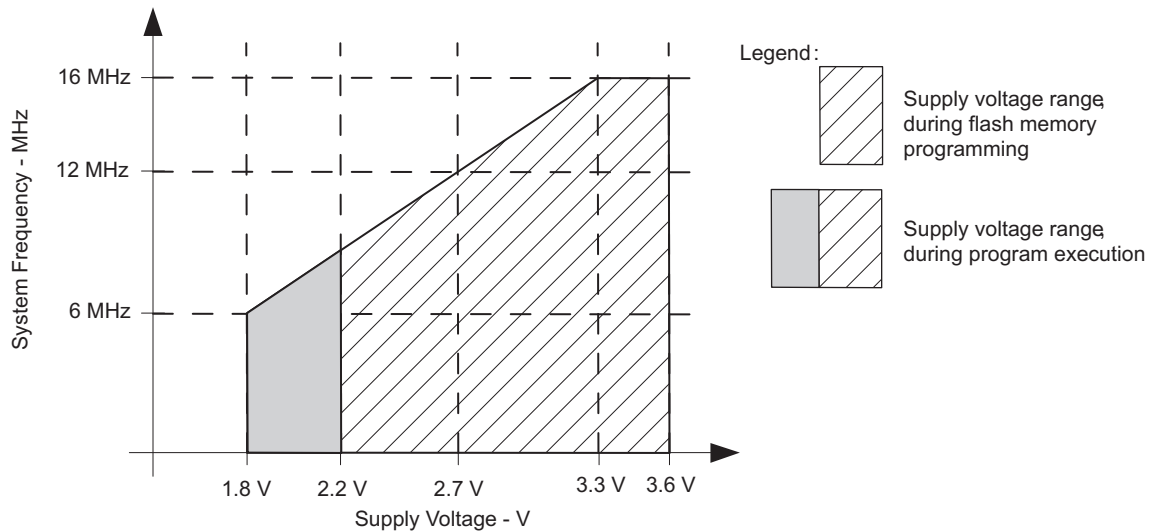
| | | |
|---|---------------------|----------------------------|
| Voltage applied at V_{CC} to V_{SS} | | –0.3 V to 4.1 V |
| Voltage applied to any pin ⁽²⁾ | | –0.3 V to $V_{CC} + 0.3$ V |
| Diode current at any device pin | | ±2 mA |
| Storage temperature range, T_{stg} ⁽³⁾ | Unprogrammed device | –55°C to 150°C |
| | Programmed device | –55°C to 150°C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS} . The JTAG fuse-blow voltage, V_{FB} , is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|--------------|--|---|-----|-----|------|
| V_{CC} | Supply voltage | | | | V |
| | During program execution | 1.8 | | 3.6 | |
| | During flash programming or erase | 2.2 | | 3.6 | |
| V_{SS} | Supply voltage | 0 | | | V |
| T_A | Operating free-air temperature | I version | | | °C |
| | | –40 | | 85 | |
| f_{SYSTEM} | Processor frequency (maximum MCLK frequency) ⁽¹⁾⁽²⁾ | $V_{CC} = 1.8$ V, Duty cycle = 50% ± 10% | dc | 6 | MHz |
| | | $V_{CC} = 2.7$ V, Duty cycle = 50% ± 10% | dc | 12 | |
| | | $V_{CC} = 3.3$ V, Duty cycle = 50% ± 10% | dc | 16 | |

- (1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
- (2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Safe Operating Area

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾⁽²⁾

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|---|--|-------|----------|-----|-----|-----|---------|
| $I_{AM,1MHz}$ Active mode (AM) current at 1 MHz | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 1\text{ MHz}$, $f_{ACLK} = 0\text{ Hz}$, Program executes in flash, $BCSCTL1 = CALBC1_1MHz$, $DCOCTL = CALDCO_1MHz$, $CPUOFF = 0$, $SCG0 = 0$, $SCG1 = 0$, $OSCOFF = 0$ | | 2.2 V | | 230 | | μA |
| | | | 3 V | | 330 | 420 | |

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

Typical Characteristics, Active Mode Supply Current (Into V_{CC})

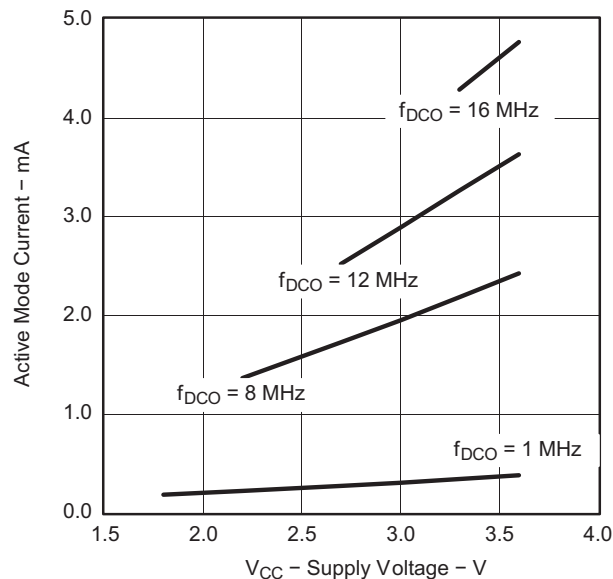


Figure 2. Active Mode Current vs V_{CC} , $T_A = 25^\circ C$

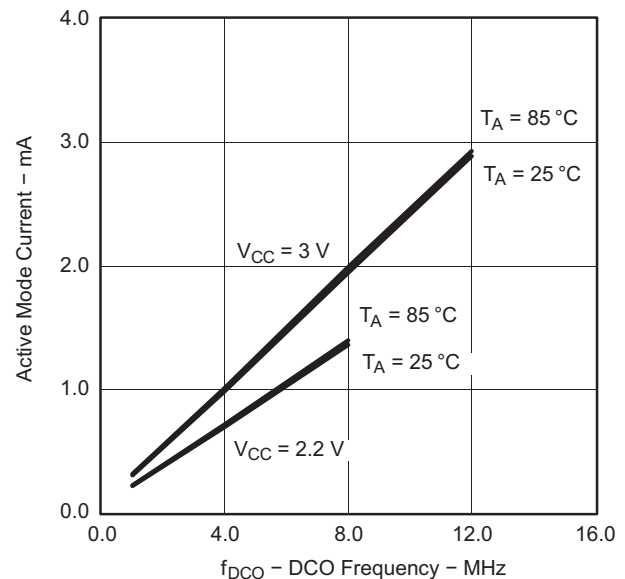


Figure 3. Active Mode Current vs DCO Frequency

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|---|---|-------|----------|-----|-----|-----|---------|
| $I_{LPM0,1MHz}$ Low-power mode 0 (LPM0) current ⁽³⁾ | $f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO} = 1$ MHz, $f_{ACLK} = 32768$ Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | 25°C | 2.2 V | | 56 | | μA |
| I_{LPM2} Low-power mode 2 (LPM2) current ⁽⁴⁾ | $f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{DCO} = 1$ MHz, $f_{ACLK} = 32768$ Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | | 22 | | μA |
| $I_{LPM3,LFXT1}$ Low-power mode 3 (LPM3) current ⁽⁴⁾ | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 32768$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | | 0.7 | 1.5 | μA |
| $I_{LPM3,VLO}$ Low-power mode 3 current, (LPM3) ⁽⁴⁾ | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | | 0.5 | 0.7 | μA |
| I_{LPM4} Low-power mode 4 (LPM4) current ⁽⁵⁾ | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 0$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 | 25°C | 2.2 V | | 0.1 | 0.5 | μA |
| | | 85°C | | | 0.8 | 1.7 | |

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
- (3) Current for brownout and WDT clocked by SMCLK included.
- (4) Current for brownout and WDT clocked by ACLK included.
- (5) Current for brownout included.

Typical Characteristics, Low-Power Mode Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

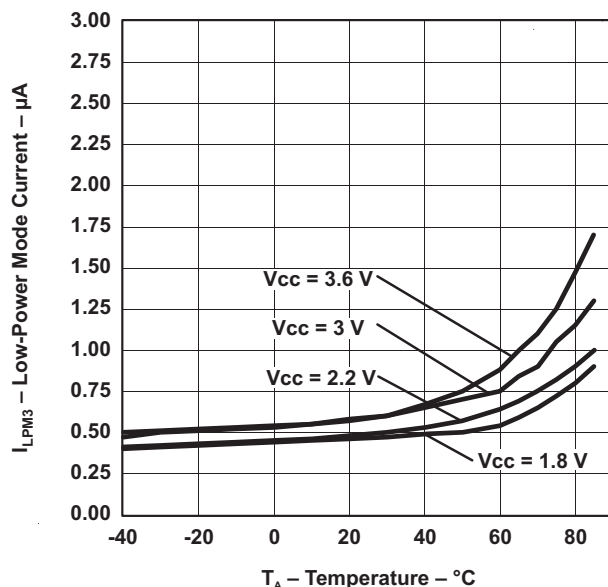


Figure 4. LPM3 Current vs Temperature

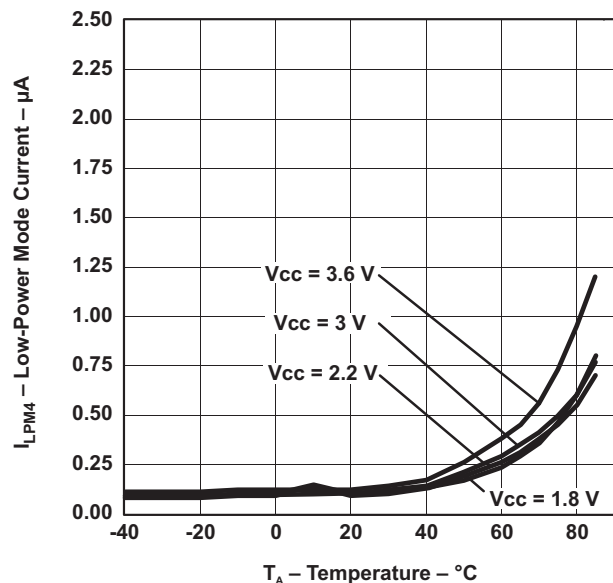


Figure 5. LPM4 Current vs Temperature

Schmitt-Trigger Inputs, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|-----------------|----------------------|-----|----------------------|------|
| V _{IT+} Positive-going input threshold voltage | | | 0.45 V _{CC} | | 0.75 V _{CC} | V |
| | | 3 V | 1.35 | | 2.25 | |
| V _{IT–} Negative-going input threshold voltage | | | 0.25 V _{CC} | | 0.55 V _{CC} | V |
| | | 3 V | 0.75 | | 1.65 | |
| V _{hys} Input voltage hysteresis (V _{IT+} – V _{IT–}) | | 3 V | 0.3 | | 1 | V |
| R _{Pull} Pullup/pulldown resistor | For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC} | 3 V | 20 | 35 | 50 | kΩ |
| C _I Input capacitance | V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |

Leakage Current, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|--|-----------------|-----------------|-----|-----|------|
| I _{lkg} (Px.y) High-impedance leakage current | (1) (2) | 3 V | | ±50 | nA |

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Outputs, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|-----------------|-----|-----------------------|-----|------|
| V _{OH} High-level output voltage | I _(OHmax) = –6 mA ⁽¹⁾ | 3 V | | V _{CC} – 0.3 | | V |
| V _{OL} Low-level output voltage | I _(OLmax) = 6 mA ⁽¹⁾ | 3 V | | V _{SS} + 0.3 | | V |

(1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|--|-----------------|-----|-----|-----|------|
| f _{Px.y} Port output frequency (with load) | Px.y, C _L = 20 pF, R _L = 1 kΩ ⁽¹⁾ (2) | 3 V | | 12 | | MHz |
| f _{Port_CLK} Clock output frequency | Px.y, C _L = 20 pF ⁽²⁾ | 3 V | | 16 | | MHz |

(1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.

(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics, Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

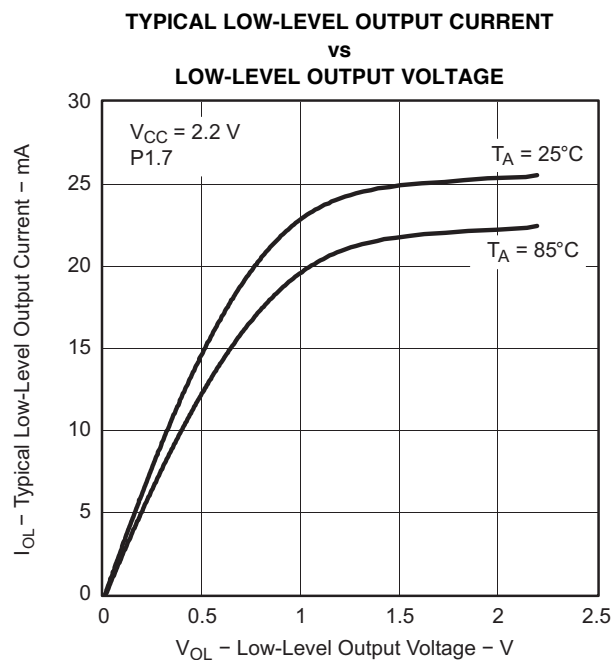


Figure 6.

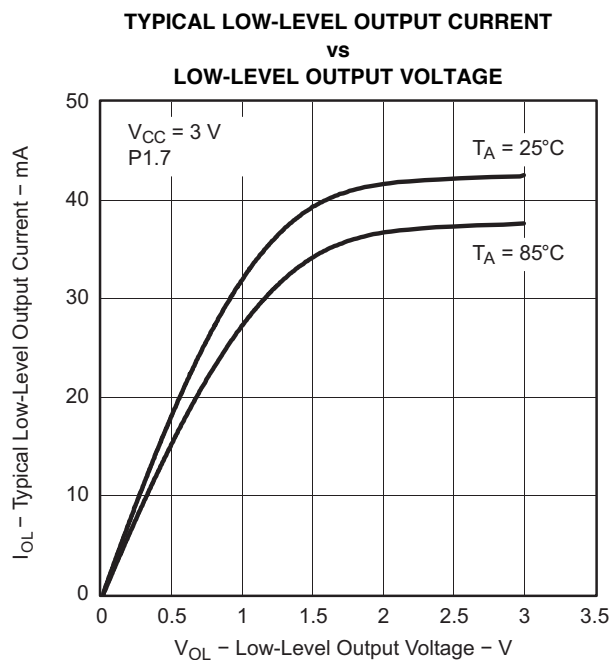


Figure 7.

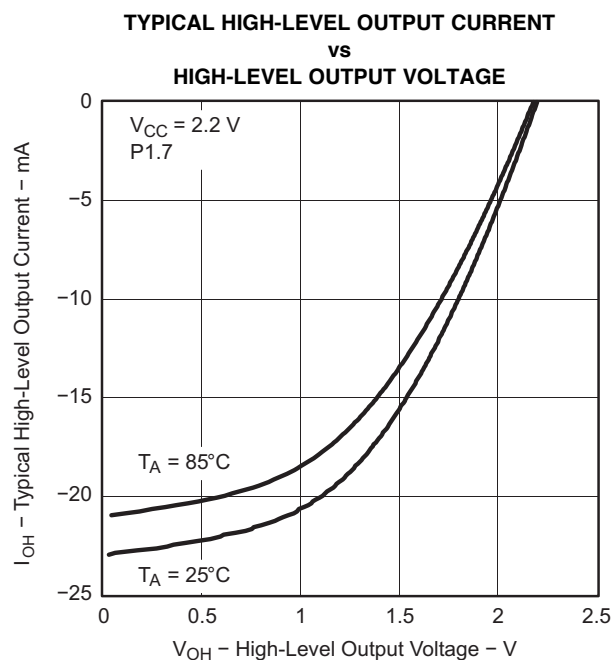


Figure 8.

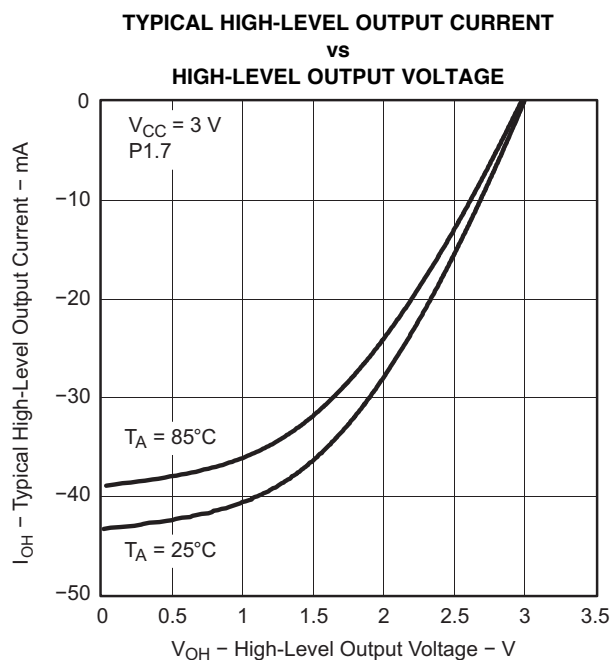


Figure 9.

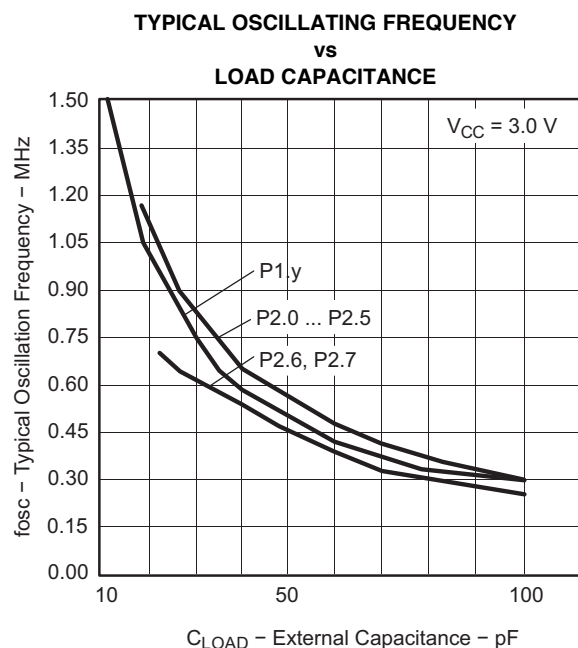
Pin-Oscillator Frequency – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|-----------------|-----|------|-----|------|
| f _{OP1.x} Port output oscillation frequency | P1.y, C _L = 10 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾ | 3 V | | 1400 | | kHz |
| | P1.y, C _L = 20 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾ | | | 900 | | |
| f _{OP2.x} Port output oscillation frequency | P2.0 to P2.5, C _L = 10 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾ | 3 V | | 1800 | | kHz |
| | P2.0 to P2.5, C _L = 20 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾ | | | 1000 | | |
| f _{OP2.6/7} Port output oscillation frequency | P2.6 and P2.7, C _L = 20 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾ | 3 V | | 700 | | kHz |
| f _{OP3.x} Port output oscillation frequency | P3.y, C _L = 10 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾ | | | 1800 | | kHz |
| | P3.y, C _L = 20 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾ | | | 1000 | | |

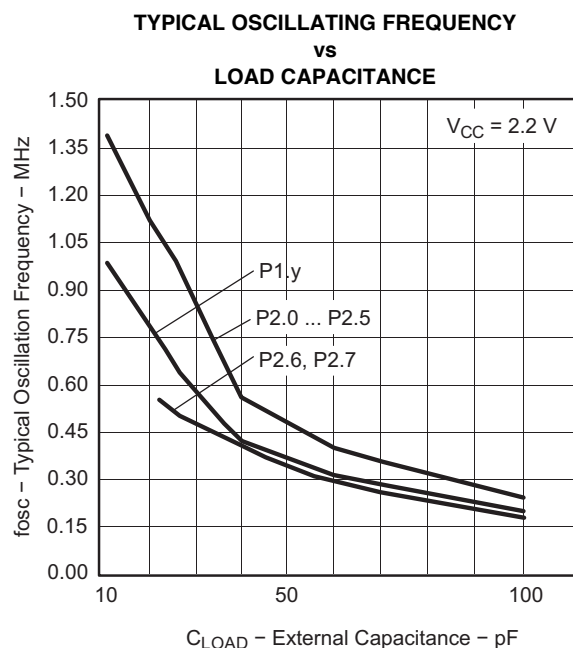
- (1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics, Pin-Oscillator Frequency



A. One output active at a time.

Figure 10.



A. One output active at a time.

Figure 11.

POR/Brownout Reset (BOR)⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|--|-----------------|-----|-------------------------------|-----|------|
| V _{CC(start)} | See Figure 12 | | | 0.7 × V _(B_IT-) | | V |
| V _(B_IT-) | See Figure 12 through Figure 14 | | | 1.35 | | V |
| V _{hys(B_IT-)} | See Figure 12 | | | 140 | | mV |
| t _{d(BOR)} | See Figure 12 | | | 2000 | | μs |
| t _(reset) | Pulse length needed at $\overline{\text{RST}}/\text{NMI}$ pin to accepted reset internally | 2.2 V | 2 | | | μs |

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level V_(B_IT-) + V_{hys(B_IT-)} is ≤ 1.8 V.

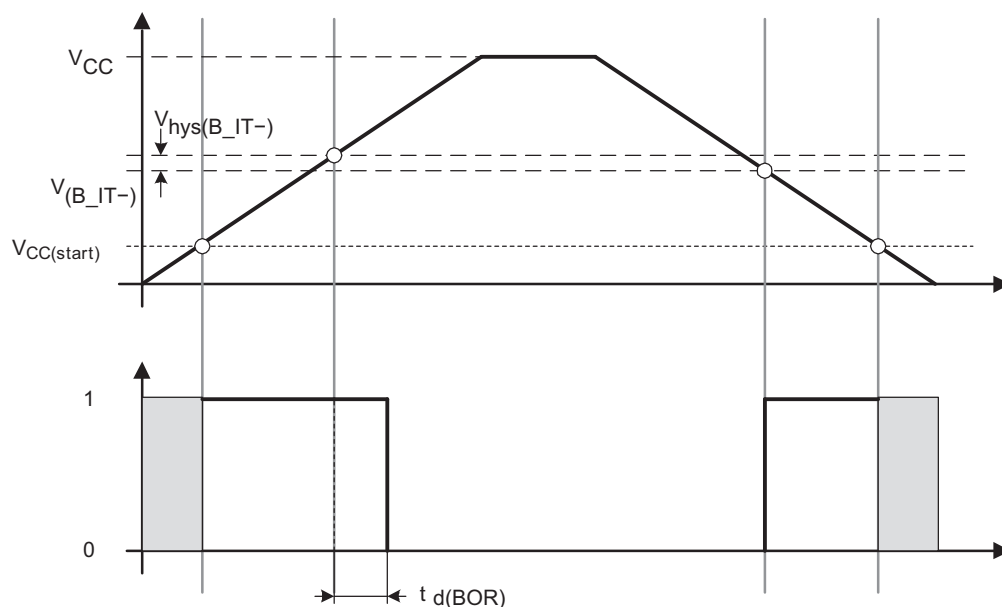


Figure 12. POR/Brownout Reset (BOR) vs Supply Voltage

Typical Characteristics, POR/Brownout Reset (BOR)

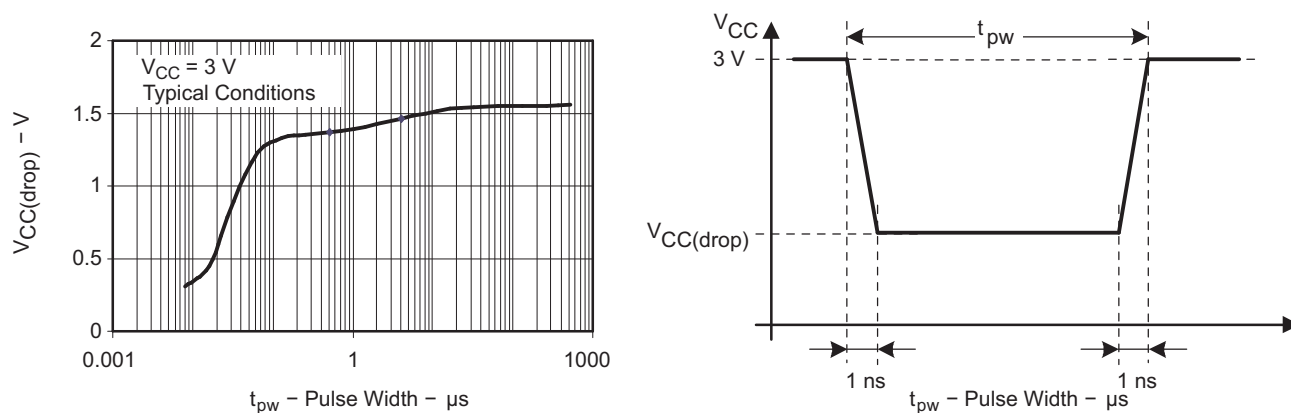


Figure 13. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

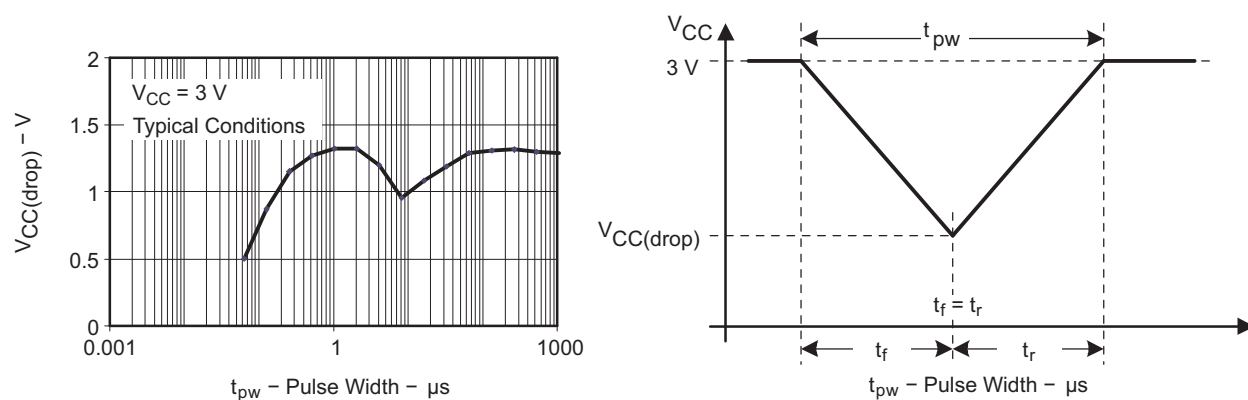


Figure 14. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|--|--|-----------------|------|------|------|-------|
| V _{CC} | Supply voltage | RSELx < 14 | | 1.8 | | 3.6 | V |
| | | RSELx = 14 | | 2.2 | | 3.6 | |
| | | RSELx = 15 | | 3 | | 3.6 | |
| f _{DCO(0,0)} | DCO frequency (0, 0) | RSELx = 0, DCOx = 0, MODx = 0 | 3 V | 0.06 | | 0.14 | MHz |
| f _{DCO(0,3)} | DCO frequency (0, 3) | RSELx = 0, DCOx = 3, MODx = 0 | 3 V | 0.07 | | 0.17 | MHz |
| f _{DCO(1,3)} | DCO frequency (1, 3) | RSELx = 1, DCOx = 3, MODx = 0 | 3 V | | 0.15 | | MHz |
| f _{DCO(2,3)} | DCO frequency (2, 3) | RSELx = 2, DCOx = 3, MODx = 0 | 3 V | | 0.21 | | MHz |
| f _{DCO(3,3)} | DCO frequency (3, 3) | RSELx = 3, DCOx = 3, MODx = 0 | 3 V | | 0.30 | | MHz |
| f _{DCO(4,3)} | DCO frequency (4, 3) | RSELx = 4, DCOx = 3, MODx = 0 | 3 V | | 0.41 | | MHz |
| f _{DCO(5,3)} | DCO frequency (5, 3) | RSELx = 5, DCOx = 3, MODx = 0 | 3 V | | 0.58 | | MHz |
| f _{DCO(6,3)} | DCO frequency (6, 3) | RSELx = 6, DCOx = 3, MODx = 0 | 3 V | 0.54 | | 1.06 | MHz |
| f _{DCO(7,3)} | DCO frequency (7, 3) | RSELx = 7, DCOx = 3, MODx = 0 | 3 V | 0.80 | | 1.50 | MHz |
| f _{DCO(8,3)} | DCO frequency (8, 3) | RSELx = 8, DCOx = 3, MODx = 0 | 3 V | | 1.6 | | MHz |
| f _{DCO(9,3)} | DCO frequency (9, 3) | RSELx = 9, DCOx = 3, MODx = 0 | 3 V | | 2.3 | | MHz |
| f _{DCO(10,3)} | DCO frequency (10, 3) | RSELx = 10, DCOx = 3, MODx = 0 | 3 V | | 3.4 | | MHz |
| f _{DCO(11,3)} | DCO frequency (11, 3) | RSELx = 11, DCOx = 3, MODx = 0 | 3 V | | 4.25 | | MHz |
| f _{DCO(12,3)} | DCO frequency (12, 3) | RSELx = 12, DCOx = 3, MODx = 0 | 3 V | 4.30 | | 7.30 | MHz |
| f _{DCO(13,3)} | DCO frequency (13, 3) | RSELx = 13, DCOx = 3, MODx = 0 | 3 V | 6.00 | 7.8 | 9.60 | MHz |
| f _{DCO(14,3)} | DCO frequency (14, 3) | RSELx = 14, DCOx = 3, MODx = 0 | 3 V | 8.60 | | 13.9 | MHz |
| f _{DCO(15,3)} | DCO frequency (15, 3) | RSELx = 15, DCOx = 3, MODx = 0 | 3 V | 12.0 | | 18.5 | MHz |
| f _{DCO(15,7)} | DCO frequency (15, 7) | RSELx = 15, DCOx = 7, MODx = 0 | 3 V | 16.0 | | 26.0 | MHz |
| S _{RSEL} | Frequency step between range RSEL and RSEL+1 | $S_{RSEL} = f_{DCO(RSEL+1,DCO)} / f_{DCO(RSEL,DCO)}$ | 3 V | | 1.35 | | ratio |
| S _{DCO} | Frequency step between tap DCO and DCO+1 | $S_{DCO} = f_{DCO(RSEL,DCO+1)} / f_{DCO(RSEL,DCO)}$ | 3 V | | 1.08 | | ratio |
| | Duty cycle | Measured at SMCLK output | 3 V | | 50 | | % |

Calibrated DCO Frequencies, Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|----------------|-----------------|-----|------|-----|------|
| 1-MHz tolerance over temperature ⁽¹⁾ | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V | 0°C to 85°C | 3 V | -3 | ±0.5 | +3 | % |
| 1-MHz tolerance over V _{CC} | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V | 30°C | 1.8 V to 3.6 V | -3 | ±2 | +3 | % |
| 1-MHz tolerance overall | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V | -40°C to 85°C | 1.8 V to 3.6 V | -6 | ±3 | +6 | % |
| 8-MHz tolerance over temperature ⁽¹⁾ | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V | 0°C to 85°C | 3 V | -3 | ±0.5 | +3 | % |
| 8-MHz tolerance over V _{CC} | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V | 30°C | 2.2 V to 3.6 V | -3 | ±2 | +3 | % |
| 8-MHz tolerance overall | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V | -40°C to 85°C | 2.2 V to 3.6 V | -6 | ±3 | +6 | % |
| 12-MHz tolerance over temperature ⁽¹⁾ | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V | 0°C to 85°C | 3 V | -3 | ±0.5 | +3 | % |
| 12-MHz tolerance over V _{CC} | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V | 30°C | 2.7 V to 3.6 V | -3 | ±2 | +3 | % |
| 12-MHz tolerance overall | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V | -40°C to 85°C | 2.7 V to 3.6 V | -6 | ±3 | +6 | % |
| 16-MHz tolerance over temperature ⁽¹⁾ | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V | 0°C to 85°C | 3 V | -3 | ±0.5 | +3 | % |
| 16-MHz tolerance over V _{CC} | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V | 30°C | 3.3 V to 3.6 V | -3 | ±2 | +3 | % |
| 16-MHz tolerance overall | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V | -40°C to 85°C | 3.3 V to 3.6 V | -6 | ±3 | +6 | % |

(1) This is the frequency change from the measured frequency at 30°C over temperature.

Wake-Up From Lower-Power Modes (LPM3/4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|---|-----------------|-----|--|-----|------|
| t _{DCO,LPM3/4} | DCO clock wake-up time from LPM3/4 ⁽¹⁾ BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz | 3 V | | 1.5 | | μs |
| t _{CPU,LPM3/4} | CPU wake-up time from LPM3/4 ⁽²⁾ | | | 1/f _{MCLK} + t _{Clock,LPM3/4} | | |

- (1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
 (2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics, DCO Clock Wake-Up Time From LPM3/4

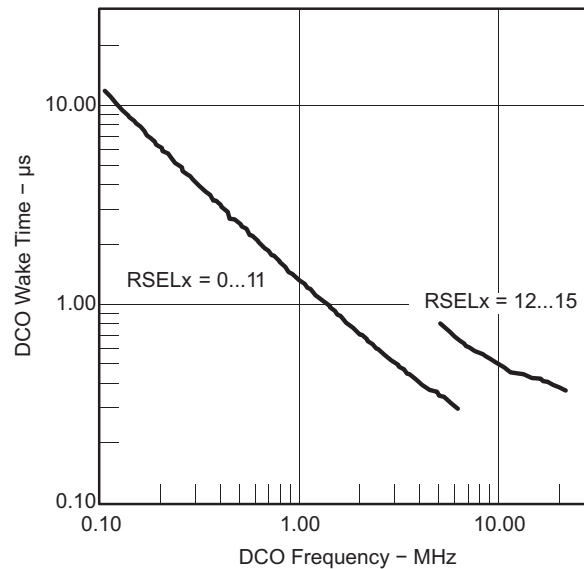


Figure 15. DCO Wake-Up Time From LPM3 vs DCO Frequency

Crystal Oscillator, XT1, Low-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------|--|-----------------|-------|-------|-------|------|
| f _{LFXT1,LF} | LFXT1 oscillator crystal frequency, LF mode 0, 1 | 1.8 V to 3.6 V | | 32768 | | Hz |
| f _{LFXT1,LF,logic} | LFXT1 oscillator logic level square wave input frequency, LF mode | 1.8 V to 3.6 V | 10000 | 32768 | 50000 | Hz |
| O _{A,LF} | XTS = 0, LFXT1Sx = 0, f _{LFXT1,LF} = 32768 Hz, C _{L,eff} = 6 pF | | | 500 | | kΩ |
| | XTS = 0, LFXT1Sx = 0, f _{LFXT1,LF} = 32768 Hz, C _{L,eff} = 12 pF | | | 200 | | |
| C _{L,eff} | XTS = 0, XCAPx = 0 | | | 1 | | pF |
| | XTS = 0, XCAPx = 1 | | | 5.5 | | |
| | XTS = 0, XCAPx = 2 | | | 8.5 | | |
| | XTS = 0, XCAPx = 3 | | | 11 | | |
| | Duty cycle, LF mode | 2.2 V | 30 | 50 | 70 | % |
| f _{Fault,LF} | Oscillator fault frequency, LF mode ⁽³⁾ | 2.2 V | 10 | | 10000 | Hz |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - (a) Keep the trace between the device and the crystal as short as possible.
 - (b) Design a good ground plane around the oscillator pins.
 - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
 - (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (4) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|----------------|-----------------|-----|-----|-----|------|
| f _{VLO} | -40°C to 85°C | 3 V | 4 | 12 | 20 | kHz |
| df _{VLO} /dT | -40°C to 85°C | 3 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} | 25°C | 1.8 V to 3.6 V | | 4 | | %/V |

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------------|-----------------|-----|---------------------|-----|------|
| f _{TA} | SMCLK, duty cycle = 50% ± 10% | | | f _{SYSTEM} | | MHz |
| t _{TA,cap} | TA0, TA1 | 3 V | 20 | | | ns |

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|--|-------------------------------|-----|---------------------|-----|------|
| f _{USCI} | USCI input clock frequency | SMCLK, duty cycle = 50% ± 10% | | f _{SYSTEM} | | MHz |
| f _{max,BITCLK} | Maximum BITCLK clock frequency (equals baudrate in MBaud) ⁽¹⁾ | 3 V | 2 | | | MHz |
| t _r | UART receive deglitch time ⁽²⁾ | 3 V | 50 | 100 | 600 | ns |

(1) The DCO wake-up time must be considered in LPM3 and LPM4 for baud rates above 1 MHz.

(2) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 16](#) and [Figure 17](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|-----------------------------|---|-----|---------------------|-----|------|
| f _{USCI} | USCI input clock frequency | SMCLK, duty cycle = 50% ± 10% | | f _{SYSTEM} | | MHz |
| t _{SU,MI} | SOMI input data setup time | 3 V | 75 | | | ns |
| t _{HD,MI} | SOMI input data hold time | 3 V | 0 | | | ns |
| t _{VALID,MO} | SIMO output data valid time | UCLK edge to SIMO valid, C _L = 20 pF | | | 20 | ns |



Figure 16. SPI Master Mode, CKPH = 0

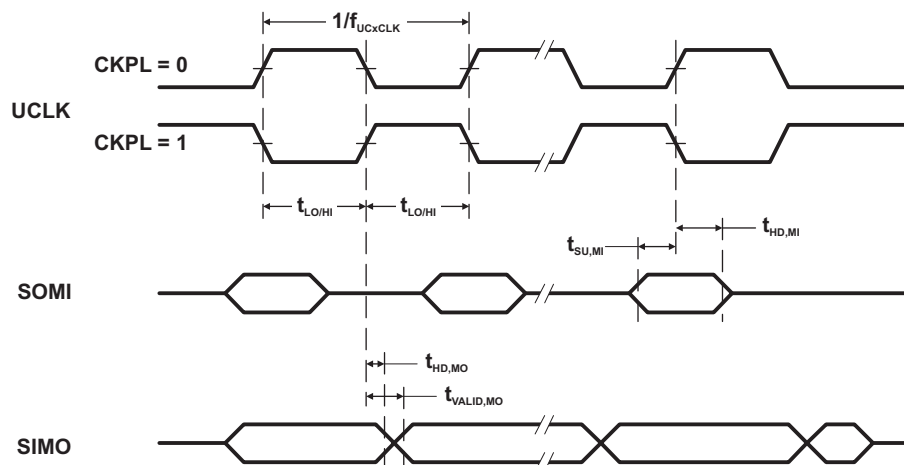


Figure 17. SPI Master Mode, CKPH = 1

USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 18](#) and [Figure 19](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|-----|-----|-----|------|
| t _{STE,LEAD} | STE lead time, STE low to clock | 3 V | | 50 | | ns |
| t _{STE,LAG} | STE lag time, Last clock to STE high | 3 V | 10 | | | ns |
| t _{STE,ACC} | STE access time, STE low to SOMI data out | 3 V | | 50 | | ns |
| t _{STE,DIS} | STE disable time, STE high to SOMI high impedance | 3 V | | 50 | | ns |
| t _{SU,SI} | SIMO input data setup time | 3 V | 15 | | | ns |
| t _{HD,SI} | SIMO input data hold time | 3 V | 10 | | | ns |
| t _{VALID,SO} | SOMI output data valid time | UCLK edge to SOMI valid, C _L = 20 pF | | 50 | 75 | ns |

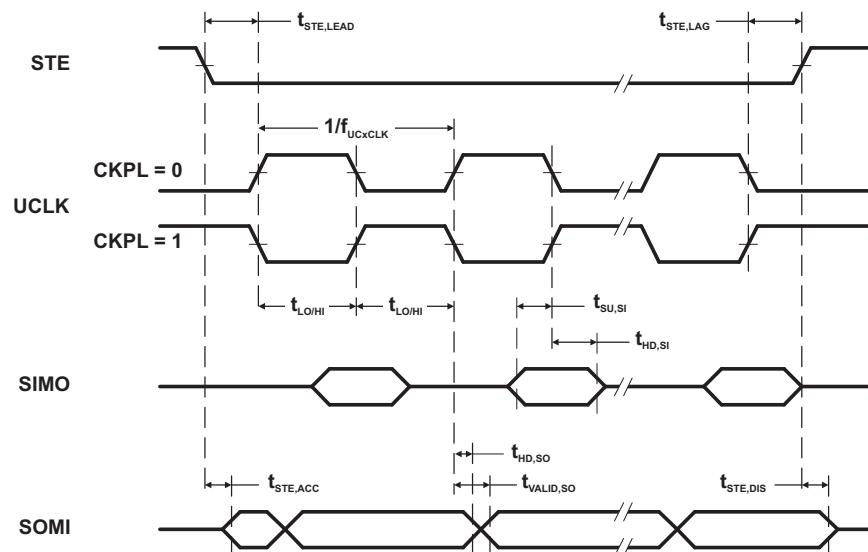


Figure 18. SPI Slave Mode, CKPH = 0

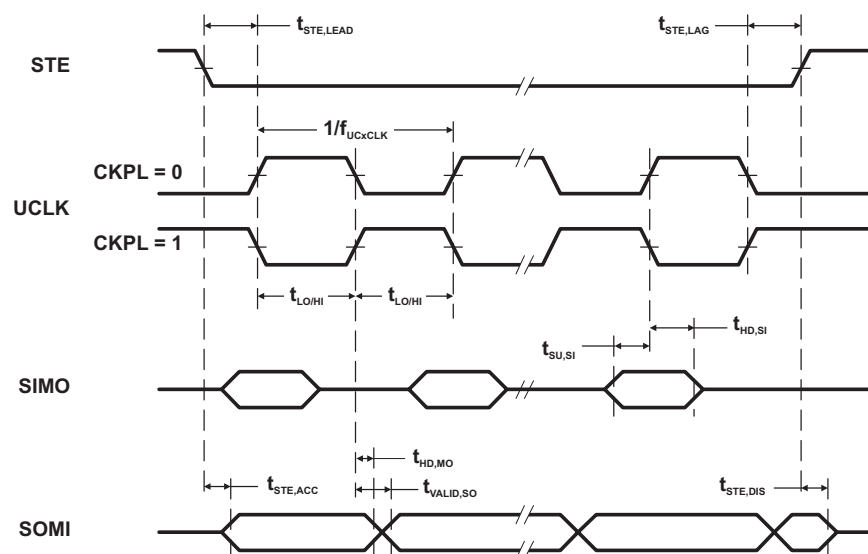


Figure 19. SPI Slave Mode, CKPH = 1

USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 20](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|--|-----------------|----------------------------|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | | | | f _{SYSTEM} | MHz |
| f _{SCL} | SCL clock frequency | 3 V | 0 | | 400 | kHz |
| t _{HD,STA} | Hold time (repeated) START | 3 V | f _{SCL} ≤ 100 kHz | | 4.0 | μs |
| | | | f _{SCL} > 100 kHz | | 0.6 | |
| t _{SU,STA} | Setup time for a repeated START | 3 V | f _{SCL} ≤ 100 kHz | | 4.7 | μs |
| | | | f _{SCL} > 100 kHz | | 0.6 | |
| t _{HD,DAT} | Data hold time | 3 V | 0 | | | ns |
| t _{SU,DAT} | Data setup time | 3 V | 250 | | | ns |
| t _{SU,STO} | Setup time for STOP | 3 V | 4.0 | | | μs |
| t _{SP} | Pulse width of spikes suppressed by input filter | 3 V | 50 | 100 | 600 | ns |

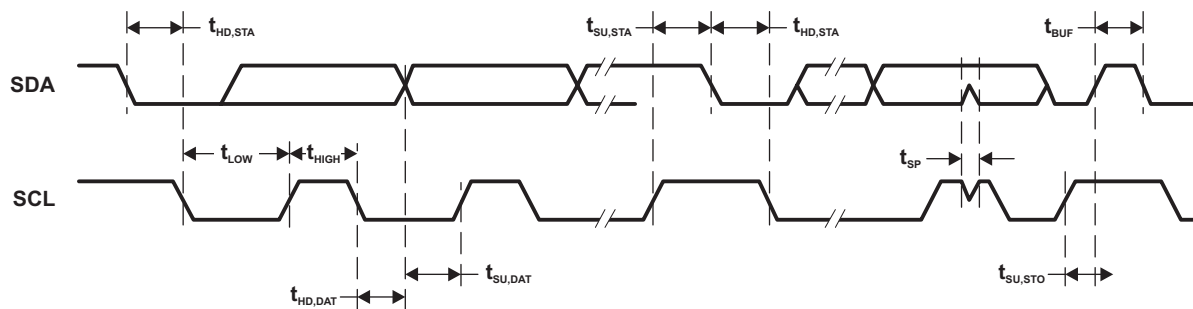


Figure 20. I2C Mode Timing

Comparator_A+

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|-----------------|-----|------|--------------------|------|
| I _(DD) ⁽¹⁾ | CAON = 1, CARSEL = 0, CAREF = 0 | 3 V | | 45 | | μA |
| I _(Refladder/ RefDiode) | CAON = 1, CARSEL = 0, CAREF = 1, 2, or 3, No load at CA0 and CA1 | 3 V | | 45 | | μA |
| V _(IC) | Common-mode input voltage | 3 V | 0 | | V _{CC} -1 | V |
| V _(Ref025) | (Voltage at 0.25 V _{CC} node) / V _{CC} | 3 V | | 0.24 | | |
| V _(Ref050) | (Voltage at 0.5 V _{CC} node) / V _{CC} | 3 V | | 0.48 | | |
| V _(RefVT) | See Figure 21 and Figure 22 | 3 V | | 490 | | mV |
| V _(offset) | Offset voltage ⁽²⁾ | 3 V | | ±10 | | mV |
| V _{hys} | Input hysteresis | 3 V | | 0.7 | | mV |
| t _(response) | Response time (low-high and high-low) | 3 V | | 120 | | ns |
| | | | | 1.5 | | μs |

(1) The leakage current for the Comparator_A+ terminals is identical to I_{lkg(Px.y)} specification.

(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.

Typical Characteristics – Comparator_A+

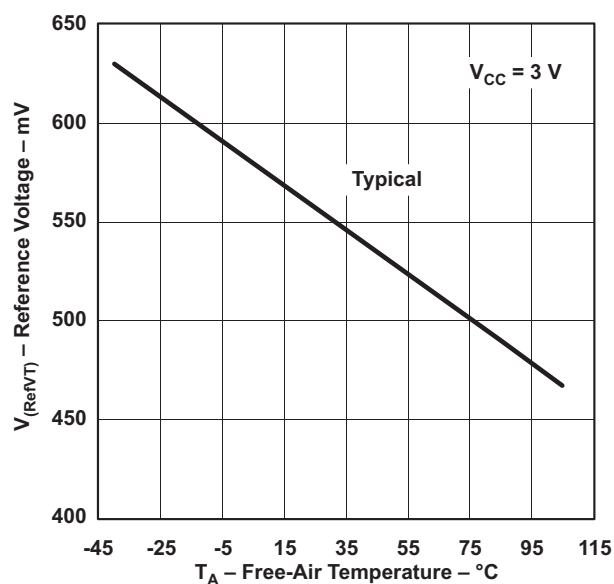


Figure 21. $V_{(RefVT)}$ vs Temperature, $V_{CC} = 3\text{ V}$

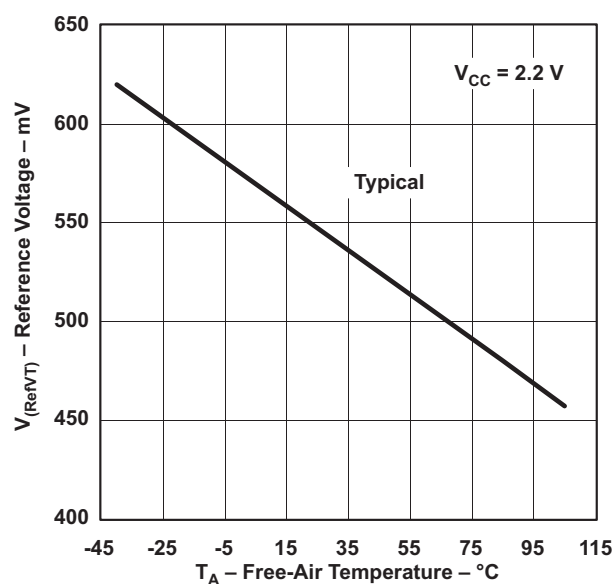


Figure 22. $V_{(RefVT)}$ vs Temperature, $V_{CC} = 2.2\text{ V}$

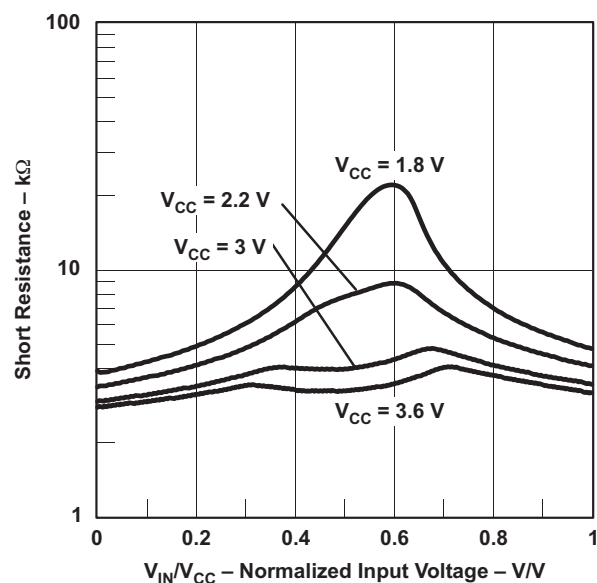


Figure 23. Short Resistance vs V_{IN}/V_{CC}

10-Bit ADC, Power Supply and Input Range Conditions (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|--|---|-----------------|-----|------|-----------------|------|
| V _{CC} | Analog supply voltage | V _{SS} = 0 V | | 2.2 | | 3.6 | V |
| V _{AX} | Analog input voltage ⁽²⁾ | All Ax terminals, Analog inputs selected in ADC10AE register | 3 V | 0 | | V _{CC} | V |
| I _{ADC10} | ADC10 supply current ⁽³⁾ | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0 | 25°C | 3 V | 0.6 | | mA |
| I _{REF+} | Reference supply current, reference buffer disabled ⁽⁴⁾ | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0 | 25°C | 3 V | 0.25 | | mA |
| | | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0 | | | 0.25 | | |
| I _{REFB,0} | Reference buffer supply current with ADC10SR = 0 ⁽⁴⁾ | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0 | 25°C | 3 V | 1.1 | | mA |
| I _{REFB,1} | Reference buffer supply current with ADC10SR = 1 ⁽⁴⁾ | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1 | 25°C | 3 V | 0.5 | | mA |
| C _I | Input capacitance | Only one terminal Ax can be selected at one time | 25°C | 3 V | | 27 | pF |
| R _I | Input MUX ON resistance | 0 V ≤ V _{AX} ≤ V _{CC} | 25°C | 3 V | 1000 | | Ω |

- (1) The leakage current is defined in the leakage current table with Px.y/Ax parameter.
- (2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
- (3) The internal reference supply current is not included in current consumption parameter I_{ADC10}.
- (4) The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

10-Bit ADC, Built-In Voltage Reference (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|-----------------|------|-----|------|--------|
| V _{CC,REF+} | Positive built-in reference analog supply voltage range I _{VREF+} ≤ 1 mA, REF2_5V = 0 | | 2.2 | | | V |
| | I _{VREF+} ≤ 1 mA, REF2_5V = 1 | | 2.9 | | | |
| V _{REF+} | Positive built-in reference voltage I _{VREF+} ≤ I _{VREF+} max, REF2_5V = 0 | 3 V | 1.41 | 1.5 | 1.59 | V |
| | I _{VREF+} ≤ I _{VREF+} max, REF2_5V = 1 | | 2.35 | 2.5 | 2.65 | |
| I _{LD,VREF+} | Maximum VREF+ load current | 3 V | | | ±1 | mA |
| VREF+ load regulation | I _{VREF+} = 500 μA ± 100 μA, Analog input voltage V _{AX} ≠ 0.75 V, REF2_5V = 0 | 3 V | | | ±2 | LSB |
| | I _{VREF+} = 500 μA ± 100 μA, Analog input voltage V _{AX} ≠ 1.25 V, REF2_5V = 1 | | | | ±2 | |
| VREF+ load regulation response time | I _{VREF+} = 100 μA → 900 μA, V _{AX} ≠ 0.5 × VREF+, Error of conversion result ≤ 1 LSB, ADC10SR = 0 | 3 V | | | 400 | ns |
| C _{VREF+} | Maximum capacitance at pin VREF+ | 3 V | | | 100 | pF |
| TC _{REF+} | Temperature coefficient ⁽¹⁾ | 3 V | | | ±100 | ppm/°C |
| t _{REFON} | Settling time of internal reference voltage to 99.9% VREF I _{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 → 1 | 3.6 V | | | 30 | μs |
| t _{REFBURST} | Settling time of reference buffer to 99.9% VREF I _{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1, ADC10SR = 0 | 3 V | | | 2 | μs |

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (-40°C))

10-Bit ADC, External Reference⁽¹⁾ (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|-----------------|-----|-----|-----------------|------|
| VEREF+ Positive external reference input voltage range ⁽²⁾ | VEREF+ > VREF−, SREF1 = 1, SREF0 = 0 | | 1.4 | | V _{CC} | V |
| | VEREF− ≤ VREF+ ≤ V _{CC} − 0.15 V, SREF1 = 1, SREF0 = 1 ⁽³⁾ | | 1.4 | | 3 | |
| VEREF− Negative external reference input voltage range ⁽⁴⁾ | VEREF+ > VREF− | | 0 | | 1.2 | V |
| ΔVEREF Differential external reference input voltage range, ΔVEREF = VREF+ − VREF− | VEREF+ > VREF− ⁽⁵⁾ | | 1.4 | | V _{CC} | V |
| I _{VEREF+} Static input current into VREF+ | 0 V ≤ VREF+ ≤ V _{CC} , SREF1 = 1, SREF0 = 0 | 3 V | | ±1 | | μA |
| | 0 V ≤ VREF+ ≤ V _{CC} − 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1 ⁽³⁾ | 3 V | | 0 | | |
| I _{VEREF−} Static input current into VREF− | 0 V ≤ VREF− ≤ V _{CC} | 3 V | | ±1 | | μA |

- (1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
- (4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

10-Bit ADC, Timing Parameters (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|--|-----------------|------|---|------|------|
| f _{ADC10CLK} ADC10 input clock frequency | For specified performance of ADC10 linearity parameters | 3 V | 0.45 | | 6.3 | MHz |
| | ADC10SR = 0 ADC10SR = 1 | | 0.45 | | 1.5 | |
| f _{ADC10OSC} ADC10 built-in oscillator frequency | ADC10DIVx = 0, ADC10SSELx = 0, f _{ADC10CLK} = f _{ADC10OSC} | 3 V | 3.7 | | 6.3 | MHz |
| t _{CONVERT} Conversion time | ADC10 built-in oscillator, ADC10SSELx = 0, f _{ADC10CLK} = f _{ADC10OSC} | 3 V | 2.06 | | 3.51 | μs |
| | f _{ADC10CLK} from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0 | | | 13 × ADC10DIV × 1/f _{ADC10CLK} | | |
| t _{ADC10ON} Turn-on settling time of the ADC | (1) | | | | 100 | ns |

- (1) The condition is that the error in a conversion started after t_{ADC10ON} is less than ±0.5 LSB. The reference and input signal are already settled.

10-Bit ADC, Linearity Parameters (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|-----------------|-----|------|-----|------|
| E _I Integral linearity error | | 3 V | | | ±1 | LSB |
| E _D Differential linearity error | | 3 V | | | ±1 | LSB |
| E _O Offset error | Source impedance R _S < 100 Ω | 3 V | | | ±1 | LSB |
| E _G Gain error | | 3 V | | ±1.1 | ±2 | LSB |
| E _T Total unadjusted error | | 3 V | | ±2 | ±5 | LSB |

10-Bit ADC, Temperature Sensor and Built-In V_{MID} (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|----------------------|---|---|----------|------|------|----------------|----------------------|
| I_{SENSOR} | Temperature sensor supply current ⁽¹⁾ | REFON = 0, INCHx = 0Ah, $T_A = 25^\circ\text{C}$ | 3 V | | 60 | | μA |
| TC_{SENSOR} | | ADC10ON = 1, INCHx = 0Ah ⁽²⁾ | 3 V | | 3.55 | | mV/ $^\circ\text{C}$ |
| $t_{Sensor(sample)}$ | Sample time required if channel 10 is selected ⁽³⁾ | ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB | 3 V | 30 | | | μs |
| I_{VMID} | Current into divider at channel 11 | ADC10ON = 1, INCHx = 0Bh | 3 V | | | ⁽⁴⁾ | μA |
| V_{MID} | V_{CC} divider at channel 11 | ADC10ON = 1, INCHx = 0Bh, $V_{MID} \neq 0.5 \times V_{CC}$ | 3 V | | 1.5 | | V |
| $t_{VMID(sample)}$ | Sample time required if channel 11 is selected ⁽⁵⁾ | ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB | 3 V | 1220 | | | ns |

- (1) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+} . When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
- (2) The following formula can be used to calculate the temperature sensor output voltage:

$$V_{Sensor,typ} = TC_{Sensor} (273 + T [^\circ\text{C}]) + V_{Offset,sensor} [\text{mV}] \text{ or } V_{Sensor,typ} = TC_{Sensor} T [^\circ\text{C}] + V_{Sensor}(T_A = 0^\circ\text{C}) [\text{mV}]$$
- (3) The typical equivalent impedance of the sensor is 51 k Ω . The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
- (4) No additional current is needed. The V_{MID} is used during sampling.
- (5) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|---------------------|---|--------------------------|-------------|--------|--------|-----|-----------|
| $V_{CC(PGM/ERASE)}$ | Program and erase supply voltage | | | 2.2 | | 3.6 | V |
| f_{FTG} | Flash timing generator frequency | | | 257 | | 476 | kHz |
| I_{PGM} | Supply current from V_{CC} during program | | 2.2 V/3.6 V | | 1 | 5 | mA |
| I_{ERASE} | Supply current from V_{CC} during erase | | 2.2 V/3.6 V | | 1 | 7 | mA |
| t_{CPT} | Cumulative program time ⁽¹⁾ | | 2.2 V/3.6 V | | | 10 | ms |
| $t_{CMErase}$ | Cumulative mass erase time | | 2.2 V/3.6 V | 20 | | | ms |
| | Program/erase endurance | | | 10^4 | 10^5 | | cycles |
| $t_{Retention}$ | Data retention duration | $T_J = 25^\circ\text{C}$ | | 100 | | | years |
| t_{Word} | Word or byte program time | ⁽²⁾ | | | 30 | | t_{FTG} |
| $t_{Block, 0}$ | Block program time for first byte or word | ⁽²⁾ | | | 25 | | t_{FTG} |
| $t_{Block, 1-63}$ | Block program time for each additional byte or word | ⁽²⁾ | | | 18 | | t_{FTG} |
| $t_{Block, End}$ | Block program end-sequence wait time | ⁽²⁾ | | | 6 | | t_{FTG} |
| $t_{Mass Erase}$ | Mass erase time | ⁽²⁾ | | | 10593 | | t_{FTG} |
| $t_{Seg Erase}$ | Segment erase time | ⁽²⁾ | | | 4819 | | t_{FTG} |

- (1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
- (2) These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--|-----------------|-----|-----|------|
| $V_{(RAMh)}$ RAM retention supply voltage ⁽¹⁾ | CPU halted | 1.6 | | V |

- (1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|--|-----------------|----------|-------|-----|-----|------------|
| f_{SBW} Spy-Bi-Wire input frequency | | 2.2 V | 0 | | 20 | MHz |
| $t_{SBW,Low}$ Spy-Bi-Wire low clock pulse duration | | 2.2 V | 0.025 | | 15 | μs |
| $t_{SBW,En}$ Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge ⁽¹⁾) | | 2.2 V | | | 1 | μs |
| $t_{SBW,Ret}$ Spy-Bi-Wire return to normal operation time | | 2.2 V | 15 | | 100 | μs |
| f_{TCK} TCK input frequency ⁽²⁾ | | 2.2 V | 0 | | 5 | MHz |
| $R_{Internal}$ Internal pulldown resistance on TEST | | 2.2 V | 25 | 60 | 90 | k Ω |

- (1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse ⁽¹⁾

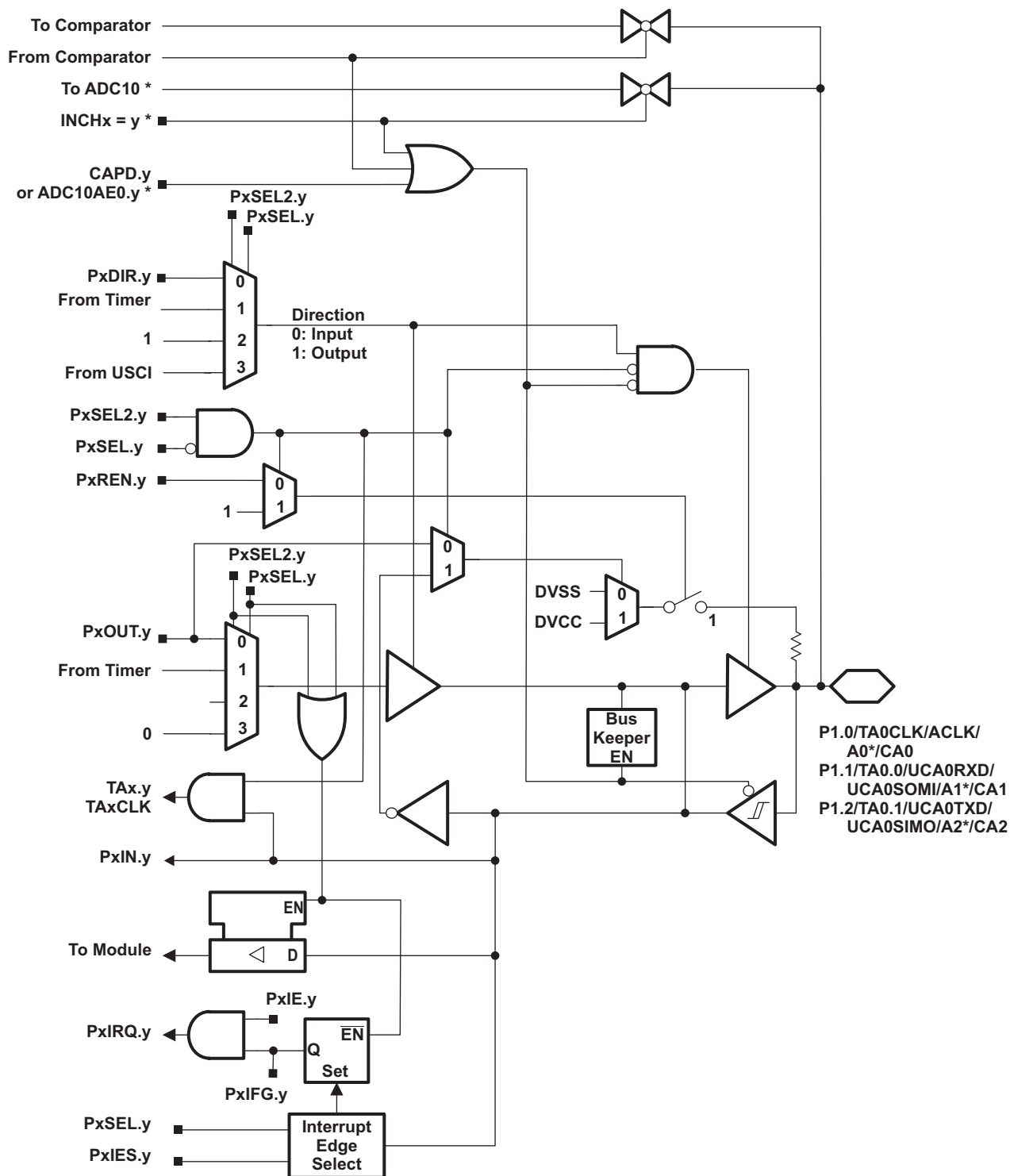
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--|--------------------|-----|-----|------|
| $V_{CC(FB)}$ Supply voltage during fuse-blow condition | $T_A = 25^\circ C$ | 2.5 | | V |
| V_{FB} Voltage level on TEST for fuse blow | | 6 | 7 | V |
| I_{FB} Supply current into TEST during fuse blow | | | 100 | mA |
| t_{FB} Time to blow fuse | | | 1 | ms |

- (1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

PORT SCHEMATICS

Port P1 Pin Schematic: P1.0 to P1.2, Input/Output With Schmitt Trigger



* Note: MSP430G2x53 devices only. MSP430G2x13 devices have no ADC10.

Table 16. Port P1 (P1.0 to P1.2) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | | | |
|--|---|--------------------|---|---------|----------|--------------------------------------|-----------|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x | ADC10AE.x INCH.x=1 ⁽²⁾ | CAPD.y |
| P1.0/ TA0CLK/ ACLK/ A0 ⁽²⁾ / CA0/ Pin Osc | 0 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 |
| | | TA0.TACLK | 0 | 1 | 0 | 0 | 0 |
| | | ACLK | 1 | 1 | 0 | 0 | 0 |
| | | A0 | X | X | X | 1 (y = 0) | 0 |
| | | CA0 | X | X | X | 0 | 1 (y = 0) |
| | | Capacitive sensing | X | 0 | 1 | 0 | 0 |
| P1.1/ TA0.0/ UCA0RXD/ UCA0SOMI/ A1 ⁽²⁾ / CA1/ Pin Osc | 1 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 |
| | | TA0.0 | 1 | 1 | 0 | 0 | 0 |
| | | TA0.CCI0A | 0 | 1 | 0 | 0 | 0 |
| | | UCA0RXD | from USCI | 1 | 1 | 0 | 0 |
| | | UCA0SOMI | from USCI | 1 | 1 | 0 | 0 |
| | | A1 | X | X | X | 1 (y = 1) | 0 |
| | | CA1 | X | X | X | 0 | 1 (y = 1) |
| | | Capacitive sensing | X | 0 | 1 | 0 | 0 |
| P1.2/ TA0.1/ UCA0TXD/ UCA0SIMO/ A2 ⁽²⁾ / CA2/ Pin Osc | 2 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 |
| | | TA0.1 | 1 | 1 | 0 | 0 | 0 |
| | | TA0.CCI1A | 0 | 1 | 0 | 0 | 0 |
| | | UCA0TXD | from USCI | 1 | 1 | 0 | 0 |
| | | UCA0SIMO | from USCI | 1 | 1 | 0 | 0 |
| | | A2 | X | X | X | 1 (y = 2) | 0 |
| | | CA2 | X | X | X | 0 | 1 (y = 2) |
| | | Capacitive sensing | X | 0 | 1 | 0 | 0 |

(1) X = don't care

(2) MSP430G2x53 devices only

[illegible]

* Note: MSP430G2x53 devices only. MSP430G2x13 devices have no ADC10.

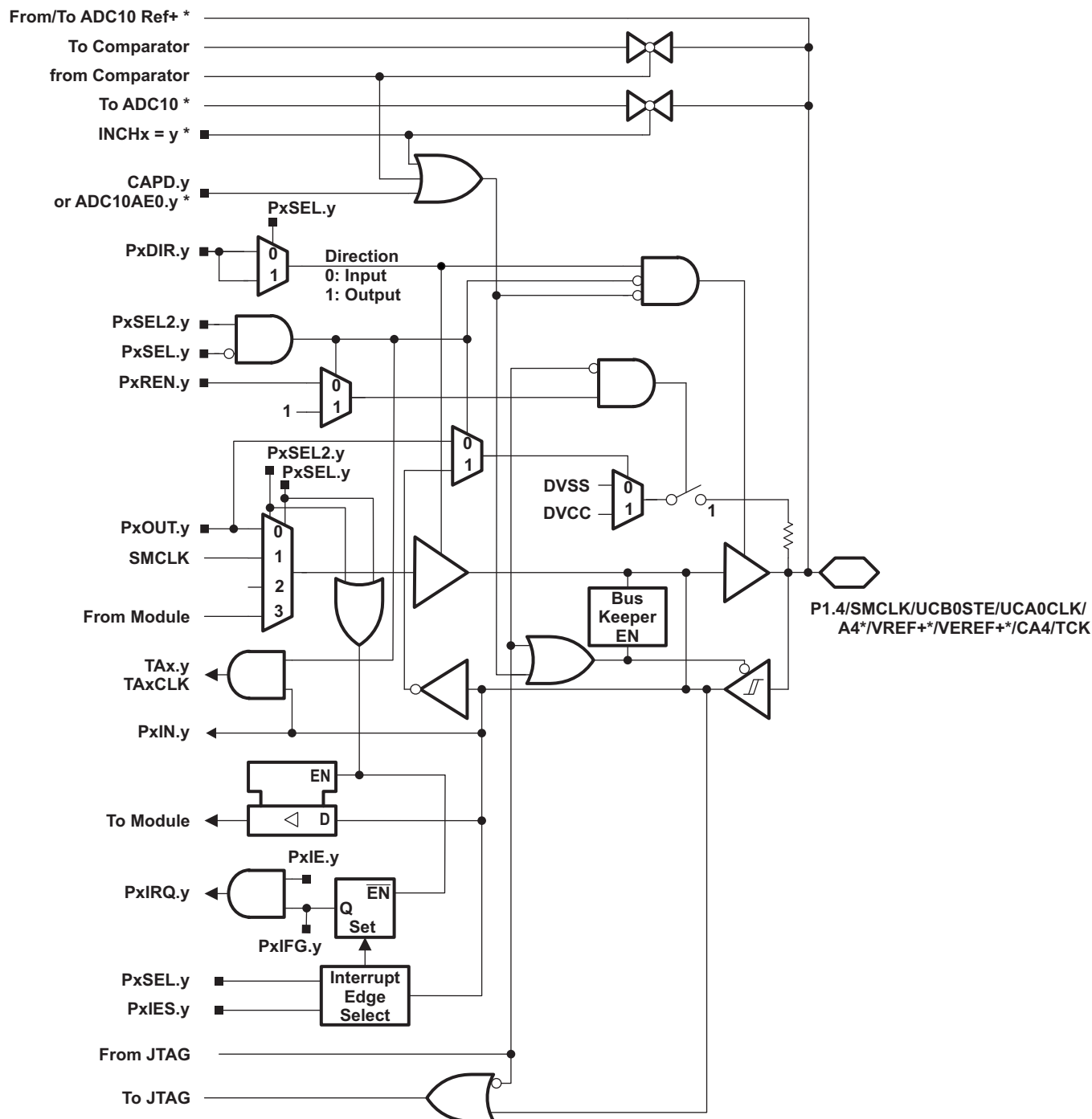
Table 17. Port P1 (P1.3) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | | | |
|---|---|--------------------|---|---------|----------|--------------------------------------|-----------|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x | ADC10AE.x INCH.x=1 ⁽²⁾ | CAPD.y |
| P1.3/ ADC10CLK ⁽²⁾ / CAOUT/ A3 ⁽²⁾ / VREF- ⁽²⁾ / VEREF- ⁽²⁾ / CA3/ Pin Osc | 3 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 |
| | | ADC10CLK | 1 | 1 | 0 | 0 | 0 |
| | | CAOUT | 1 | 1 | 1 | 0 | 0 |
| | | A3 | X | X | X | 1 (y = 3) | 0 |
| | | VREF- | X | X | X | 1 | 0 |
| | | VEREF- | X | X | X | 1 | 0 |
| | | CA3 | X | X | X | 0 | 1 (y = 3) |
| | | Capacitive sensing | X | 0 | 1 | 0 | 0 |

(1) X = don't care

(2) MSP430G2x53 devices only

Port P1 Pin Schematic: P1.4, Input/Output With Schmitt Trigger



* Note: MSP430G2x52 devices only. MSP430G2x12 devices have no ADC10.

Table 18. Port P1 (P1.4) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | | | | |
|-------------------------|---|--------------------|---|---------|----------|--------------------------------------|-----------|-----------|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x | ADC10AE.x INCH.x=1 ⁽²⁾ | JTAG Mode | CAPD.y |
| P1.4/ | 4 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 |
| SMCLK/ | | SMCLK | 1 | 1 | 0 | 0 | 0 | 0 |
| UCB0STE/ | | UCB0STE | from USCI | 1 | 1 | 0 | 0 | 0 |
| UCA0CLK/ | | UCA0CLK | from USCI | 1 | 1 | 0 | 0 | 0 |
| VREF+ ⁽²⁾ / | | VREF+ | X | X | X | 1 | 0 | 0 |
| VEREF+ ⁽²⁾ / | | VEREF+ | X | X | X | 1 | 0 | 0 |
| A4 ⁽²⁾ / | | A4 | X | X | X | 1 (y = 4) | 0 | 0 |
| CA4 | | CA4 | X | X | X | 0 | 0 | 1 (y = 4) |
| TCK/ | | TCK | X | X | X | 0 | 1 | 0 |
| Pin Osc | | Capacitive sensing | X | 0 | 1 | 0 | 0 | 0 |

(1) X = don't care

(2) MSP430G2x53 devices only

Port P1 Pin Schematic: P1.5 to P1.7, Input/Output With Schmitt Trigger

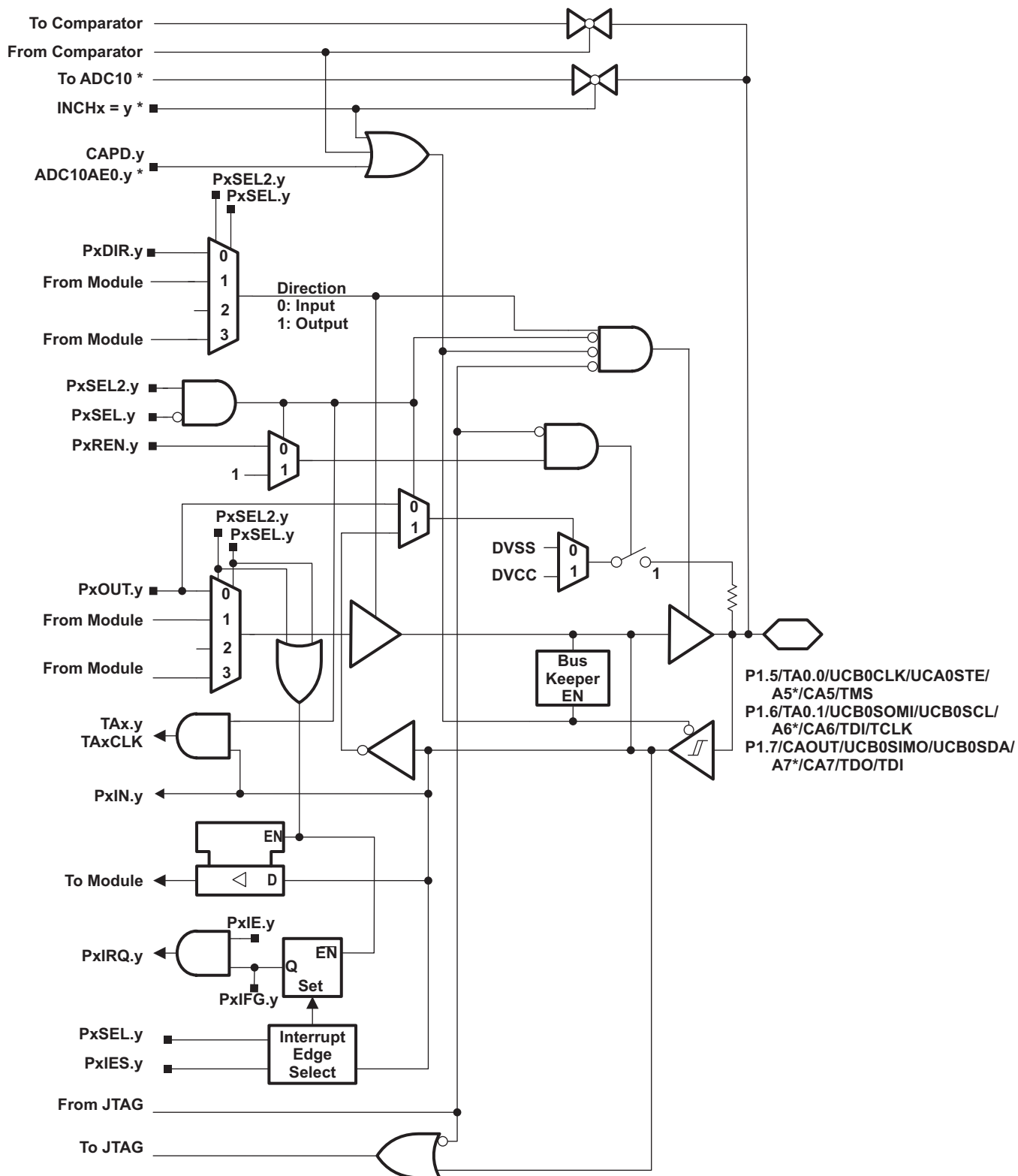


Table 19. Port P1 (P1.5 to P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | | | | |
|--|---|--------------------|---|---------|----------|--------------------------------------|-----------|-----------|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x | ADC10AE.x INCH.x=1 ⁽²⁾ | JTAG Mode | CAPD.y |
| P1.5/ TA0.0/ UCB0CLK/ UCA0STE/ A5 ⁽²⁾ / CA5 TMS Pin Osc | 5 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 |
| | | TA0.0 | 1 | 1 | 0 | 0 | 0 | 0 |
| | | UCB0CLK | from USCI | 1 | 1 | 0 | 0 | 0 |
| | | UCA0STE | from USCI | 1 | 1 | 0 | 0 | 0 |
| | | A5 | X | X | X | 1 (y = 5) | 0 | 0 |
| | | CA5 | X | X | X | 0 | 0 | 1 (y = 5) |
| | | TMS | X | X | X | 0 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 | 0 | 0 | 0 |
| P1.6/ TA0.1/ UCB0SOMI/ UCB0SCL/ A6 ⁽²⁾ / CA6 TDI/TCLK/ Pin Osc | 6 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 |
| | | TA0.1 | 1 | 1 | 0 | 0 | 0 | 0 |
| | | UCB0SOMI | from USCI | 1 | 1 | 0 | 0 | 0 |
| | | UCB0SCL | from USCI | 1 | 1 | 0 | 0 | 0 |
| | | A6 | X | X | X | 1 (y = 6) | 0 | 0 |
| | | CA6 | X | X | X | 0 | 0 | 1 (y = 6) |
| | | TDI/TCLK | X | X | X | 0 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 | 0 | 0 | 0 |
| P1.7/ UCB0SIMO/ UCB0SDA/ A7 ⁽²⁾ / CA7 CAOUT TDO/TDI/ Pin Osc | 7 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 |
| | | UCB0SIMO | from USCI | 1 | 1 | 0 | 0 | 0 |
| | | UCB0SDA | from USCI | 1 | 1 | 0 | 0 | 0 |
| | | A7 | X | X | X | 1 (y = 7) | 0 | 0 |
| | | CA7 | X | X | X | 0 | 0 | 1 (y = 7) |
| | | CAOUT | 1 | 1 | 0 | 0 | 0 | 0 |
| | | TDO/TDI | X | X | X | 0 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 | 0 | 0 | 0 |

(1) X = don't care

(2) MSP430G2x53 devices only

Port P2 Pin Schematic: P2.0 to P2.5, Input/Output With Schmitt Trigger

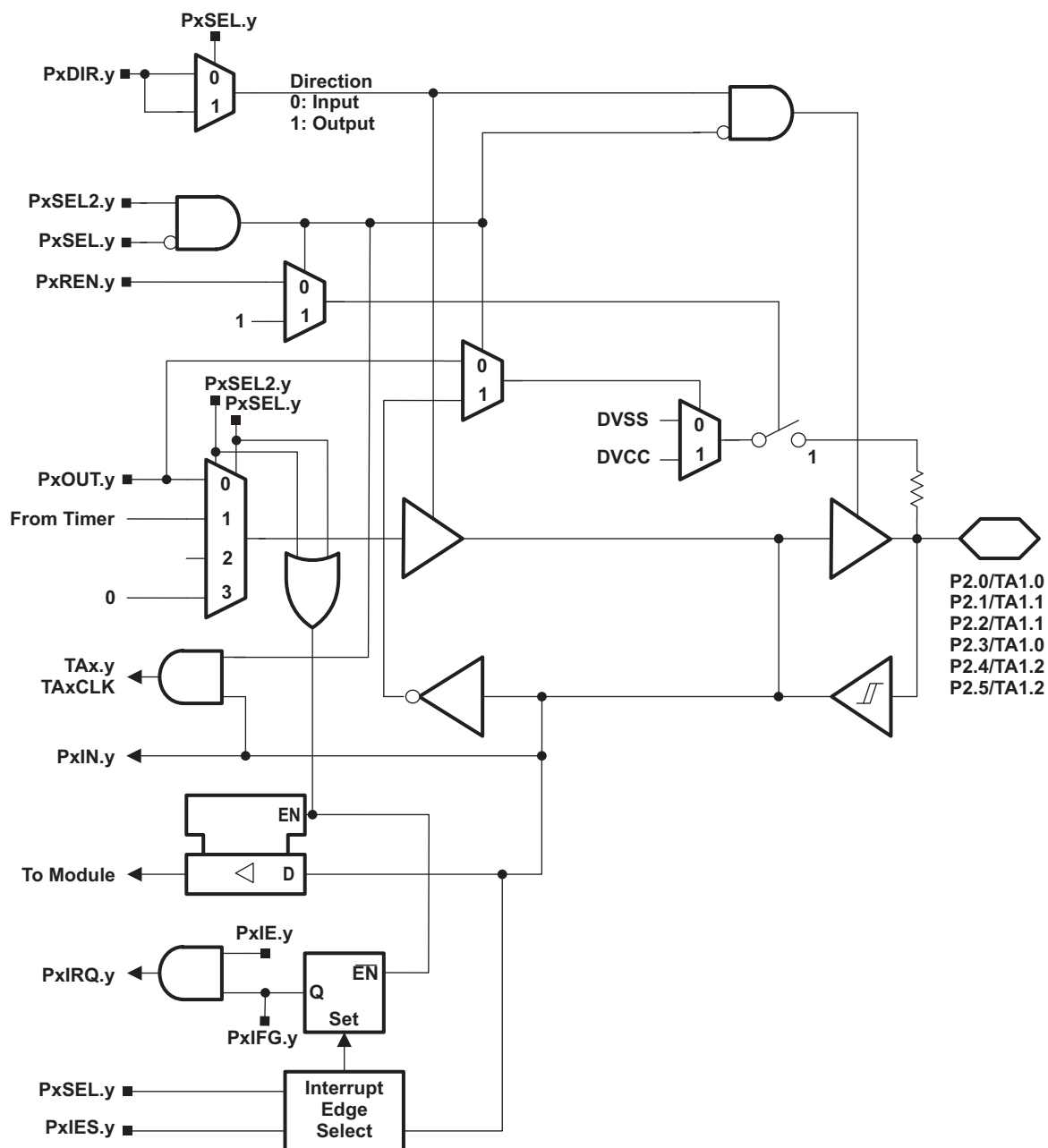


Table 20. Port P2 (P2.0 to P2.5) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | |
|--------------------------------|---|--------------------|---|---------|----------|
| | | | P2DIR.x | P2SEL.x | P2SEL2.x |
| P2.0/ TA1.0/ Pin Osc | 0 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer1_A3.CCI0A | 0 | 1 | 0 |
| | | Timer1_A3.TA0 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |
| P2.1/ TA1.1/ Pin Osc | 1 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer1_A3.CCI1A | 0 | 1 | 0 |
| | | Timer1_A3.TA1 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |
| P2.2/ TA1.1/ Pin Osc | 2 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer1_A3.CCI1B | 0 | 1 | 0 |
| | | Timer1_A3.TA1 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |
| P2.3/ TA1.0/ Pin Osc | 3 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer1_A3.CCI0B | 0 | 1 | 0 |
| | | Timer1_A3.TA0 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |
| P2.4/ TA1.2/ Pin Osc | 4 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer1_A3.CCI2A | 0 | 1 | 0 |
| | | Timer1_A3.TA2 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |
| P2.5/ TA1.2/ Pin Osc | 5 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer1_A3.CCI2B | 0 | 1 | 0 |
| | | Timer1_A3.TA2 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |

(1) X = don't care

The logic diagram illustrates the internal architecture of the P2.6 peripheral module. Key components and signals include:

- Inputs:** LF off, PxSEL.6 and PxSEL.7, BCCTL3.LFXT1Sx = 11, PxSEL.y, PxDIR.y, PxSEL2.y, PxSEL.y, PxREN.y, PxOUT.y, From Module, Tax.y, TaxCLK, PxiN.y, PxiE.y, PxiFG.y, PxSEL.y, PxiES.y.
- Outputs:** XOUT/P2.7, Lfxt1CLK, Direction (0: Input, 1: Output), DVSS, DVCC, XIN/P2.6/TA0.1, To Module, PxiIRQ.y.
- Internal Logic:** The diagram features a complex network of logic gates (AND, OR, NOT, NAND, NOR), multiplexers (0/1, 0/1/2/3), and a D flip-flop. It also includes a block labeled "Interrupt Edge Select" and a "Q Set" block.
- Control Signals:** The "Direction" signal (0: Input, 1: Output) and the "Q Set" block are used to configure the module's operation.

Table 21. Port P2 (P2.6) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | |
|--------------------|---|--------------------|---|--------------------|----------------------|
| | | | P2DIR.x | P2SEL.6 P2SEL.7 | P2SEL2.6 P2SEL2.7 |
| XIN | 6 | XIN | 0 | 1 1 | 0 0 |
| P2.6 | | P2.x (I/O) | I: 0; O: 1 | 0 X | 0 0 |
| TA0.1 | | Timer0_A3.TA1 | 1 | 1 0 | 0 0 |
| Pin Osc | | Capacitive sensing | X | 0 X | 1 X |

(1) X = don't care

Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger

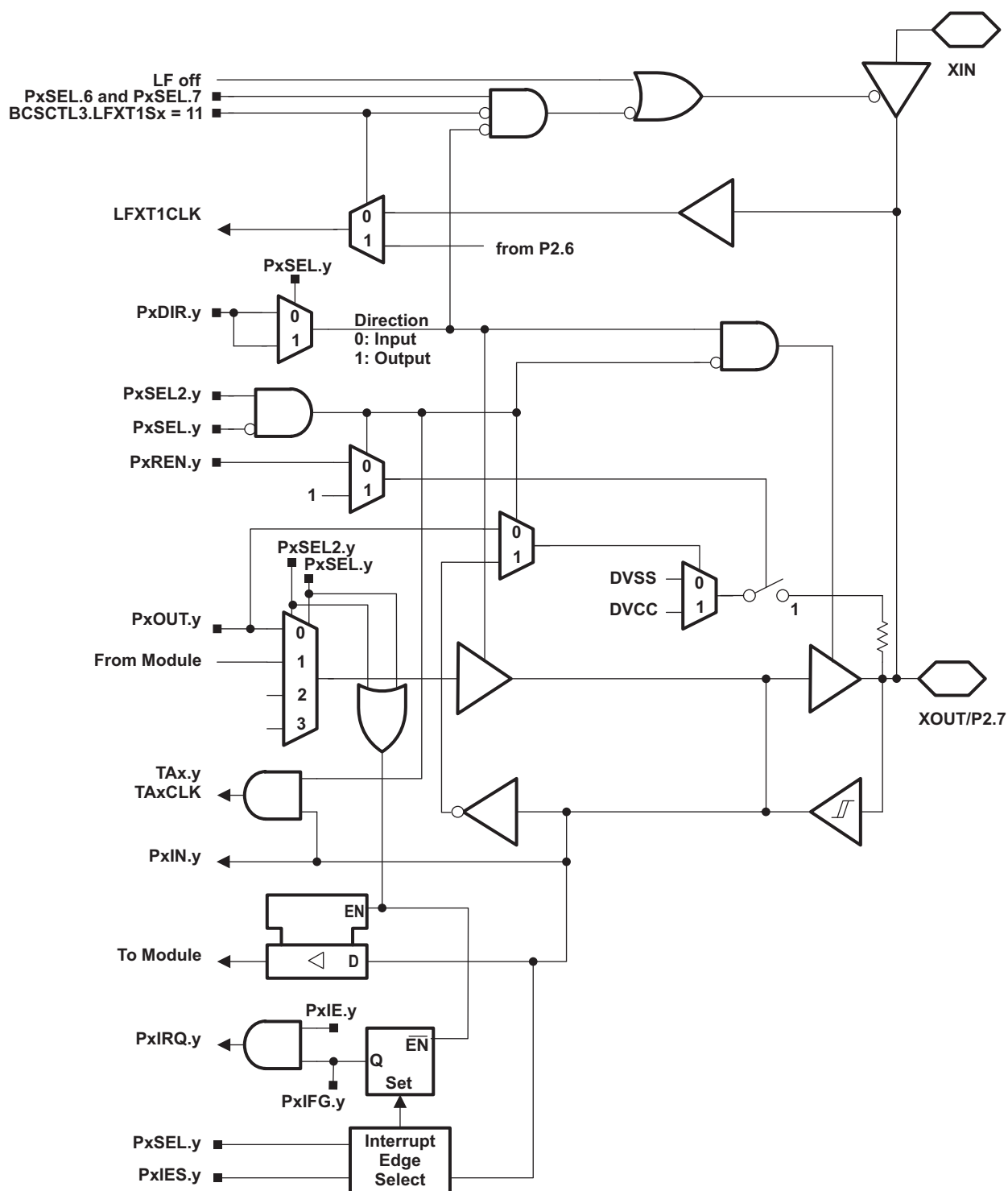


Table 22. Port P2 (P2.7) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | |
|--------------------|---|--------------------|---|--------------------|----------------------|
| | | | P2DIR.x | P2SEL.6 P2SEL.7 | P2SEL2.6 P2SEL2.7 |
| XOUT/ | 7 | XOUT | 1 | 1 1 | 0 0 |
| P2.7/ | | P2.x (I/O) | I: 0; O: 1 | 0 X | 0 0 |
| Pin Osc | | Capacitive sensing | X | 0 X | 1 X |

(1) X = don't care

Port P3 Pin Schematic: P3.0 to P3.7, Input/Output With Schmitt Trigger (28-Pin PW and 32-Pin RHB Packages Only)

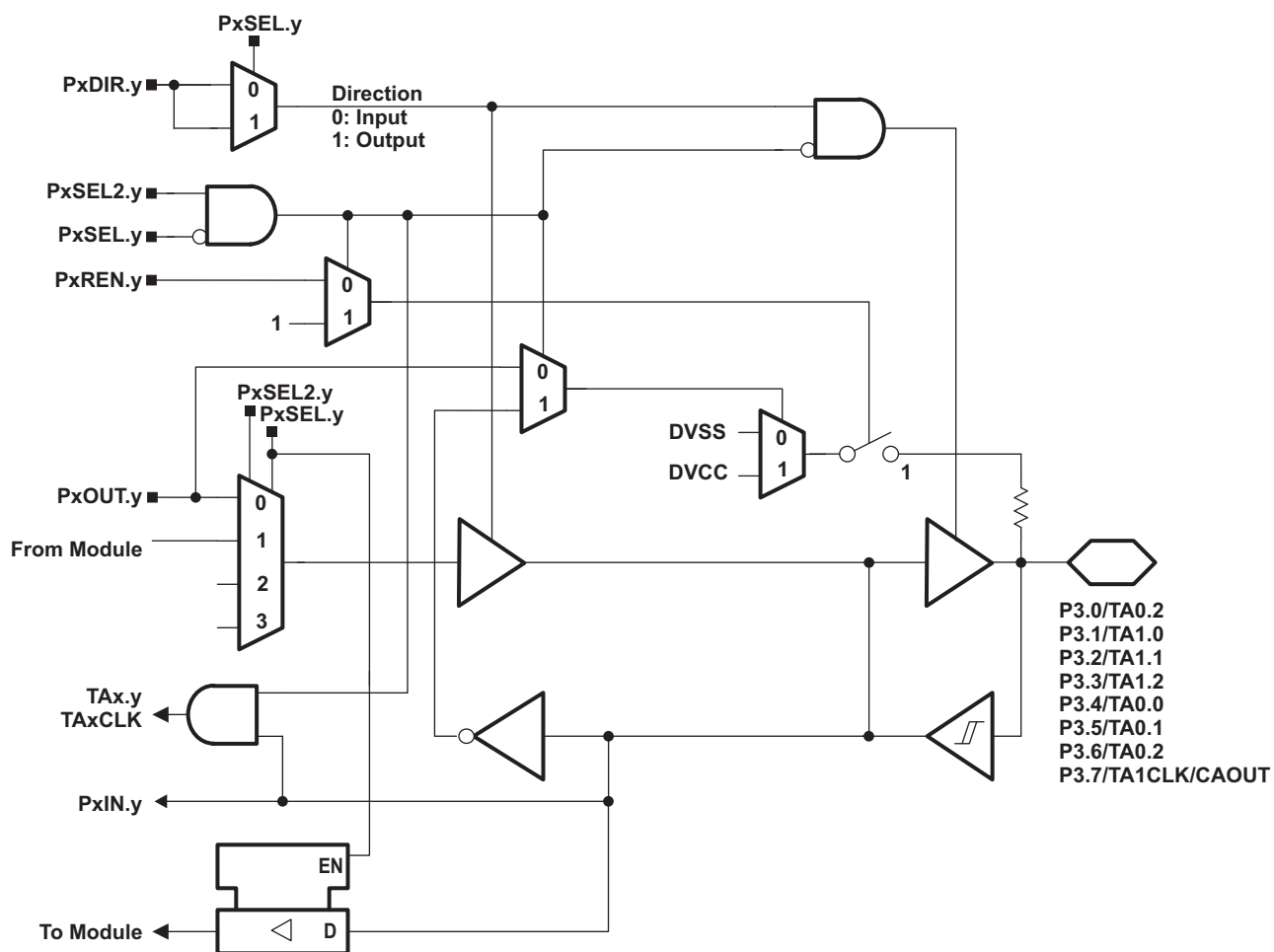


Table 23. Port P3 (P3.0 to P3.7) Pin Functions (28-Pin PW and 32-Pin RHB Packages Only)

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | |
|---------------------------------------|---|--------------------|---|---------|----------|
| | | | P3DIR.x | P3SEL.x | P3SEL2.x |
| P3.0/ TA0.2/ Pin Osc | 0 | P3.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer0_A3.CCI2A | 0 | 1 | 0 |
| | | Timer0_A3.TA2 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |
| P3.1/ TA1.0/ Pin Osc | 1 | P3.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer1_A3.TA0 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |
| P3.2/ TA1.1/ Pin Osc | 2 | P3.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer1_A3.TA1 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |
| P3.3/ TA1.2/ Pin Osc | 3 | P3.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer1_A3.TA2 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |
| P3.4/ TA0.0/ Pin Osc | 4 | P3.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer0_A3.TA0 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |
| P3.5/ TA0.1/ Pin Osc | 5 | P3.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer0_A3.TA1 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |
| P3.6/ TA0.2/ Pin Osc | 6 | P3.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer0_A3.TA2 | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |
| P3.7/ TA1CLK/ CAOUT/ Pin Osc | 7 | P3.x (I/O) | I: 0; O: 1 | 0 | 0 |
| | | Timer1_A3.TACLK | 0 | 1 | 0 |
| | | Comparator output | 1 | 1 | 0 |
| | | Capacitive sensing | X | 0 | 1 |

(1) X = don't care

REVISION HISTORY

| REVISION | DESCRIPTION |
|----------|--|
| SLAS735 | Initial release |
| SLAS735A | Changed Control Bits / Signals column in Table 18 Changed Pin Name and Function columns in Table 23 |
| SLAS735B | Changed Storage temperature range limit in Absolute Maximum Ratings Added BSL functions to P1.1 and P1.5 in Table 2 . Added CAOUT information to Table 17 . |
| SLAS735C | Changed T _{stg} , Programmed device, to -55°C to 150°C in Absolute Maximum Ratings . Changed TAG_ADC10_1 value to 0x10 in Table 10 . |
| SLAS735D | Added AVCC (RHB package only, pin 29) to Table 2 Terminal Functions. Corrected typo in P3.7/TA1CLK/CAOUT description in Table 2 . Corrected PW28 terminal assignment in Input and Output Pin Number columns in Table 13 . Changed all port schematics (added buffer after PxOUT.y mux) in Port Schematics . |
| SLAS735E | Table 5 and Table 14 , Corrected Timer_A register names. |
| SLAS735F | Added note on TC _{REF+} in 10-Bit ADC, Built-In Voltage Reference (MSP430G2x53 Only) . Corrected signal names on Port P1 Pin Schematic: P1.4, Input/Output With Schmitt Trigger . |
| SLAS735G | Recommended Operating Conditions , Removed mention of USART module from f _{SYSTEM} description. Port P3 Pin Schematic: P3.0 to P3.7, Input/Output With Schmitt Trigger (28-Pin PW and 32-Pin RHB Packages Only) , Added PW28 to available packages. |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|--------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|-----------------------------|
| MSP430G2113IN20 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2113IPW20 | ACTIVE | TSSOP | PW | 20 | 1 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2113IPW20R | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2113IPW28 | ACTIVE | TSSOP | PW | 28 | 1 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2113IPW28R | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2113IRHB32R | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2113IRHB32T | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2153IN20 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2153IPW20 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2153IPW20R | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2153IPW28 | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2153IPW28R | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2153IRHB32R | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2153IRHB32T | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2213IN20 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2213IPW20 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2213IPW20R | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|--------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|-----------------------------|
| MSP430G2213IPW28 | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2213IPW28R | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2213IRHB32R | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2213IRHB32T | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2253IN20 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2253IPW20 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2253IPW20R | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2253IPW28 | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2253IPW28R | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2253IRHB32R | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2253IRHB32T | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2313IN20 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2313IPW20 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2313IPW20R | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2313IPW28 | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2313IPW28R | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2313IRHB32R | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2313IRHB32T | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|--------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|-----------------------------|
| MSP430G2353IN20 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2353IPW20 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2353IPW20R | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2353IPW28 | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2353IPW28R | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2353IRHB32R | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2353IRHB32T | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2413IN20 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2413IPW20 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2413IPW20R | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2413IPW28 | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2413IPW28R | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2413IRHB32R | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2413IRHB32T | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2453IN20 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2453IPW20 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2453IPW20R | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2453IPW28 | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|--------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|-----------------------------|
| MSP430G2453IPW28R | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2453IRHB32R | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2453IRHB32T | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2513IN20 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2513IPW20 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2513IPW20R | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2513IPW28 | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2513IPW28R | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2513IRHB32R | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2513IRHB32T | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430G2553CY | PREVIEW | DIESALE | Y | 0 | 405 | Green (RoHS & no Sb/Br) | Call TI | N / A for Pkg Type | |
| MSP430G2553CYS | PREVIEW | WAFERSALE | YS | 0 | | TBD | Call TI | Call TI | |
| MSP430G2553GACYS | PREVIEW | WAFERSALE | YS | 0 | 1 | TBD | Call TI | Call TI | |
| MSP430G2553IN20 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2553IPW20 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2553IPW20R | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2553IPW28 | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2553IPW28R | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430G2553IRHB32R | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|--------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|-----------------------------|
| MSP430G2553IRHB32T | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



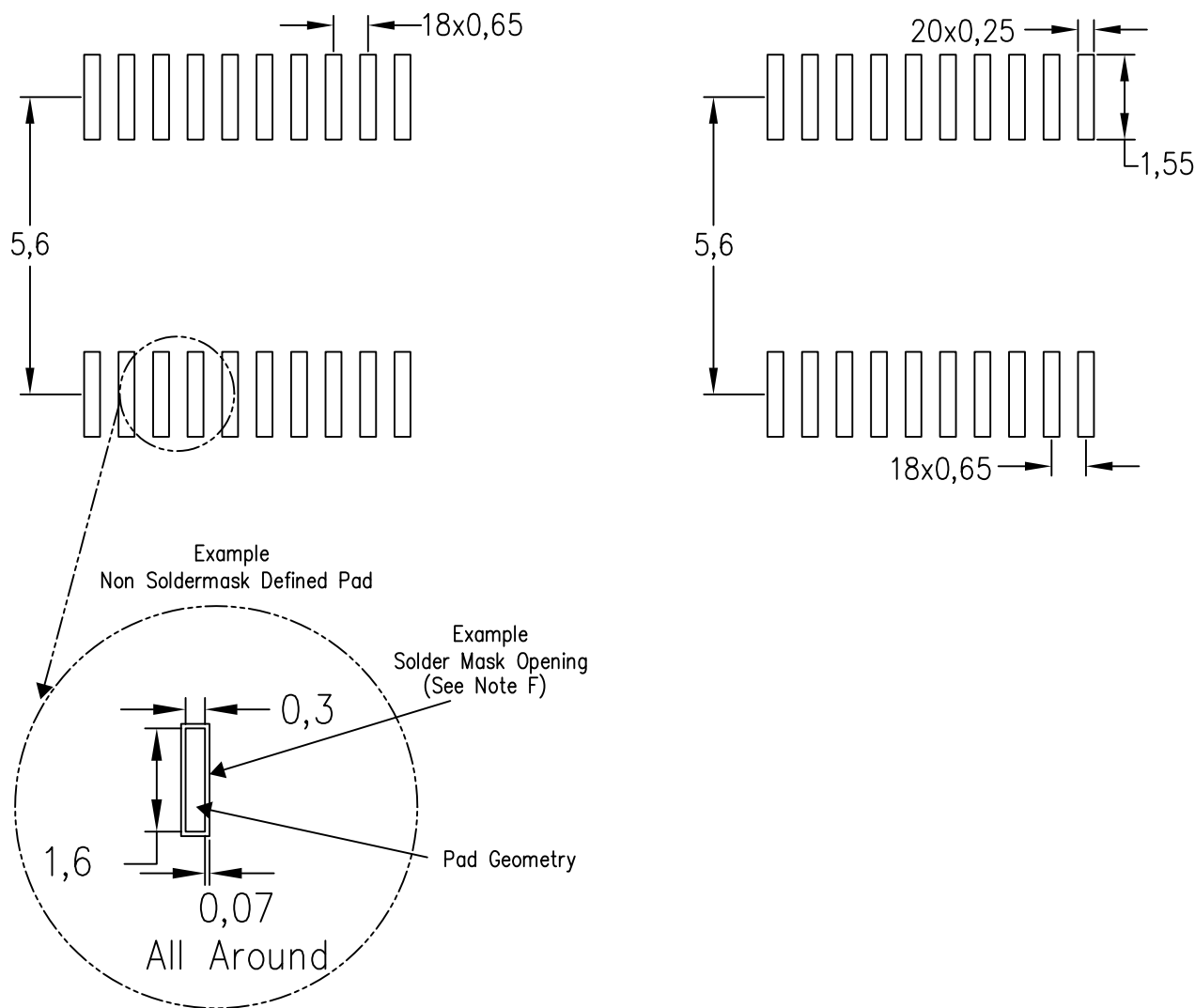
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

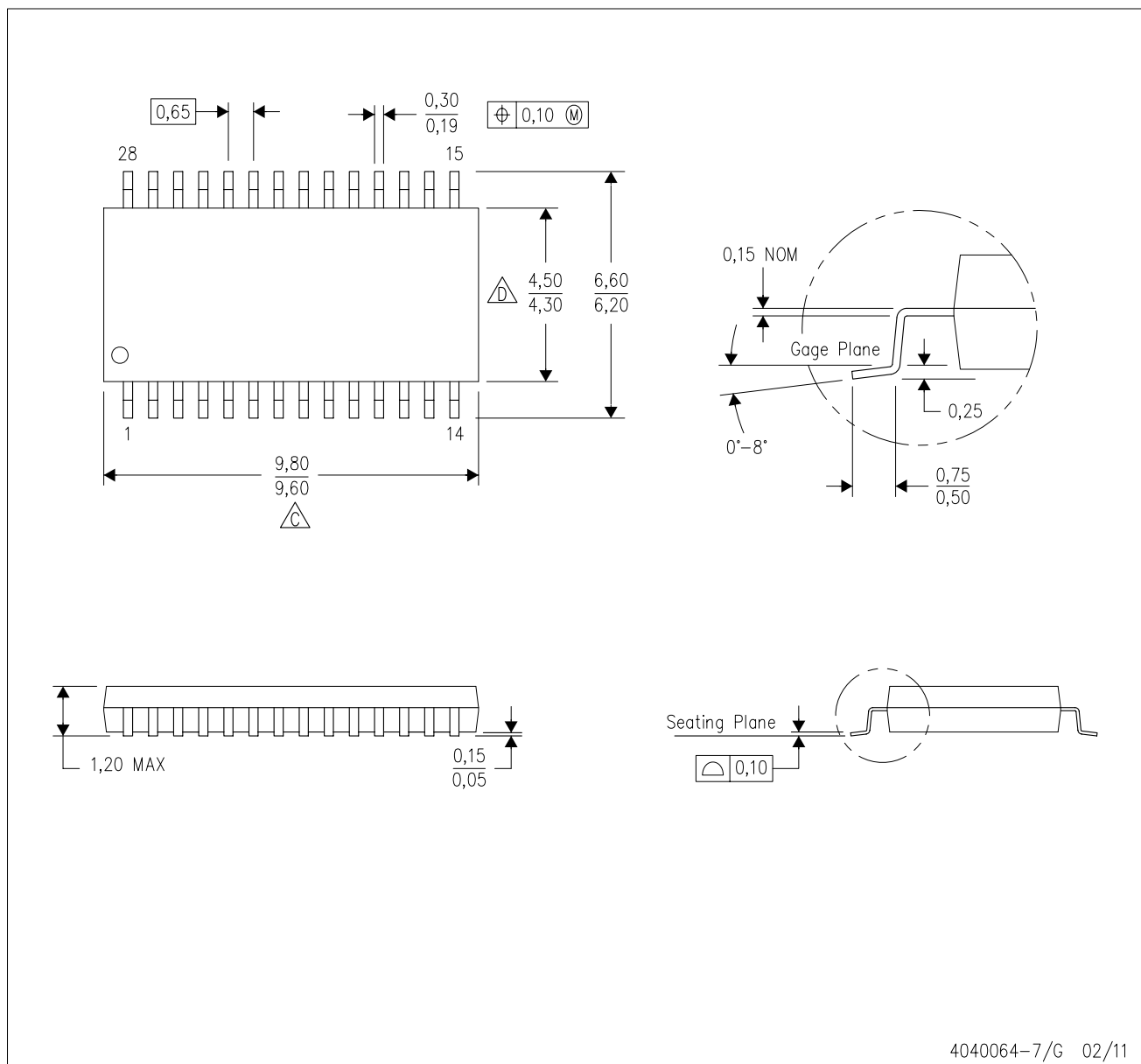


4211284-5/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

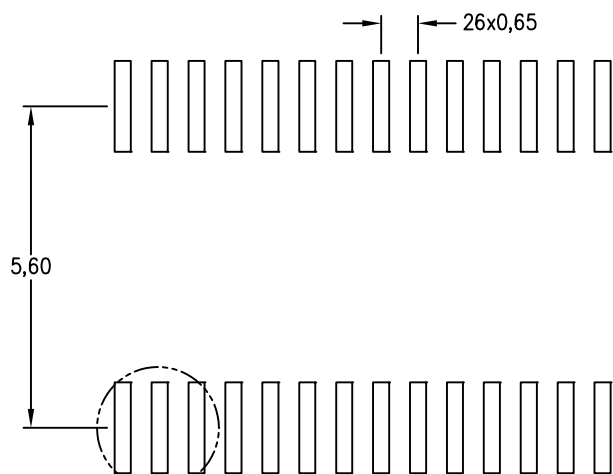


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

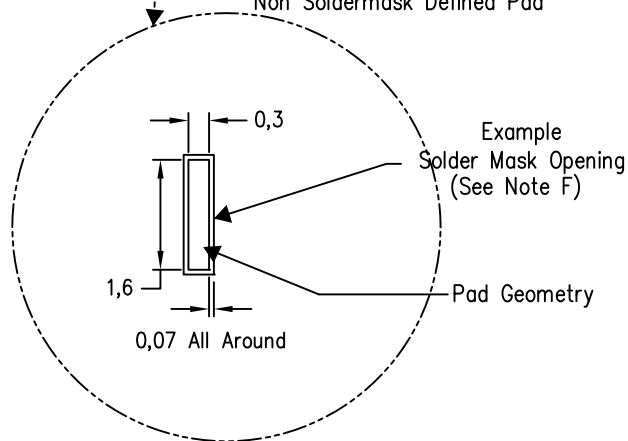
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

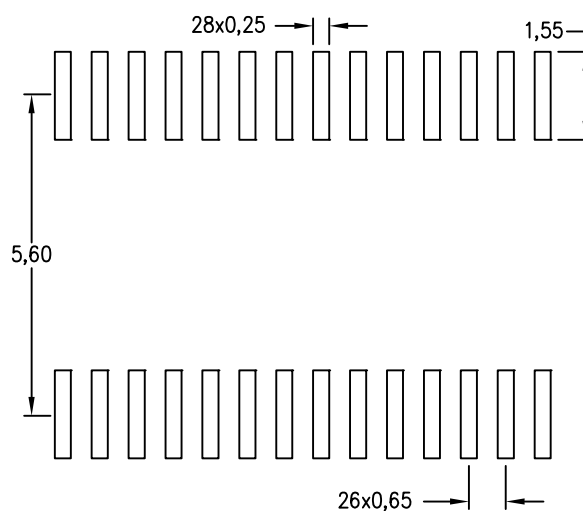
Example Board Layout



Example
Non Soldermask Defined Pad



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



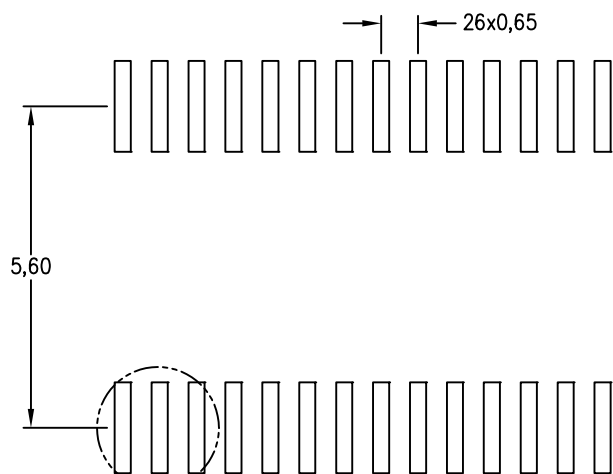
4211284-6/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

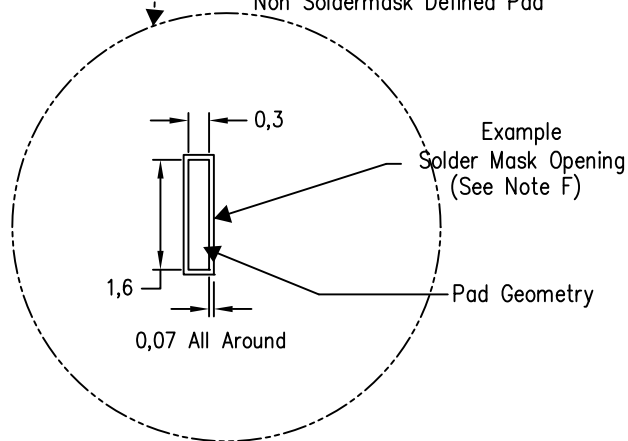
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

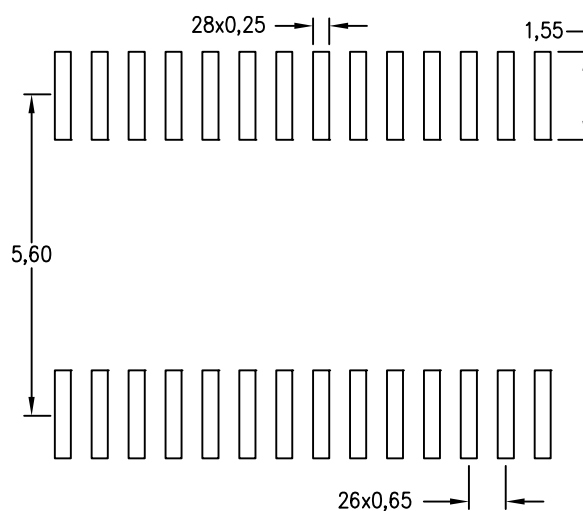
Example Board Layout



Example
Non Soldermask Defined Pad



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

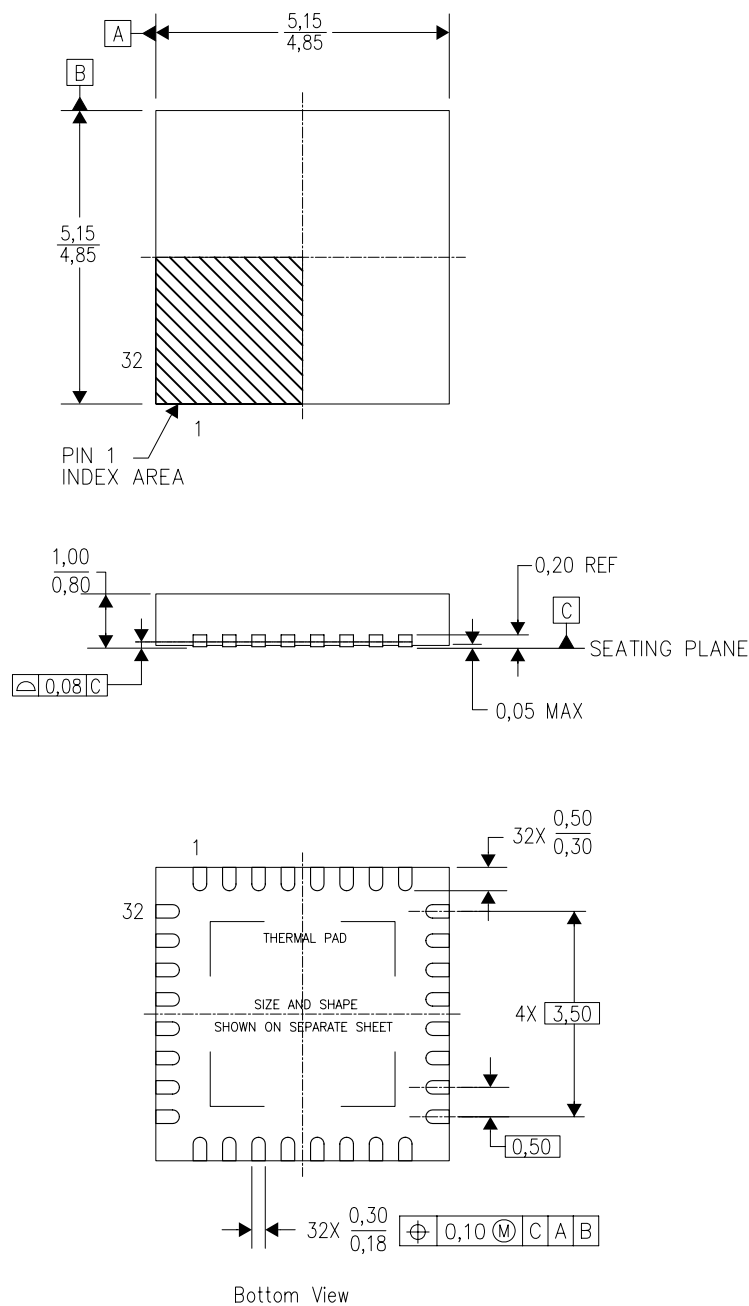


4211284-6/F 12/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate design.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4204326/D 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

RHB (S-PVQFN-N32)

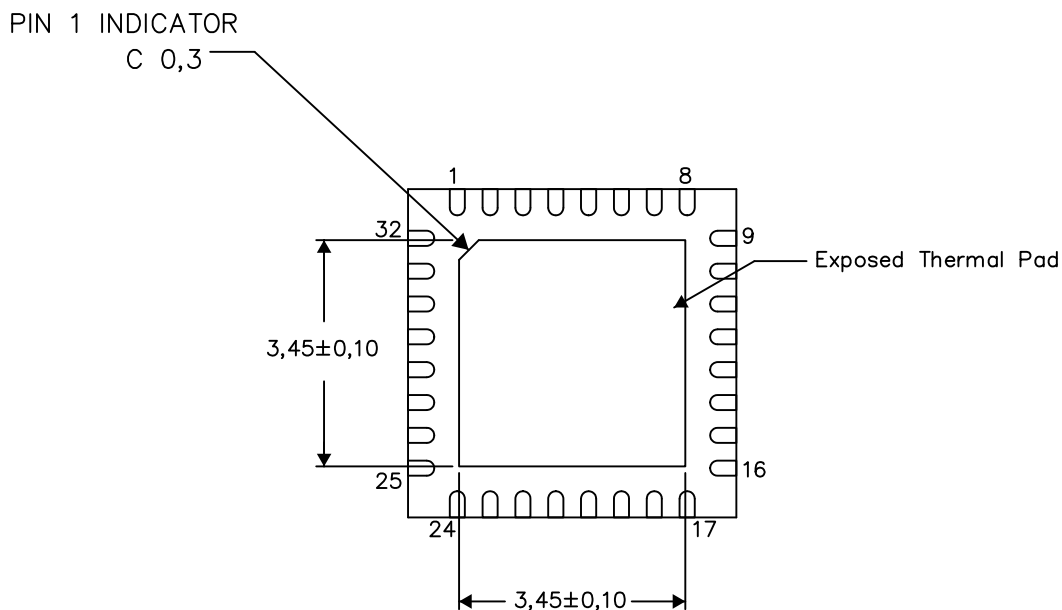
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

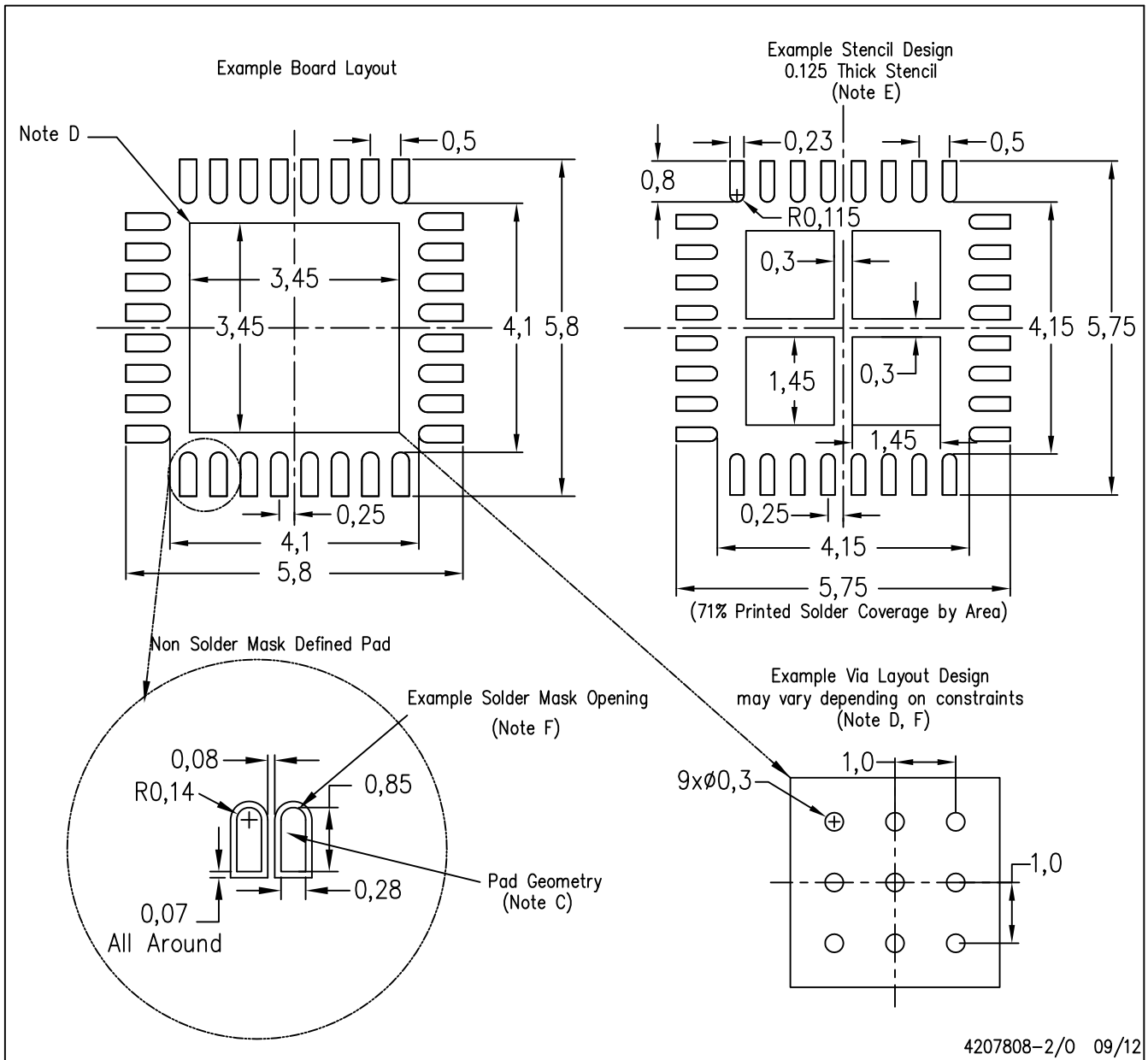
Exposed Thermal Pad Dimensions

4206356-2/W 09/12

NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4207808-2/0 09/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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