ELEC 327 S15
February 9, 2015

Lab 3 - Coding up the Mood Ring

video link: http://youtu.be/Z30bg3RnkCk

If the above link does not work, please click the following link: http://youtu.be/ib2a5W_ORRc, which will take you to my video for lab02. From there you will get into my channel, and then you should be able to see my video for lab03. Its title is "ELEC327 S15 Lab03"

1. For optimal power, which clock should you use for PWM? Ideally the PWM control frequency should be one or two orders of magnitude higher than the minimum (let's say > 5KHz). How would you set the PWM control clock to run at 6KHz?

For optimal power, you still want to use VLO, because this is the clock with the minimum oscillation frequency.

To run the PWM control clock to run at 6KHz, assuming we are using the VLO (12 kHz by default), we need to divide the clock by 2. This can be done by setting bit 6-7, input divider (IDx), to 01, which represents "divide by 2". (user guide page 378)

2. The MSP430G2553 has 3 timer modules - two are the TimerA type, and one is the Watchdog Timer (WDT+). Unlike the TimerA module, the WDT+ module cannot control PWM outputs and has less flexibility in general. However, it is very useful as a tool to trigger low level state changes. How would you configure the WDT+ module to generate periodic (maskable) interrupts?

One way to do this is to set WDT to interval timer mode, by setting the WDTTMSEL bit to 1. And when the WDTIE bit and the GIE bit are set, the WDTIFG flag requests an interrupt. Notice that we need to use interrupt vector address in interval timer mode.

3. If your `main( )` function contains an instruction which puts the CPU into a low power mode, what are the minimal interrupt service routine instructions required to wake the CPU and return function to the `main( )` function?

You achieve this in ISR by clearing the SR, system reset bit. This can be done by the command LPM3_EXIT, or _bic_SR_register_on_exit(LPM3_bits). (user guide 38, msp430g2452.h line 95, 96).

4. Assuming you use the VLO to control the WDT and TimerA modules, what is the lowest LPM which will allow your device to continue to function?

LPM3 is the lowest LPM. As long as WDT+ is not configured in watchdog mode with SMCLK as its clock source, since SMCLK is disabled in LPM3.

5. How would you turn on the ADC10 module and tell it to sample from the internal temperature sensor? What is the default voltage range for conversion?

Set bit 4, ADC10ON, in ADC10CTL0 register, to 1, thus enabling ADC10. (user guide 567)

To sample from the internal temperature sensor, set bit 12-15, INCHx, in ADC10CTL1 register, to 1010. (user guide 569)

The default voltage range for conversion is 0 to 3V. (data sheet 37 second row in table)

6. What are two ways of discovering when the ADC10 module has finished a conversion? Which method will be more efficient from a power perspective?

Method 1: ADC10BUSY bit in ADC10CTL1 register is an indication of whether there is active conversion: 0 means no operation active, and 1 means a conversion is active. By polling. (user guide 570)

Method 2: ADC10IFG bit in ADC10CTL0 is automatically reset when ADC interrupt routine request is accepted. When using interrupt, ADC conversion happens inside the interrupt. So when the flag is reset, it signals that the conversion has finished.

Method 2 is more power efficient because when using interrupt, CPU is sleeping, and only active when doing the conversion, thus saving a lot of power.

7. What is the minimum sampling period for the internal temperature sensor on the ADC10 module? Assuming that you run the ADC10 using the VLO at 12kHz, what is the maximum sampling rate for temperature?

The sampling period must be greater than 30 microsecond. (user guide 563)

According to figure 22-3 on page 552 of user guide, sampling consists of synchronization time, which is 1 clock cycle, and sampling time, which is 4 cycles in its minimum. There are, therefore, minimum 5 clock cycles for sampling. The maximum frequency is 12000/5 = 2400Hz.