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MAX77686A Datasheet

for

Samsung LSI AP (Pegasus Prime, Gaia and Hercules)

REV0.0

I Revision History

REVISION	Date	Changes	Issued by
0.0	7/6/2012	Initial Release	ChiYoung Kim

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General Description

MAX77686A is complete power management IC for the latest 3G/4G smart phones. MAX77686A contains nine high efficient buck converters, 26 LDOs to power all RF and application processor and a RTC, 3-channel 32kHz sleep clock, a backup battery charger, a manual reset, power on/off control logic, and I^2C serial interface to program individual regulator output voltages as well as on/off control for complete flexibility.

The linear regulators provide greater than 60dB PSRR and less than 45μV of output noise.
The real-time clock/calendar provides 32.768kHz buffered output, seconds, minutes, hours, day, date, month, and year information as well as two time/date-programmable alarms.

The MAX77686A features a revision 3 I^2C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL).
The MAX77686A supports SCL clock rates from 0Hz to 3.4MHz.

Features

- **Nine High Efficiency Buck Converters**
  - **1.5A for BUCK1, 5, 6, 7, 8 & 9**
  - **5A for BUCK2 & 4**
  - **2.5A for BUCK3**

26 Linear Regulators with Green Mode
  - **One 450mA NMOS LDO**
  - **One 300mA NMOS LDO**
  - **Four 150mA NMOS LDOs**
  - **Six 300mA PMOS LDOs**
  - **Fourteen 150mA PMOS LDOs**

- **Programmable voltage options for all PMOS LDOs from 0.8V to 3.95V in 50mV step**
- **Programmable voltage options for all NMOS LDOs from 0.8V to 2.375V in 25mV step**
- **Green Mode with 1uA typ for all LDOs**
- **RTC with two alarms**
- **Buffered 3-ch 32.768kHz Outputs with Low Jitter**
- **Backup battery charger and RTC**
- **Dual / single Button Manual RESET**

Applications

- **GSM, GPRS, EDGE, CDMA WCDMA & LTE Smart Phones**

Ordering Information

Die Type	Part No	Package No	Temp Range	Pin-Package
PR87B-1	MAX77686AEWE+T	W1445A5+2	-40°C to 85°C	12x12 144 Pins, 0.4mm Pitch, 5.18mm x 5.18mm
MAX77686A-6A[NOTE1]	MAX77686AQ	W1445A5+2		

Note1. MAX77686A-6A is for center trimmed samples.

Pin Configuration

TO BE UPDATED (SUBJECT TO CHANGE WITH NO NOTICE)

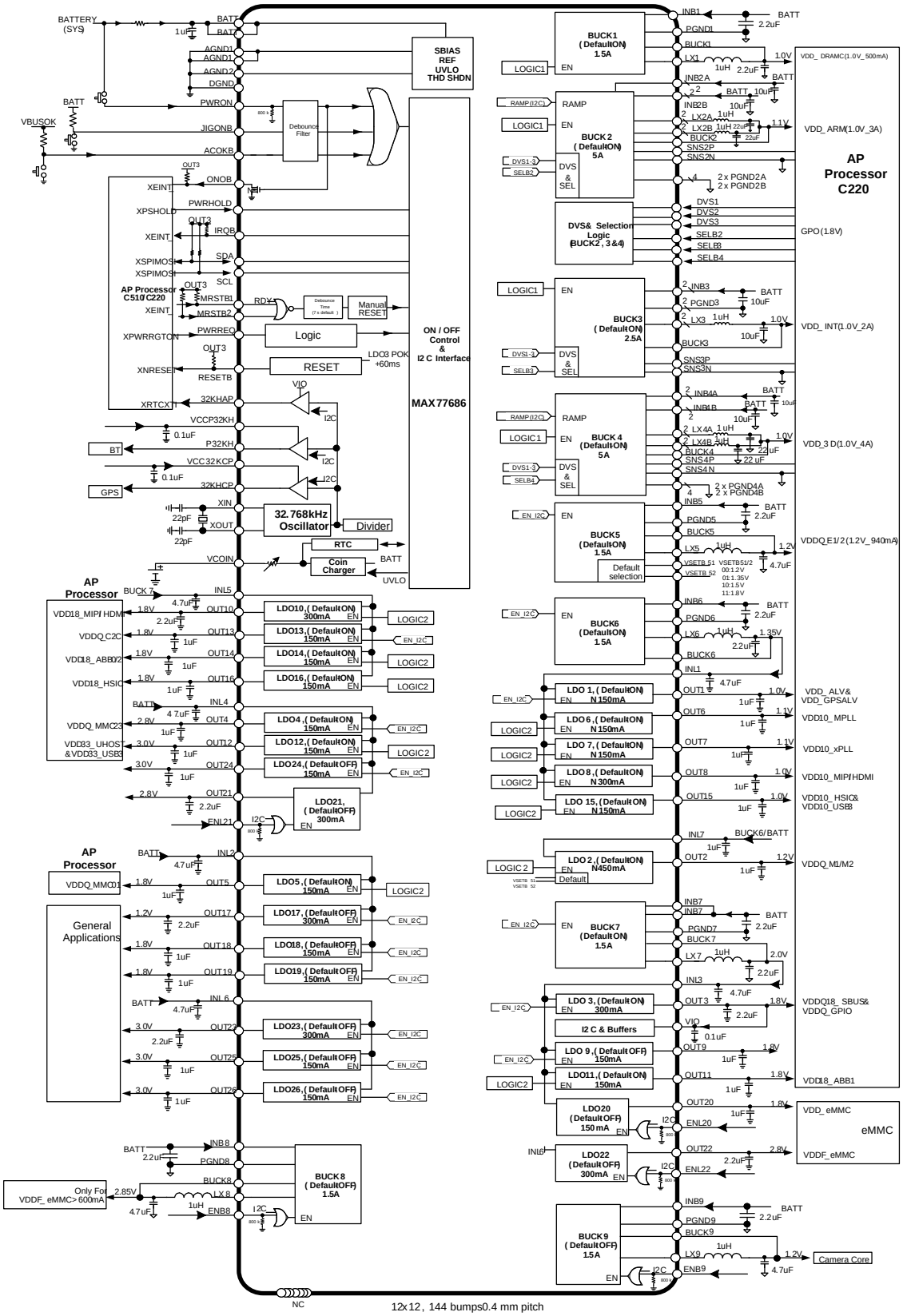
TOP-VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	
A	NC	LX6	PGND 6	INL7	INL1	INL2	INL6	INL4	INL5	INL3	PGND 7	NC	A
B	INB6	BUCK 6	ENB9	OUT2	OUT8	OUT 17	OUT 22	OUT 21	OUT 10	OUT3	INB7	LX7	B
C	PGND 1	BUCK 1	ENB8	OUT7	OUT1	OUT5	OUT 25	OUT4	OUT 13	OUT9	INB7	PGND 5	C
D	LX1	INB1	ENL20	OUT 15	OUT6	OUT 18	OUT 23	OUT 12	OUT 14	OUT 11	BUCK 7	LX5	D
E	PGND 4A	PGND 4A	ENL21	ENL22	OUT 26	OUT 19	ONOB	OUT 24	OUT 16	OUT 20	BUCK 5	INB5	E
F	LX4A	LX4A	BUCK 4	AC OKB	RE SETB	IRQB	MR STB1	DVS1	DGND	AGND 2	AGND 1	AGND 1	F
G	INB4A	INB4A	SNS 4P	JIG ONB	PWR ON	PWR HOLD	MR STB2	DVS2	VIO	BUCK 3	PGND 3	PGND 3	G
H	INB4B	INB4B	SNS 4N	VSET B51	VSET B52	SELB2	SELB3	DVS3	PWR REQ	SNS 3P	LX3	LX3	H
J	LX4B	LX4B	BUCK 9	VCC 32KCP	P32 KH	32KH AP	SELB4	SCL	SDA	SNS 3N	INB3	INB3	J
K	PGND 4B	PGND 4B	NC	32KH CP	VCCP 32KH	V COIN	NC	SNS 2N	SNS 2P	BUCK 2	NC	PGND 8	K
L	PGND 9	INB9	BATT	XOUT	PGND 2B	LX2B	INB2B	INB2A	LX2A	PGND 2A	BUCK 8	LX8	L
M	NC	LX9	BATT	XIN	PGND 2B	LX2B	INB2B	INB2A	LX2A	PGND 2A	INB8	NC	M
	1	2	3	4	5	6	7	8	9	10	11	12	

12x12, 144 Bumps, 0.4mm Pitch

Typical Operation Circuit

MAX77686A Application Circuit with Samsung LSI Chipset, C220



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Absolute Maximum Ratings

BATT, INB1, INB2, INB3, INB4, INB5, INB6, INB7, INB8, INB9, INL1, INL2, INL3, INL4, INL5, INL6 , INL7, VCOIN, VCCP32KH, VCC32KCP, VIO to AGND1.....-0.3V to +6V

INB1, INB2, INB3, INB4, INB5, INB6, INB7, INB8, INB9, JIGONB, PWRON, ACOKB, ENL20, ENL21 , ENL22, ENB8, ENB9, VSETB51, VSETB52 to AGND1.....-0.3V to (V_{BATT}+0.3V)

PWRHOLD, MRSTB1, MRSTB2, PWRREQ, DVS1-3, SELB2, SELB3, SELB4, RESETB, IRQB , 32KHAP, ONOB, SDA, SCL to AGND1.....-0.3V to (V_{VIO} + 0.3V)

BUCK1, LX1 to PGND1.....-0.3V to (V_{INB1} + 0.3V)
BUCK2, LX2A, LX2B, SNS2P to PGND2A/B.....-0.3V to ($V_{INB2\_}$ + 0.3V)
BUCK3, LX3, SNS3P to PGND3.....-0.3V to (V_{INB3} + 0.3V)
BUCK4, LX4A, LX4B, SNS4P to PGND4A/B.....-0.3V to ($V_{INB4\_}$ + 0.3V)
BUCK5, LX5 to PGND5.....-0.3V to (V_{INB5} + 0.3V)
BUCK6, LX6 to PGND6.....-0.3V to (V_{INB6} + 0.3V)
BUCK7, LX7 to PGND7.....-0.3V to (V_{INB7} + 0.3V)
BUCK8, LX8 to PGND8.....-0.3V to (V_{INB8} + 0.3V)
BUCK9, LX9 to PGND9.....-0.3V to (V_{INB9} + 0.3V)

OUT1, OUT6, OUT7, OUT8, OUT15 to AGND1 .....-0.3V to (V_{INL1}+ 0.3V)
OUT5, OUT17 OUT18, OUT19 to AGND1.....-0.3V to (V_{INL2}+ 0.3V)
OUT3, OUT9, OUT11, OUT20 to AGND1.....-0.3V to (V_{INL3}+ 0.3V)
OUT4, OUT12, OUT21, OUT24 to AGND1.....-0.3V to (V_{INL4}+ 0.3V)
OUT10, OUT13, OUT14, OUT16 to AGND1.....-0.3V to (V_{INL5}+ 0.3V)
OUT22, OUT23, OUT25, OUT26 to AGND1.....-0.3V to (V_{INL6}+ 0.3V)
OUT2 to AGND1.....-0.3V to (V_{INL7}+ 0.3V)

XIN, XOUT to AGND1 -0.3V to 1.8V
P32KH to AGND1.....-0.3V to ($V_{VCCP32KH}$+ 0.3V)
32KHCP to AGND1 .....-0.3V to ($V_{VCC32KCP}$+ 0.3V)

PGND1-9, AGND2, DGND, SNS2N, SNS3N, SNS4N to AGND1.....-0.3V to +0.3V

LX1, 5, 6, 7, 8 & 9 Continuous RMS Current (Note1) 1.5A
LX2A, LX2B, LX3, LX4A, LX4B Continuous RMS Current (Note1)..... 2.5A

Continuous Power Dissipation (T_A = 70◦C)
(Derate 33.3mW/°C above +70 °C)..... .....2670mW
Operating Temperature.....-40◦C to +85◦C
Junction Temperature.....+150◦C
Storage Temperature Range.....-65◦C to +150◦C
Soldering Temperature (reflow).....+260◦C

Note 1: LX_ has internal clamp diodes to PGND_ and INB_. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

General Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT}=VIN_= +3.7V, VIO=V_{OUT3}=1.8V, $C_{BATT+}\Sigma_{IN\_}$=47µF, T_A=-40°C to +85°C

EC#	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	TEST#
	Shutdown Supply Current	I_{SHDN}	V_{BATT}= V_{IN} = 4.2V, Backup battery is fully charged, All other functions OFF.		6	20	µA	
	No Load Supply Current 1	I_{NO_LOAD1}	V_{BATT}= $V_{IN\_}$ = 3.7V, BUCK1-7=ON (BUCK2, 3&4 in green mode), BUCK8-9=OFF, LDO1-16=ON in low power mode (except LDO9), other LDOs=OFF, ENL20=ENL21=ENL22=ENB8=ENB9=LOW, other functions off, Backup battery is fully charged.		180		µA	
	No Load Supply Current 2	I_{NO_LOAD1}	V_{BATT}= $V_{IN\_}$ = 3.7V, BUCK1-7=ON (BUCK2, 3&4 in green mode), BUCK8-9=OFF, LDO1-16=ON (except LDO9)in normal mode, other LDOs=OFF,other functions off, ENL20=ENL21=ENL22=ENB8=ENB9=LOW, Backup battery is fully charged.		490		µA	
BATT UNDERVOLTAGE LOCK-OUT								
	Battery Undervoltage Lockout Threshold	V_{UVLO_R}	V_{BATT} rising	-5%	3.0	+5%	V	
		V_{UVLO_F}	V_{BATT} falling		2.25		V	
THERMAL SHUTDOWN								
	Threshold, T_{SHDN}	T_{JSHDN}	T_J Rising, 15°C hysteresis		165		°C	
	Thermal Interrupt 1	T_{J120}	T_J Rising, 15°C hysteresis		120		°C	
	Thermal Interrupt 2	T_{J140}	T_J Rising, 15°C hysteresis		140		°C	
LOGIC AND CONTROL INPUTS								
	Input Low Level	V_{IL}	PWRON, JIGONB, ACOKB, PWRHOLD, MRSTB1, MRSTB2, ENL20, ENL21, ENL22, ENB8, ENB9, DVS1-3, SELB2-4, PWRREQ, VSETB51, VSETB52, T_A=25°C			0.4	V	
	Input High Level	V_{IH}	PWRON, JIGONB, ACOKB, PWRHOLD, MRSTB1, MRSTB2, ENL20, ENL21, ENL22, ENB8, ENB9, DVS1-3, SELB2-4, PWRREQ, VSETB51, VSETB52, T_A=25°C	1.40			V	

EC#	PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	TEST#
	Logic Input Leakage Current	I_{LEAK}	VSETB51, VSETB52, ACOKB, JIGONB (0V < V_{BATT} < 5.5V)	T_A= 25°C	-1		1	µA	
			PWRHOLD, MRSTB1, MRSTB2, PWRREQ, DVS1-3, SELB2-4 (0V<V_{VIO} <2.0V)	T_A= 85°C		0.1		µA	
	ONOB, RESETB, IRQB Output Low Voltage	V_{OL}	I_{SINK}=1mA				0.4	V	
	ONOB, RESETB, IRQB Output High Leakage	I_{OZH}	V_{VIO}=5.5V	T_A=25°C	-1	0	1	µA	
				T_A=85°C		0.1			
INTERNAL PULL-DOWN RESISTANCE									
	PWRON, ENL20, ENL21, ENL22, ENB8, ENB9	R_{PD}	Pull-down resistor to AGND1		400	800	1600	kΩ	
TIMER									
	Power-On Debounce filter timer	T_{DEB_PON}	JIGONB, PWRON, ACOKB			16		ms	
	Interrupt Debounce filter timer	T_{DEB_INT}	PWRONR, PWRONF, JIGONBR, JIGONBF, ACOKBR, ACOKBF			16		ms	
	SMPL Timer (Sudden Momentary Power Loss)	T_{SMPL}	SMPLT=00			0.5		sec	
			SMPLT =01(Default)			1.0			
			SMPLT =10			1.5			
			SMPLT =11			2.0			
	RESETB Low Holding Time on WTSR		Time to hold RESETB=LOW			58.6		ms	
	WTSR Reset Timer (Time to Keep the default supplies ON until WTSR reset timer expires)		WTSRT =00			250		ms	
			WTSRT =01			500			
			WTSRT =10			750			
			WTSRT =11(Default)			1000			
	ONKEY1S Timer	T_{ON_1SEC}	If PWRON stays longer than 1s, Interrupt will trigger			1000		ms	
	One Shot Timer on ACOKB	$T_{ONESHOT}$	From falling edge of ACOKB until timer is complete.			1000		ms	

I²C Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT}=3.7V, V_{VIO}= V_{OUT3}=1.8V, T_A=-40°C to +85°C, typical values are at T_A=+25°C. (Note 1)

EC#	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	TEST#
Power Supply								
	VIO Voltage	V_{VIO}		1.7		3.6	V	
SDA and SCL I/O Stages								
	SCL, SDA Input High Voltage	V_{IH}		0.7* V_{VIO}			V	
	SCL, SDA Input Low Voltage	V_{IL}				0.3* V_{VIO}	V	
	SCL, SDA Input Hysteresis	Vhys			0.05* V_{VIO}		V	
	SCL, SDA Input Current	I_I	V_{VIO} =3.6V	-10		+10	µA	
	SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V	
	SCL, SDA Pin Capacitance	C_i			10		pF	
	Output Fall Time from V_{VIO} to 0.3* V_{VIO}	t_{OF}				120	ns	
I²C Compatible Interface Timing for Standard, Fast, and Fast-mode Plus (Note 2)								
	Clock Frequency	f_{SCL}				1000	kHz	
	Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs	
	CLK Low Period	t_{LOW}		0.5			µs	
	CLK High Period	t_{HIGH}		0.26			µs	
	Set-Up Time Repeated START Condition	$t_{SU;STA}$		0.26			µs	
	DATA Hold Time	$t_{HD:DAT}$		0			µs	
	DATA Set-Up time	$t_{SU;DAT}$		50			ns	
	Set-Up Time for STOP Condition	$t_{SU;STO}$		0.26			µs	
	Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs	
	Capacitive Load for Each Bus Line	C_B				550	pF	
	Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter				50		ns	

Note 1. Limits are 100% production tested at T_A=+25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 2. Guaranteed by design. Not production tested.

Operating conditions (unless otherwise specified) V_{BATT}=3.7V, V_{VIO}= V_{OUT3}=1.8V, T_A=-40°C to +85°C, typical values are at T_A=+25°C. (Note 1, Note 2)

EC#	PARAMETER	SYMBOL	CONDITIONS	C_B=100pF		C_B=400pF		UNIT	TEST#
				Min	Max	Min	Max		
I^2C Compatible Interface Timing for HS-Mode									
	Clock Frequency	f_{SCL}			3.4		1.7	MHz	
	Set-Up Time Repeated START Condition	$t_{SU;STA}$		160		160		ns	
	Hold Time (Repeated) START Condition	$t_{HD;STA}$		160		160		ns	
	CLK Low Period	t_{LOW}		160		320		ns	
	CLK High Period	t_{HIGH}		60		120		ns	
	DATA Set-Up time	$t_{SU;DAT}$		10		10		ns	
	DATA Hold Time	$t_{HD;DAT}$		0	70	0	150	ns	
	SCL Rise Time (Note 2)	t_{RCL}		10	40	20	80	ns	
	Rise Time of SCL Signal after a Repeated START condition and after an Acknowledge bit (Note2)	t_{rCL1}		10	80	20	80	ns	
	SCL Fall Time (Note 2)	t_{fCL}		10	40	20	80	ns	
	SDA Rise Time (Note 2)	t_{rDA}		10	80	20	160	ns	
	SDA Fall Time (Note 2)	tf_{DA}		10	80	20	160	ns	
	Set-Up Time for STOP Condition	$t_{SU;STO}$		160		160		ns	
	Capacitive Load for Each Bus Line	C_B			100		400	pF	
	Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		10	ns	

Note 1. Limits are 100% production tested at T_A=+25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 2. Guaranteed by design. Not production tested.

Buck Converter1 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT}=$V_{INB\_}$= +3.6V, $C_{BUCK\_}$ =4.7µF, L_=1µH, T_A =-40°C to +85°C (Note 2)

EC#	PARAMETER	CONDITIONS		MIN	TYP	MAX	Unit	TEST#
	Input Voltage Range	Guaranteed by Output Voltage Accuracy and supply current		2.7		5.5	V	
	Shutdown Current (Note 1)	Regulator Disabled, $V_{INB\_}$=4.8V			0.1		µA	
	Ground Current (Note 1)	I_{LOAD} =0mA, no switching, Regulator Enabled			25		µA	
	Default output Voltage	in continuous conductionmode		-3%	1.00	+3%	V	
	Programmable Output Voltage	I_{Load}=0mA, Programmable in 12.5mV Steps		0.75		1.5375	V	
	Maximum Output Current (Note 1)			1500			mA	
	Current Limit		PFET Switch	1800	2750	3700	mA	
			NFET Rectifier	1300	2250	3200		
	On-Resistance		PFET Switch		0.15		Ω	
			NFET Rectifier		0.08			
	N-Channel Zero-Crossing Threshold				50		mA	
	Startup Time	V_{OUT}=1.0V			40		µs	
	Minimum On-and Off-Times		T_{ON}		60		ns	
			T_{OFF}		60			
	LX Active Resistance	I2C programmable. Default ON, Resistance from LX_ to PGND_			1		kΩ	
	Output Load Regulation (Voltage Positioning)	R_L = Inductor DC resistance			R_L/4		V/A	
	Output Line Regulation	V_{INB} = 3.0V to 5.5V			0.3		%	
	LX_ Leakage Current	LX_=PGND_ or INB_	T_A=25℃	-1		1	µA	
			T_A=85℃		0.1			

Note 1: Design guidance only, not tested during final test.

Note 2. Limits are 100% production tested at T_A=+25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Buck Converter 2 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT}=V_{INB2\_}$ = 3.6V, C_{BUCK2} =44µF, V_{BUCK2}=1.1V, $L_{2A}=L_{2B}$= 1µH, T_A =-40°C to +85°C, Typical specifications are at T_A = +25°C (Note 2)

EC#	PARAMETER	CONDITIONS	MIN	TYP	MAX	Unit	TEST#
	Default Voltage	FPWM, T_A=25°C, (Note4)	-1%	1.1	+1%	V	
	Input Voltage Range	BATT and INB2A/B must be connected together.	2.6		5.5	V	
	Output Voltage Accuracy	V_{BUCK2}=1.1V, No load at PWM mode, Normal Power Mode, T_A=25°C (Note4).	-1%	0	+1%	%	
		V_{BUCK2} = 0.8V and 1.5V, No load at PWM mode, Normal Power Mode, T_A=25°C (Note4).	-1.5%	0	+1.5%		
		V_{BUCK2}= 0.8V and 1.5V, accuracy includes static variations in line, load, and temperature PWM mode, Normal Power Mode	- 2.5		+ 2.5		
		Low Power Mode I_{LOAD} =0mA to 5mA, Default output voltage.		± 3			
	Load Regulation	0-2A, Input voltage operating range, PWM mode		0.125		%/A	
	Line Regulation	V_{INB2} = 2.6V to 5V		0.2		%/V	
	Load transient FPWM (Note 1)	FPWM Mode, VINB operating range, V_{OUT} = 1.1V, Load steps between 0.2 to 1.2A in 20us, 22µF x 2, 1µH x2		± 40		mV	
	Load transient PFM enabled (Note 1)	PFM Mode, VIN operating range, Load steps between 0 and 400mA in 30ns.		± 40		mV	
	Shutdown Supply Current (Note 1)			0.1		µA	
	Supply Quiescent Current (Note 1)	No Switching, Remote Output Voltage Sensing Off		32	50	µA	
		Switching, No Load, Skip Mode		40			
		Low- Power Mode, V_{OUT} = 1.8V		10	16		
		Additional Current Consumed by BUCK2 Remote Output Voltage Sense Circuitry total in normal mode is $I_Q=I_{Q\ BUCK2}+I_{Q\ SNS\ EN0}$ — ROVS_EN_B2=1		10			
		ROVS_EN_B2=0		0.1			
		Switching, No Load, Forced PWM Mode		20		mA	
	Programmable Output Voltage	Programmable in 12.5mV Steps, 8 bits	0.6		3.7875	V	
	Maximum Output Current	Normal Operation	5000			mA	
		Low-Power Mode	5				
	Switching Frequency	Normal Operation	2.25	2.5	2.75	MHz	
	Peak Current Limit	FPWM Mode, Each for I_{LX2A} or I_{LX2B}	2900	3750	4800	mA	
	Valley Current Limit	FPWM Mode, Each for I_{LX2A} or I_{LX2B}	2500	3125		mA	
	Negative Current limit	FPWM Mode, Each for I_{LX2A} or I_{LX2B}		1000		mA	
	On-Resistance	INB_=3.6V, PFET Switch		60		mΩ	

EC#	PARAMETER	CONDITIONS		MIN	TYP	MAX	Unit	TEST#
		INB_=3.6V, NFET Switch			50		mΩ	
	NMOS Zero-Crossing Threshold	Skip Mode			20		mA	
	V_{BUCK2} Ripple in Skip Mode (Note 3)	No Load, C_{OUT}=22uF x 2			40		mV_{P-P}	
	V_{BUCK2} Ripple in PWM Mode	No Load			10		mV_{P-P}	
	LX2 Leakage Current	LX2_ = $V_{INB\_}$ or PGND2_	T_A=25°C		0.1	±1	μA	
			T_A=85°C		1		μA	
	BUCK2 Active Discharge	Output Disabled nAD_EN_B2=0, resistance from BUCK2 to PGND2A/B			100		Ω	
	Output Capacitance Required for Stability (Note 1)	0A< I_{BUCK2}< 5A, MAX ESR=20mΩ		30	44		μF	
	OUTPUT Inductor	MAX DCR=100mΩ			1.0		μH	
	Turn-On Time	Time from the enable signal to the output starting to increase			22		μs	
	Turn Off Time	After the regulator is disabled; The output voltage will discharge based on Load and C_{OUT}. To ensure fast discharge times enable the active discharge resistor			0.1		μs	
	Dynamic Change Ramp Rate on BUCK2 (Note 1)	Dynamic Voltage Change	RAMP:00		15		mV/μs	
			RAMP:01 (Default)		30			
			RAMP:10		60			
			RAMP:11		disabled			
	Soft-Start Slew Rate (Note1)				25		mV/μs	
	Remote Sense Compensation Range	Voltage drop through power and ground plane, $V_{RSR}=V_{BUCK2}-(V_{SNSP}-V_{SNSN})$				200	mV	

Note 1. Design guidance only, Guaranteed by design. Not production tested.
Note 2. Limits are 100% production tested at T_A=+25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.
Note 3. Skip mode output voltage ripple decreases as the output capaciatance increases. Typically a system's point-of-load capacitance will contribute to the step-down regulators local output capacitance to decrease the overall skip-mode output voltage ripple.
Note 4. Accuracyt trimmed in production. Guaranteed by design.

Buck Converter 3 Electrical Characteristics

V_{BATT}=V_{INB3}= 3.6V, C_{BUCK3} = 22μF, V_{BUCK3}=1.0V, L_3= 1μH, T_A =-40°C to +85°C, Typical specifications are at T_A = +25°C (Note 2)

EC#	PARAMETER	CONDITIONS	MIN	TYP	MAX	Unit	TEST#
	Default Voltage	FPWM,T_A=25°C (Note4)	-1%	1.00	+1%	V	
	Input Voltage Range	BATT and INB3 must be connected together.	2.6		5.5	V	
	Output Voltage Accuracy	V_{BUCK3}=1.0V, No load at PWM mode, Normal Power Mode, T_A=25°C (Note4)	-1%	0	+1%	%	
		V_{BUCK3} = 0.8Vand 1.5V, , No load at PWM mode Normal Power Mode, T_A=25°C (Note4)	-1.5%	0	+1.5%		
		V_{BUCK3} =0.8V and 1.5V, accuracy includes static variations in line, load, and temperature PWM mode, Normal Power Mode	-2.5		+2.5		
		Low Power Mode I_{LOAD} =0mA to 5mA, Default output voltage.		± 3			
	Load Regulation	0-1A, Input voltage operating range, PWM mode		0.125		%/A	
	Output Line Regulation	$V_{INB3\_}$= 2.6V to 5V		0.2		%/V	
	Load transient FPWM (Note 1)	FPWM Mode, VINB operating range, V_{BUCK3} = 1.0V, Load steps between 0.1 to 0.6A in 20us, 22μF, 1μH		± 40		mV	
	Load transient PFM enabled (Note 1)	PFM Mode, VIN operating range, Load steps between 0 and 200mA in 30ns.		± 40		mV	
	Shutdown Supply Current (Note 1)			0.1		μA	
	Supply Quiescent Current (Note 1)	No Switching, Remote Output Voltage Sensing Off		16	25	μA	
		Switching, No Load, Skip Mode		20			
		Low- Power Mode, V_{BUCK3} = 1.8V		5	8		
		Additional Current Consumed by BUCK3 Remote Output Voltage Sense Circuitry total in normal mode is I_Q=$I_{Q\ BUCK3}$+$I_{Q\ SNS\ EN0}$ — ROVS_EN_B3=1		10			
		ROVS_EN_B3=0		0.1			
		Switching, No Load, Forced PWM Mode		10		mA	
	Programmable Output Voltage	Programmable in 12.5mV Steps, 8 bits	0.6		3.7875	V	
	Maximum Output Current	Normal Operation	2500			mA	
		Low-Power Mode	5				
	Switching Frequency	Normal Operation	2.25	2.5	2.75	MHz	
	Peak Current Limit	FPWM Mode	2900	3750	4800	mA	
	Valley Current Limit	FPWM Mode	2500	3125		mA	

EC#	PARAMETER	CONDITIONS		MIN	TYP	MAX	Unit	TEST#
	Negative Current limit	FPWM Mode			1000		mA	
	On-Resistance	INB3=3.6V, PFET Switch			60		mΩ	
		INB3=3.6V, NFET Switch			50		mΩ	
	NMOS Zero-Crossing Threshold	Skip Mode			20		mA	
	V_{BUCK3} Ripple in Skip Mode (Note 3)	No Load, C_{OUT}=22uF			40		mV_{P-P}	
	V_{BUCK3} Ripple in PWM Mode	No Load			10		mV_{P-P}	
	LX3 Leakage Current	LX3 = V_{INB3} or PGND3	T_A=25°C		0.1	±1	μA	
			T_A=85°C		1		μA	
	BUCK3 Active Discharge	Output Disabled nAD_EN_B3=0, resistance from BUCK3 to PGND3			100		Ω	
	Output Capacitance Required for Stability (Note 1)	0A< I_{BUCK3}< 2.5A, MAX ESR=20mΩ		15	22		μF	
	OUTPUT Inductor	MAX DCR=100mΩ			1.0		μH	
	Turn-On Time	Time from the enable signal to the output starting to increase			22		μs	
	Turn Off Time	After the regulator is disabled; The output voltage will discharge based on Load and C_{OUT}. To ensure fast discharge times enable the active discharge resistor			0.1		μs	
	Dynamic Change Ramp Rate on BUCK3 (Note 1)	Dynamic Voltage Change	RAMP:00		15		mV/μs	
			RAMP:01 (Default)		30			
			RAMP:10		60			
			RAMP:11		disabled			
	Soft-Start Slew Rate (Note1)				25		mV/μs	
	Remote Sense Compensation Range	Voltage drop through power and ground plane, $V_{RSR}=V_{BUCK3}-(V_{SNS3P}-V_{SNS3N})$				200	mV	

Note 1. Design guidance only,Guaranteed by design. Not production tested.
Note 2. Limits are 100% production tested at T_A=+25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.
Note 3. Skip mode output voltage ripple decreases as the output capaciatance increases. Typically a system's point-of-load capacitance will contribute to the step-down regulators local output capacitance to decrease the overall skip-mode output voltage ripple.
Note 4. Accuracyt trimmed in production. Guaranteed by design.

Buck Converter 4 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT}=V_{INB4\_}$ = 3.6V, C_{BUCK4} =44µF, V_{BUCK4}=1.0V, $L_{4A}=L_{4B}$= 1µH, T_A =-40°C to +85°C, Typical specifications are at T_A = +25°C (Note 2)

EC#	PARAMETER	CONDITIONS	MIN	TYP	MAX	Unit	TEST#
	Default Voltage	FPWM, T_A=25°C (Note4)	-1%	1.00	+1%	V	
	Input Voltage Range	AVS, INB4A/B must be connected together.	2.6		5.5	V	
	Output Voltage Accuracy	V_{BUCK4}=1.0V, No load at PWM mode, Normal Power Mode, T_A=25°C (Note4)	-1%	0	+1%	%	
		V_{BUCK4} =0.8V and 1.5V, No load at PWM mode Normal Power Mode	-1.5%	0	+1.5%		
		V_{BUCK4} = 0.8V and 1.5V, accuracy includes static variations in line, load, and temperature, PWM mode, Normal Power Mode	-2.5		+2.5		
		Low Power Mode I_{LOAD} =0mA to 5mA, Default output voltage.		± 3			
	Load Regulation	0-2A, Input voltage operating range, PWM mode		0.125		%/A	
	Line Regulation	V_{INB4} = 2.6V to 5V		0.2		%/V	
	Load transient FPWM (Note 1)	FPWM Mode, VINB operating range, V_{OUT} = 1.0V, Load steps between 0.2 to 1.2A in 20us, 22µF x 2, 1µH x2		± 40		mV	
	Load transient PFM enabled (Note 1)	PFM Mode, VIN operating range, Load steps between 0 and 400mA in 30ns.		± 40		mV	
	Shutdown Supply Current (Note 1)			0.1		µA	
	Supply Quiescent Current (Note 1)	No Switching, Remote Output Voltage Sensing Off		32	50	µA	
		Switching, No Load, Skip Mode		40			
		Low- Power Mode, V_{OUT} = 1.8V		10	16		
		Additional Current Consumed by BUCK4 Remote Output Voltage Sense Circuitry total in normal mode is $I_Q=I_{Q\ BUCK4}+I_{Q\ SNS\ EN0}$ — ROVS_EN_B4 =1		10			
		ROVS_EN_B4 =0		0.1			
		Switching, No Load, Forced PWM Mode		20		mA	
	Programmable Output Voltage	Programmable in 12.5mV Steps, 8 bits	0.6		3.7875	V	
	Maximum Output Current	Normal Operation	5000			mA	
		Low-Power Mode	5				
	Switching Frequency	Normal Operation	2.25	2.5	2.75	MHz	
	Peak Current Limit	FPWM Mode, Each for I_{LX4A} or I_{LX4B}	2900	3750	4800	mA	
	Valley Current Limit	FPWM Mode, Each for I_{LX4A} or I_{LX4B}	2500	3125		mA	
	Negative Current limit	FPWM Mode, Each for I_{LX4A} or I_{LX4B}		1000		mA	
	On-Resistance	INB_=3.6V, PFET Switch		60		mΩ	

EC#	PARAMETER	CONDITIONS		MIN	TYP	MAX	Unit	TEST#
		INB_=3.6V, NFET Switch			50		mΩ	
	NMOS Zero-Crossing Threshold	Skip Mode			20		mA	
	V_{BUCK4} Ripple in Skip Mode (Note 3)	No Load, C_{OUT}=22uF x 2			40		mV_{P-P}	
	V_{BUCK4} Ripple in PWM Mode	No Load			10		mV_{P-P}	
	LX4 Leakage Current	LX4_ = $V_{INB\_}$ or PGND4_	T_A=25°C		0.1	±1	μA	
			T_A=85°C		1		μA	
	BUCK4 Active Discharge	Output Disabled nAD_EN_B4=0, resistance from BUCK4 to PGND4_			100		Ω	
	Output Capacitance Required for Stability (Note 1)	0A< I_{BUCK4}< 5A, MAX ESR=20mΩ		30	44		μF	
	OUTPUT Inductor	MAX DCR=100mΩ			1.0		μH	
	Turn-On Time	Time from the enable signal to the output starting to increase			22		μs	
	Turn Off Time	After the regulator is disabled; The output voltage will discharge based on Load and C_{OUT}. To ensure fast discharge times enable the active discharge resistor			0.1		μs	
	Dynamic Change Ramp Rate on BUCK4 (Note 1)	Dynamic Voltage Change	RAMP:00		15		mV/μs	
			RAMP:01 (Default)		30			
			RAMP:10		60			
			RAMP:11		disabled			
	Soft-Start Slew Rate (Note1)				25		mV/μs	
	Remote Sense Compensation Range	Voltage drop through power and ground plane, $V_{RSR}=V_{BUCK4}-(V_{SNSP}-V_{SNSN})$				200	mV	

Note 1. Design guidance only,Guaranteed by design. Not production tested.
Note 2. Limits are 100% production tested at T_A=+25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.
Note 3. Skip mode output voltage ripple decreases as the output capaciatance increases. Typically a system's point-of-load capacitance will contribute to the step-down regulators local output capacitance to decrease the overall skip-mode output voltage ripple.
Note 4. Accuracyt trimmed in production. Guaranteed by design.

Buck Converter 5 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT}=$V_{INB\_}$= +3.6V, $C_{BUCK\_}$ =4.7µF, L_=1µH, T_A =-40°C to +85°C (Note 2)

EC#	PARAMETER	CONDITIONS			MIN	TYP	MAX	Unit	TEST #
	Input Voltage Range	Guaranteed by Output Voltage Accuracy and supply current			2.7		5.5	V	
	Shutdown Current (Note 1)	Regulator Disabled, $V_{INB\_}$=4.8V				0.1		µA	
	Ground Current (Note 1)	I_{LOAD} =0mA, no switching, Regulator Enabled				25		µA	
	Default output Voltage	in continuous conduction mode	VSETB51 & VSETB52	00	-3%	1.20	+3%	V	
				01	-3%	1.35	+3%		
				10	-3%	1.50	+3%		
				11	-3%	1.80	+3%		
	Programmable Output Voltage	I_{Load}=0mA, Programmable in 50mV Steps			0.75		3.90	V	
	Maximum Output Current (Note 1)				1500			mA	
	Current Limit		PFET Switch		1800	2750	3700	mA	
			NFET Rectifier		1300	2250	3200		
	On-Resistance		PFET Switch			0.15		Ω	
			NFET Rectifier			0.08			
	N-Channel Zero-Crossing Threshold					50		mA	
	Startup Time	V_{OUT}=1.0V				40		µs	
	Minimum On-and Off-Times		T_{ON}			60		ns	
			T_{OFF}			60			
	LX Active Resistance	I2C programmable. Default ON, Resistance from LX_ to PGND_				1		kΩ	
	Output Load Regulation (Voltage Positioning)	R_L = Inductor DC resistance				R_L/4		V/A	
	Output Line Regulation	$V_{INB\_}$ = 3.0V to 5.5V				0.3		%	
	LX_ Leakage Current	LX_=PGND_ or INB_	T_A=25℃		-1		1	µA	
			T_A=85℃			0.1			

Note 1: Design guidance only, not tested during final test.

Note 2. Limits are 100% production tested at T_A=+25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Buck Converter 6 Electrical Characteristics

Operating conditions (unless otherwise specified) $V_{BATT}=V_{INB\_}$= +3.6V, $C_{BUCK\_}$ =4.7µF, L_=1µH, T_A =-40°C to +85°C (Note 2)

EC#	PARAMETER	CONDITIONS		MIN	TYP	MAX	Unit	TEST #
	Input Voltage Range	Guaranteed by Output Voltage Accuracy and supply current		2.7		5.5	V	
	Shutdown Current (Note 1)	Regulator Disabled, $V_{INB\_}$=4.8V			0.1		µA	
	Ground Current (Note 1)	I_{LOAD} =0mA, no switching, Regulator Enabled			25		µA	
	Default output Voltage	in continuous conductionmode		-3%	1.35	+3%	V	
	Programmable Output Voltage	I_{Load}=0mA, Programmable in 50mV Steps		0.75		3.90	V	
	Maximum Output Current (Note 1)			1500			mA	
	Current Limit		PFET Switch	1800	2750	3700	mA	
			NFET Rectifier	1300	2250	3200		
	On-Resistance		PFET Switch		0.15		Ω	
			NFET Rectifier		0.08			
	N-Channel Zero-Crossing Threshold				50		mA	
	Startup Time	V_{OUT}=1.0V			40		µs	
	Minimum On-and Off-Times		T_{ON}		60		ns	
			T_{OFF}		60			
	LX Active Resistance	I2C programmable. Default ON, Resistance from LX_ to PGND_			1		kΩ	
	Output Load Regulation (Voltage Positioning)	R_L = Inductor DC resistance			R_L/4		V/A	
	Output Line Regulation	V_{INB} = 3.0V to 5.5V			0.3		%	
	LX_ Leakage Current	LX_=PGND_ or INB_	T_A=25℃	-1		1	µA	
			T_A=85℃		0.1			

Note 1: Design guidance only, not tested during final test.

Note 2. Limits are 100% production tested at T_A=+25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Buck Converter 7 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT}=$V_{INB\_}$= +3.6V, $C_{BUCK\_}$ =4.7µF, L_=1µH, T_A =-40°C to +85°C (Note 2)

EC#	PARAMETER	CONDITIONS		MIN	TYP	MAX	Unit	TEST #
	Input Voltage Range	Guaranteed by Output Voltage Accuracy and supply current		2.7		5.5	V	
	Shutdown Current (Note 1)	Regulator Disabled, $V_{INB\_}$=4.8V			0.1		µA	
	Ground Current (Note 1)	I_{LOAD} =0mA, no switching, Regulator Enabled			25		µA	
	Default output Voltage	in continuous conductionmode		-3%	2.00	+3%	V	
	Programmable Output Voltage	I_{Load}=0mA, Programmable in 50mV Steps		0.75		3.90	V	
	Maximum Output Current (Note 1)			1500			mA	
	Current Limit		PFET Switch	1800	2750	3700	mA	
			NFET Rectifier	1300	2250	3200		
	On-Resistance		PFET Switch		0.15		Ω	
			NFET Rectifier		0.08			
	N-Channel Zero-Crossing Threshold				50		mA	
	Startup Time	V_{OUT}=1.0V			40		µs	
	Minimum On-and Off-Times		T_{ON}		60		ns	
			T_{OFF}		60			
	LX Active Resistance	I2C programmable. Default ON, Resistance from LX_ to PGND_			1		kΩ	
	Output Load Regulation (Voltage Positioning)	R_L = Inductor DC resistance			R_L/4		V/A	
	Output Line Regulation	V_{INB} = 3.0V to 5.5V			0.3		%	
	LX_ Leakage Current	LX_=PGND_ or INB_	T_A=25℃	-1		1	µA	
			T_A=85℃		0.1			

Note 1: Design guidance only, not tested during final test.

Note 2. Limits are 100% production tested at T_A=+25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Buck Converter 8 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT}=$V_{INB\_}$= +3.6V, $C_{BUCK\_}$ =4.7µF, L_=1µH, T_A =-40°C to +85°C (Note 2)

EC#	PARAMETER	CONDITIONS		MIN	TYP	MAX	Unit	TEST#
	Input Voltage Range	Guaranteed by Output Voltage Accuracy and supply current		2.7		5.5	V	
	Shutdown Current (Note 1)	Regulator Disabled, $V_{INB\_}$=4.8V			0.1		µA	
	Ground Current (Note 1)	I_{LOAD} =0mA, no switching, Regulator Enabled			25		µA	
	Default output Voltage	in continuous conductionmode		-3%	2.85	+3%	V	
	Programmable Output Voltage	I_{Load}=0mA, Programmable in 50mV Steps		0.75		3.90	V	
	Maximum Output Current (Note 1)			1500			mA	
	Current Limit		PFET Switch	1800	2750	3700	mA	
			NFET Rectifier	1300	2250	3200		
	On-Resistance		PFET Switch		0.15		Ω	
			NFET Rectifier		0.08			
	N-Channel Zero-Crossing Threshold				50		mA	
	Startup Time	V_{OUT}=1.0V			40		µs	
	Minimum On-and Off-Times		T_{ON}		60		ns	
			T_{OFF}		60			
	LX Active Resistance	I2C programmable. Default ON, Resistance from LX_ to PGND_			1		kΩ	
	Output Load Regulation (Voltage Positioning)	R_L = Inductor DC resistance			R_L/4		V/A	
	Output Line Regulation	V_{INB} = 3.0V to 5.5V			0.3		%	
	LX_ Leakage Current	LX_=PGND_ or INB_	T_A=25℃	-1		1	µA	
			T_A=85℃		0.1			

Note 1: Design guidance only, not tested during final test.

Note 2. Limits are 100% production tested at T_A=+25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Buck Converter 9 Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT}=$V_{INB\_}$= +3.6V, $C_{BUCK\_}$ =4.7µF, L_=1µH, T_A =-40°C to +85°C (Note 2)

EC#	PARAMETER	CONDITIONS		MIN	TYP	MAX	Unit	TEST #
	Input Voltage Range	Guaranteed by Output Voltage Accuracy and supply current		2.7		5.5	V	
	Shutdown Current (Note 1)	Regulator Disabled, $V_{INB\_}$=4.8V			0.1		µA	
	Ground Current (Note 1)	I_{LOAD} =0mA, no switching, Regulator Enabled			25		µA	
	Default output Voltage	in continuous conductionmode		-3%	1.20	+3%	V	
	Programmable Output Voltage	I_{Load}=0mA, Programmable in 50mV Steps		0.75		3.90	V	
	Maximum Output Current (Note 1)			1500			mA	
	Current Limit		PFET Switch	1800	2750	3700	mA	
			NFET Rectifier	1300	2250	3200		
	On-Resistance		PFET Switch		0.15		Ω	
			NFET Rectifier		0.08			
	N-Channel Zero-Crossing Threshold				50		mA	
	Startup Time	V_{OUT}=1.0V			40		µs	
	Minimum On-and Off-Times		T_{ON}		60		ns	
			T_{OFF}		60			
	LX Active Resistance	I2C programmable. Default ON, Resistance from LX_ to PGND_			1		kΩ	
	Output Load Regulation (Voltage Positioning)	R_L = Inductor DC resistance			R_L/4		V/A	
	Output Line Regulation	V_{INB} = 3.0V to 5.5V			0.3		%	
	LX_ Leakage Current	LX_=PGND_ or INB_	T_A=25℃	-1		1	µA	
			T_A=85℃		0.1			

Note 1: Design guidance only, not tested during final test.

Note 2. Limits are 100% production tested at T_A=+25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Table: Summary of BUCK1-BUCK9

No	INPUT PIN	CTRL1 Register Address	DEFAULT		
			Default Voltage (V)	Default ON	CTRL Register RESET
BUCK1	INB1	0x10	1.0	ON	0x0B
BUCK2	INB2	0x12	1.1	ON	0x72
BUCK3	INB3	0x1C	1.0	ON	0x72
BUCK4	INB4	0x26	1.0	ON	0x72
BUCK5	INB5	0x30	1.2,1.35, 1.50, 1.8	ON	0x0B
BUCK6	INB6	0x32	1.35	ON	0x0B
BUCK7	INB7	0x34	2.00	ON	0x0B
BUCK8	INB8	0x36	2.85	OFF	0x08
BUCK9	INB9	0x38	1.20	OFF	0x08

The default on BUCK5 is set to one of four options by VSETB51 and VSETB52.

VSETB51	VSETB52	OUTPUT (V)
0	0	1.2
0	1	1.35
1	0	1.5
1	1	1.8

0: refer to logic low, typically connected to ground.
1: refer to logic high, typically connected to BATT.

LDO Electrical Characteristics

LDO1 (150mA NMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL1}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2, L3)		V_{OUT}		V_{BATT}	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 25mV steps		0.80		2.375	V	
	Maximum Output current	Normal Mode		150			mA	
		Low Power Mode		5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		27	54		
			Low-Power Mode		1.5	3		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation Mode		2.5	5		
			Low-Power Mode		0	1		
	Output Voltage Accuracy	Normal Mode	V_{INL1} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage. V_{BATT} = V_{NOM}+1.5V with 2.45V minimum	-3		+3	%	
		Low Power Mode	V_{INL1} = V_{NOM}+0.3V, I_{OUT} = 0.1mA to 5mA, V_{BATT} = V_{NOM}+1.5V to 5.5V with 2.45V minimum	-3		+3		
	Load regulation (Note L7)	Normal Mode	I_{OUT} = 0.1mA to I_{MAX}, V_{INL1} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum		0.1		%	
		Low Power Mode	I_{OUT}= 0.1mA to 5mA, V_{INL1} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL1} = V_{NOM}+0.3V to 5.5V. I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{INL1}=V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode, I_{OUT}=I_{MAX}	V_{BATT} -V_{OUT}=2.5V		50	100	mV	
			V_{BATT} -V_{OUT}=1.5V		75	300		
		Low Power Mode, I_{OUT}=5mA	BATT to OUT, V_{BATT} =3.6V		50	100		
	Output Current limit	V_{OUT} =90% of V_{NOM}		150	255	400	mA	

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
	Output Load Transient (Note L7)	Normal Mode, $V_{INL1} = V_{NOM}+0.3V$, I_{OUT} = 1% to 100% to 1% of I_{MAX}, $t_R = t_F = 1\mu s$, C_{OUT}=0.66uF/100mA of load current.			60		mV	
		Low-Power Mode, $V_{INL1} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL1}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL1}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$, I_{OUT}=5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{BATT} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT}=C_{OUT1}$ (Note L7)	$V_{INL1DC}=V_{NOM}+0.3V$ V_{INL1AC}=50mV f=1kHz		88		dB	
			f=10kHz		65			
			f=100kHz		51			
			f=1MHz		22			
			f=4.45MHz		15			
		Low Power Mode, Rejection from V_{BATT} and V_{INL1} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz-100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		55		μV_{RMS}	
			V_{OUT} = 1.8V		65			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	V_{BATT}=3.7V, V_{OUT}=1V, Output Diusabled.	Enabled, ADSLDO_=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO_=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L1_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO2 (450mA NMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL7}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2, L3)		V_{OUT}		V_{BATT}	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 25mV steps		0.80		2.375	V	
	Maximum Output current	Normal Mode		450			mA	
		Low Power Mode		5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		<0.1		µA	
			Normal Regulation		31	62		
			Low-Power Mode		1.5	3		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation Mode		2.5	5		
			Low-Power Mode		0	1		
	Output Voltage Accuracy	Normal Mode	V_{INL7} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage. V_{BATT} = V_{NOM}+1.5V with 2.45V minimum	-3		+3	%	
		Low Power Mode	V_{INL7} = V_{NOM}+0.3V, I_{OUT} = 0.1mA to 5mA, V_{BATT} = V_{NOM}+1.5V to 5.5V with 2.45V minimum	-3		+3		
	Load regulation (Note L7)	Normal Mode	I_{OUT} = 0.1mA to I_{MAX}, V_{INL7} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum		0.1		%	
		Low Power Mode	I_{OUT}= 0.1mA to 5mA, V_{INL7} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL7} = V_{NOM}+0.3V to 5.5V. I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{INL7}=V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode, I_{OUT}=I_{MAX}	V_{BATT} -V_{OUT}=2.5V		50	100	mV	
			V_{BATT} -V_{OUT}=1.5V		75	300		
		Low Power Mode, I_{OUT}=5mA	BATT to OUT, V_{BATT} =3.6V		50	100		
	Output Current limit	V_{OUT} =90% of V_{NOM}		450	765	1200	mA	

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
	Output Load Transient (Note L7)	Normal Mode, $V_{INL7} = V_{NOM}+0.3V$, I_{OUT} = 1% to 100% to 1% of I_{MAX}, $t_R = t_F = 1\mu s$, C_{OUT}=0.66uF/100mA of load current.			60		mV	Note 3 ,4
		Low-Power Mode, $V_{INL7} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL7}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	Note 3,4
		Low-Power Mode, $V_{INL7}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$, I_{OUT}=5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{BATT} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT}=C_{OUT2}$ (Note L7)	$V_{INL7DC}=V_{NOM}+0.3V$ V_{INL7AC}=50mV f=1kHz		88		dB	
			f=10kHz		65			
			f=100kHz		51			
			f=1MHz		22			
			f=4.45MHz		15			
		Low Power Mode, Rejection from V_{BATT} and V_{INL7} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz-100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		55		μV_{RMS}	
			V_{OUT} = 1.8V		65			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	V_{BATT}=3.7V, V_{OUT}=1V, Output Diusabled.	Enabled, ADSLDO2=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO2=0	1000				
Overvoltage Clamp(Note L8)								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L2_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay(Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay(Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO3: (300mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL3}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	300			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	2.2		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		17	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL3} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL3\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL3} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL3} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL3} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL3} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX}, V_{INL3}=3.6V		60	120	mV	
			I_{OUT}=I_{MAX}, V_{INL3}=1.7V		150	300		
		Low Power Mode	INL3 to OUT3 I_{OUT}= 5mA, V_{INL3}=3.6V		50	100		
	Output Current limit	V_{OUT} =90% of V_{NOM}		300	510	800	mA	
	Output Load Transient (L3_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL3} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L3_COMP=00		55		mV	
			L3_COMP=01		66			
			L3_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L3_COMP=11		120			
		Low-Power Mode, $V_{INL3} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL3}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL3}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT3}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL3} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO3=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO3=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage (Note L8)	Clamp Active (L3_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent(Note L8)	$V_{OUT3}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO4: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL4}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL4} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL4\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL4} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL4} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL4} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL4} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX} V_{INL4}=3.6V		60	120	mV	
			V_{INL4}=1.7V		150	300		
		Low Power Mode	INL4 to OUT I_{OUT}= 5mA, V_{INL4}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L4_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL4} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L4_COMP=00		55		mV	
			L4_COMP=01		66			
			L4_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L4_COMP=11		120			
		Low-Power Mode, $V_{INL4} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL4}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL4}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT4}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL4} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO4=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO4=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L4_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO5: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL2}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL2} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL2\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL2} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL2} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL2} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL2} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX} V_{INL2}=3.6V		60	120	mV	
			V_{INL2}=1.7V		150	300		
		Low Power Mode	INL2 to OUT I_{OUT}= 5mA, V_{INL2}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L5_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL2} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L5_COMP=00		55		mV	
			L5_COMP=01		66			
			L5_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L5_COMP=11		120			
		Low-Power Mode, $V_{INL2} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL2}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL2}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT5}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL2} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO5=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO5=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L5_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO6 (150mA NMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL1}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2, L3)		V_{OUT}		V_{BATT}	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 25mV steps		0.80		2.375	V	
	Maximum Output current	Normal Mode		150			mA	
		Low Power Mode		5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		<0.1		µA	
			Normal Regulation		27	54		
			Low-Power Mode		1.5	3		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation Mode		2.5	5		
			Low-Power Mode		0	1		
	Output Voltage Accuracy	Normal Mode	V_{INL1} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage. V_{BATT} = V_{NOM}+1.5V with 2.45V minimum	-3		+3	%	
		Low Power Mode	V_{INL1} = V_{NOM}+0.3V, I_{OUT} = 0.1mA to 5mA, V_{BATT} = V_{NOM}+1.5V to 5.5V with 2.45V minimum	-3		+3		
	Load regulation (Note L7)	Normal Mode	I_{OUT} = 0.1mA to I_{MAX}, V_{INL1} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum		0.1		%	
		Low Power Mode	I_{OUT}= 0.1mA to 5mA, V_{INL1} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL1} = V_{NOM}+0.3V to 5.5V. I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{INL1}=V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode, I_{OUT}=I_{MAX}	V_{BATT} -V_{OUT}=2.5V		50	100	mV	
			V_{BATT} -V_{OUT}=1.5V		75	300		
		Low Power Mode, I_{OUT}=5mA	BATT to OUT, V_{BATT} =3.6V		50	100		
	Output Current limit	V_{OUT} =90% of V_{NOM}		150	255	400	mA	

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
	Output Load Transient (Note L7)	Normal Mode, $V_{INL1} = V_{NOM}+0.3V$, I_{OUT} = 1% to 100% to 1% of I_{MAX}, $t_R = t_F = 1\mu s$, C_{OUT}=0.66uF/100mA of load current.			60		mV	Note 3 ,4
		Low-Power Mode, $V_{INL1} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL1}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	Note 3,4
		Low-Power Mode, $V_{INL1}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$, I_{OUT}=5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{BATT} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT}=C_{OUT6}$ (Note L7)	$V_{INL1DC}=V_{NOM}+0.3V$ V_{INL1AC}=50mV f=1kHz		88		dB	
			f=10kHz		65			
			f=100kHz		51			
			f=1MHz		22			
			f=4.45MHz		15			
		Low Power Mode, Rejection from V_{BATT} and V_{INL1} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz-100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		55		μV_{RMS}	
			V_{OUT} = 1.8V		65			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	V_{BATT}=3.7V, V_{OUT}=1V, Output Diusabled.	Enabled, ADSLDO6=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO6=0	1000				
Overvoltage Clamp(Note L8)								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L6_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO7 (150mA NMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL1}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2, L3)		V_{OUT}		V_{BATT}	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 25mV steps		0.80		2.375	V	
	Maximum Output current	Normal Mode		150			mA	
		Low Power Mode		5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		<0.1		µA	
			Normal Regulation		27	54		
			Low-Power Mode		1.5	3		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation Mode		2.5	5		
			Low-Power Mode		0	1		
	Output Voltage Accuracy	Normal Mode	V_{INL1} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage. V_{BATT} = V_{NOM}+1.5V with 2.45V minimum	-3		+3	%	
		Low Power Mode	V_{INL1} = V_{NOM}+0.3V, I_{OUT} = 0.1mA to 5mA, V_{BATT} = V_{NOM}+1.5V to 5.5V with 2.45V minimum	-3		+3		
	Load regulation (Note L7)	Normal Mode	I_{OUT} = 0.1mA to I_{MAX}, V_{INL1} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum		0.1		%	
		Low Power Mode	I_{OUT}= 0.1mA to 5mA, V_{INL1} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL1} = V_{NOM}+0.3V to 5.5V. I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{INL1}=V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode, I_{OUT}=I_{MAX}	V_{BATT} -V_{OUT}=2.5V		50	100	mV	
			V_{BATT} -V_{OUT}=1.5V		75	300		
		Low Power Mode, I_{OUT}=5mA	BATT to OUT, V_{BATT} =3.6V		50	100		
	Output Current limit	V_{OUT} =90% of V_{NOM}		150	255	400	mA	

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
	Output Load Transient (Note L7)	Normal Mode, $V_{INL1} = V_{NOM}+0.3V$, I_{OUT} = 1% to 100% to 1% of I_{MAX}, $t_R = t_F = 1\mu s$, C_{OUT}=0.66uF/100mA of load current.			60		mV	Note 3 ,4
		Low-Power Mode, $V_{INL1} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL1}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	Note 3,4
		Low-Power Mode, $V_{INL1}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$, I_{OUT}=5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{BATT} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT}=C_{OUT7}$ (Note L7)	$V_{INL1DC}=V_{NOM}+0.3V$ V_{INL1AC}=50mV f=1kHz		88		dB	
			f=10kHz		65			
			f=100kHz		51			
			f=1MHz		22			
			f=4.45MHz		15			
		Low Power Mode, Rejection from V_{BATT} and V_{INL1} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz-100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		55		μV_{RMS}	
			V_{OUT} = 1.8V		65			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	V_{BATT}=3.7V, V_{OUT}=1V, Output Diusabled.	Enabled, ADSLDO7=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO7=0	1000				
Overvoltage Clamp(Note L8)								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L7_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO8 (300mA NMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL1}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2, L3)		V_{OUT}		V_{BATT}	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 25mV steps		0.80		2.375	V	
	Maximum Output current	Normal Mode		300			mA	
		Low Power Mode		5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		<0.1		µA	
			Normal Regulation		27	54		
			Low-Power Mode		1.5	3		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation Mode		2.5	5		
			Low-Power Mode		0	1		
	Output Voltage Accuracy	Normal Mode	V_{INL1} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage. V_{BATT} = V_{NOM}+1.5V with 2.45V minimum	-3		+3	%	
		Low Power Mode	V_{INL1} = V_{NOM}+0.3V, I_{OUT} = 0.1mA to 5mA, V_{BATT} = V_{NOM}+1.5V to 5.5V with 2.45V minimum	-3		+3		
	Load regulation (Note L7)	Normal Mode	I_{OUT} = 0.1mA to I_{MAX}, V_{INL1} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum		0.1		%	
		Low Power Mode	I_{OUT}= 0.1mA to 5mA, V_{INL1} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL1} = V_{NOM}+0.3V to 5.5V. I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{INL1}=V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode, I_{OUT}=I_{MAX}	V_{BATT} -V_{OUT}=2.5V		50	100	mV	
			V_{BATT} -V_{OUT}=1.5V		75	300		
		Low Power Mode, I_{OUT}=5mA	BATT to OUT, V_{BATT} =3.6V		50	100		
	Output Current limit	V_{OUT} =90% of V_{NOM}		300	510	800	mA	

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
	Output Load Transient (Note L7)	Normal Mode, $V_{INL1} = V_{NOM}+0.3V$, I_{OUT} = 1% to 100% to 1% of I_{MAX}, $t_R = t_F = 1\mu s$, C_{OUT}=0.66uF/100mA of load current.			60		mV	Note 3 ,4
		Low-Power Mode, $V_{INL1} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL1}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	Note 3,4
		Low-Power Mode, $V_{INL1}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$, I_{OUT}=5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{BATT} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT}=C_{OUT8}$ (Note L7)	$V_{INL1DC}=V_{NOM}+0.3V$ V_{INL1AC}=50mV f=1kHz		88		dB	
			f=10kHz		65			
			f=100kHz		51			
			f=1MHz		22			
			f=4.45MHz		15			
		Low Power Mode, Rejection from V_{BATT} and V_{INL1} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz-100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		55		μV_{RMS}	
			V_{OUT} = 1.8V		65			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	V_{BATT}=3.7V, V_{OUT}=1V, Output Diusabled.	Enabled, ADSLDO8=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO8=0	1000				
Overvoltage Clamp(Note L8)								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L8_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO9: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL3}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL3} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL3\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL3} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL3} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL3} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL3} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX} V_{INL3}=3.6V		60	120	mV	
			V_{INL3}=1.7V		150	300		
		Low Power Mode	INL3 to OUT I_{OUT}= 5mA, V_{INL3}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L9_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL3} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L9_COMP=00		55		mV	
			L9_COMP=01		66			
			L9_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L9_COMP=11		120			
		Low-Power Mode, $V_{INL3} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL3}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL3}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT9}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL3} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO9=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO9=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L9_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO10: (300mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL5}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION			MIN	TYP	MAX	UNITS	TEST#
Operational Specifications									
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)			1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis				1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing			2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps			0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode		300			mA	
			Low Power Mode		5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)			-30%	2.2		µF	
CORE Performance Specifications									
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)			< 0.1		µA	
			Normal Regulation			3.5	10		
			Low-Power Mode			0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)			0	1	µA	
			Normal Regulation			17	40		
			Low-Power Mode			1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL5} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.		-3		+3	%	
		Low Power Mode	$V_{INL5\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.		-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL5} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}			0.1		%	
		Low Power Mode	V_{INL5} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA			0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL5} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA			0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL5} = V_{NOM}+0.3V I_{OUT} = 0.1mA			0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX}	V_{INL5}=3.6V		60	120	mV	
				V_{INL5}=1.7V		150	300		
		Low Power Mode	INL5 to OUT3 I_{OUT}= 5mA, V_{INL5}=3.6V			50	100		
	Output Current limit	V_{OUT} =90% of V_{NOM}			330	510	750	mA	
	Output Load Transient (L10_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL5} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L10_COMP=00			55		mV	
			L10_COMP=01			66			
			L10_COMP=10			99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L10_COMP=11		120			
		Low-Power Mode, $V_{INL5} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL5}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL5}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT10}$(Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL5} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO10=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO10=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage (Note L8)	Clamp Active (L10_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent(Note L8)	$V_{OUT3}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO11: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL3}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL3} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL3\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL3} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL3} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL3} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL3} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX} V_{INL3}=3.6V		60	120	mV	
			V_{INL3}=1.7V		150	300		
		Low Power Mode	INL3 to OUT I_{OUT}= 5mA, V_{INL3}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L11_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL3} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L11_COMP=00		55		mV	
			L11_COMP=01		66			
			L11_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L11_COMP=11		120			
		Low-Power Mode, $V_{INL3} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL3}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL3}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT11}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL3} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO11=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO11=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L11_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO12: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL4}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL4} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL4\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL4} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL4} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL4} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL4} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX} V_{INL4}=3.6V		60	120	mV	
			V_{INL4}=1.7V		150	300		
		Low Power Mode	INL4 to OUT I_{OUT}= 5mA, V_{INL4}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L12_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL4} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L12_COMP=00		55		mV	
			L12_COMP=01		66			
			L12_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L12_COMP=11		120			
		Low-Power Mode, $V_{INL4} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL4}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL4}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT12}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL4} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO12=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO12=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L12_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO13: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL5}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL5} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL5\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL5} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL5} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL5} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL5} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX}, V_{INL5}=3.6V		60	120	mV	
			I_{OUT}=I_{MAX}, V_{INL5}=1.7V		150	300		
		Low Power Mode	INL5 to OUT I_{OUT}= 5mA, V_{INL5}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L13_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL5} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L13_COMP=00		55		mV	
			L13_COMP=01		66			
			L13_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L13_COMP=11		120			
		Low-Power Mode, $V_{INL5} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL5}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL5}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT13}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL5} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO13=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO13=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L13_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO14: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL5}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL5} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL5\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL5} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL5} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL5} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL5} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX}, V_{INL5}=3.6V		60	120	mV	
			I_{OUT}=I_{MAX}, V_{INL5}=1.7V		150	300		
		Low Power Mode	INL5 to OUT I_{OUT}= 5mA, V_{INL5}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L14_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL5} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L14_COMP=00		55		mV	
			L14_COMP=01		66			
			L14_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L14_COMP=11		120			
		Low-Power Mode, $V_{INL5} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL5}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL5}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT14}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL5} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO14=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO14=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L14_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO15 (150mA NMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL1}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2, L3)		V_{OUT}		V_{BATT}	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 25mV steps		0.80		2.375	V	
	Maximum Output current	Normal Mode		150			mA	
		Low Power Mode		5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		<0.1		µA	
			Normal Regulation		27	54		
			Low-Power Mode		1.5	3		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation Mode		2.5	5		
			Low-Power Mode		0	1		
	Output Voltage Accuracy	Normal Mode	V_{INL1} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage. V_{BATT} = V_{NOM}+1.5V with 2.45V minimum	-3		+3	%	
		Low Power Mode	V_{INL1} = V_{NOM}+0.3V, I_{OUT} = 0.1mA to 5mA, V_{BATT} = V_{NOM}+1.5V to 5.5V with 2.45V minimum	-3		+3		
	Load regulation (Note L7)	Normal Mode	I_{OUT} = 0.1mA to I_{MAX}, V_{INL1} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum		0.1		%	
		Low Power Mode	I_{OUT}= 0.1mA to 5mA, V_{INL1} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL1} = V_{NOM}+0.3V to 5.5V. I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{INL1}=V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode, I_{OUT}=I_{MAX}	V_{BATT} -V_{OUT}=2.5V		50	100	mV	
			V_{BATT} -V_{OUT}=1.5V		75	300		
		Low Power Mode, I_{OUT}=5mA	BATT to OUT, V_{BATT} =3.6V		50	100		
	Output Current limit	V_{OUT} =90% of V_{NOM}		150	255	400	mA	

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
	Output Load Transient (Note L7)	Normal Mode, $V_{INL1} = V_{NOM}+0.3V$, I_{OUT} = 1% to 100% to 1% of I_{MAX}, $t_R = t_F = 1\mu s$, C_{OUT}=0.66uF/100mA of load current.			60		mV	Note 3 ,4
		Low-Power Mode, $V_{INL1} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL1}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	Note 3,4
		Low-Power Mode, $V_{INL1}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$, $t_R = t_F = 1\mu s$, I_{OUT}=5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{BATT} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT}=C_{OUT15}$ (Note L7)	$V_{INL1DC}=V_{NOM}+0.3V$ V_{INL1AC}=50mV f=1kHz		88		dB	
			f=10kHz		65			
			f=100kHz		51			
			f=1MHz		22			
			f=4.45MHz		15			
		Low Power Mode, Rejection from V_{BATT} and V_{INL1} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz-100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		55		μV_{RMS}	
			V_{OUT} = 1.8V		65			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	V_{BATT}=3.7V, V_{OUT}=1V, Output Diusabled.	Enabled, ADSLDO15=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO15=0	1000				
Overvoltage Clamp(Note L8)								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L15_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO16: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL5}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL5} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL5\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL5} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL5} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL5} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL5} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX}, V_{INL5}=3.6V		60	120	mV	
			I_{OUT}=I_{MAX}, V_{INL5}=1.7V		150	300		
		Low Power Mode	INL5 to OUT I_{OUT}= 5mA, V_{INL5}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L16_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL5} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L16_COMP=00		55		mV	
			L16_COMP=01		66			
			L16_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L16_COMP=11		120			
		Low-Power Mode, $V_{INL5} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL5}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL5}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT16}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL5} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO16=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO16=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L16_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO17: (300mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL2}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION			MIN	TYP	MAX	UNITS	TEST#
Operational Specifications									
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)			1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis				1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing			2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps			0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode		300			mA	
			Low Power Mode		5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)			-30%	2.2		µF	
CORE Performance Specifications									
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)			< 0.1		µA	
			Normal Regulation			3.5	10		
			Low-Power Mode			0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)			0	1	µA	
			Normal Regulation			17	40		
			Low-Power Mode			1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL2} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.		-3		+3	%	
		Low Power Mode	$V_{INL2\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.		-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL2} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}			0.1		%	
		Low Power Mode	V_{INL2} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA			0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL2} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA			0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL2} = V_{NOM}+0.3V I_{OUT} = 0.1mA			0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX}	V_{INL2}=3.6V		60	120	mV	
				V_{INL2}=1.7V		150	300		
		Low Power Mode	INL2 to OUT3 I_{OUT}= 5mA, V_{INL2}=3.6V			50	100		
	Output Current limit	V_{OUT} =90% of V_{NOM}			330	510	750	mA	
	Output Load Transient (L17_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL2} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L17_COMP=00			55		mV	
			L17_COMP=01			66			
			L17_COMP=10			99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L17_COMP=11		120			
		Low-Power Mode, $V_{INL2} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL2}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL2}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT17}$(Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL2} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO17=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO17=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage (Note L8)	Clamp Active (L17_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent(Note L8)	$V_{OUT3}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO18: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL2}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL2} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL2\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL2} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL2} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL2} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL2} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX} V_{INL2}=3.6V		60	120	mV	
			V_{INL2}=1.7V		150	300		
		Low Power Mode	INL2 to OUT I_{OUT}= 5mA, V_{INL2}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L18_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL2} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L9_COMP=00		55		mV	
			L9_COMP=01		66			
			L9_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L18_COMP=11		120			
		Low-Power Mode, $V_{INL2} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL2}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL2}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT18}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL2} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO18=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO18=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L18_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO19: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL2}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL2} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL2\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL2} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL2} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL2} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL2} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX} V_{INL2}=3.6V		60	120	mV	
			V_{INL2}=1.7V		150	300		
		Low Power Mode	INL2 to OUT I_{OUT}= 5mA, V_{INL2}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L19_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL2} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L19_COMP=00		55		mV	
			L19_COMP=01		66			
			L19_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L19_COMP=11		120			
		Low-Power Mode, $V_{INL2} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL2}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL2}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT19}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL2} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO19=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO19=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L19_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO20: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL3}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL3} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL3\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL3} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL3} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL3} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL3} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX} V_{INL3}=3.6V		60	120	mV	
			V_{INL3}=1.7V		150	300		
		Low Power Mode	INL3 to OUT I_{OUT}= 5mA, V_{INL3}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L20_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL3} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L20_COMP=00		55		mV	
			L20_COMP=01		66			
			L20_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L20_COMP=11		120			
		Low-Power Mode, $V_{INL3} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL3}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL3}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT20}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL3} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO20=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO20=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L20_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO21: (300mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL4}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	300			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	2.2		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		17	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL4} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL4\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL4} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL4} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL4} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL4} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX} V_{INL4}=3.6V		60	120	mV	
			V_{INL4}=1.7V		150	300		
		Low Power Mode	INL4 to OUT3 I_{OUT}= 5mA, V_{INL4}=3.6V		50	100		
	Output Current limit	V_{OUT} =90% of V_{NOM}		330	510	750	mA	
	Output Load Transient (L21_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL4} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L21_COMP=00		55		mV	
			L21_COMP=01		66			
			L21_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L21_COMP=11		120			
		Low-Power Mode, $V_{INL4} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL4}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL4}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT21}$(Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL4} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO21=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO21=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage (Note L8)	Clamp Active (L21_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent(Note L8)	$V_{OUT3}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO22: (300mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL6}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION			MIN	TYP	MAX	UNITS	TEST#
Operational Specifications									
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)			1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis				1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing			2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps			0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode		300			mA	
			Low Power Mode		5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)			-30%	2.2		µF	
CORE Performance Specifications									
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)			< 0.1		µA	
			Normal Regulation			3.5	10		
			Low-Power Mode			0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)			0	1	µA	
			Normal Regulation			17	40		
			Low-Power Mode			1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL6} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.		-3		+3	%	
		Low Power Mode	$V_{INL6\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.		-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL6} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}			0.1		%	
		Low Power Mode	V_{INL6} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA			0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL6} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA			0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL6} = V_{NOM}+0.3V I_{OUT} = 0.1mA			0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX}	V_{INL6}=3.6V		60	120	mV	
				V_{INL6}=1.7V		150	300		
		Low Power Mode	INL6 to OUT3 I_{OUT}= 5mA, V_{INL6}=3.6V			50	100		
	Output Current limit	V_{OUT} =90% of V_{NOM}			330	510	750	mA	
	Output Load Transient (L22_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL6} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L22_COMP=00			55		mV	
			L22_COMP=01			66			
			L22_COMP=10			99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L22_COMP=11		120			
		Low-Power Mode, $V_{INL6} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL6}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL6}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT22}$(Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL6} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO22=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO22=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage (Note L8)	Clamp Active (L22_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent(Note L8)	$V_{OUT3}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO23: (300mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL6}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION			MIN	TYP	MAX	UNITS	TEST#
Operational Specifications									
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)			1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis				1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing			2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps			0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode		300			mA	
			Low Power Mode		5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)			-30%	2.2		µF	
CORE Performance Specifications									
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)			< 0.1		µA	
			Normal Regulation			3.5	10		
			Low-Power Mode			0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)			0	1	µA	
			Normal Regulation			17	40		
			Low-Power Mode			1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL6} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.		-3		+3	%	
		Low Power Mode	$V_{INL6\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.		-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL6} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}			0.1		%	
		Low Power Mode	V_{INL6} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA			0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL6} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA			0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL6} = V_{NOM}+0.3V I_{OUT} = 0.1mA			0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX}	V_{INL6}=3.6V		60	120	mV	
				V_{INL6}=1.7V		150	300		
		Low Power Mode	INL6 to OUT3 I_{OUT}= 5mA, V_{INL6}=3.6V			50	100		
	Output Current limit	V_{OUT} =90% of V_{NOM}			330	510	750	mA	
	Output Load Transient (L23_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL6} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L23_COMP=00			55		mV	
			L23_COMP=01			66			
			L23_COMP=10			99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L23_COMP=11		120			
		Low-Power Mode, $V_{INL6} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL6}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL6}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT23}$(Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL6} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO23=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO23=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage (Note L8)	Clamp Active (L23_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent(Note L8)	$V_{OUT3}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO24: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL4}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL4} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL4\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL4} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL4} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL4} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL4} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX} V_{INL4}=3.6V		60	120	mV	
			V_{INL4}=1.7V		150	300		
		Low Power Mode	INL4 to OUT I_{OUT}= 5mA, V_{INL4}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L24_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL4} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L24_COMP=00		55		mV	
			L24_COMP=01		66			
			L24_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L24_COMP=11		120			
		Low-Power Mode, $V_{INL4} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL4}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL4}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT24}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL4} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO24=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO24=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L24_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO25: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL6}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL6} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL6\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL6} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL6} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL6} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL6} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX} V_{INL6}=3.6V		60	120	mV	
			V_{INL6}=1.7V		150	300		
		Low Power Mode	INL6 to OUT I_{OUT}= 5mA, V_{INL6}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L25_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL6} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L25_COMP=00		55		mV	
			L25_COMP=01		66			
			L25_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L25_COMP=11		120			
		Low-Power Mode, $V_{INL6} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL6}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL6}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT25}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL6} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO25=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO25=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L25_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

LDO26: (150mA PMOS)

Operating conditions (unless otherwise specified) V_{BATT}=V_{INL6}= +3.7V, T_A =-40°C to +85°C (Note L1)

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
Operational Specifications								
	Input Voltage Range	Guaranteed by Output Accuracy and Undervoltage Threshold. (Note L2)		1.7		5.5	V	
	Undervoltage Lockout	Rising, 100mV Hysteresis			1.6	1.7	V	
	System Voltage Range	Guaranteed by main bias testing		2.45		5.5	V	
	Output Voltage Range	Programmable in 50mV steps		0.80		3.95	V	
	Maximum Output current	Guaranteed by Output Accuracy	Normal Mode	150			mA	
			Low Power Mode	5				
	Minimum Output Capacitance	For stability, guranteed by design and not production tested (Note L4)		-30%	1.0		µF	
CORE Performance Specifications								
	System Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L5)		< 0.1		µA	
			Normal Regulation		3.5	10		
			Low-Power Mode		0.5	1		
	Input Supply Current	No Load (Note L8)	Shutdown, T_A=25°C (Note L6)		0	1	µA	
			Normal Regulation		15	40		
			Low-Power Mode		1	2		
	Output Voltage Accuracy	Normal Mode	V_{INL6} = V_{NOM}+0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage.	-3		+3	%	
		Low Power Mode	$V_{INL6\_}$ = V_{NOM}+0.3V V_{BATT}= V_{NOM}+1.5V to 5.5V with 2.45V minimum. I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage.	-3		+3		
	Load regulation (Note L7)	Normal Mode	V_{INL6} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+1.5V with 2.45V minimum, I_{OUT} = 0.1mA to I_{MAX}		0.1		%	
		Low Power Mode	V_{INL6} = V_{NOM}+0.3V, V_{BATT} = V_{NOM}+0.3V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA		0.2			
	Line regulation (Note L7)	Normal Mode	V_{INL6} = V_{NOM}+0.3V to 5.5V I_{OUT} = 0.1mA		0.03		%/V	
		Low Power Mode	V_{BATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{INL6} = V_{NOM}+0.3V I_{OUT} = 0.1mA		0.1			
	Drop-out voltage	Normal Mode	I_{OUT}=I_{MAX} V_{INL6}=3.6V		60	120	mV	
			V_{INL6}=1.7V		150	300		
		Low Power Mode	INL6 to OUT I_{OUT}= 5mA, V_{INL6}=3.6V		50	100		
	Output Current limit	$V_{OUT\_}$=90% of V_{NOM}		165	255	375	mA	
	Output Load Transient (L26_OVCLMP_EN=1) (Note L7)	Normal Mode, V_{INL6} = V_{NOM}+0.3V, I_{OUT} = 1% to 100%	L26_COMP=00		55		mV	
			L26_COMP=01		66			
			L26_COMP=10		99			

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST#
		to 1% of I_{MAX}, $t_R = t_F = 1\mu s$	L26_COMP=11		120			
		Low-Power Mode, $V_{INL6} = V_{NOM}+0.3V$, I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. $t_R = t_F = 1\mu s$			25			
	Output Line Transient (Note L7)	Normal Mode, $V_{INL6}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum. $t_R = t_F = 1\mu s$, $I_{OUT} = I_{MAX}$, V_{NOM} set to any voltage.			5		mV	
		Low-Power Mode, $V_{INL6}=V_{NOM}+0.3V$ to $V_{NOM}+0.8V$ to $V_{NOM}+0.3V$ with 1.7V absolute minimum, $t_R = t_F = 1\mu s$, I_{OUT} =5mA, V_{NOM} set to any voltage.			5			
	Power Supply Rejection	Rejection from V_{IN} to V_{OUT}, I_{OUT}=10% of I_{MAX}, $C_{OUT} = C_{OUT26}$ (Note L7) $V_{INDC}=V_{NOM}+0.3V$, V_{INAC}=50mV	f=1kHz		79		dB	
			f=10kHz		68			
			f=100kHz		50			
			f=1MHz		39			
			f=4.45MHz		35			
		Low Power Mode, Rejection from V_{BATT} and V_{INL6} to V_{OUT}, I_{OUT}=1mA, f=1kHz,			50			
	Output Noise	f=10Hz to100kHz, I_{OUT}=10% of I_{MAX}	V_{OUT} = 0.8V		45		μV_{RMS}	
			V_{OUT} = 1.8V		50			
			V_{OUT} = 3.6V		60			
	Start-Up Ramp Rate (Note L8)	After enabling			100		mV/µs	
	Active Discharge Resistance	$V_{OUT\_}$=1V, Output Disabled	Enabled, ADSLDO26=1	0.05	0.08	0.15	kΩ	
			Disabled, ADSLDO26=0	1000				
Overvoltage Clamp								
	Clamp Active Regulation Voltage(Note L8)	Clamp Active (L26_OVCLMP_EN=1), LDO Output sinking 0.1mA			V_{NOM}		V	
	Clamp Disabled Overvoltage Sink Curent (Note L8)	$V_{OUT}=V_{NOM}$ *110%			2.2		µA	
Timing								
	Enable Delay (Note L8)	Time from LDO enable command received to the output starting to slew, LDO bias enabled.			10		µs	
	Disable Delay (Note L8)	After LDO is disabled; The LDO output voltage will discharge based on Load and C_{OUT}.			0.1		µs	
	Transition time from Low Power mode to Normal Mode(Note L8)	From Low-Power Mode disable to Normal Mode active.			10		µs	
Thermal Shutdown								
	Thermal Shutdown	Output Disabled or Enabled	T_j Rising		165		°C	
			T_j Falling		150			

Note L1: Limits are 100% production tested at T_A=+25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods. Each LDOs EC tables are copied from HHP_LDO ET table at the share point updated on June-6. Added Note L8 to several EC items for the test issue.
Note L2: Input Voltage Range is guaranteed from VOUT+0.3V to 5.5V by Output Accuracy specifications. Inputs between VOUT and VOUT+0.3V are guaranteed by design and subject to drop-out resistance limitations [VIN(min)=VOUT+IOUT*RDO] and may have reduced PSRR and transient performance. For example, with VOUT=0.8V and VMBATT= 2.7V, RDO=0.5W therefore with IOUT=0.2A, the input voltage must be at lease 0.9V (VIN>=VOUT+IOUT*RDO=0.8V+0.2A*0.5Ω=0.9V).
Note L3: VIN(min)=VOUT+0.3V for operation at full load. Default input voltage is 3.7V or VOUT+0.3V, whichever is higher. For NMOS LDO's, VIN must not exceed V_{BATT}.
Note L4: For stability requirements refer to the Remote Capacitor Design with Register Adjustable Compensation section.
Note L5: SYS Shutdown Supply Current is measured in combination with the current of other sections.
Note L6: Input Shutdown Supply Current is only guaranteed to be less than 1uA/LDO when all LDO inputs are combined.
Note L7: Performance may be altered by PCB layout and external components.
Note L8: Design guidance only, not tested during final test

Linear Regulator LDO1-26 Feature Matrix

No	LDO Type	Default Output Voltage (V)	Default ON	Output Voltage Range (V)	Max Output current (mA)	Typ Input Supply Current (μA) (Normal/ Low Power)	Output Cap (μF)	CTRL1		CTRL2	
								Add	RESET	Add	RESET
1	NDRV1	1.00	ON	0.8 to 2.375	150	18 / 0	1	0x40	0XC8	0x60	0x9A
2	NDRV3	1.20	ON		450	22 / 0	1	0x41	0XD0	0x61	0x9A
3	PDRV2	1.80	ON	0.8 to 3.95	300	20 / 1	2.2	0x42	0XD4	0x62	0x9A
4	PDRV1	2.80	ON		150	18 / 1	1	0x43	0XE8	0x63	0x9A
5	PDRV1	1.80	ON		150	18 / 1	1	0x44	0XD4	0x64	0x1A
6	NDRV1	1.1	ON	0.8 to 2.375	150	18 / 0	1	0x45	0xCC	0x65	0x9A
7	NDRV1	1.1	ON		150	18 / 0	1	0x46	0xCC	0x66	0x9A
8	NDRV2	1.00	ON		300	20 / 0	1	0x47	0xC8	0x67	0x9A
9	PDRV1	1.80	OFF	0.8 to 3.95	150	18 / 1	1	0x48	0x14	0x68	0x92
10	PDRV2	1.80	ON		300	20 / 1	2.2	0x49	0xD4	0x69	0x9A
11	PDRV1	1.80	ON		150	18 / 1	1	0x4A	0xD4	0x6A	0x9A
12	PDRV1	3.00	ON		150	18 / 1	1	0x4B	0xEC	0x6B	0x9A
13	PDRV1	1.80	ON		150	18 / 1	1	0x4C	0xD4	0x6C	0x9A
14	PDRV1	1.80	ON		150	18 / 1	1	0x4D	0xD4	0x6D	0x9A
15	NDRV1	1.00	ON	0.8 to 2.375	150	18 / 0	1	0x4E	0xC8	0x6E	0x9A
16	PDRV1	1.80	ON	0.8 to 3.95	150	18 / 1	1	0x4F	0xD4	0x6F	0x1A
17	PDRV2	1.2	OFF		300	20 / 1	2.2	0x50	0x08	0x70	0x92
18	PDRV1	1.8	OFF		150	18 / 1	1	0x51	0x14	0x71	0x92
19	PDRV1	1.8	OFF		150	18 / 1	1	0x52	0x14	0x72	0x92
20	PDRV1	1.80	OFF		150	18 / 1	1	0x53	0x14	0x73	0x92
21	PDRV2	2.8	OFF		300	20 / 1	2.2	0x54	0x28	0x74	0x92
22	PDRV2	2.80	OFF		300	20 / 1	2.2	0x55	0x28	0x75	0x92
23	PDRV2	3.00	OFF		300	20 / 1	2.2	0x56	0x2C	0x76	0x92
24	PDRV1	3.00	OFF		150	18 / 1	1	0x57	0x2C	0x77	0x92
25	PDRV1	3.00	OFF		150	18 / 1	1	0x58	0x2C	0x78	0x92
26	PDRV1	3.00	OFF		150	18 / 1	1	0x59	0x2C	0x79	0x92

Note that LDO20 has the external pin, ENL20, to enable/disable.
Note that LDO21 has the external pin, ENL21, to enable/disable.
Note that LDO22 has the external pin, ENL22, to enable/disable.
Note that LDO2's default is set by VSETB51 & VSETB52 status.

RESETB Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT}=+3.7V, V_{VIO}=V_{OUT3}=1.8V, T_A=-40°C to +85°C

EC#	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS	TEST#
	RESETB Threshold	With respect to LDO3 POK=HIGH		92	95	%	
	RESETB Active Time-out Period	From LDO3 POK=HIGH to RESETB = HIGH		60		ms	

Manual Reset (MRSTB) Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT}=+3.7V, V_{VIO}=V_{OUT3}=1.8V, T_A=-40°C to +85°C

EC#	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS	TEST#
	Manual Reset Debounce Timer	The period between MRSTB1 & MRSTB2=Low and Automatic reboot start (7sec is Default)		3		sec	
				4			
				5			
				6			
				7			
				8			
				9			
				10			
	Power ON Waiting time	After RESETB=LOW until default on regulators turn on in sequence.		256		ms	
	PWRHOLD Waiting Time	From LDO3 POK=H until the default on regulators are held on		1024		ms	

32KHCP, 32KHAP & P32KH Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT}=+3.7V, V_{RTC}=2.5V, VCCP32KH=VCC32KCP=V_{VIO}=V_{OUT3}=1.8V, Typical values are at T_A=25°C

EC#	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS	TEST #
Oscillator Specification								
	Output duty cycle	Required Operation			50		%	
	Output High Voltage	Internal logic supply I_{SOURCE} = 2mA	32KHCP	$V_{VCC32kCP}$ – 0.4			V	
			P32KH	$V_{VCCP32KH}$ – 0.4				
			32KHAP	V_{VIO}– 0.4				
	Output Low Voltage	Internal logic supply I_{SINK} = 2mA	32KHCP			0.4	V	
			P32KH			0.4		
			32KHAP			0.4		

RTC Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT}=+3.7V, VCOIN=3.0V default, T_A=-40°C to +85°C

EC#	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS	TEST#
	Operating Voltage Range VCOIN (Note 1)	BATT=OPEN	1.8		3.6	V	
	Timekeeping Current, IBK	BATT=OPEN, VCOIN=3.0V		2	4	µA	9028
	Start-up time (Note 1)			2.5		sec	
	Time Accuracy (Note 1)	Per day		2		sec	
	XIN to ground capacitance			22		pF	
	XOUT to ground capacitance			22		pF	

Note 1: Design guidance only, not tested during final test.

VCOIN (Coin Charger) Electrical Characteristics

Operating conditions (unless otherwise specified) V_{BATT}=+3.7V, T_A=-40°C to +85°C

EC#	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS	TESET#
	Default Output Voltage	I_{LOAD}=1µA	-3%	3.0	+3%	V	
	Programmble Output voltage	I_{LOAD}=1µA		2.5		V	
			-3%	3.0	+3%	V	
				3.3		V	
				3.5			
	Constant Current Limit	V_{VCOIN} short to AGND1, (100uA default)		80		µA	
				100			
				200			
				400			
				600			
				800			
	Internal Series Resistor	1k Default		Bypass		kΩ	
				1			
				3			
				6			
	Reverse Leakage current from VCOIN to V_{BATT}	BATT=0V, V_{VCOIN}=3.0V		2	10	µA	9028
	Regulator ground current (Note 1)	I_{LOAD}=1µA		5		µA	

Note 1: Design guidance only, not tested during final test.

Power Summary

Power	Input	LDO Type	Default (V)	Voltage Range (V)	Step (mV)	Min Load current (mA)	Default ON at initial power-on	ON/OFF Control after initial power-on	Note
BUCK1	INB1		1.0	0.75~ 1.5375	12.5	1500	ON	PWRREQ or I2C	
BUCK2	2x INB2A 2x INB2B		1.1	0.6-3.7875	12.5	5000	ON	PWRREQ or I2C	1. DVS Function
BUCK3	2x INB3		1.0		12.5	2500	ON	PWRREQ or I2C	
BUCK4	2x INB4A 2x INB4B		1.0		12.5	5000	ON	PWREWQ or I2C	
BUCK5	INB5		1.2 (in VSETB51 =VBSET B2=L)	0.75~ 3.90	50	1500	ON	I2C	1. Default Output adjustment by the status on VSETB51/2 2. It's not fly-over in normal mode.
BUCK6	INB6		1.35			1500	ON	I2C	
BUCK7	2x INB7		2.00			1500	ON	I2C	
BUCK8	INB8		2.85			1500	OFF	I2C or ENB8	The external enable/disable pin, ENB8
BUCK9	INB9		1.20			1500	OFF	I2C or ENB9	The external enable/disable pin, ENB9
LDO1	INL1	NDRV1	1.00	0.8~ 2.375	25	150	ON	I2C	
LDO2	INL7	NDRV3	1.20			450	ON	PWRREQ or I2C	Default by VSETB51 & VSETB52 status
LDO3	INL3	PDRV2	1.80	0.8~ 3.95	50	300	ON	I2C	
LDO4	INL4	PDRV1	2.80			150	ON	I2C	
LDO5	INL2	PDRV1	1.80			150	ON	I2C	
LDO6	INL1	NDRV1	1.1	0.8~ 2.375	25	150	ON	PWRREQ or I2C	
LDO7	INL1	NDRV1	1.10			150	ON	PWRREQ or I2C	
LDO8	INL1	NDRV2	1.00			300	ON	PWRREQ or I2C	
LDO9	INL3	PDRV1	1.80	0.8~ 3.95	50	150	OFF	I2C	
LDO10	INL5	PDRV2	1.80			300	ON	PWRREQ or I2C	
LDO11	INL3	PDRV1	1.80			150	ON	PWRREQ or I2C	
LDO12	INL4	PDRV1	3.00			150	ON	PWRREQ or I2C	
LDO13	INL5	PDRV1	1.80			150	ON	I2C	
LDO14	INL5	PDRV1	1.80			150	ON	PWRREQ or I2C	
LDO15	INL1	NDRV1	1.00	0.8~ 2.375	25	150	ON	PWRREQ or I2C	
LDO16	INL5	PDRV1	1.80	0.8~ 3.95	50	150	ON	PWRREQ or I2C	
LDO17	INL2	PDRV2	1.20			300	OFF	I2C	
LDO18	INL2	PDRV1	1.80			150	OFF	I2C	
LDO19	INL2	PDRV1	1.80			150	OFF	I2C	
LDO20	INL3	PDRV1	1.80			150	OFF	I2C OR ENL20	ENL20, external enable/disable pin
LDO21	INL4	PDRV2	2.80			300	OFF	I2C OR ENL21	ENL21, external enable/disable pin
LDO22	INL6	PDRV2	2.80			300	OFF	I2C OR ENL22	ENL22, external enable/disable pin
LDO23	INL6	PDRV2	3.00			300	OFF	I2C	
LDO24	INL4	PDRV1	3.00			150	OFF	I2C	
LDO25	INL6	PDRV1	3.00			150	OFF	I2C	
LDO26	INL6	PDRV1	3.00			150	OFF	I2C	

Pin Description

WLP Pkg	Name	Description
BUCK CONVERTERS		
BUCK1		
D2	INB1	Input terminal to Buck1 converter. Bypass with a 2.2uF to ground.
C1	PGND1	Power ground for Buck1 converter
D1	LX1	DC/DC switching node for Buck1 converter
C2	BUCK1	Voltage Feedback for Buck1. For a better load transient response, place the pin as close to the load as possible. Bypass with a 4.7uF to ground.
BUCK2		
L7	INB2B	Input terminal to second-phase Buck2 converter. Bypass with a 10uF to power ground.
M7	INB2B	
L8	INB2A	nput terminal to first-phase Buck2 converter. Bypass with a 10uF to power ground.
M8	INB2A	
L6	LX2B	DC/DC switching node for the second-phase Buck2 converter. Use a 1uH
M6	LX2B	
L9	LX2A	DC/DC switching node for the first-phase Buck2 converter. Use a 1uH
M9	LX2A	
K10	BUCK2	Voltage Feedback for Buck2. Place the pin as close to the load as possible. Bypass with two 22uF to power ground.
K9	SNS2P	Sense +. place the pin as close to the load as possible.
K8	SNS2N	Sense -. place the pin as close to the load as possible.
L5	PGND2B	Power ground for the second-phase.
M5	PGND2B	
L10	PGND2A	Power ground for the first-phase.
M10	PGND2A	
BUCK3		
J11	INB3	Input terminal to Buck3 converter. Bypass with a 10uF to ground.
J12	INB3	
H10	SNS3P	Sense +. place the pin as close to the load as possible.
J10	SNS3N	Sense -. place the pin as close to the load as possible.
G11	PGND3	Power ground
G12	PGND3	
H11	LX3	DC/DC switching node Buck3 converter
H12	LX3	
G10	BUCK3	Voltage Feedback for Buck3. Place the pin as close to the load as possible. Bypass with a 22uF to ground.
BUCK4		
G1	INB4A	Input terminal to dual-phase Buck4 converter. Bypass with a 10uF to power ground.
G2	INB4A	
H1	INB4B	Input terminal to dual-phase Buck4 converter. Bypass with a 10uF to power ground.
H2	INB4B	
F1	LX4A	DC/DC switching node for the first-phase Buck4 converter.
F2	LX4A	
J1	LX4B	DC/DC switching node for the second-phase Buck4 converter.
J2	LX4B	
F3	BUCK4	Voltage Feedback for Buck4. Place the pin as close to the load as possible. Bypass with a 22uF to power ground.
E1	PGND4A	Power ground for the first-phase converter.
E2	PGND4A	
K1	PGND4B	Power ground for the second-phase converter.
K2	PGND4B	

WLP Pkg	Name	Description
G3	SNS4P	Sense +. place the pin as close to the load as possible.
H3	SNS4N	Sense -. place the pin as close to the load as possible.
BUCK5		
E12	INB5	Input terminal to Buck5 converter. Bypass with a 2.2uF to ground
C12	PGND5	Power ground
D12	LX5	DC/DC switching node Buck5 converter
E11	BUCK5	Voltage Feedback for Buck5. For a better load transient response, place the pin as close to the load as possible. Bypass with a 4.7uF to ground
H4	VSETB51	Logic input to set the BUCK5 default. For the details, refer to the EC table.
H5	VSETB52	
BUCK6		
B1	INB6	Input terminal to Buck6 converter. Bypass with a 2.2uF to ground
A3	PGND6	Power ground
A2	LX6	DC/DC switching node Buck6 converter
B2	BUCK6	Voltage Feedback for Buck6. For a better load transient response, place the pin as close to the load as possible. Bypass with a 4.7uF to ground
BUCK7		
B11	INB7	Input terminal to BUCK7 converter. Bypass with a 2.2uF to ground
C11	INB7	
A11	PGND7	Power ground
B12	LX7	DC/DC switching node Buck7 converter
D11	BUCK7	Voltage Feedback for Buck7. For a better load transient response, place the pin as close to the load as possible. Bypass with a 2.2uF to ground
BUCK8		
M11	INB8	Input terminal to Buck8 converter. Bypass with a 2.2uF to ground
K12	PGND8	Power ground
L12	LX8	DC/DC switching node Buck8 converter
L11	BUCK8	Voltage Feedback for Buck8. For a better load transient response, place the pin as close to the load as possible. Bypass with a 4.7uF to ground
C3	ENB8	External enable/disable pin, Active-high to enable. A 800kΩ internal pull-down resistance to the ground. If this pin is not used, leave it open.
BUCK9		
L2	INB9	Input terminal to Buck9 converter. Bypass with a 2.2uF to ground
L1	PGND9	Power ground
M2	LX9	DC/DC switching node Buck9 converter
J3	BUCK9	Voltage Feedback for Buck9. For a better load transient response, place the pin as close to the load as possible. Bypass with a 4.7uF to ground
B3	ENB9	External enable/disable pin, Active-high to enable. A 800kΩ internal pull-down resistance to the ground. If this pin is not used, leave it open.
DVS INPUTS		
F8	DVS1	Dynamic Voltage Scalling logic input for BUCK2, 3, 4. For the details, refer to the technical description on DVS section.
G8	DVS2	
H8	DVS3	
H6	SELB2	Voltage selection logic input for BUCK2. Logic-high for no DVS, logic low for DVS enabled. For the details, refer to the technical description.
H7	SELB3	Voltage selection logic input for BUCK3. Logic-high for no DVS, logic low for DVS enabled. For the details, refer to the technical description.
J7	SELB4	Voltage selection logic input for BUCK4. Logic-high for no DVS, logic low for DVS enabled. For the details, refer to the technical description.
LINEAR REGULATORS		
A5	INL1	Input to LDO1, 6, 7, 8, 15. Bypass with a 4.7uF to ground.
C5	OUT1	150mA NMOS LDO1 OUTPUT. Bypass with a 1uF to ground.
D5	OUT6	150mA NMOS LDO6 OUTPUT. Bypass with a 1uF to ground.
C4	OUT7	150mA NMOS LDO7 OUTPUT. Bypass with a 1uF to ground.
B5	OUT8	300mA NMOS LDO8 OUTPUT. Bypass with a 1uF to ground.

WLP Pkg	Name	Description
D4	OUT15	150mA NMOS LDO15 OUTPUT. Bypass with a 1uF to ground.
A6	INL2	Input to LDO5, 17, 18,19. Bypass with a 4.7uF to ground.
C6	OUT5	150mA PMOS LDO5 OUTPUT. Bypass with a 1uF to ground.
B6	OUT17	300mA PMOS LDO17 OUTPUT. Bypass with a 2.2uF to ground.
D6	OUT18	150mA PMOS LDO18 OUTPUT. Bypass with a 1uF to ground.
E6	OUT19	150mA PMOS LDO19 OUTPUT. Bypass with a 1uF to ground.
A10	INL3	Input to LDO3, 9, 11, 20. Bypass with a 4.7uF to ground.
B10	OUT3	300mA PMOS LDO3 OUTPUT. Bypass with a 2.2uF to ground.
C10	OUT9	150mA PMOS LDO9 OUTPUT. Bypass with a 1uF to ground.
D10	OUT11	150mA PMOS LDO11 OUTPUT. Bypass with a 1uF to ground.
E10	OUT20	150mA PMOS LDO20 OUTPUT. Bypass with a 1uF to ground.
D3	ENL20	Active high to enable LDO20. A 800kΩ internal pull-down resistance to the ground.
A8	INL4	Input to LDO4, 12, 21, 24. Bypass with a 4.7uF to ground.
C8	OUT4	150mA PMOS LDO4 OUTPUT. Bypass with a 1uF to ground.
D8	OUT12	150mA PMOS LDO12 OUTPUT. Bypass with a 1uF to ground.
B8	OUT21	300mA PMOS LDO21 OUTPUT. Bypass with a 2.2uF to ground.
E3	ENL21	Active high to enable LDO21. A 800kΩ internal pull-down resistance to the ground.
E8	OUT24	150mA PMOS LDO24 OUTPUT. Bypass with a 1uF to ground.
A9	INL5	Input to LDO10, 13, 14, 16. Bypass with a 4.7uF to ground.
B9	OUT10	300mA PMOS LDO10 OUTPUT. Bypass with a 2.2uF to ground.
C9	OUT13	150mA PMOS LDO13 OUTPUT. Bypass with a 1uF to ground.
D9	OUT14	150mA PMOS LDO14 OUTPUT. Bypass with a 1uF to ground.
E9	OUT16	150mA PMOS LDO16 OUTPUT. Bypass with a 1uF to ground.
A7	INL6	Input to LDO22, 23, 25, 26. Bypass with a 4.7uF to ground.
B7	OUT22	300mA PMOS LDO22 OUTPUT. Bypass with a 2.2uF to ground.
E4	ENL22	Active high to enable LDO22. A 800kΩ internal pull-down resistance to the ground.
D7	OUT23	300mA PMOS LDO23 OUTPUT. Bypass with a 2.2uF to ground.
C7	OUT25	150mA PMOS LDO25 OUTPUT. Bypass with a 1uF to ground.
E5	OUT26	150mA PMOS LDO26 OUTPUT. Bypass with a 1uF to ground.
A4	INL7	Input to LDO2. Bypass with a 1uF to ground
B4	OUT2	450mA NMOS LDO2 OUTPUT. Bypass with a 1uF to ground.
ON/OFF Power Control and Input		
L3	BATT	Main Supply input for internal circuitry. Bypass with a 1uF to GND.
M3	BATT	Bypass with a 1uF to ground.
G4	JIGONB	External ON control signal. Active-high with 16msec debounced time initiates the power-on sequence. This pin has to have an external pull-up resistance such as 800kΩ. If this pin is not used, must be connected to BATT via a pull-up resistor.
F4	ACOKB	External ON control signal. Active-Low with 16msec debounced time initiates the power-on sequence and one-shot timer simultaneously. After one-shot timer expires, this power-on source is no longer valid. The PWRHOLD signal must be set to high before this one-shot timer expires. If not, the PMIC will shutdown as soon as the one-shot timer expires. This pin needs an external pull-up resistance such as a 800kΩ. If this pin is not used, this pin must be connected to BATT with a pull-up resistance such as 800kΩ.
G5	PWRON	External ON control signal. Active-high with 16msec debounced time initiates the power-on sequence. This pin has an internal pull-down 800kΩ. If this pin is not used, leave it open.
G6	PWRHOLD	Logic high input from application processor keeps the PMIC enabled and logic low can turn off the PMIC. See Power ON/OFF Sequence for a detailed description. Hi-Z in off condition. If necessary, put a pull-down resistor.

WLP Pkg	Name	Description
H9	PWRREQ	Enable pin for BUCKs and LDOs. For the details, refer to the technical description.
G9	VIO	IO supply voltage. Bypass with a 0.1uF. Connect this pin to the OUT3 Output.
Manual Reset		
F7	MRSTB1	Manual Reset Input 1. Active low longer than the 7sec, default, to generate the manual reset process. A external pull-up resistance is required. If this pin is not used, this pin must be connected to OUT3 with a pull-up resistance such as 200kΩ.
G7	MRSTB2	Manual Reset Input 2. Active low longer than the 7sec, default, to generate the manual reset process. A external pull-up resistance is required. If this pin is not used, this pin must be connected to OUT3 with a pull-up resistance such as 200kΩ.
LOGIC OUPUT		
F6	IRQB	Interrupt Output. A external pull-up resistance, 14k, to the OUT3.
F5	RESETB	Reset output. Active low. A external pull-up resistance, 14k, to the OUT3.
E7	ONOB	Inverted output signal of PWRON. A external pull-up resistance, 100k, to the OUT3. If this pin is not used, this pin must be connected to OUT3 with a pull-up resistance such as 200kΩ.
RTC		
M4	XIN	32.768kHz Crystal Input. Connect a 22pF load capacitance to ground.
L4	XOUT	32.768kHz Crystal Output. Connect a 22pF load capacitance to ground.
J6	32KHAP	32.768kHz Clock Output with VIO. The default ON in the low power mode.
K4	32KHCP	32.768kHz Clock Output with VCC32KCP. The default is OFF.
J5	P32KHZ	32.768kHz Clock Output with VCCP32KH. The default is OFF.
K5	VCCP32KH	IO power rail for P32KH output.
J4	VCC32KCP	IO power rail for 32KHCP output.
K6	VCOIN	Back up battery charger output. The default is 3.0V.
SERIAL INTERFACE		
J8	SCL	Clock input for serial interface. Hi-Z in off condition. Use a pull-up resistor, 1.5k~2.2kΩ, to OUT3.
J9	SDA	Data input for serial interface. Hi-Z in off condition. Use a pull-up resistor, 1.5k~2.2kΩ, to OUT3.
Analog GROUND		
F11	AGND1	Analog ground for internal analog.
F12	AGND1	
F10	AGND2	Analog ground for reference.
DIGITAL GROUND		
F9	DGND	Digital ground for internal digital blocks. Connect it to AGND1/2.
NO CONNECTION		
A1	NC	Not Connected (No Internal Connection)
A12	NC	Not Connected (No Internal Connection)
K3	NC	Not Connected (No Internal Connection)
K7	NC	Not Connected (No Internal Connection)
K11	NC	Not Connected (No Internal Connection)
M1	NC	Not Connected (No Internal Connection)
M12	NC	Not Connected (No Internal Connection)

External Components

FUNCTION/PIN	External component	Notes
INPUT		
BATT	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
BUCK1 CONVERTER		
INB1	2.2μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA
LX1	1μH	TOKO, DFR252010-1R0N, 49mΩ(typ) DCR, 2.0x2.5x1.0mm3
BUCK1	4.7μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ475MA
BUCK2 CONVERTER		
INB2A	10μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ106MA
INB2B	10μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ106MA
LX2A	1μH	TOKO, DFR252010-1R0N, 49mΩ(typ) DCR, 2.0x2.5x1.0mm3
LX2B	1μH	TOKO, DFR252010-1R0N, 49mΩ(typ) DCR, 2.0x2.5x1.0mm3
BUCK2	2x 22μF	6.3V, X5R , 0805, Ceramic capacitor,Taiyo Yuden JMK212BJ226MG
BUCK3 CONVERTER		
INB3	10μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ106MA
LX3	1μH	TOKO, DFR252010-1R0N, 49mΩ(typ) DCR, 2.0x2.5x1.0mm3
BUCK3	22μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ106MA
BUCK4 CONVERTER		
INB4A	10μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ106MA
INB4B	10μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ106MA
LX4A	1μH	TOKO, DFR252010-1R0N, 49mΩ(typ) DCR, 2.0x2.5x1.0mm3
LX4B	1μH	TOKO, DFR252010-1R0N, 49mΩ(typ) DCR, 2.0x2.5x1.0mm3
BUCK4	2x 22μF	6.3V, X5R , 0805, Ceramic capacitor,Taiyo Yuden JMK212BJ226MG
BUCK5 CONVERTER		
INB5	2.2μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA
LX5	1μH	TOKO, DFR252010-1R0N, 49mΩ(typ) DCR, 2.0x2.5x1.0mm3
BUCK5	4.7μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ475MA
BUCK6 CONVERTER		
INB6	2.2μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA
LX6	1μH	TOKO, DFR252010-1R0N, 49mΩ(typ) DCR, 2.0x2.5x1.0mm3
BUCK6	4.7μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ475MA
BUCK7 CONVERTER		
INB7	2.2μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA
LX7	1μH	TOKO, DFR252010-1R0N, 49mΩ(typ) DCR, 2.0x2.5x1.0mm3
BUCK7	4.7μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ475MA
BUCK8 CONVERTER		
INB8	2.2μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA
LX8	1μH	TOKO, DFR252010-1R0N, 49mΩ(typ) DCR, 2.0x2.5x1.0mm3
BUCK8	4.7μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ475MA
BUCK9 CONVERTER		
INB9	2.2μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA
LX9	1μH	TOKO, DFR252010-1R0N, 49mΩ(typ) DCR, 2.0x2.5x1.0mm3
BUCK9	4.7μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ475MA
Linear Regulators		
INL1	4.7μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ475MA
INL2	4.7μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ475MA
INL3	4.7μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ475MA
INL4	4.7μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ475MA
INL5	4.7μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ475MA
INL6	4.7μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ475MA
INL7	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT1	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT2	1μF (or 2.2μF)	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV (6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA)
OUT3	2.2μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA
OUT4	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT5	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT6	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT7	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT8	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT9	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT10	2.2μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA

OUT11	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT12	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT13	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT14	1μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA
OUT15	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT16	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT17	2.2μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA
OUT18	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT19	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT20	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT21	2.2μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA
OUT22	2.2μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA
OUT23	2.2μF	6.3V, X5R , 0603, Ceramic capacitor,Taiyo Yuden JMK107BJ225MA
OUT24	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT25	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
OUT26	1μF	6.3V, X5R, 0402, Ceramic capacitor, Taiyo Yuden, JMK105BJ105MV
PERIPHERALS		
VCCP32KH	0.1μF	10V, X5R, 0402, Ceramic capacitor,Taiyo Yuden LMK105BJ104MV
VCC32KCP	0.1μF	10V, X5R, 0402, Ceramic capacitor,Taiyo Yuden LMK105BJ104MV
VCOIN		Con battery or super-cap
X-tal		32.768kHz crystal, 12.5pF load capacitance, 20ppm Crystal between XIN and XOUT
XIN	22pF	C0H, 0402, 50V, Taiyo Yuden UMK105CH220JV
XOUT	22pF	C0H, 0402, 50V, Taiyo Yuden UMK105CH220JV
ACOKB	800kΩ	Pull-Up Resistance
ONOB	200kΩ	Pull-Up Resistance to OUT3
IRQB	200kΩ	Pull-Up Resistance to OUT3
MRSTB1	200kΩ	Pull-Up Resistance to OUT3
MRSTB2	200kΩ	Pull-Up Resistance to OUT3
SDA	5.6kΩ for 100KHz speed 1.5kΩ for 400KHz speed 680Ω for 1MHz speed	Pull-Up Resistance to OUT3
SCL	5.6kΩ for 100KHz speed 1.5kΩ for 400KHz speed 680Ω for 1MHz speed	Pull-Up Resistance to OUT3
RESETB	14kΩ	Pull-Up Resistance to OUT3
ETC		
Any pin required to pass 8kV module level ESD	0.1 μF	Absorb ESD energy

Top System Management

System Faults

The PMIC monitors the system for the following faults:

- Global Thermal Fault
- Local Thermal Shutdown
- Under-Voltage Lock Out

Global Thermal Fault

MAX77686A has 1 centralized thermal circuit which senses temperature on the die. If temperature increases >165C (T_{SHDN}) this constitutes a thermal shutdown event and the MAX77686A enters its global shutdown state.
In addition to the 165°C threshold, there are 2 additional comparators which trip at 120°C and 140°C. Interrupts are generated in the event the die temperature reaches 120°C or 140°C.
There is a 15°C thermal hysteresis. After thermal shutdown, if the die temperature reduces by 15°C, the thermal shutdown bus is de-asserted and the default power-on supplies can be enabled in the sequencing again.

Local Thermal Shutdown

If any of LDOs or Step-down regulators reaches thermal shut down threshold, the PMIC will shut down that block locally. If the temperature goes below a threshold, that block goes back to normal operation. The charger has an independent thermal control circuit that regulates die temperature during charging.

Under-Voltage Lock Out

When the power supply source, BATT, is below V_{UVLO}, the PMIC enters its under-voltage lockout mode (UVLO). The UVLO forces the PMIC to a dormant state until the source voltage is high enough to allow the PMIC to be securely functional. The I^2C does not function in UVLO and the I^2C type-O register contents are reset in UVLO.
The rising UVLO threshold is set at 3.2V to turn on default-on power supplies.

Power ON/OFF Events

The power management circuit must be able to handle all issues regarding power on the handset. The following pins and battery voltage determines the power on/off status of the handset:

PWRON / JIGONB / ACOKB
SMPL
WTSR
RTC Internal Alarm1 &2
PWRHOLD

Power ON Events

PWRON=HIGH

A Logic High on PWRON pin is the normal way of powering up a handset. Once PWRON is held high for longer than the debounce time, 16ms typ; default power supplies turn on in sequencing. When OUT3 reaches 92% of its final value, a 60ms reset timer is started. At the completion of the 60ms reset timer, RESETB is allowed to be held high (provided no other circuit pulls low on this WIRED-OR output). After RESETB is asserted high; now the AP processor is initialized and will assert PWRHOLD high. Then PWRHOLD maintains the default-on supplies on. If active-high on PWRON is released before the PWRHOLD signal is asserted then the default power supplies turn off. Once the PMIC is ON, the default power supplies can be turned off by the AP processor asserting PWRHOLD low as long as PWRON=low and a valid power supply on BATT.

JIGONB=LOW

A Logic Low on JIGONB pin is the normal way of powering up a handset. Once JIGONB is held low for longer than the debounce time, 16ms typ; default power supplies turn on in sequencing. When OUT3 reaches 92% of its final value, a 60ms reset timer is started. At the completion of the 60ms reset timer, RESETB is allowed to be held high (provided no other circuit pulls low on this WIRED-OR output). After RESETB is asserted high; now the AP processor is initialized and will assert PWRHOLD high. Then PWRHOLD maintains the default-on supplies on. If active-low on JIGONB is released before the PWRHOLD signal is asserted then the default power supplies turn off. Once the PMIC is ON, the

default power supplies can be turned off by the AP processor asserting PWRHOLD low as long as JIGONB=High and a valid power supply on BATT.

ACOKB=LOW

Logic Low on ACOKB is the normal way of powering up a handset. Once ACOKB is held low for longer than the debounce timer, 16ms typ; default power supplies turn on in sequencing and one-shot timer is counted simultaneously. The AP processor must pull PWRHOLD high before the completion of the 1 second one-shot to keep the PMIC ON since ACOKB=LOW is no longer power-on source to keep the PMIC ON. If PWRHOLD is not pulled high before the completion of the 1 second one-shot, the part will shutdown all regulators and rest of circuits.
When OUT3 reaches 92% of its final value, a 60ms reset timer is started. At the completion of the 60ms reset timer, RESETB is allowed to be held high (provided no other circuit pulls low on this WIRED-OR output). After RESETB is asserted high; now the AP processor is initialized and will assert PWRHOLD high. Then PWRHOLD maintains the default-on supplies on.

SMPL

SMPL (Sudden Momentary Power Loss) event could also turns on the default power supplies as long as SMPL_EN is set to 1. The detailed functions are described as below:
SMPL circuits run off coin battery. It is default 0. If SMPL_EN bit is set to 1, BATT UVLO falling (power loss) will start SMPL timer (default is 1.0s). If BATT UVLO rising is detected before the SMPL timer expires, the default-on supplies will turn on in sequencing and an interrupt event will be asserted. The default-on supplies are kept on as long as the interrupt event is not read in PWRHOLD=Low. In order to keep all default-on supplies on, the PWRHOLD must be held high before the interrupt event is read.
If BATT UVLO rising is detected after the SMPL timer is expired, the PMIC will remain off and reset the SMPL enable bit in the register, resetting SMPL_EN bit to 0. For the details, refer to the SPML technical description in the RTC.

WTSR

WTSR (Watchdog Timeout and Software Resets) event would keep the PMIC on and reset all type-O registers. WTSR is powered from coin battery. It is disabled by default. If WTSR_EN is set to 1 (enabled), PMIC will be kept on and PWRHOLD falling edge will pull RESETB low and will trigger a 58.6ms timer. After 58.6ms timer expires, RESETB is released high. In addition, PWRHOLD falling edge does also initiate a WTSR timer, 250msec, 500msec, 750msec and 1000msec (default), 4 options, the default on supplies are still kept ON with the POR value until the WTSR timer expires, regardless of PWRHOLD signal. However, the default ON supplies are OFF if the PWRHOLD is held high after the WTSR timer expires. For details, refer to the WTSR section.

RTC Alarm

RTC Alarm signals (RTCA1 & RTCA2) can wake up the PMIC once the alarm triggers. These alarm signals do no power down the PMIC.

PWRHOLD

The PWRHOLD is the signal coming from the AP to hold the default-on supplies on in the initial power-on mode and keep the PMIC on.
For the global shutdown in BATTOK=High, pull the PWRHOLD low to turn off all rails in the PMIC.

Power OFF Events

This document uses the term of “global shutdown” to refer to any event that causes a shutdown of all regulators and reset all type-O registers within the PMIC.

Global Shutdown Events with automatic sequenced wakeup

The following events can initiate “ globle shutdown and automatic wake-up”. The events in this category are associated with faulty system states where the system may not be working properly but the system could potentially recover by powering down the processor, resetting all type-O registers, then powering up the processor again.

- Manual Reset (MRSTB1&2=LOW > 7sec typ)
- SMPL Event (BATTOK=High before the timer expires)

Note that In this SMPL event, the immediate shutdown occurs in BATTOK=L and the sequenced power-on in BATTOK=H prior to the timer timeout.

Global Shutdown Events to the OFF state

The following events can initiate “globle shutdown to the OFF state”. The events in this category are associated with undesireable system states that may occur in a “normal” functions product. Powering down the processor and resetting all type-O registers helps the system resolve these undesireable events. In general, a wake-up event such as PWRON=High / JIGONB=Low is required to power up the PMIC again. It is possible for the system software to program a wake-up event based on an RTC alarm.

- PWRHOLD=Low when PWRON=Low/JIGONB=High and PMIC=ON
- PWRHOLD=High after WTSR timer expires
- BATT rising UVLO threshold detected after the SMPL timer expires

Global Shutdwon Events with Immediate Shutdown

The following events can initiate an “immdediate shutdown”. The events in this category are associated with potentially hazardous system events. Powering down the processor and resetting all the type-O registers helps mitigate any issues that may occur due to these potentially hazardous system events. In general, a wake-up event such as PWRON=High / JIGONB=Low is required to power up the PMIC again.

- Thermal protection ($T_{Junction}$ > 165°C)
- V_{BATT} < V_{BATT} ($V_{BATTUVLO}$) Fault
- OUT3 POK=Low

ON/OFF Sequence Control in the initial Power-On Mode

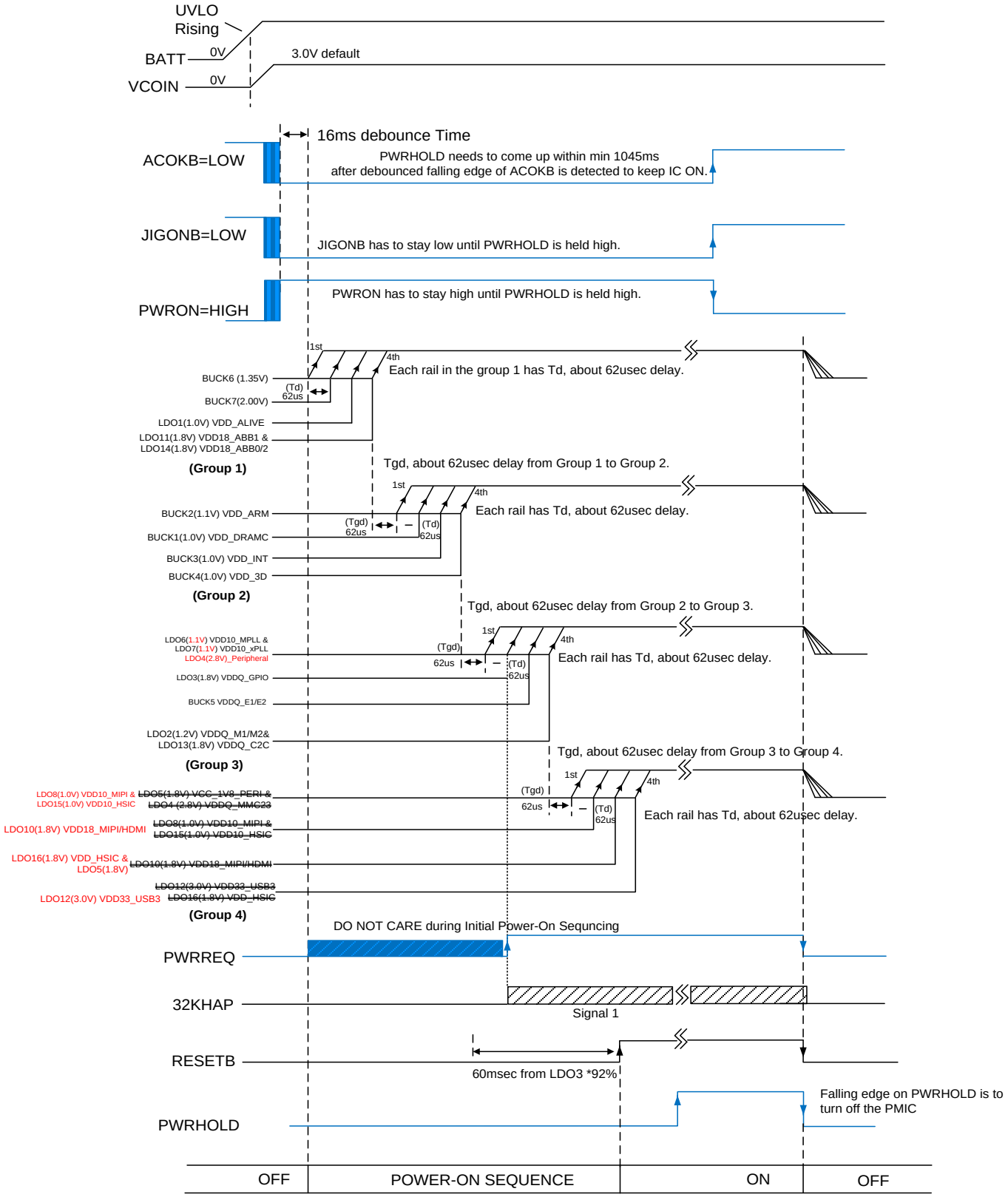
The on-delay (Td) for each power rail, group on-delay (Tdg) and off-delay (Tdoff) are also programmable via I2C. For the details about the sequencing, pls see the register below.

ONOFFDELAY Configuration

Address (hex)	**MODE**		Type: S	**RESET: 0x00**
09	**R/W**			
BIT	**NAME**	**POR**	**Description**	
7:5	reserved	000	Write “000”	
4:2	GRDELAY	000	Program the delay time for each group 000: 62usec 001: 124usec 010: 240usec 011: 1msec 100: 2msec >100: 2msec	
1:0	ONDELAY	00	Program the delay for each power rail 00: 62usec 01: 92usec 10: 120usec 11: 240usec	

I2C serieal interface is enabled as soon as RESETB is held high.
REFOK = REF enable && (REF > 90%)
I2C Enable = REFOK && RESETB=HIGH

Power ON/OFF timing diagram in the Initial Power-On Mode



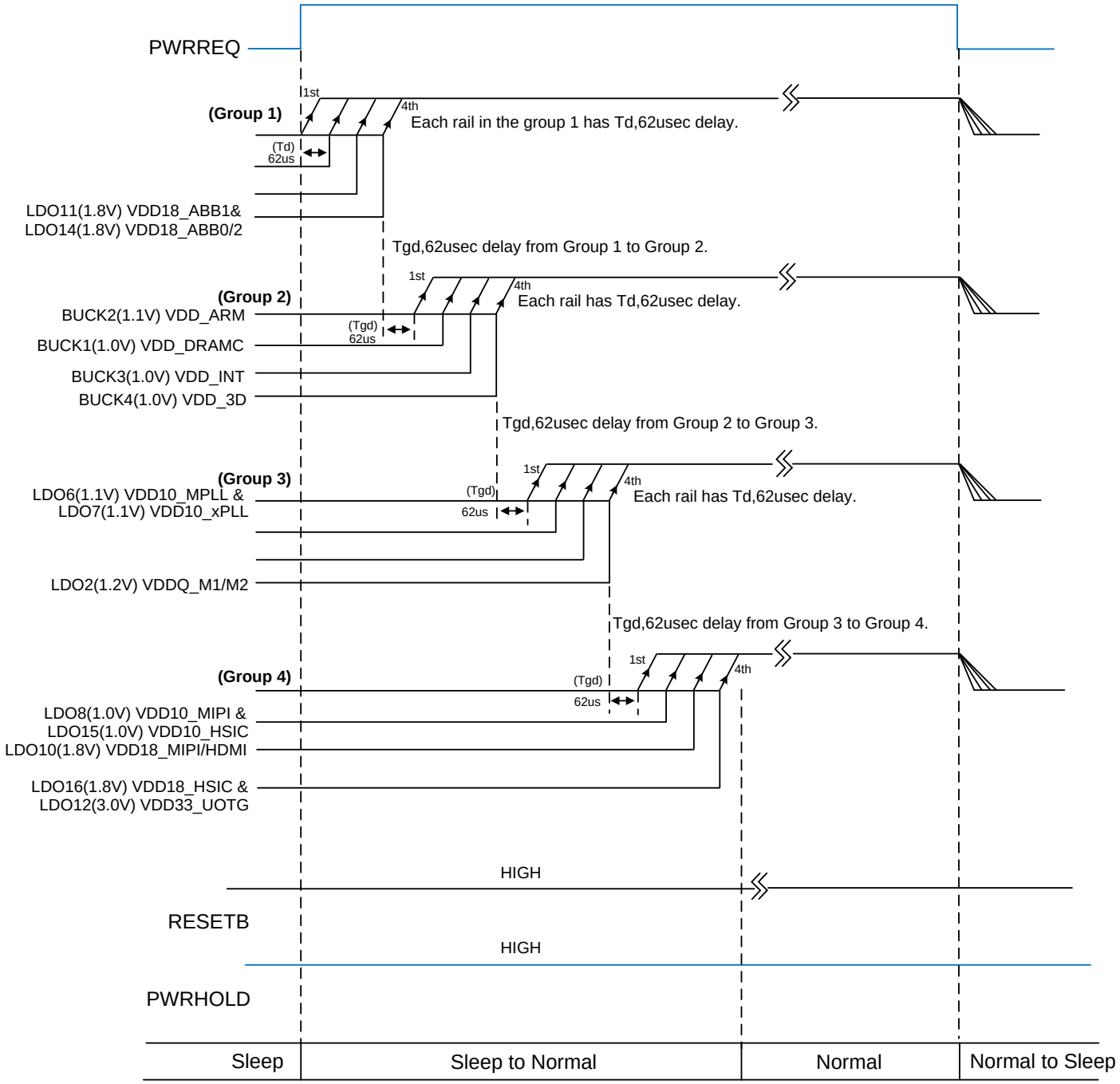
<Power ON/OFF Sequence in Initial Power-On>

Note that all type-O registers are reset to their POR in RESETB=LOW.
Note the signals in blue are ones from the processor or end-user.

The following table is the summary on the default-on supplies at the initial power-on mode.

Group	Order	Power	Default (V)	Note
1	1	BUCK6	1.35	
	2	BUCK7	2.00	
	3	LDO1	1.00	
	4	LDO11	1.80	
		LDO14	1.80	
2	1	BUCK2	1.10	
	2	BUCK1	1.00	
	3	BUCK3	1.00	
	4	BUCK4	1.00	
3	1	LDO4	2.8	
		LDO6	1.1	
		LDO7	1.1	
	2	LDO3	1.8	
	3	BUCK5	1.2	Based on VSETB51=VSETB52=LOW
	4	LDO2	1.2	Based on VSETB51=VSETB52=LOW
		LDO13	1.8	
4				
	1	LDO8	1.0	
		LDO15	1.0	
	2	LDO10	1.8	
	3	LDO5	1.8	
		LDO16	1.8	
	4			
		LDO12	3.0	

Power ON/OFF timing diagram by PWRREQ in PMIC=ON



Note that the signal in blue comes from the application processor.
Thses sequence is only effective when ON/OFF on all regulators above are assigned by PWRREQ=H/L.

ON/OFF Control by PWRREQ

PWRREQ Signal

Once the Application Processor (AP) boots up, the AP is able to power down and up key core supplies and other voltage rails via PWRREQ signal to enter / exit (deep) sleep mode. PWRREQ status is ignored during initial power up and down processes. All programming must be done before the AP enterns the sleep mode by pulling PWRREQ low since the AP does not have programming capability in (deep) sleep mode.

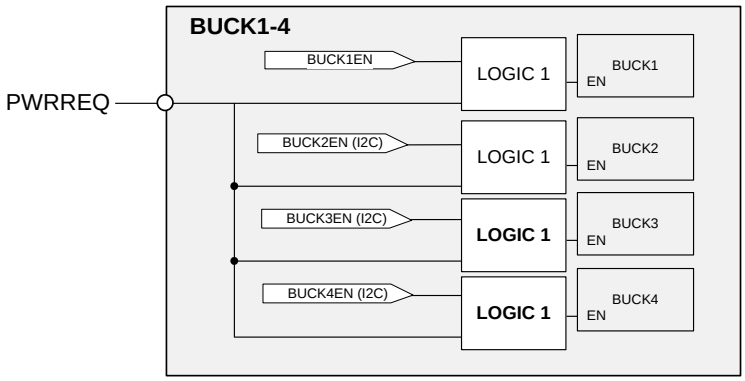
For those BUCKs or LDOs that are controlled by PWRREQ, the on-sequence follows the same on-sequecne at initial start-up mode, except for some regulators.

The default ON sequence is as follows.

Group	Order	Power-ON	Power-OFF	Default (V)	Note
1	1		Off at the same time		
	2				
	3	LDO11		1.80	
		LDO14		1.80	
	4				
2	1	BUCK2		1.10	
	2	BUCK1		1.00	
	3	BUCK3		1.00	
	4	BUCK4		1.00	
3	1	LDO6		1.1	
		LDO7		1.1	
	2				
	3				
	4	LDO2		1.2	By VSETB51=VSETB52=LOW
4	1				
	2	LDO8		1.0	
		LDO15		1.0	
	3	LDO10		1.8	
	4	LDO16		1.8	
		LDO12		3.0	

Control Scheme for BUCK1-4 by PWRREQ

All Buck1-4 have independent I^2C enable bits and external enable pin (PWRREQ). As shown in the figure below bits are logically ORed with the PWRREQ. The PWRREQ is typically connect to the dedicated pin on the Application Processor.



<ON/OFF Control Scheme by PWRREQ on BUCK1-4>

<LOGIC 1> Enable Mode Control on BUCK1,2,3,4 by PWRREQ
00: OFF (regardless of PWRREQ)

01: Output ON/OFF controlled by PWRREQ
PWRREQ=H (1) : Output ON
PWRREQ=L (0) : Output OFF
10: unused
11: ON (Regardless of PWRREQ)

Following is an example on how to control BUCK4 by the PWRREQ.

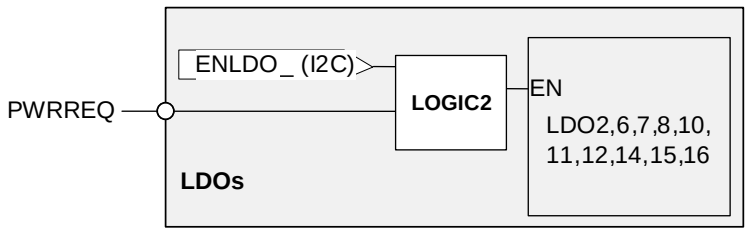
Example:
Once AP is booted up and running, start the programming via I^2C;

1. Write (0x12, 0x35, 0x09) → Attach the BUCK4 to PWRREQ-dependant control

Once the above programming is done the BUCK4 shuts down when the PWRREQ goes low and powers up when PWRREQ goes high with no effect to other voltage rail and RESETB output.

Control Scheme for LDOs by PWRREQ

For LDO2,6,7,8,10,11,12,14,15 and 16 have independent I^2C enable bits and hardware enable pins (PWRREQ). As shown in the figure below bits are logically ORed with the PWRREQ. The PWRREQ is typically connect to the dedicated pin on the Application Processor.



<ON/OFF Control Scheme by PWRREQ on LDO >

<LOGIC 2> Enable Mode Control on LDOs by PWRREQ

00: OFF (regardless of PWRREQ)

01: Output ON /OFF controlled by PWRREQ
PWRREQ=H (1) : Output ON in Normal Mode
PWRREQ=L (0) : Output OFF
10: Output ON with Low Power Mode by PWRREQ
PWRREQ=H (1) : Output ON in Normal Mode
PWRREQ=L (0) : Output ON in Low Power Mode
11: ON in normal mode (Regardless of PWRREQ)

Register Power-On Reset (POR)

Power-On Reset (POR) occurs by any power-off events. This shutdown causes RESETB=LOW. This condition resets all previously programmed values in the O-Type registers to their POR value.
But, all S-type registers are only reset when VCOIN are below its UVLO threshold.

Reset Output (RESETB) Assertion and De-Assertion

In the initial power-on sequencing, a 60ms reset timer is started after LDO3 POK=High. At the completion of the 60ms reset timer, RESETB goes high (based on no other circuit pulls low on this WIRED-OR output). After RESETB is asserted high; the default-on supplies will be maintained ON as long as PWRHOLD=High. Note that PWRON/JIGONB must be set to an appropriate status until PWRHOLD is able to keep all default-on regulators on in the initial power-on mode.

If V_{OUT3} voltage drops below 82% of its regulation voltage (OUT3 POK=Low), the PMIC shuts down immediately.
RESETB is an open drain output with an external pull-up resistor, 14k typical, to the OUT3 on PCB.
RESETB output is forced low when one or more of the following conditions occur;

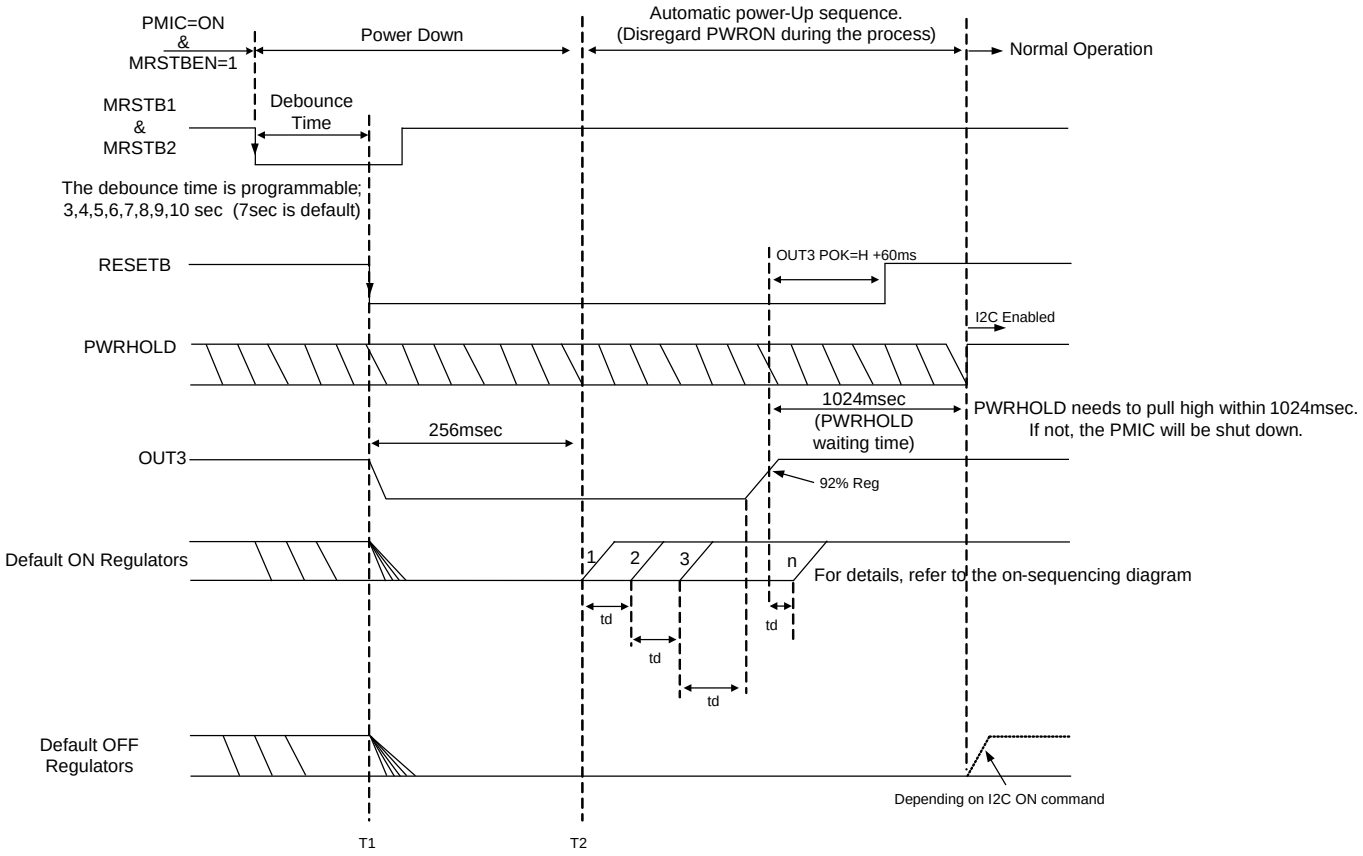
1. MRSTB1 and MRSTB2=Logic Low with 7sec (default)
2. OUT3 POK=Low
3. Thermal protection ($T_{Junction}$ > 165°C)
4. V_{BATT} Fault < ($V_{BATTSUVLO}$)
5. SMPL Event
6. PWRHOLD=LOW by AP
7. PWRHOLD=LOW in SMPL

When the RESETB is held low, all O-type registers are reset to their default values.

Manual Reset (MRSTB)

MRSTB is the hard manual reset process in normal operating mode by both MRSTB1 and MRSTB2=Low with a preset debounce time while the MRSETEB bit is set to 1, enabled. This bit is enabled by default. The debounce time is programmable from 3 sec to 10 sec, 1 sec increments, over I2C. After the debounce timer is expired, RESETB is held low and all type-O registers and serially-set voltage settings return to their default values. Once it enters the automatic power up sequence, the PMIC disregards another MRSTB 1&2=LOW signal and completes the cycle of power up sequence. Refer to the timing diagram below for the hard manual reset process.
MRSTB has a high priority over the watchdog function. It means that This manual reset process occurs even though WTSR_EN is set to 1. All default-on regulators must remain off for 256msec even in WTSR_EN set to 1. MRSTB is not a booting source to initiate the power-on sequence in the PMIC off.
If the manual reset function is not used, connect MRSTB1 and MRSTB2 to OUT3.
The following is the simplified logic diagram for the manual reset.

The details about the power-down and reboot-up process is depicted as below.
Note that the manual reset circuit detects the falling edge of those two pins and then counts the debounced timer. For example, if two pins are held low for 14sec for some reason, the manual reset happens only one time since a signle falling edge is detected.



<Manual Reset Timing Diagram by both MRSTB1 & MRSTB2=LOW>

OTP option for the PWRHOLD waiting time: 512msec, 768msec, 1536msec.

Time stamp T1: all pre-set voltages on the Type-O registers are reset to the default valve.
Time stamp T2: all default-on supplies will be on with their default valve.

Current Mode BUCK Converters, BUCK2, 3 & 4

Feature

- 32µA Quiescent Current in Normal Mode (BUCK2 & 4)
- 16µA Quiescent Current in Normal Mode (BUCK3)
- 5µA Quiescent Current in Low-Power Mode
- 5A with differential remote sense (BUCK2 & 4)
- 2.5A with differential remote sense (BUCK3)
- Small 1.0µH Inductors
- No External MOSFETs, Synchronous Rectifiers or Current Sense Resistors are Required
- Dynamically Programmable Output Voltage
- Programmable Output Voltage Slew Rate during dynamic voltage changes.
- Low-Power Mode Increases Light-Load Efficiency
- Forced PWM Operation Selectable through Serial Interface
- Remote Output Voltage Sensing
- ±1% Steady-State Accuracy
- Soft-Start into Pre-Biased Output

Detailes Description

The MAX77686A features two ultra-low I_Q step-down regulators.
In normal operation, BUCK2 & 4 step-down regulators consume only 32µA of quiescent current while BUCK3 consumes 16µA of quiescent current. In standby mode, the quiescent current is reduced to 10µA per step-down regulator. Each step-down regulator can be independently put into standby mode by writing a bit in a control register. Each step-down regulator provides internal feedback, minimizing external component count by allowing all step-down regulator output voltages to be programmed through the serial interface. These three step-down regulators feature dynamic voltage scaling through (DVS3/2/1) through the external DVS3/2/1 and SELB4/3/2 interface. Additionally, these three step-down regulators automatically transition from PFM to PWM operation (FPWM=0). Forced PWM operation can be independently enabled for each step-down regulator by setting FPWM. Each phase of BUCK2 and 4 is interleaved.

Soft-Start

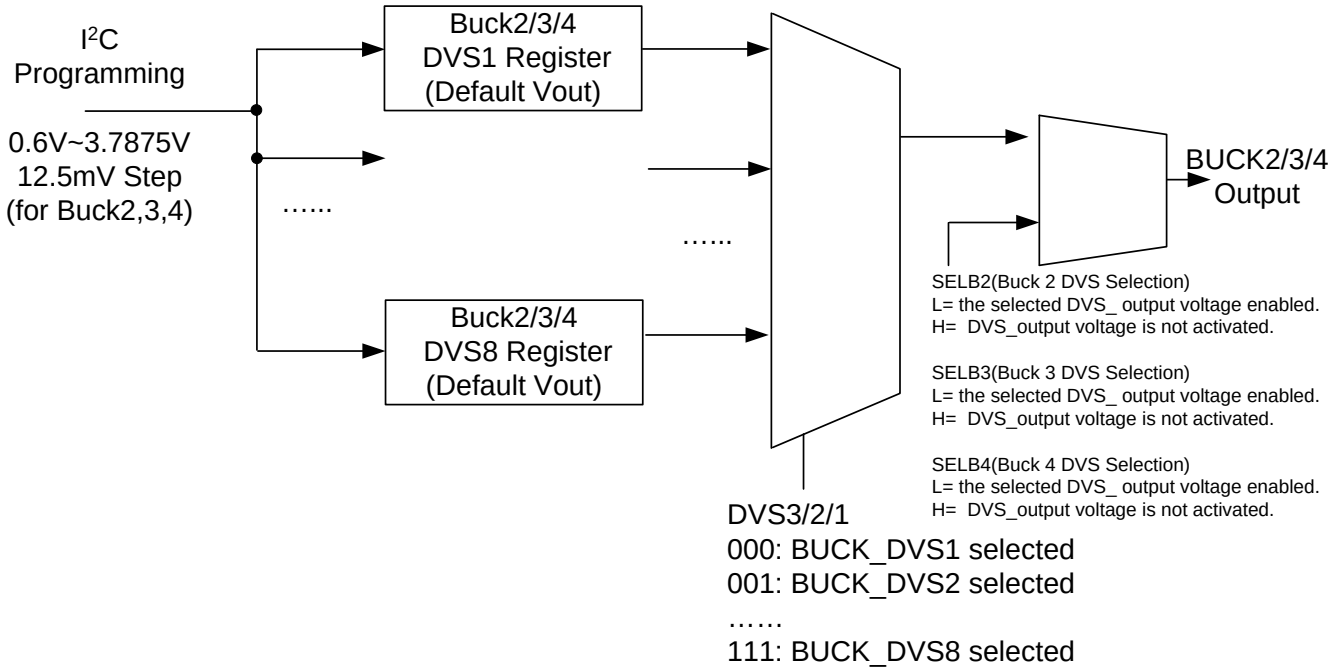
The step-down regulators have a soft-start rate of 25mV/us (dV/dt). When a step-down regulator is enabled, the output voltage ramps to its final voltage with a slew rate of 25mV/us. The controlled soft-start rate and the step-down regulator current limit (I_{LIMP}) limit the input inrush current to the output capacitor (I_{INRUSH}). I_{INRUSH}=min(I_{LIMP} & C_{OUT}*dV/dt). Note that the input current on the step-down converter will be lower than the inrush current to the output capacitor by the ratio of output to input voltage.
The step-down regulators support starting into a pre-biased output. For example, if the output capacitor has an initial voltage of 0.4V when the regulator is enabled, the regulator gracefully increases the capacitor voltage to the required target voltage such as 1.0V. This is unlike other regulators without the start into pre-bias feature where they may force the output capacitor voltage to 0V before the soft-start ramp begins.

Example: What is the inrush current when starting BUCK2 with an output capacitance (C_{OUT}) of 22uF?

- I_{INRUSH}=min(I_{LIMP} & C_{OUT}*dV/dt).
- BUCK2 is a two phase regulator with a typical PMOS current limit (I_{LIMP}) of 3.75A per phase. For I_{LIMP} in the above equation we will use 2x3.75A=7.5A.
- BUCK2 has a typical soft-start rate (dV/dt) of 25mV/us. For dv/dt in the above equation we will use 25mV/us.
- I_{INRUSH}=min(7.5A & 22uF*25mV/us).
- I_{INRUSH}=min(7.5A & 0.55A).
- I_{INRUSH}=0.55A

Dynamic Voltage Scaling (DVS)

Buck 2, 3 and 4 include DVS feature that allows each output voltage to change dynamically.
The Buck 2 and 4 output voltage is selected by DVS1-3 and SELB2/4. See the table below.



To have a specific voltage in the DVS mode, both DVS3/2/1 and SELB2/3/4 need to be set accordingly.
In the initial power on Mode, the output on these three regulators is set by each BUCK_DVS1 register since all DVS3/2/1 stay at low.
In order to have a pre-set output in DVS scheme, the SELB_ must be set to Low. If this stays low, a previous set voltage is only valid on each regulator.

Remote Output Voltage Sensing (ROVS)

BUCK2/3/4 feature remote output voltage sensing (ROVS) for improved output voltage accuracy. The SNSxN and SNSxP inputs connect directly across the load, with the SNSxN pin connected to a quiet analog ground near the load, and SNSxP connected directly to the load's power input. The ROVS can be independently disabled through software order to reduce quiescent current consumption (ROVS_EN_Bx). Disabling the ROVS reduces the quiescent current consumption. When BUCK2/3/4 is placed in low power mode, the ROVS is automatically disabled. Although the ROVS is automatically disabled, the ROVS_EN_Bx bits are not be automatically cleared.
If ROVS_EN_Bx is set when BUCK2/4 enters normal power mode, the ROVS feature will automatically re-enable.

Inductor Selection

BUCK2 and 4 operate with two 1.0uH inductors and BUCk3 operates with one 1.0uH inductor. Reduce the inductor's series resistance for maximum efficiency.

MANUFACTURER	SERIES	INDUCTANCE (uH)	DC RESISTANCE (mohms typ)	CURRENT RATING (A) -30% (ΔL/L)	CURRENT RATING (A) ΔT=40ºC rise	DIMENSIONS L x W x H (mm)
TOKO	DFR252010-1R0	1	50	3.5	3.1	2.5x2.0x1.0
TOKO	DFE252010-1R0	1	78	2.7	2.5	2.5x2.0x1.0
TOKO	DFE201610-1R0	1	96	2.2	2.0	2.0x1.6x1.0
TDK	TFM252010-1R0	1	54	3.5	2.5	2.5x2.0x1.0
TDK	TFM201610-1R0	1	60	2.5	2.2	2.0x1.6x1.0
CYNTEC	PIFE25201T-1R0MS	1	41	4.5	3.5	2.5x2.0x1.0
Murata	LQM2HPN1R0MGHL08	1	48	2.2	2.9	2.5x2.0x1.0

Input Capacitor Selection

The input capacitor, C_{IN}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications a 10μF capacitor is sufficient.

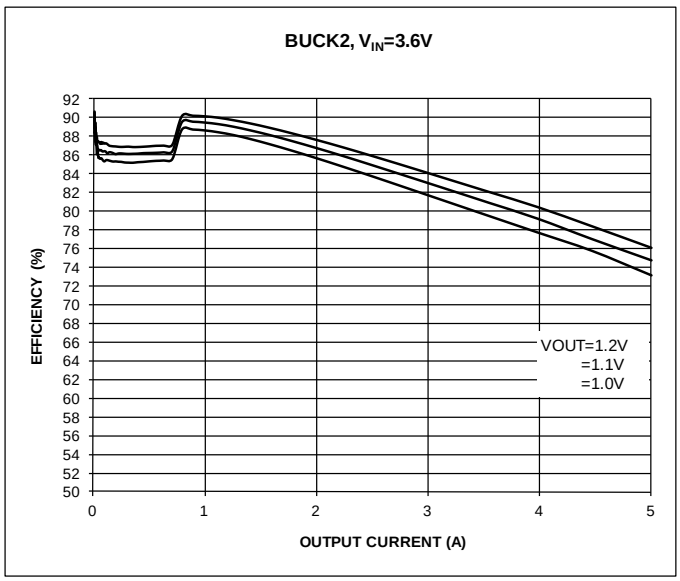
Output Capacitor Selection

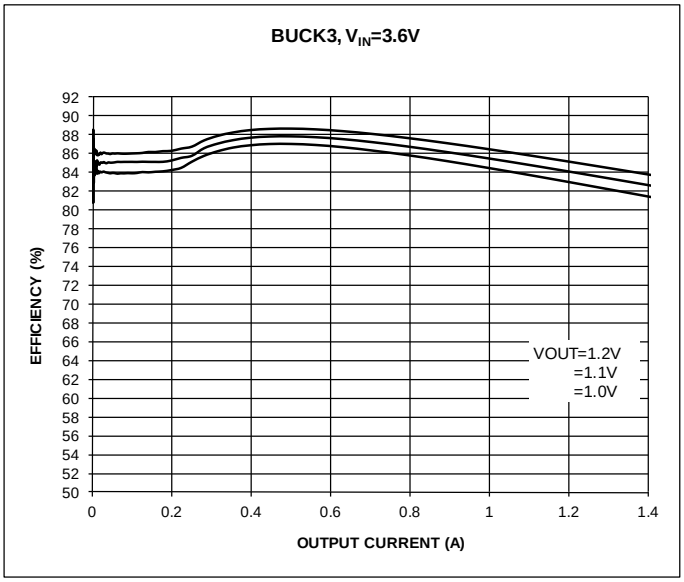
The output capacitor, C_{OUT}, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. The recommended valuses are summarized in the following table.

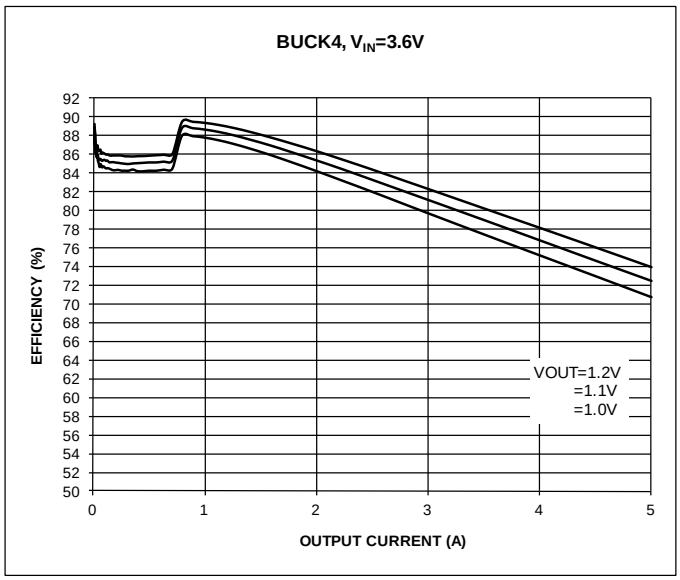
Regulator	Capacitance
BUCK2	2x 22(μF)
BUCK3	22(μF)
BUCK4	2x 22(μF)

Efficiency Graphs on Buck2,3,4

The efficiency graphs were measured with TOKO DFE252010-1R0.







Hysteresis BUCK Converters, BUCK1,5,6,7,8 & 9

Feature

- 25μA Quiescent Current in Normal Mode
- 1.5A for BUCK1, 5, 6, 7, 8 & 9
- BUCK5 has two external pins to set the default for a different type of memory
- A 1.0μH Inductor on all BUCKs
- No External MOSFETs and Synchronous Rectifiers are Required
- Forced PWM Operation Selectable through Serial Interface
- ±3% Steady-State Accuracy
- Soft-Start

Setting the default on BUCK 5

The default on BUCK5 is set to one of four options by VSETB51 and VSETB52.

VSETB51	VSETB52	OUTPUT (V)
0	0	1.2
0	1	1.35
1	0	1.5
1	1	1.8

0: refer to logic low, typically connected to ground.
1: refer to logic high, typically connected to BATT.

Over-write any programmable voltage via the I2C is also possible once the default is settled down.

Inductor Selection

The MAX77686A step-down converters operate with inductors of 1μH to 4.7μH. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. The inductor's DC current rating only needs to match the maximum load current of the application +100mA because the MAX77686A step-down converters feature zero current overshoot during startup and load transients.
For optimum voltage positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range. For higher efficiency at heavy loads (above 200mA) or minimal load regulation (but some transient overshoot), the resistance should be kept below 100mΩ. For light load applications up to 200mA, much higher resistance is acceptable with very little impact on performance.

Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (uH)	DC RESISTANCE (mohms typ)	CURRENT RATING (A) -30% (ΔL/L)	CURRENT RATING (A) ΔT=40ºC rise	DIMENSIONS L x W x H (mm)
TOKO	DFR252010-1R0	1	50	3.5	3.1	2.5x2.0x1.0
TOKO	DFE252010-1R0	1	78	2.7	2.5	2.5x2.0x1.0
TOKO	DFE201610-1R0	1	96	2.2	2.0	2.0x1.6x1.0
TDK	TFM252010-1R0	1	54	3.5	2.5	2.5x2.0x1.0
TDK	TFM201610-1R0	1	60	2.5	2.2	2.0x1.6x1.0
CYNTEC	PIFE25201T-1R0MS	1	41	4.5	3.5	2.5x2.0x1.0
Murata	LQM2HPN1R0MGHL08	1	48	2.2	2.9	2.5x2.0x1.0

Output Capacitor Selection

The output capacitor, C_{OUT}, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. The recommended valuses are summarized in the following table.

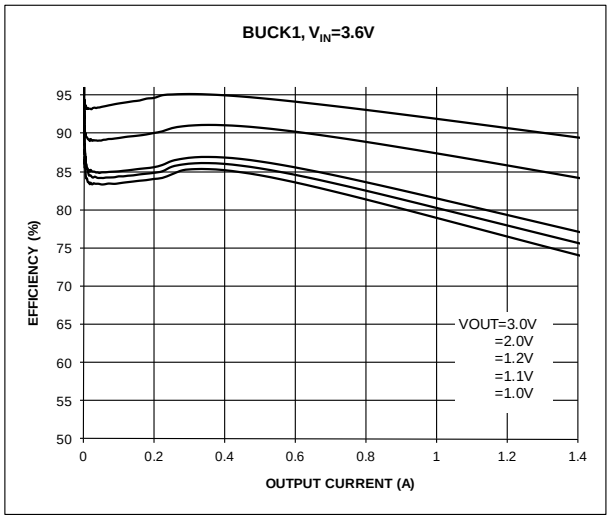
Regulator	Capacitance (μF)
BUCK1	4.7
BUCK5	4.7
BUCK6	4.7
BUCK7	4.7
BUCK8	4.7
BUCK9	4.7

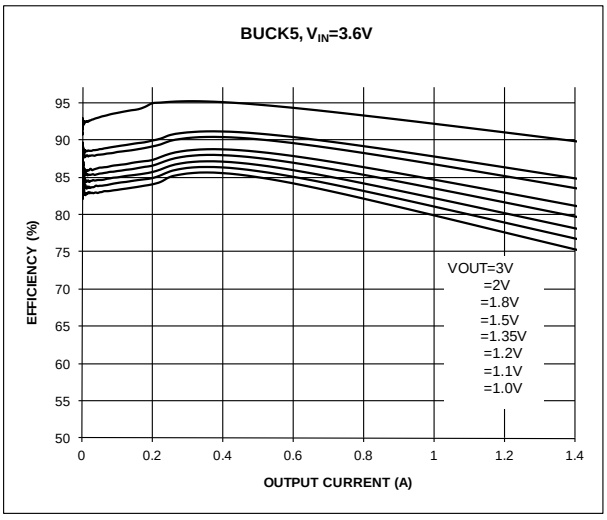
Input Capacitor Selection

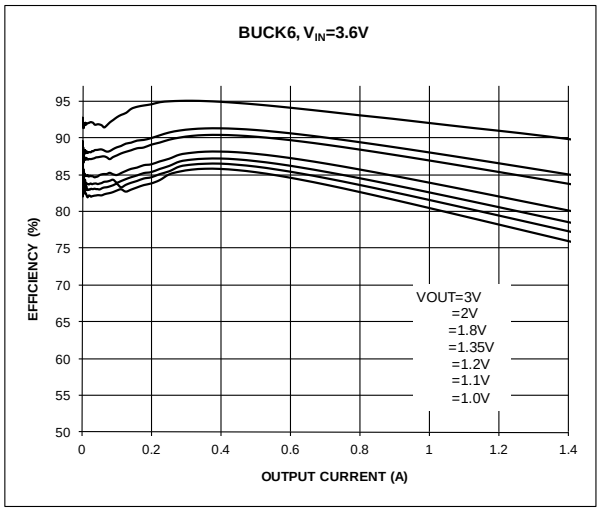
The input capacitor, C_{IN}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the MAX77686A step-down converter's fast soft-start, the input capacitance can be very low. For most applications a 2.2μF or 4.7μF capacitor is sufficient.

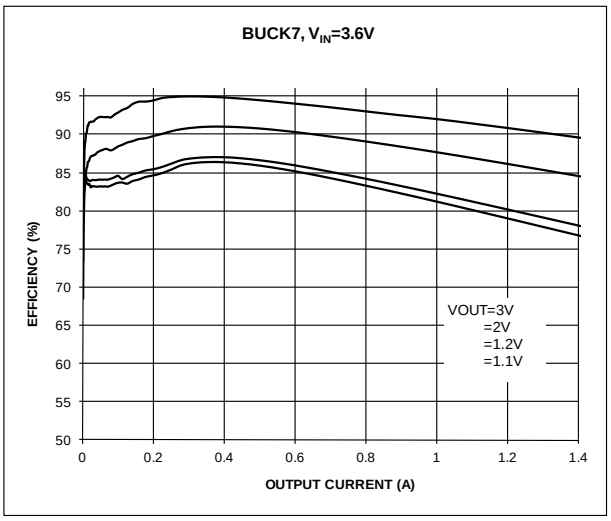
Efficiency Graphs on Hysteresis Bucks

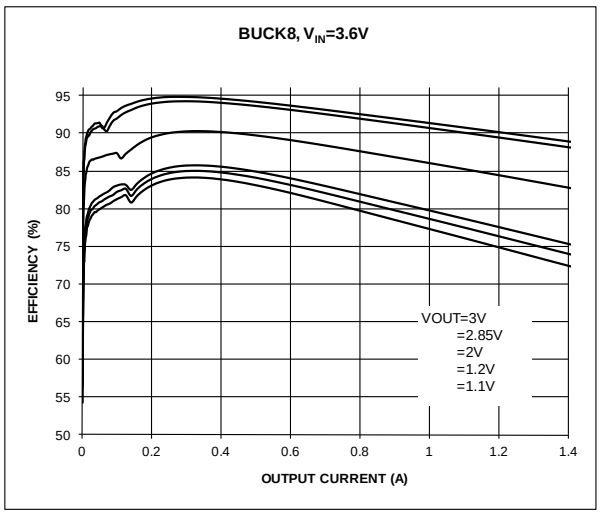
The efficiency graphs were measured with TOKO DFE201610-1R0.

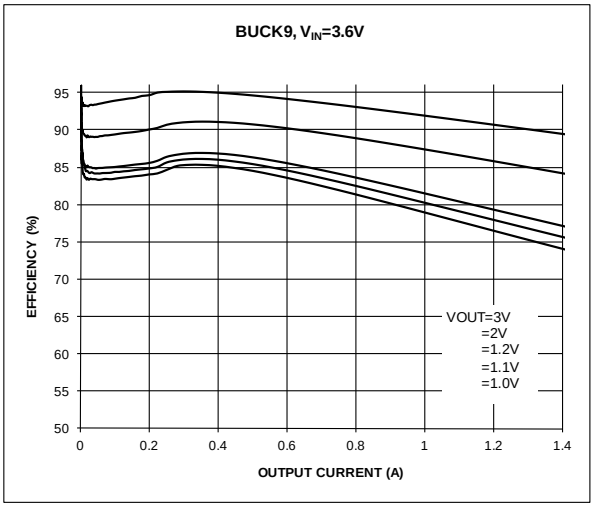












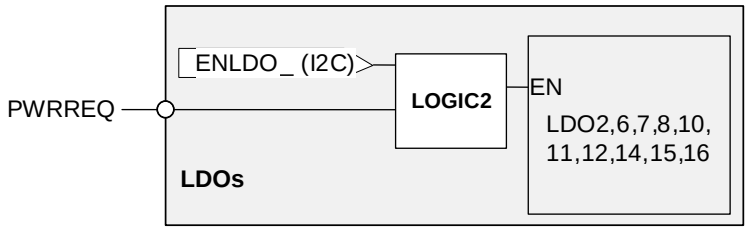
Linear Regulators

Feature

- 22µA Quiescent Current in Normal Mode (LDO2)
- 20 µA Quiescent Current in Normal Mode (300mA LDOs)
- 18 µA Quiescent Current in Normal Mode (150mA LDOs)
- 1µA Quiescent Current in Low Power Mode
- Soft-Start
- Low Drop-Out Voltage, 50mV typ at full load

Control Scheme for the LDOs by PWRREQ

For LDO2, 6,7,8,10,11,12,14,15 and 16 have independent I^2C enable bits and hardware enable pins (PWRREQ). As shown in the figure below bits are logically ORed with the PWRREQ. The PWRREQ is typically connect to Application Processor's GPIOs.



<ON/OFF Control Scheme by PWRREQ on LDO >

<LOGIC 2> Enable Mode Control on LDOs by PWRREQ

00: OFF (regardless of PWRREQ)

01: Output ON /OFF controlled by PWRREQ
PWRREQ=H (1) : Output ON in Normal Mode
PWRREQ=L (0) : Output OFF
10: Output ON with Low Power Mode by PWRREQ
PWRREQ=H (1) : Output ON in Normal Mode
PWRREQ=L (0) : Output ON in Low Power Mode
11: ON in normal mode (Regardless of PWRREQ)

Control Scheme for non-PWRREQ LDOs

For LDOs,LDO1, 3, 4, 5, 9, 13, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26 that are not ON/OFF by PWRREQ, the logic table is as below.

7:6	OPMODE		00: OFF, except LDO3. LDO3 is always ON. 01: ON in Low Power Mode 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode**

The LDO20, LDO21 and LDO22 with the external pin, ENL20, ENL21 & ENL22

LDO20, LDO21 and LDO22 have its own external pin, ENL20, ENL21 & ENL22, to enable/disable the output.
The control of enabling the LDOs is OR gate by either I2C=ON or ENL20/ENL21/ENL22=High.
Refer to the registers for the details.

7:6	OPMODE		00: OFF (when ENL2x is Low) 01: ON in Low Power Mode 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode (Regardless of ENL2x status)**

Low Power Mode

Each regulator includes a low-power mode where the quiescent current drop to only 1μA.

Soft-Start and Dynamic Voltage Change

When a regulator is enabled, the output voltage ramps to the final voltage at the slew rate of 100mV/μs.
The 100mV/μs ramp rate results in around 220mA inrush current with a 2.2μF output capacitor and no load, but achieves regulation within 50μs. The soft-start ramp rate is also the rate of change at the output when switching dynamically between two output voltages without disabling.

Active-Discharge

Each LDO regulator has an active-discharge resistor that can be enabled/disabled with the ADSLDOxx bit.
This is enabled by default. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. The default condition of the active-discharge resistor feature is enabled such that whenever BATT is below its UVLO threshold all regulators will be disabled with their active discharge resistors turned on.

Overvoltage Clamp

Each LDO has an overvoltage clamp that allows it to sink current when the output voltage is above its target voltage.
This overvoltage clamp is default enabled but can be disabled with LxxOVCLMP_EN.

Adjustable Compensation

All PDRV LDOs that have a remote capacitor have adjustable compensation. This feature can be used to adjust the compensation of the LDO based on the resistance and inductance to the remote capacitor. This ability will allow each LDO to be programmed for optimal load transient performance based on the location of its remote capacitor. Please refer to the Control Register for more details. The LDO compensation should be switched only when that LDO is off. If the compensation switches when the LDO is enabled, it will cause unknown output glitches, due to switching in uncharged capacitors (as compensation changes).

LDO2's Default

the default on LDO2 is set to one of four options by VSETB51 and VSETB52

VSETB51	VSETB52	OUTPUT(V)
0	0	1.20
0	1	1.35
1	0	1.50
1	1	1.80

0: refer to logic low, typically connected to ground
1: refer to logic high, typically connected to BATT.

PCB Layout Guidelines

DC Power Distrbution Guidelines

Use wide trance for power supply lines. Use a multi plated VIA holes to connect power supply traces between layers.

PCB Trace Width vs. Current and Length
Adequate trace or fill area width is needed to limit the IR drop as current is routed across the board. An IR drop of 1% or less is strongly recommended between the regulator outputs and their loads. The typical way to calculate a minimum trace width is described below;

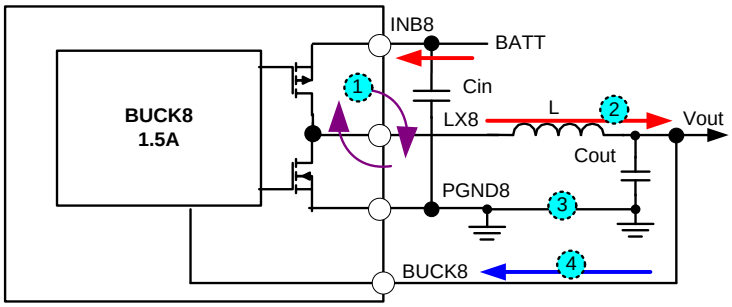
1. Deterine the maximum load current (Iload_max)
2. Know the regulator's target output voltage(Vout)
3. Calculate the maximum tolerable trace resistance (Rpcb_Max) assuming a 1% IR drop. Rpcb_Max=(0.01 x Vout) / Iload_max
4. determine accurate trace length (L) and the copper thickness (T); 1 ounce copper foil thickness is 1.34mil.
5. Calculate the minimum trace width (W) as;
   W = (p x L) /(Rpcb_max x T)
   where; p = the resistivity of copper (1.7×10^{-8} ohm-m)

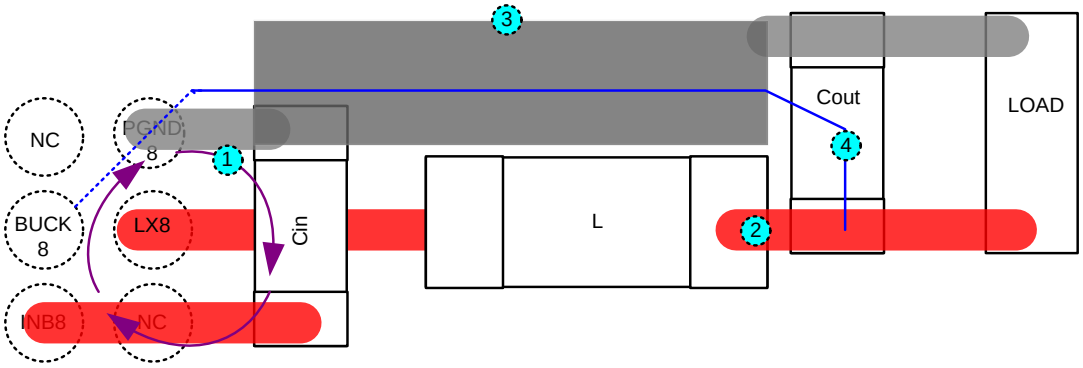
Guidelines for BUCK converters

Hyesteresis Buck Converter

All Hyesteresis buck converers on Max77686A have an input, output capacitor and inductor. These components must be placed in a right location to maximize the performance. To maximize the performance, two example PCB layouts for BUCK8 are depicted as below;

- The loop (1) is the most important in layout design. In order to reduce the loop impedance, place the input capacitor closer to the PMIC Pins (PGND and INB_).
- Feedback line does not have to be a thick trace.
- Connect the feedback line (Buck8) to the end of load.
- Place each output capacitor near its corresponding input capacitor to share a common layer ground.
- Use a thick trace for the main high current paths.

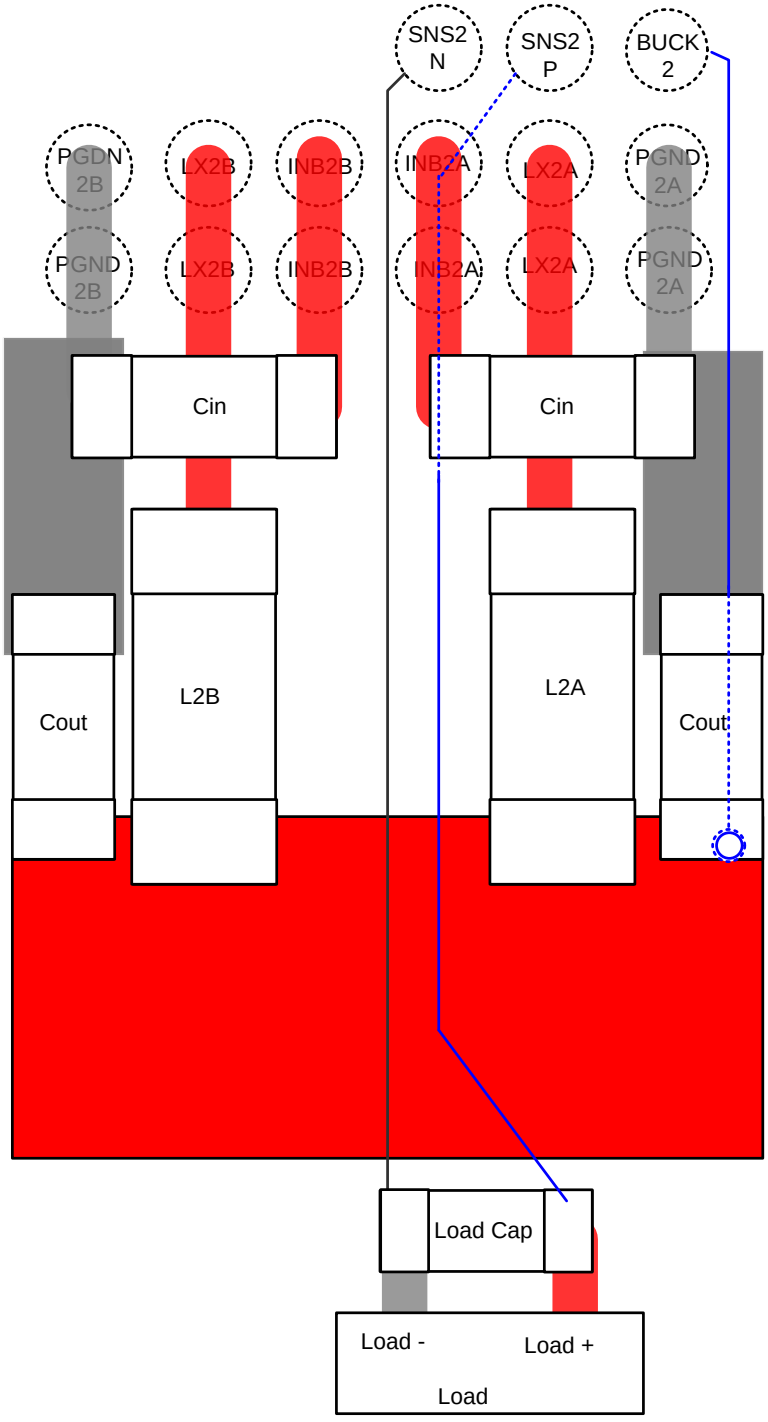




Current Mode Buck Converter

To maximize the buck performance, an example of PCB layout for Buck2 is depicted below.

- The loop (1) is the most important in layout design. In order to reduce the loop impedance, place the input capacitor closer to the PMIC Pins (PGND and INB_).
- Feedback line does not have to be a thick trace.
- Connect the sense + and - lines to the end of load.
- Place each output capacitor near its corresponding input capacitor to share a common layer ground.
- Use a thick trace for the main high current paths.



BACK-UP CHARGER

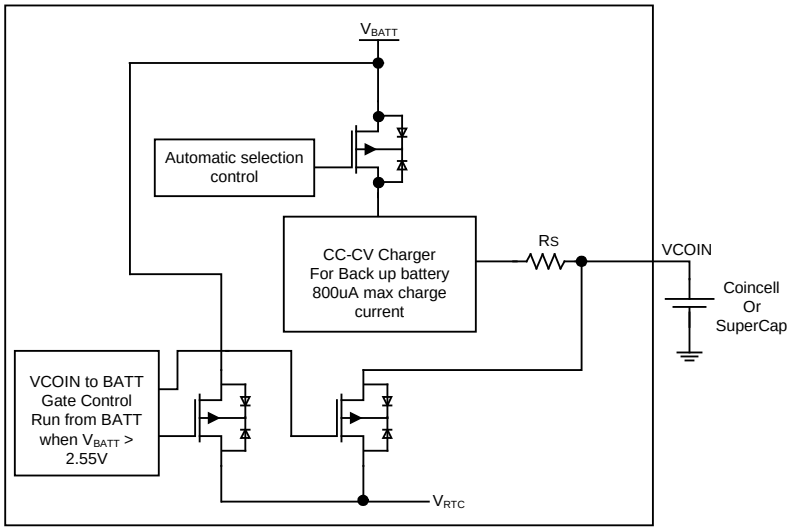
Features

- 800uA maximum CC-CV back up battery charger.
- 2.5V – 3.5V adjustable back up battery setting with ± 3% Tolerance

Description

The Back-up battery charger remains ON as long there is a valid power input source obn BATT and BBCHOSTEN bit is set to 1.

The backup battery charger is a voltage limited current source with a default 1kΩ output resistor. Backup Charger has an I2C adjustable output voltage in 2.5V, 3.0V, 3.3V, or 3.5V with 3.0V as the default output voltage. The power up default is ON. See the register section for details on how to adjust the output voltage.

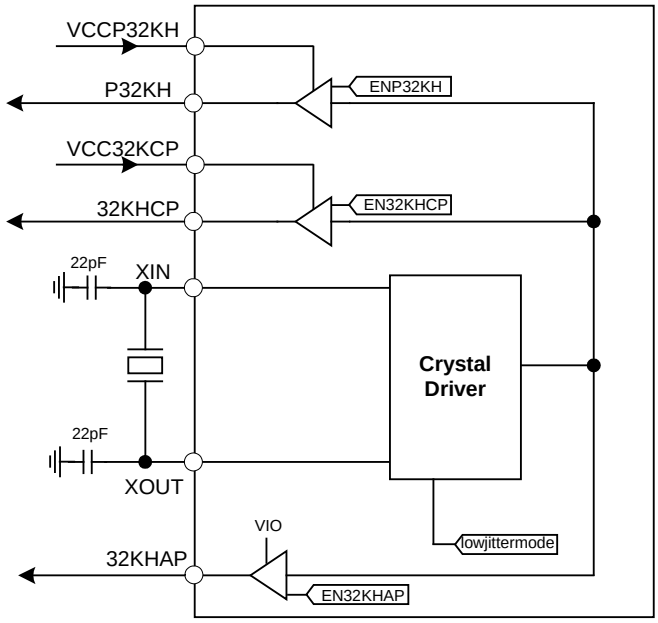


<Functional Block Diagram>

32KHz CRYSTAL OSCILLATOR

MAX77686A consists of a crystal driver with an external load capacitance. When the crystal driver is enabled, it starts up in low power mode, drawing only 1.5uA of current. The Lowjittermode bit controls the crystal driver in either low power mode or low jitter mode (high power mode). When the LowJittermode bit is set to 1, low jitter mode on three channels is activated at the same time. In the low-jitter mode, the current consumes about 30uA typically. In worse case, this current goes up to 50uA. These three 32khz buffer outputs (32KHAP, 32KHCP, P32KH) are independently enabled/disabled over I2C. However, the low-jitter mode on each output can not be applied. The crystal driver is supplied from the internal V_{RTC} node which is equal to V_{BATT} if V_{BATT} > 2.55V otherwise V_{RTC} is equal to V_{VCOIN}

The crystal driver will generate three channel 32k buffered outputs. The 32KHAP output is normally routed to the AP Processor. The other two outputs (32KHCP, P32KH) are intended for the BT,WLAN, BB or peripheral chipsets. The 32KHAP has a supply voltage of VIO supplied from OUT3 when VIO is connected to OUT3 externally while 32KHCP and P32KH supply voltage are provided by VCC32KCP and VCCP32KH respectively.



<32KHZ Crystal Oscillator Block Diagram>

IRQB Description

The MAX77686A uses the Interrupt pin, IRQB, to indicate to the application processor that the status on the MAX77686A has changed. The IRQB signal is asserted whenever one or more interrupts are toggled. The application processor shall read the interrupt source register to see the source of interrupt event. If the bit 0, RTC, in the register, INTSRC 0x01, is asserted high, it indicates the source of interrupt event from RTC section. In this moment, application processor should read the RTC interrupt register, RTCINT, 0x00, in the RTC slave address, 0x0C/0D.
Each Interrupt register can be read at a time. The IRQB pin becomes high (cleared) as soon as the read sequence finishes. If an interrupt is captured during the read sequence, the IRQB pin will become active (low) after minimum 24 clock cycle of I2C CLK. All interrupts can be masked to prevent the IRQB from being asserted for masked interrupts. A mask bit in the INTxMSK registers implements masking. The INT1 register can still provide the actual interrupt status of the masked interrupts. If the mask bit is cleared for an active interrupt, the IRQ goes low at the next falling edge of the 32KHz-clock output.

RTC Functional Description

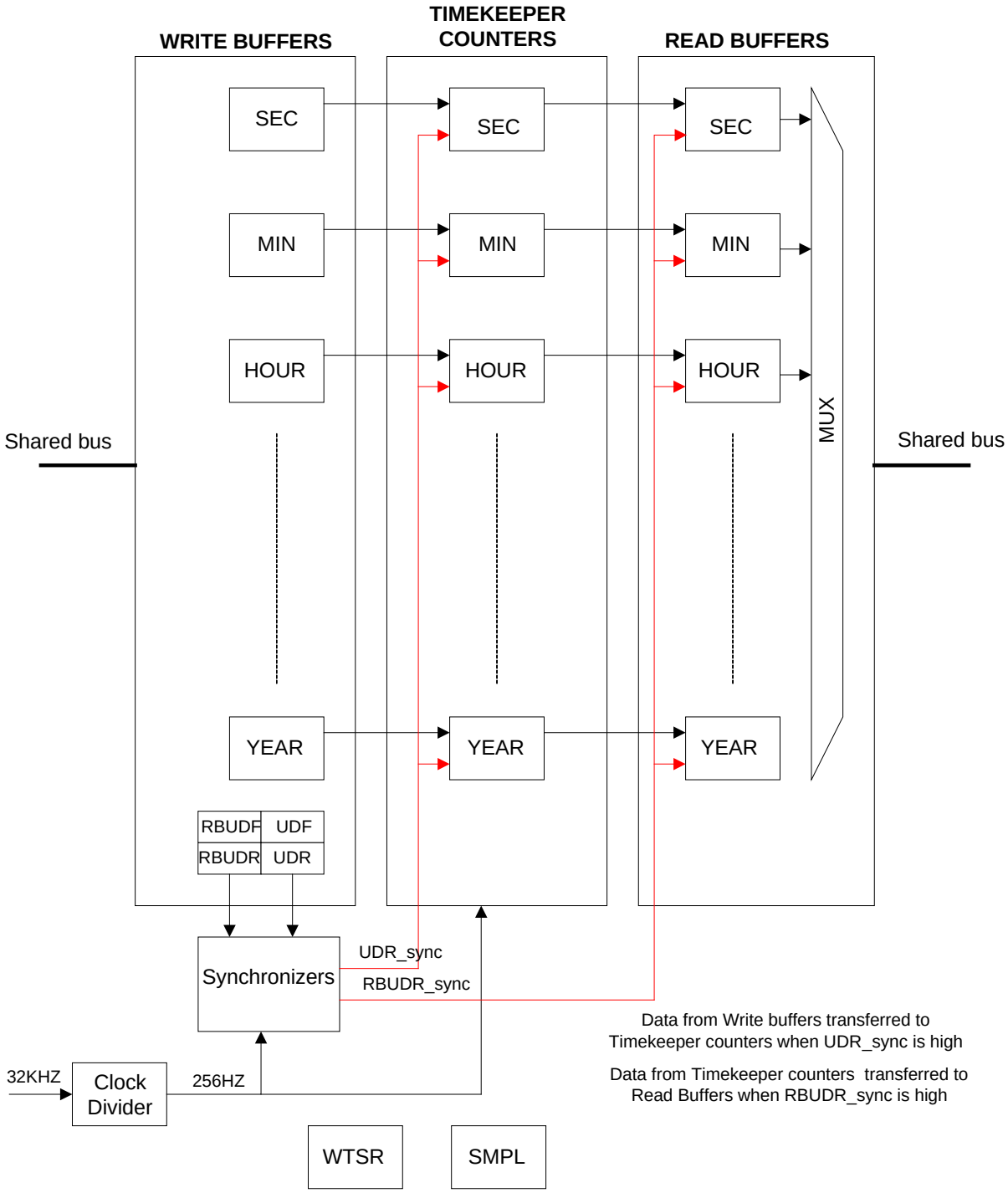
This Real-time clock (RTC) is responsible for keeping track of the time. It records seconds, minutes, hours, days, months and years with a calendar structure that accounts for leap years. The RTC is further equipped with two alarms and has a host of interrupt capabilities.

Through a set of control registers various modes of operation are possible. RTC supports both “Binary”, and “Binary Coded Decimal”, and supports features such as AM/PM, 24/12 modes of operation. Additional sudden momentary power loss (SMPL) and watchdog timeout and software reset (WTSR) are available.

Write/Read Operation

Before proceeding further, we need to get familiar with how a write to and a read from RTC is going to occur. The user uses I2C to interface with RTC registers. However, the I2C and RTC operate in totally asynchronous clock domains. For example, while I2C may operate at 400KHz, the main clock runs at 32.768 kHz. In addition to the fact that meta-stability may be introduced during a read or a write operation, other side effects such as a read error could occur. A read error may be observed when reading a single timing register (such as a SECOND register) as the register is changing its value. The other read error possibility occurs when reading multiple registers (such as a MINUTE and SECOND registers together) and one register value changes between the reads (such as SECOND register changing after it is already been read and the user is in process of reading the MINUTE register).
Therefore, it is needed to make sure that both writing to and reading from RTC happens as reliably as possible.
For this reason, two sets of independent buffers “Write Buffers”, and “Read Buffers” are implemented which are used for writing to and reading from RTC.

The following sections define how Write and Read are possible to/from RTC:



<RTC Block Diagram>

Writing to RTC

In order to safely write to various registers on-board the RTC, all RTC registers (except RTCINT register, bit 0 and 4 of UPDATE0 Register) have a corresponding “Write Buffer”. When the user writes to the RTC, the user is actually

performing a write to these “Write Buffers”. Therefore, in writing to RTC there are 2 steps needed to update a particular register or set of registers:

1. User writes desired value(s) to the register(s) located between 0x01 and 0x24. Behind the scene, only the “Write Buffers” are updated with these new values.
2. The user then writes a 1 to UDR bit 0 of the “UPDATE0 Register” at address 0x04 to transfer the modified “Write Buffers” to the corresponding time registers.

The logic subsequently would perform a transfer of data from Write Buffers to the actual registers and then clears *the* “UDR” bit automatically as well as clearing the Write Buffers (marking them as not modified). The user then has to either poll the UDF “UPDATE Flag” bit (bit 0 of UPDATE1 register), or rely on the interrupt to initiate a new write operation (The UDF is set to 1 as soon as the write operation occurs).

Pseudo code for setting clock to Saturday, Jan 01, 2011, 1:00:00 PM

```
Set RTCCNT to 0x01          //12hr mode, BCD mode
Set RTCSEC to 0x00          // 0 second
Set RTCMIN to 0x00          // 0 minute
Set RTCHOUR to 0x41         // 1 PM
Set RTCDOW to 0x40          // Saturday
Set RTCMONTH to 0x01        // January
Set RTCYEAR to 0x11         // 11
Set RTCDOM to 0x01          // First
Set RTCUPDATE0 to 0x01  // transfer write buffers to counters
Loop: Read RTCUPDATE1
If UDF is 0 then go back to Loop  //wait until UDF is set before initiating new write

Set RTCSEC to 0x…           //new write
```

Pseudo code for setting ALARM1 to every Wednesday at 7:30:00 AM

```
Set RTCCNT to 0x01          //12hr mode, BCD mode
Set RTCSECA1 to 0x80        //0 sec, enabled
Set RTCMINA1 to 0xB0        //30 minute, enabled
Set RTCHOURA1 to 0x87   //7 AM, enabled
Set RTCDOWA1 to 0x08        /Wednesday, enabled
Set RTCMONTHA1 to 0x00 //Disabled
Set RTCYEARA1 to 0x00       //Disabled
Set RTCDOMA1 to 0x00        //Disabled
Set RTCUPDATE0 to 0x01  // transfer write buffers to counters
Loop: Read RTCUPDATE1
If UDF is 0 then go back to Loop  //wait until UDF is set before initiating new write

Set RTCSEC to 0x…           //new write
```

Under the hood, the logic first does a double synchronization of the UDR bit to the 32.768 kHz clock before using it as an enable bit (UDR_sync in figure 1) to transfer from Write buffers to the actual registers thus allowing a safe update of these 2 unsynchronized clock events.

Reading from RTC

Corresponding to most timing registers there are a series of “Read Buffers”.

In order to safely read from various registers on-board the RTC, all RTC registers (except RTCINT register and bit 0 and 4 of UPDATE0 Register) have a corresponding “Read Buffer”. When the user reads from the RTC, the user is actually performing a read from these “Read Buffers”. Therefore, there are 2 steps needed to read a particular register or set of registers:

1. The user writes a 1 to RBUDR bit 4 of the “UPDATE0 Register” at address 0x04 to transfer the most timing registers to “Read Buffers”. Behind the scene, the “Read Buffers” are updated.
2. The user then reads from the desired register location.

After step 1, the logic subsequently would perform a transfer of data from the actual registers to the “Read Buffers” and then clears the “RBUDR” bit. The user then has to either poll the RBUDF “UPDATE Flag” bit (bit 1 of FLAG register), or rely on the interrupt to initiate a new write operation (The RBUDF is set to 1 as soon as the transfer operation occurs).

Pseudo code for reading the time

```
Set RTCUPDATE0 to 0x10  // transfer timekeeper counters to read buffers
Loop: Read RTCUPDATE1
If RBUDF is 0 then go back to Loop  //wait until UDF is set before initiating new write
Read RTCSEC            // second
Read RTCMIN            //  minute
Read RTCHOUR           //  hour
Read RTCDOW           // Day of Week
Read RTCMONTH         // Month
Read RTCYEAR          //  Year
Read RTCDOM            //  Day of Month
```

Pseudo code for reading ALARM1 setting

```
Set RTCUPDATE0 to 0x10  // transfer timekeeper counters to read buffers
Loop: Read RTCUPDATE1
If RBUDF is 0 then go back to Loop  //wait until UDF is set before initiating new write
Read RTCSECA1           //sec
Read RTCMINA1          //minute
Read RTCHOURA1         //hour
Read RTCDOWA1          // Day of Week
Read RTCMONTHA1        // Month
Read RTCYEARA1         //  Year
Read RTCDOMA1          //  Day of Month
```

Under the hood, the logic first does a double synchronization of the RBUDR bit to the 32.768 kHz clock before using it as a clock to transfer from the actual registers to the “Read Buffers” thus allowing a safe update of these 2 unsynchronized clock events.

SMPL (Sudden Momentary Power Loss) Function

The SMPL function can be used to initiate a power up sequence after momentarily loosing contact to the battery pack. If the PMIC is powered down and the battery voltage is below the UVLO threshold, a SMPL timer is started in the event that the SMPL_EN is set to 1.
If the battery voltage rises above the UVLO threshold before the SMPL timer expires, the PMIC is automatically booted up in sequence. If the battery UVLO rising threshold is detected after SMPL timer expires, the SMPL_EN bit is automatically set to the POR value, 0, in order to avoid a next coming SMPL event.
The following is the state diagram.

BATTOK=High before SMPL timer expires

If the SMPL_EN bit is set to 1 over the I2C, the PMIC monitors the status of BATTOK (UVLO Threshold). When the falling UVLO threshold of BATT is detected, the pre-set SMPL timer is initiated. The timer has 0.5s, 1.0s, 1.5s and 2.0s options where 1.0s is the default. If the rising UVLO threshold is detected before the SMPL timer expires.

BATTOK=High after SMPL timer expires

However, if the rising UVLO threshold is detected after SMPL timer expires, the SMPL_EN bit is automatically reser to the POR value, 0, in order to avoid a next coming SMPL event operation. In this mode, all power supplies are off due to no PWRHOLD active high. In order to power the PMIC on again, one of the power-on sources has to be applied.

WTSR (Software Reset) Function

The WTSR reset timer and software reset is used to ensure that the PMIC is keep on regardless of the PWRHOLD condition. The following is the state diagram for software reset function.

PWRHOLD is held high before WTSR timer expires

If the WTSR_EN is set to 1 over the I2C, the PMIC will monitor the status of PWRHOLD. When the falling edge of PWRHOLD is detected, the fixed 58.6msec RESETB timer and WTSR timer will be initiated. After the reset timer expires, the RESETB signal is held high. If the PWRHOLD is held high before the WTSR timer expires, the default-On supplies are kept on. Note that there is max 10msec internal delay to pull RESETB low since PWRHOLD went off.

PWRHOLD is held High/Low after WTSR timer expires

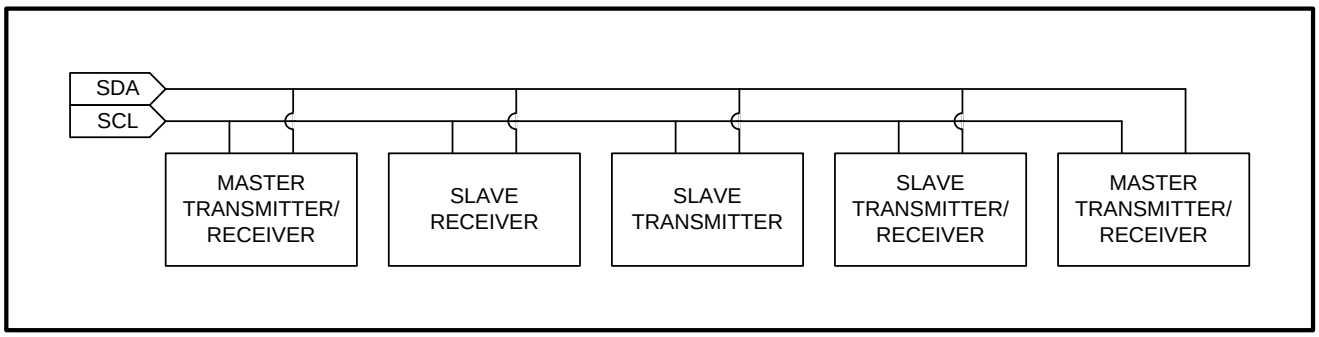
On the contrast, if the PWRHOLD signal is held high after the WTSR timer expires, the default-ON supplies will be off. The timing diagram is presented as below.
Note that there is max 10msec internal delay to pull RESETB low since PWRHOLD went off.

Serial Interface

An I^2C-compatible 2-wire serial interface is used for regulator on/off control, setting output voltages, and other functions. See for the complete register map.
The I^2C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I^2C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I^2C bus is a multi-master bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

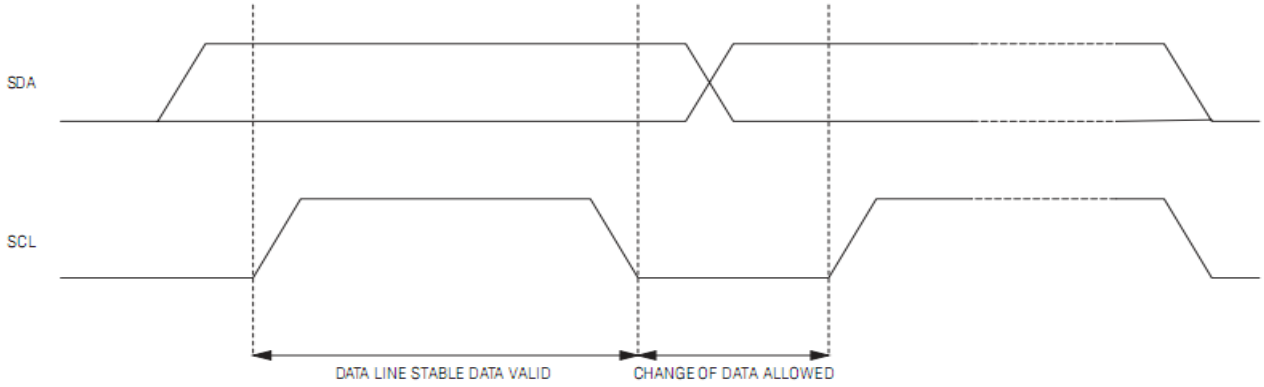


<Figure: Functional Logic Diagram for communications controller>

The figure above shows an example of a typical I^2C system. A device on the I^2C bus that sends data to the bus in called a "transmitter." A device that receives data from the bus is called a "receiver." The device that initiates a data transfer and generates the SCL clock signals to control the data transfer is a "master." Any device that is being addressed by the master is considered a "slave." When the MAX77686A I^2C compatible interface is operating in normal mode, it is a slave on the I^2C bus and it can be both a transmitter and a receiver.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of the SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

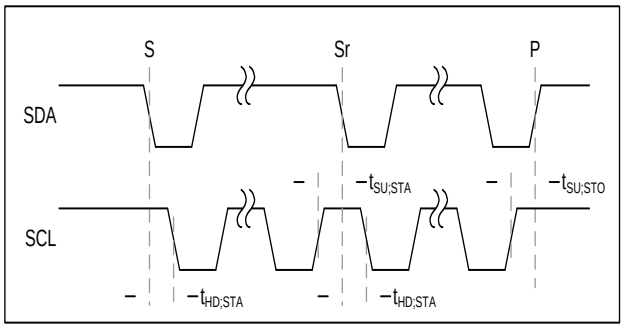


<Figure : I^2C Bit transfer>

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to MAX77686A. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition.



The STOP condition frees the bus. To issue a series of commands to the slave, the master may issue repeated start (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a repeated start command is functionally equivalent to a regular start command.
When a STOP condition or incorrect address is detected, MAX77686A internally disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feed-through.

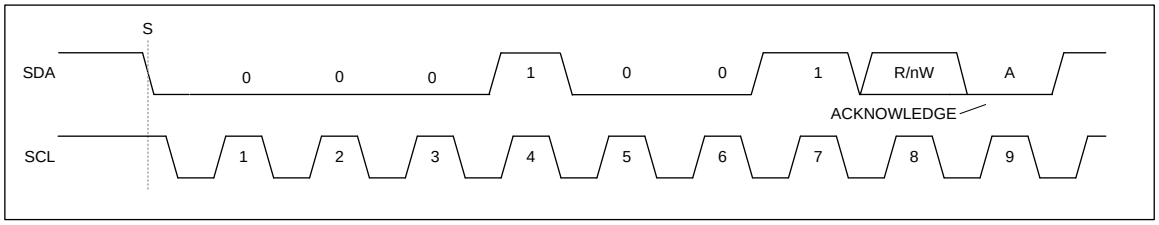
Acknowledge

Both the I^2C bus master and MAX77686A (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse.
To generate a not-acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.
Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

The MAX77686A has two I2C slave addresses as below.

Block	Slave Address in binary	Slave Address (Write) in hex	Slave Address (Read) In hex
Power block (BUCK, LDO, back-up charger)	0001 001x	12	13
RTC	0000 110x	0C	0D



< Slave Address Byte Example for Power Block>

Clock Stretching

In general the clock signal generation for the I^2C bus is the responsibility of the master device. The I^2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. MAX77686A does not use any form of clock stretching to hold down the clock line.

General Call Address

The MAX77686A does not implement the I2C specification “general call address.” If the MAX77686A sees the general call address (0b0000_0000) it will not issue an acknowledge.

Communication Speed

MAX77686A provides an I^2C 3.0-compatible (3.4MHz) serial interface.

- I^2C Revision 3 Compatible Serial Communications Channel
  - 0Hz to 100kHz (Standard Mode)
  - 0Hz to 400kHz (Fast Mode)
  - 0Hz to 1MHz (Fast Mode Plus)
  - 0Hz to 3.4MHz (High-Speed Mode)
- Does not utilize I^2C Clock Stretching

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pull-up resistors. Higher time constants created by the bus capacitance and pull-up resistance (C*R) slow the bus operation. Therefore, when increasing bus speeds the pull-up resistance must be decreased to maintain a reasonable time constant. See the "pull-up resistor sizing" section of the I^2C revision 3 specification for detailed guidance on the pull-up resistor selection. In general for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pull-up resistors, a 400kHz bus needs about a 1.5kΩ pull-up resistors, and a 1MHz bus needs 680Ω pull-up resistors. Note that when the open drain bus is low, the pull-up resistor is dissipating power, lower value pull-up resistors dissipate more power (V^2/R). Operating in high-speed mode requires some special considerations. For a full list of considerations see the I^2C 3.0 specification. The major considerations with respect to MAX77686A are:

- The I^2C bus master use current source pull-ups to shorten the signal rise times.
- The I^2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, MAX77686A inputs filters are set for standard mode, fast mode, or fast mode plus (i.e. 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in Protocols section.

Communication Protocols

The MAX77686A supports both writing and reading from its registers. The table below shows the I^2C communication protocols that each functional block. The power block uses the same communications protocols. The RTC section does not support the "writing multiple bytes using register-data paris" protocols - instead, the RTC section supports the 'writing to sequential registers" protocol.

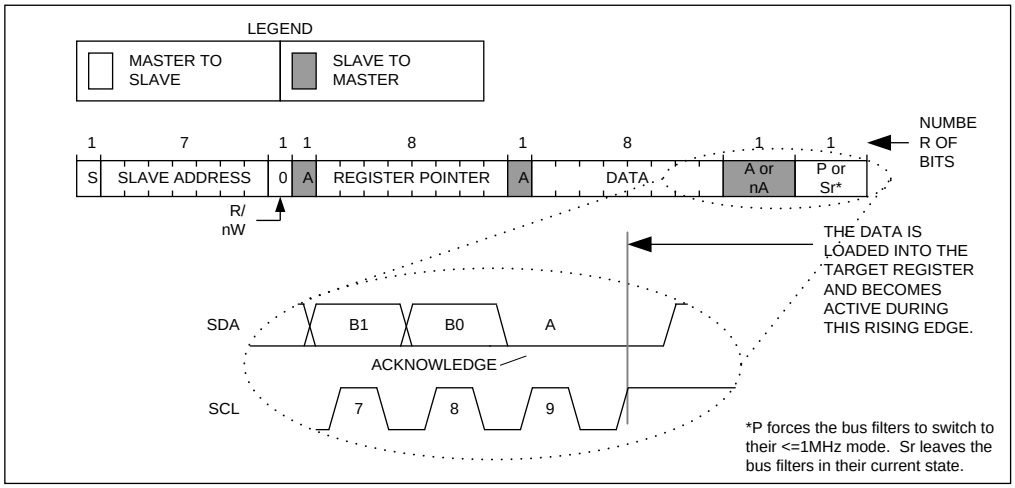
Power Block	RTC
Writing to a Single Register	Writing to a single Register
Writing Multiple Bytes using Register-Data paris	Writing to Sequential Registers
Reading from a Single Register	Reading from a Single Register
Reading from Sequential Registers	Reading from Sequential Registers

Writing to a Single Register

The figure below shows the protocol for the I^2C master device to write one byte of data to the MAX77686A. This protocol is the same as the SMBus specification's "write byte" protocol.

The "write byte" protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW=0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4)]The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data
8) The slave acknowledges or not acknowledges the data byte. The next rising edge on SDA will load the data byte into its target register and the data will become active.
9) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.



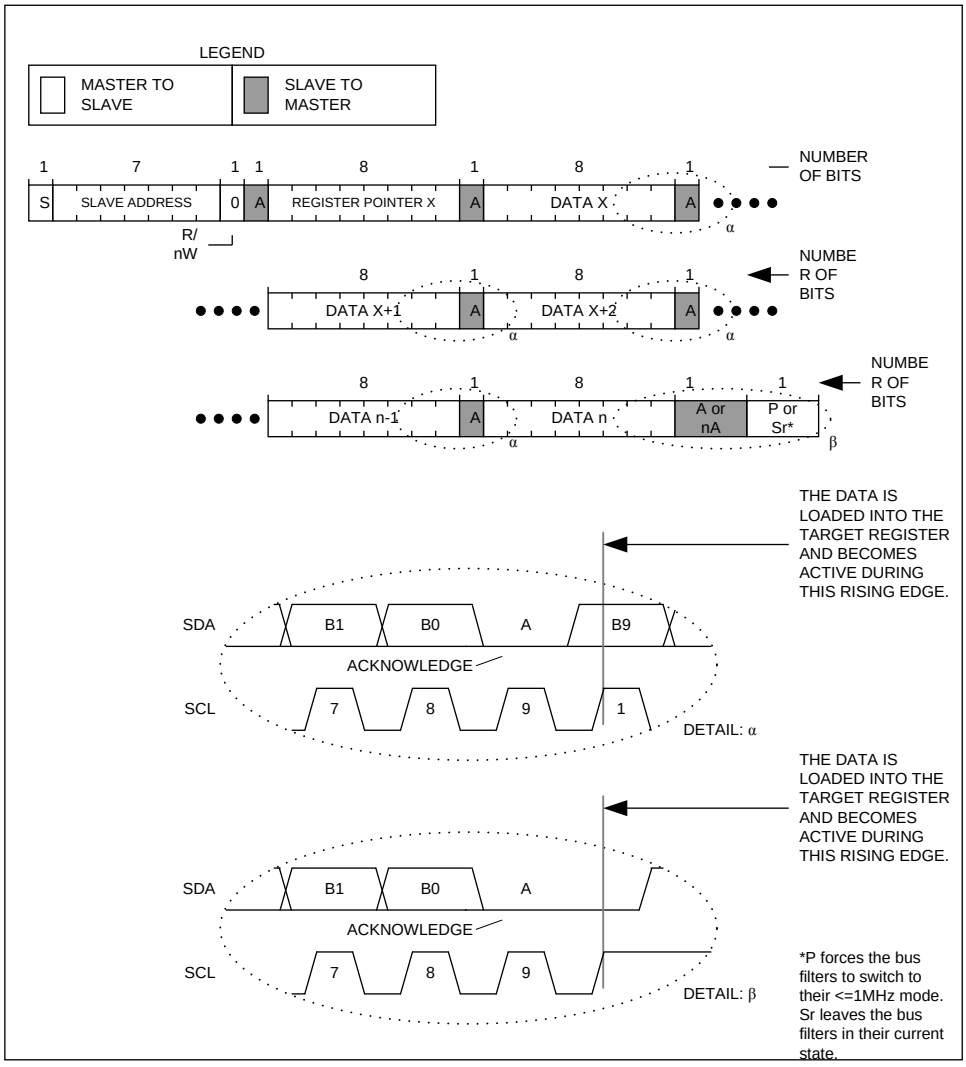
<Figure: Writing to a single register with the “write byte” protocol

Writing to Sequential Registers

The figure below shows the protocol for writing to a sequential registers. This protocol is similar to the “write byte” protocol, except the master continues to write after it receives the first byte of data. When the master is done writing it issues a stop or repeated start. This protocol is recommended when writing the RTC timekeeping registers (RTC_SEC, RTC_MIN, RTC_HOURS, RTC_WEEKDAY, RTC_DATE, RTC_DATE, RTC_MONTH, RTC_YEAR1, RTC_YEAR2).

The “writing to sequential registers” protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW=0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. The next rising edge on SDA will load the data byte into its target register and the data will become active.
8) Steps 6 to 7 are repeated as many times as the master requires.
9) During the last acknowledge related clock pulse, the master may issue an acknowledge or a not-acknowledge.
10) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.



<Figure: Writing to sequential registers “x” to “n”>

Writing Multiple Bytes using register-Data Pairs

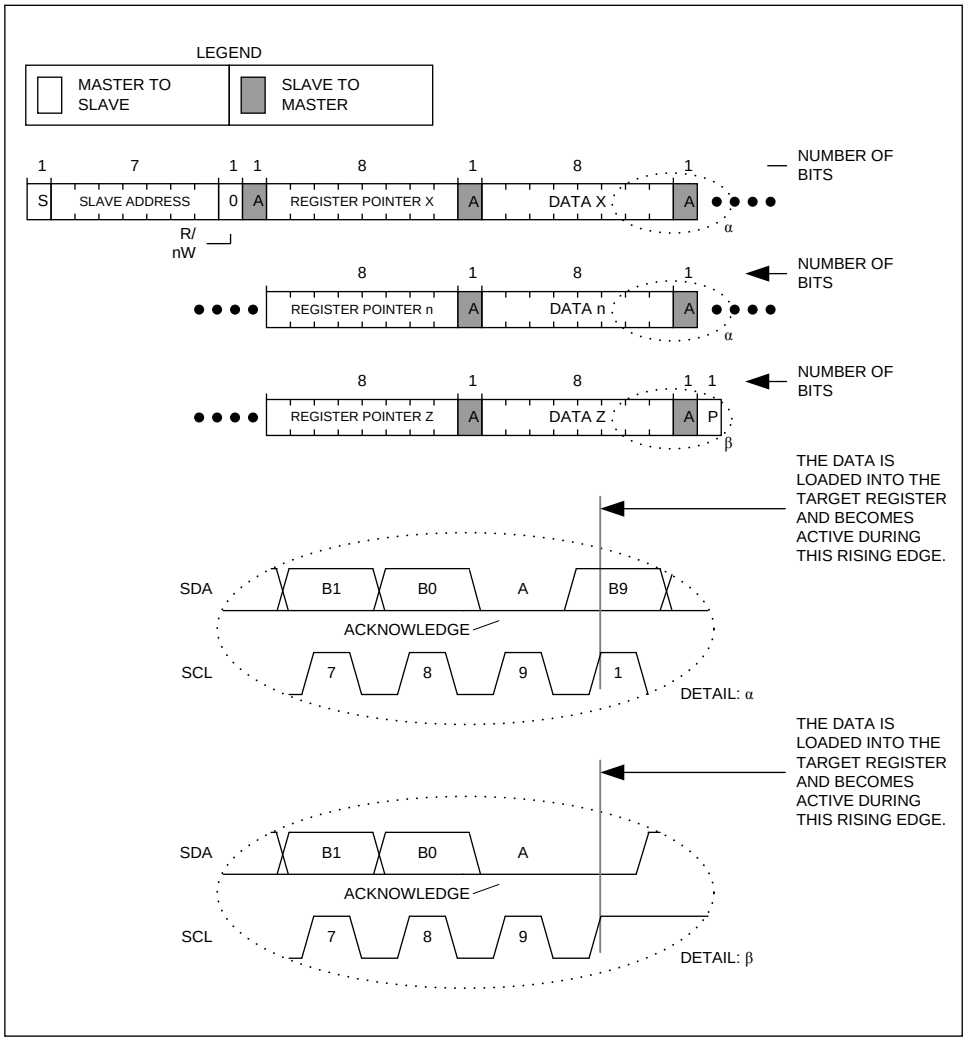
The figure below shows the protocol for the I^2C master device to write multiple bytes to the MAX77686A using register-data pairs. This protocol allows the I^2C master device to address the slave only once and then send data to multiple registers in a random order. Registers may be written continuously until the master issues a stop condition.

The “writing multiple bytes using register-data paris” protocol is not supported by the RTC functional block (I2C slave address 0x0C/0x0D)

The “multiple byte register-data pair” protocol is as follows:

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. The next rising edge on SDA will load the data byte into its target register and the data will become active.
8) Steps 5 to 7 are repeated as many times as the master requires.

9) The master sends a stop condition. During the rising edge of the stop related SDA edge, the data byte that was previously written is loaded into the target register and becomes active.



<Figure: Writing to multiple registers with the “multiple byte register-data pari” protocol>

Reading from a single register

The I^{2}C master device reads one byte of data to the MAX77686A. This protocol is the same as the SMBus specification’s “read byte” protocol.

The “read byte” protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW=0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a repeated start command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/nW=1).
8) The addressed slave asserts an acknowledge by pulling SDA low.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues a not-acknowledge (nA).
11) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that every time the MAX77686A receives a stop its register pointer is set to 0x00. If reading register 0x00 after a stop has been issued, steps 1 to 6 in the above algorithm can be skipped.

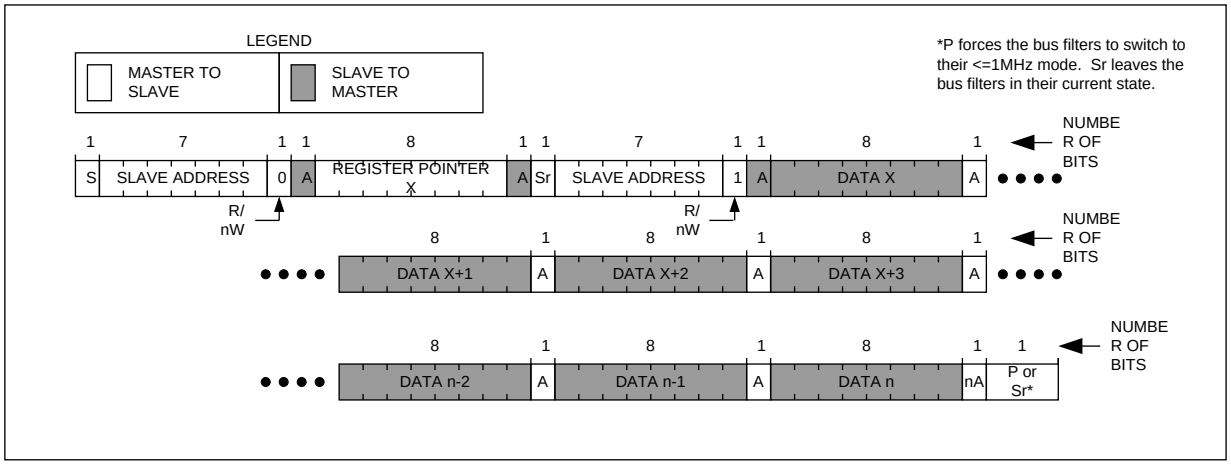
Reading from Sequential Registers

The figure below shows the protocol for reading from sequential registers. This protocol is similar to the “read byte” protocol except the master issues an acknowledge to signal the slave that it wants more data – when the master has all the data it requires it issues a not-acknowledge (nA) and a stop (P) to end the transmission.
This protocol is recommended when reading the RTC timekeeping registers (RTC_SEC, RTC_MIN, RTC_HOURS, RTC_WEEKDAY, RTC_DATE, RTC_DATE, RTC_MONTH, RTC_YEAR1, RTC_YEAR2). When reading the RTC timekeeping registers, seconady buffers are used to prvent errors when the internal register update. The secondary buffers are loaded with the timekeeping register data during an address read byte to the RTC (0x0D) and when the register pointer rolls over to zero.the time information is read from these secondary registers, while the clock continues to run. This eliminates the need to re-read the registers in case the main registers update during a read.

The “continuous read from sequential registers” protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW=0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a repeated start command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/nW=1). When reading the RTC timekeeping registers, secondary buffers are loaded with the timekeeping register data during this operation.
8) The addressed slave asserts an acknowledge by pulling SDA low.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
11) Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
12) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that every time the MAX77686A receives a stop its register pointer is set to 0x00. If reading register 0x00 after a stop has been issued, steps 1 to 6 in the above algorithm can be skipped.



<Figure: Reading continuously from sequential registers “x” to “n”>

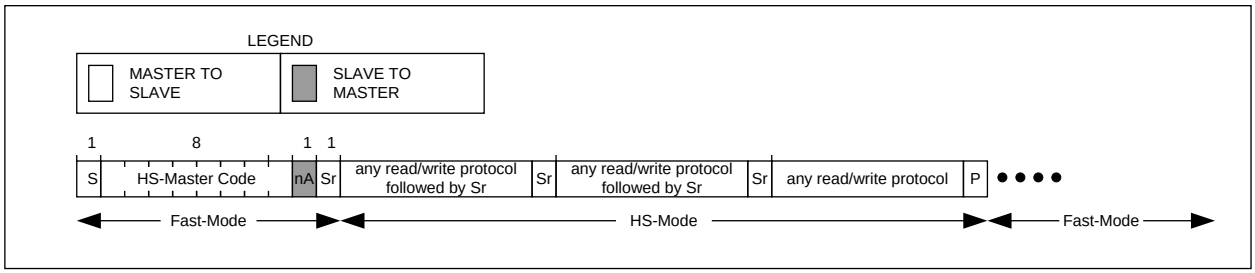
Engaging HS-Mode for operation up to 3.4MHz

The figure below shows the protocol for engaging HS-mode operation. HS-mode operation allows for a bus operating speed up to 3.4MHz.

The "engaging HS-mode" protocol is as follows:

1) Begin the protocol while operating at a bus speed of 1MHz or lower
2) The master sends a start command (S).
3) The master sends the 8-bit master code of 0b0000 1XXX where 0bXXX are don't care bits.
4) The addressed slave issues a not acknowledge (nA).
5) The master may now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master may continue to issue high-speed read/write operations until a stop (P) is issued. Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. After a stop has been issued, steps 1 to 6 in the above algorithm may be skipped.



<Figure: Engaing HS-Mode>

Register Reset Conditions

Type S: Registers are reset each time when V_{COIN} < V_{COIN} UVLO (~1.55V) and BATT < POR (1.55V)
Type O: Registers are reset each time when BATT < BATT UVLO (2.55V) or the MAX77686A transitions from ON to OFF state (ex: RESETB from HIGH to LOW)

HEX REGISTER ADDRESS/DESCRIPTION SUMMARY for Power Management Section

address	register name / function	RESET (hex)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
00	Device ID	-	Metal option					CHIP_REV		
01	INTSRC	00	reserved	reserved	reserved	reserved	reserved	reserved	reserved	RTC
02	INT1	00	MRSTB	ONKEY1S	ACOKBR	ACOKBF	JIGONBR	JIGONBF	PWRONR	PWRONF
03	INT2	00	reserved	reserved	reserved	reserved	reserved	reserved	120C	140C
04	INT1MSK	C0	MRSTBM	ONKEY1SM	ACOKBRM	ACOKBFM	JIGONBRM	JIGONBFM	PWRONFM	PWRONRM
05	INT2MSK	03	reserved	reserved	reserved	reserved	reserved	reserved	120CM	140CM
06	STATUS1		reserved	reserved	reserved	MRSTB	ONKEY1S	ACOKB	JIGONB	PWRON
07	STATUS2		reserved	reserved	WTSREVENT	SMPLEVENT	RTCA2	RTCA1	120C	140C
08	PWRON		WSTRON	SMPLON	RTCA2	RTCA1	MRSTB	ACOKB	JIGONB	PWRON
09	ONOFFDELAY	00	reserved	reserved	reserved	GRDELAY			ONDELAY	
0A	MRSTB	0C	reserved	reserved	reserved	reserved	MRSTBEN	MRDBTMER		
0B-0F	reserved									
10	BUCK1CTRL	0B	reserved	reserved	reserved	reserved	SD1DIS	FPWM	BUCK1EN	
11	BUCK1OUT	05	reserved	reserved	B1OUT					
12	BUCK2CTRL1	72	RAMP		BUCK2EN		SD2DIS	FPWM	ROCS_EN_B2	nFSRADE_B2
14-1B	BUCK2DVS1-8	28	B2DVS							
1C	BUCK3CTRL1	72	RAMP		BUCK3EN		SD3DIS	FPWM	ROCS_EN_B3	nFSRADE_B3
1D	reserved									
1E-25	BUCK3DVS1-8	20	B3DVS							
26	BUCK4CTRL1	72	RAMP		BUCK4EN		SD4DIS	FPWM	ROCS_EN_B4	nFSRADE_B4
27	reserved									
28-2F	BUCK4DVS1-8	20	B4DVS							
30	BUCK5CTRL	0B	reserved	reserved	reserved	reserved	SD5DIS	FPWM	BUCK5EN	
31	BUCK5OUT		reserved	reserved	B5OUT					
32	BUCK6CTRL	0B	reserved	reserved	reserved	reserved	SD6DIS	FPWM	BUCK6EN	
33	BUCK6OUT	0C	reserved	reserved	B6OUT					
34	BUCK7CTRL	0B	reserved	reserved	reserved	reserved	SD7DIS	FPWM	BUCK7EN	
35	BUCK7OUT	19	reserved	reserved	B7OUT					
36	BUCK8CTRL	08	reserved	reserved	reserved	reserved	SD8DIS	FPWM	BUCK8EN	
37	BUCK8OUT	2A	reserved	reserved	B8OUT					
38	BUCK9CTRL	08	reserved	reserved	reserved	reserved	SD9DIS	FPWM	BUCK9EN	
39	BUCK9OUT	09	reserved	reserved	B9OUT					
3A-3F	reserved									
40	LDO1CTRL1	C8	OPMODE		L01_TV					
60	LDO1CTRL2	9A	L01OVCLMP_EN	reserved	reserved		reserved	reserved	ADSLDO1	reserved
41	LDO2CTRL1		OPMODE		L02_TV					
61	LDO2CTRL2	9A	L02OVCLMP_EN	reserved	reserved		reserved	reserved	ADSLDO2	reserved
42	LDO3CTRL1	D4	OPMODE		L03_TV					
62	LDO3CTRL2	9A	L03OVCLMP_EN	reserved	L03_COMP		reserved	reserved	ADSLDO3	reserved
43	LDO4CTRL1	E8	OPMODE		L04_TV					
63	LDO4CTRL2	9A	L04OVCLMP_EN	reserved	L04_COMP		reserved	reserved	ADSLDO4	reserved
44	LDO5CTRL1	D4	OPMODE		L05_TV					
64	LDO5CTRL2	1A	L05OVCLMP_EN	reserved	L05_COMP		reserved	reserved	ADSLDO5	reserved
45	LDO6CTRL1	CC	OPMODE		L06_TV					
65	LDO6CTRL2	9A	L06OVCLMP_EN	reserved	reserved		reserved	reserved	ADSLDO6	reserved
46	LDO7CTRL1	CC	OPMODE		L07_TV					
66	LDO7CTRL2	9A	L07OVCLMP_EN	reserved	reserved		reserved	reserved	ADSLDO7	reserved
47	LDO8CTRL1	C8	OPMODE		L08_TV					
67	LDO8CTRL2	9A	L08OVCLMP_EN	reserved	reserved		reserved	reserved	ADSLDO8	reserved
48	LDO9CTRL1	14	OPMODE		L09_TV					
68	LDO9CTRL2	92	L09OVCLMP_EN	reserved	L09_COMP		reserved	reserved	ADSLDO9	reserved
49	LDO10CTRL1	D4	OPMODE		L10_TV					
69	LDO10CTRL2	9A	L10OVCLMP_EN	reserved	L10_COMP		reserved	reserved	ADSLDO10	reserved
4A	LDO11CTRL1	D4	OPMODE		L11_TV					
6A	LDO11CTRL2	9A	L11OVCLMP_EN	reserved	L11_COMP		reserved	reserved	ADSLDO11	reserved
4B	LDO12CTRL1	EC	OPMODE		L12_TV					
6B	LDO12CTRL2	9A	L12OVCLMP_EN	reserved	L12_COMP		reserved	reserved	ADSLDO12	reserved

address	register name / function	RESET (hex)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
4C	LDO13CTRL1	D4	OPMODE		L13_TV					
6C	LDO13CTRL2	9A	L13OVCLMP_EN	reserved	L13_COMP		reserved	reserved	ADSLDO13	reserved
4D	LDO14CTRL1	D4	OPMODE		L14_TV					
6D	LDO14CTRL2	9A	L14OVCLMP_EN	reserved	L14_COMP		reserved	reserved	ADSLDO14	reserved
4E	LDO15CTRL1	C8	OPMODE		L15_TV					
6E	LDO15CTRL2	9A	L15OVCLMP_EN	reserved	reserved		reserved	reserved	ADSLDO15	reserved
4F	LDO16CTRL1	D4	OPMODE		L16_TV					
6F	LDO16CTRL2	1A	L16OVCLMP_EN	reserved	L16_COMP		reserved	reserved	ADSLDO16	reserved
50	LDO17CTRL1	08	OPMODE		L17_TV					
70	LDO17CTRL2	92	L17OVCLMP_EN	reserved	L17_COMP		reserved	reserved	ADSLDO17	reserved
51	LDO18CTRL1	14	OPMODE		L18_TV					
71	LDO18CTRL2	92	L18OVCLMP_EN	reserved	L18_COMP		reserved	reserved	ADSLDO18	reserved
52	LDO19CTRL1	14	OPMODE		L19_TV					
72	LDO19CTRL2	92	L19OVCLMP_EN	reserved	L19_COMP		reserved	reserved	ADSLDO19	reserved
53	LDO20CTRL1	14	OPMODE		L20_TV					
73	LDO20CTRL2	92	L20OVCLMP_EN	reserved	L20_COMP		reserved	reserved	ADSLDO20	reserved
54	LDO21CTRL1	28	OPMODE		L21_TV					
74	LDO21CTRL2	92	L21OVCLMP_EN	reserved	L21_COMP		reserved	reserved	ADSLDO21	reserved
55	LDO22CTRL1	28	OPMODE		L22_TV					
75	LDO22CTRL2	92	L22OVCLMP_EN	reserved	L22_COMP		reserved	reserved	ADSLDO22	reserved
56	LDO23CTRL1	2C	OPMODE		L23_TV					
76	LDO23CTRL2	92	L23OVCLMP_EN	reserved	L23_COMP		reserved	reserved	ADSLDO23	reserved
57	LDO24CTRL1	2C	OPMODE		L24_TV					
77	LDO24CTRL2	92	L24OVCLMP_EN	reserved	L24_COMP		reserved	reserved	ADSLDO24	reserved
58	LDO25CTRL1	2C	OPMODE		L25_TV					
78	LDO25CTRL2	92	L25OVCLMP_EN	reserved	L25_COMP		reserved	reserved	ADSLDO25	reserved
59	LDO26CTRL1	2C	OPMODE		L26_TV					
79	LDO26CTRL2	92	L26OVCLMP_EN	reserved	L26_COMP		reserved	reserved	ADSLDO26	reserved
5A-5F	reserved									
7A-7D	reserved									
7E	BBAT Charger	4F	BBCRS		BBCLOWIEN	BBCVS		BBCCS		BBCHOSTEN
7F	32KHZ	01	reserved	reserved	reserved	reserved	LowjitterMode	ENP32KH	ENP32KHCP	ENP32KHAP

Power Management Control Registers

Block	Slave Address in binary	Slave Address (Write) in hex	Slave Address (Read) In hex
Power block	0001 001x	12	13

Device ID

Address (hex)	MODE		Type: O	RESET: N/A
00	R			
BIT	**NAME**	**POR**	**Description**	
7	Null-trim	-	1: Null-trim, 0: normal OTP for mass production.	
6:3	Version	-	0000: Plain or -6Z, 0001: -1Z or -5Z, 0010: -2Z or -4Z	
2:0	CHIP_REV		Chip Revision History 001 :PASS1, 010: PASS2 and so on	

INTSRC- Interrupt Source register

The register to indicate the source of Interrupt Event

Address (hex)	MODE		Type: S	RESET:0x00
01	R/C			
BIT	**NAME**	**POR**	**Description**	
7:1	Reserved	0000000	Write “0000000”	
0	RTC	0	1: The Interrupt event on RTC detected. (All Interrupt Events under the slave address, 0xD0/D1)	

INT1- TOPSYSINT register 1

Address (hex)	MODE		Type: S	RESET:0x00
02	R/C			
BIT	**NAME**	**POR**	**Description**	
7	MRSTB	0	1: MRSTB1&2 maintains logic low for longer than Manual Reset Debounce time (MRDBTMER).	
6	ONKEY1S	0	1: PWRON =High for longer than 1sec.	
5	ACOKBR	0	1: ACOKB rising edge is detected, Debounced	
4	ACOKBF	0	1: ACOKB falling edge is detected, Debounced	
3	JIGONBR	0	1: JIGONB rising edge is detected. Debounced.	
2	JIGONBF	0	1: JIGONB falling edge is detected. Debounced.	
1	PWRONR	0	1: PWRON rising edge is detected. Debounced.	
0	PWRONF	0	1: PWRON falling edge is detected. Debounced.	

INT2- TOPSYSINT register 2

Address (hex)	MODE		Type: S	RESET:0x00
03	R/C			
BIT	**NAME**	**POR**	**Description**	
7:2	reserved			
1	120C	0	120C Thermal Interrupt . This interrupt is set when T_{DIE}>120C 0 = Not detected 1 = Detected	
0	140C	0	140C Thermal Interrupt. This interrupt is set when T_{DIE}>140C 0 = Not Detected 1 = Detected	

INT1MSK – TOPSYSINT Mask Register 1

Address (hex)	MODE		Type: S	RESET:0xC0
04	R/W			
BIT	**NAME**	**POR**	**Description**	
7	MRSTBM	1	0: Manual Reset Interrupt is enabled **1: Mask MRSTB Interrupt**	
6	ONKEY1SM	1	0: Interrupt enabled **1: Mask ONKEY1S interrupt**	
5	ACOKBRM	0	**0: Interrupt enabled** 1: Mask ACOKBF rising edge detection	
4	ACOKBFM	0	**0: Interrupt enabled** 1: Mask ACOKBR falling edge detection	
3	JIGONBRM	0	**0: Interrupt enabled** 1: Mask JIGONBR rising edge detection	
2	JIGONBFM	0	**0: Interrupt enabled** 1: Mask JIGONBF falling edge detection	
1	PWRONRM	0	**0: Interrupt enabled** 1: Mask PWRON rising edge detection interrupt	
0	PWRONFM	0	**0: Interrupt enabled** 1: Mask PWRON falling edge detection interrupt	

INT2MSK – TOPSYSINT Mask Register 2

Address (hex)	MODE		Type: S	RESET:0x03
05	R/W			
BIT	**NAME**	**POR**	**Description**	
7:2	reserved		**Write "000000"**	
1	120CM	1	0: Interrupt enabled **1: Mask 120C Interrupt**	
0	140CM	1	0: Interrupt enabled **1: Mask 140C interrupt**	

STATUS1 – TOPSYS Status Register 1

Address (hex)	MODE		Type: O	RESET: N/A
06	R			
BIT	**NAME**	**POR**	**Description**	
7:5	reserved	-		
4	MRSTB	-	0: Manual Reset is not detected 1: Manual Reset is detected.	
3	ONKEY1S	-	0: PWRON key is not pressed longer than 1sec 1: PWRON key is pressed longer than 1sec	
2	ACOKB	-	0: ACOKB's falling edge is not detected 1: ACOKB's falling edge is detected	
1	JIGONB	-	0: JIGONB is low 1: JIGONB is high	
0	PWRON	-	0: PWRON is low 1: PWRON is high	

STATUS2 – TOPSYS Status Register 2

Address (hex)	MODE		Type: O	RESET: N/A
07	R			
BIT	**NAME**	**POR**	**Description**	
7:6	reserved			
5	WTSR EVENT	-	0: software Reset (WTSR) event hasn't happened 1: WTSR event has happened	
4	SMPLEVENT	-	0: SMPL event does not occur 1: SMPL event did occur	
3	RTCA2	-	0: RTC ALARM2 is not reached 1: RTC ALARM2 has reached	
2	RTCA1	-	0: RTC ALARM1 is not reached 1: RTC ALARM1 has reached	
1	120C	-	120C Thermal Status Bit 0 = Die Temperature (T_{DIE})<120C 1 = Die Temperature (T_{DIE})>120C	
0	140C	-	140C Thermal Status Bit 0 = Die Temperature (T_{DIE})<140C 1 = Die Temperature (T_{DIE})>140C	

PWRON – Power-On Source Register

Address (hex)	MODE		Type: S1	RESET: N/A
08	R			
BIT	**NAME**	**POR**	**Description**	
7	WSTRON	0	1=Power on triggered by WTSR Event	
6	SMPLON	0	1=Power on triggered by SMPL Event	
5	RTCA2	0	1=Power on triggered by ALARM2	
4	RTCA1	0	1=Power on triggered by ALARM1	
3	MRSTB	0	1=Power on triggered by Manual Reset Event	
2	ACOKB	0	1= Power on triggered by ACOKB=Low	
1	JIGONB	0	1=Power on triggered by JIGONB=Low	
0	PWRON	0	1=Power on triggered by PWRON=High	

Note that the last power-on source is maintained until a new power-on source is detected.

ONOFFDELAY Configuration

Address (hex)	MODE		Type: S	RESET: 0x00
09	R/W			
BIT	**NAME**	**POR**	**Description**	
7:5	reserved	000	Write “000”	
4:2	GRDELAY	000	Program the delay time for each group **000: 62usec** 001: 124usec 010: 240usec 011: 1msec 100: 2msec >100: 2msec	
1:0	ONDELAY	00	Program the delay for each power rail **00: 62usec** 01: 92usec 10: 120usec 11: 240usec	

MRSTB Register

Program the Manual Reset ON/OFF and Debounce Timer

Address (hex)	MODE		Type: O	RESET: 0x0C
0A	R/W			
BIT	**Name**	**POR**	**Description**	
7:4	Reserved	0000	Write “0000” to these bits	
3	MRSTBEN	1	Manual Reset Enable 0: Manual Reset is disabled **1: Manual Reset is enabled**	
2:0	MRDBTMER	100	Program Manual Reset Debounce Timer when both MRSTB1 and MRSTB2 = Logic Low for a set debounced time	

0x0: 3sec	0x2: 5sec	**0x4: 7sec**	0x6: 9sec
0x1: 4sec	0x3: 6sec	0x5: 8sec	0x7: 10sec

0x0B-0x0F: reserved

BUCK Registers

BUCK1CTRL

ON/OFF Control for BUCK1, Active Discharge and PWM

Address (hex)	MODE		Type: O	RESET:0x0B
10	R/W			
BIT	**Name**	**POR**	**Description**	
7:4	reserved	0000	Write “0000”	
3	SD1DIS	1	0: Active discharge OFF **1: Active discharge ON**	
2	FPWM	0	Forced PWM **0: Turn forced PWM OFF** **(automatically skip pulse under light load)** 1: Turn forced PWM on	
1:0	BUCK1EN	11	00: OFF (regardless of PWRREQ) 01 & 10: Output ON/OFF controlled by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output OFF **11: ON in normal mode (Regardless of PWRREQ)**	

BUCK1OUT

Control for BUCK1 Output

Address (hex)	MODE		Type: O	RESET:0x14
11	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:6	reserved	00	Write “00” to these bits	
5:0	B1OUT	01 0100	BUCK1 Output Voltage	

6'h00: 0.7500V	6'h10: 0.9500V	6'h20: 1.1500V	6'h30: 1.3500V
6'h01: 0.7625V	6'h11: 0.9625V	6'h21: 1.1625V	6'h31: 1.3625V
6'h02: 0.7750V	6'h12: 0.9750V	6'h22: 1.1750V	6'h32: 1.3750V
6'h03: 0.7875V	6'h13: 0.9875V	6'h23: 1.1875V	6'h33: 1.3875V
6'h04: 0.8000V	**6'h14: 1.0000V**	6'h24: 1.2000V	6'h34: 1.4000V
6'h05: 0.8125V	6'h15: 1.0125V	6'h25: 1.2125V	6'h35: 1.4125V
6'h06: 0.8250V	6'h16: 1.0250V	6'h26: 1.2250V	6'h36: 1.4250V
6'h07: 0.8375V	6'h17: 1.0375V	6'h27: 1.2375V	6'h37: 1.4375V
6'h08: 0.8500V	6'h18: 1.0500V	6'h28: 1.2500V	6'h38: 1.4500V
6'h09: 0.8625V	6'h19: 1.0625V	6'h29: 1.2625V	6'h39: 1.4625V
6'h0A: 0.8750V	6'h1A: 1.0750V	6'h2A: 1.2750V	6'h3A: 1.4750V
6'h0B: 0.8875V	6'h1B: 1.0875V	6'h2B: 1.2875V	6'h3B: 1.4875V
6'h0C: 0.9000V	6'h1C: 1.1000V	6'h2C: 1.3000V	6'h3C: 1.5000V
6'h0D: 0.9125V	6'h1D: 1.1125V	6'h2D: 1.3125V	6'h3D: 1.5125V
6'h0E: 0.9250V	6'h1E: 1.1250V	6'h2E: 1.3250V	6'h3E: 1.5250V
6'h0F: 0.9375V	6'h1F: 1.1375V	6'h2F: 1.3375V	6'h3F: 1.5375V

BUCK2CTRL1

ON/OFF Control for BUCK2, Active Discharge, ramp rate and PWM

Address (hex)	MODE		Type: O	RESET:0x72
12	R/W			
BIT	**Name**	**POR**	**Description**	
7:6	RAMP	01	Programs the BUCK2 rising ramp rate in mV/us 00: 13.75mV/µs Ramp Rate **01: 27.5mV/µs Ramp Rate** 10: 55mV/µs Ramp Rate 11: No slew rate control. Buck output voltage increases as fast as the current limit allows.	
5:4	BUCK2EN	11	00: OFF (regardless of PWRREQ) 01: Output ON/OFF controlled by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode(Remote Sense enabled) PWRREQ=L (0) : Output OFF 10: Low Power Mode. Be forced into low-power mode. The Max load current is 5mA and the quiescent supply current is 5uA. **11: ON in normal mode (Regardless of PWRREQ)** (Remote Sense enabled)	
3	SD2DIS	0	**0: Active discharge ON** 1: Active discharge OFF	
2	FPWM	0	Forced PWM **0: Turn forced PWM OFF** **(automatically skip pulse under light load)** Regulator skips pulses under light load conditions, and operates at a fixed frequency with medium to heavy load conditions. The regulator automatically transitions between pulse skipping and fixed frequency as needed. 1: Turn forced PWM on (with fixed frequency under all load conditions)	
1	ROVS_EN_B2	1	BUCK2 Remote Output Voltage Sense Enable 0= Disabled **1= Enabled** Note that when BUCK2 is operating in low-power mode, the ROVS function is automatically disabled however; this bit will not be affected. If this bit is set, then ROVS will automatically be re-enabled when BUCK2 enters its normal operating mode.	
0	nFSRADE_B2	0	Active-Low SDx Falling Slew Rate Active-Discharge Enable. **0= Active-Discharge Enabled. BUCK2 operates in forced PWM mode during the time the output voltage decreases. With forced PWM mode enabled, BUCK2 can sink current from the output capacitor to ensure that the output voltage falls at the rate programmed by RAMP[1:0]. To ensure a smooth output voltage decrease, the PMW mode will remain engaged for 50us after the output voltage decreases to its target voltage.** 1= Active Discharge Disabled. BUCK2 is allowed to operate in skip mode during the time the output voltage decreases (only if FPWM=0). In skip mode, BUCK2 cannot sink current from the output capacitor. Since BUCK2 cannot sink current in skip mode the output voltage falling slew rate is a function of the external load on BUCK2. If the external load on BUCK2 is heavy, then the output voltage falling slew rate will be the rate programmed by RAMP[1:0]. If the external load on BUCK2 is light, then the output voltage falling slew rate will be a function of the output capacitance and the external load. Note that the BUCK2 internal feedback string will always impose a 2uA load on the output.	

BUCK2DVS1

Control for BUCK2 Output in DVS3=DVS2=DVS1=LOW

Address (hex)	MODE		Type: O	RESET:0x28
14	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B2DVS	0010 1000	BUCK2 Output Voltage when DVS3=DVS2=DVS1=LOW	

BUCK2DVS2

Control for BUCK2 Output in DVS3=DVS2=LOW, DVS1=HIGH

Address (hex)	MODE		Type: O	RESET:0x28
15	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B2DVS	0010 1000	BUCK2 Output Voltage when DVS3=DVS2=LOW, DVS1=HIGH	

BUCK2DVS3

Control for BUCK2 Output in DVS3=LOW, DVS2=HIGH, DVS1=LOW

Address (hex)	MODE		Type: O	RESET:0x28
16	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B2DVS	0010 1000	BUCK2 Output Voltage when DVS3=LOW, DVS2=HIGH, DVS1=LOW	

BUCK2DVS4

Control for BUCK2 Output in DVS3=LOW, DVS2=DVS1=HIGH

Address (hex)	MODE		Type: O	RESET:0x28
17	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B2DVS	0010 1000	BUCK2 Output Voltage when DVS3=LOW, DVS2=DVS1=HIGH	

BUCK2DVS5

Control for BUCK2 Output in DVS3=HIGH, DVS2=DVS1=LOW

Address (hex)	MODE		Type: O	RESET:0x28
18	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B2DVS	0010 1000	BUCK2 Output Voltage when DVS3=HIGH, DVS2=DVS1=LOW	

BUCK2DVS6

Control for BUCK2 Output in DVS3=HIGH, DVS2=LOW, DVS1=HIGH

Address (hex)	MODE		Type: O	RESET:0x28
19	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B2DVS	0010 1000	BUCK2 Output Voltage when	

BUCK2DVS7

Control for BUCK2 Output in DVS3=DVS2=HIGH, DVS1=LOW

Address (hex)	MODE		Type: O	RESET:0x28
1A	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B2DVS	0010 1000	BUCK2 Output Voltage when DVS3=DVS2=HIGH, DVS1=LOW	

BUCK2DVS8

Control for BUCK2 Output in DVS3=DVS2=DVS1=HIGH

Address (hex)	MODE		Type: O	RESET:0x28
1B	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B2DVS	0010 1000	BUCK2 Output Voltage when DVS3=DVS2=DVS1=HIGH	

BUCK2 Output Voltage Table

0x00=0.6000V	**0x20=1.0000V**	0x40=1.4000V	0x60=1.8000V	0x80=2.2000V	0xA0=2.6000V	0xC0=3.0000V	0xE0=3.4000V

0x01=0.6125V	0x21=1.0125V	0x41=1.4125V	0x61=1.8125V	0x81=2.2125V	0xA1=2.6125V	0xC1=3.0125V	0xE1=3.4125V
0x02=0.6250V	0x22=1.0250V	0x42=1.4250V	0x62=1.8250V	0x82=2.2250V	0xA2=2.6250V	0xC2=3.0250V	0xE2=3.4250V
0x03=0.6375V	0x23=1.0375V	0x43=1.4375V	0x63=1.8375V	0x83=2.2375V	0xA3=2.6375V	0xC3=3.0375V	0xE3=3.4375V
0x04=0.6500V	0x24=1.0500V	0x44=1.4500V	0x64=1.8500V	0x84=2.2500V	0xA4=2.6500V	0xC4=3.0500V	0xE4=3.4500V
0x05=0.6625V	0x25=1.0625V	0x45=1.4625V	0x65=1.8625V	0x85=2.2625V	0xA5=2.6625V	0xC5=3.0625V	0xE5=3.4625V
0x06=0.6750V	0x26=1.0750V	0x46=1.4750V	0x66=1.8750V	0x86=2.2750V	0xA6=2.6750V	0xC6=3.0750V	0xE6=3.4750V
0x07=0.6875V	0x27=1.0875V	0x47=1.4875V	0x67=1.8875V	0x87=2.2875V	0xA7=2.6875V	0xC7=3.0875V	0xE7=3.4875V
0x08=0.7000V	**0x28=1.1000V**	0x48=1.5000V	0x68=1.9000V	0x88=2.3000V	0xA8=2.7000V	0xC8=3.1000V	0xE8=3.5000V
0x09=0.7125V	0x29=1.1125V	0x49=1.5125V	0x69=1.9125V	0x89=2.3125V	0xA9=2.7125V	0xC9=3.1125V	0xE9=3.5125V
0x0A=0.7250V	0x2A=1.1250V	0x4A=1.5250V	0x6A=1.9250V	0x8A=2.3250V	0xAA=2.7250V	0xCA=3.1250V	0xEA=3.5250V
0x0B=0.7375V	0x2B=1.1375V	0x4B=1.5375V	0x6B=1.9375V	0x8B=2.3375V	0xAB=2.7375V	0xCB=3.1375V	0xEB=3.5375V
0x0C=0.7500V	0x2C=1.1500V	0x4C=1.5500V	0x6C=1.9500V	0x8C=2.3500V	0xAC=2.7500V	0xCC=3.1500V	0xEC=3.5500V
0x0D=0.7625V	0x2D=1.1625V	0x4D=1.5625V	0x6D=1.9625V	0x8D=2.3625V	0xAD=2.7625V	0xCD=3.1625V	0xED=3.5625V
0x0E=0.7750V	0x2E=1.1750V	0x4E=1.5750V	0x6E=1.9750V	0x8E=2.3750V	0xAE=2.7750V	0xCE=3.1750V	0xEE=3.5750V
0x0F=0.7875V	0x2F=1.1875V	0x4F=1.5875V	0x6F=1.9875V	0x8F=2.3875V	0xAF=2.7875V	0xCF=3.1875V	0xEF=3.5875V
0x10=0.8000V	0x30=1.2000V	0x50=1.6000V	0x70=2.0000V	0x90=2.4000V	0xB0=2.8000V	0xD0=3.2000V	0xF0=3.6000V
0x11=0.8125V	0x31=1.2125V	0x51=1.6125V	0x71=2.0125V	0x91=2.4125V	0xB1=2.8125V	0xD1=3.2125V	0xF1=3.6125V
0x12=0.8250V	0x32=1.2250V	0x52=1.6250V	0x72=2.0250V	0x92=2.4250V	0xB2=2.8250V	0xD2=3.2250V	0xF2=3.6250V
0x13=0.8375V	0x33=1.2375V	0x53=1.6375V	0x73=2.0375V	0x93=2.4375V	0xB3=2.8375V	0xD3=3.2375V	0xF3=3.6375V
0x14=0.8500V	0x34=1.2500V	0x54=1.6500V	0x74=2.0500V	0x94=2.4500V	0xB4=2.8500V	0xD4=3.2500V	0xF4=3.6500V
0x15=0.8625V	0x35=1.2625V	0x55=1.6625V	0x75=2.0625V	0x95=2.4625V	0xB5=2.8625V	0xD5=3.2625V	0xF5=3.6625V
0x16=0.8750V	0x36=1.2750V	0x56=1.6750V	0x76=2.0750V	0x96=2.4750V	0xB6=2.8750V	0xD6=3.2750V	0xF6=3.6750V
0x17=0.8875V	0x37=1.2875V	0x57=1.6875V	0x77=2.0875V	0x97=2.4875V	0xB7=2.8875V	0xD7=3.2875V	0xF7=3.6875V
0x18=0.9000V	0x38=1.3000V	0x58=1.7000V	0x78=2.1000V	0x98=2.5000V	0xB8=2.9000V	0xD8=3.3000V	0xF8=3.7000V
0x19=0.9125V	0x39=1.3125V	0x59=1.7125V	0x79=2.1125V	0x99=2.5125V	0xB9=2.9125V	0xD9=3.3125V	0xF9=3.7125V
0x1A=0.9250V	0x3A=1.3250V	0x5A=1.7250V	0x7A=2.1250V	0x9A=2.5250V	0xBA=2.9250V	0xDA=3.3250V	0xFA=3.7250V
0x1B=0.9375V	0x3B=1.3375V	0x5B=1.7375V	0x7B=2.1375V	0x9B=2.5375V	0xBB=2.9375V	0xDB=3.3375V	0xFB=3.7375V
0x1C=0.9500V	0x3C=1.3500V	0x5C=1.7500V	0x7C=2.1500V	0x9C=2.5500V	0xBC=2.9500V	0xDC=3.3500V	0xFC=3.7500V
0x1D=0.9625V	0x3D=1.3625V	0x5D=1.7625V	0x7D=2.1625V	0x9D=2.5625V	0xBD=2.9625V	0xDD=3.3625V	0xFD=3.7625V
0x1E=0.9750V	0x3E=1.3750V	0x5E=1.7750V	0x7E=2.1750V	0x9E=2.5750V	0xBE=2.9750V	0xDE=3.3750V	0xFE=3.7750V
0x1F=0.9875V	0x3F=1.3875V	0x5F=1.7875V	0x7F=2.1875V	0x9F=2.5875V	0xBF=2.9875V	0xDF=3.3875V	0xFF=3.7875V

BUCK3CTRL1

ON/OFF Control for BUCK3, Active Discharge, ramp rate and PWM

Address (hex)	**MODE**		Type: O	**RESET:0x72**
1C	R/W			
BIT	**Name**	**POR**	**Description**	
7:6	RAMP	01	Programs the BUCK3 rising ramp rate in mV/us 00: 13.75mV/µs Ramp Rate **01: 27.5mV/µs Ramp Rate** 10: 55mV/µs Ramp Rate 11: No slew rate control. Buck output voltage increases as fast as the current limit allows.	

5:4	BUCK3EN	11	00: OFF (regardless of PWRREQ) 01: Output ON/OFF controlled by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode(Remote Sense enabled) PWRREQ=L (0) : Output OFF 10: Low Power Mode. Be forced into low-power mode. The Max load current is 5mA and the quiescent supply current is 5uA. **11: ON in normal mode (Regardless of PWRREQ)** (Remote Sense enabled)
3	SD3DIS	0	**0: Active discharge ON** 1: Active discharge OFF
2	FPWM	0	Forced PWM **0: Turn forced PWM OFF** **(automatically skip pulse under light load)** Regulator skips pulses under light load conditions, and operates at a fixed frequency with medium to heavy load conditions. The regulator automatically transitions between pulse skipping and fixed frequency as needed. 1: Turn forced PWM on (with fixed frequency under all load conditions)
1	ROVS_EN_B3	1	BUCK3 Remote Output Voltage Sense Enable 0= Disabled **1= Enabled** Note that when BUCK3 is operating in low-power mode, the ROVS function is automatically disabled however; this bit will not be affected. If this bit is set, then ROVS will automatically be re-enabled when BUCK3 enters its normal operating mode.
0	nFSRADE_B3	0	Active-Low SDx Falling Slew Rate Active-Discharge Enable. 0= Active-Discharge Enabled. BUCK3 operates in forced PWM mode during the time the output voltage decreases. With forced PWM mode enabled, BUCK3 can sink current from the output capacitor to ensure that the output voltage falls at the rate programmed by RAMP[1:0]. To ensure a smooth output voltage decrease, the PMW mode will remain engaged for 50us after the output voltage decreases to its target voltage. 1= Active Discharge Disabled. BUCK3 is allowed to operate in skip mode during the time the output voltage decreases (only if FPWM=0). In skip mode, BUCK3 cannot sink current from the output capacitor. Since BUCK3 cannot sink current in skip mode the output voltage falling slew rate is a function of the external load on BUCK3. If the external load on BUCK3 is heavy, then the output voltage falling slew rate will be the rate programmed by RAMP[1:0]. If the external load on BUCK3 is light, then the output voltage falling slew rate will be a function of the output capacitance and the external load. Note that the BUCK3 internal feedback string will always impose a 2uA load on the output.

BUCK3DVS1

Control for BUCK3 Output in DVS3=DVS2=DVS1=LOW

Address (hex)	MODE		Type: O	RESET:0x20
1E	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B3DVS	0010 0000	BUCK3 Output Voltage when DVS3=DVS2=DVS1=LOW	

Note that the output voltage is controlled by this register when the DVS function is disabled.

BUCK3DVS2

Control for BUCK3 Output in DVS3=DVS2=LOW, DVS1=HIGH

Address (hex)	MODE		Type: O	RESET:0x20
1F	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B3DVS	0010 0000	BUCK3 Output Voltage when DVS3=DVS2=LOW, DVS1=HIGH	

BUCK3DVS3

Control for BUCK3 Output in DVS3=LOW, DVS2=HIGH, DVS1=LOW

Address (hex)	MODE		Type: O	RESET:0x20
20	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B3DVS	0010 0000	BUCK3 Output Voltage when DVS3=LOW, DVS2=HIGH, DVS1=LOW	

BUCK3DVS4

Control for BUCK3 Output in DVS3=LOW, DVS2=DVS1=HIGH

Address (hex)	MODE		Type: O	RESET:0x20
21	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B3DVS	0010 0000	BUCK3 Output Voltage when DVS3=LOW, DVS2=DVS1=HIGH	

BUCK3DVS5

Control for BUCK3 Output in DVS3=HIGH, DVS2=DVS1=LOW

Address (hex)	MODE		Type: O	RESET:0x20
22	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B3DVS	0010 0000	BUCK3 Output Voltage when DVS3=HIGH, DVS2=DVS1=LOW	

BUCK3DVS6

Control for BUCK3 Output in DVS3=HIGH, DVS2=LOW, DVS1=HIGH

Address (hex)	MODE		Type: O	RESET:0x20
23	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B3DVS	0010 0000	BUCK3 Output Voltage when	

BUCK3DVS7

Control for BUCK3 Output in DVS3=DVS2=HIGH, DVS1=LOW

Address (hex)	MODE		Type: O	RESET:0x20
24	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B3DVS	0010 0000	BUCK3 Output Voltage when DVS3=DVS2=HIGH, DVS1=LOW	

BUCK3DVS8

Control for BUCK3 Output in DVS3=DVS2=DVS1=HIGH

Address (hex)	MODE		Type: O	RESET:0x20
25	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B3DVS	0010 0000	BUCK3 Output Voltage when DVS3=DVS2=DVS1=HIGH	

BUCK3 Output Voltage Table

0x00=0.6000V	**0x20=1.0000V**	0x40=1.4000V	0x60=1.8000V	0x80=2.2000V	0xA0=2.6000V	0xC0=3.0000V	0xE0=3.4000V
0x01=0.6125V	0x21=1.0125V	0x41=1.4125V	0x61=1.8125V	0x81=2.2125V	0xA1=2.6125V	0xC1=3.0125V	0xE1=3.4125V
0x02=0.6250V	0x22=1.0250V	0x42=1.4250V	0x62=1.8250V	0x82=2.2250V	0xA2=2.6250V	0xC2=3.0250V	0xE2=3.4250V
0x03=0.6375V	0x23=1.0375V	0x43=1.4375V	0x63=1.8375V	0x83=2.2375V	0xA3=2.6375V	0xC3=3.0375V	0xE3=3.4375V
0x04=0.6500V	0x24=1.0500V	0x44=1.4500V	0x64=1.8500V	0x84=2.2500V	0xA4=2.6500V	0xC4=3.0500V	0xE4=3.4500V
0x05=0.6625V	0x25=1.0625V	0x45=1.4625V	0x65=1.8625V	0x85=2.2625V	0xA5=2.6625V	0xC5=3.0625V	0xE5=3.4625V
0x06=0.6750V	0x26=1.0750V	0x46=1.4750V	0x66=1.8750V	0x86=2.2750V	0xA6=2.6750V	0xC6=3.0750V	0xE6=3.4750V
0x07=0.6875V	0x27=1.0875V	0x47=1.4875V	0x67=1.8875V	0x87=2.2875V	0xA7=2.6875V	0xC7=3.0875V	0xE7=3.4875V
0x08=0.7000V	0x28=1.1000V	0x48=1.5000V	0x68=1.9000V	0x88=2.3000V	0xA8=2.7000V	0xC8=3.1000V	0xE8=3.5000V
0x09=0.7125V	0x29=1.1125V	0x49=1.5125V	0x69=1.9125V	0x89=2.3125V	0xA9=2.7125V	0xC9=3.1125V	0xE9=3.5125V
0x0A=0.7250V	0x2A=1.1250V	0x4A=1.5250V	0x6A=1.9250V	0x8A=2.3250V	0xAA=2.7250V	0xCA=3.1250V	0xEA=3.5250V
0x0B=0.7375V	0x2B=1.1375V	0x4B=1.5375V	0x6B=1.9375V	0x8B=2.3375V	0xAB=2.7375V	0xCB=3.1375V	0xEB=3.5375V
0x0C=0.7500V	0x2C=1.1500V	0x4C=1.5500V	0x6C=1.9500V	0x8C=2.3500V	0xAC=2.7500V	0xCC=3.1500V	0xEC=3.5500V
0x0D=0.7625V	0x2D=1.1625V	0x4D=1.5625V	0x6D=1.9625V	0x8D=2.3625V	0xAD=2.7625V	0xCD=3.1625V	0xED=3.5625V
0x0E=0.7750V	0x2E=1.1750V	0x4E=1.5750V	0x6E=1.9750V	0x8E=2.3750V	0xAE=2.7750V	0xCE=3.1750V	0xEE=3.5750V
0x0F=0.7875V	0x2F=1.1875V	0x4F=1.5875V	0x6F=1.9875V	0x8F=2.3875V	0xAF=2.7875V	0xCF=3.1875V	0xEF=3.5875V
0x10=0.8000V	0x30=1.2000V	0x50=1.6000V	0x70=2.0000V	0x90=2.4000V	0xB0=2.8000V	0xD0=3.2000V	0xF0=3.6000V
0x11=0.8125V	0x31=1.2125V	0x51=1.6125V	0x71=2.0125V	0x91=2.4125V	0xB1=2.8125V	0xD1=3.2125V	0xF1=3.6125V
0x12=0.8250V	0x32=1.2250V	0x52=1.6250V	0x72=2.0250V	0x92=2.4250V	0xB2=2.8250V	0xD2=3.2250V	0xF2=3.6250V
0x13=0.8375V	0x33=1.2375V	0x53=1.6375V	0x73=2.0375V	0x93=2.4375V	0xB3=2.8375V	0xD3=3.2375V	0xF3=3.6375V
0x14=0.8500V	0x34=1.2500V	0x54=1.6500V	0x74=2.0500V	0x94=2.4500V	0xB4=2.8500V	0xD4=3.2500V	0xF4=3.6500V
0x15=0.8625V	0x35=1.2625V	0x55=1.6625V	0x75=2.0625V	0x95=2.4625V	0xB5=2.8625V	0xD5=3.2625V	0xF5=3.6625V
0x16=0.8750V	0x36=1.2750V	0x56=1.6750V	0x76=2.0750V	0x96=2.4750V	0xB6=2.8750V	0xD6=3.2750V	0xF6=3.6750V
0x17=0.8875V	0x37=1.2875V	0x57=1.6875V	0x77=2.0875V	0x97=2.4875V	0xB7=2.8875V	0xD7=3.2875V	0xF7=3.6875V
0x18=0.9000V	0x38=1.3000V	0x58=1.7000V	0x78=2.1000V	0x98=2.5000V	0xB8=2.9000V	0xD8=3.3000V	0xF8=3.7000V
0x19=0.9125V	0x39=1.3125V	0x59=1.7125V	0x79=2.1125V	0x99=2.5125V	0xB9=2.9125V	0xD9=3.3125V	0xF9=3.7125V
0x1A=0.9250V	0x3A=1.3250V	0x5A=1.7250V	0x7A=2.1250V	0x9A=2.5250V	0xBA=2.9250V	0xDA=3.3250V	0xFA=3.7250V
0x1B=0.9375V	0x3B=1.3375V	0x5B=1.7375V	0x7B=2.1375V	0x9B=2.5375V	0xBB=2.9375V	0xDB=3.3375V	0xFB=3.7375V
0x1C=0.9500V	0x3C=1.3500V	0x5C=1.7500V	0x7C=2.1500V	0x9C=2.5500V	0xBC=2.9500V	0xDC=3.3500V	0xFC=3.7500V
0x1D=0.9625V	0x3D=1.3625V	0x5D=1.7625V	0x7D=2.1625V	0x9D=2.5625V	0xBD=2.9625V	0xDD=3.3625V	0xFD=3.7625V
0x1E=0.9750V	0x3E=1.3750V	0x5E=1.7750V	0x7E=2.1750V	0x9E=2.5750V	0xBE=2.9750V	0xDE=3.3750V	0xFE=3.7750V
0x1F=0.9875V	0x3F=1.3875V	0x5F=1.7875V	0x7F=2.1875V	0x9F=2.5875V	0xBF=2.9875V	0xDF=3.3875V	0xFF=3.7875V

BUCK4CTRL1

ON/OFF Control for BUCK4, Active Discharge, ramp rate and PWM

Address (hex)	MODE		Type: O	RESET:0x72
26	R/W			
BIT	**Name**	**POR**	**Description**	
7:6	RAMP	01	Programs the BUCK4 rising ramp rate in mV/us 00: 13.75mV/µs Ramp Rate **01: 27.5mV/µs Ramp Rate** 10: 55mV/µs Ramp Rate 11: No slew rate control. Buck output voltage increases as fast as the current limit allows.	
5:4	BUCK4EN	11	00: OFF (regardless of PWRREQ) 01: Output ON/OFF controlled by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode(Remote Sense enabled) PWRREQ=L (0) : Output OFF 10: Low Power Mode. Be forced into low-power mode. The Max load current is 5mA and the quiescent supply current is 5uA. **11: ON in normal mode (Regardless of PWRREQ)** (Remote Sense enabled)	
3	SD4DIS	0	**0: Active discharge ON** 1: Active discharge OFF	
2	FPWM	0	Forced PWM **0: Turn forced PWM OFF** **(automatically skip pulse under light load)** Regulator skips pulses under light load conditions, and operates at a fixed frequency with medium to heavy load conditions. The regulator automatically transitions between pulse skipping and fixed frequency as needed. 1: Turn forced PWM on (with fixed frequency under all load conditions)	
1	ROVS_EN_B4	1	BUCK4 Remote Output Voltage Sense Enable 0= Disabled **1= Enabled** Note that when BUCK4 is operating in low-power mode, the ROVS function is automatically disabled however; this bit will not be affected. If this bit is set, then ROVS will automatically be re-enabled when BUCK4 enters its normal operating mode.	
0	nFSRADE_B4	0	Active-Low SDx Falling Slew Rate Active-Discharge Enable. **0= Active-Discharge Enabled. BUCK4 operates in forced PWM mode during the time the output voltage decreases. With forced PWM mode enabled, BUCK4 can sink current from the output capacitor to ensure that the output voltage falls at the rate programmed by RAMP[1:0]. To ensure a smooth output voltage decrease, the PMW mode will remain engaged for 50us after the output voltage decreases to its target voltage.** 1= Active Discharge Disabled. BUCK4 is allowed to operate in skip mode during the time the output voltage decreases (only if FPWM=0). In skip mode, BUCK4 cannot sink current from the output capacitor. Since BUCK4 cannot sink current in skip mode the output voltage falling slew rate is a function of the external load on BUCK4. If the external load on BUCK4 is heavy, then the output voltage falling slew rate will be the rate programmed by RAMP[1:0]. If the external load on BUCK4 is light, then the output voltage falling slew rate will be a function of the output capacitance and the external load. Note that the BUCK4 internal feedback string will always impose a 2uA load on the output.	

BUCK4DVS1

Control for BUCK4 Output in DVS3=DVS2=DVS1=LOW

Address (hex)	MODE		Type: O	RESET:0x20
28	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B4DVS	0010 0000	BUCK4 Output Voltage when DVS3=DVS2=DVS1=LOW	

Note that the output voltage is controlled by this register when the DVS function is disabled.

BUCK4DVS2

Control for BUCK4 Output in DVS3=DVS2=LOW, DVS1=HIGH

Address (hex)	MODE		Type: O	RESET:0x20
29	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B4DVS	0010 0000	BUCK4 Output Voltage when DVS3=DVS2=LOW, DVS1=HIGH	

BUCK4DVS3

Control for BUCK4 Output in DVS3=LOW, DVS2=HIGH, DVS1=LOW

Address (hex)	MODE		Type: O	RESET:0x20
2A	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B4DVS	0010 0000	BUCK4 Output Voltage when DVS3=LOW, DVS2=HIGH, DVS1=LOW	

BUCK4DVS4

Control for BUCK4 Output in DVS3=LOW, DVS2=DVS1=HIGH

Address (hex)	MODE		Type: O	RESET:0x20
2B	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B4DVS	0010 0000	BUCK4 Output Voltage when DVS3=LOW, DVS2=DVS1=HIGH	

BUCK4DVS5

Control for BUCK4 Output in DVS3=HIGH, DVS2=DVS1=LOW

Address (hex)	MODE		Type: O	RESET:0x20
2C	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B4DVS	0010 0000	BUCK4 Output Voltage when DVS3=HIGH, DVS2=DVS1=LOW	

BUCK4DVS6

Control for BUCK4 Output in DVS3=HIGH, DVS2=LOW, DVS1=HIGH

Address (hex)	MODE		Type: O	RESET:0x20
2D	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B4DVS	0010 0000	BUCK4 Output Voltage when	

BUCK4DVS7

Control for BUCK4 Output in DVS3=DVS2=HIGH, DVS1=LOW

Address (hex)	MODE		Type: O	RESET:0x20
2E	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B4DVS	0010 0000	BUCK4 Output Voltage when DVS3=DVS2=HIGH, DVS1=LOW	

BUCK4DVS8

Control for BUCK4 Output in DVS3=DVS2=DVS1=HIGH

Address (hex)	MODE		Type: O	RESET:0x20
2F	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:0	B4DVS	0010 0000	BUCK4 Output Voltage when DVS3=DVS2=DVS1=HIGH	

BUCK4 Output Voltage Table

0x00=0.6000V	**0x20=1.0000V**	0x40=1.4000V	0x60=1.8000V	0x80=2.2000V	0xA0=2.6000V	0xC0=3.0000V	0xE0=3.4000V
0x01=0.6125V	0x21=1.0125V	0x41=1.4125V	0x61=1.8125V	0x81=2.2125V	0xA1=2.6125V	0xC1=3.0125V	0xE1=3.4125V
0x02=0.6250V	0x22=1.0250V	0x42=1.4250V	0x62=1.8250V	0x82=2.2250V	0xA2=2.6250V	0xC2=3.0250V	0xE2=3.4250V
0x03=0.6375V	0x23=1.0375V	0x43=1.4375V	0x63=1.8375V	0x83=2.2375V	0xA3=2.6375V	0xC3=3.0375V	0xE3=3.4375V
0x04=0.6500V	0x24=1.0500V	0x44=1.4500V	0x64=1.8500V	0x84=2.2500V	0xA4=2.6500V	0xC4=3.0500V	0xE4=3.4500V
0x05=0.6625V	0x25=1.0625V	0x45=1.4625V	0x65=1.8625V	0x85=2.2625V	0xA5=2.6625V	0xC5=3.0625V	0xE5=3.4625V
0x06=0.6750V	0x26=1.0750V	0x46=1.4750V	0x66=1.8750V	0x86=2.2750V	0xA6=2.6750V	0xC6=3.0750V	0xE6=3.4750V
0x07=0.6875V	0x27=1.0875V	0x47=1.4875V	0x67=1.8875V	0x87=2.2875V	0xA7=2.6875V	0xC7=3.0875V	0xE7=3.4875V
0x08=0.7000V	0x28=1.1000V	0x48=1.5000V	0x68=1.9000V	0x88=2.3000V	0xA8=2.7000V	0xC8=3.1000V	0xE8=3.5000V
0x09=0.7125V	0x29=1.1125V	0x49=1.5125V	0x69=1.9125V	0x89=2.3125V	0xA9=2.7125V	0xC9=3.1125V	0xE9=3.5125V
0x0A=0.7250V	0x2A=1.1250V	0x4A=1.5250V	0x6A=1.9250V	0x8A=2.3250V	0xAA=2.7250V	0xCA=3.1250V	0xEA=3.5250V
0x0B=0.7375V	0x2B=1.1375V	0x4B=1.5375V	0x6B=1.9375V	0x8B=2.3375V	0xAB=2.7375V	0xCB=3.1375V	0xEB=3.5375V
0x0C=0.7500V	0x2C=1.1500V	0x4C=1.5500V	0x6C=1.9500V	0x8C=2.3500V	0xAC=2.7500V	0xCC=3.1500V	0xEC=3.5500V
0x0D=0.7625V	0x2D=1.1625V	0x4D=1.5625V	0x6D=1.9625V	0x8D=2.3625V	0xAD=2.7625V	0xCD=3.1625V	0xED=3.5625V
0x0E=0.7750V	0x2E=1.1750V	0x4E=1.5750V	0x6E=1.9750V	0x8E=2.3750V	0xAE=2.7750V	0xCE=3.1750V	0xEE=3.5750V
0x0F=0.7875V	0x2F=1.1875V	0x4F=1.5875V	0x6F=1.9875V	0x8F=2.3875V	0xAF=2.7875V	0xCF=3.1875V	0xEF=3.5875V
0x10=0.8000V	0x30=1.2000V	0x50=1.6000V	0x70=2.0000V	0x90=2.4000V	0xB0=2.8000V	0xD0=3.2000V	0xF0=3.6000V
0x11=0.8125V	0x31=1.2125V	0x51=1.6125V	0x71=2.0125V	0x91=2.4125V	0xB1=2.8125V	0xD1=3.2125V	0xF1=3.6125V
0x12=0.8250V	0x32=1.2250V	0x52=1.6250V	0x72=2.0250V	0x92=2.4250V	0xB2=2.8250V	0xD2=3.2250V	0xF2=3.6250V
0x13=0.8375V	0x33=1.2375V	0x53=1.6375V	0x73=2.0375V	0x93=2.4375V	0xB3=2.8375V	0xD3=3.2375V	0xF3=3.6375V
0x14=0.8500V	0x34=1.2500V	0x54=1.6500V	0x74=2.0500V	0x94=2.4500V	0xB4=2.8500V	0xD4=3.2500V	0xF4=3.6500V
0x15=0.8625V	0x35=1.2625V	0x55=1.6625V	0x75=2.0625V	0x95=2.4625V	0xB5=2.8625V	0xD5=3.2625V	0xF5=3.6625V
0x16=0.8750V	0x36=1.2750V	0x56=1.6750V	0x76=2.0750V	0x96=2.4750V	0xB6=2.8750V	0xD6=3.2750V	0xF6=3.6750V
0x17=0.8875V	0x37=1.2875V	0x57=1.6875V	0x77=2.0875V	0x97=2.4875V	0xB7=2.8875V	0xD7=3.2875V	0xF7=3.6875V
0x18=0.9000V	0x38=1.3000V	0x58=1.7000V	0x78=2.1000V	0x98=2.5000V	0xB8=2.9000V	0xD8=3.3000V	0xF8=3.7000V
0x19=0.9125V	0x39=1.3125V	0x59=1.7125V	0x79=2.1125V	0x99=2.5125V	0xB9=2.9125V	0xD9=3.3125V	0xF9=3.7125V
0x1A=0.9250V	0x3A=1.3250V	0x5A=1.7250V	0x7A=2.1250V	0x9A=2.5250V	0xBA=2.9250V	0xDA=3.3250V	0xFA=3.7250V
0x1B=0.9375V	0x3B=1.3375V	0x5B=1.7375V	0x7B=2.1375V	0x9B=2.5375V	0xBB=2.9375V	0xDB=3.3375V	0xFB=3.7375V
0x1C=0.9500V	0x3C=1.3500V	0x5C=1.7500V	0x7C=2.1500V	0x9C=2.5500V	0xBC=2.9500V	0xDC=3.3500V	0xFC=3.7500V
0x1D=0.9625V	0x3D=1.3625V	0x5D=1.7625V	0x7D=2.1625V	0x9D=2.5625V	0xBD=2.9625V	0xDD=3.3625V	0xFD=3.7625V
0x1E=0.9750V	0x3E=1.3750V	0x5E=1.7750V	0x7E=2.1750V	0x9E=2.5750V	0xBE=2.9750V	0xDE=3.3750V	0xFE=3.7750V
0x1F=0.9875V	0x3F=1.3875V	0x5F=1.7875V	0x7F=2.1875V	0x9F=2.5875V	0xBF=2.9875V	0xDF=3.3875V	0xFF=3.7875V

BUCK5CTRL

ON/OFF Control for BUCK5, Active Discharge and PWM

Address (hex)	MODE		Type: O	RESET:0x0B
30	R/W			
BIT	**Name**	**POR**	**Description**	
7:4	reserved	0000	Write “0000”	
3	SD5DIS	1	0: Active discharge OFF **1: Active discharge ON**	
2	FPWM	0	Forced PWM **0: Turn forced PWM OFF** **(automatically skip pulse under light load)** 1: Turn forced PWM on	
1:0	BUCK5EN	11	00, 01 & 10: Turn BUCK5 Off **11: Turn BUCK5 On**	

BUCK5OUT

Control for BUCK5 Output

Address (hex)	MODE		Type: O	RESET:0x09 in VSETB51/2=L/L RESET:0x0C in VSETB51/2=L/H RESET:0x0F in VSETB51/2=H/L RESET:0x15 in VSETB51/2=H/H
31	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:6	Reserved	00	Write “00” to these bits	
5:0	B5OUT	00 1001 (VSETB51/2=L/L) 00 1100 (VSETB51/2=L/H) 00 1111 (VSETB51/2=H/L) 01 0101 (VSETB51/2=HIGH)	BUCK5 Output Voltage depending on VSETB51 & VSETB52. This output voltage is also overwritten by I^{2}C once it’s set to one of the conditions.	

0x00: 0.75V	0x10: 1.55V	0x20: 2.35V	0x30: 3.15V
0x01: 0.80V	0x11: 1.60V	0x21: 2.40V	0x31: 3.20V
0x02: 0.85V	0x12: 1.65V	0x22: 2.45V	0x32: 3.25V
0x03: 0.90V	0x13: 1.70V	0x23: 2.50V	0x33: 3.30V
0x04: 0.95V	0x14: 1.75V	0x24: 2.55V	0x34: 3.35V
0x05: 1.00V	**0x15: 1.80V**	0x25: 2.60V	0x35: 3.40V
0x06: 1.05V	0x16: 1.85V	0x26: 2.65V	0x36: 3.45V
0x07: 1.10V	0x17: 1.90V	0x27: 2.70V	0x37: 3.50V
0x08: 1.15V	0x18: 1.95V	0x28: 2.75V	0x38: 3.55V
0x09: 1.20V	0x19: 2.00V	0x29: 2.80V	0x39: 3.60V
0x0A: 1.25V	0x1A: 2.05V	0x2A: 2.85V	0x3A: 3.65V
0x0B: 1.30V	0x1B: 2.10V	0x2B: 2.90V	0x3B: 3.70V
0x0C: 1.35V	0x1C: 2.15V	0x2C: 2.95V	0x3C: 3.75V
0x0D: 1.40V	0x1D: 2.20V	0x2D: 3.00V	0x3D: 3.80V
0x0E: 1.45V	0x1E: 2.25V	0x2E: 3.05V	0x3E: 3.85V
0x0F: 1.50V	0x1F: 2.30V	0x2F: 3.10V	0x3F: 3.90V

BUCK6CTRL

ON/OFF Control for BUCK6, Active Discharge and PWM

Address (hex)	MODE		Type: O	RESET:0x0B
32	R/W			
BIT	**Name**	**POR**	**Description**	
7:4	reserved	0000	Write “0000”	
3	SD6DIS	1	0: Active discharge OFF **1: Active discharge ON**	
2	FPWM	0	Forced PWM **0: Turn forced PWM OFF** **(automatically skip pulse under light load)** 1: Turn forced PWM on	
1:0	BUCK6EN	11	00, 01 & 10: Turn BUCK6 Off **11: Turn BUCK6 On**	

BUCK6OUT

Control for BUCK6 Output

Address (hex)	MODE		Type: O	RESET:0x0C
33	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:6	Reserved	00	Write “00” to these bits	
5:0	B6OUT	00 1100	BUCK6 Output Voltage	

0x00: 0.75V	0x10: 1.55V	0x20: 2.35V	0x30: 3.15V
0x01: 0.80V	0x11: 1.60V	0x21: 2.40V	0x31: 3.20V
0x02: 0.85V	0x12: 1.65V	0x22: 2.45V	0x32: 3.25V
0x03: 0.90V	0x13: 1.70V	0x23: 2.50V	0x33: 3.30V
0x04: 0.95V	0x14: 1.75V	0x24: 2.55V	0x34: 3.35V
0x05: 1.00V	0x15: 1.80V	0x25: 2.60V	0x35: 3.40V
0x06: 1.05V	0x16: 1.85V	0x26: 2.65V	0x36: 3.45V
0x07: 1.10V	0x17: 1.90V	0x27: 2.70V	0x37: 3.50V
0x08: 1.15V	0x18: 1.95V	0x28: 2.75V	0x38: 3.55V
0x09: 1.20V	0x19: 2.00V	0x29: 2.80V	0x39: 3.60V
0x0A: 1.25V	0x1A: 2.05V	0x2A: 2.85V	0x3A: 3.65V
0x0B: 1.30V	0x1B: 2.10V	0x2B: 2.90V	0x3B: 3.70V
0x0C: 1.35V	0x1C: 2.15V	0x2C: 2.95V	0x3C: 3.75V
0x0D: 1.40V	0x1D: 2.20V	0x2D: 3.00V	0x3D: 3.80V
0x0E: 1.45V	0x1E: 2.25V	0x2E: 3.05V	0x3E: 3.85V
0x0F: 1.50V	0x1F: 2.30V	0x2F: 3.10V	0x3F: 3.90V

BUCK7CTRL

ON/OFF Control for BUCK7, Active Discharge and PWM

Address (hex)	MODE		Type: O	RESET:0x0B
34	R/W			
BIT	**Name**	**POR**	**Description**	
7:4	reserved	0000	Write “0000”	
3	SD7DIS	1	0: Active discharge OFF **1: Active discharge ON**	
2	FPWM	0	Forced PWM **0: Turn forced PWM OFF** **(automatically skip pulse under light load)** 1: Turn forced PWM on	
1:0	BUCK7EN	11	00, 01 & 10: Turn BUCK7 Off **11: Turn BUCK7 On**	

BUCK7OUT

Control for BUCK7 Output

Address (hex)	MODE		Type: O	RESET:0x19
35	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:6	Reserved	00	Write “00” to these bits	
5:0	B7OUT	01 1001	BUCK7 Output Voltage	

0x00: 0.75V	0x10: 1.55V	0x20: 2.35V	0x30: 3.15V
0x01: 0.80V	0x11: 1.60V	0x21: 2.40V	0x31: 3.20V
0x02: 0.85V	0x12: 1.65V	0x22: 2.45V	0x32: 3.25V
0x03: 0.90V	0x13: 1.70V	0x23: 2.50V	0x33: 3.30V
0x04: 0.95V	0x14: 1.75V	0x24: 2.55V	0x34: 3.35V
0x05: 1.00V	0x15: 1.80V	0x25: 2.60V	0x35: 3.40V
0x06: 1.05V	0x16: 1.85V	0x26: 2.65V	0x36: 3.45V
0x07: 1.10V	0x17: 1.90V	0x27: 2.70V	0x37: 3.50V
0x08: 1.15V	0x18: 1.95V	0x28: 2.75V	0x38: 3.55V
0x09: 1.20V	**0x19: 2.00V**	0x29: 2.80V	0x39: 3.60V
0x0A: 1.25V	0x1A: 2.05V	0x2A: 2.85V	0x3A: 3.65V
0x0B: 1.30V	0x1B: 2.10V	0x2B: 2.90V	0x3B: 3.70V
0x0C: 1.35V	0x1C: 2.15V	0x2C: 2.95V	0x3C: 3.75V
0x0D: 1.40V	0x1D: 2.20V	0x2D: 3.00V	0x3D: 3.80V
0x0E: 1.45V	0x1E: 2.25V	0x2E: 3.05V	0x3E: 3.85V
0x0F: 1.50V	0x1F: 2.30V	0x2F: 3.10V	0x3F: 3.90V

BUCK8CTRL

ON/OFF Control for BUCK8, Active Discharge and PWM

Address (hex)	MODE	Type: O	RESET:0x08

36	R/W		
BIT	**Name**	**POR**	**Description**
7:4	reserved	0000	Write “0000”
3	SD8DIS	1	0: Active discharge OFF **1: Active discharge ON**
2	FPWM	0	Forced PWM **0: Turn forced PWM OFF** **(automatically skip pulse under light load)** 1: Turn forced PWM on
1:0	BUCK8EN	00	00, 01 & 10: Turn BUCK8 Off **(when ENB8=Low)** **11: Turn BUCK8 On** (regardless of ENB8)

BUCK8OUT

Control for BUCK8 Output

Address (hex)	**MODE**		Type: O	**RESET:0x2A**
37	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:6	reserved	00	Write “00” to these bits	
5:0	B8OUT	10 1010	BUCK8 Output Voltage	

0x00: 0.75V	0x10: 1.55V	0x20: 2.35V	0x30: 3.15V
0x01: 0.80V	0x11: 1.60V	0x21: 2.40V	0x31: 3.20V
0x02: 0.85V	0x12: 1.65V	0x22: 2.45V	0x32: 3.25V
0x03: 0.90V	0x13: 1.70V	0x23: 2.50V	0x33: 3.30V
0x04: 0.95V	0x14: 1.75V	0x24: 2.55V	0x34: 3.35V
0x05: 1.00V	0x15: 1.80V	0x25: 2.60V	0x35: 3.40V
0x06: 1.05V	0x16: 1.85V	0x26: 2.65V	0x36: 3.45V
0x07: 1.10V	0x17: 1.90V	0x27: 2.70V	0x37: 3.50V
0x08: 1.15V	0x18: 1.95V	0x28: 2.75V	0x38: 3.55V
0x09: 1.20V	0x19: 2.00V	0x29: 2.80V	0x39: 3.60V
0x0A: 1.25V	0x1A: 2.05V	0x2A: 2.85V	0x3A: 3.65V
0x0B: 1.30V	0x1B: 2.10V	0x2B: 2.90V	0x3B: 3.70V
0x0C: 1.35V	0x1C: 2.15V	0x2C: 2.95V	0x3C: 3.75V
0x0D: 1.40V	0x1D: 2.20V	0x2D: 3.00V	0x3D: 3.80V
0x0E: 1.45V	0x1E: 2.25V	0x2E: 3.05V	0x3E: 3.85V
0x0F: 1.50V	0x1F: 2.30V	0x2F: 3.10V	0x3F: 3.90V

BUCK9CTRL

ON/OFF Control for BUCK8, Active Discharge and PWM

Address (hex)	**MODE**	Type: O	**RESET:0x08**

38	R/W		
BIT	**Name**	**POR**	**Description**
7:4	reserved	0000	Write “0000”
3	SD9DIS	1	0: Active discharge OFF **1: Active discharge ON**
2	FPWM	0	Forced PWM **0: Turn forced PWM OFF** **(automatically skip pulse under light load)** 1: Turn forced PWM on
1:0	BUCK9EN	00	**00, 01 & 10: TURN BUCK9 OFF (when ENB9=Low)** 11: TURN BUC9 ON (regardless of ENB9)

BUCK9OUT

Control for BUCK9 Output

Address (hex)	**MODE**		Type: O	**RESET:0x09**
39	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:6	reserved	00	Write “00” to these bits	
5:0	B9OUT	00 1001	BUCK9 Output Voltage	

0x00: 0.75V	0x10: 1.55V	0x20: 2.35V	0x30: 3.15V
0x01: 0.80V	0x11: 1.60V	0x21: 2.40V	0x31: 3.20V
0x02: 0.85V	0x12: 1.65V	0x22: 2.45V	0x32: 3.25V
0x03: 0.90V	0x13: 1.70V	0x23: 2.50V	0x33: 3.30V
0x04: 0.95V	0x14: 1.75V	0x24: 2.55V	0x34: 3.35V
0x05: 1.00V	0x15: 1.80V	0x25: 2.60V	0x35: 3.40V
0x06: 1.05V	0x16: 1.85V	0x26: 2.65V	0x36: 3.45V
0x07: 1.10V	0x17: 1.90V	0x27: 2.70V	0x37: 3.50V
0x08: 1.15V	0x18: 1.95V	0x28: 2.75V	0x38: 3.55V
0x09: 1.20V	0x19: 2.00V	0x29: 2.80V	0x39: 3.60V
0x0A: 1.25V	0x1A: 2.05V	0x2A: 2.85V	0x3A: 3.65V
0x0B: 1.30V	0x1B: 2.10V	0x2B: 2.90V	0x3B: 3.70V
0x0C: 1.35V	0x1C: 2.15V	0x2C: 2.95V	0x3C: 3.75V
0x0D: 1.40V	0x1D: 2.20V	0x2D: 3.00V	0x3D: 3.80V
0x0E: 1.45V	0x1E: 2.25V	0x2E: 3.05V	0x3E: 3.85V
0x0F: 1.50V	0x1F: 2.30V	0x2F: 3.10V	0x3F: 3.90V

0x3A-0x3F are reserved

LDO Registers

LDO1CTRL1

Control OUT1 (LDO1) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0xC8**
40	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	11	00: OFF 01: Output ON in Low Power Mode 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode**
5:0	L01_TV	00 1000	Output Voltage

0x00: 0.800V	0x10: 1.200V	0x20: 1.600V	0x30: 2.000V
0x01: 0.825V	0x11: 1.225V	0x21: 1.625V	0x31: 2.025V
0x02: 0.850V	0x12: 1.250V	0x22: 1.650V	0x32: 2.050V
0x03: 0.875V	0x13: 1.275V	0x23: 1.675V	0x33: 2.075V
0x04: 0.900V	0x14: 1.300V	0x24: 1.700V	0x34: 2.100V
0x05: 0.925V	0x15: 1.325V	0x25: 1.725V	0x35: 2.125V
0x06: 0.950V	0x16: 1.350V	0x26: 1.750V	0x36: 2.150V
0x07: 0.975V	0x17: 1.375V	0x27: 1.775V	0x37: 2.175V
0x08: 1.000V	0x18: 1.400V	0x28: 1.800V	0x38: 2.200V
0x09: 1.025V	0x19: 1.425V	0x29: 1.825V	0x39: 2.225V
0x0A: 1.050V	0x1A: 1.450V	0x2A: 1.850V	0x3A: 2.250V
0x0B: 1.075V	0x1B: 1.475V	0x2B: 1.875V	0x3B: 2.275V
0x0C: 1.100V	0x1C: 1.500V	0x2C: 1.900V	0x3C: 2.300V
0x0D: 1.125V	0x1D: 1.525V	0x2D: 1.925V	0x3D: 2.325V
0x0E: 1.150V	0x1E: 1.550V	0x2E: 1.950V	0x3E: 2.350V
0x0F: 1.175V	0x1F: 1.575V	0x2F: 1.975V	0x3F: 2.375V

LDO1CTRL2

Control OUT1 (LDO1) Active Discharge and Compensation

Address (hex)	Type: O			**RESET:0x9A**
60				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L01OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	reserved	01	R/W	Write “01” to these bits
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO1	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO2CTRL1

Control OUT2 (LDO2) ON/OFF and Programmable Output

Address (hex)	MODE		Type: O	RESET: depend on VSETB51/2 condition
41	R/W			
BIT	**Name**	**POR**	**Description**	
7:6	OPMODE	11	00: OFF (regardless of PWRREQ) 01: Output ON/OFF controlled by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output OFF 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode (Regardless of PWRREQ)**	
5:0	L02_TV	01 0000 (VSETB51/2=L/L) 01 0110 (VSETB51/2=L/H) 01 1100 (VSETB51/2=H/L) 10 1000 (VSETB51/2=HIGH)	Output Voltage	

0x00: 0.800V	**0x10: 1.200V**	0x20: 1.600V	0x30: 2.000V
0x01: 0.825V	0x11: 1.225V	0x21: 1.625V	0x31: 2.025V
0x02: 0.850V	0x12: 1.250V	0x22: 1.650V	0x32: 2.050V
0x03: 0.875V	0x13: 1.275V	0x23: 1.675V	0x33: 2.075V
0x04: 0.900V	0x14: 1.300V	0x24: 1.700V	0x34: 2.100V
0x05: 0.925V	0x15: 1.325V	0x25: 1.725V	0x35: 2.125V
0x06: 0.950V	**0x16: 1.350V**	0x26: 1.750V	0x36: 2.150V
0x07: 0.975V	0x17: 1.375V	0x27: 1.775V	0x37: 2.175V
0x08: 1.000V	0x18: 1.400V	**0x28: 1.800V**	0x38: 2.200V
0x09: 1.025V	0x19: 1.425V	0x29: 1.825V	0x39: 2.225V
0x0A: 1.050V	0x1A: 1.450V	0x2A: 1.850V	0x3A: 2.250V
0x0B: 1.075V	0x1B: 1.475V	0x2B: 1.875V	0x3B: 2.275V
0x0C: 1.100V	**0x1C: 1.500V**	0x2C: 1.900V	0x3C: 2.300V
0x0D: 1.125V	0x1D: 1.525V	0x2D: 1.925V	0x3D: 2.325V
0x0E: 1.150V	0x1E: 1.550V	0x2E: 1.950V	0x3E: 2.350V
0x0F: 1.175V	0x1F: 1.575V	0x2F: 1.975V	0x3F: 2.375V

Note that the default of LDO2 is set by the status of VSETB51 and VSETB52.

LDO2CTRL2

Register for OUT2 (LDO2) Active Discharge and Compensation

Address (hex)	Type: O			RESET:0x9A
61				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L02OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	reserved	01	R/W	Write “01”
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO2	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO3CTRL1

Control OUT3 (LDO3) ON/OFF and Programmable Output

Address (hex)	MODE		Type: O	RESET:0xD4
42	R/W			
BIT	**Name**	**POR**	**Description**	
7:6	OPMODE	11	~~**00: OFF ; OFF**~~ **is not available for LDO3** 01: Output ON with Low Power Mode 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode**	
5:0	L03_TV	01 0100	Output Voltage	

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	**0x14: 1.80V**	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO3CTRL2

Control OUT3 (LDO3) Active Discharge and Compensation

Address (hex)	Type: O			RESET:0x9A
62				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L03OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L03_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO3	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO4CTRL1

Control OUT4 (LDO4) ON/OFF and Programmable Output

Address (hex)	MODE		Type: O	RESET:0xE8
43	R/W			
BIT	**Name**	**POR**	**Description**	
7:6	OPMODE	11	00: OFF 01: Output ON with Low Power Mode 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode**	
5:0	L04_TV	10 1000	Output Voltage	

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	**0x28: 2.80V**	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO4CTRL2

Control OUT4 (LDO4) Active Discharge and Compensation

Address (hex)	Type: O			RESET: 0x9A
63				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L04OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L04_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO4	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO5CTRL1

Control OUT5 (LDO5) ON/OFF and Programmable Output

Address (hex)	MODE		Type: O	RESET:0XD4
44	R/W			
BIT	**Name**	**POR**	**Description**	
7:6	OPMODE	11	00: OFF 01: Don't' use; ON in Normal Mode 10: Don't' use; On in Normal mode **11: ON in normal mode**	
5:0	L05_TV	01 0100	Output Voltage	

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	**0x14: 1.80V**	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO5CTRL2

Control OUT5 (LDO5) Active Discharge and Compensation

Address (hex)	Type: O			RESET: 0x1A
64				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L05OVCLMP_EN	0	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write "0" to this bit
5:4	L05_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	10	R	Write "10" to these bits
1	ADSLDO5	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write "0" to this bit

LDO6CTRL1

Control OUT6 (LDO6) ON/OFF and Programmable Output

Address (hex)	MODE	Type: O	RESET:0xCC

45	R/W		
BIT	**Name**	**POR**	**Description**
7:6	OPMODE	11	00: OFF (regardless of PWRREQ) 01: Output ON/OFF controlled by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output OFF 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode (Regardless of PWRREQ)**
5:0	L06_TV	00 1100	Output Voltage

0x00: 0.800V	0x10: 1.200V	0x20: 1.600V	0x30: 2.000V
0x01: 0.825V	0x11: 1.225V	0x21: 1.625V	0x31: 2.025V
0x02: 0.850V	0x12: 1.250V	0x22: 1.650V	0x32: 2.050V
0x03: 0.875V	0x13: 1.275V	0x23: 1.675V	0x33: 2.075V
0x04: 0.900V	0x14: 1.300V	0x24: 1.700V	0x34: 2.100V
0x05: 0.925V	0x15: 1.325V	0x25: 1.725V	0x35: 2.125V
0x06: 0.950V	0x16: 1.350V	0x26: 1.750V	0x36: 2.150V
0x07: 0.975V	0x17: 1.375V	0x27: 1.775V	0x37: 2.175V
0x08: 1.000V	0x18: 1.400V	0x28: 1.800V	0x38: 2.200V
0x09: 1.025V	0x19: 1.425V	0x29: 1.825V	0x39: 2.225V
0x0A: 1.050V	0x1A: 1.450V	0x2A: 1.850V	0x3A: 2.250V
0x0B: 1.075V	0x1B: 1.475V	0x2B: 1.875V	0x3B: 2.275V
0x0C: 1.100V	0x1C: 1.500V	0x2C: 1.900V	0x3C: 2.300V
0x0D: 1.125V	0x1D: 1.525V	0x2D: 1.925V	0x3D: 2.325V
0x0E: 1.150V	0x1E: 1.550V	0x2E: 1.950V	0x3E: 2.350V
0x0F: 1.175V	0x1F: 1.575V	0x2F: 1.975V	0x3F: 2.375V

LDO6CTRL2

Control OUT6 (LDO6) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x9A**
65				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L06OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	reserved	01	R/W	Write “01”
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO6	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO7CTRL1

Control OUT7 (LDO7) ON/OFF and Programmable Output

Address (hex)	**MODE**	Type: O	**RESET:0xCC**
46	R/W		

BIT	Name	POR	Description
7:6	OPMODE	11	00: OFF (regardless of PWRREQ) 01: Output ON/OFF controlled by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output OFF 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode (Regardless of PWRREQ)**
5:0	L07_TV	00 1100	Output Voltage

0x00: 0.800V	0x10: 1.200V	0x20: 1.600V	0x30: 2.000V
0x01: 0.825V	0x11: 1.225V	0x21: 1.625V	0x31: 2.025V
0x02: 0.850V	0x12: 1.250V	0x22: 1.650V	0x32: 2.050V
0x03: 0.875V	0x13: 1.275V	0x23: 1.675V	0x33: 2.075V
0x04: 0.900V	0x14: 1.300V	0x24: 1.700V	0x34: 2.100V
0x05: 0.925V	0x15: 1.325V	0x25: 1.725V	0x35: 2.125V
0x06: 0.950V	0x16: 1.350V	0x26: 1.750V	0x36: 2.150V
0x07: 0.975V	0x17: 1.375V	0x27: 1.775V	0x37: 2.175V
0x08: 1.000V	0x18: 1.400V	0x28: 1.800V	0x38: 2.200V
0x09: 1.025V	0x19: 1.425V	0x29: 1.825V	0x39: 2.225V
0x0A: 1.050V	0x1A: 1.450V	0x2A: 1.850V	0x3A: 2.250V
0x0B: 1.075V	0x1B: 1.475V	0x2B: 1.875V	0x3B: 2.275V
0x0C: 1.100V	0x1C: 1.500V	0x2C: 1.900V	0x3C: 2.300V
0x0D: 1.125V	0x1D: 1.525V	0x2D: 1.925V	0x3D: 2.325V
0x0E: 1.150V	0x1E: 1.550V	0x2E: 1.950V	0x3E: 2.350V
0x0F: 1.175V	0x1F: 1.575V	0x2F: 1.975V	0x3F: 2.375V

LDO7CTRL2

Control OUT7 (LDO7) Active Discharge and Compensation

Address (hex)	Type: O			RESET: 0x9A
66				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L07OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	reserved	01	R/W	Write “01”
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO7	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO8CTRL1

Control OUT8 (LDO8) ON/OFF and Programmable Output

Address (hex)	MODE	Type: O	RESET:0xC8
47	R/W		

BIT	Name	POR	Description
7:6	OPMODE	11	00: OFF (regardless of PWRREQ) 01: Output ON/OFF controlled by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output OFF 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode (Regardless of PWRREQ)**
5:0	L08_TV	00 1000	Output Voltage

0x00: 0.800V	0x10: 1.200V	0x20: 1.600V	0x30: 2.000V
0x01: 0.825V	0x11: 1.225V	0x21: 1.625V	0x31: 2.025V
0x02: 0.850V	0x12: 1.250V	0x22: 1.650V	0x32: 2.050V
0x03: 0.875V	0x13: 1.275V	0x23: 1.675V	0x33: 2.075V
0x04: 0.900V	0x14: 1.300V	0x24: 1.700V	0x34: 2.100V
0x05: 0.925V	0x15: 1.325V	0x25: 1.725V	0x35: 2.125V
0x06: 0.950V	0x16: 1.350V	0x26: 1.750V	0x36: 2.150V
0x07: 0.975V	0x17: 1.375V	0x27: 1.775V	0x37: 2.175V
0x08: 1.000V	0x18: 1.400V	0x28: 1.800V	0x38: 2.200V
0x09: 1.025V	0x19: 1.425V	0x29: 1.825V	0x39: 2.225V
0x0A: 1.050V	0x1A: 1.450V	0x2A: 1.850V	0x3A: 2.250V
0x0B: 1.075V	0x1B: 1.475V	0x2B: 1.875V	0x3B: 2.275V
0x0C: 1.100V	0x1C: 1.500V	0x2C: 1.900V	0x3C: 2.300V
0x0D: 1.125V	0x1D: 1.525V	0x2D: 1.925V	0x3D: 2.325V
0x0E: 1.150V	0x1E: 1.550V	0x2E: 1.950V	0x3E: 2.350V
0x0F: 1.175V	0x1F: 1.575V	0x2F: 1.975V	0x3F: 2.375V

LDO8CTRL2

Control OUT8 (LDO8) Active Discharge and Compensation

Address (hex)	Type: O			RESET: 0x9A
67				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L08OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	reserved	01	R/W	Write “01”
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO8	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO9CTRL1

Control OUT9 (LDO9) ON/OFF and Programmable Output

Address (hex)	MODE		Type: O	RESET:0x14
48	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	00	**00: OFF** 01: Output ON in Low Power Mode 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode 11: ON in normal mode
5:0	L09_TV	01 0100	Output Voltage

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	**0x14: 1.80V**	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO9CTRL2

Control OUT9 (LDO9) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x92**
68				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L09OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L09_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	00	R	Write “00” to these bits
1	ADSLDO9	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO10CTRL1

Control OUT10 (LDO10) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0xD4**
49	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	11	00: OFF (regardless of PWRREQ) 01: Output ON/OFF controlled by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output OFF 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode (Regardless of PWRREQ)**
5:0	L10_TV	01 0100	Output Voltage

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	**0x14: 1.80V**	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO10CTRL2

Control for OUT10 (LDO10) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x9A**
69				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L10OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L10_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO10	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO11CTRL1

Control OUT11 (LDO11) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0xD4**
4A	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	11	00: OFF (regardless of PWRREQ) 01: Output ON/OFF controlled by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output OFF 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode (Regardless of PWRREQ)**
5:0	L11_TV	01 0100	Output Voltage 0x00: 0.80V / 0x10: 1.60V / 0x20: 2.40V / 0x30: 3.20V 0x01: 0.85V / 0x11: 1.65V / 0x21: 2.45V / 0x31: 3.25V 0x02: 0.90V / 0x12: 1.70V / 0x22: 2.50V / 0x32: 3.30V 0x03: 0.95V / 0x13: 1.75V / 0x23: 2.55V / 0x33: 3.35V 0x04: 1.00V / **0x14: 1.80V** / 0x24: 2.60V / 0x34: 3.40V 0x05: 1.05V / 0x15: 1.85V / 0x25: 2.65V / 0x35: 3.45V 0x06: 1.10V / 0x16: 1.90V / 0x26: 2.70V / 0x36: 3.50V 0x07: 1.15V / 0x17: 1.95V / 0x27: 2.75V / 0x37: 3.55V 0x08: 1.20V / 0x18: 2.00V / 0x28: 2.80V / 0x38: 3.60V 0x09: 1.25V / 0x19: 2.05V / 0x29: 2.85V / 0x39: 3.65V 0x0A: 1.30V / 0x1A: 2.10V / 0x2A: 2.90V / 0x3A: 3.70V 0x0B: 1.35V / 0x1B: 2.15V / 0x2B: 2.95V / 0x3B: 3.75V 0x0C: 1.40V / 0x1C: 2.20V / 0x2C: 3.00V / 0x3C: 3.80V 0x0D: 1.45V / 0x1D: 2.25V / 0x2D: 3.05V / 0x3D: 3.85V 0x0E: 1.50V / 0x1E: 2.30V / 0x2E: 3.10V / 0x3E: 3.90V 0x0F: 1.55V / 0x1F: 2.35V / 0x2F: 3.15V / 0x3F: 3.95V

LDO11CTRL2

Control OUT11 (LDO11) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x9A**
6A				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L11OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L11_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO11	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO12CTRL1

Control OUT12 (LDO12) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0xEC**
4B	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	11	00: OFF (regardless of PWRREQ) 01: Output ON/OFF controlled by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output OFF 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode (Regardless of PWRREQ)**
5:0	L12_TV	10 1100	Output Voltage

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	**0x2C: 3.00V**	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO12CTRL2

Control OUT12 (LDO12) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x9A**
6B				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L12OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L12_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO12	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO13CTRL1

Control OUT13 (LDO13) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0XD4**
4C	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	11	00: OFF 01: ON in Low Power Mode 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode**
5:0	L13_TV	01 0100	Output Voltage

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	**0x14: 1.80V**	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO13CTRL2

Control OUT13 (LDO13) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x9A**
6C				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L13OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L13_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO13	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO14CTRL1

Control OUT14 (LDO14) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0xD4**
4D	R/W			
BIT	**Name**	**POR**	**Description**	

<table>
<tr><td>7:6</td><td>OPMODE</td><td>11</td><td>00: OFF (regardless of PWRREQ)

01: Output ON/OFF controlled by PWRREQ
PWRREQ=H (1) : Output ON in Normal Mode
PWRREQ=L (0) : Output OFF
10: Output ON with Low Power Mode by PWRREQ
PWRREQ=H (1) : Output ON in Normal Mode
PWRREQ=L (0) : Output ON in Low Power Mode

11: ON in normal mode (Regardless of PWRREQ)</td></tr>
<tr><td>5:0</td><td>L14_TV</td><td>01 0100</td><td>Output Voltage

<table>
<tr><td>0x00: 0.80V</td><td>0x10: 1.60V</td><td>0x20: 2.40V</td><td>0x30: 3.20V</td></tr>
<tr><td>0x01: 0.85V</td><td>0x11: 1.65V</td><td>0x21: 2.45V</td><td>0x31: 3.25V</td></tr>
<tr><td>0x02: 0.90V</td><td>0x12: 1.70V</td><td>0x22: 2.50V</td><td>0x32: 3.30V</td></tr>
<tr><td>0x03: 0.95V</td><td>0x13: 1.75V</td><td>0x23: 2.55V</td><td>0x33: 3.35V</td></tr>
<tr><td>0x04: 1.00V</td><td>0x14: 1.80V</td><td>0x24: 2.60V</td><td>0x34: 3.40V</td></tr>
<tr><td>0x05: 1.05V</td><td>0x15: 1.85V</td><td>0x25: 2.65V</td><td>0x35: 3.45V</td></tr>
<tr><td>0x06: 1.10V</td><td>0x16: 1.90V</td><td>0x26: 2.70V</td><td>0x36: 3.50V</td></tr>
<tr><td>0x07: 1.15V</td><td>0x17: 1.95V</td><td>0x27: 2.75V</td><td>0x37: 3.55V</td></tr>
<tr><td>0x08: 1.20V</td><td>0x18: 2.00V</td><td>0x28: 2.80V</td><td>0x38: 3.60V</td></tr>
<tr><td>0x09: 1.25V</td><td>0x19: 2.05V</td><td>0x29: 2.85V</td><td>0x39: 3.65V</td></tr>
<tr><td>0x0A: 1.30V</td><td>0x1A: 2.10V</td><td>0x2A: 2.90V</td><td>0x3A: 3.70V</td></tr>
<tr><td>0x0B: 1.35V</td><td>0x1B: 2.15V</td><td>0x2B: 2.95V</td><td>0x3B: 3.75V</td></tr>
<tr><td>0x0C: 1.40V</td><td>0x1C: 2.20V</td><td>0x2C: 3.00V</td><td>0x3C: 3.80V</td></tr>
<tr><td>0x0D: 1.45V</td><td>0x1D: 2.25V</td><td>0x2D: 3.05V</td><td>0x3D: 3.85V</td></tr>
<tr><td>0x0E: 1.50V</td><td>0x1E: 2.30V</td><td>0x2E: 3.10V</td><td>0x3E: 3.90V</td></tr>
<tr><td>0x0F: 1.55V</td><td>0x1F: 2.35V</td><td>0x2F: 3.15V</td><td>0x3F: 3.95V</td></tr>
</table>
</td></tr>
</table>

LDO14CTRL2

Control OUT14 (LDO14) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x9A**
6D				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L14OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L14_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO14	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO15CTRL1

Control OUT15 (LDO15) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0xC8**
4E	R/W			
BIT	**Name**	**POR**	**Description**	

<table>
<tr><td>7:6</td><td>OPMODE</td><td>11</td><td>00: OFF (regardless of PWRREQ)

01: Output ON/OFF controlled by PWRREQ
PWRREQ=H (1) : Output ON in Normal Mode
PWRREQ=L (0) : Output OFF
10: Output ON with Low Power Mode by PWRREQ
PWRREQ=H (1) : Output ON in Normal Mode
PWRREQ=L (0) : Output ON in Low Power Mode

11: ON in normal mode (Regardless of PWRREQ)</td></tr>
<tr><td>5:0</td><td>L15_TV</td><td>00 1000</td><td>Output Voltage

<table>
<tr><td>0x00: 0.800V</td><td>0x10: 1.200V</td><td>0x20: 1.600V</td><td>0x30: 2.000V</td></tr>
<tr><td>0x01: 0.825V</td><td>0x11: 1.225V</td><td>0x21: 1.625V</td><td>0x31: 2.025V</td></tr>
<tr><td>0x02: 0.850V</td><td>0x12: 1.250V</td><td>0x22: 1.650V</td><td>0x32: 2.050V</td></tr>
<tr><td>0x03: 0.875V</td><td>0x13: 1.275V</td><td>0x23: 1.675V</td><td>0x33: 2.075V</td></tr>
<tr><td>0x04: 0.900V</td><td>0x14: 1.300V</td><td>0x24: 1.700V</td><td>0x34: 2.100V</td></tr>
<tr><td>0x05: 0.925V</td><td>0x15: 1.325V</td><td>0x25: 1.725V</td><td>0x35: 2.125V</td></tr>
<tr><td>0x06: 0.950V</td><td>0x16: 1.350V</td><td>0x26: 1.750V</td><td>0x36: 2.150V</td></tr>
<tr><td>0x07: 0.975V</td><td>0x17: 1.375V</td><td>0x27: 1.775V</td><td>0x37: 2.175V</td></tr>
<tr><td>0x08: 1.000V</td><td>0x18: 1.400V</td><td>0x28: 1.800V</td><td>0x38: 2.200V</td></tr>
<tr><td>0x09: 1.025V</td><td>0x19: 1.425V</td><td>0x29: 1.825V</td><td>0x39: 2.225V</td></tr>
<tr><td>0x0A: 1.050V</td><td>0x1A: 1.450V</td><td>0x2A: 1.850V</td><td>0x3A: 2.250V</td></tr>
<tr><td>0x0B: 1.075V</td><td>0x1B: 1.475V</td><td>0x2B: 1.875V</td><td>0x3B: 2.275V</td></tr>
<tr><td>0x0C: 1.100V</td><td>0x1C: 1.500V</td><td>0x2C: 1.900V</td><td>0x3C: 2.300V</td></tr>
<tr><td>0x0D: 1.125V</td><td>0x1D: 1.525V</td><td>0x2D: 1.925V</td><td>0x3D: 2.325V</td></tr>
<tr><td>0x0E: 1.150V</td><td>0x1E: 1.550V</td><td>0x2E: 1.950V</td><td>0x3E: 2.350V</td></tr>
<tr><td>0x0F: 1.175V</td><td>0x1F: 1.575V</td><td>0x2F: 1.975V</td><td>0x3F: 2.375V</td></tr>
</table>
</td></tr>
</table>

LDO15CTRL2

Control OUT15 (LDO15) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x9A**
6E				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L15OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	reserved	01	R/W	Write “01”
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO15	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO16CTRL1

Control OUT16 (LDO16) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0xD4**
4F	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	11	00: OFF (regardless of PWRREQ) 01: Output ON/OFF controlled by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output OFF 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode **11: ON in normal mode (Regardless of PWRREQ)**
5:0	L16_TV	01 0100	Output Voltage

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	**0x14: 1.80V**	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO16CTRL2

Control OUT16 (LDO16) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x1A**
6F				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L16OVCLMP_EN	0	R/W	Overvoltage Clamp Enable **0=Overvoltage Clamp disabled** 1=Overvoltage Clamp enabled
6	reserved	0	R	Write “0” to this bit
5:4	L16_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	10	R	Write “10” to these bits
1	ADSLDO16	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO17CTRL1

Control OUT17 (LDO17) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0x08**
50	R/W			
BIT	**Name**	**POR**	**Description**	

<table>
<tr><td>7:6</td><td>OPMODE</td><td>00</td><td>00: OFF
01: ON in Low Power Mode
10: Output ON with Low Power Mode by PWRREQ
PWRREQ=H (1) : Output ON in Normal Mode
PWRREQ=L (0) : Output ON in Low Power Mode

11: ON in normal mode</td></tr>
<tr><td>5:0</td><td>L17_TV</td><td>00 1000</td><td>Output Voltage

<table>
<tr><td>0x00: 0.80V</td><td>0x10: 1.60V</td><td>0x20: 2.40V</td><td>0x30: 3.20V</td></tr>
<tr><td>0x01: 0.85V</td><td>0x11: 1.65V</td><td>0x21: 2.45V</td><td>0x31: 3.25V</td></tr>
<tr><td>0x02: 0.90V</td><td>0x12: 1.70V</td><td>0x22: 2.50V</td><td>0x32: 3.30V</td></tr>
<tr><td>0x03: 0.95V</td><td>0x13: 1.75V</td><td>0x23: 2.55V</td><td>0x33: 3.35V</td></tr>
<tr><td>0x04: 1.00V</td><td>0x14: 1.80V</td><td>0x24: 2.60V</td><td>0x34: 3.40V</td></tr>
<tr><td>0x05: 1.05V</td><td>0x15: 1.85V</td><td>0x25: 2.65V</td><td>0x35: 3.45V</td></tr>
<tr><td>0x06: 1.10V</td><td>0x16: 1.90V</td><td>0x26: 2.70V</td><td>0x36: 3.50V</td></tr>
<tr><td>0x07: 1.15V</td><td>0x17: 1.95V</td><td>0x27: 2.75V</td><td>0x37: 3.55V</td></tr>
<tr><td>0x08: 1.20V</td><td>0x18: 2.00V</td><td>0x28: 2.80V</td><td>0x38: 3.60V</td></tr>
<tr><td>0x09: 1.25V</td><td>0x19: 2.05V</td><td>0x29: 2.85V</td><td>0x39: 3.65V</td></tr>
<tr><td>0x0A: 1.30V</td><td>0x1A: 2.10V</td><td>0x2A: 2.90V</td><td>0x3A: 3.70V</td></tr>
<tr><td>0x0B: 1.35V</td><td>0x1B: 2.15V</td><td>0x2B: 2.95V</td><td>0x3B: 3.75V</td></tr>
<tr><td>0x0C: 1.40V</td><td>0x1C: 2.20V</td><td>0x2C: 3.00V</td><td>0x3C: 3.80V</td></tr>
<tr><td>0x0D: 1.45V</td><td>0x1D: 2.25V</td><td>0x2D: 3.05V</td><td>0x3D: 3.85V</td></tr>
<tr><td>0x0E: 1.50V</td><td>0x1E: 2.30V</td><td>0x2E: 3.10V</td><td>0x3E: 3.90V</td></tr>
<tr><td>0x0F: 1.55V</td><td>0x1F: 2.35V</td><td>0x2F: 3.15V</td><td>0x3F: 3.95V</td></tr>
</table>
</td></tr>
</table>

LDO17CTRL2

Control OUT17 (LDO17) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x92**
70				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L17OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L17_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	00	R	Write “00” to these bits
1	ADSLDO17	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO18CTRL1

Control OUT18 (LDO18) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0x14**
51	R/W			
BIT	**Name**	**POR**	**Description**	

<table>
<tr><td>7:6</td><td>OPMODE</td><td>00</td><td>00: OFF
01: ON in Low Power Mode
10: Output ON with Low Power Mode by PWRREQ
PWRREQ=H (1) : Output ON in Normal Mode
PWRREQ=L (0) : Output ON in Low Power Mode

11: ON in normal mode</td></tr>
<tr><td>5:0</td><td>L18_TV</td><td>01 0100</td><td>Output Voltage

<table>
<tr><td>0x00: 0.80V</td><td>0x10: 1.60V</td><td>0x20: 2.40V</td><td>0x30: 3.20V</td></tr>
<tr><td>0x01: 0.85V</td><td>0x11: 1.65V</td><td>0x21: 2.45V</td><td>0x31: 3.25V</td></tr>
<tr><td>0x02: 0.90V</td><td>0x12: 1.70V</td><td>0x22: 2.50V</td><td>0x32: 3.30V</td></tr>
<tr><td>0x03: 0.95V</td><td>0x13: 1.75V</td><td>0x23: 2.55V</td><td>0x33: 3.35V</td></tr>
<tr><td>0x04: 1.00V</td><td>0x14: 1.80V</td><td>0x24: 2.60V</td><td>0x34: 3.40V</td></tr>
<tr><td>0x05: 1.05V</td><td>0x15: 1.85V</td><td>0x25: 2.65V</td><td>0x35: 3.45V</td></tr>
<tr><td>0x06: 1.10V</td><td>0x16: 1.90V</td><td>0x26: 2.70V</td><td>0x36: 3.50V</td></tr>
<tr><td>0x07: 1.15V</td><td>0x17: 1.95V</td><td>0x27: 2.75V</td><td>0x37: 3.55V</td></tr>
<tr><td>0x08: 1.20V</td><td>0x18: 2.00V</td><td>0x28: 2.80V</td><td>0x38: 3.60V</td></tr>
<tr><td>0x09: 1.25V</td><td>0x19: 2.05V</td><td>0x29: 2.85V</td><td>0x39: 3.65V</td></tr>
<tr><td>0x0A: 1.30V</td><td>0x1A: 2.10V</td><td>0x2A: 2.90V</td><td>0x3A: 3.70V</td></tr>
<tr><td>0x0B: 1.35V</td><td>0x1B: 2.15V</td><td>0x2B: 2.95V</td><td>0x3B: 3.75V</td></tr>
<tr><td>0x0C: 1.40V</td><td>0x1C: 2.20V</td><td>0x2C: 3.00V</td><td>0x3C: 3.80V</td></tr>
<tr><td>0x0D: 1.45V</td><td>0x1D: 2.25V</td><td>0x2D: 3.05V</td><td>0x3D: 3.85V</td></tr>
<tr><td>0x0E: 1.50V</td><td>0x1E: 2.30V</td><td>0x2E: 3.10V</td><td>0x3E: 3.90V</td></tr>
<tr><td>0x0F: 1.55V</td><td>0x1F: 2.35V</td><td>0x2F: 3.15V</td><td>0x3F: 3.95V</td></tr>
</table>
</td></tr>
</table>

LDO18CTRL2

Control OUT18 (LDO18) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x92**
71				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L18OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L18_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	00	R	Write “00” to these bits
1	ADSLDO18	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO19CTRL1

Control for OUT19 (LDO19) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0x14**
52	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	00	**00: OFF** 01: ON in Low Power Mode 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode 11: ON in normal mode
5:0	L19_TV	01 0100	Output Voltage

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	**0x14: 1.80V**	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO19CTRL2

Control OUT19 (LDO19) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x92**
72				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L19OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L19_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	00	R	Write “00” to these bits
1	ADSLDO19	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO20CTRL1

Control for OUT20 (LDO20) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0x14**
53	R/W			
BIT	**Name**	**POR**	**Description**	

<table>
<tr><td>7:6</td><td>OPMODE</td><td>00</td><td>00: OFF (when ENL20=Low)

01: Output ON in Low Power Mode
10: Output ON with Low Power Mode by PWRREQ
PWRREQ=H (1) : Output ON in Normal Mode
PWRREQ=L (0) : Output ON in Low Power Mode

11: ON in normal mode (regardless of ENL20 status)</td></tr>
<tr><td>5:0</td><td>L20_TV</td><td>01 0100</td><td>Output Voltage

<table>
<tr><td>0x00: 0.80V</td><td>0x10: 1.60V</td><td>0x20: 2.40V</td><td>0x30: 3.20V</td></tr>
<tr><td>0x01: 0.85V</td><td>0x11: 1.65V</td><td>0x21: 2.45V</td><td>0x31: 3.25V</td></tr>
<tr><td>0x02: 0.90V</td><td>0x12: 1.70V</td><td>0x22: 2.50V</td><td>0x32: 3.30V</td></tr>
<tr><td>0x03: 0.95V</td><td>0x13: 1.75V</td><td>0x23: 2.55V</td><td>0x33: 3.35V</td></tr>
<tr><td>0x04: 1.00V</td><td>0x14: 1.80V</td><td>0x24: 2.60V</td><td>0x34: 3.40V</td></tr>
<tr><td>0x05: 1.05V</td><td>0x15: 1.85V</td><td>0x25: 2.65V</td><td>0x35: 3.45V</td></tr>
<tr><td>0x06: 1.10V</td><td>0x16: 1.90V</td><td>0x26: 2.70V</td><td>0x36: 3.50V</td></tr>
<tr><td>0x07: 1.15V</td><td>0x17: 1.95V</td><td>0x27: 2.75V</td><td>0x37: 3.55V</td></tr>
<tr><td>0x08: 1.20V</td><td>0x18: 2.00V</td><td>0x28: 2.80V</td><td>0x38: 3.60V</td></tr>
<tr><td>0x09: 1.25V</td><td>0x19: 2.05V</td><td>0x29: 2.85V</td><td>0x39: 3.65V</td></tr>
<tr><td>0x0A: 1.30V</td><td>0x1A: 2.10V</td><td>0x2A: 2.90V</td><td>0x3A: 3.70V</td></tr>
<tr><td>0x0B: 1.35V</td><td>0x1B: 2.15V</td><td>0x2B: 2.95V</td><td>0x3B: 3.75V</td></tr>
<tr><td>0x0C: 1.40V</td><td>0x1C: 2.20V</td><td>0x2C: 3.00V</td><td>0x3C: 3.80V</td></tr>
<tr><td>0x0D: 1.45V</td><td>0x1D: 2.25V</td><td>0x2D: 3.05V</td><td>0x3D: 3.85V</td></tr>
<tr><td>0x0E: 1.50V</td><td>0x1E: 2.30V</td><td>0x2E: 3.10V</td><td>0x3E: 3.90V</td></tr>
<tr><td>0x0F: 1.55V</td><td>0x1F: 2.35V</td><td>0x2F: 3.15V</td><td>0x3F: 3.95V</td></tr>
</table>
</td></tr>
</table>

LDO20CTRL2

Control OUT20 (LDO20) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x92**
73				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L20OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L20_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	00	R	Write “00” to these bits
1	ADSLDO20	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO21CTRL1

Control for OUT21 (LDO21) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0x28**
54	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	00	**00: OFF (when ENL21=LOW)** 01: ON in Low Power Mode (Regardless of ENL21) 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode 11: ON in normal mode (Regardless of ENL21)
5:0	L21_TV	10 1000	Output Voltage

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	**0x28: 2.80V**	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	0x2C: 3.00V	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO21CTRL2

Control OUT21 (LDO21) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x92**
74				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L21OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L21_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	00	R	Write “00” to these bits
1	ADSLDO21	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO22CTRL1

Control for OUT22 (LDO22) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0x28**
55	R/W			
BIT	**Name**	**POR**	**Description**	

<table>
<tr><td>7:6</td><td>OPMODE</td><td>00</td><td>00: OFF (when ENL22=Low)

01: Output ON in Low Power Mode
10: Output ON with Low Power Mode by PWRREQ
PWRREQ=H (1) : Output ON in Normal Mode
PWRREQ=L (0) : Output ON in Low Power Mode

11: ON in normal mode (regardless of ENL22 status)</td></tr>
<tr><td>5:0</td><td>L22_TV</td><td>10 1000</td><td>Output Voltage

<table>
<tr><td>0x00: 0.80V</td><td>0x10: 1.60V</td><td>0x20: 2.40V</td><td>0x30: 3.20V</td></tr>
<tr><td>0x01: 0.85V</td><td>0x11: 1.65V</td><td>0x21: 2.45V</td><td>0x31: 3.25V</td></tr>
<tr><td>0x02: 0.90V</td><td>0x12: 1.70V</td><td>0x22: 2.50V</td><td>0x32: 3.30V</td></tr>
<tr><td>0x03: 0.95V</td><td>0x13: 1.75V</td><td>0x23: 2.55V</td><td>0x33: 3.35V</td></tr>
<tr><td>0x04: 1.00V</td><td>0x14: 1.80V</td><td>0x24: 2.60V</td><td>0x34: 3.40V</td></tr>
<tr><td>0x05: 1.05V</td><td>0x15: 1.85V</td><td>0x25: 2.65V</td><td>0x35: 3.45V</td></tr>
<tr><td>0x06: 1.10V</td><td>0x16: 1.90V</td><td>0x26: 2.70V</td><td>0x36: 3.50V</td></tr>
<tr><td>0x07: 1.15V</td><td>0x17: 1.95V</td><td>0x27: 2.75V</td><td>0x37: 3.55V</td></tr>
<tr><td>0x08: 1.20V</td><td>0x18: 2.00V</td><td>0x28: 2.80V</td><td>0x38: 3.60V</td></tr>
<tr><td>0x09: 1.25V</td><td>0x19: 2.05V</td><td>0x29: 2.85V</td><td>0x39: 3.65V</td></tr>
<tr><td>0x0A: 1.30V</td><td>0x1A: 2.10V</td><td>0x2A: 2.90V</td><td>0x3A: 3.70V</td></tr>
<tr><td>0x0B: 1.35V</td><td>0x1B: 2.15V</td><td>0x2B: 2.95V</td><td>0x3B: 3.75V</td></tr>
<tr><td>0x0C: 1.40V</td><td>0x1C: 2.20V</td><td>0x2C: 3.00V</td><td>0x3C: 3.80V</td></tr>
<tr><td>0x0D: 1.45V</td><td>0x1D: 2.25V</td><td>0x2D: 3.05V</td><td>0x3D: 3.85V</td></tr>
<tr><td>0x0E: 1.50V</td><td>0x1E: 2.30V</td><td>0x2E: 3.10V</td><td>0x3E: 3.90V</td></tr>
<tr><td>0x0F: 1.55V</td><td>0x1F: 2.35V</td><td>0x2F: 3.15V</td><td>0x3F: 3.95V</td></tr>
</table>
</td></tr>
</table>

LDO22CTRL2

Control OUT22 (LDO22) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x92**
75				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L22OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L22_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	00	R	Write “00” to these bits
1	ADSLDO22	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO23CTRL1

Control for OUT23 (LDO23) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0x2C**
56	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	00	**00: OFF** 01: ON in Low Power Mode 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode 11: ON in normal mode
5:0	L23_TV	10 1100	Output Voltage

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	**0x2C: 3.00V**	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO23CTRL2

Control OUT23 (LDO23) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x92**
76				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L23OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L23_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	00	R	Write “00” to these bits
1	ADSLDO23	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO24CTRL1

Control for OUT24 (LDO24) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0x2C**
57	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	00	**00: OFF** 01: ON in Low Power Mode 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode 11: ON in normal mode
5:0	L24_TV	10 1100	Output Voltage

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	**0x2C: 3.00V**	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO24CTRL2

Control OUT24 (LDO24) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x92**
77				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L24OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L24_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	00	R	Write “00” to these bits
1	ADSLDO24	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO25CTRL1

Control for OUT25 (LDO25) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0x2C**
58	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	00	**00: OFF** 01: ON in Low Power Mode 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode 11: ON in normal mode
5:0	L25_TV	10 1100	Output Voltage

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	**0x2C: 3.00V**	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO25CTRL2

Control OUT25 (LDO25) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x92**
78				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L25OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L25_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	00	R	Write “00” to these bits
1	ADSLDO25	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

LDO26CTRL1

Control for OUT26 (LDO26) ON/OFF and Programmable Output

Address (hex)	**MODE**		Type: O	**RESET:0x2C**
59	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	OPMODE	00	**00: OFF** 01: ON in Low Power Mode 10: Output ON with Low Power Mode by PWRREQ PWRREQ=H (1) : Output ON in Normal Mode PWRREQ=L (0) : Output ON in Low Power Mode 11: ON in normal mode
5:0	L26_TV	10 1100	Output Voltage

0x00: 0.80V	0x10: 1.60V	0x20: 2.40V	0x30: 3.20V
0x01: 0.85V	0x11: 1.65V	0x21: 2.45V	0x31: 3.25V
0x02: 0.90V	0x12: 1.70V	0x22: 2.50V	0x32: 3.30V
0x03: 0.95V	0x13: 1.75V	0x23: 2.55V	0x33: 3.35V
0x04: 1.00V	0x14: 1.80V	0x24: 2.60V	0x34: 3.40V
0x05: 1.05V	0x15: 1.85V	0x25: 2.65V	0x35: 3.45V
0x06: 1.10V	0x16: 1.90V	0x26: 2.70V	0x36: 3.50V
0x07: 1.15V	0x17: 1.95V	0x27: 2.75V	0x37: 3.55V
0x08: 1.20V	0x18: 2.00V	0x28: 2.80V	0x38: 3.60V
0x09: 1.25V	0x19: 2.05V	0x29: 2.85V	0x39: 3.65V
0x0A: 1.30V	0x1A: 2.10V	0x2A: 2.90V	0x3A: 3.70V
0x0B: 1.35V	0x1B: 2.15V	0x2B: 2.95V	0x3B: 3.75V
0x0C: 1.40V	0x1C: 2.20V	**0x2C: 3.00V**	0x3C: 3.80V
0x0D: 1.45V	0x1D: 2.25V	0x2D: 3.05V	0x3D: 3.85V
0x0E: 1.50V	0x1E: 2.30V	0x2E: 3.10V	0x3E: 3.90V
0x0F: 1.55V	0x1F: 2.35V	0x2F: 3.15V	0x3F: 3.95V

LDO26CTRL2

Control OUT26 (LDO26) Active Discharge and Compensation

Address (hex)	Type: O			**RESET: 0x92**
79				
BIT	**Name**	**POR**	**MODE**	**Description**
7	L26OVCLMP_EN	1	R/W	Overvoltage Clamp Enable 0=Overvoltage Clamp disabled **1=Overvoltage Clamp enabled**
6	reserved	0	R	Write “0” to this bit
5:4	L26_COMP	01	R/W	Compensation scheme 00 = assume 50mΩ / 5nH trace impedance to remote capacitor – Load transient is 55mV typical (at the IC pin) **01 = assume 100mΩ / 10nH trace impedance to remote capacitor – Load transient is 66mV typical (at the IC pin)** 10 = assume 200mΩ / 20nH trace impedance to remote capacitor – load transient is 99mV typical (at the IC pin) 11 = assume 400mΩ / 40nH trace impedance to remote capacitor – load transient 120mV typical (at the IC pin)
3:2	reserved	00	R	Write “00” to these bits
1	ADSLDO25	1	R/W	0: Active discharge is OFF **1: Active discharge is ON**
0	reserved	0	R	Write “0” to this bit

BBAT Charger Register

Control backup charger

Address (hex)	**MODE**		Type: S	**RESET: 0x4F**
7E	R/W			
BIT	**Name**	**POR**	**Description**	

7:6	BBCRS	01	Output Resistor 00: Bypass 1kΩ **01: 1kΩ** 10: 3kΩ 11: 6kΩ
5	BBCLOWIEN	0	Low Charging Current enable **0: Enable** 1: Disable
4:3	BBCVS	01	Limit Voltage Setting 00: 2.5V **01: 3.0V** 10 :3.3V 11: 3.5V
2:1	BBCCS	11	Set the charging current If BBCLOWIEN =0 (Default) 00: 80uA 01: 80uA 10: 80uA **11: 100uA** If BBCLOWIEN =1 00: 200uA 01: 600uA 10: 800uA 11: 400uA
0	BBCHOSTEN	1	Enable the back-up charger 0: Backup battery charger OFF **1: Backup battery charger ON**

32KHZ

Control ON/OFF 32KHAP,32KHCP and P32KH Buffer and Low Jitter Mode

Address (hex)	**MODE**		Type: O	**RESET: 0x01**
7F	R/W			
BIT	**Name**	**POR**	**Description**	
7:4	Reserved	00	Write “00” to these bits	
3	LowJitterMode	0	**0: Disable Low Jitter Mode on these three outputs (Low Power Mode enabled)** 1: Enable Low Jitter Mode on these three outputs (Low Power Mode enabled)	
2	ENP32KH	0	1: P32KH Clock Output is activated **0: P32KH Clock Output turned off**	
1	EN32KHCP	0	1: 32KHZCP Clock Output is activated **0: 32KHZCP Clock Output turned off**	
0	EN32KHAP	1	**1: 32KHZAP Clock Output is activated** 0: 32KHZAP Clock Output turned off	

DO NOT WRITE ANY VALUES ON THE REGISTERS FROM 0x80 TO 0x97 SINCE THESE REGISTERS ARE RESERVED ARE OTHER PURPOSE.

RTC Control Registers

RTC Slave Address: 0x0C/0x0D

Block	Slave Address in binary	Slave Address (Write) in hex	Slave Address (Read) In hex
RTC	0000 110x	0C	0D

HEX REGISTER ADDRESS/DESCRIPTION SUMMARY for RTC section

Addr	Register name	RESET (hex)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
00	RTCINT	00	reserved	reserved	WTSR EVNT	RTC1S	SMPL EVENT	RTCA2	RTCA1	RTC60S
01	RTCINTM	FF	reserved	reserved	WTSR EVNTM	RTC1SM	SMPL EVENTM	RTCA2M	RTCA1M	RTC60SM
02	Control Mask (RTCCNTLM)	03	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HRMODEM	BCDM
03	Control (RTCCNTL)	00	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HRMODE	BCD
04	Update 0 (RTCUPDATE0)	0A	Reserved	Reserved	Reserved	RBUDR	RTCWAKE	FREEZE_SEC	FCUR	UDR
05	Update 1 (RTCUPDATE1)	00	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RBUDF	UDR
06	SMPL & WTSR	07	SMPL_EN	WTSR_EN	Reserved	Reserved	SMPLT		WTSRT	
07	Second (RTCSEC)	00	Reserved	SEC						
08	Minutes (RTCMIN)	00	Reserved	MIN						
09	Hour (RTCHOUR)	00	Reserved	AMPM	HOUR					
0A	Day of Week (RTCDOW)	01	Reserved	SAT	FRI	THU	WED	TUE	MON	SUN
0B	Month (RTCMONTH)	01	Reserved	Reserved	Reserved	MONTH				
0C	Year (RTCYEAR)	00	YEAR							
0D	Day of Month (RTCDOM)	01	Reserved	Reserved	DAY					
0E	Second on Alarm 1 (RTCSECA1)	00	AESECA1	SECA1						
0F	Minute on Alarm 1 (RTCMINA1)	00	AEMINA1	MINA1						
10	Hour on Alarm 1 (RTCHOURA1)	00	AEHOURA1	AMPM	HOURA1					
11	Day of Week on Alarm 1 (RTCDOWA1)	01	AEDOWA1	SAT	FRI	THU	WED	TUE	MON	SUN
12	Month on Alarm 1 (RTCMONTHA1)	00	AEMONTHA1	Reserved	Reserved	MONTHA1				
13	Year on Alarm 1 (RTCYEARA1)	00	AEYEARA1	YEARA1						
14	Day of Month on Alarm 1 (RTCDOMA1)	01	AEDOMA1	Reserved	DAYA1					
15	Second on Alarm 2 (RTCSECA2)	00	AESECA2	SECA2						
16	Minute on Alarm 2 (RTCMINA2)	00	AEMINA2	MINA2						
17	Hour on Alarm 2 (RTCHOURA2)	00	AEHOURA2	AMPM	HOURA2					
18	Day of Week on Alarm 2 (RTCDOWA2)	01	AEDOWA2	SAT	FRI	THU	WED	TUE	MON	SUN
19	Month on Alarm 2 (RTCMONTHA2)	00	AEMONTHA2	Reserved	Reserved	MONTHA2				
1A	Year on Alarm 2 (RTCYEARA2)	00	AEYEARA2	YEARA2						
1B	Day of Month on Alarm 2 (RTCDOMA2)	01	AEDOMA2	Reserved	DAYA2					

RTCINT – Interrupt Register

Address (hex)	**MODE**		Type: S	**RESET: 0x00**
00	R/C			
BIT	**NAME**	**POR**	**Description**	
7:6	Reserved	00	Write “00”	
5	WTSREVENT	0	**0: WTSR Event is not detected** 1: WTSR Event is detected	
4	RTC1S	0	RTC periodic 1 second Timer expired interrupt **0 : 1s Timer is not expired** 1 : 1s Timer expired	
3	SMPLEVENT	0	**0 : SMPL Event is not detected** 1: SMPL Event is detected	

2	RTCA2	0	**0: RTC ALARM2 rising edge is not detected** 1: RTC ALARM2 rising edge is detected
1	RTCA1	0	**0: RTC ALARM1 rising edge is not detected** 1: RTC ALARM1 rising edge is detected
0	RTC60S	0	**0: RTC periodic 60s event is not detected** 1: RTC periodic 60s event is detected

RTCINTM- Interrupt Mask Register

Address (hex)	**MODE**		Type: S	**RESET: 0x3F**
01	R/W			
BIT	**NAME**	**POR**	**Description**	
7:6	Reserved	00	Write “00” to these bits	
5	WTSREVNTM	1	0: Interrupt enabled **1: Mask WTSREVNT interrupt**	
4	RTC1SM	1	0: Interrupt enabled **1: Mask RTC1S event interrupt**	
3	SMPLEVNTM	1	0: Interrupt enabled **1: Mask SMPLEVNT interrupt**	
2	RTCA2M	1	0: Interrupt enabled **1: Mask RTC ALARM2 interrupt**	
1	RTCA1M	1	0: Interrupt enabled **1: Mask RTC ALARM1 interrupt**	
0	RTC60SM	1	0: Interrupt enabled **1: Mask RTC60S event interrupt**	

RTCCNTLM Register

RTC Control Register Mask			Address: 0x02	Type: S	Reset: 0x03
BIT	Mode	Name	Reset	Description	
7-2	R/W	reserved	000000	Reserved	
1	R/W	HRMODEM	1	Access control of HRMODE Bit in register RTC control register 0: Writes to bit 1 of register address 0x03 (RTCCNTL) not allowed **1: Writes to bit 1 of register address 0x03 (RTCCNTL) allowed**	
0	R/W	BCDM	1	Access control of BCD Bit in register RTCCNTL Register 0: Writes to bit 0 (BCD) of register address 0x03	

				(RTCCNTL) not allowed **1: Writes to bit 0 (BCD) of register address 0x03 (RTCCNTL) allowed**

RTCCNTL Register

Control Register			Address: 0x03	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description	
7:2	R/W	reserved	000000	Reserved	
1	R/W	HRMODE	0	Hour Format Control **0: 12 hour mode** 1: 24 hour mode Note that AMPM bit defined for the HOUR or HOURA register only make sense for the 12-hr mode as the 24-hr mode already has AM/PM implied. If HRMODEM=0, writes to HRMODE are not allowed. When switching between 12-hour and 24-hour mode, the registers do not automatically update. User must reprogram all registers.	
0	R/W	BCD	0	Data Mode for Time and Calendar Updates **0: Binary** 1: BCD (Binary-Coded-Decimal) If BCDM=0, writes to BCD are not allowed.	

RTCUPDATE0 Register

Update Register 0			Address: 0x04	Type: S	Reset: 0x0A
BIT	Mode	Name	Reset	Description	
7: 5	R/W	Reserved	000	Reserved	
4	W	RBUDR	0	Access Control to update RTC registers by transferring data from the actual registers to the “Read Buffers” **0: No action** 1: Update “Read Buffers” Maximum transfer time from timekeeper counters to read is 16msec after RBUDR is set. RBUDR is internally cleared to after the registers data has been transferred. User should not read this bit to verify operation is completed. User should RBUDF flag	

				in RTCUPDATE1 register instead.
3	R/W	RTCWAKE	1	PMIC Wake-Up Upon RTC Alarm Control 0: PMIC does not wake up if RTC1A or RTC2A set **1: PMIC wakes up if RTC1A or RTC2A is set**
2	R/W	FREEZE_SEC	0	This bit freezes the SEC counter from incrementing **0: SEC counter increments normally** 1: SEC counter stops incrementing which stops all subsequent registers in the timer string (MIN, HOUR, DAY, etc). This setting effectively stops the clock.
1	R/W	FCUR	1	Flags Cleared Upon Read Control Bit 0: User must write 0 to clear interrupt **1: Flags interrupt cleared upon read**
0	W	UDR	0	Access Control to Update RTC registers by transferring data from the "Write Buffers" to the actual registers **0: No action** 1: Update register. Maximum transfer time from write buffers to the timekeeper counters is 16msec after UDR is set. UDR is internally cleared to after the registers data has been transferred. User should not read this bit to verify operation is completed. User should UDF flag in RTCUPDATE1 register instead.

RTCUPDATE1 Register

Update Register 1		Address: 0x05	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description
7:2	Read Only/ Clear on Read	Reserved	000000	Reserved
1		RBUDF	0	This bit is an Update Flag that indicates when an actual transfer of data from the actual registers to "Read Buffers" occurs. When this bit is 1, then the user can initiate a new read operation, otherwise it is not safe to do so **0 = Update Not Done** 1 = Update Done Maximum update time is 16msec after the UDR bit is set. If FCUR bit (RTCUPDATE0 register) is 1, this bit is automatically cleared after a read operation. If FCUR is 0, the user must write a 0 to clear it.
0		UDF	0	This bit is an Update Flag that indicates when an actual transfer of data from the "write Buffers" to the corresponding register occurs. When this bit is 1, then the user can initiate a new write operation, otherwise it is not safe to do so **0 = Update Not Done** 1 = Update Done Maximum update time is 16msec after the RBUDR bit is set. If FCUR bit (RTCUPDATE0 register) is 1, this bit is automatically cleared after a read operation. If FCUR is 0, the user must write a 0 to clear it.

WTSR and SMPL Register

WTSR and SMPL Register	Address: 0x06	Type: S	Reset: 0x07

BIT	Mode	Name	Reset	Description
7	R/W	SMPL_EN	0	SMPL Function Enable Control **0: SMPL disabled** 1: SMPL enabled
6	R/W	WTSR_EN	0	WTSR Function Enable Control **0: WTSR disabled** 1: WTSR enabled
5:4	R/W	Reserved	00	Write “00”
3:2	R/W	SMPLT	01	Set the SMPL timer Threshold 00: 0.5s **01: 1.0s** 10: 1.5s 11: 2.0s
1:0	R/W	WTSRT	11	Set the WTSR timer Threshold 00: 250ms 01: 500ms 10: 750ms **11: 1000ms**

RTCSEC Register

Second Register			Address: 0x07	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description	
7	R/W	Reserved	0	Reserved	
6:0	R/W	SEC	0000000	RTC Seconds Counter Register In Binary format (BCD=0), valid values for B6 through B0 are 0 through 59. In BCD format (BCD=1), valid data for B6 through B4 are 0 through 5, and valid data for B3 through B0 are 0 through 9.	

RTCMIN Register

Minutes Register			Address: 0x08	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description	
7	R/W	Reserved	0	Reserved	
6:0	R/W	MIN	0000000	RTC Minutes Counter Register In Binary format (BCD=0), valid values for B6 through B0 are 0 through 59. In BCD format (BCD=1), valid data for B6 through B4 are 0 through 5, and valid data for B3 through B0 are 0 through 9	

RTCHOUR Register

Hour Register			Address: 0x09	Type: S	Reset: 0x01
BIT	Mode	Name	Reset	Description	
7	R/W	Reserved	0	Reserved	
6	R/W	AMPM	0	AM/PM Selection, AMPM is only valid when the clock is set for 12-hour mode (HRMODE=0). When the clock is set for 24-hour mode (HRMODE=1), this bit is a “don’t care”. **0: AM** 1: PM	
5:0	R/W	HOUR	000001	RTC Hours Counter Register Note that there would be two possibilities for values chosen for B5 through B0 depending on current status of HRMODE Bit: If HRMODE =1 (24 hours mode): a. Binary Mode (BCD=0): B5 is zero, and B4 through B0 valid values are 0 through 23. b. BCD Mode (BCD=1): Valid values for B5 through B4 are 0 through 2, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 23) **If HRMODE =0 (12 hours mode)** **a. Binary Mode (BCD=0): B5 and B4 are 0, and valid values for B3 through B0 are 1 through 12** b. BCD Mode (BCD=1): Valid values for B5 through B4 are 0 through 1, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 12)	

RTCDOW Register

DAY OF WEEK Register			Address: 0x0A	Type: S	Reset: 0x01
BIT	Mode	Name	Reset	Description	
7	R/W	Reserved	0	Reserved	
6	R/W	SAT	0	B[6:0] = 100_0000 represents Saturday	
5	R/W	FRI	0	B[6:0] = 010_0000 represents Friday	
4	R/W	THU	0	B[6:0] = 001_0000 represents Thursday	
3	R/W	WED	0	B[6:0] = 000_1000 represents Wednesday	
2	R/W	TUE	0	B[6:0] = 000_0100 represents Tuesday	
1	R/W	MON	0	B[6:0] = 000_0010 represents Monday	
0	R/W	SUN	1	B[6:0] = 000_0001 represents Sunday	

Note: Such a format selection, instead of using 3 bits, becomes obvious when dealing with alarms, as multiple days could be set. It is imperative to realize that there is no BCD representation for B6 through B0, and thus no conversion from BCD to Binary will be performed by the logic.

RTCMONTH Register

MONTH Register			Address: 0x0B	Type: S	Reset: 0x01
BIT	Mode	Name	Reset	Description	
7:5	R/W	Reserved	000	Write “000” to these bits	
4:0	R/W	MONTH	00001	RTC Month Counter Register In Binary format (BCD=0), valid values for B4 through B0 are 1 through 12. In BCD format (BCD=1), valid data for B4 is either 0 or 1, and valid data for B3 through B0 are 0 through 9 (the full value in BCD format should not exceed 12 and must be greater than zero). Month of January is represented by 1, while December is shown as 12.	

RTCYEAR Register

YEAR Register			Address: 0x0C	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description	
7:0	R/W	YEAR	00000000	RTC Year Counter Register In Binary format (BCD=0), valid values for B7 through B0 are 0 through 99. In BCD format (BCD=1), valid data for B7 through B4 are 0 through 9, and similarly valid data for B3 through B0 are 0 through 9.	

RTCDOM Register

DAY of MONTH Register			Address: 0x0D	Type: S	Reset: 0x01
BIT	Mode	Name	Reset	Description	
7:6	R/W	Reserved	00	Write “00” to these bits	
5:0	R/W	DAY	000001	RTC Days in a month Register In Binary format (BCD=0), valid values for B5 through B0 are 1 through 31. In BCD format (BCD=1), valid data for B4 through B5 are 0 through 3, and valid data for B3 through B0 are 0 through 9 (the full value should not exceed 31). Furthermore, there is a restriction on chosen number of days in a month according to the selected month and year as shown below: 1. For months 1, 3, 5, 7, 8, 10, and 12 the selected value for B5 through B0 must be 1	

				through 31. 2. For months 4, 6, 9, and 11 the selected value for B5 through B0 must be 1 through 30. 3. For month 2, or month of Feb., the selected value for B5 through B0 must be 1 through 28 for normal years, or must be 1 through 29 for leap years. Leap years are those that are evenly divisible by 4. 0, 4, 8, …, 24, 28,..,92,96. Note that 2100 tear is not a leap year, but this calendar considers Feb 29, 2100 a valid day.

RTCSECA1 Register

SEC RTCA1			Address: 0x0E	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description	
7	R/W	AESECA1	0	Alarm Enable Control **0: Alarm disable** 1: Alarm enable	
6:0	R/W	SECA1	0000000	RTC Seconds Alarm Register If the value of SECA1 is equal to the value of SEC and AESECA1=1, RTCA1 alarm interrupt is generated.	

RTCMINA1 Register

MIN RTCA1			Address: 0x0F	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description	
7	R/W	AEMINA1	0	Alram Enable Control **0: Alarm disable** 1: Alarm enable	
6:0	R/W	MINA1	0000000	RTC Minute Alarm Register If the value of MINA1 is equal to the value of MIN and AEMINA1=1, RTCA1 alarm interrupt is generated.	

RTCHOURA1 Register

HOUR RTCA1			Address: 0x10	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description	

7	R/W	AEHOURA1	0	Alram Enable Control **0: Alarm disable** 1: Alarm enable
6	R/W	AMPM	0	AM/PM selection, Only valid during 12-Hr Mode **0: AM** 1: PM
5:0	R/W	HOURA1	000000	RTC Hour Alarm Register If the value of HOURA1 is equal to the value of HOUR and AEHOURA1=1, RTCA1 alarm interrupt is generated. If HRMODE = 1 (24 hours mode): a. Binary Mode: B5 is zero, and B4 through B0 valid values are 0 through 23. b. BCD Mode: Valid values for B5 through B4 are 0 through 2, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 23) If HRMODE = 0 (12 hours mode) a. Binary Mode: B5 and B4 are 0, and valid values for B3 through B0 are 1 through 12 b. BCD Mode: Valid values for B5 through B4 are 0 through 1, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 12)

RTCDOWA1 Register

DAY OF WEEK RTCA1			Address: 0x11	Type: S	Reset: 0x01
BIT	Mode	Name	Reset	Description	
7	R/W	AEDOWA1	0	Alarm Enable Control **0: Alarm disable** 1: Alarm enable	
6	R/W	SAT	0	RTC Day Of Week Alarm Register If the value of RTCDOWA1 is equal to the value of DOW and AEDOWA1 is 1, an RTCA1 alarm interrupt is generated Bits B6 through B0 each represents one day of the week. This would dictate that only one bits at a time is allowed to be set as shown below: B[6:0] = 000_0001 represents Sunday B[6:0] = 000_0010 represents Monday B[6:0] = 000_0100 represents Tuesday B[6:0] = 000_1000 represents Wednesday B[6:0] = 001_0000 represents Thursday B[6:0] = 010_0000 represents Friday B[6:0] = 100_0000 represents Saturday	
5	R/W	FRI	0		
4	R/W	THU	0		
3	R/W	WED	0		
2	R/W	TUE	0		
1	R/W	MON	0		
0	R/W	SUN	1		

Note: This configuration allows for either selecting multiple days (such as generation of an alarm on Tue., and Thu. of each week by setting both B2 and B4 to one), or selecting a single day of the week (such as generation of the alarm weekly on each Sunday by setting B0 to one) for a weekly alarm generation.

RTCMONTHA1 Register

MONTH RTCA1			Address: 0x12	Type: S	Reset: 0x01
BIT	Mode	Name	Reset	Description	
7	R/W	AEMONTHA1	0	Alarm Enable Control **0: Alarm disable** 1: Alarm enable	
6: 5	R/W	Reserved	0	Write “00” to these bits	
4:0	R/W	MONTHA1	00001	RTC Month Alarm Register If the value of MONTHA1 is equal to the value of MONTH and AEMONTHA1 is 1, an RTCA1 alarm interrupt is generated	

RTCYEARA1 Register

YEAR RTCA1			Address: 0x13	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description	
7	R/W	AEYEARA1	0	Alarm Enable Control **0: Alarm disable** 1: Alarm enable	
6:0	R/W	YEARA1	0000000	RTC Year Alarm Register If the value of YEARA1 is equal to the value of YEAR and AEYEARA1 is 1, an RTCA1 alarm interrupt is generated Note that In binary format (BCD=0), valid data for YEARA1 [6:0] are 0 to 99. In BCD format (BCD=1), valid data for YEARA1 [6:0] are 0 to 79.	

RTCDOMA1 Register

DAY of MONTH RTCA1			Address: 0x14	Type: S	Reset: 0x01
BIT	Mode	Name	Reset	Description	
7	R/W	AEDOMA1	0	Alarm Enable Control **0: Alarm disable** 1: Alarm enable	
6	R/W	Reserved	0	Write “0” to this bit	
5:0	R/W	DAYA1	000001	RTC Day Of Month Alarm Register If the value of DAYA1 is equal to the value of DAY and AEDOMA1 is 1, an RTCA1 alarm interrupt is generated	

Note: It is the responsibility of the user to make sure that days selected for the month actually matches the intended number of days in the month. For example, it is rather obvious that if the user selects day 31 in this register, month of Feb would be excluded as well as months of Apr, June, Sep, and Nov.

RTCSECA2 Register

SEC RTCA2			Address: 0x15	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description	
7	R/W	AESECA2	0	Alram Enable Control **0: Alarm disable** 1: Alarm enable	
6:0	R/W	SECA2	0000000	RTC Second Alarm Register If the value of SECA2 is equal to the value of SEC and AESECA2=1, RTCA2 alarm interrupt is generated.	

RTCMINA2 Register

MIN RTCA2			Address: 0x16	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description	
7	R/W	AEMINA2	0	Alram Enable Control **0: Alarm disable** 1: Alarm enable	
6:0	R/W	MINA2	0000000	RTC Minute Alarm Register If the value of MINA2 is equal to the value of MIN and AEMINA2=1, RTCA2 alarm interrupt is generated.	

RTCHOURA2 Register

HOUR RTCA2			Address: 0x17	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description	
7	R/W	AEHOURA2	0	Alarm Enable Control **0: Alarm disable** 1: Alarm enable	
6	R/W	AMPM	0	AM/PM Selection, Only Valid during 12-Hr Mode **0: AM** 1: PM	
5:0	R/W	HOURA2	000000	RTC Hour Alarm Register If the value of HOURA2 is equal to the value of HOUR and AEHOURA2=1, RTCA2 alarm interrupt is generated. If HRMODE = 1 (24 hours mode): c. Binary Mode: B5 is zero, and B4 through B0 valid values are 0 through 23. d. BCD Mode: Valid values for B5 through B4	

				are 0 through 2, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 23) If HRMODE = 0 (12 hours mode) c. Binary Mode: B5 and B4 are 0, and valid values for B3 through B0 are 1 through 12 d. BCD Mode: Valid values for B5 through B4 are 0 through 1, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 12)

RTCDOWA2 Register

DAY OF WEEK RTCA2			Address: 0x18	Type: S	Reset: 0x01
BIT	Mode	Name	Reset	Description	
7	R/W	AEDOWA2	0	Alarm Enable Control **0: Alarm disable** 1: Alarm enable	
6	R/W	SAT	0		
5	R/W	FRI	0	RTC Day Of Week Alarm Register If the value of RTCDOWA2 is equal to the value of DOW and AEDOWA2 is 1, an RTCA2 alarm interrupt is generated Bits B6 through B0 each represents one day of the week. This would dictate that only one bits at a time is allowed to be set as shown below: B[6:0] = 000_0001 represents Sunday B[6:0] = 000_0010 represents Monday B[6:0] = 000_0100 represents Tuesday B[6:0] = 000_1000 represents Wednesday B[6:0] = 001_0000 represents Thursday B[6:0] = 010_0000 represents Friday B[6:0] = 100_0000 represents Saturday	
4	R/W	THU	0		
3	R/W	WED	0		
2	R/W	TUE	0		
1	R/W	MON	0		
0	R/W	SUN	1		

Note: This configuration allows for either selecting multiple days (such as generation of an alarm on Tue., and Thu. of each week by setting both B2 and B4 to one), or selecting a single day of the week (such as generation of the alarm weekly on each Sunday by setting B0 to one) for a weekly alarm generation.

RTCMONTHA2 Register

MONTH RTCA2			Address: 0x19	Type: S	Reset: 0x01
BIT	Mode	Name	Reset	Description	
7	R/W	AEMONTHA2	0	Alarm Enable Control **0: Alarm disable** 1: Alarm enable	
6: 5	R/W	Reserved	0	Write “00” to these bits	
4:0	R/W	MONTHA2	00001	RTC Month Alarm Register If the value of MONTHA2 is equal to the value of MONTH and AEMONTHA2 is 1, an RTCA2 alarm interrupt is generated	

RTCYEARA2 Register

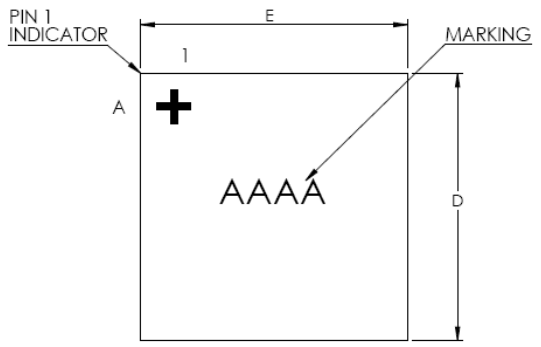
YEAR RTCA2			Address: 0x1A	Type: S	Reset: 0x00
BIT	Mode	Name	Reset	Description	
7	R/W	AEYEARA2	0	Alarm Enable Control **0: Alarm disable** 1: Alarm enable	
6:0	R/W	YEARA2	0000000	RTC Year Alarm Register If the value of YEARA2 is equal to the value of YEAR and AEYEARA2 is 1, an RTCA2 alarm interrupt is generated. Note that In binary format (BCD=0), valid data for YEARA2 [6:0] are 0 to 99. In BCD format (BCD=1), valid data for YEARA2 [6:0] are 0 to 79.	

RTCDOMA2 Register

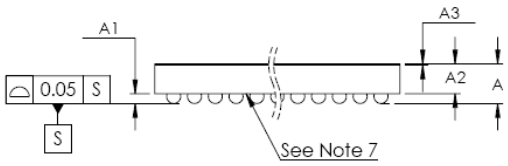
DAY of MONTH RTCA2			Address: 0x1B	Type: S	Reset: 0x01
BIT	Mode	Name	Reset	Description	
7	R/W	AEDOMA2	0	Alarm Enable Control **0: Alarm disable** 1: Alarm enable	
6	R/W	Reserved	0	Write “0” to this bit	
5:0	R/W	DAYA2	000001	RTC Day Of Month Alarm Register If the value of DAYA2 is equal to the value of DAY and AEDOMA2 is 1, an RTCA2 alarm interrupt is generated	

Note: It is the responsibility of the user to make sure that days selected for the month actually matches the intended number of days in the month. For example, it is rather obvious that if the user selects day 31 in this register, month of Feb would be excluded as well as months of Apr, June, Sep, and Nov.

Package Outline.

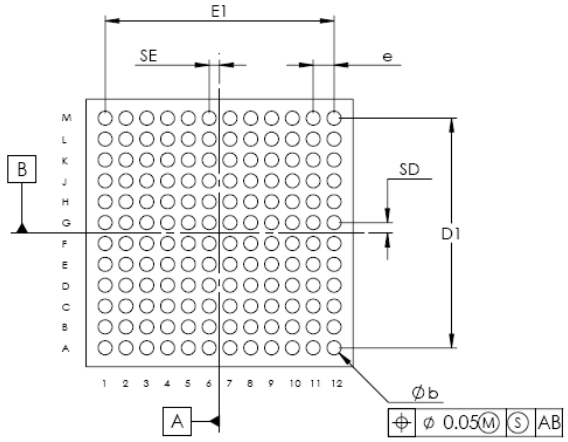


TOP VIEW



SIDE VIEW

COMMON DIMENSIONS		
A	0.76	±0.05
A1	0.19	±0.03
A2	0.57	REF
A3	0.025	BASIC
b	Ø0.27	±0.03
D1	4.40	
E1	4.40	
e	0.40	BASIC
SD	0.20	BASIC
SE	0.20	BASIC



BOTTOM VIEW

PKG. CODE	E MIN	E MAX	D MIN	D MAX	DEPOPULATED BUMPS
W1445A5+2	5.13	5.16	5.13	5.16	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

- DRAWING NOT TO SCALE -

MAXIM

TITLE: PACKAGE OUTLINE
144 BUMPS WLP PKG. 0.4mm PITCH

APPROVAL | DOCUMENT CONTROL NO. 21-0584 | REV. A | 1/1