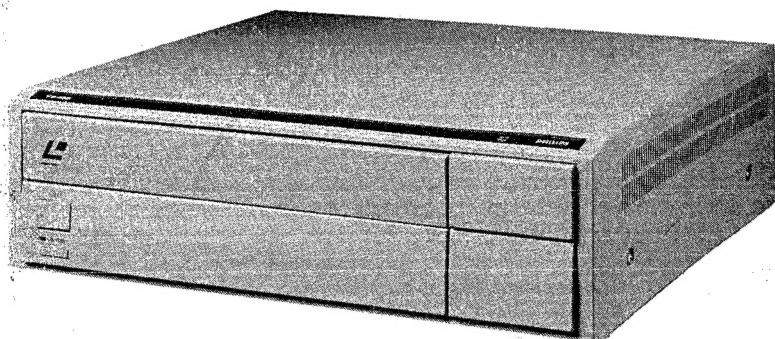


Service
Service
Service



00/05/23/30

42 047 A12

Service Manual

The VP406 is a Standard LaserVision disc drive for use in computerized audiovisual systems, involving a high degree of interactivity. The Drive is suitable for playback of pre-recorded optical video discs, according to the LaserVision system (PAL standard).

The differences between /00 and /05 are only related to the mainscords.

Version /00 = LV disc drive with Euro mainscord.

/05 = /00 with GB mainscord

/23 = /00 without cabinet for special purposes

/30 = /00 with extra screening for reducing radiation

Contents:

Chapter 1 Technical data
Controls, indicators, connections
Connector pinning

Chapter 2 Remarks
Warnings
Modification levels
Adjustments
Demounting instructions
Service hints
Service tools
List of used symbols
Connections of semiconductors

Chapter 3 Module- and connector lay-out
Signal listing
Wiring diagram
Blockdiagram Control routes
Blockdiagram AUDIO/VIDEO signal path
Blockdiagram Servo

Chapter 4 Survey of modules and panels
– Circuit diagram
– PCB lay-out
Remote control

Chapter 5 Exploded view drawings
List of mechanical parts
List of electrical parts

Chapter 6 Repair method

Chapter 7 Circuit description

Chapter 8 Service Information

Caution

"Use of controls or adjustments or performance of procedures other than those specified here in may result in hazardous radiation exposure".

Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.

Documentation Technique Service Dokumentation Documentazione di Servizio Huolte-Ohje Manual de Servicio Manual de Servicio



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Chapter 1

Technical data
Controls, indicators, connections
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Chapter 2

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Demounting instructions
Service hints
Service tools
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Connections of semiconductors

Chapter 3

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– Circuit diagram
– PCB lay-out
Remote control

Chapter 5

Exploded view drawings
List of mechanical parts
List of electrical parts

Chapter 6

Repair method

Chapter 7

Circuit description

Chapter 8

Service Information

**Technical data
Controls, indicators, connections
Connector pinning**

TECHNICAL DATA VP406

LASERVISION DISC

Disc diameter	30 cm (12") or 20 cm (8")
Disc thickness	2.7 mm (0.1")
Disc speed	CAV disc: 1500 r.p.m. CLV disc: 1500-570 r.p.m.
Maximum capacity (30 cm - 12" disc)	CAV disc: 54000 pictures per side
Max. playingtime	CAV disc: 36 minutes per side CLV disc: 1 hour per side
Average track pitch	1.6-1.8 μ m

Audio

Audio output (cinch)	650 mV r.m.s. into 1 k (max. deviation)
Audio output (Euroconnector pins 1 & 3)	650 mV r.m.s. into 1 k 40-20 000 Hz
Audio bandwidth	≥ 50 dB typ. weighted
Signal-to noise ratio	(disc dependent)
Channel separation	better than 55 dB

LASERVISION DISC DRIVE

General

Front loading motor-powered disc-tray
startup time <13 s
unload time (time
between Eject
command
and disc out of player) <15 s

SSL (solid state laser)

Laser type	AlGaAs semiconductor
Wavelength	780 nm
Aperture	0.5
Output of laser	3 - 5 mW

Random access time CAV: max. 3s (≤ 1 s average)
CLV: max. 15s (≤ 5 s average)

Instant jump up to 50 frames (forward or
reverse) within vertical interval time

On-board programming Up to 16 picture number/chapter
number segments

Mains voltage	220-240 V ($\pm 10\%$) a.c.
Mains frequency	50 to 60 Hz
Power consumption	46 W approx.
Electrical safety	acc. to IEC 65
operational conditions	10 to 35 °C
Rel. humidity	20-80%
storage conditions	-40 to 70 °C
Rel. humidity	10-95%

Dimensions disc-tray open	420x125x400mm
Weight	14 kg (approx.)

TV system 625/50 PAL

Video

CVBS output (BNC) 1 V into 75 Ω

CVBS output

(Euroconnector pin 19) 1 V into 75 Ω

RGB output

(Euroconnector)

R (pin 15) 0.7 V into 75 Ω

G (pin 11) 0.7 V into 75 Ω

B (pin 7) 0.7 V into 75 Ω

Video bandwidth RGB: 5 MHz (-3dB)
CVBS: 3 MHz (-3 dB), encoded

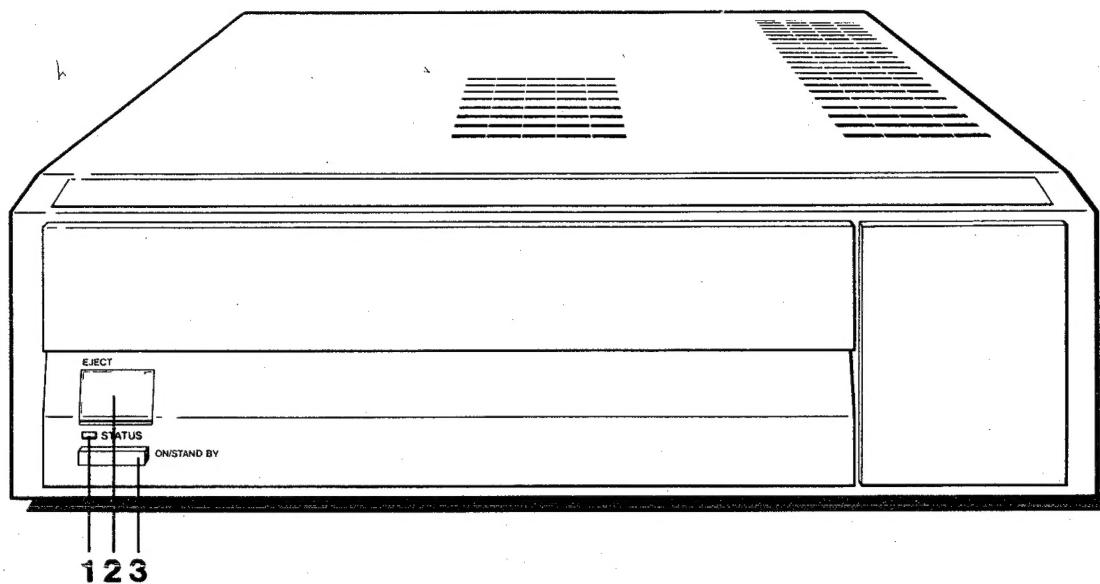
Signal-to-noise ratio 40 dB typ. unweighted
(disc dependent)

50 dB typ. weighted

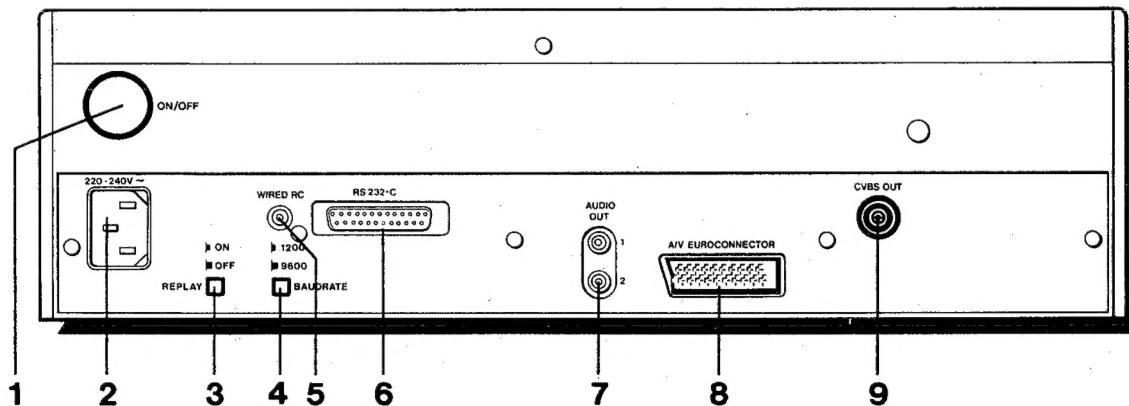
(disc dependent)

Timebase instability less than 10ns (normal play)

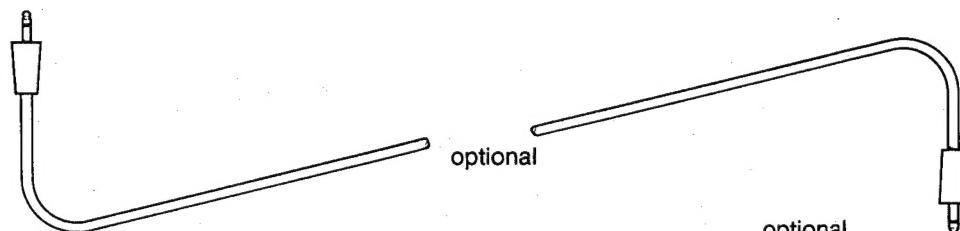
CONTROLS, INDICATORS AND CONNECTIONS



1 2 3



1 2 3 4 5 6 7 8 9



VP406 (front)

1 STATUS indicator

2 EJECT button

3 ON/STANDBY button

VP406 (rear)

1 ON/OFF push button

2 MAINS lead socket

3 REPLAY on/off push button

4 BAUD RATE push button

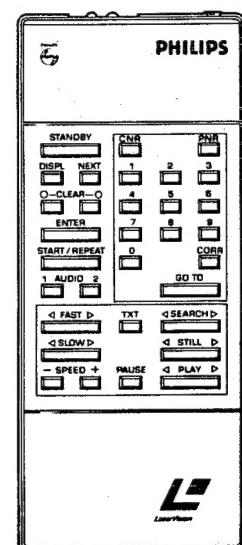
5 WIRED RC socket

6 RS232-C socket

7 AUDIO OUT (1 & 2) sockets

8 A/V EUROCONNECTOR

9 CVBS OUT socket



CONNECTOR PINNING

<p>A/V Euroconnector</p> <table border="0"> <thead> <tr> <th>Pin</th> <th>signal</th> </tr> </thead> <tbody> <tr><td>1</td><td>audio out (right) 650 mV rms/1k</td></tr> <tr><td>2</td><td>not connected</td></tr> <tr><td>3</td><td>audio out (left) 650 mV rms/1k</td></tr> <tr><td>4</td><td>audio earth</td></tr> <tr><td>5</td><td>blue earth</td></tr> <tr><td>6</td><td>not connected</td></tr> <tr><td>7</td><td>blue out 700 mV/75 Ω</td></tr> <tr><td>8</td><td>player status (player in standby: 2 V, player on : 12 V)</td></tr> <tr><td>9</td><td>green earth</td></tr> <tr><td>10</td><td>not connected</td></tr> <tr><td>11</td><td>green out 700 mV/75 Ω</td></tr> <tr><td>12</td><td>not connected</td></tr> <tr><td>13</td><td>red earth</td></tr> <tr><td>14</td><td>earth</td></tr> <tr><td>15</td><td>red out 700 mV/75 Ω</td></tr> <tr><td>16</td><td>fast blanking: 2.5 V into 75 Ω (RGB status)</td></tr> <tr><td>17</td><td>CVBS earth</td></tr> <tr><td>18</td><td>RGB status earth</td></tr> <tr><td>19</td><td>CVBS out 1 V/75 Ω (also acts as sync out when using RGB)</td></tr> <tr><td>20</td><td>not connected</td></tr> <tr><td>21</td><td>socket earth</td></tr> </tbody> </table>	Pin	signal	1	audio out (right) 650 mV rms/1k	2	not connected	3	audio out (left) 650 mV rms/1k	4	audio earth	5	blue earth	6	not connected	7	blue out 700 mV/75 Ω	8	player status (player in standby: 2 V, player on : 12 V)	9	green earth	10	not connected	11	green out 700 mV/75 Ω	12	not connected	13	red earth	14	earth	15	red out 700 mV/75 Ω	16	fast blanking: 2.5 V into 75 Ω (RGB status)	17	CVBS earth	18	RGB status earth	19	CVBS out 1 V/75 Ω (also acts as sync out when using RGB)	20	not connected	21	socket earth	<p>RS232-C interface</p> <p>Serial computer interface, in accordance with international communication standards.</p> <p>Full duplex</p> <p>8 data bits, 1 stop bit, no parity</p> <p>Data transmission speed may be set to 1200/9600 baud according to the position of the baud rate switch at the rear of the drive.</p> <table border="0"> <thead> <tr> <th>Baud rate</th> <th>switch</th> </tr> </thead> <tbody> <tr><td>1200</td><td>PRESSED</td></tr> <tr><td>9600</td><td>NOT PRESSED</td></tr> </tbody> </table> <p>The drive is fitted with a 25-pole female D-connector with the following pin connections:</p> <table border="0"> <thead> <tr> <th>pin</th> <th>signal</th> </tr> </thead> <tbody> <tr><td>2 (TxD)</td><td>transmitted data from the drive to computer</td></tr> <tr><td>3 (RxD)</td><td>received data from computer to drive</td></tr> <tr><td>5 (CTS)</td><td>clear to send: a signal from computer to drive indicating the computer is ready to receive data ($\geq +3$ V means O.K. to transmit)</td></tr> <tr><td>7 (GND)</td><td>logic ground</td></tr> <tr><td>9</td><td>* +12 V/100 mA</td></tr> <tr><td>10</td><td>* -12 V/10 mA</td></tr> <tr><td>20 (DTR)</td><td>data terminal ready: a signal from the drive to computer indicating that the drive is ready to receive data ($\geq +3$ V means O.K. for data)</td></tr> </tbody> </table> <p>* Optional</p>	Baud rate	switch	1200	PRESSED	9600	NOT PRESSED	pin	signal	2 (TxD)	transmitted data from the drive to computer	3 (RxD)	received data from computer to drive	5 (CTS)	clear to send: a signal from computer to drive indicating the computer is ready to receive data ($\geq +3$ V means O.K. to transmit)	7 (GND)	logic ground	9	* +12 V/100 mA	10	* -12 V/10 mA	20 (DTR)	data terminal ready: a signal from the drive to computer indicating that the drive is ready to receive data ($\geq +3$ V means O.K. for data)
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Chapter 2

**Remarks
Warnings
Modification levels
Adjustments
Demounting instructions
Service hints
Service tools
List of used symbols
Connections of semiconductors**

REMARKS

1. Care of the disc drive

The disc drive requires no special maintenance. It is, however, recommended to clean the objective lens from time to time with a piece of wadding, dipped in alcohol.

2. Set-up of the Service Manual

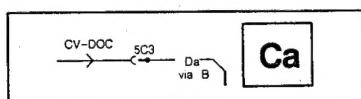
The set is composed of various panels or modules. The circuit diagrams, PCB layouts and parts lists have also been classified per panel or module.

a) Circuit diagrams

Of each module a functional circuit diagram has been given, with the incoming signals drawn as much as possible at the left-hand side and the outgoing signals at the right-hand side. Each incoming and outgoing signal has a unique name, the meaning of which can be read in the Signal listing.
If a signal enters or leaves the module, this takes place via a connector (e.g. 6B2 = pin 6 of connector B2) and via a letter indication in the line. This indication mentions to which module the line is connected.
If the letter indication in the line is the same as the module on which the signal is present, the signal remains on the module mentioned and, naturally, no connector is drawn.

If a signal is going from one diagram to another via the Radial + TBC panel B, the letter indication in the line is extended with the indication "via B".

Example:



Means:

The signal CV-DOC is going from diagram Ca to diagram Da via interconnection on panel B.
A survey of interconnections and signals on panel B is given in the "List of loop-through signals on panel B" in chapter 4.

b) Oscilloscopes and voltages in the circuit diagrams

- The oscilloscopes in the diagrams have been measured with a dual-beam scope with Delayed Timebase PM3214. The set has been connected to a monitor by means of a SCART cable
Video : still picture, picture number 5530
(EBU colour bar, 75% saturation)
- Audio 1: normal play, picture numbers 6200 – 6500,
1 kHz modulation
- Audio 2: normal play, picture numbers 6500 – 6900,
1 kHz modulation
- The DC voltages have been measured with a Digital Multimeter PM2524, still picture, picture number 5530, unless stated otherwise.

c) PCB layouts

Most modules in the set have been equipped with double-sided copper pattern and plated-through holes. For each module a PCB layout is drawn, consisting of a drawing of the component side and of the soldering side (chip side) with corresponding copper pattern.

d) Parts lists

For each module an electrical parts list is given in Chapter 5, stating the service code numbers of the specific electrical components that have been applied on the module.

The code numbers of the standard components (ICs, transistors, diodes, standard resistors, etc.) have been placed on a collective list in Chapter 5.

e) Service code numbers of the modules

In this Service Manual service code numbers for the panels and the modules have not been mentioned. Please consult your parts supplier.

3. Repair on modules

To enable repair/adjustment on modules use can be made of extension PCBs or extension cables. A survey can be found sub Service Tools in this chapter.

4. The optical deck

The optical deck in the disc drive is composed of various critical components and at the production department adjusted by complicated alignment equipment.

For the time being repair of the Deck Electronics and of the Laser Detection Unit by a service technician is not allowed.

If a failure analysis reveals that the Deck Electronics or LDU are defective, the entire deck should be submitted for repair to the production centre via the Central Repair Procedure of the Concern Service Centre. Please inquire at your parts supplier's for this procedure.

Repairs on the slide drive assy and the Automatic Tilt Control (ATC) assy are possible. See the List of mechanical parts for the correct code numbers.

5. Coding of items

The coding of component items in the service printing of the PCB's can differ from the coding of the items in the circuit diagrams. On the PCB's, a letter/number coding has been used (e.g. R1, C1) and in the diagram a 4 number coding (e.g. 3001,2001). The table below shows the conversion between both coding systems.

Circuit diagram
4 number coding

2 001

item nbr
component nbr:

- | | |
|--------------------------|-------------|
| 1 = Unit, battery | = U |
| 2 = capacitor | = C |
| 3 = resistor | = R |
| 5 = coil, trafo, cristal | = S,L,K |
| 6 = diode | = D |
| 7 = transistor, IC | = T,TS,I,IC |

Service printing on PCB
letter/number coding

C 1

item nbr
component letter:

WARNINGS

1. Laser radiation

The Laser Detection Unit (LDU) in the optical deck has been equipped with a semiconductor laser. This laser emits invisible light which is focussed on the disc by the objective.

If the objective would be removed in case of repair, the laser light exits from the objective aperture. Avoid looking directly into the laser beam, as this might cause permanent injury to the eye.

2. Replacement of modules

Before replacing a module upon repair, first the mains switch should be switched off. This should be done to prevent damage to the circuits on the modules.

3. Service position of the set

If measurements or repair require that the set is placed on its side (90° position), this may only be done when a 6" test disc is played on the optical deck and the front loader has been removed. If a disc with a larger diameter is used (8" or 12"), the risk that the disc will come loose from the turntable (motor) and cause injury to people in the vicinity will be too great. Also ensure that the disc is always locked on the turntable by the magnetic disc clamping piece (see service tools).

In the above-mentioned 90° position of the set not all signals will be present according to specification. Adjustments and checks for correct functioning are therefore only allowed in the horizontal position of the set.

4. The 6" test disc

The 6" test disc may only be played when the front loader has been removed. With mounted front loader playback of 8" and 12" discs is possible.

MODIFICATION LEVELS

In the entire set various modification levels have been indicated.

1. Modification level of the set

The modification level of the set can be found at the rear of the cabinet.

a) Change code on the type number plate

Under the type number a letter and digit code is given which looks as follows :

A	H	0	1	8	7	2	7	8	0	0	1	2	0
production centre				change code				week number				serial number	

The change code is preceded by the production centre.

b) Modification level assembly

On a sticker an ML code is marked, indicating the modification level, in this case ML3.

ML	5	8	11	14
X	6	9	12	15
X	4	7	10	13

c) Production number

Each produced set has a unique following order number, preceded by the type number.

2. Modification level of the module or panel

In the circuit diagram: top right, under the name of the module (e.g. MOD LEVEL 3).

On the PCB: in the service printing at the component side (e.g. X X X 4 5 6 7 8 9 0), or with a sticker as described under 1b.

The modification level is marked then.

3. Modification level of the software in the EPROM's

On Codrive module SR two EPROM's have been applied, which are programmed as follows:

Item	Name	Program number
7104	Drive	3104 103 6821.1
7105	Control	3104 103 6820.1

The program number of the software has been applied on a sticker on the EPROM.

The modification level of the software is the last digit of the program number (behind the dot).

The modification level of the software in the EPROM can also be retrieved by means of an external computer. To achieve this, an F-code command "?=" should be sent to the disc drive (see the directions for use, chapter F-CODE COMMANDS : Revision level request).

The feedback of the disc drive is a 5-digit code of the software revision.

Digit 1 = 0

Digit 2 = major level drive

Digit 3 = minor level drive

Digit 4 = major level control

Digit 5 = minor level control

The modification level of the Drive software will then e.g. be 1.3 (digit 2 . digit 3) and of the Control software e.g. 1.3 (digit 4 . digit 5).

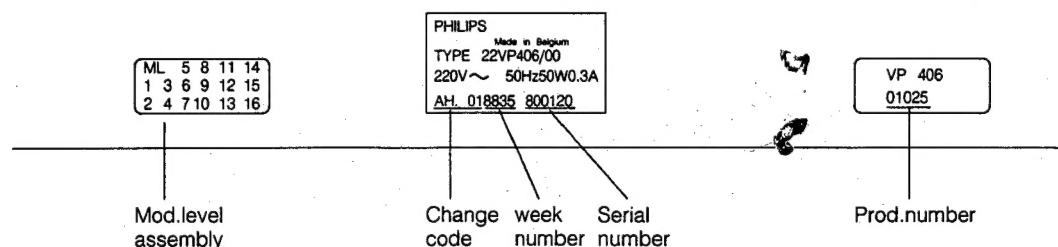
The relation with the modification level in the program number is as follows:

	mod. level progr. number	mod. level software revision
Control	3104 103 6820.1	6.1
Drive	3104 103 6821.1	6.1

Each time a change takes place in the software, the modification level will be raised by one for both software parts.

A survey of the modification levels of the set, the modules and the software can be found in the Service Information, chapter 8.

POSITIONING OF LABELS



ADJUSTMENTS

1. General

For each panel or module, an adjustment procedure is given for components, replaced during repair. Each adjustment procedure is preceded by a description of required tools, adjusting conditions and a summary of items that have to be adjusted when a certain item has been replaced.

The items to be adjusted have been marked  in the diagrams and PCB drawings.

2. Required

To perform the adjustments, the following equipment is required:

- Test disc 6" or 8"
- Dual-beam scope with X-deflection via B-channel (e.g. PM3226P)
- Frequency counter ($\geq 10\text{MHz}$)
- HF generator (10kHz–10MHz)
- Scope probes with 1:10 attenuator, preferable FET probes or probes, having a capacitance $< 3\text{pF}$
- BNC terminator 75Ω (4822 263 60037)

3. Adjustments when panels replaced

If panels or modules are replaced to repair a fault in the drive, some signals have to be checked and/or adjusted.

- Panels A, B, or C : Video signals and MTF
- Motorseq + TBC module D : Sawtooth voltage

1. Panels A, B, or C

In principle, the panels have been adjusted in the factory. Only slight adjustment of the video signals and MTF are required, because of tolerances in components and panels.

First check undermentioned video signals on peak to peak value, black level, sync level and chroma contents. Then the MTF has to be adjusted.

The check procedure is as follows: (Fig.1 Video Adjustments VP406)

a. Video signals

- Use the 6" testdisc and search for pict. nbr 6200 (colour bar)
- Terminate the CVBS OUT connector (BNC) with 75Ω .

Measure CV-DOC on conn. 5C3 Adjust R3243 on panel C (CV-DOC ampl.) for correct oscilloscope.

Measure CV-TBC on conn. 2B6 Adjust R3484 on panel B (CV-TBC ampl.) for correct oscilloscope.

Measure CVBS on BNC conn. (CVBS OUT) Adjust R3408 on panel A (CVBS ampl.) for correct oscilloscope.

Measure G-signal on pin 11 of SCART Adjust R3465 on panel A (RGB ampl.) for 700 mV white.

Measure R- and B -signal on pin 15, resp. pin 7 of SCART Check if the colour amplitude is $525\text{mV} \pm 25\text{mV}$. If not, than adjust R3550 or R3539 on panel A (see adj. A11 on panel A).

b. MTF adjustment

- Use the 6" test disc and search for pict. nbr 515
- Measure the CV-DOC signal on conn. 5C3
- Switch the scope to frame frequency
- Display the 6 frequency blocks in the first quarter of the frame. These frequencies represent the multiburst signals MB I upto MB VI (see Fig. 2)
- Adjust R3450 on panel C until the amplitude of MB I = MB IV

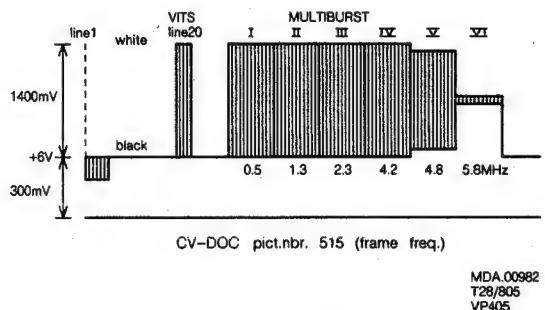


Fig. 2

2. Motorseq. + TBC module D

- Switch the drive into the STAND BY position
- Adjust the sawtooth voltage on p.3-IC7201 for a peak amplitude of $5.2\text{V} \pm 0.1\text{V}$ with R3017 on module D (see Fig. 3).

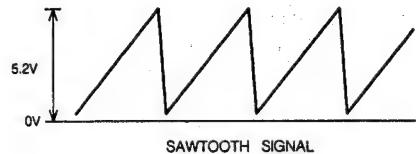


Fig. 3

3. Supply module F

- Switch the drive into the STAND BY position
- Measure the DC voltage (+5SB) on 1B14 on panel B
- Adjust R508 on the Supply module F for a DC voltage of $5.2\text{V} \pm 50\text{mV}$
- Adjust the sawtooth voltage on Motor seq. module D, as described under 2.

ADJUSTMENT OF SEPARATE PANELS

VIDEO PROC PANEL A

Required:

- Test disc 6"
- Scope, dual beam, with X-deflection via B-channel
- Frequency counter

Adjustment conditions:

- Still picture, pict.nbr 6200 (colour bars), unless otherwise mentioned.

Adjustment when item replaced:

replaced	adjust
IC7061	L5001
IC7253	R3213
IC7351	R3327, L5307, C2313, R3539, R3550, R3536, R3545
IC7651	R3539, R3550, R3614, R3465
IC7753	R3536, R3545, R3705, R3709, C2713
IC7153	R3118
IC7352	R3408, R3539, R3550, R3536, R3545

A1 L5001 (Slave source)

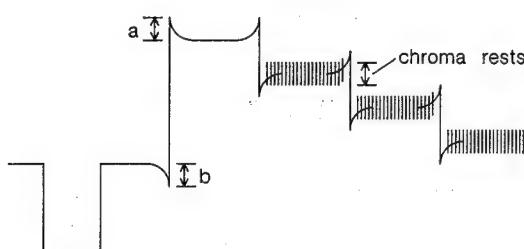
- Switch the drive into the STAND BY position
- Disconnect conn. A3
- Adjust L5001 for a frequency of 5.0 MHz \pm 50Hz on pin 10-IC7061.
- Reinstall conn. A3

A2 R3213 (Sandcastle)

- Switch the drive into the STAND BY position
- Short circuit p.12-IC7253 to mass
- Adjust R3213 for a frequency of 15625 Hz \pm 50 Hz on p.16-IC7253.
- Remove short circuit

A3 L5303 and L5304 (Notch filter)

- Using the scope, measure the luminance signal on p.17-IC7352-2A line triggered (see fig. A1)



LUMINANCE SIGNAL

Fig. A1

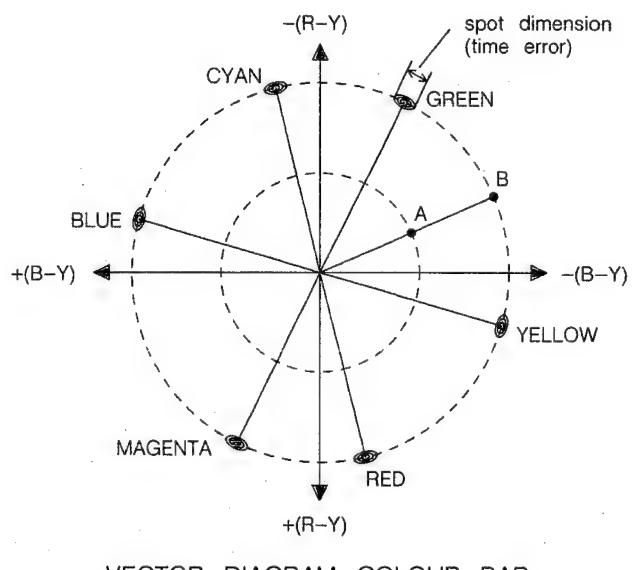
- Adjust L5303 until the chroma rests in the luminance signal have disappeared.
- Adjust L5304 until overshoot a and undershoot b have the same amplitude.

A4 L5302 (Bandpass)

- Measure the chroma signal on p.9-IC7351 with the scope.
- Adjust L5302 for maximum chroma signal.

A5 R3327 and L5307 (Delay line)

- Measure with the scope the (R-Y) signal at p.1-IC7351 with the A-channel and the (B-Y) signal on p.2-IC7351 with the B-chann., both AC coupled.
- Switch the scope to X-deflection and adjust it until the vector diagram below appears (see Fig. A2).



VECTOR DIAGRAM COLOUR BAR

Fig. A2

MDA.00585
T28/711

The colour spots visible on the scope screen are lying at a certain distance B from origin O.

- Short-circuit pins 1-2 or 3-4 of delay line L5310. The spots in the vector diagram will lie closer to the origin now, at distance A from the origin. When the short-circuit is removed, the spots move outwards again (B).
- Adjust L5307 until the dimensions of the spots (in B) are minimal.
- Adjust R3327 until distance OB is twice distance OA in case of alternate short-circuiting of the delay line.

A6 C2313 (Oscillator frequency)

- Connect the scope as described sub A5.
- Short-circuit pins 1-2 or 3-4 of delay line L5310.
- Adjust C2313 until the dimensions of the colour spots of the vector diagram are minimal.

A7 R3118 (TXT bypass)

- Search for a white picture
- Measure with the scope the signal INSERT on p.5-IC7453
- Adjust R3118 for a black-white level of 1.4V \pm 50mV. The black level should be 0V and the sync pulse is not present.

A8 R3408 (CVBS amplitude)

- Measure the CVBS signal (linefrequent) on BNC conn. (CVBS OUT). Terminate the BNC connector with 75Ω
- Adjust R3408 for a video amplitude (top white-black level) of 700mV \pm 35mV (see Fig. A3).

A9 R3614 (Black level)

- Measure with the scope the G-signal on p.11 of SCART
- Adjust R3614 for a black level of $0V \pm 100mV$.

A10 R3465 (RGB amplitude)

- Measure with the scope the G-signal on p.11 of SCART
- Adjust R3465 for a G-signal of $700mV \pm 7mV$ white (see Fig. A3).

A11 R3550 and R3539 (Colour diff. ampl.)

- Using the scope, measure the R-signal on p.15 of SCART and adjust R3550 to the same amplitude of yellow, magenta and red ($525 mV \pm 25 mV$). See Fig. A3
- Using the scope, measure the B-signal on p.7 of SCART and adjust R3539 to the same amplitude of cyan, magenta and blue ($525 mV \pm 25 mV$)

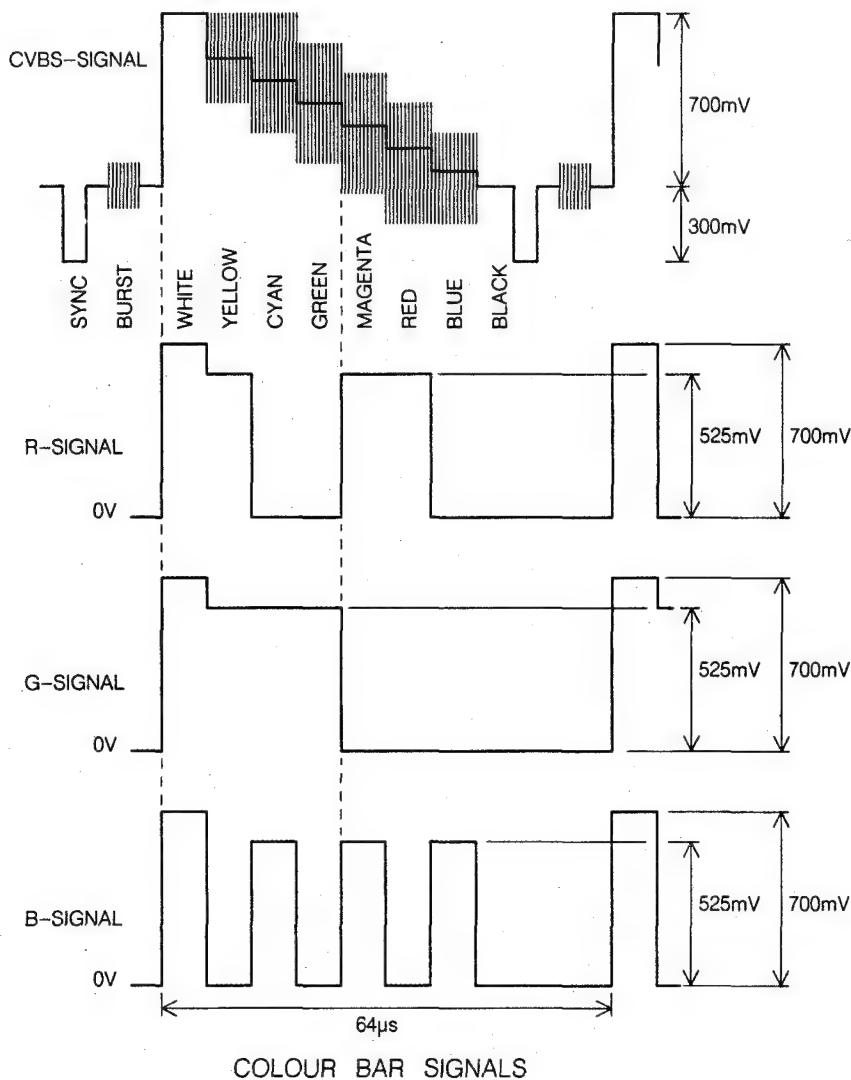


Fig. A3

MDA.01061
T-08 805
VP405

A12 R3740 (Sync amplitude)

- Measure the CVBS OUT signal on BNC (line-frequent) with the scope (see fig. A4)
- Terminate the BNC with $75\ \Omega$.
- Adjust R3740 for a sync-amplitude of $300\text{ mV} \pm 15\text{mV}$ relative to black level.

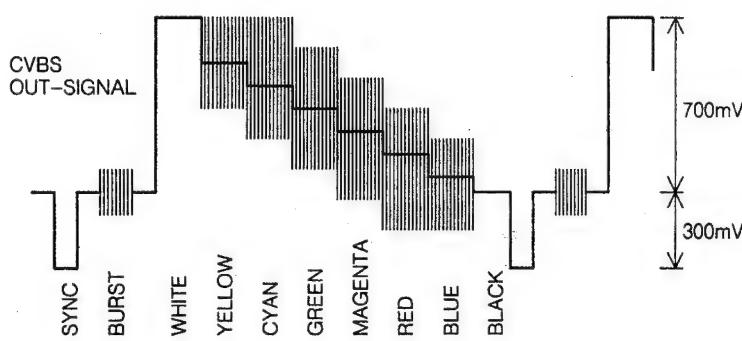
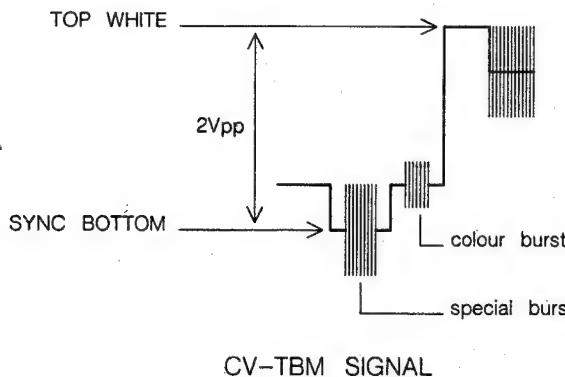


Fig. A4

MDA.00589
T28/715

A13 R3705 and R3709 (Burst amplitude)

- Switch the drive into the STAND BY position.
- Measure the CVBS OUT signal on BNC with the scope (line frequent). Terminate the BNC with $75\ \Omega$.
- Short circuit pins 10 and 12 of IC7753.
- Adjust R3705 for a burst amplitude of $210\text{ mV} \pm 10\text{ mV}$.
- Remove short circuiting of pins 10 and 12.
- Short circuit pins 5 and 10 of IC7753.
- Adjust R3709 for a burst amplitude of $210\text{ mV} \pm 10\text{ mV}$.
- Remove short circuit of pins 5 and 12.
- (The burst amplitude will increase to approx 300 mV).

A14 R3536 and R3545 (Colour diff. ampl.)

- Measure the CVBS OUT signal on BNC (line-frequent) with the scope (see fig. A4)
- Terminate the BNC with $75\ \Omega$.
- Adjust R3536 until the upper side of the chroma signal during the yellow bar lies at the same level as the white signal (700 mV).
- Adjust R3545 until the upper side of the chroma signal during the cyan bar lies at the same level as the white signal.

A15 C2713 (Chroma subcarrier)

- Adjust the carrier frequency on p.3-IC7753 for a frequency of $4433618\text{ HZ} \pm 5\text{Hz}$ with C2713.

RAD + TBC PANEL B

Required

- Test disc 6"
- Scope, dual beam
- Frequency counter

Adjustment conditions:

- Still picture, pict.nbr 6200 (colour bars), unless otherwise mentioned.

Adjustments when item replaced:

replaced	adjust
IC7401	R3419, R3484
IC7402	R3423

B1 R3423 (CCD pass through)

- Switch the drive into the STAND BY position
- Short circuit p.9-IC7402 to mass
- Measure the frequency on p.6-IC7403 with the freq. counter
- Adjust R3423 for a frequency of $9.7\text{ MHz} \pm 50\text{ kHz}$.
- Remove the short circuit

B2 R3419 (CCD adjust)

- Switch the drive into the STAND BY position
- Disconnect conn. B7 from its socket (interruption of CV-DOC on 6B7)
- Measure the DC level on p.1-IC7401
- Adjust R3419 for a DC level of $2,8\text{ V} \pm 100\text{mV}$
- Reinstall connector B7

B3 R3490 (Video time error)

- Search for pict. nbr 3000 (cyan)
- Adjust R3490 for minimum dark bars and minimum green stripes in the cyan picture.

B4 R3484 (CV-TBC amplitude)

- Search for pict. nbr 6200 (colour bars)
- Measure the CV-TBC signal on conn. 2B6
- Adjust R3484 for a video amplitude (top white-sync bottom) of $1.25\text{Vpp} \pm 50\text{mV}$ (see Fig. B1)
- Check the video amplitude on CVBS OUT (BNC) for correct value (1Vpp).

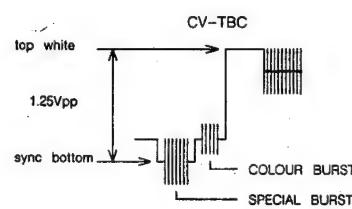


Fig. B1

MDA.00984
T28/748
VP405

HF + AUDIO PANEL C

Required

- Test disc 6"
- Scope, dual beam
- HF generator (1kHz-10MHz)

Adjustment conditions:

- Still picture, pict.nbr 6200 (colour bars), unless otherwise mentioned.

Adjustments when item replaced:

replaced	adjust
IC7220	R3243
IC7451	R3465, L5407
IC7117	R3114, R3128
IC7115	L5100, L5101, R3106, R3128, R3114, R3123

C1 L5201, L5202, L5204 (Audio dip 875kHz, MTF, Audio dip 2.8MHz)

- Disconnect conn. C1
- Connect an HF generator signal to conn. 2C1 and its ground to 3C1
- Switch the drive into the STAND BY position
- Measure the signal on 5-IC7220-3A with the scope. Use probe 1:10 attenuation and connect probe ground to minus of elco C2202

Set the generator to a frequency of 875 kHz and an amplitude of 2 Vpp and adjust L5201 for minimum amplitude of the scope signal.

- Set the generator to a frequency of 8 MHz and an amplitude of 330 mV and adjust L5202 for maximum amplitude of the scope signal.
- Measure the signal on 3C3 (HF-AUD) with the scope.
- Set the generator to a frequency of 2.8 MHz and an amplitude of 2 V and adjust L5204 for minimum amplitude of the scope signal.
- Reinstall connector C1.

C2 R3243 (CV-DOC amplitude)

- Search for picture nbr 6200 (colour bars)
- Measure CV-DOC on conn. 5C3
- Adjust R3243 for a video amplitude (top white-sync bottom) of 2Vpp (see Fig. C1)

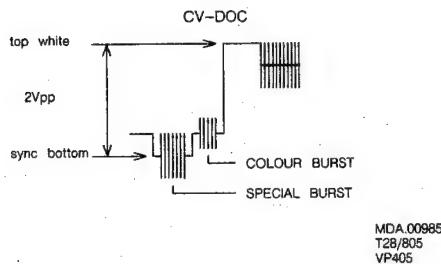


Fig. C1

- Check the video amplitude on CVBS OUT (BNC) for correct value (1Vpp)

C3 R3465, L5407 (Drop out correction)

- Search for pict. nbr 10800
- The picture on the screen is shown in Fig. C2

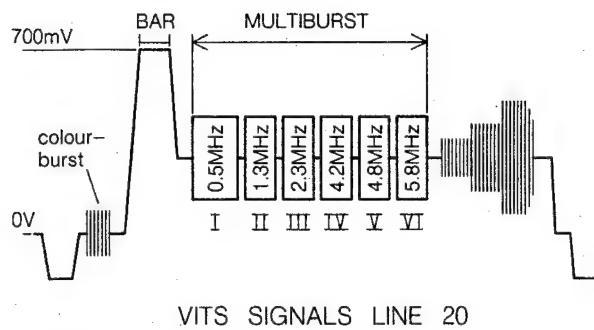
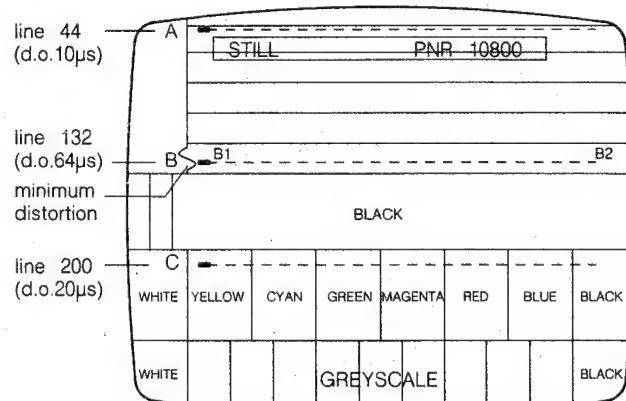


Fig. L2



DROP OUT SIGNALS

MDA.00588
T28/711

Fig. C2

- Adjust L5407 until drop-out A gives a white completion of the vertical lines at the right place and drop-out B gives minimum distortion at the place indicated.
- Adjust R3465 until drop-out B is invisible.

C4 L5403, R3450 (MTF)

- Search for picture no. 1000 (blue).
- Using the scope, measure the CVBS OUT-signal on BNC (rear), 75Ω terminated, triggered line frequent.
- Adjust L5403 for min. amplitude of the chroma signal.
- Search for pict. nbr 515
- Measure the CV-DOC signal on conn. 5C3
- Switch the scope to frame frequency
- Display the 6 frequency blocks in the first quarter of the frame. These frequencies represent the multiburst signals MB I upto MB VI (see Fig. C3)
- Adjust R3450 until the amplitude of MB I = MB IV.

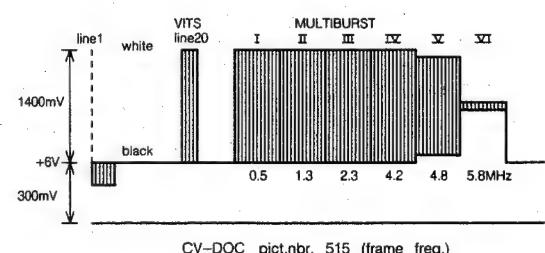


Fig. C3

C5 L5100, L5101 (Audio 90° fase shift)

- Normal play, pict. nbr 4615-5399 (replay). Continuous audio modulation 1kHz on Audio 1 and Audio 2 is audible
- Measure the output voltage on conn. 4C2 and 2C2 (AUD1 and AUD2) with the scope
- Adjust L5100 and L5101 until the distortion of the sinewave is minimal (see Fig. C4). Compare both AUD1 and AUD2 for correct symmetry of the sinewave.
- Adjust R3114 and R3123 (Audio ampl.) as described under C6.

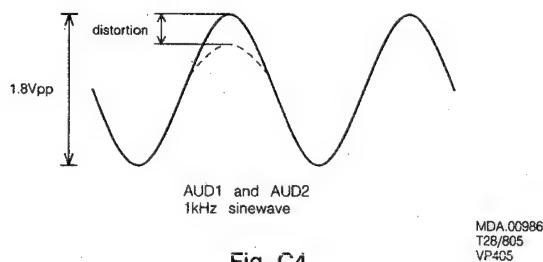


Fig. C4

C6 R3114, R3123 (Audio amplitude)

- Normal play, pict. nbr 4615-5399 (replay). Continuous audio modulation 1kHz on Audio 1 and Audio 2
- Measure the output voltage on conn. 4C2 and 2C2 (AUD1 and AUD2) with the scope
- Adjust R3114 and R3123 until the output voltage is 1.8Vpp.

C7 R3106, R3128 (Audio Drop Out correction)

- Normal play, pict. nbr 6000-6250 (replay). Continuous audio noise with several 2μsec-Drop Out pulses on Audio 1 and Audio 2 is audible
- Measure the output voltage on conn. 4C2 and 2C2 (AUD1 and AUD2) with the scope
- Adjust R3106 and R3128 until the Drop Out pulses in the noise signal just have disappeared. Pulses < 30 mVpp are allowed.

MOTORSEQ + TBC MODULE D

Required

- Test disc 6"
- Scope, dual beam
- Frequency counter

Adjustment conditions:

- Still picture, pict.nbr 6200 (colour bars), unless otherwise mentioned.

Adjustments when item replaced:

replaced	adjust
IC7201	C2215

D1 C2215 (Reference frequency)

- Switch the drive into the STAND BY position and wait at least 5 minutes before adjusting
- Measure the frequency on E-TS7218 with the freq. counter
- Adjust C2215 for a frequency of 4.5 MHz ± 20 Hz.

D2 R3392 (Sync position)

- Select STILL PICTURE 450.
- Display the CVBS-out signal on an oscilloscope.
- Select horizontal speed to 2 μsec/div.
- Adjust the time between end of the syncpulse and the beginning of the video to 12,0 ± 0,1 μsec with R3392.

D3 R3368 (Nominal tangential error)

- Switch the drive into the STAND BY position
- Measure the DC voltage on conn. 7D11 (TANG-ER) and adjust R3368 for a voltage of 1.3V ± 0.1V.

D4 L5320 (Special Burst amplitude)

- Search for pict. nbr 6200
- Measure the chroma signal on p. 1-IC7302-4A, linefrequent
- Adjust L5320 for a maximum amplitude (300mV±100mV) of the special Burst signal.

SUPPLY MODULE F

Required:

- Voltmeter

Adjustment conditions:

- STAND BY position of the drive

Adjustment when item replaced:

replaced adjust
Motor seq. R508
mod. D

F1 R119 (Output power)

a. General

The adjustment procedure for the output power is dependent on the typenumber of the disc drive. This adjustment is critical in VP415 and not critical in the other models of the VP4xx series.

In any case the output power of the Supply module should be adjusted so that the ripple on the DC voltage +13 is not lower than +12.2 V during starting up and braking of the motor of the disc drive.

b. Adjustment for VP415:

- Measure the DC voltage +13 on 1B15 on panel B with the scope.
- Intermittently switch the drive into the play mode and into the stand-by mode (starting up and braking the motor).
- Adjust R119 so that the lower part of the ripple on the DC voltage +13 just reaches the +12.2 V value during starting up and braking of the motor.
- Turn R119 approx. 45° counter-clockwise.

c. Adjustment for others

- Turn R119 fully counter-clockwise and next 45° clockwise.

F2 R508 (DC voltage +5)

- Measure the DC voltage (+5SB) on 1B14 on panel B
- Adjust R508 for a DC voltage of +5,2V ± 50 mV.

F3 R605 (DC voltage -12SB)

- Measure the DC voltage (-12SB) on 7B15 on panel B
- Adjust R605 for a DC voltage of -12 V ± 50 mV.

F4 R805 (DC voltage +12SB)

- Measure the DC voltage (+12SB) on 1B15 on panel B
- Adjust R805 for a DC voltage of +12 V ± 50 mV.

BLOCKDIAGRAM AUDIO/VIDEO SIGNALPATH VP406

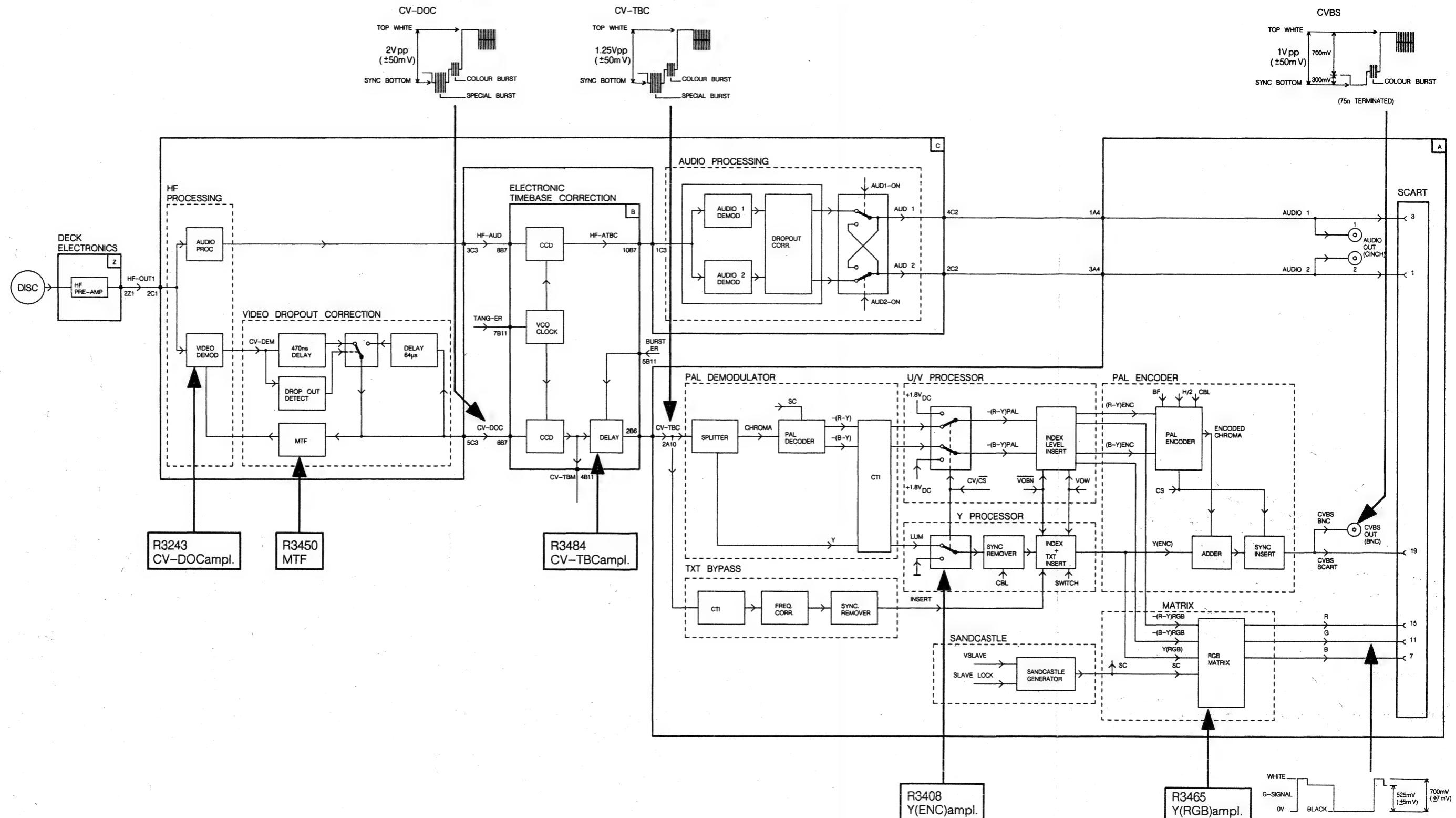
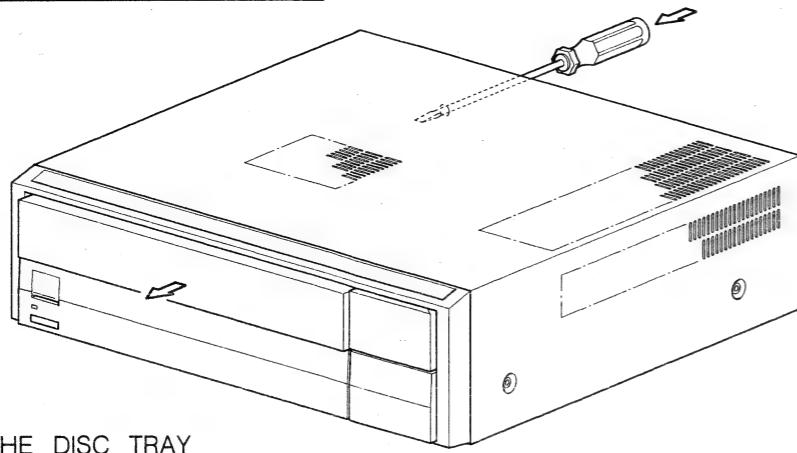


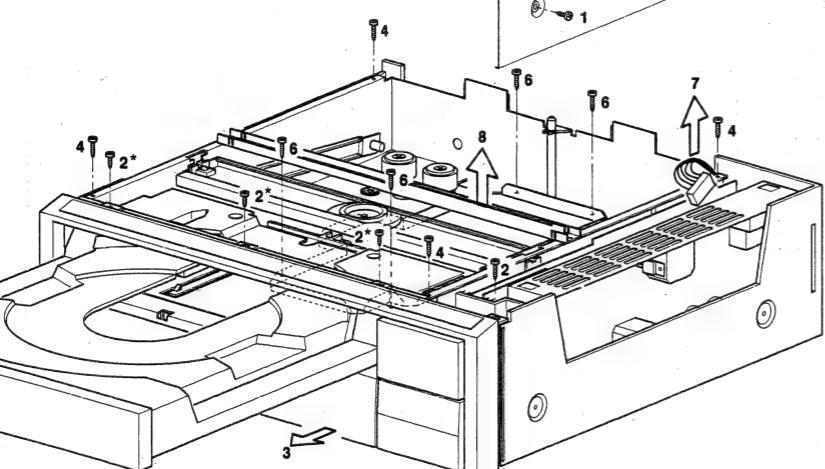
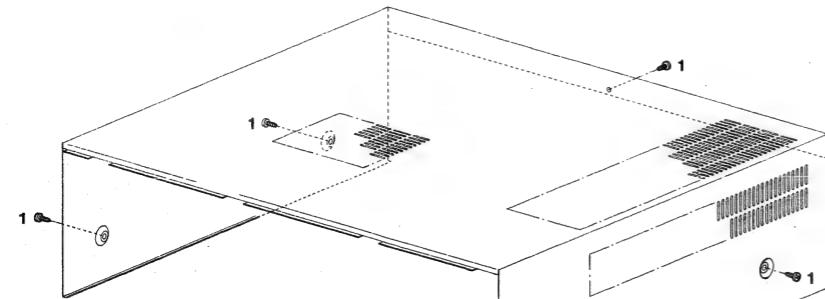
Fig.1

VIDEO ADJUSTMENTS VP406

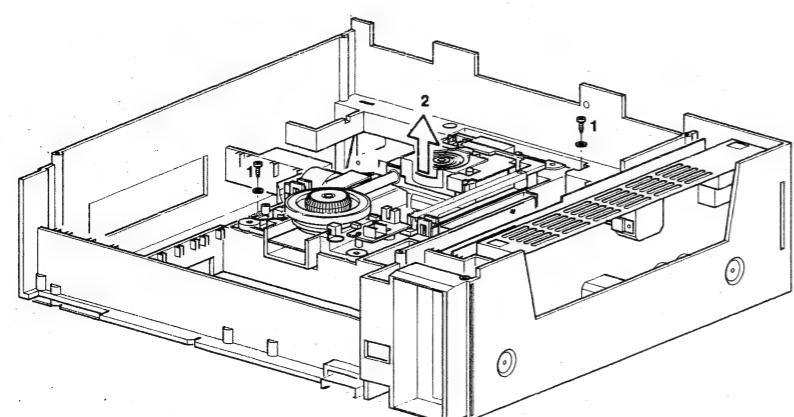
DEMOUNTING INSTRUCTIONS



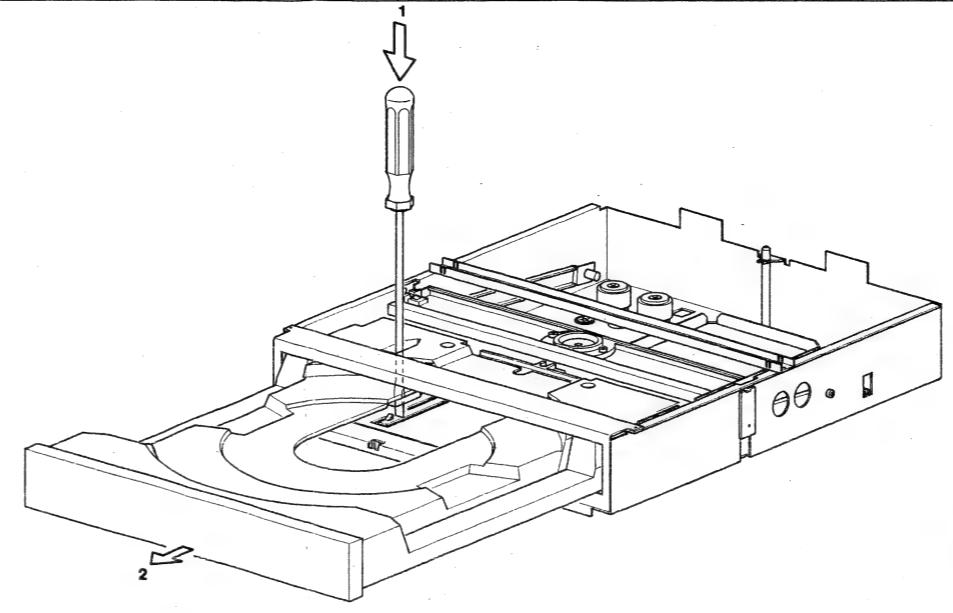
PUSHING OUT THE DISC TRAY



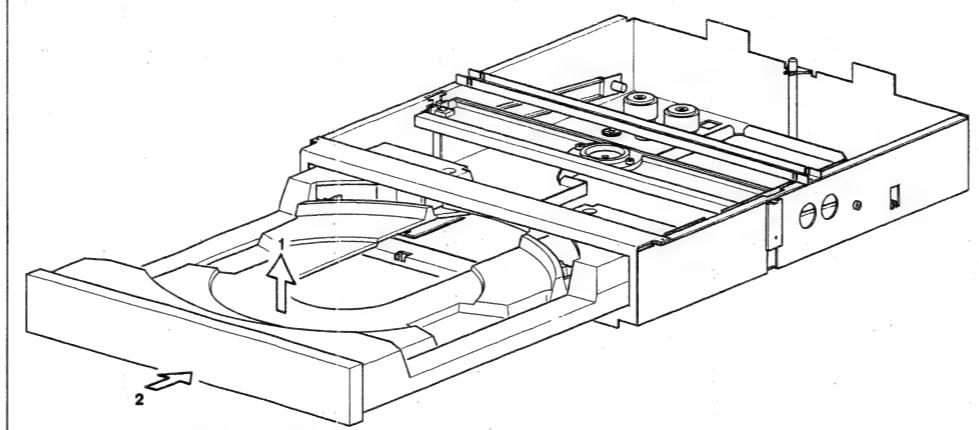
* short size
DEMOUNTING UPPERCASET AND FRONTLOADER



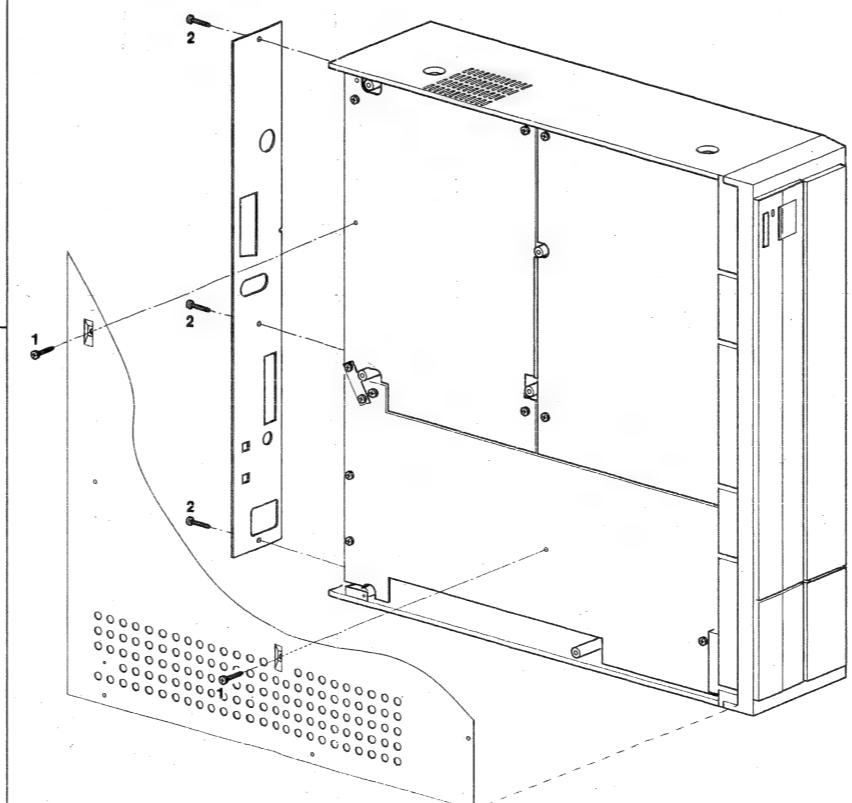
DEMOUNTING OPTICAL DECK



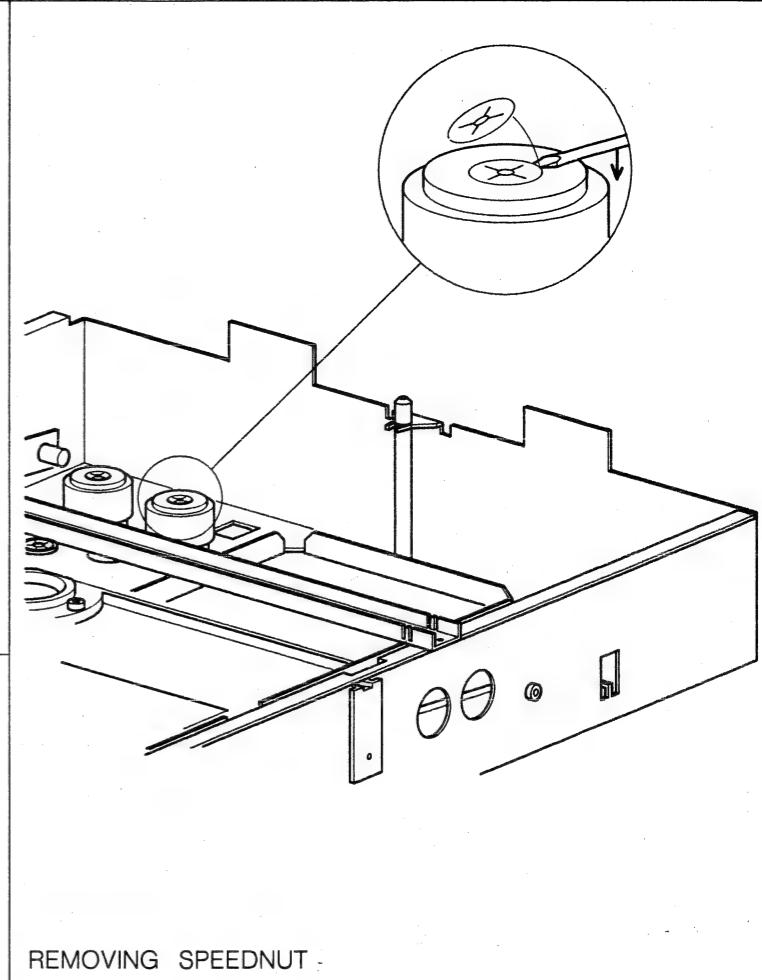
DEMOUNTING DISC TRAY ASSY



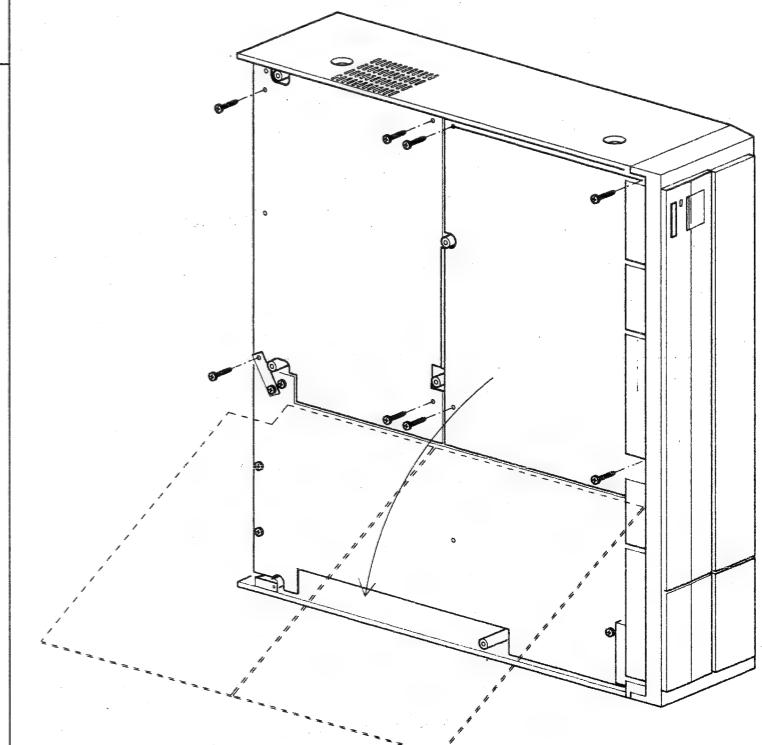
MOUNTING DISC TRAY ASSY



REMOVING COVERS



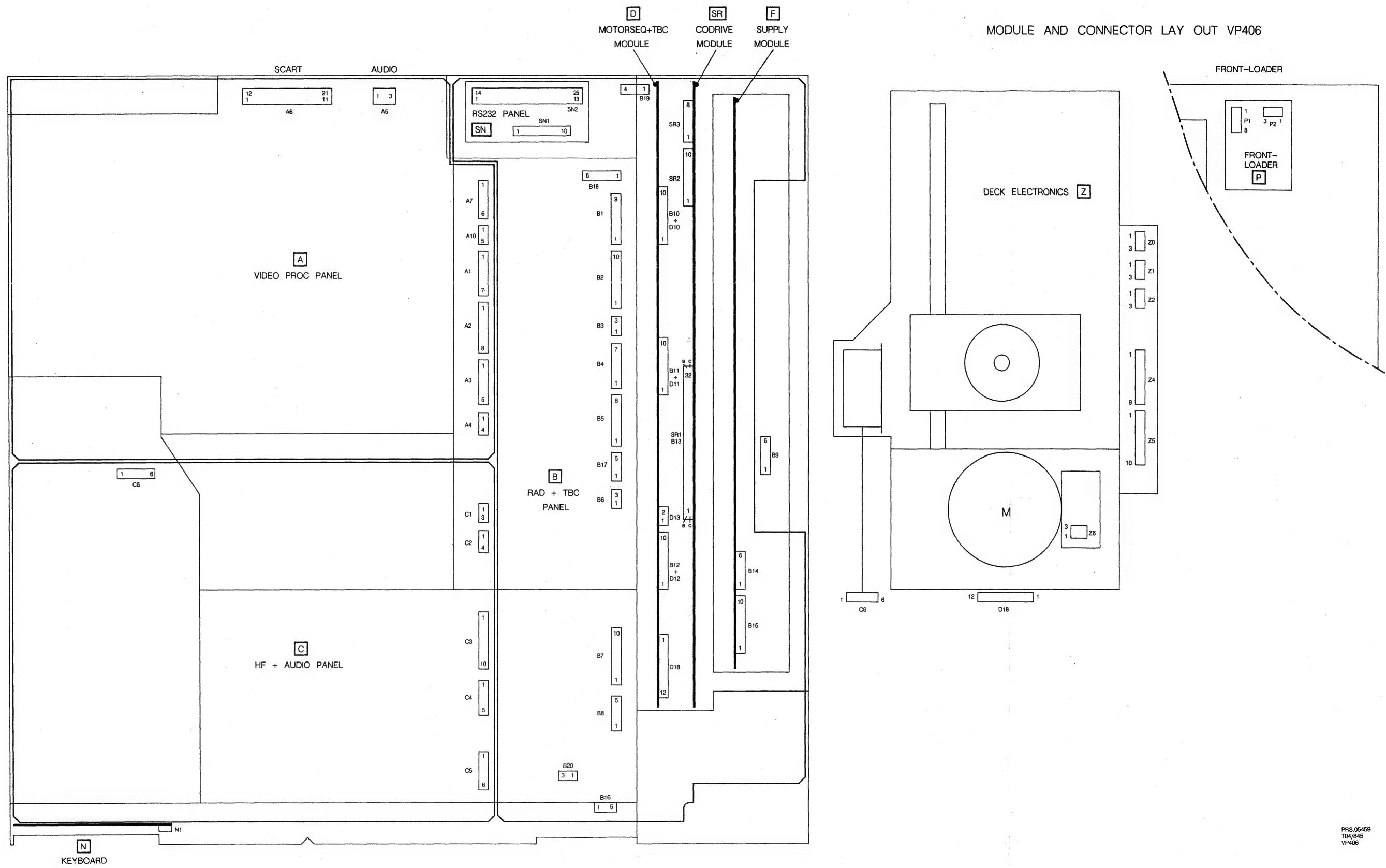
REMOVING SPEEDNUT



SERVICE POSITION PANELS

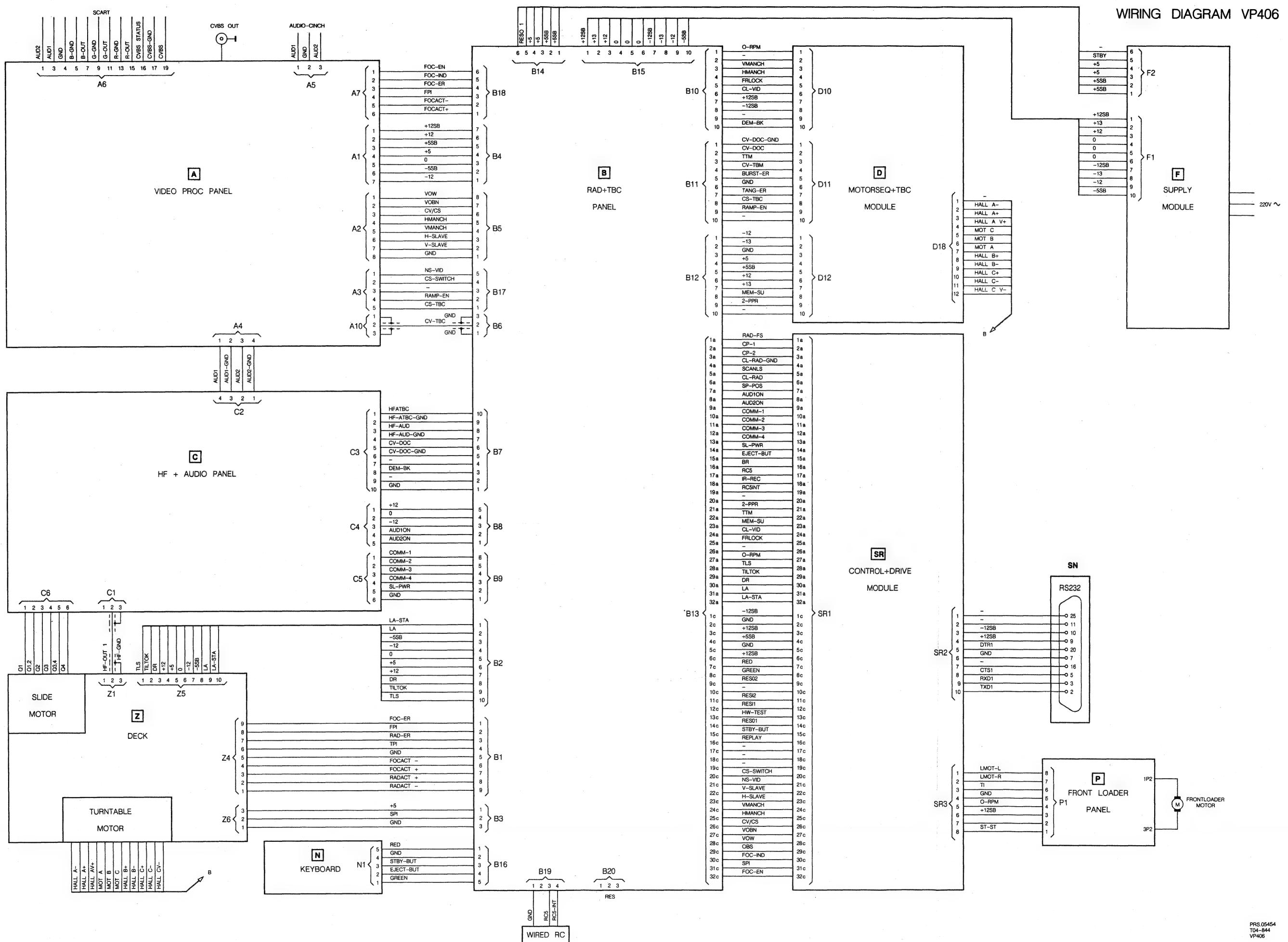
EVA.00506
T28/752

MODULE AND CONNECTOR LAY OUT VP406



ALPHABETICAL SIGNAL LISTING

WIRING DIAGRAM VP406



BLOCKDIAGRAM AUDIO/VIDEO SIGNALPATH VP406

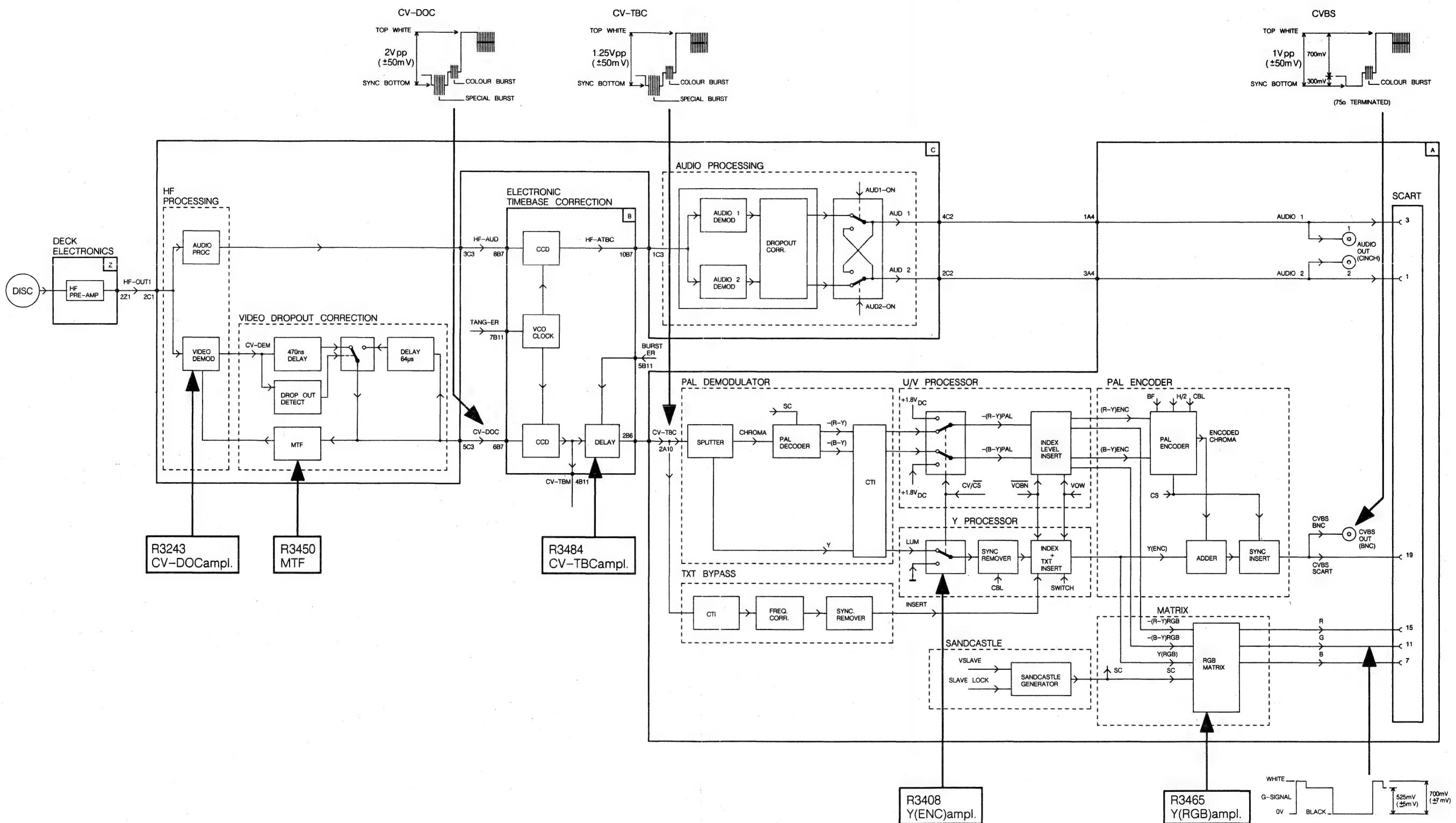


Fig.1

VIDEO ADJUSTMENTS VP406

PRS.05535
T02/847
VP406

SERVICE HINTS

WARNING

ESD



All ICs and many other semi-conductors are susceptible to electrostatic discharges (ESD). Careless handling during repair can reduce life drastically.

When repairing, make sure that you are connected with the same potential as the mass of the set via a wrist wrap with resistance.

Keep components and tools also at this potential.

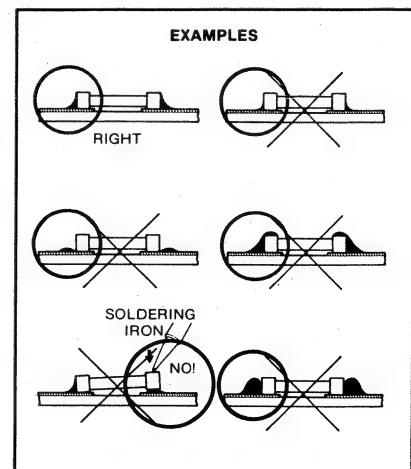
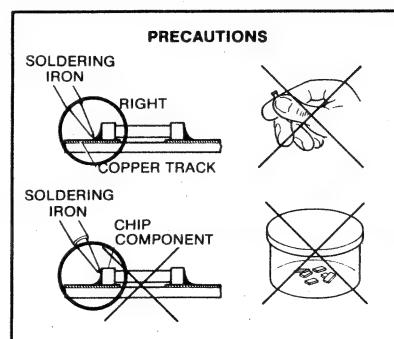
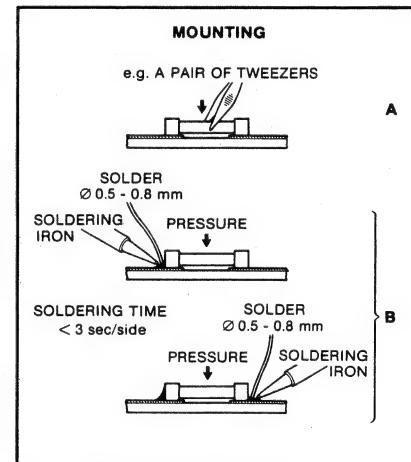
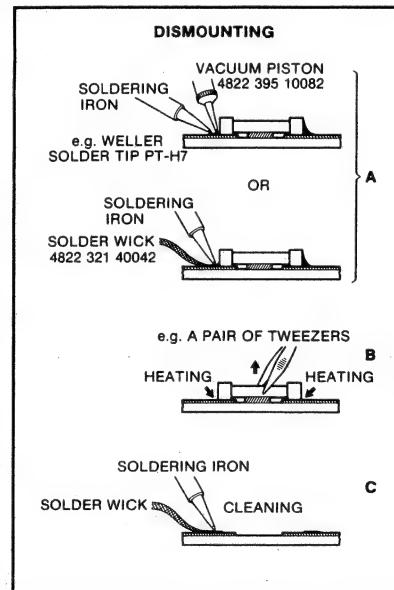
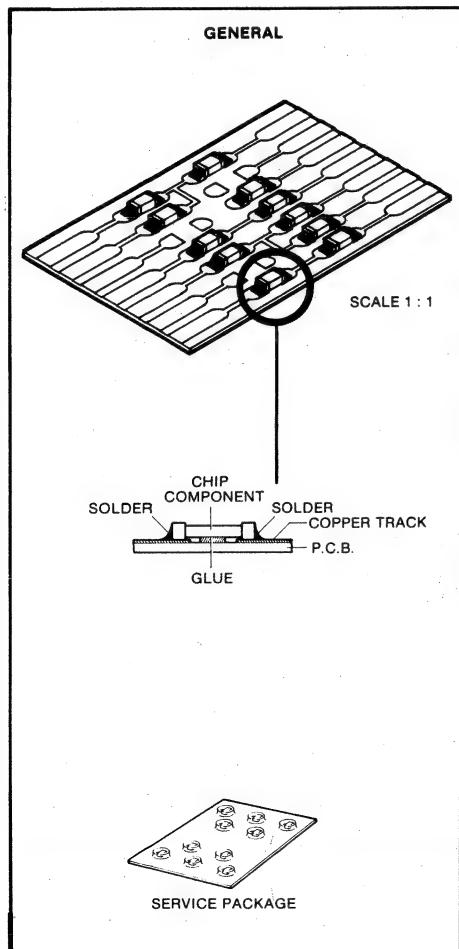
The photodiodes and the laser are more sensitive to electrostatic discharges than MOS IC's.

Careless handling during servicing may reduce life expectancy drastically.

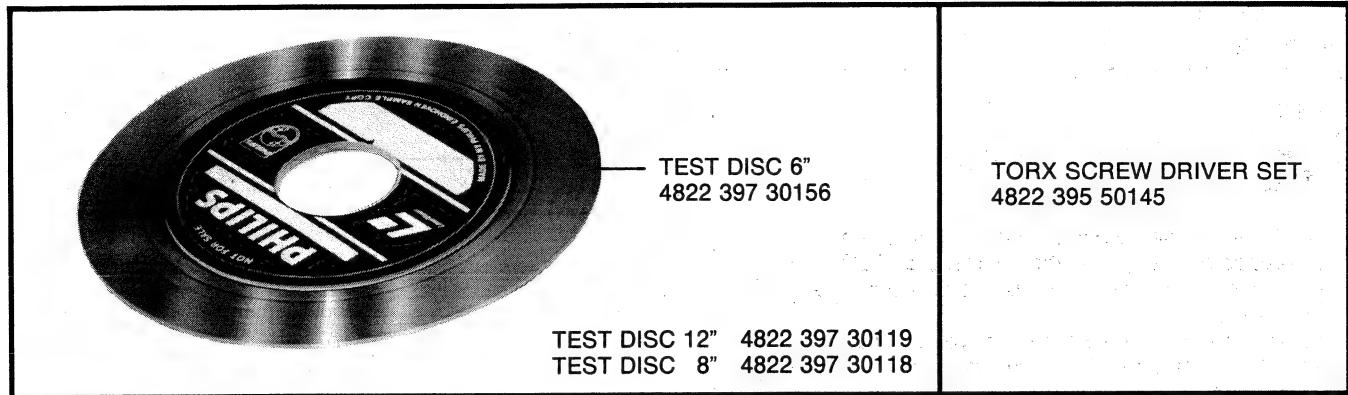
For this reason care should be taken that during servicing the potentials of the tools and yourself are equal to that of the screening of the set

Chip components (SMD)

Chip components have been applied in the set. For the insertion and removal of chip components see the figure below.

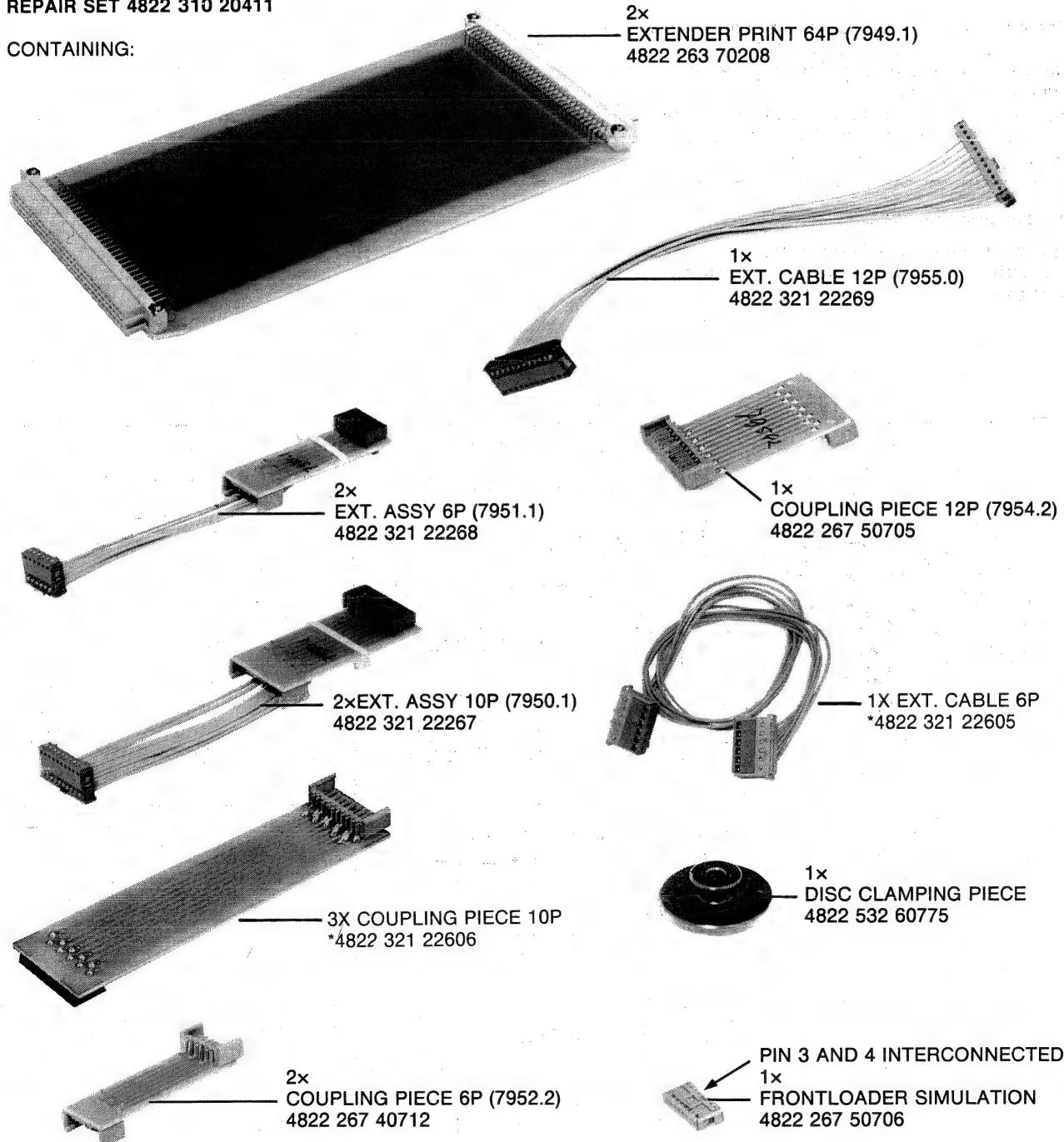


SERVICE TOOLS

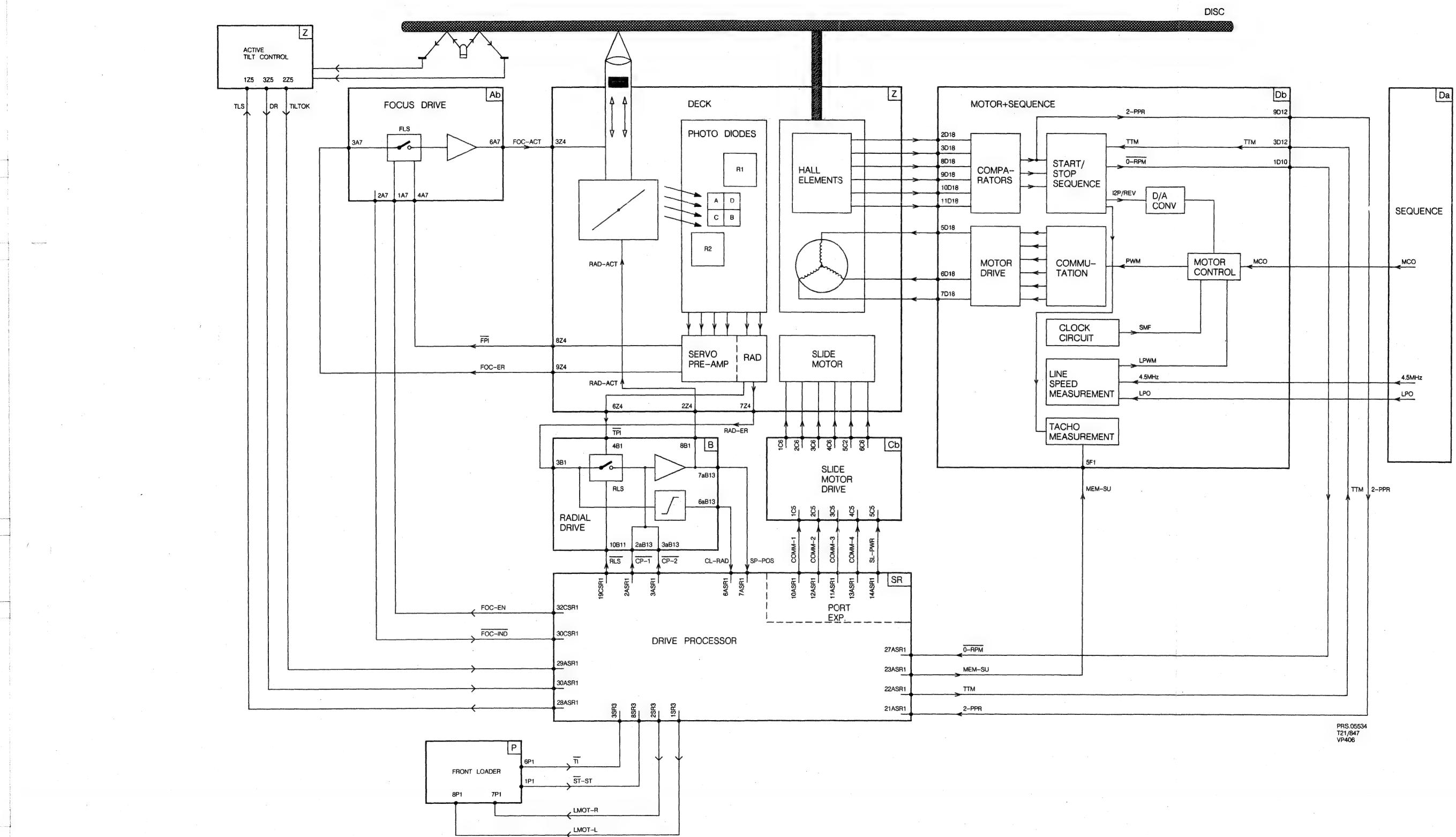


REPAIR SET 4822 310 20411

CONTAINING:

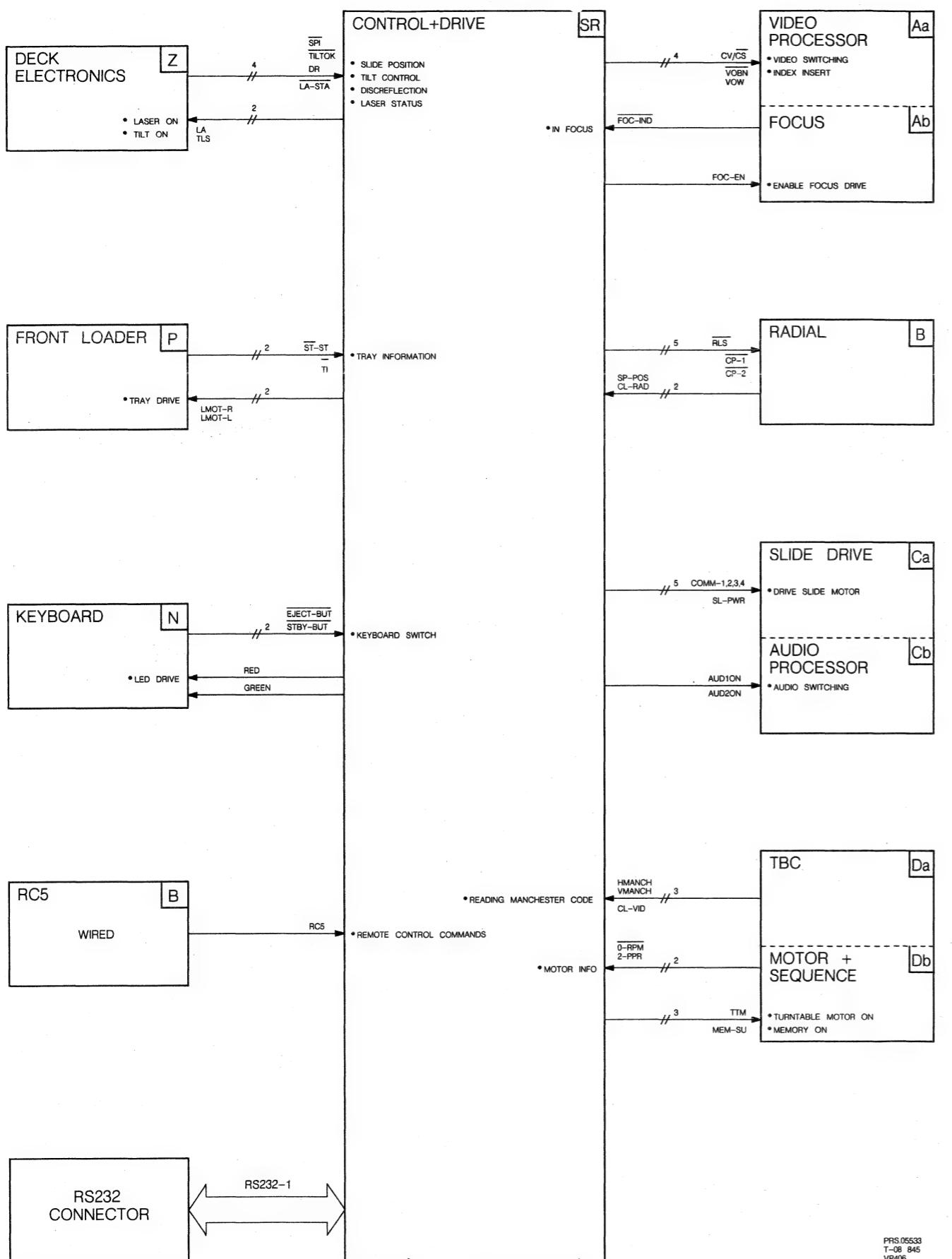


BLOCKDIAGRAM SERVO VP406

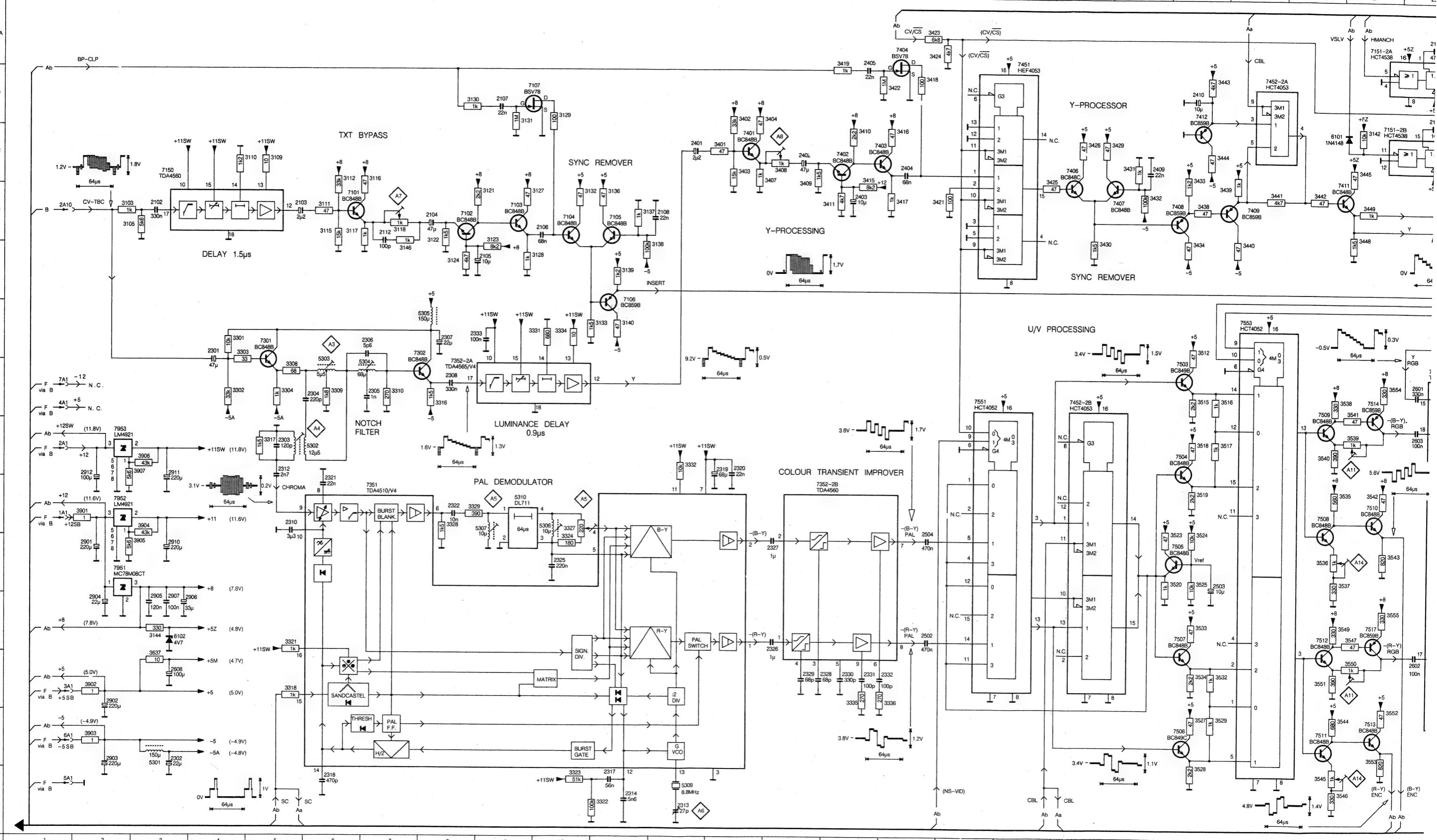


PRS 05534
T21/847
VP406

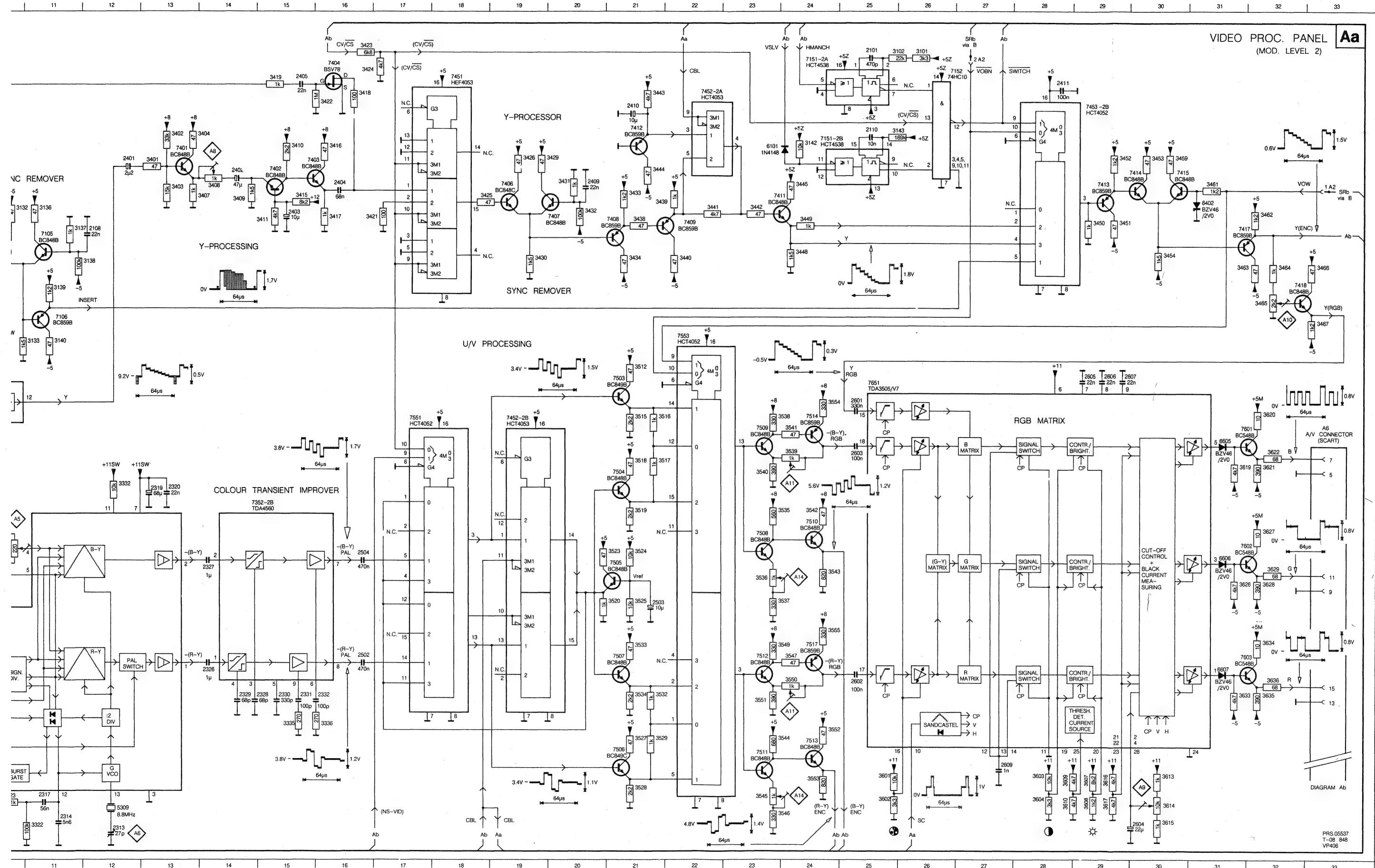
BLOCKDIAGRAM CONTROL ROUTES VP406



2101	A25	2110	B25	2307	F 8	2319	H13	2329	L14	2404	C16	2601	G25	2609	M27	2910	J 3	3110	C 5	3122	D 8	3132	D11	3302	G 4	3318	L 5	3331	F10	3404	B14	3417	D16	3426	C19	3439	D21	3449	D24	3462	D32	3516	G22	3527	M21	3537	J24	3545	N23	3554	G24	3609	M28	3620	G32		
2102	D 3	2112	D 7	2308	G 6	2320	H13	2333	L15	2405	C15	2602	L25	2901	J 2	2911	H 3	3111	D 6	3123	E 8	3136	D11	3303	F 4	3321	H12	3407	C14	3418	B16	3429	C20	3440	D22	3450	D29	3463	E31	3517	H22	3526	M21	3538	G24	3610	K24	3613	M30	3622	H32						
2103	D 5	2301	F 4	2310	I 5	2321	H 6	2331	L16	2405	C20	2602	L25	2902	J 2	2912	H 2	3112	C 6	3122	E 8	3137	D12	3304	G 5	3322	N11	3334	F10	3408	C14	3419	A15	3430	D19	3441	D29	3451	D29	3464	E32	3518	H21	3529	M21	3539	K24	3544	J24	3614	N25	3615	M28	3626	J32		
2104	D 8	2302	M 3	2312	H 5	2322	I 8	2332	L16	2410	B21	2604	F20	2903	M 2	2913	D 5	3112	C 6	3122	E 8	3137	D12	3304	G 5	3323	N10	3335	L15	3409	C14	3421	D17	3431	C20	3442	D23	3452	C29	3465	E32	3519	L21	3532	K21	3540	H23	3549	K24	3602	N25	3613	M30	3622	H32		
2105	E 9	2303	H 5	2313	N12	2323	J10	2333	F 9	2411	K14	2601	C12	2602	A25	3102	K 3	3103	D 2	3117	D 6	3129	B10	3144	K 3	3310	G 7	3327	I10	3401	C13	3411	A15	3423	C15	3433	C21	3444	C21	3454	D30	3467	F33	3520	J21	3533	K21	3541	G24	3550	L24	3603	M28	3615	N29	3627	J32
2106	D 10	2304	G 6	2314	N11	2326	K14	2401	C12	2502	K16	2606	F29	2905	K 3	3103	D 2	3117	D 6	3129	B10	3144	E 7	3316	G 8	3328	B13	3402	C13	3415	A16	3434	D21	3445	C24	3459	C30	3512	F21	3524	I21	3535	L21	3542	J21	3553	M24	3552	L24	3607	M29	3617	N29	3629	J32		
2107	B 9	2305	G 7	2317	N11	2327	J14	2402	C14	2503	K21	2607	F30	2906	K 4	3105	D 7	3118	D 9	3130	B 9	3301	F 4	3317	H 5	3329	I 8	3403	C13	3416	C16	3425	C18	3438	D21	3448	C24	3461	C31	3515	G21	3525	J23	3544	M24	3552	M24	3608	N29	3616	M28	3629	N29	3633	J32		

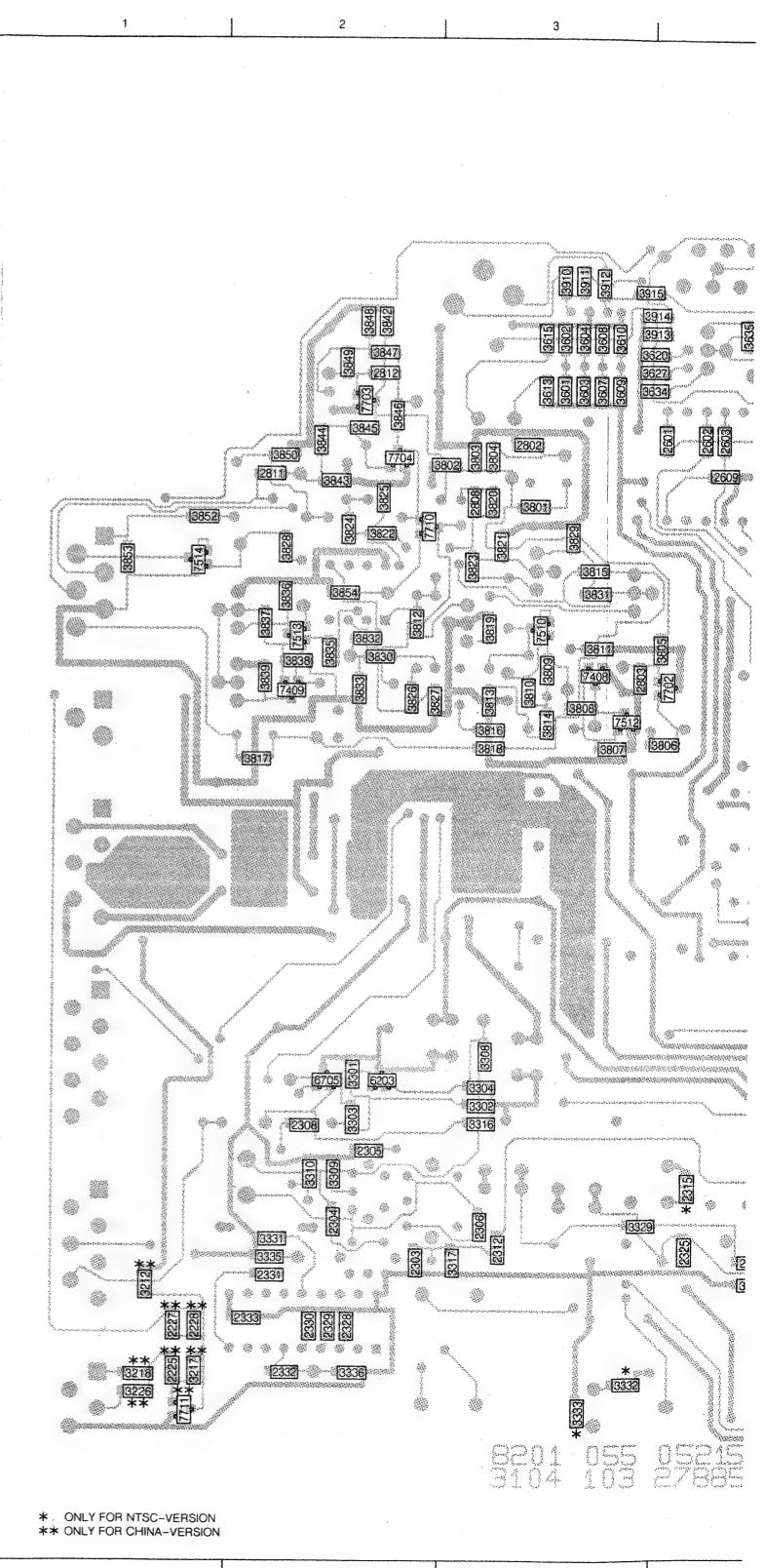
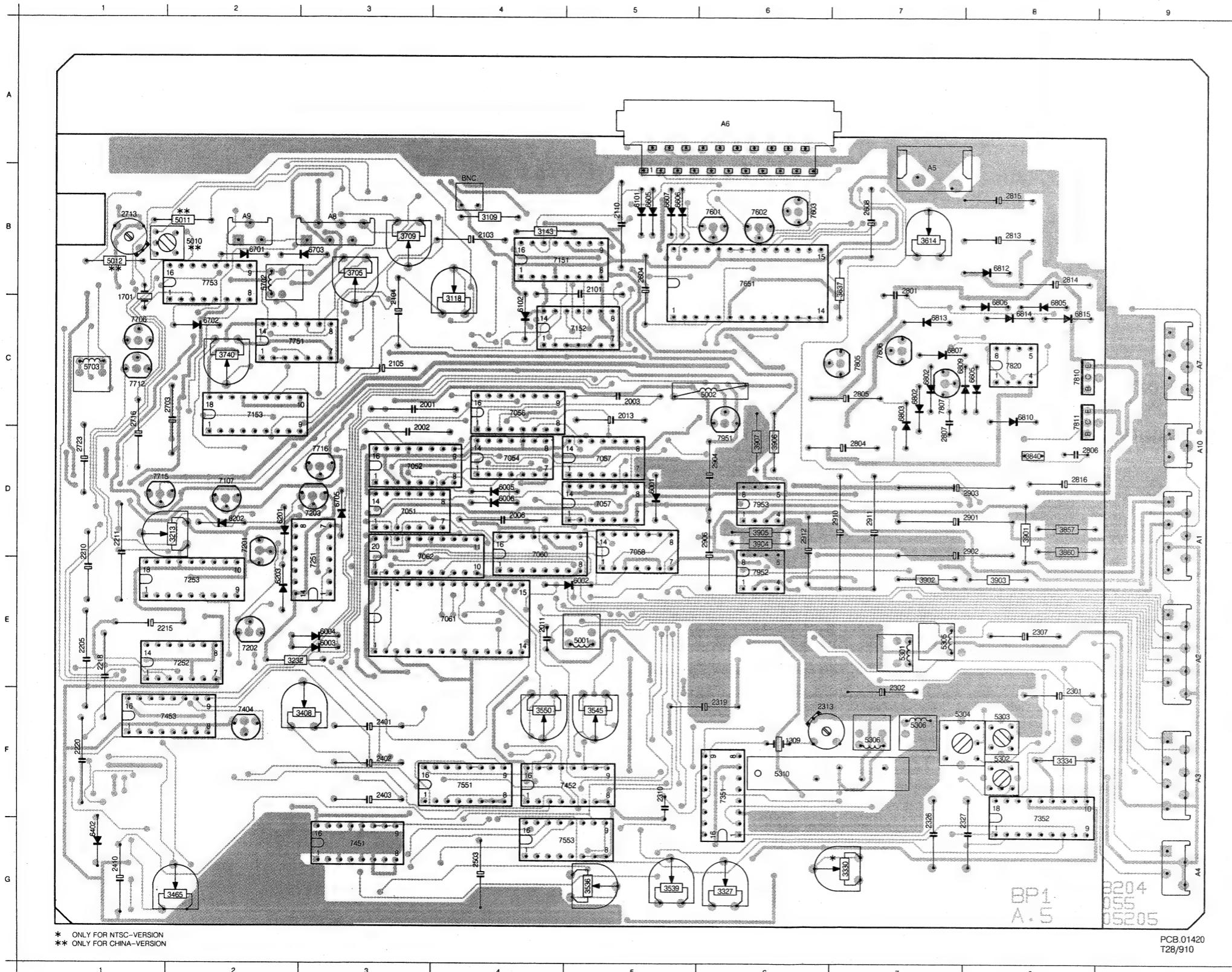


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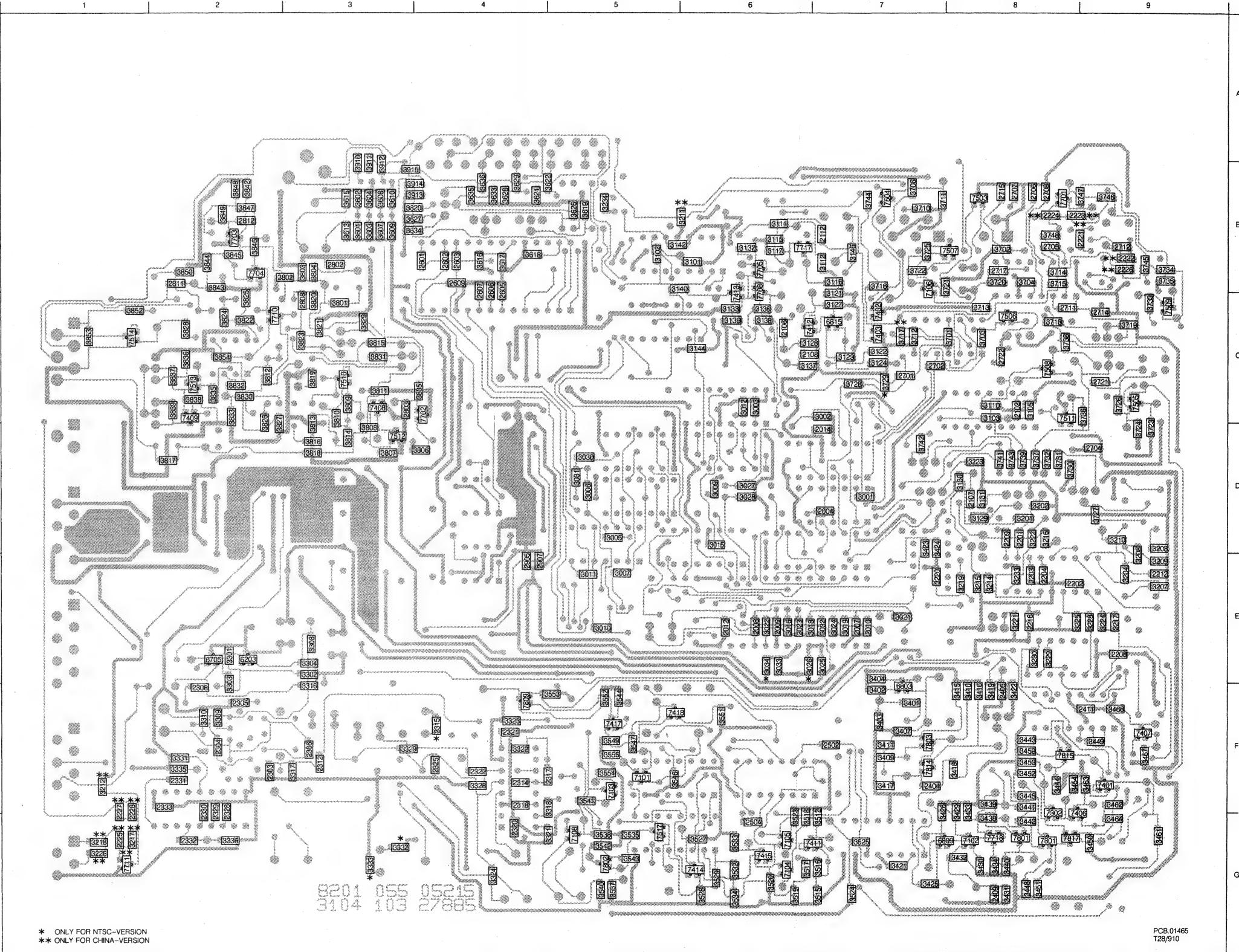
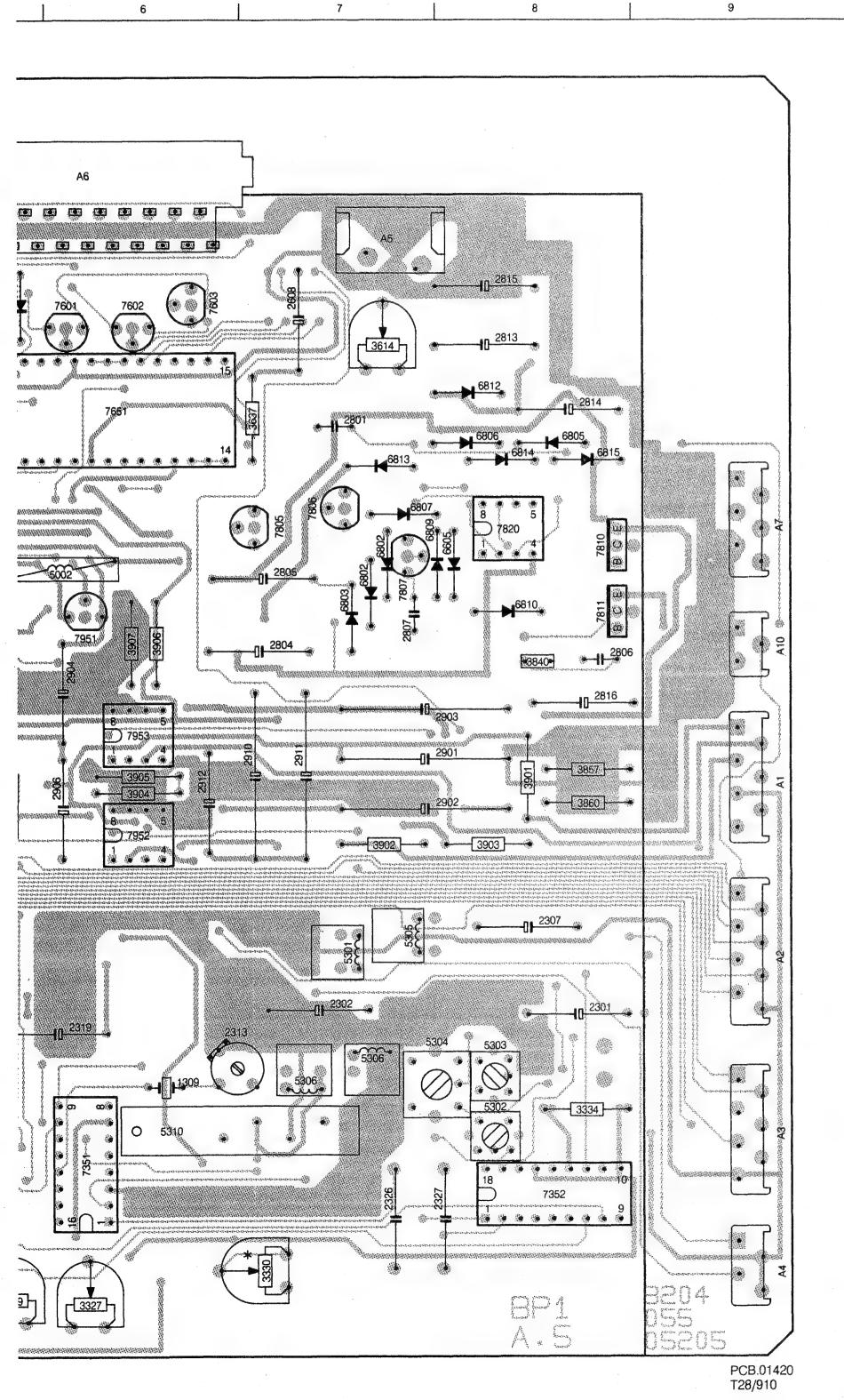
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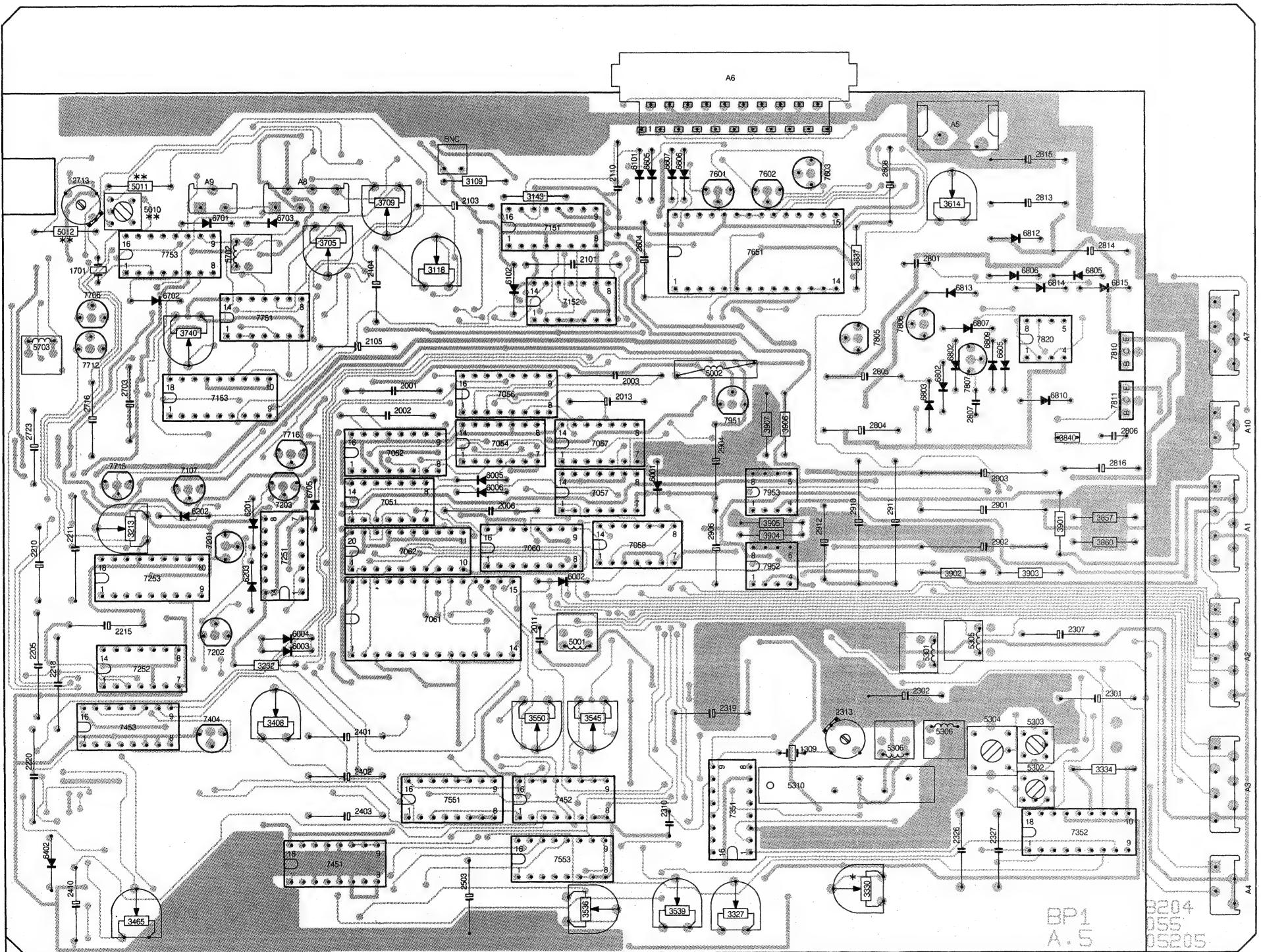
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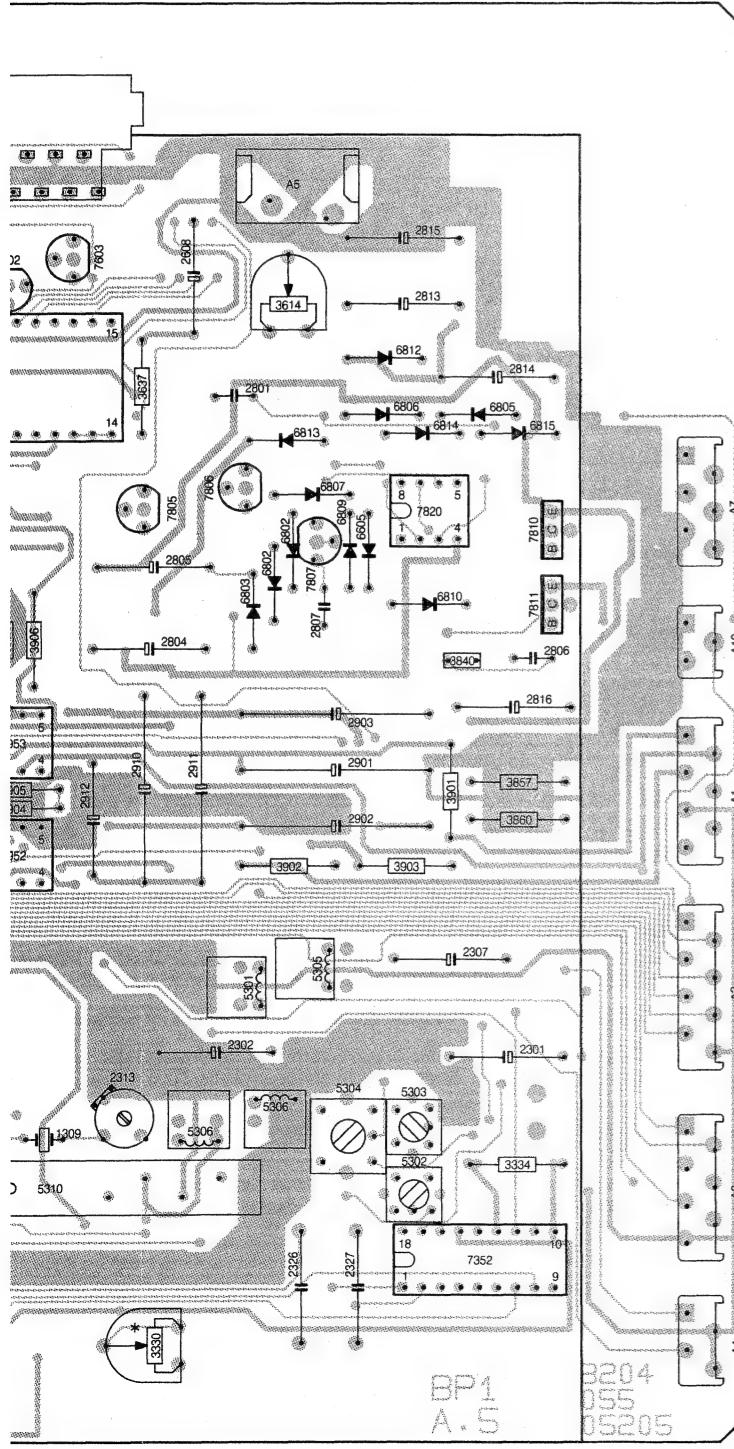
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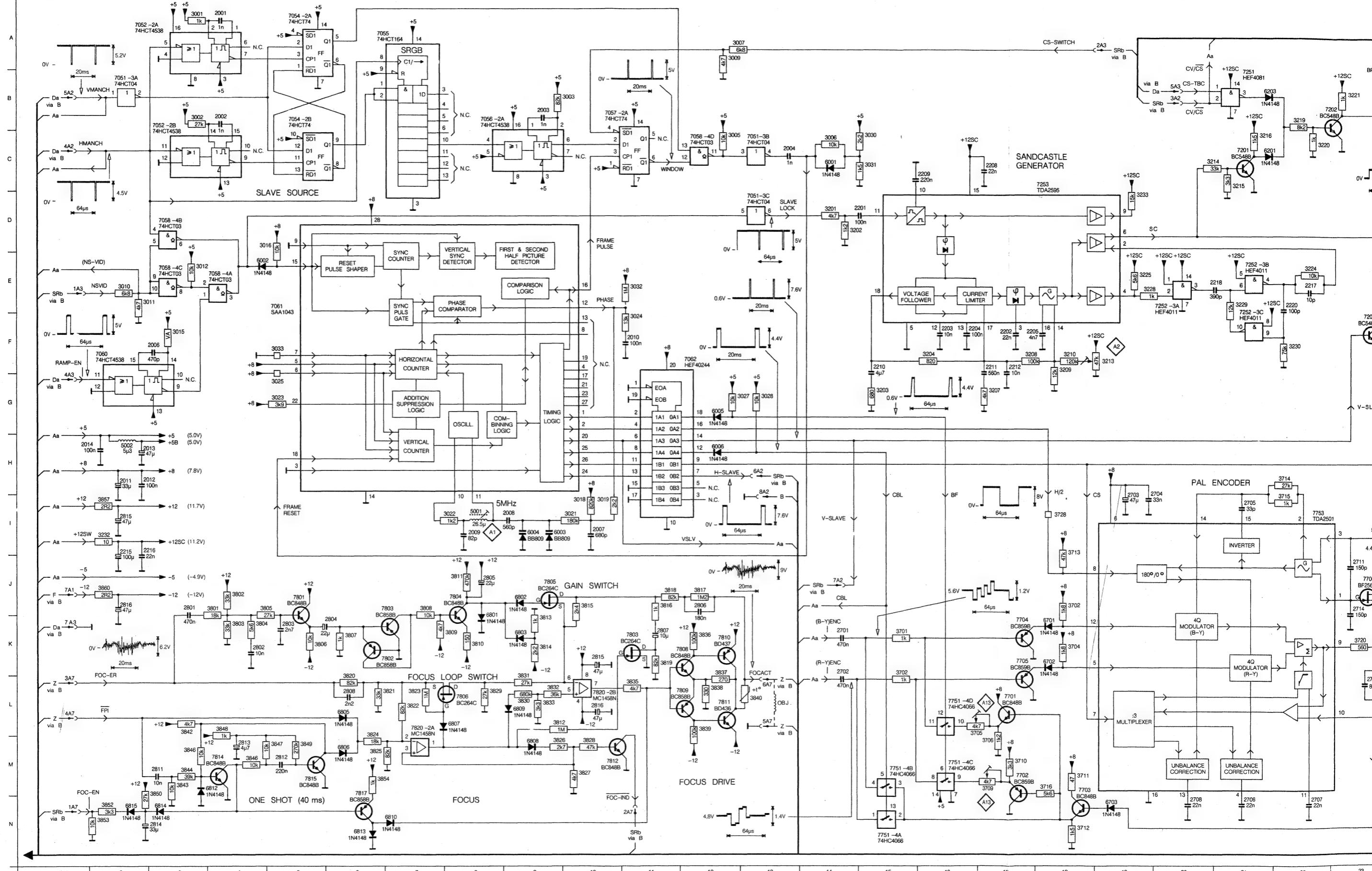
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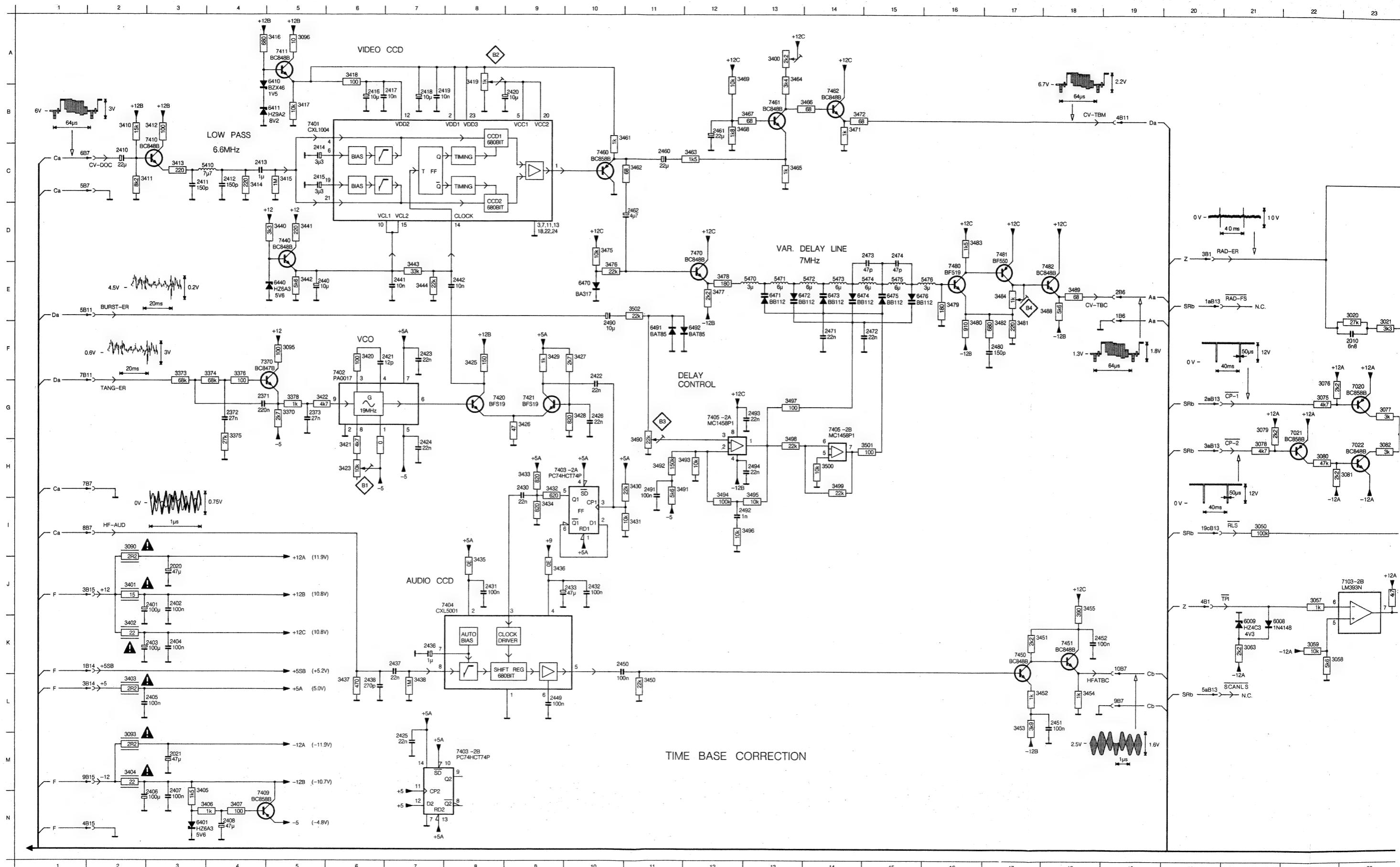
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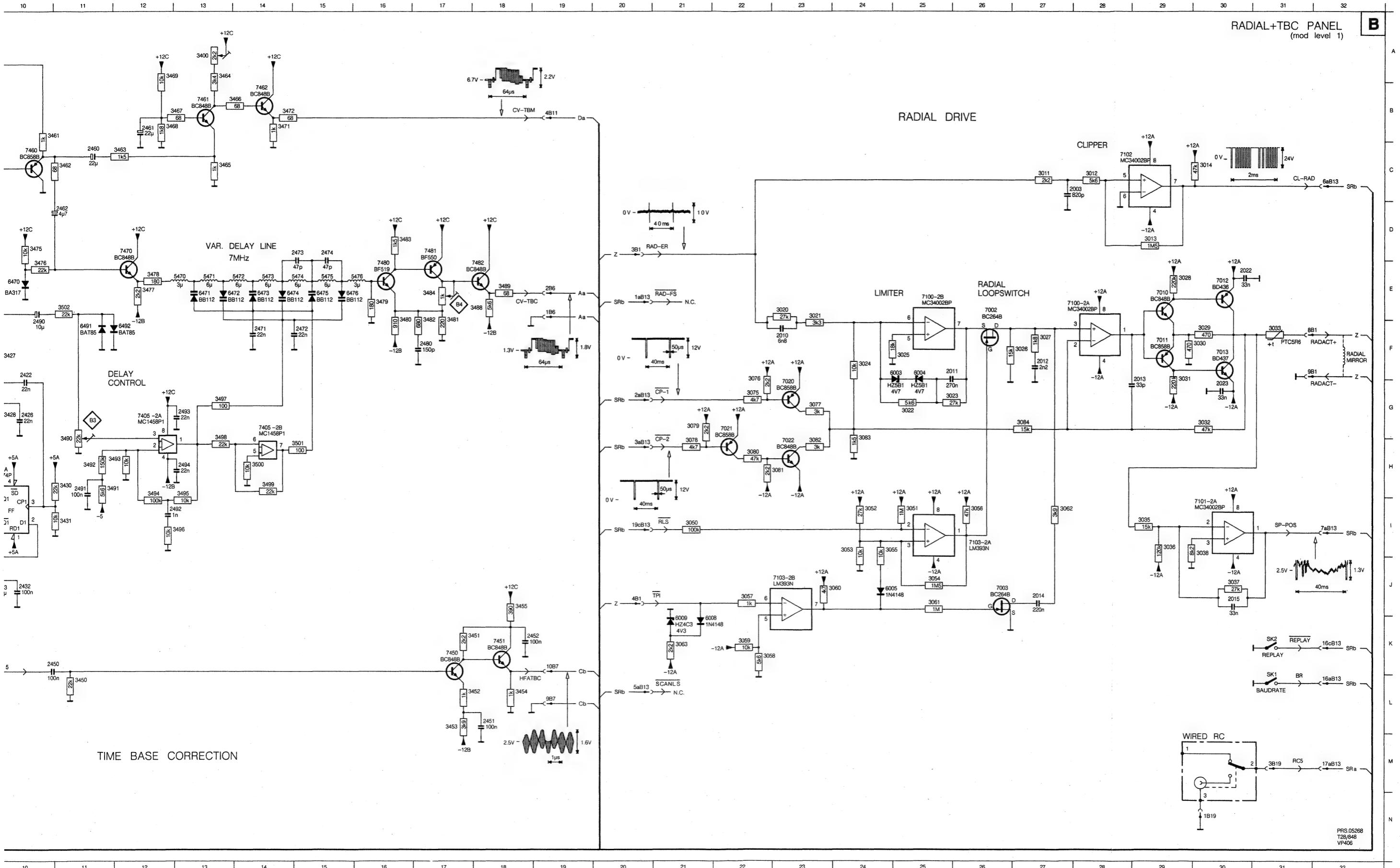


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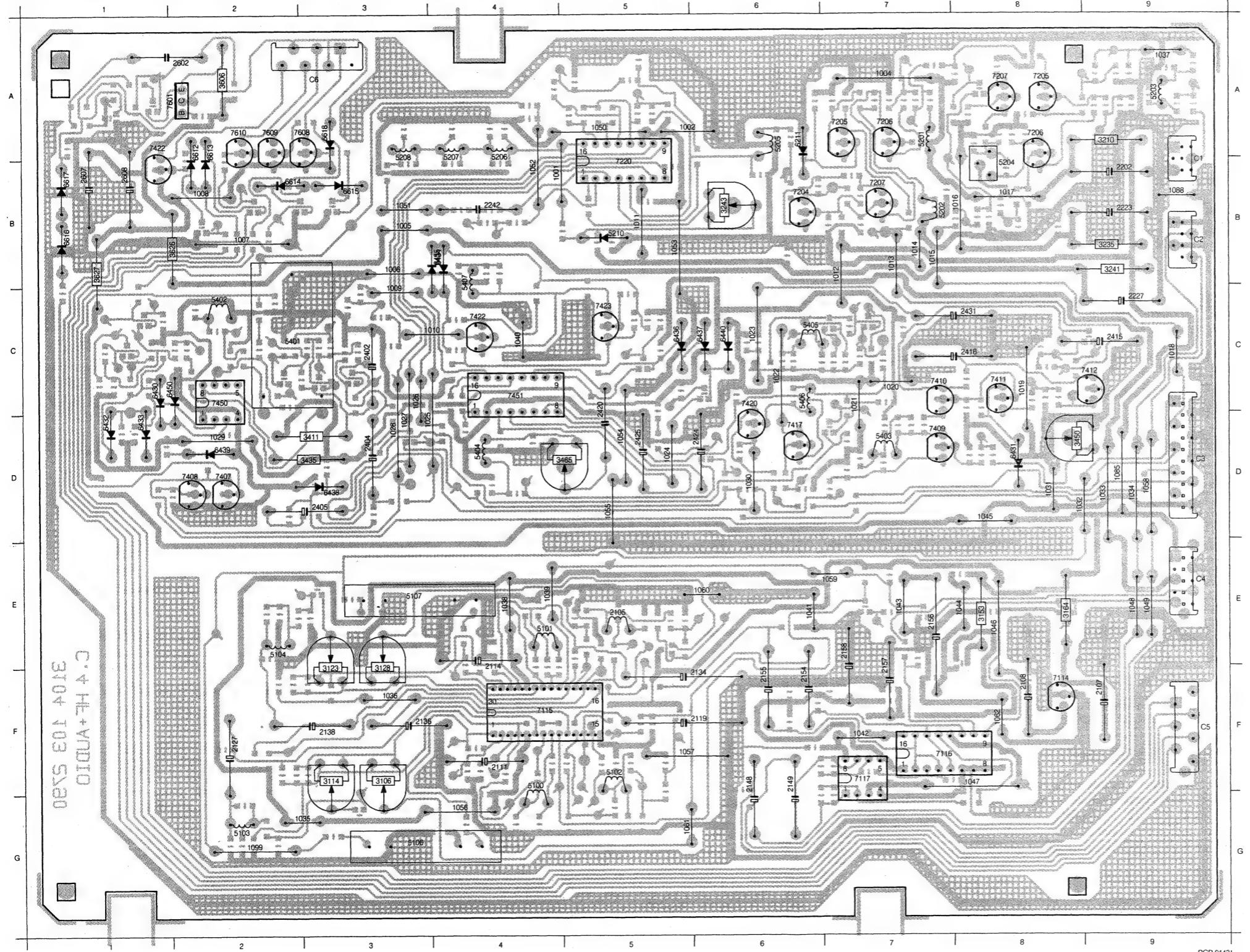


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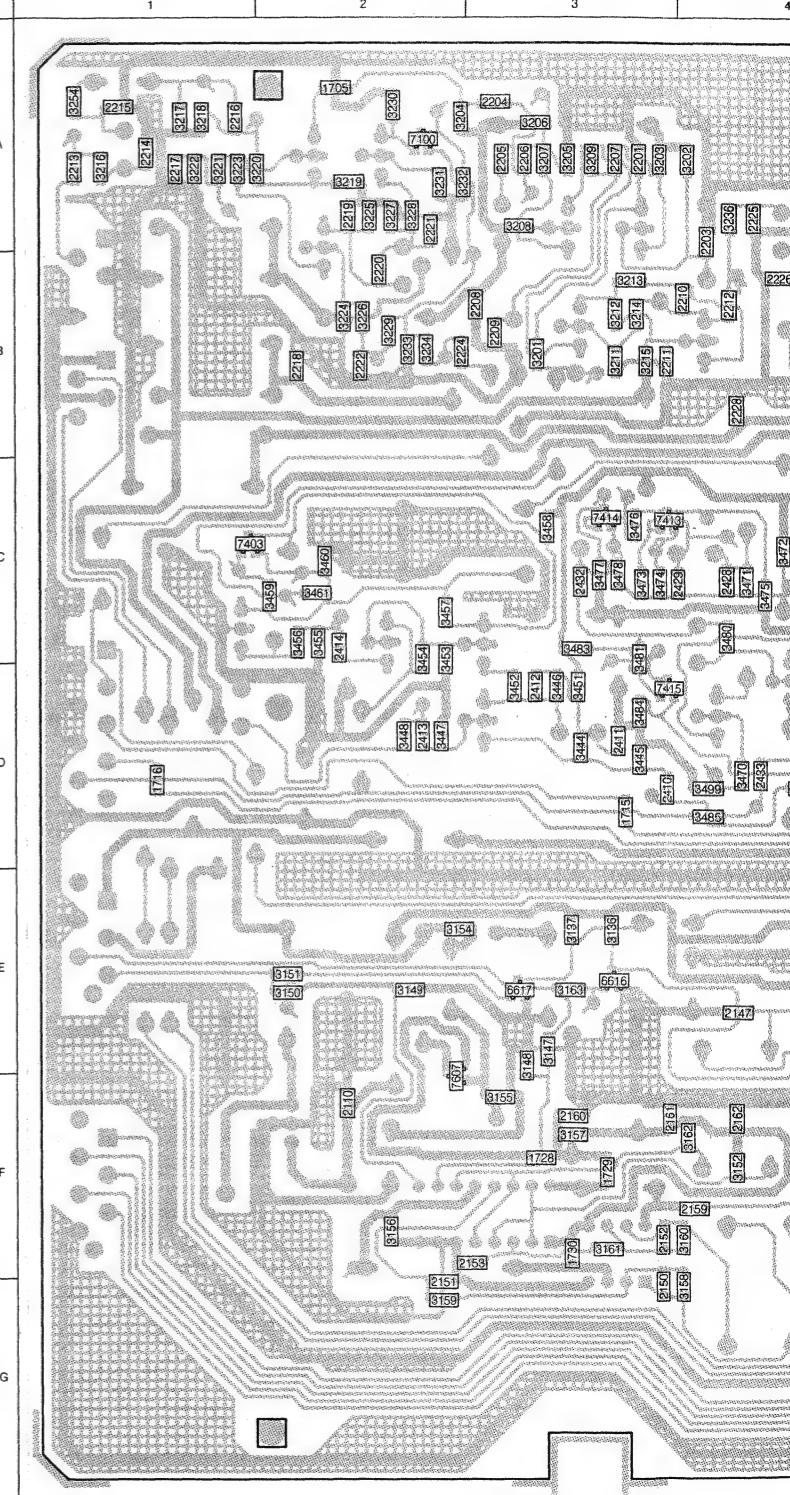
HF+AUDIO PANEL C
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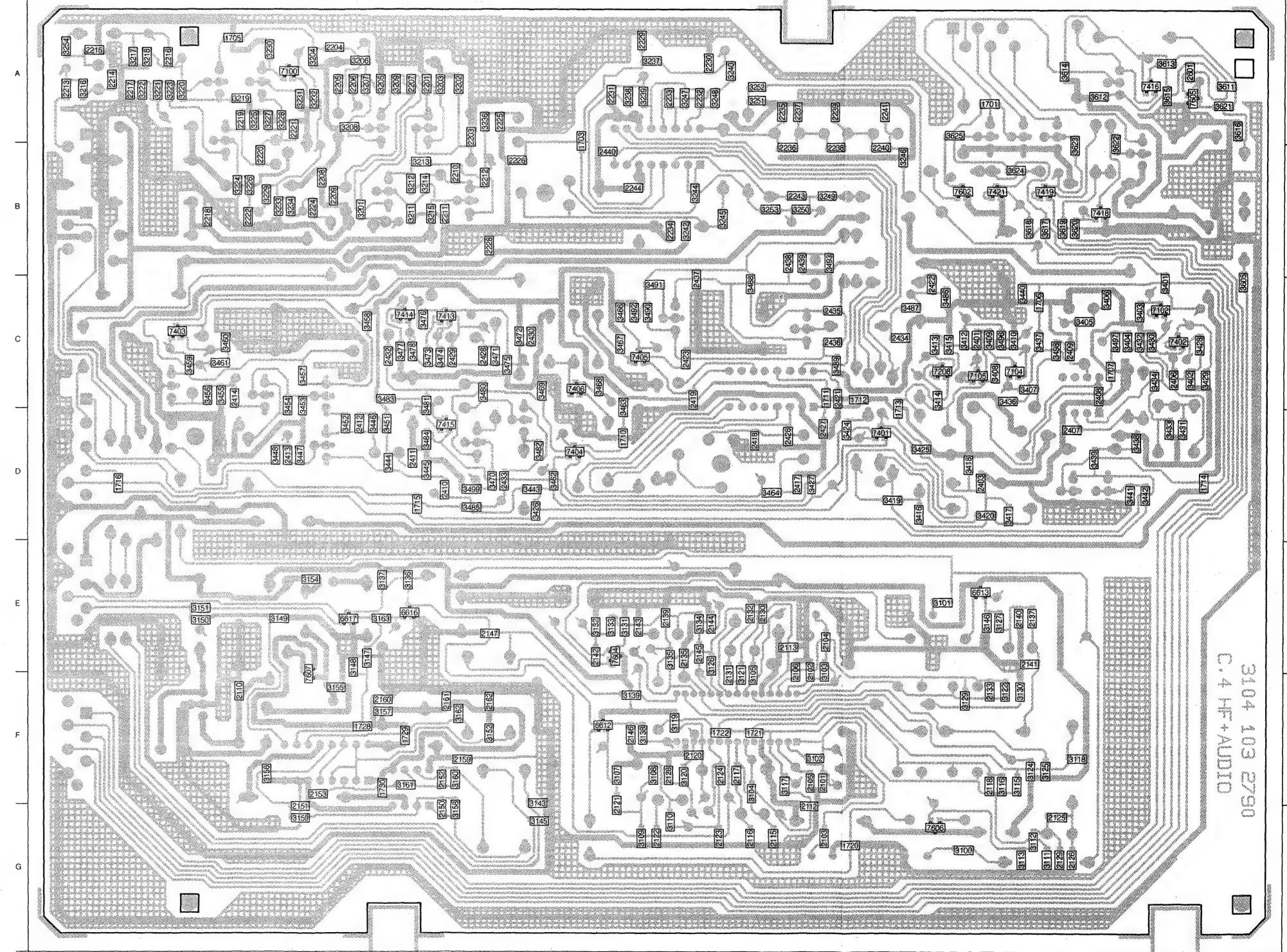
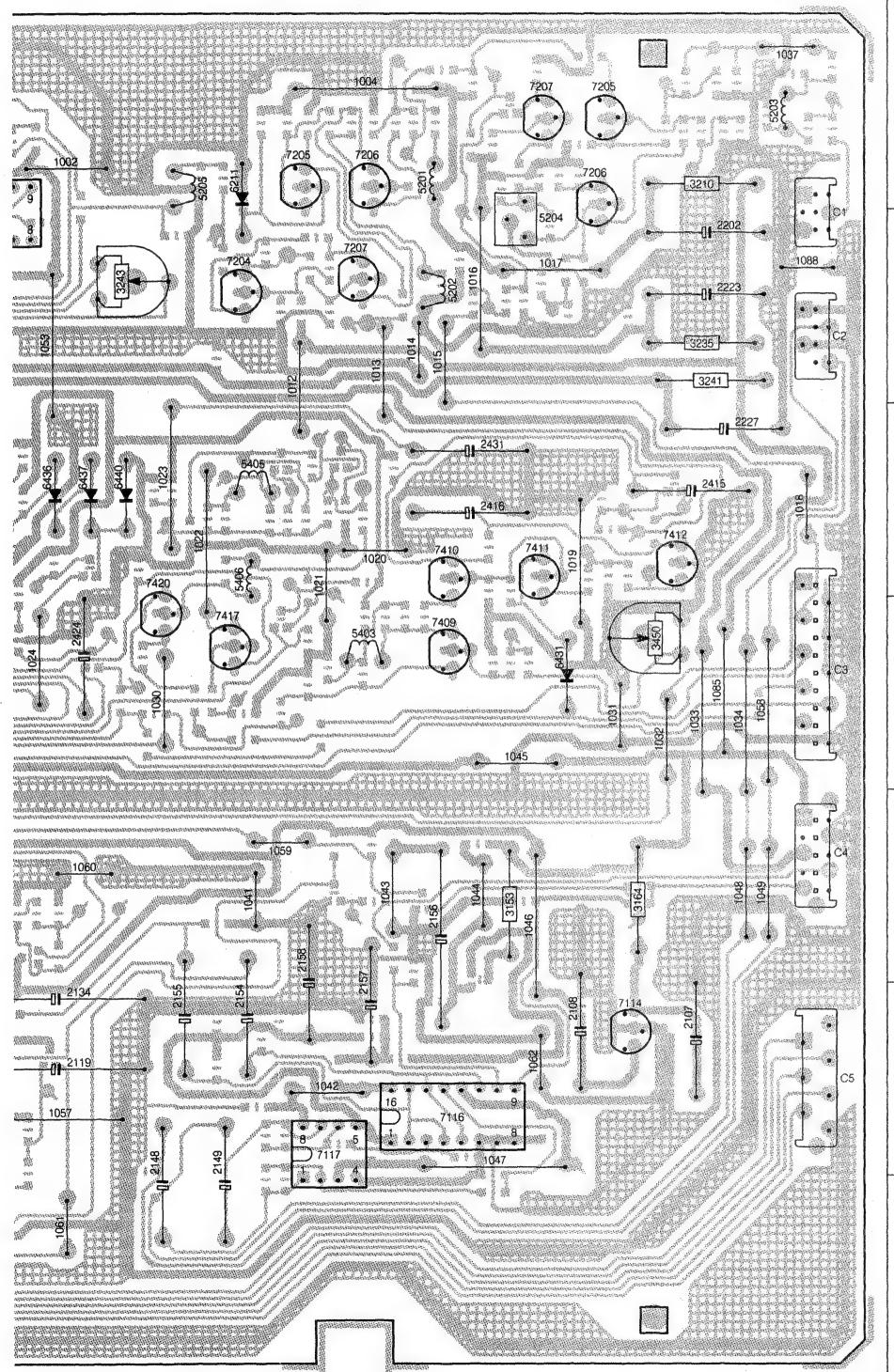
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HF+AUDIO PANEL C
mod level 3

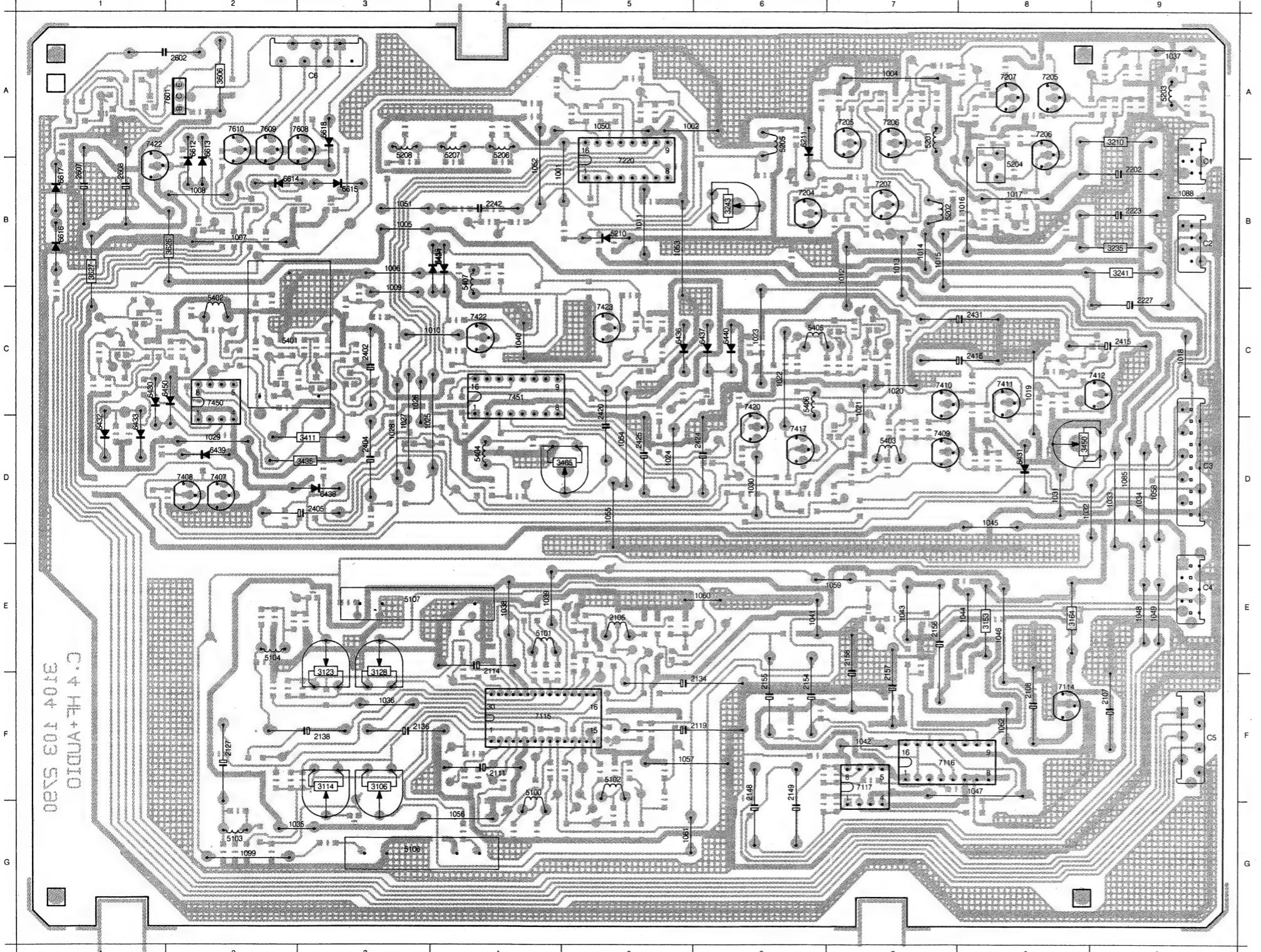
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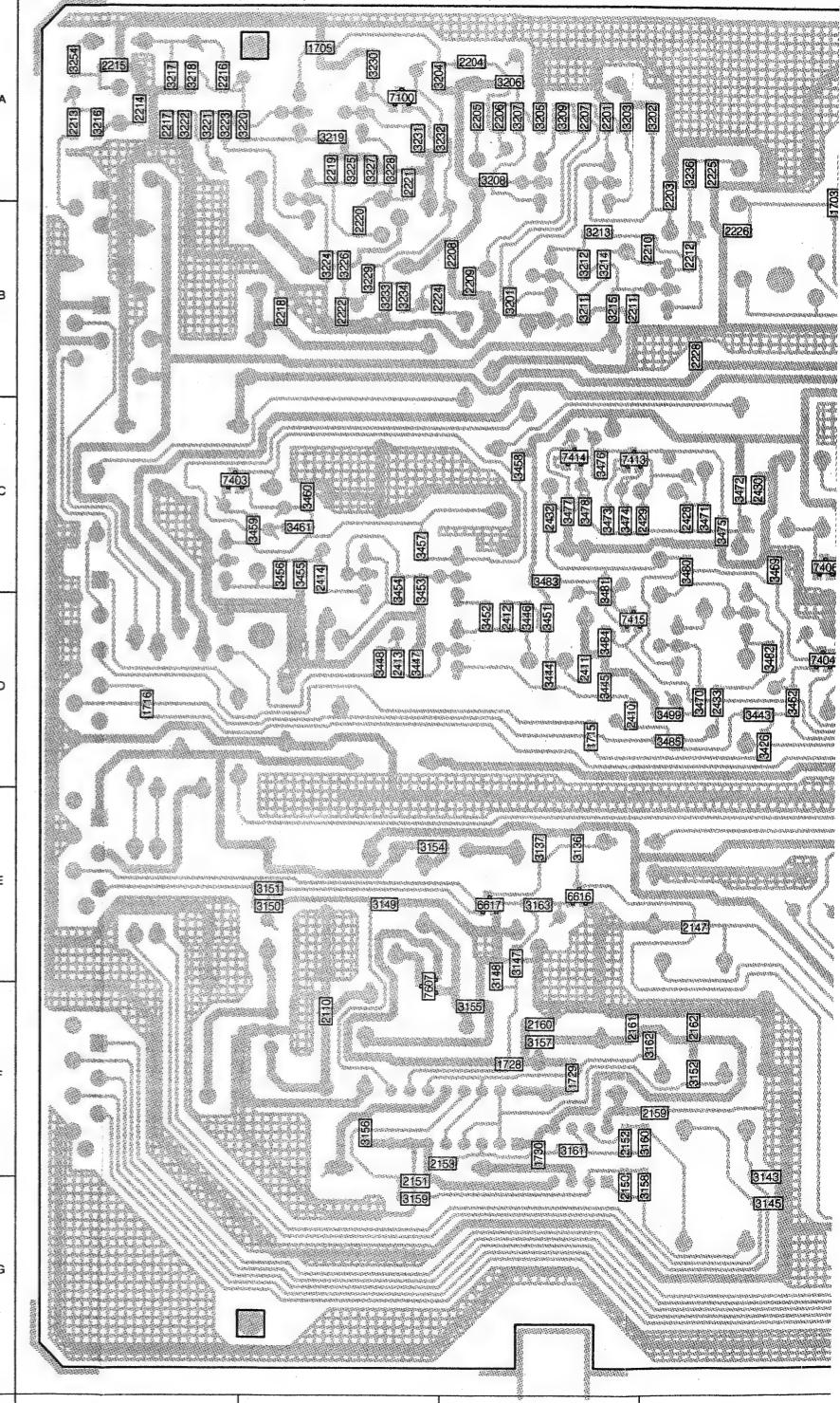
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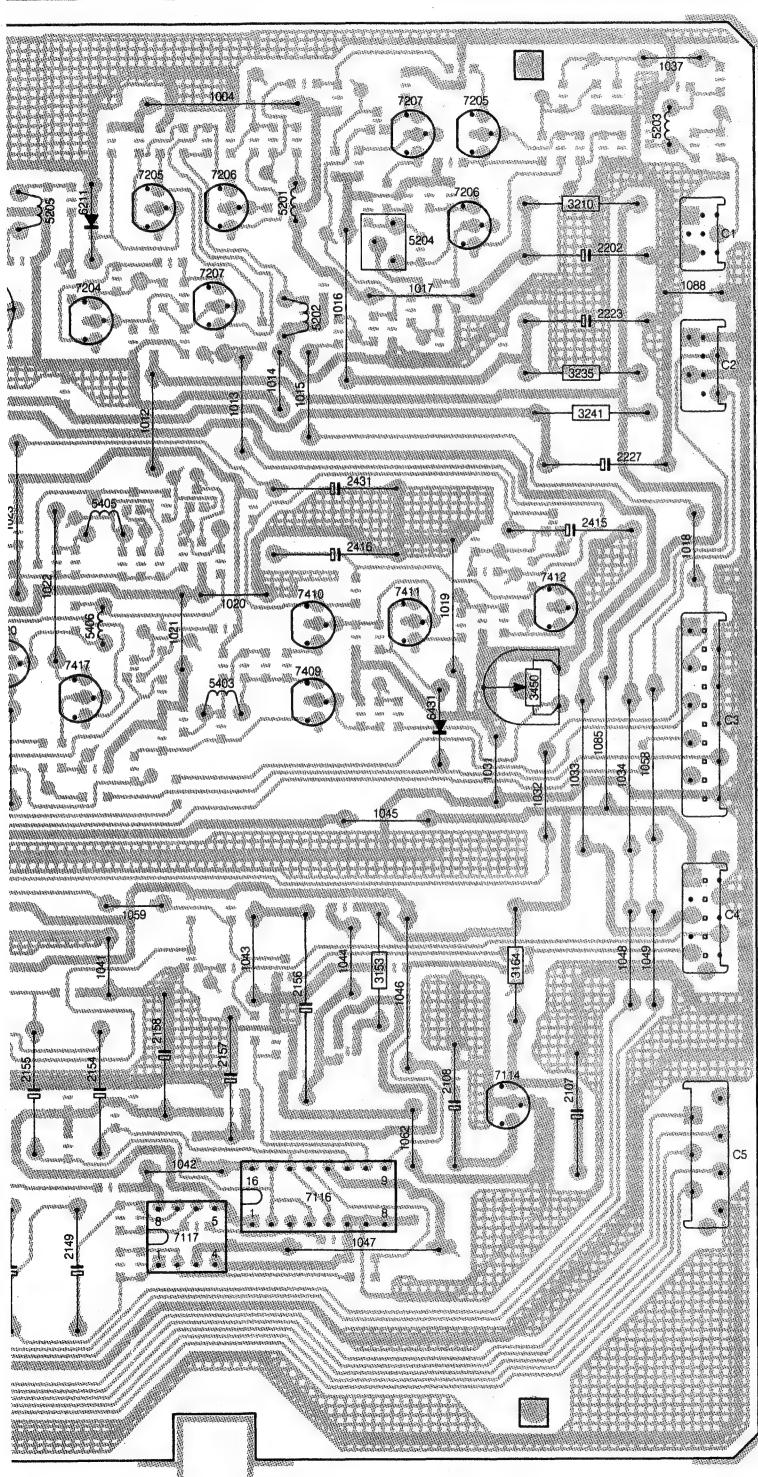
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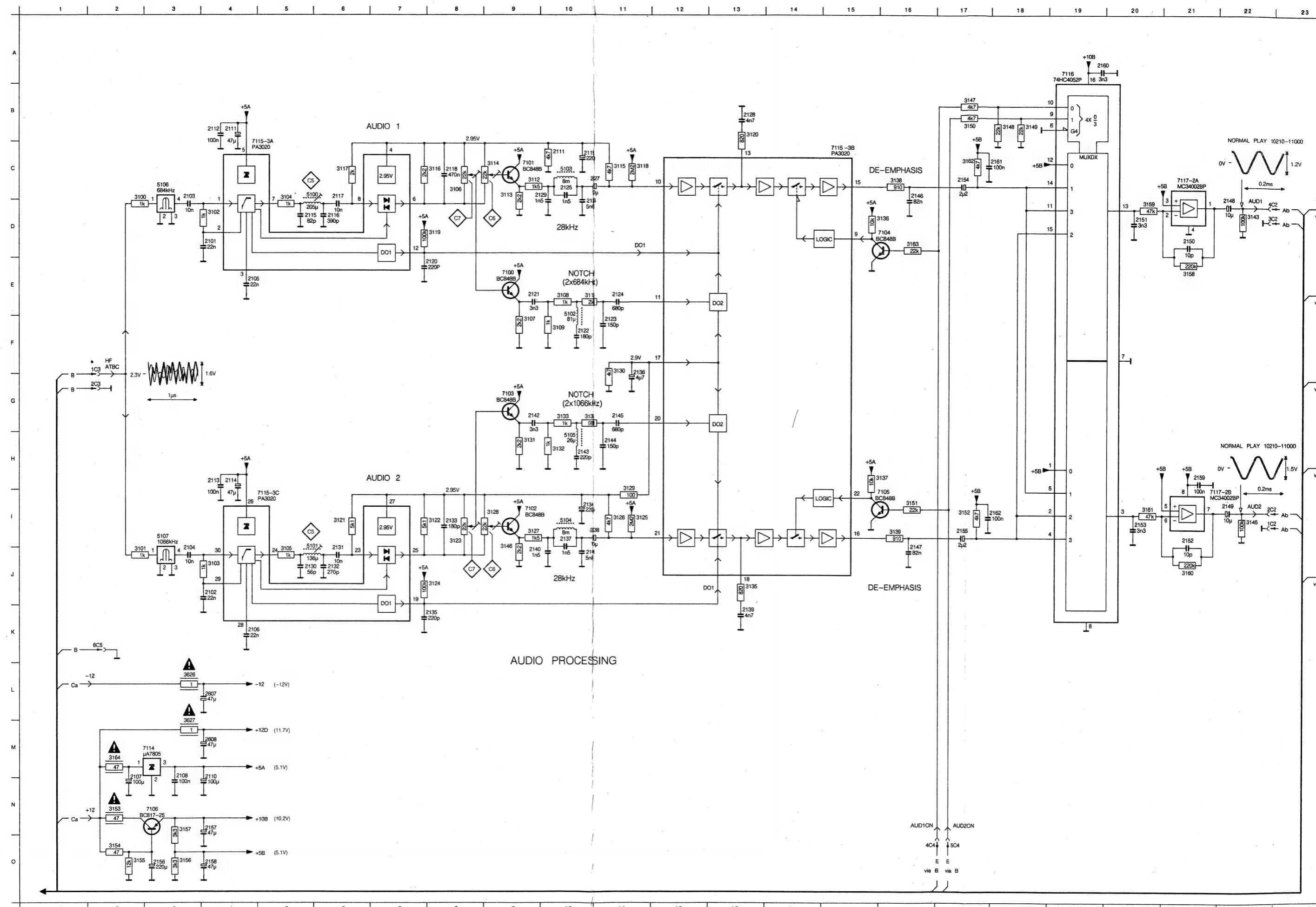


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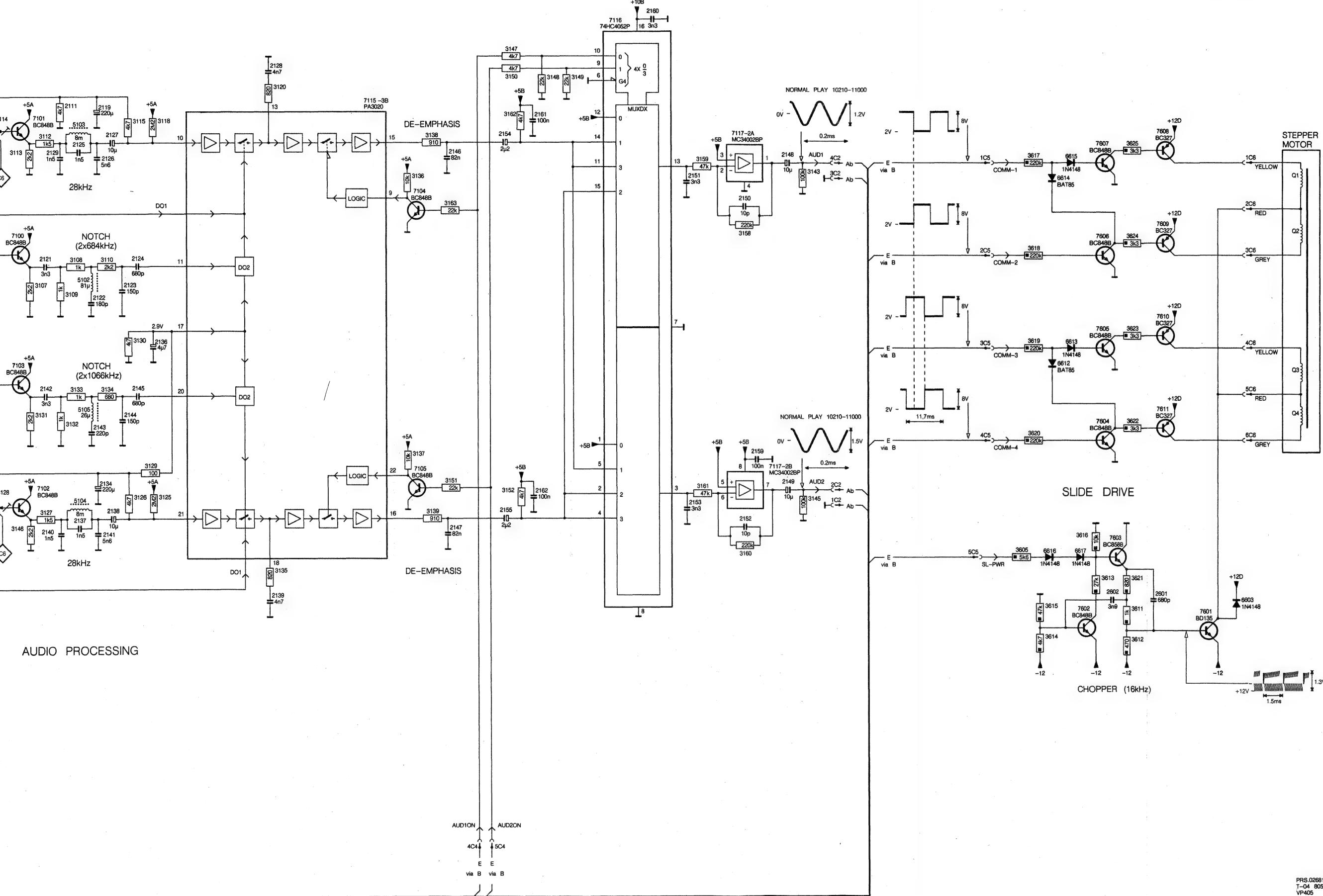
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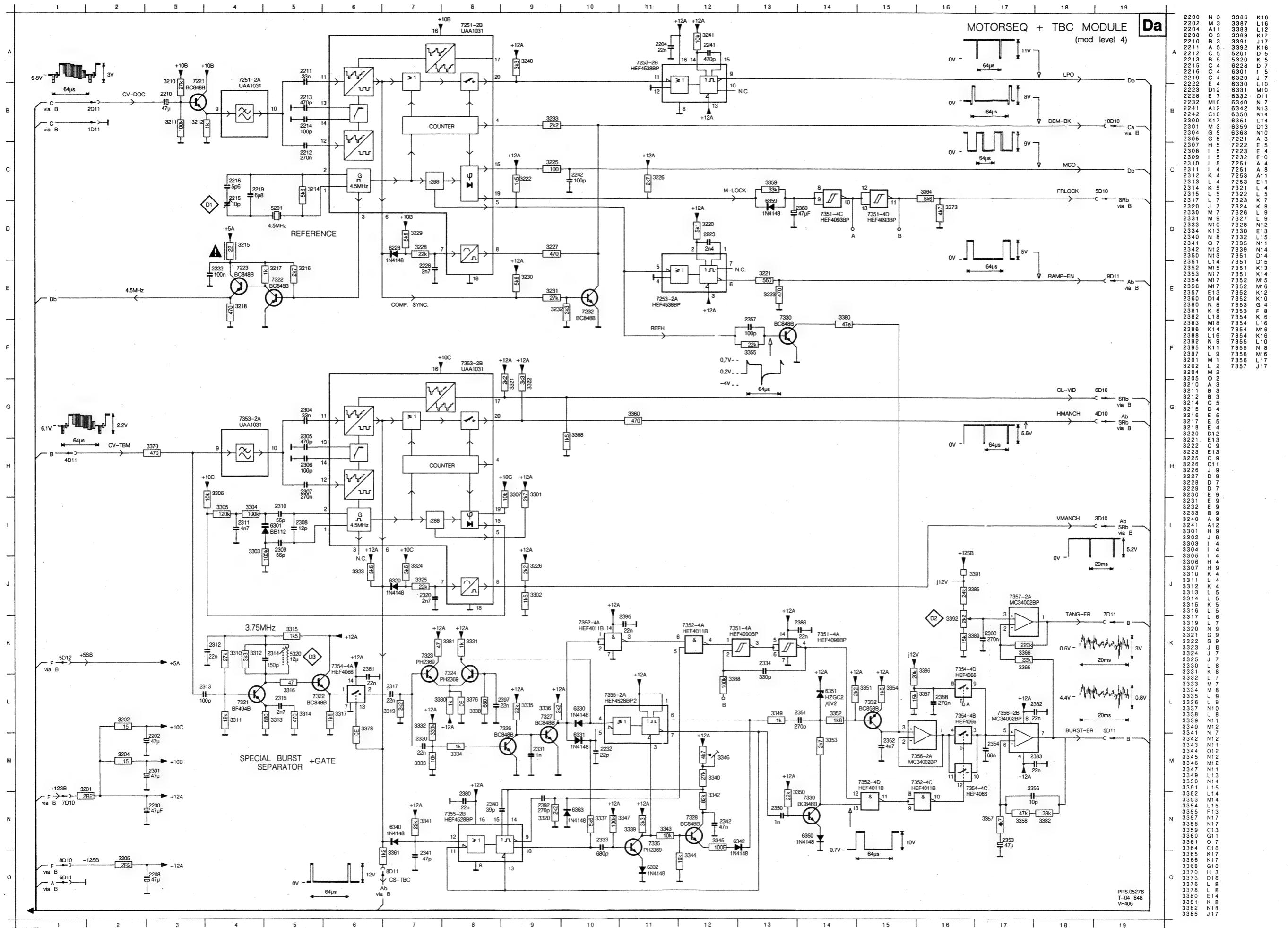


HF + AUDIO PANEL
(MOD LEVEL 3)

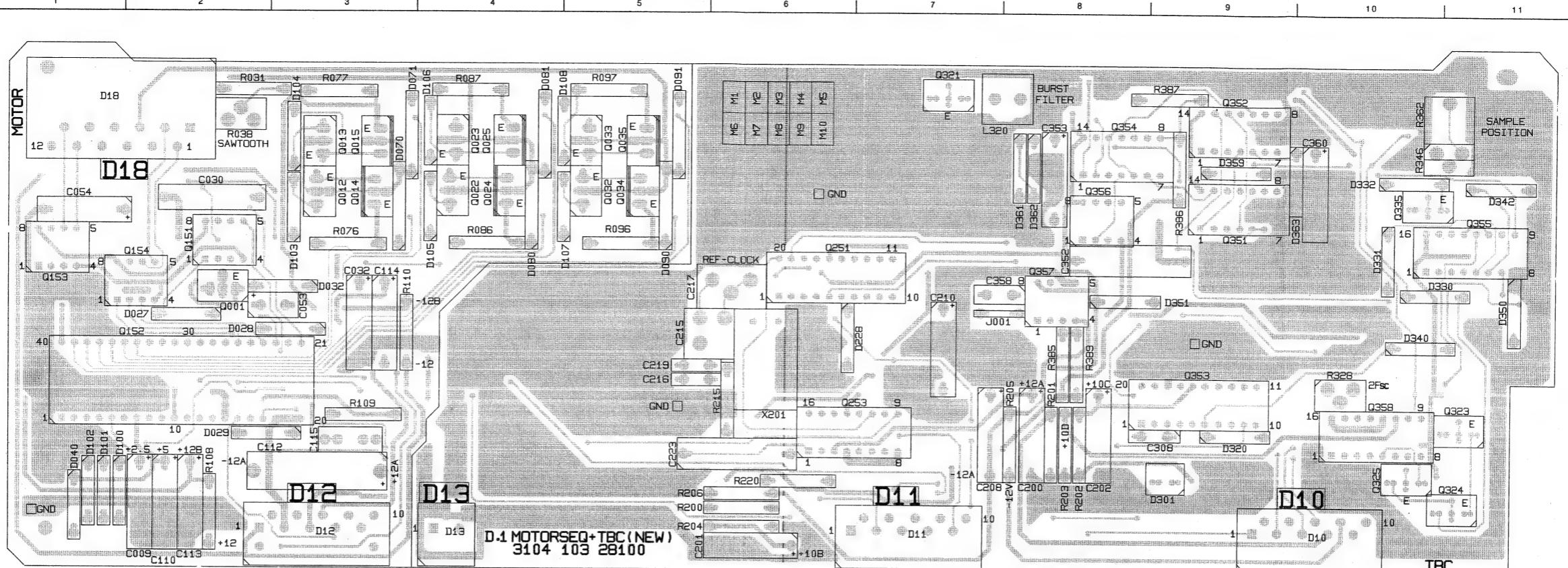
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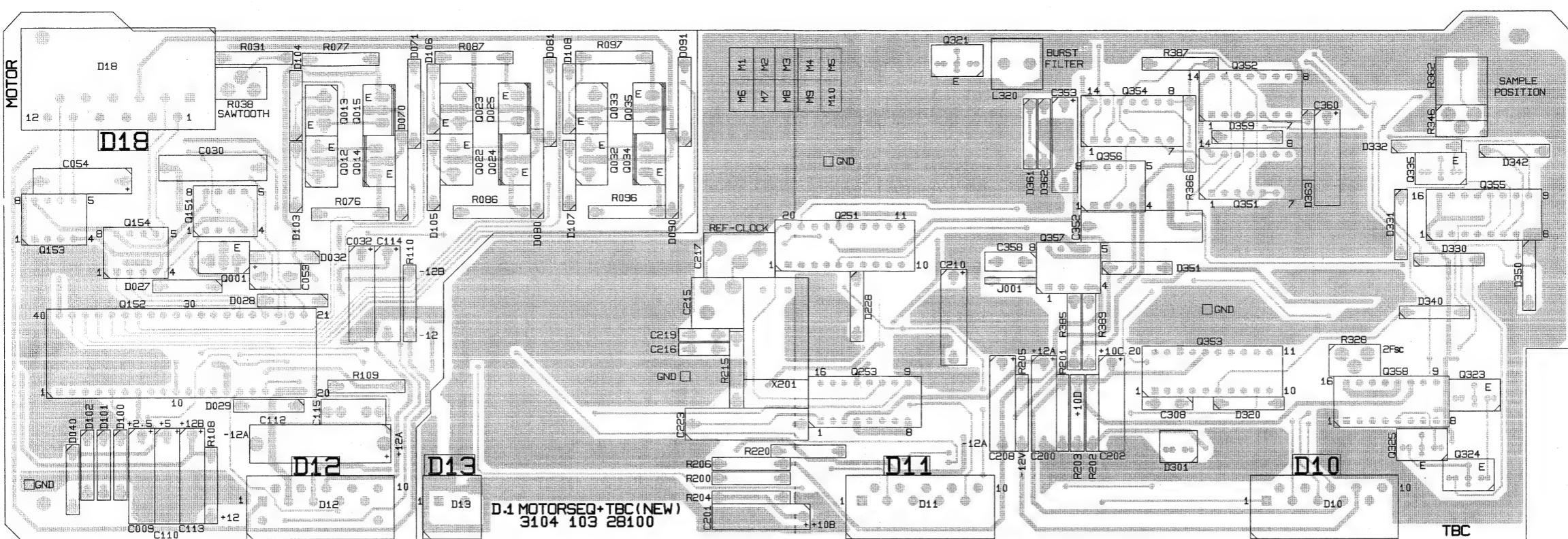
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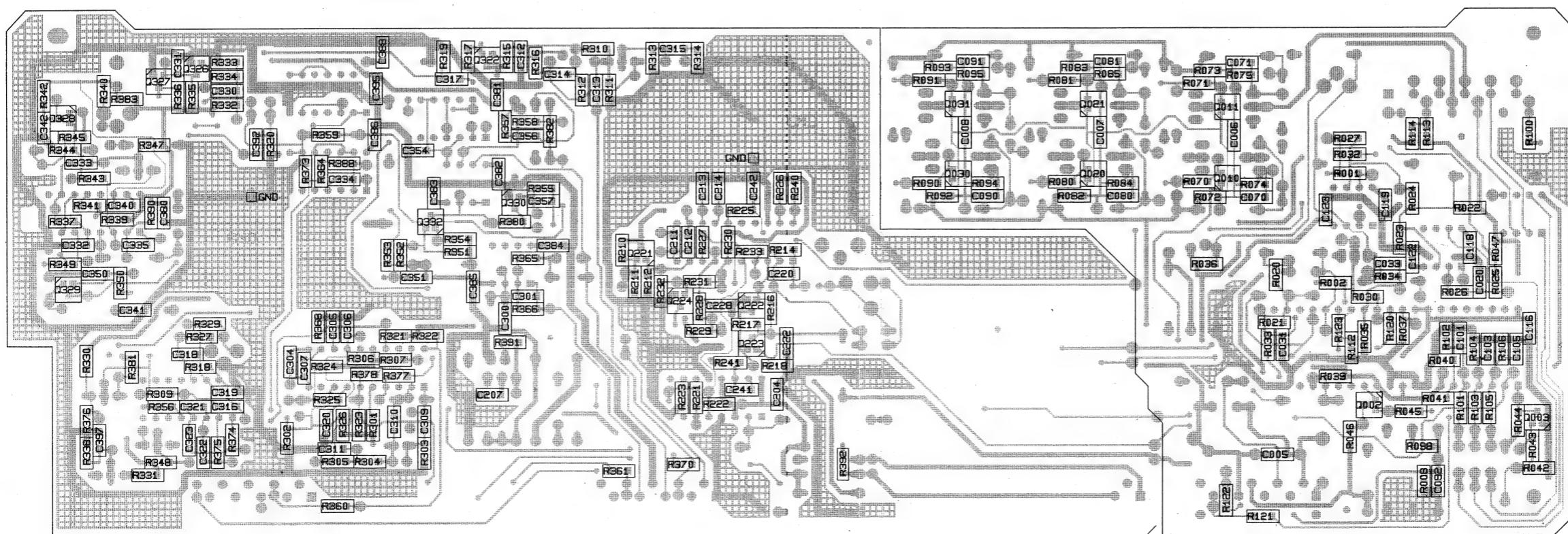
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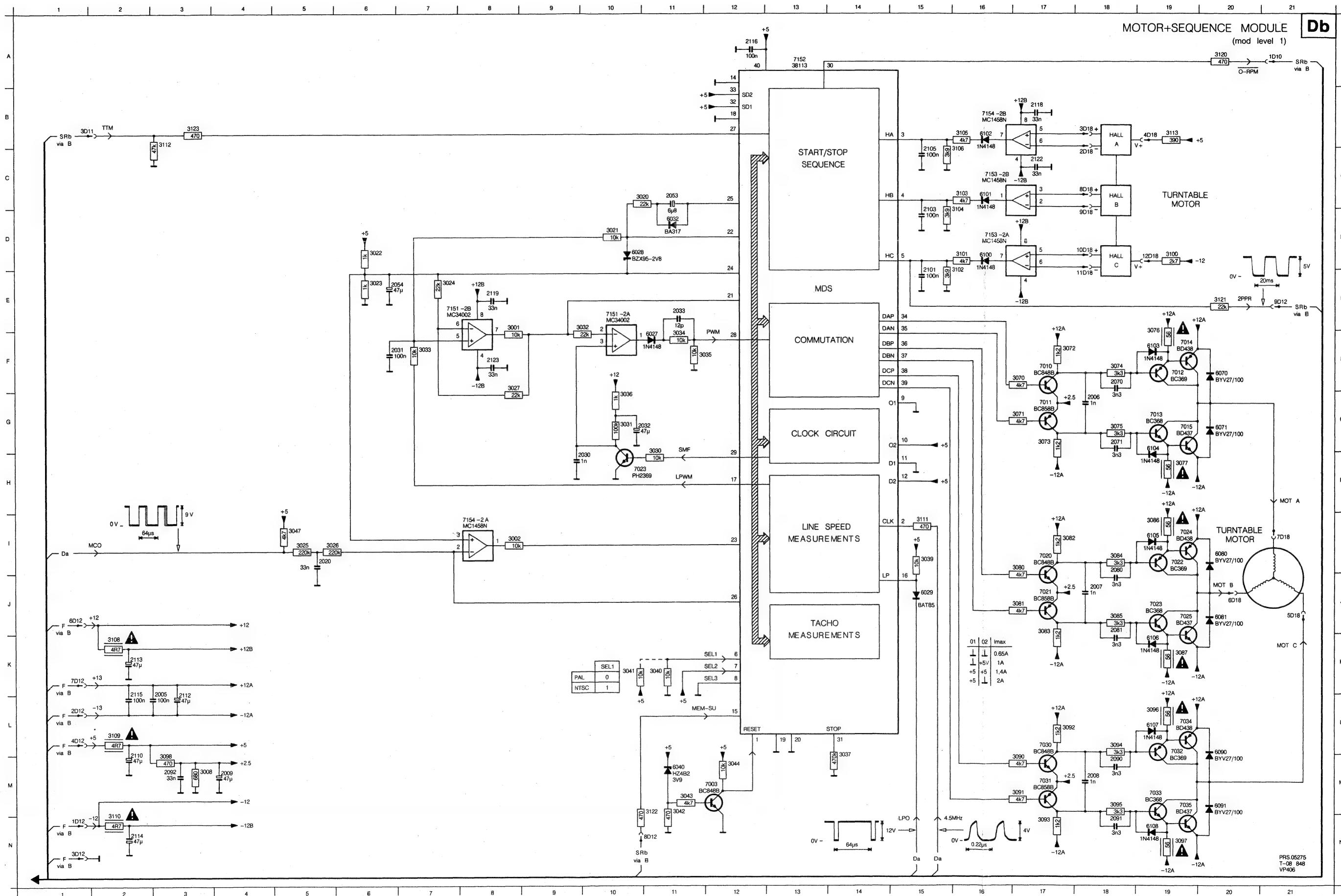
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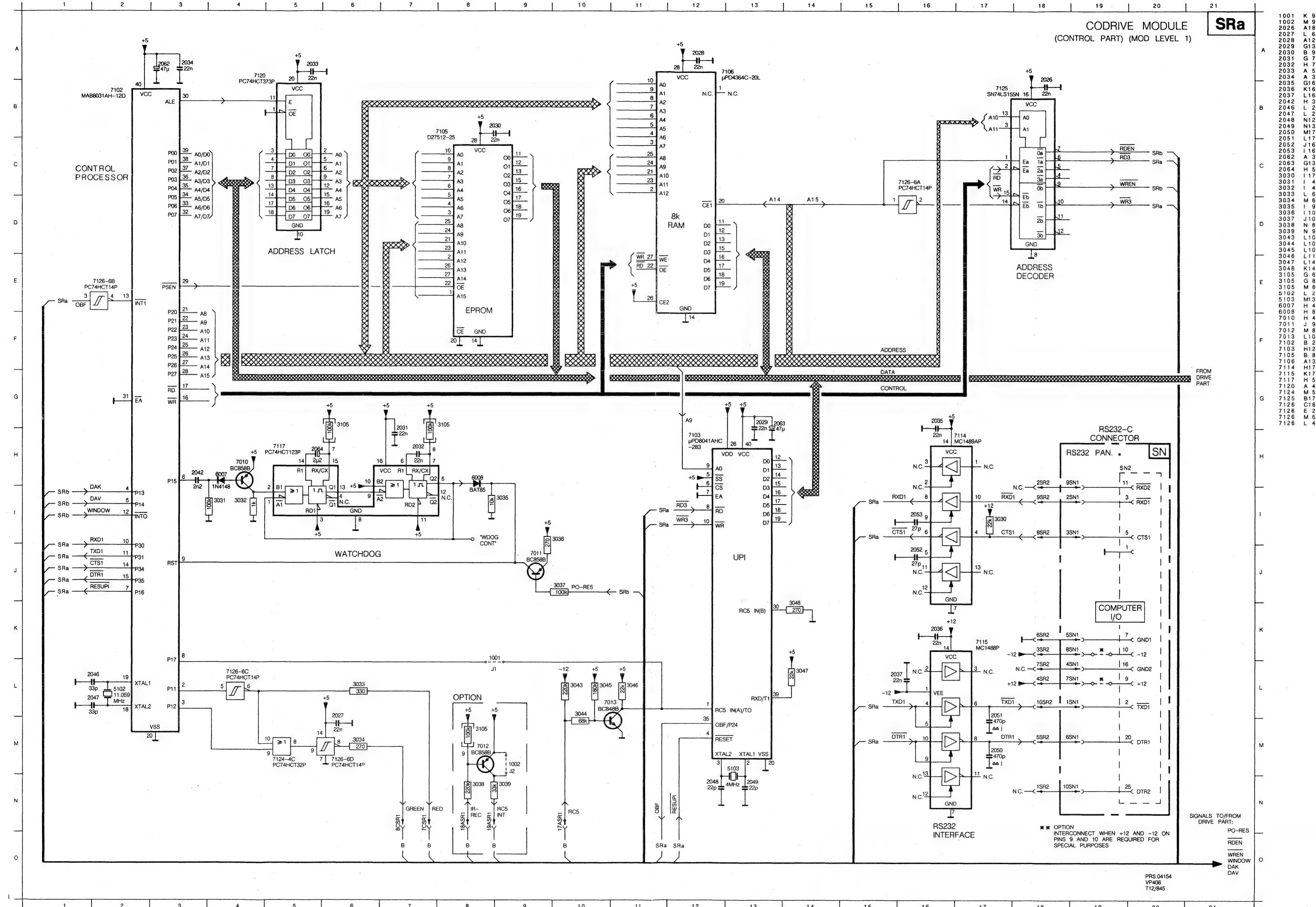


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C008	A 5	D351	B11	R121
C009	D 2	D359	A 9	D 3
C020	B 1	D361	A 8	R122
C030	B 2	D362	A 8	D 3
C031	C 3	D363	A10	R200
C032	C 3	J001	C 8	C 7
C033	B 2	L320	A 8	R202
C053	B 3	M1	A 6	C 8
C054	B 1	M10	A 6	R204
C071	B 3	M2	A 6	D 6
C080	B 4	M3	A 6	R205
C081	A 4	M5	A 6	R210
C090	B 5	M6	A 6	R211
C091	A 5	M7	A 6	B 7
C092	D 1	M8	A 6	R124
C101	C 1	M9	A 6	R215
C103	C 1	Q001	B 2	C 6
C105	C 1	Q002	C 2	R217
C110	D 2	Q003	C 1	C 7
C112	C 3	Q010	B 3	R220
C113	D 3	Q011	A 3	R221
C115	C 3	Q012	B 3	C 7
C116	C 3	Q013	A 3	R223
C118	B 1	Q014	B 3	B 6
C119	B 2	Q015	A 3	R227
C122	B 2	Q021	A 4	B 7
C123	B 2	Q022	B 4	R230
C200	D 8	Q023	A 4	B 7
C201	D 6	Q024	B 4	R231
C202	D 9	Q025	A 4	B 7
C204	C 6	Q030	B 5	R240
C207	C 8	Q031	A 5	R241
C208	D 8	Q032	B 5	R301
C210	C 7	Q033	A 4	C 9
C211	B 7	Q034	B 5	R303
C213	B 7	Q035	A 5	R304
C216	B 6	Q152	B 2	R305
C217	B 6	Q153	B 1	C 9
C218	B 2	Q307	B 2	R309
C219	C 7	Q221	B 7	C 10
C220	B 6	Q222	C 7	R310
C222	C 6	Q223	C 6	A 7
C223	C 5	Q224	C 7	R313
C228	C 7	Q253	C 6	R315
C241	B 6	Q321	A 7	R316
C242	B 6	Q322	A 8	R317
C300	C 8	Q323	C 11	R318
C301	C 8	Q324	D 11	R319
C302	C 9	Q325	C 10	R320
C305	C 9	Q326	A 10	A 9
C306	C 9	Q327	B 9	R322
C307	C 9	Q328	A 11	C 9
C308	C 9	Q329	C 11	R324
C309	C 8	Q330	B 8	R325
C310	C 9	Q332	B 9	C 9
C311	D 9	Q335	A 10	R327
C312	A 8	Q351	B 9	D 10
C313	A 7	Q352	A 9	R328
C314	A 7	Q353	C 9	C 11
C315	A 7	Q354	A 8	R330
C316	C 10	Q355	B 11	D 11
C317	A 7	Q356	B 8	R332
C318	C 10	Q357	B 8	R334
C319	C 9	Q358	A 10	R335
C320	C 9	Q359	A 10	R336
C321	C 10	Q360	B 9	R337
C322	C 10	Q368	B 3	R338
C330	A 10	R021	C 3	R340
C331	A 10	R022	B 2	R341
C332	B 11	R023	B 2	R342
C333	B 11	R024	C 2	R343
C334	B 9	R025	B 1	R344
C335	B 11	R026	C 2	R345
C340	B 11	R027	B 2	R346
C342	C 11	R030	C 2	R347
C350	B 11	R031	A 2	R348
C351	B 9	R033	B 2	R349
C352	B 8	R034	C 2	R350
C353	B 8	R035	B 2	R352
C354	B 9	R036	B 3	R353
C355	B 8	R037	C 2	R354
C357	B 8	R038	A 2	R355
C358	B 8	R039	C 2	R356
C360	B 10	R040	C 2	R357
C380	B 10	R041	D 2	R358
C381	A 8	R042	D 1	R359
C382	B 8	R043	D 1	R360
C383	B 8	R044	C 1	R361
C385	B 8	R045	D 2	R362
C386	A 9	R047	B 1	R363
C388	A 9	R048	B 1	R364
C392	A 9	R071	A 3	R368
C395	A 9	R072	B 3	R370
C397	C 11	R073	A 3	R373
D027	B 2	R074	B 3	C 10
D028	C 3	R075	A 3	R375
D029	C 3	R076	C 3	R376
D032	B 2	R077	A 3	R377
D040	D 1	R080	B 4	C 9
D070	B 4	R081	A 4	R380
D080	B 4	R082	B 4	R381
D081	A 5	R083	A 4	R382
D090	B 5	R084	A 4	A 11
D091	A 6	R085	B 4	R385
D100	D 1	R090	B 5	R388
D101	D 1	R091	A 5	C 8
D102	D 1	R092	B 5	R390
D103	B 2	R093	A 5	B 10
D104	A 3	R094	B 5	R391
D105	B 3	R095	A 5	C 6
D106	A 4	R096	B 5	X201
D107	B 4	R097	A 5	C 6
D108	D 1	R098	D 2	C 6
D12	D 3	R100	A 1	C 1
D13	D 4	R102	C 1	C 1
D18	A 1	R103	C 1	C 1
D228	C 6	R104	C 1	C 1
D301	D 6	R105	C 1	C 1
D320	C 9	R106	C 1	C 1
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D331	B 10	R109	C 3	C 1
D332	B 10	R110	C 4	C 1



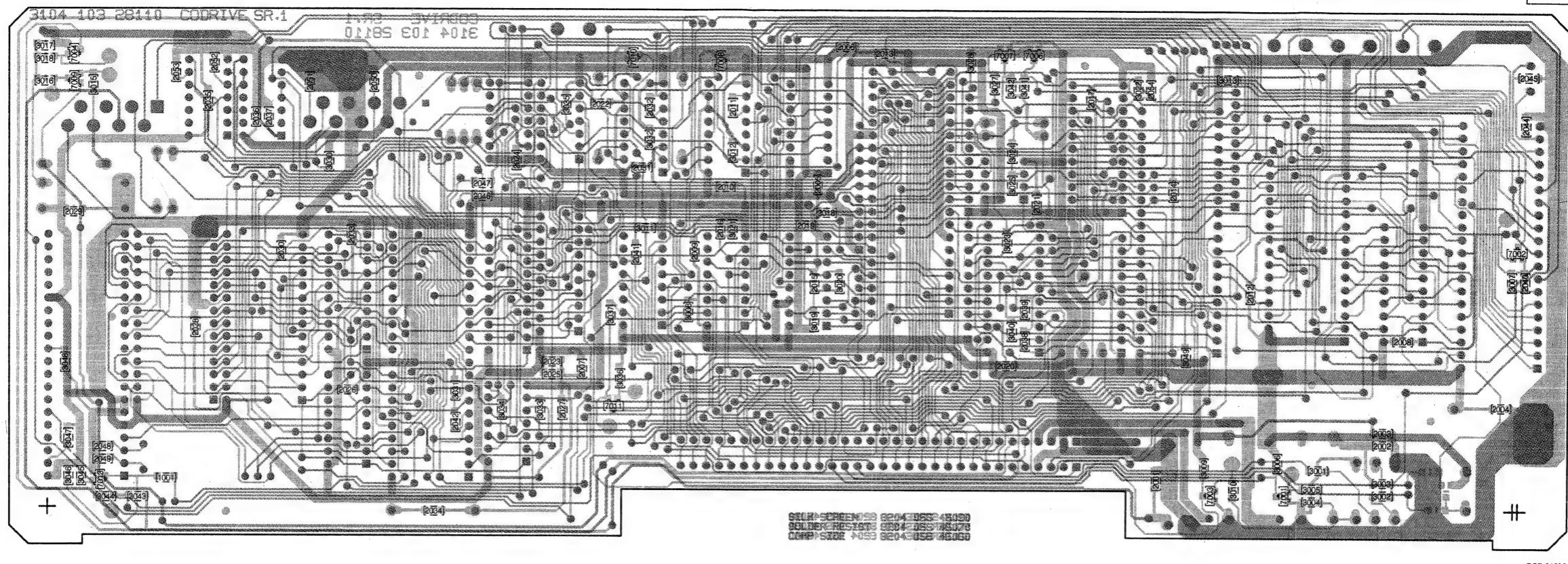
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2006	G18	2031	F	2071	G16	2101	E15	2114	N 2	2123	F 8	3022	D 6	3030	G10	3043	M1 1	3073	G17	3081	J17	3087	K19	3095	M18	3102	E16	3109	L 2	3121	E20	6032	D11	6090	L20	6104	G19	7010	F17	7020	J 17	7025	J 19	7035	M19	7154	I 8		
2007	I 19	2032	C11	2080	I 18	2103	D16	2115	K 2	2001	E 6	3023	E 7	3031	G10	3037	M1 2	3044	M1 2	3074	F18	3082	I 17	3090	M17	3096	L19	3103	C16	3110	M 2	3122	M11	6040	M11	6091	M20	6105	I 19	7011	G17	7021	J 17	7025	J 19	7030	L17	7151	E 7
2008	M18	2033	E11	2081	J18	2105	C15	2116	A12	3002	I 8	3024	E 7	3032	E10	3039	I 15	3047	I 5	3075	G18	3083	J17	3091	M17	3097	N19	3104	D16	3111	I 15	3123	B 3	6070	F20	6100	I 19	6106	K19	7012	F19	7022	I 19	7031	M17	7152	A13		
2009	M 4	2053	C11	2090	M18	2110	L 2	2118	B17	3008	M 3	3025	I 5	3033	F 7	3040	K11	3070	F17	3076	F19	3084	I 18	3092	L 3	3105	B16	3112	B 3	6027	F11	6071	G20	6101	C16	6107	L19	7013	G19	7023	J19	7032	L19	7153	M19	7154	C16		
2020	I 5	2054	E 7	2091	N18	2112	K 3	2119	E 8	3020	C11	3026	I 5	3034	F11	3041	K10	3071	G17	3077	H19	3085	J18	3093	N17	3100	D19	3113	B19	6028	D10	6080	I 20	6102	B16	6108	N19	7014	F19	7023	H10	7033	H10	7153	C16				



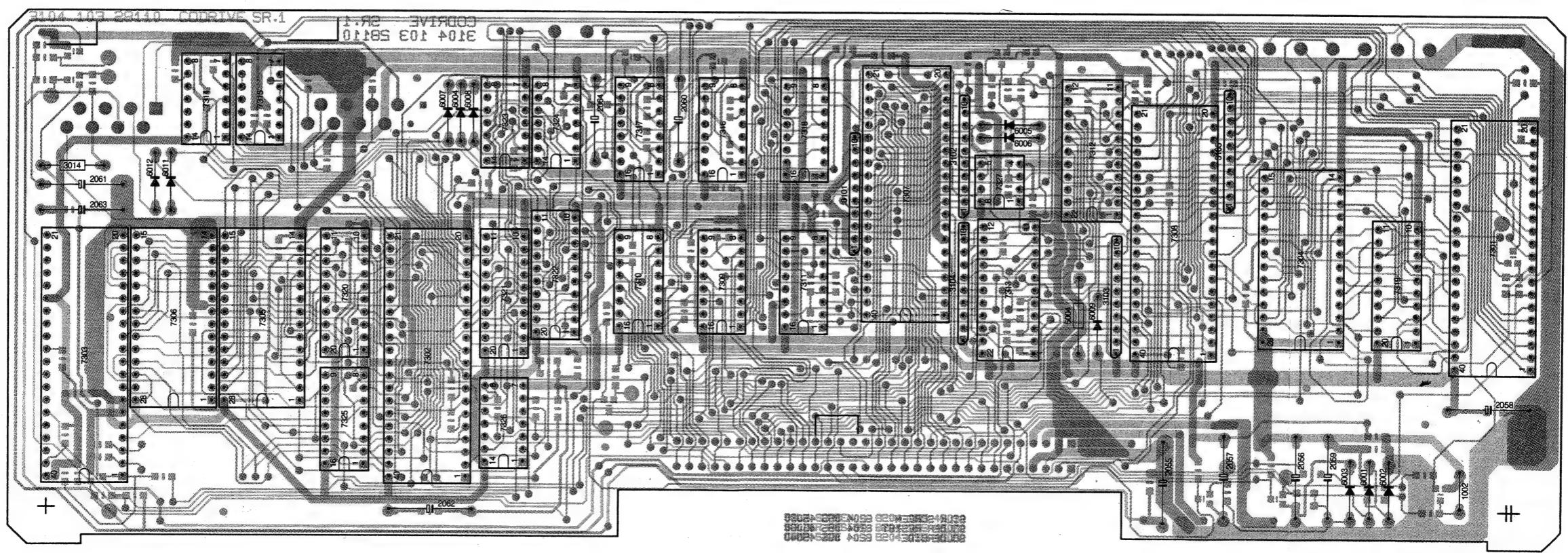


CODRIVE MODULE

SR



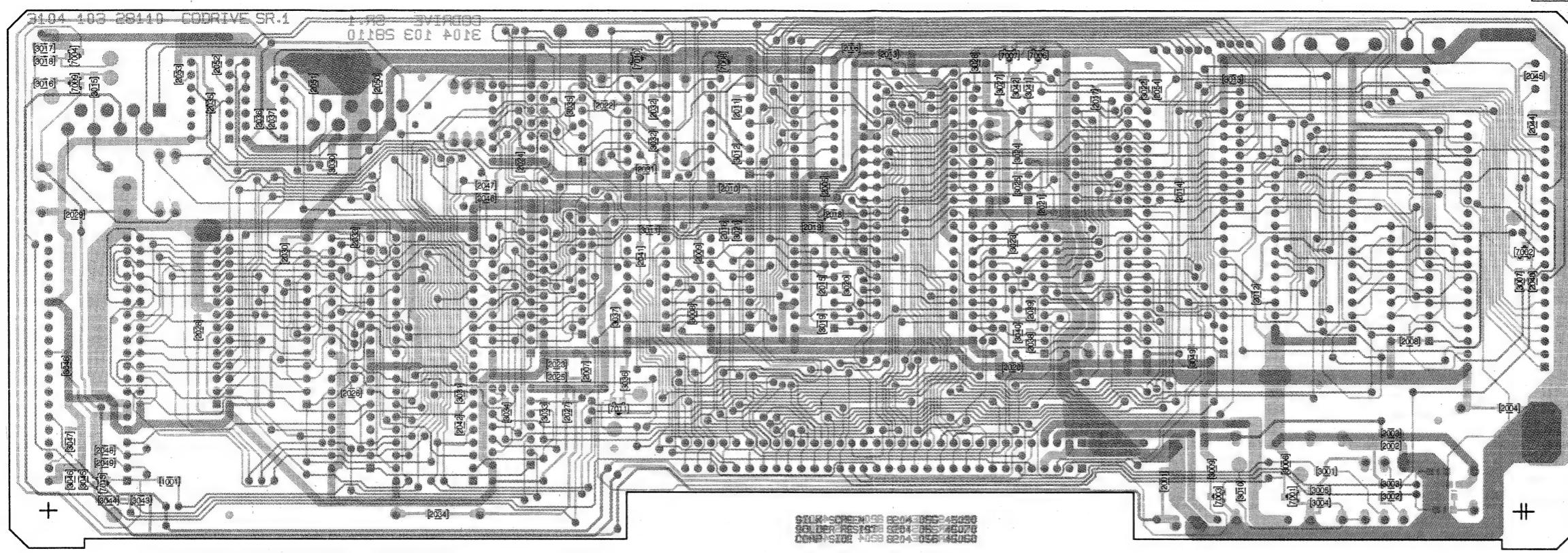
PCB.01296
TH 848



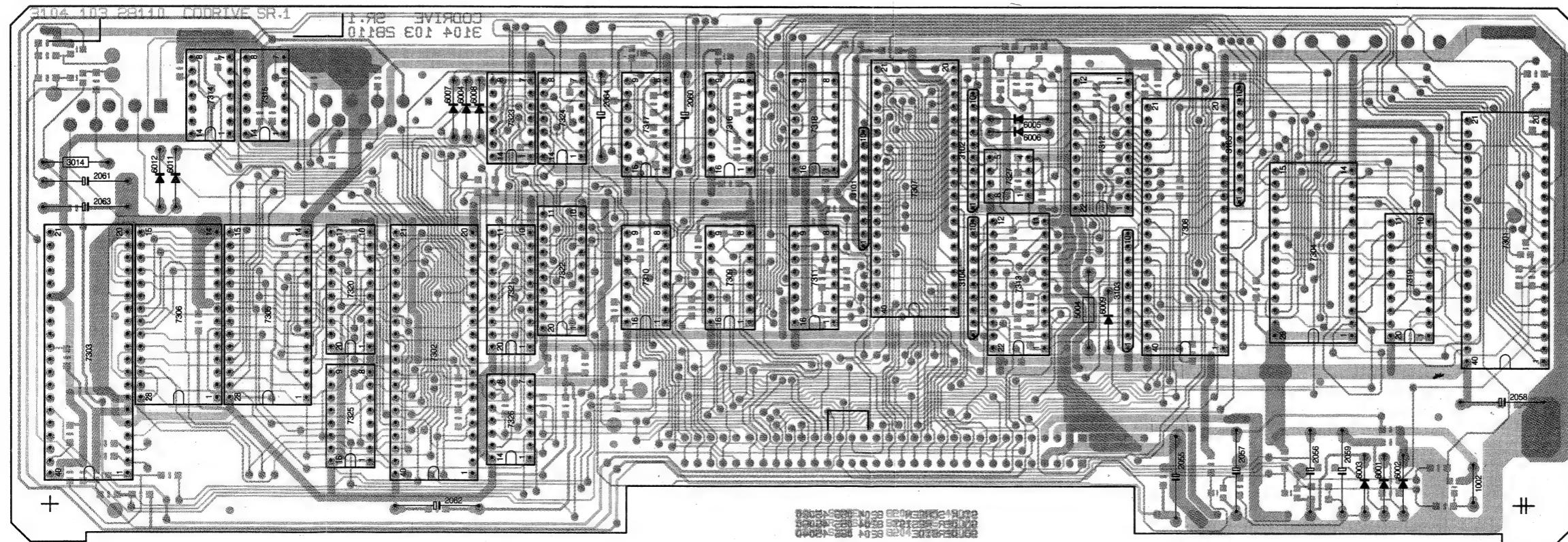
PCB.01295
TH 848

CODRIVE MODULE

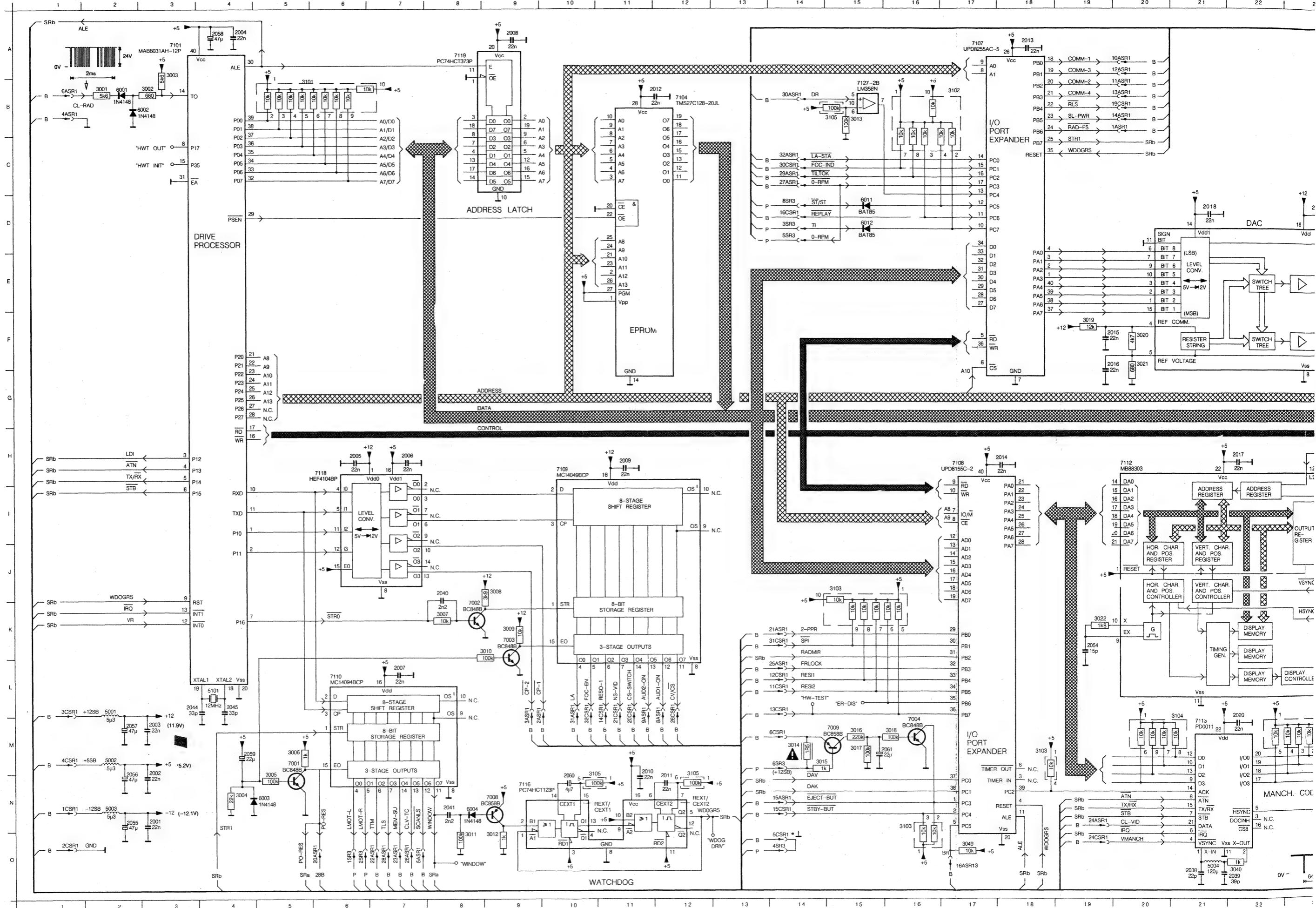
SR



PCB.01296
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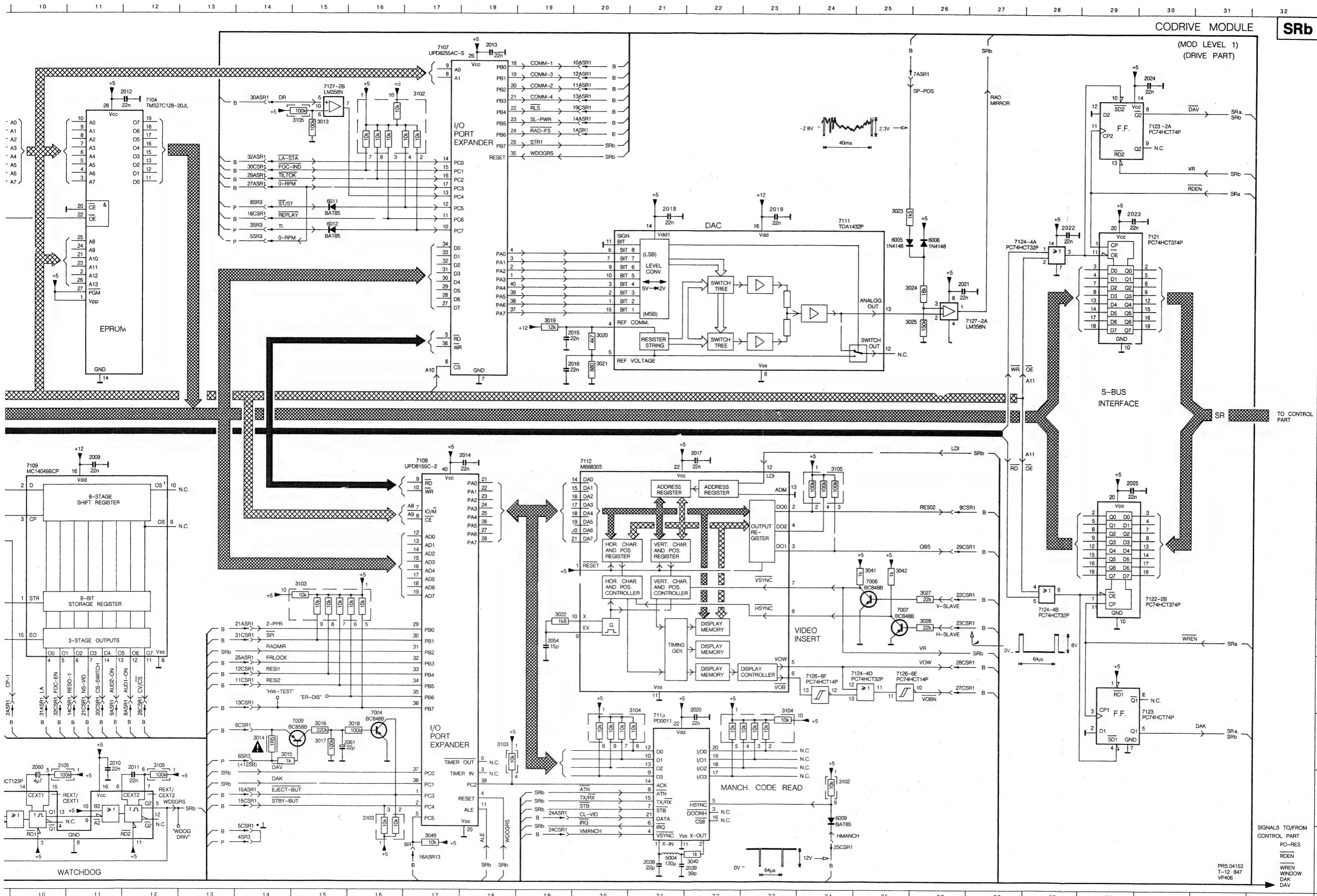
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SRb

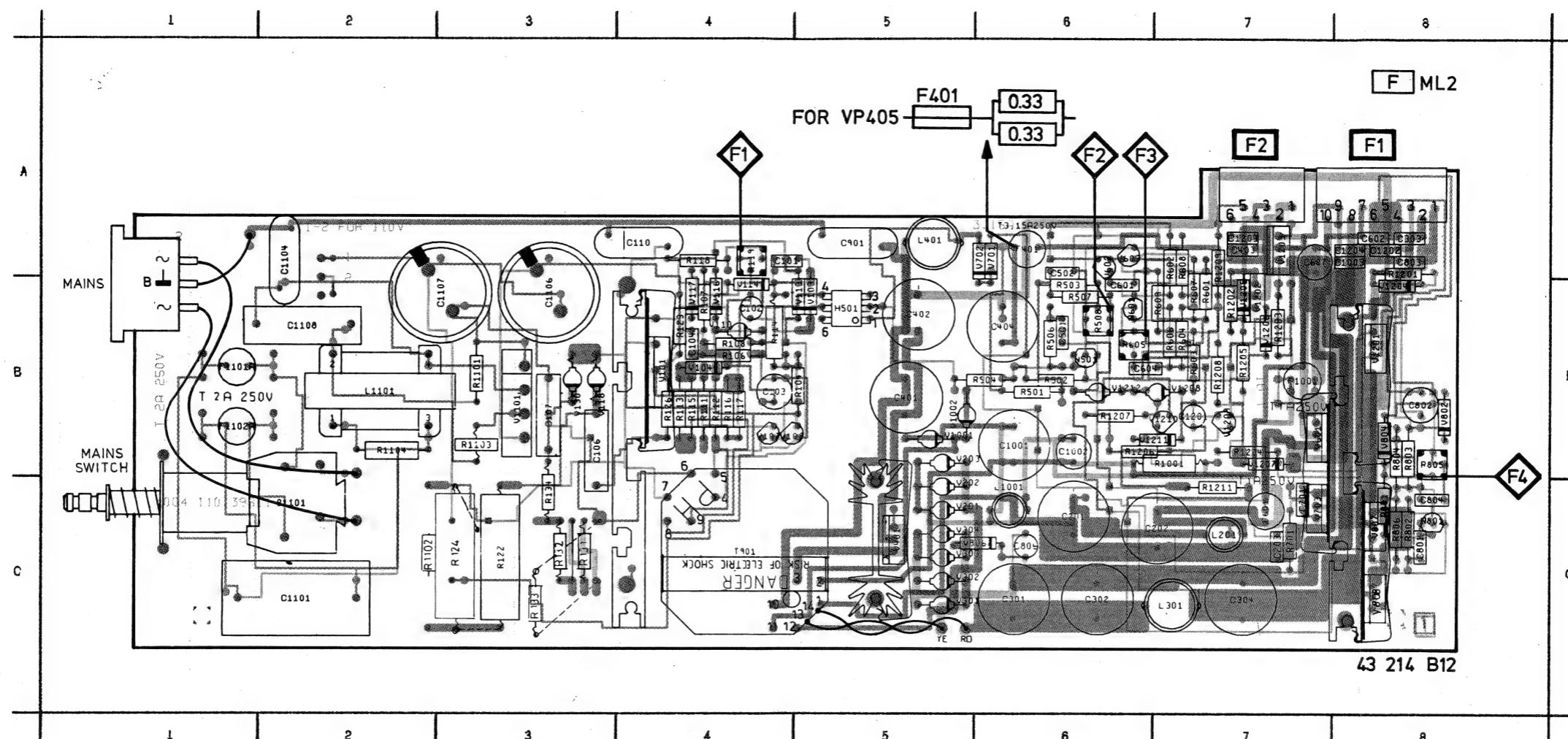
CODRIVE MODULE

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2002	M 3
2003	M 3
2004	A 4
2005	H 6
2007	L 7
2008	A 9
2009	H 1
2011	N 12
2012	B 12
2013	A 16
2014	H 8
2015	F 20
2016	H 22
2017	D 21
2018	D 23
2019	E 22
2020	E 26
2022	D 28
2023	D 29
2024	A 30
2025	G 29
2026	O 21
2027	O 22
2028	J 8
2041	L 3
2045	L 4
2054	K 19
2055	M 2
2056	M 4
2059	A 4
2060	N 10
3001	B 2
3002	A 3
3003	I 4
3005	M 5
3006	M 5
3007	K 8
3008	J 9
3009	K 9
3010	K 9
3011	O 8
3012	O 9
3013	B 15
3014	M 14
3015	M 14
3016	M 15
3017	M 15
3018	M 16
3019	P 8
3020	F 20
3021	F 20
3022	K 18
3023	E 26
3024	E 26
3025	J 26
3026	K 6
3040	C 22
3041	J 25
3049	O 17
3101	B 5
3102	B 17
3103	N 4
3104	I 15
3103	N 16
3104	M 21
3104	M 23
3105	H 24
3105	B 15
3105	M 10
3105	M 12
5001	L 2
5002	M 2
5003	N 2
5004	O 21
5101	B 2
6003	N 5
6004	N 8
6005	D 25
6006	D 26
6009	N 24
6010	D 15
7001	M 5
7002	K 8
7003	K 9
7004	M 16
7005	J 25
7006	K 25
7008	S 5
7009	M 15
7101	A 3
7104	B 12
7107	A 17
7108	H 17
7109	H 10
7110	L 5
7111	L 24
7112	H 20
7113	M 21
7116	N 9
7118	H 6
7119	A 8
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7124	L 25
7124	K 28
7126	L 24
7127	F 27
7127	B 15



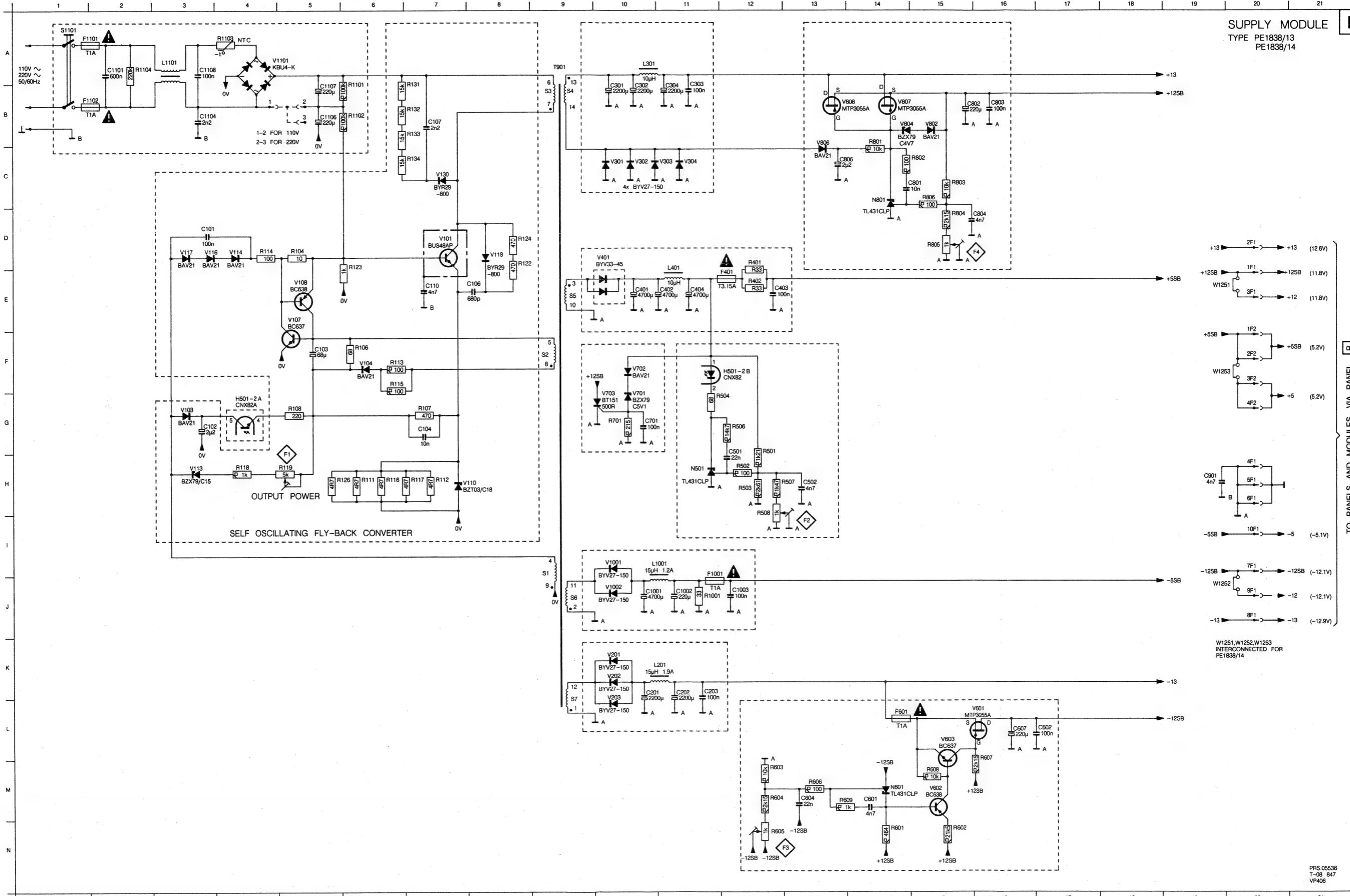
SUPPLY MODULE F

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C1002	B	6	C1106	B	3	C302	C	6	C604	B	7	F	1001	B	7	L401	A	5	R112	B	4	R1204	B	7	R131	C	3	R801	B	7	R302	C	8	V104	B	4	V1202	B	7	
C1003	A	8	C107	B	3	C303	A	8	C607	A	7	F	1101	B	1	R1001	B	7	R113	B	4	R1205	B	7	R132	C	3	R602	A	7	R803	B	8	V107	B	4	V1203	A	7	
C101	A	5	C1108	B	2	C304	C	7	C701	C	7	F	1102	B	1	R104	B	5	R114	B	5	R1206	B	6	R133	C	3	R603	B	7	R804	B	8	V108	S	5	V1204	B	7	
C102	B	4	C1201	B	7	C401	B	5	C801	C	8	F	401	A	6	R108	B	4	R115	B	4	R1207	B	6	R134	C	3	R604	B	7	R305	B	8	V110	B	4	V1204	A	8	
C103	B	4	C1202	A	3	C402	B	5	C602	B	8	F	401	A	5	R107	B	4	R116	B	4	R1208	B	7	R1501	B	6	R605	B	6	R806	C	8	V101	B	3	V1205	B	7	
C104	B	4	C1203	A	7	C403	A	7	C803	A	8	F	601	C	7	R108	B	4	R116	B	4	R1209	A	7	R1502	B	6	R606	B	7	S1101	C	2	V113	S	5	V1207	B	7	
C105	B	3	C1204	A	8	C404	B	6	C804	C	8	H	501	B	5	R1101	B	3	R118	A	4	R1211	C	7	R1503	B	6	R607	B	7	T901	C	4	V114	B	4	V1208	B	7	
C107	B	3	C201	C	6	C501	B	6	C809	C	6	L	1001	C	6	R1102	C	3	R119	A	4	R122	C	3	R504	B	6	R608	A	7	V1001	B	6	V116	B	4	V1209	B	7	
C110	A	4	C202	C	7	C502	A	6	C901	A	5	L	1101	B	2	R1103	B	3	R1201	A	8	R123	B	4	R506	B	6	R609	B	7	V1002	B	6	V117	B	4	V1210	B	7	
C1101	C	2	C203	C	7	C601	B	6	F	1	A	8	L	201	C	7	R1104	B	2	R1202	B	7	R124	C	3	R507	B	6	R701	C	7	V101	B	4	V118	B	4	V1211	B	7



C1001 J10	C106 E 8	C1108 A 3	C304 B11	C601 M14	C803 B16	F401 E12	L401 D11	R107 G 7	R112 H 7	R119 H 5	R133 B 7	R504 G12	R604 M12	R801 B14	T901 A 9	V108 E 5	V118 D 8	V303 C11	V702 F10	W1251 E19
C1002 J11	C107 B 7	C201 K10	C401 E10	C602 L17	C804 D16	F601 L11	N501 H11	R108 G 5	R113 F 6	R122 D 8	R134 C 7	R506 G12	R605 M12	R802 C15	V1001 I10	V110 H 8	V304 C11	V703 G10	W1252 J19	
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C101 D 3	C1101 A 2	C203 K11	C403 E13	C605 L16	C807 C14	H501 H 9	N801 F 12	R1102 B 6	R115 F 6	R124 D 8	R134 E12	R508 H12	R607 M15	R804 C15	V1003 I10	V110 H 8	V304 C11	V702 B15	W1254 B14	
C102 G 3	C1104 B 3	C301 B10	C404 E11	C606 L16	C808 G 10	F1001 I11	H1001 J11	R1103 A 4	R116 H 6	R125 D 8	R135 D15	R509 H14	R608 M15	R805 C15	V1003 G 3	V114 D 4	V203 K10	V602 M15	V806 B13	
C103 F 5	C1106 B 5	C302 B10	C501 G 2	C607 C15	C809 D 5	F1101 A 2	L201 K11	R1104 A 2	R117 H 7	R131 A 7	R132 B 7	R503 H12	R609 M13	R806 C15	V104 F 6	V116 D 3	V301 C10	V603 L15	V807 B14	
C104 G 7	C1107 B 5	C303 A11	C502 H 3	C608 B 2	C810 L301	F1102 B 2	L301 A10	R106 F 6	R118 H 4	R132 B 7	R503 H12	R603 M12	R701 G10	S1101 A 1	V107 E 5	V117 D 3	V302 C10	V701 G10	V808 B14	

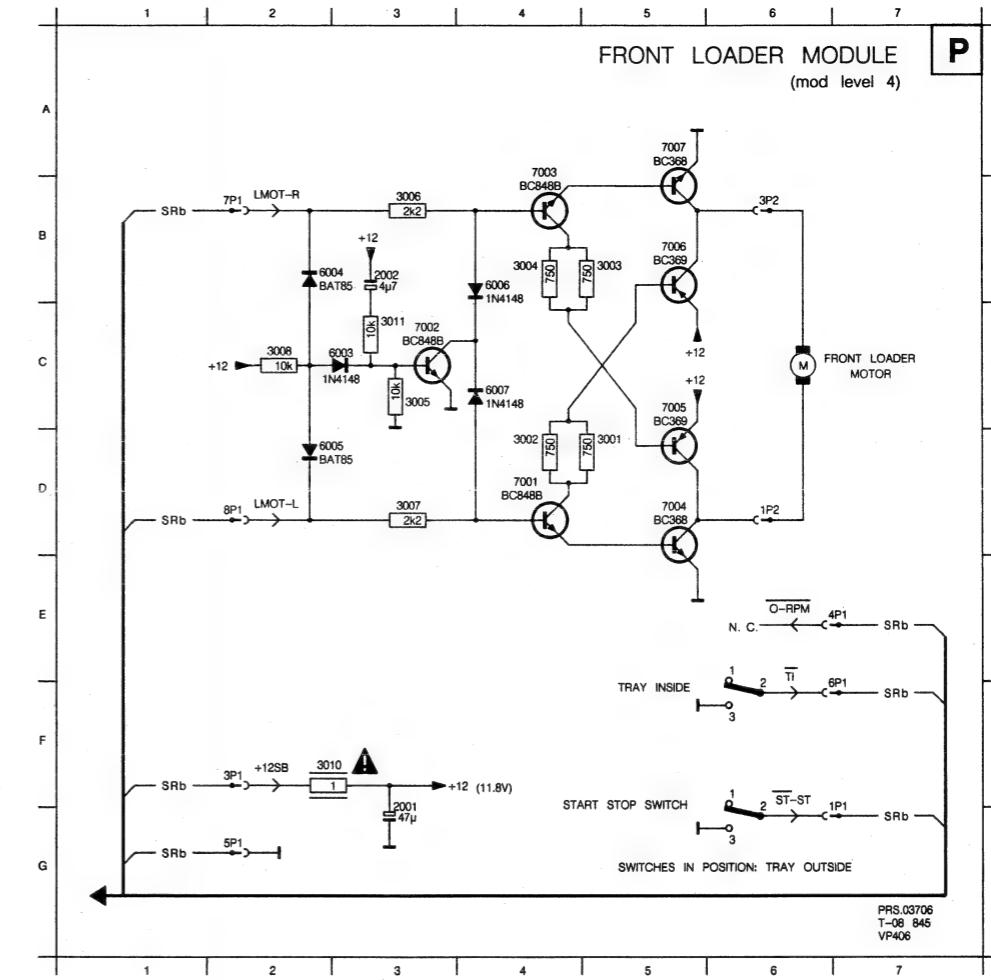
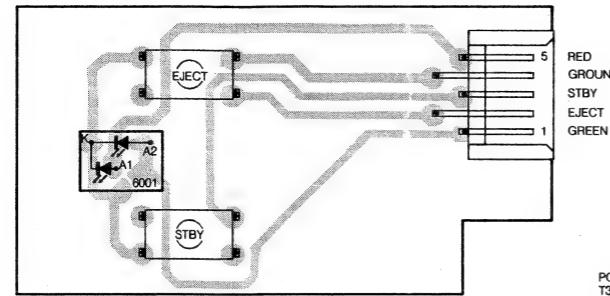
SUPPLY MODULE
TYPE PE1838/13
PE1838/14



FRONT LOADER **P**
mod level 4

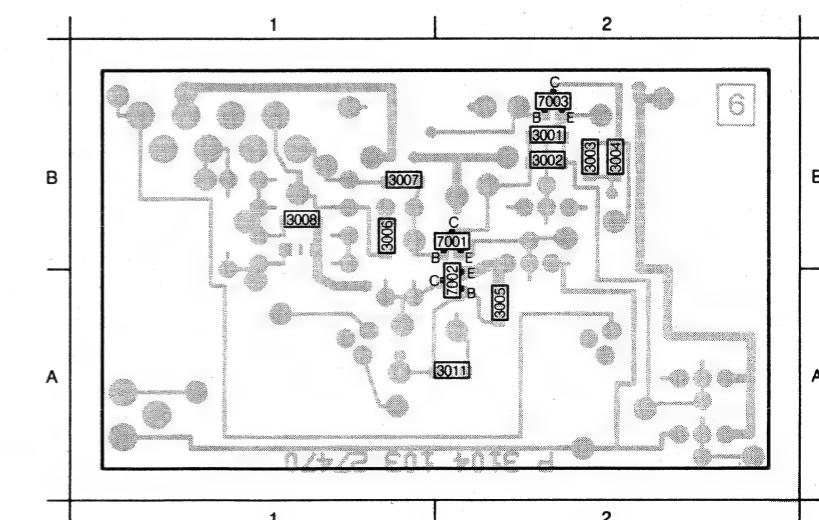
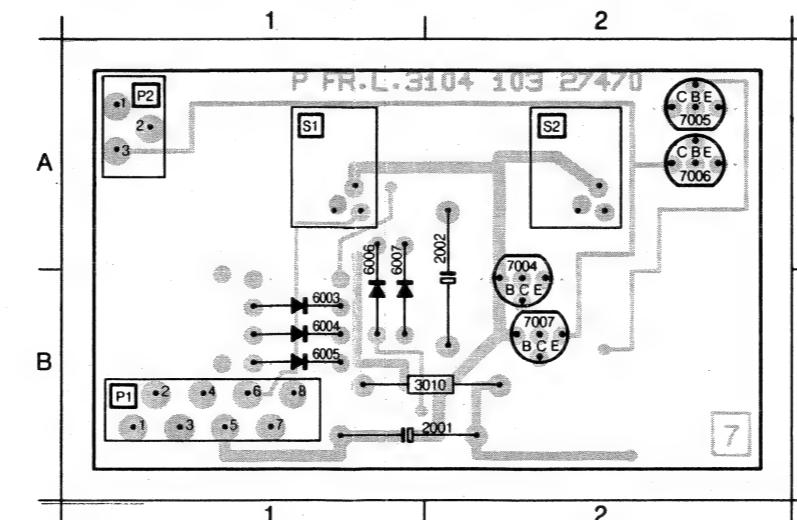
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2002 B 3	3003 B 5	3006 B 3	3010 F 2	6004 C 3	6007 C 4	7003 A 4	7006 B 5
2001 D 5	3004 B 4	3007 D 3	3011 C 3	6005 D 3	7001 D 4	7004 D 5	7007 A 5

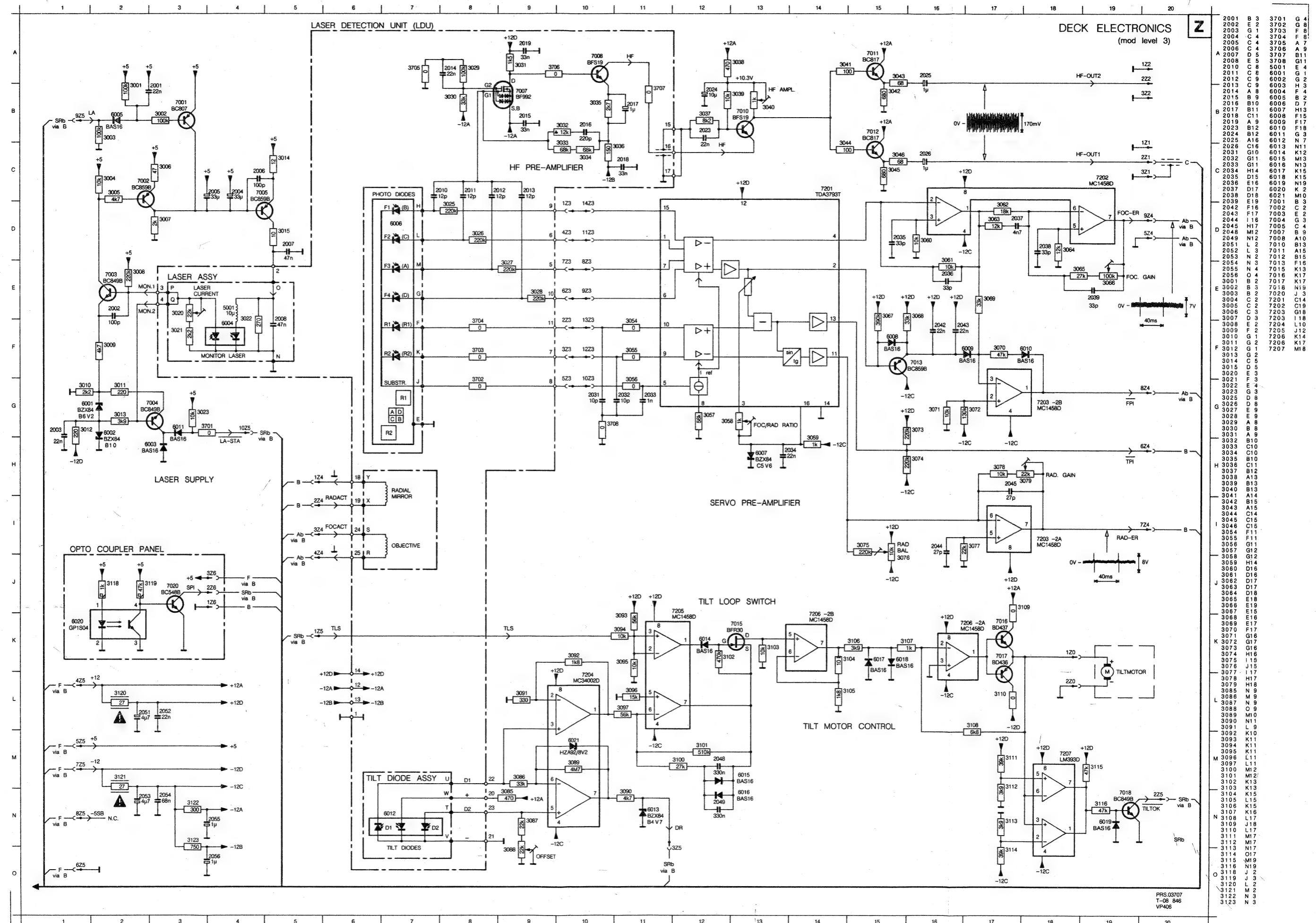
KEYBOARD **N**



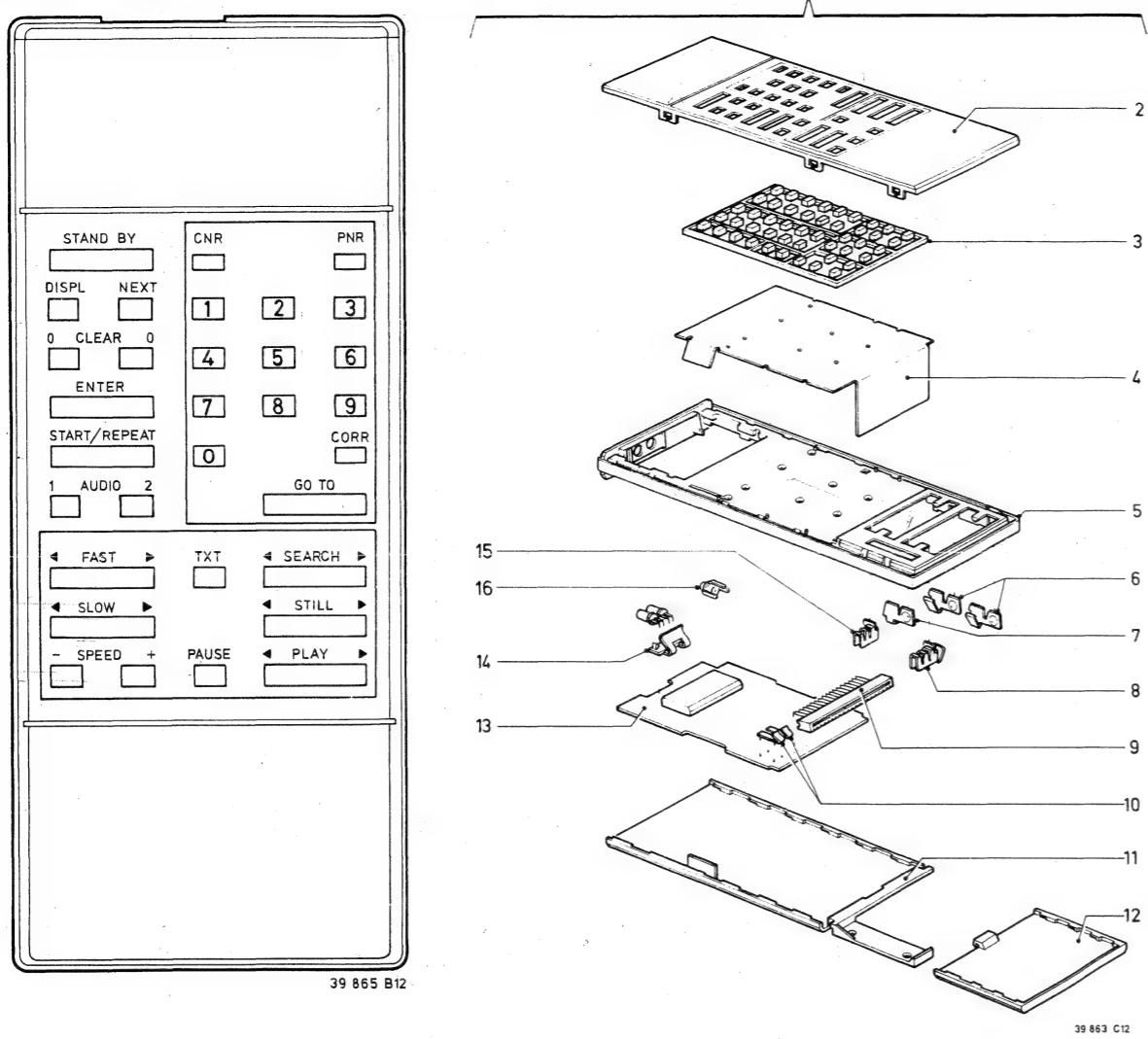
2001 B 2 3010 B 2 6004 B 1 6006 A 1 7004 A 2 7006 A 2
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3001 B 2 3003 B 2 3005 A 2 3007 B 1 3011 A 2 7002 A 2
3002 B 2 3004 B 2 3006 A 1 3008 B 1 7001 B 2 7003 B 2





REMOTE CONTROL **RC 53 VP4xx TRANSMITTER**



ELECTRICAL PARTS

Batteries
4x R03P 1.5V

Crystals

1001 4822 242 71498 CSB429

Integrated circuits

7001 4822 209 81891 SAA3006P

Transistors

7002 4822 130 40937 BC548B
7003 4822 130 41715 BC328-40

LEDs

6003 4822 130 31332 CQY89A-2
6004 4822 130 31332 CQY89A-2

Diode

6005 4822 130 30847 BA317

Capacitors

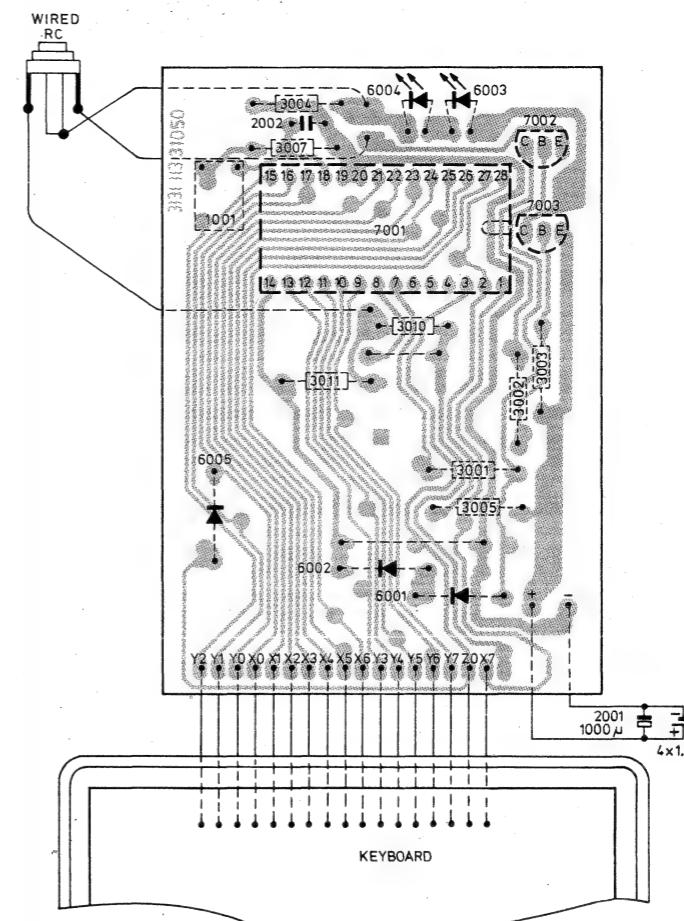
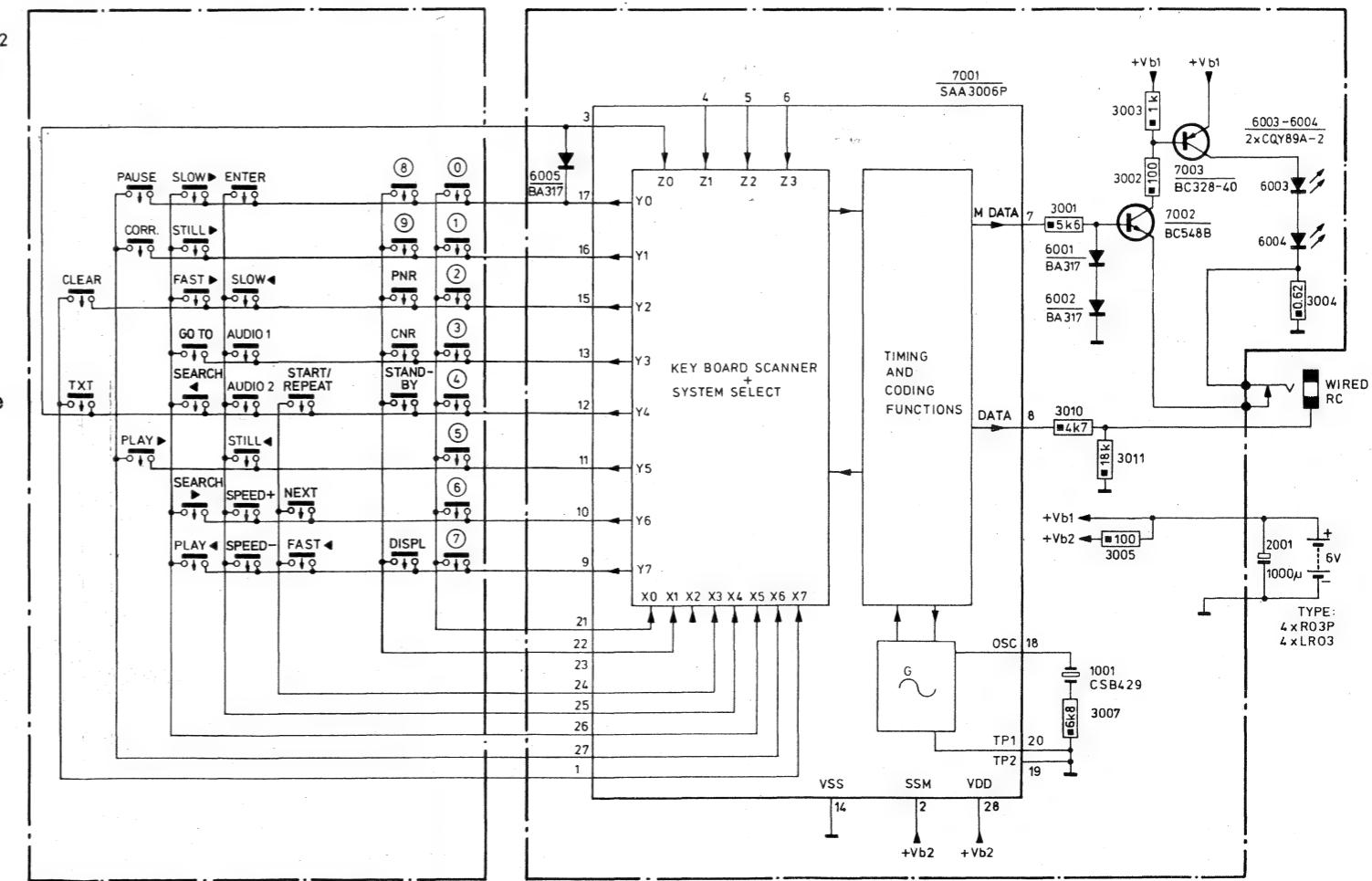
2001 4822 124 21341 1000 μ F 8V

Resistors

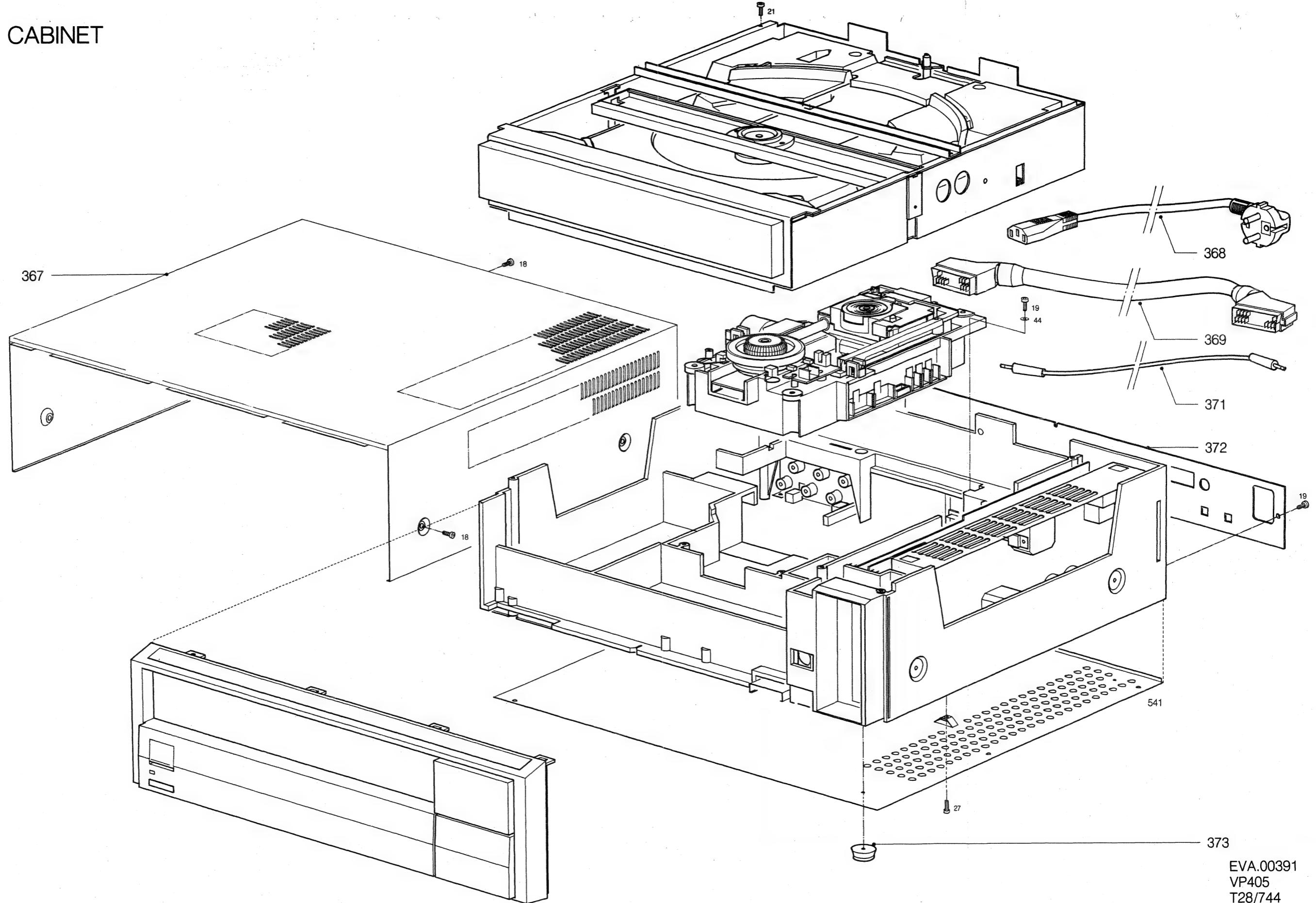
3004 4822 110 73027 0.62 Ω

MECHANICAL PARTS

- | | | |
|----|----------------|----------------------|
| 1 | 4822 218 20607 | Transmitter complete |
| 2 | 4822 432 30284 | Top cover |
| 3 | 4822 410 25423 | Knob assembly |
| 4 | 4822 276 80313 | Switch panel |
| 5 | 4822 432 30283 | Casing |
| 6 | 4822 492 62879 | Battery contact |
| 7 | 4822 492 62881 | Battery contact |
| 8 | 4822 492 62883 | Battery contact |
| 9 | 4822 267 50418 | Connector |
| 10 | 4822 492 62904 | Spring |
| 11 | 4822 432 30282 | Bottom |
| 12 | 4822 432 30281 | Battery lid |
| 13 | 4822 214 50358 | Printed board |
| 14 | 4822 256 90506 | LED holder |
| 15 | 4822 492 62882 | Battery contact |
| 16 | 4822 267 50443 | Connector |

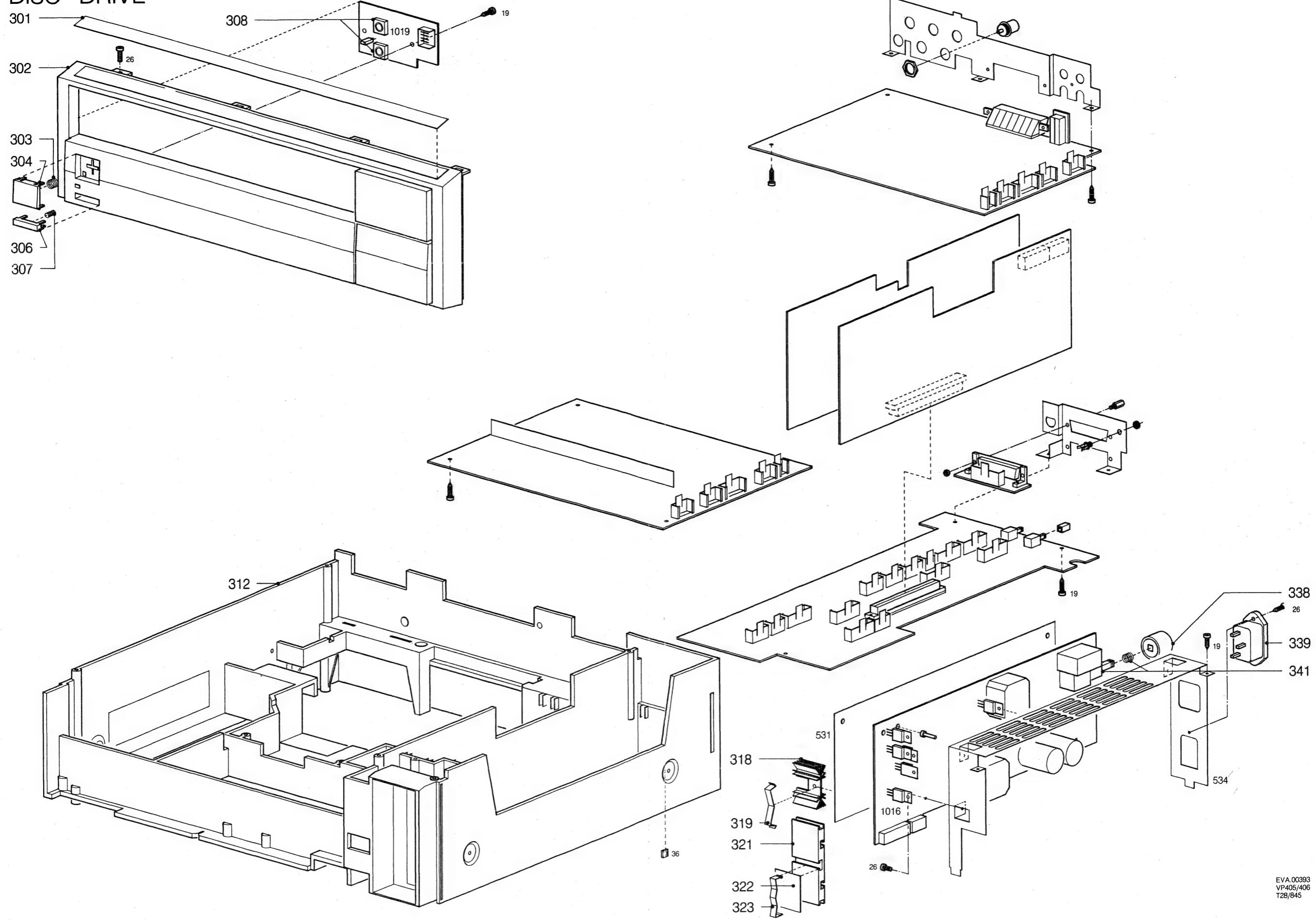


CABINET



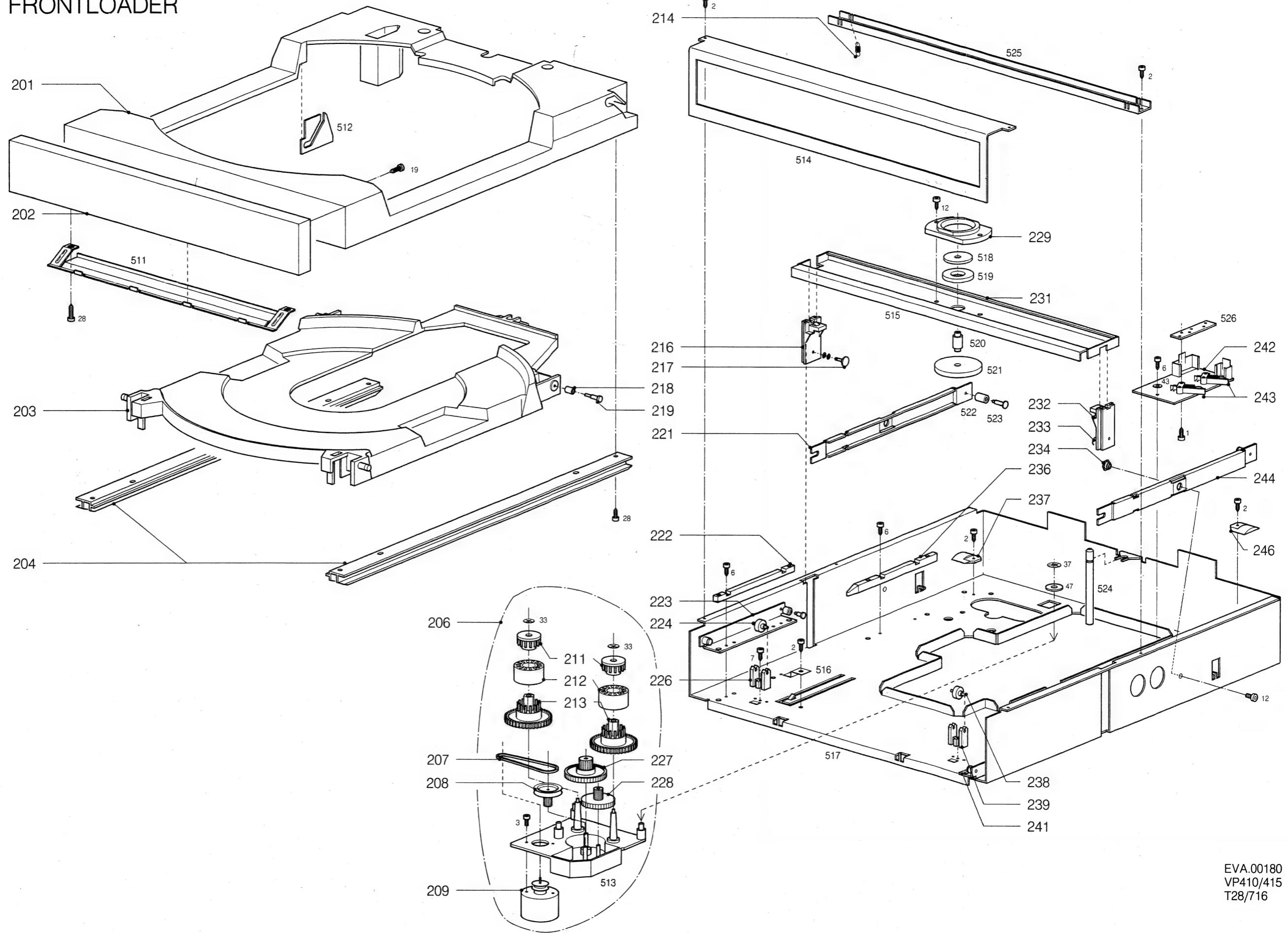
EVA.00391
VP405
T28/744

DISC DRIVE



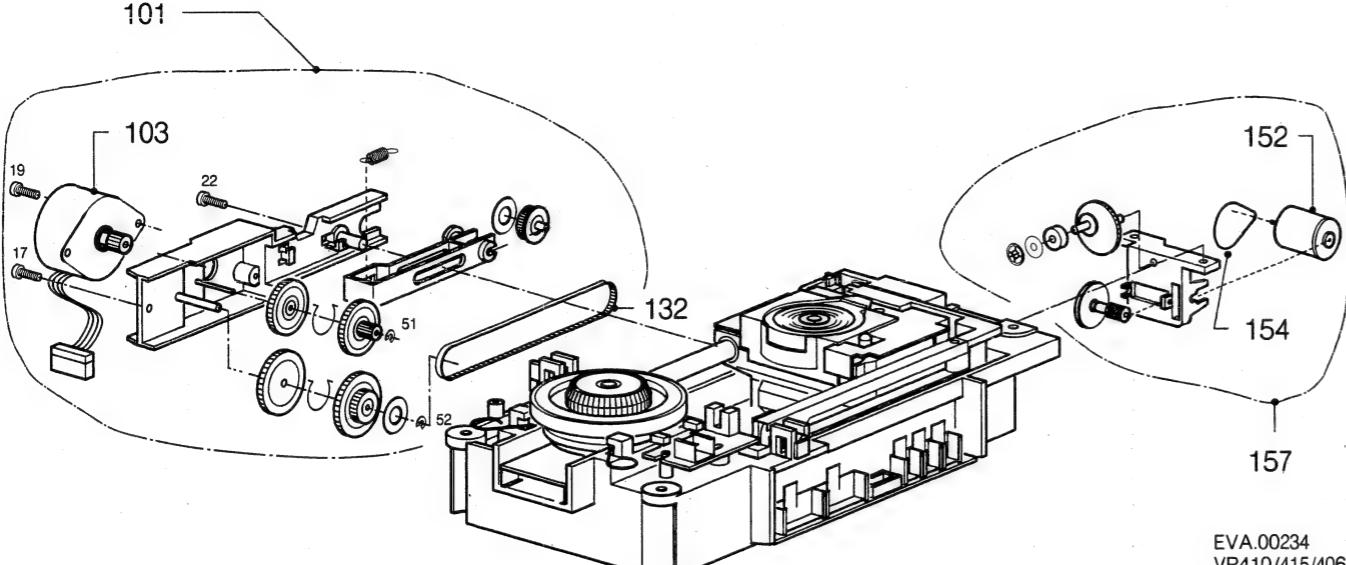
EVA.00393
VP405/406
T28/845

FRONTLOADER



EVA.00180
VP410/415
T28/716

OPTICAL DECK



EVA.00234
VP410/415/406
T28/845

22VP406/00/05 *

* For difference see item 368

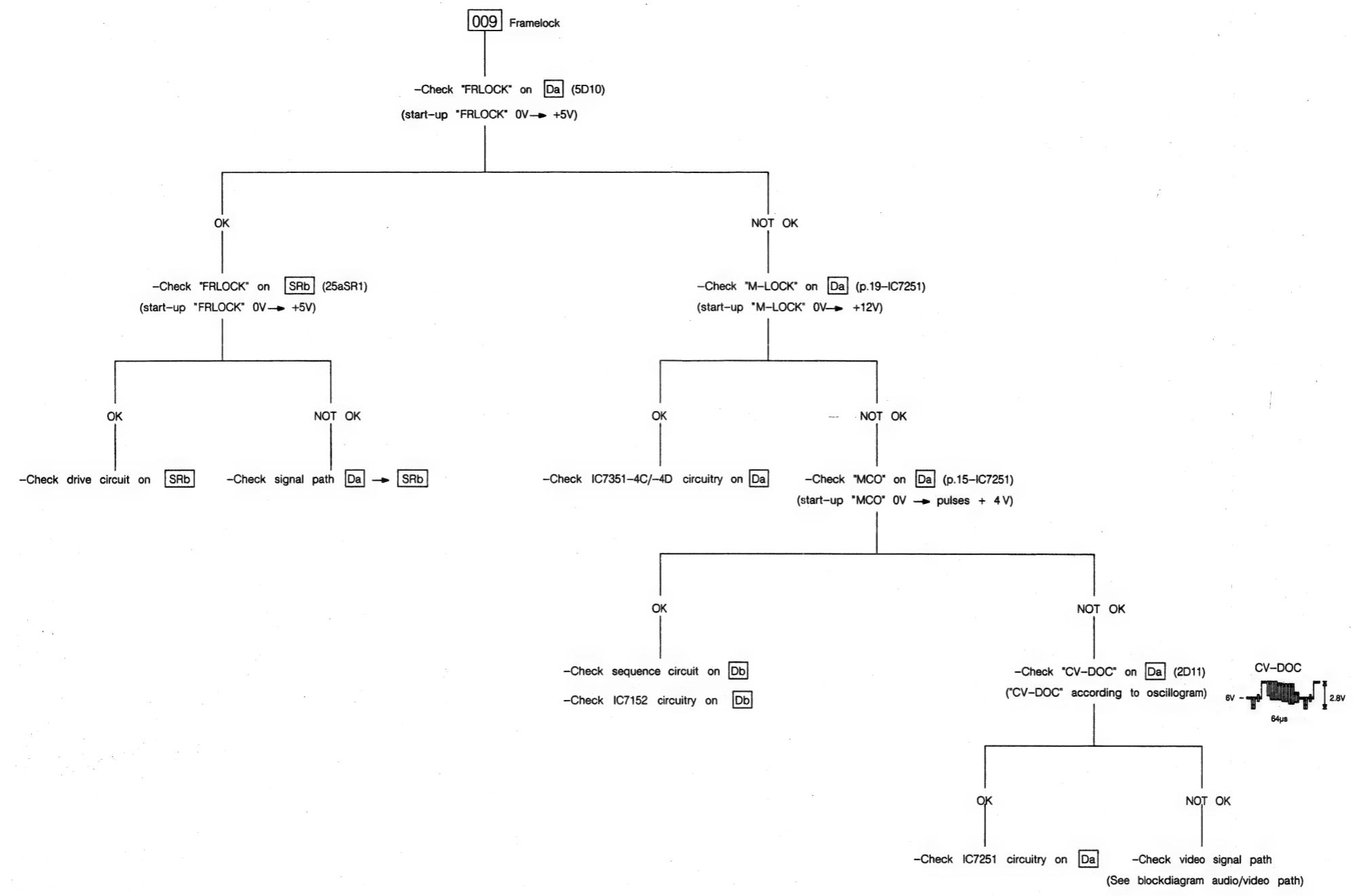
LIST OF MECHANICAL PARTS

FIXING MATERIALS

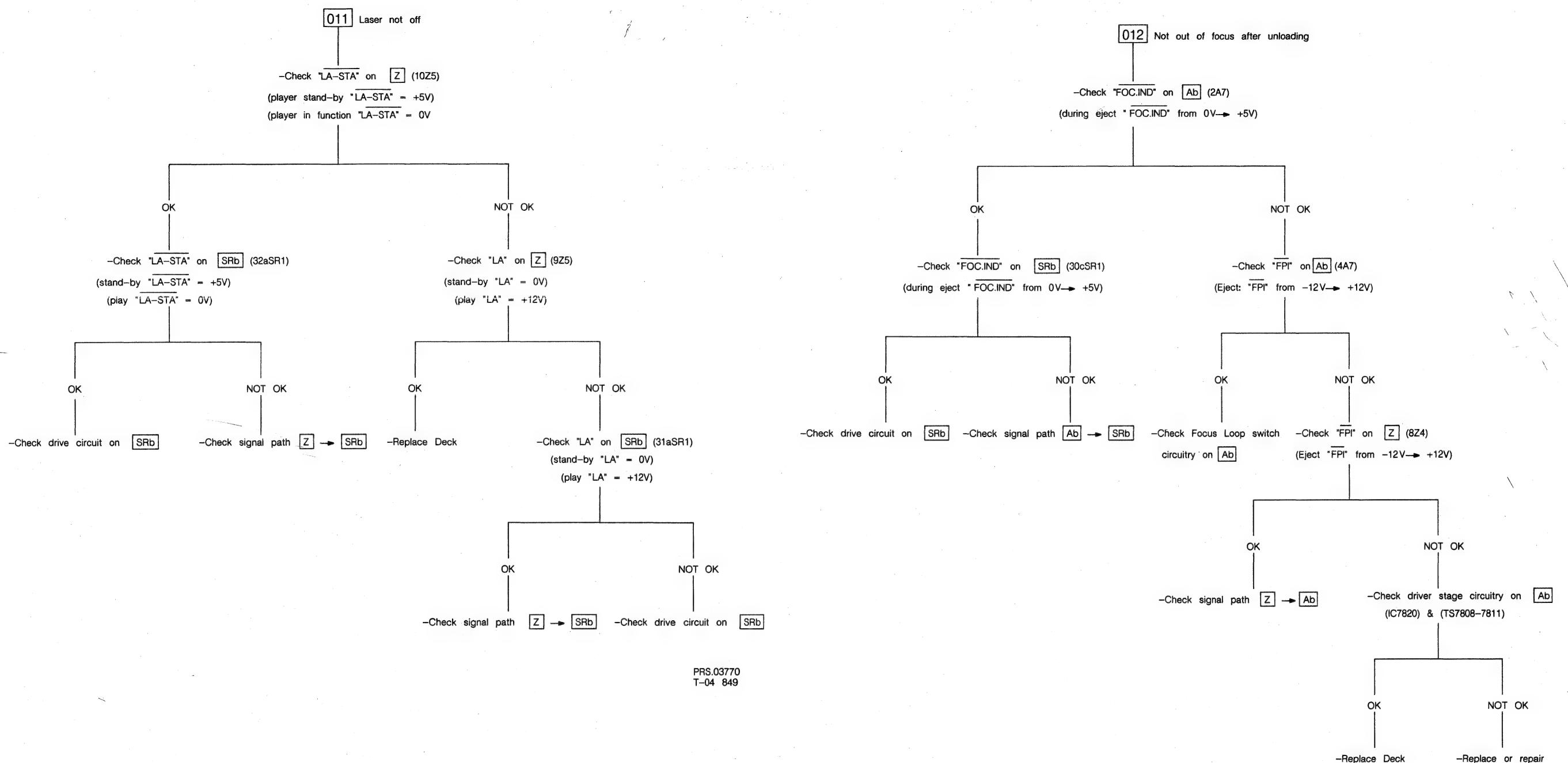
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1	4822 502 12555	Screw M 2 x 10
2	4822 502 12797	Screw M 2.5 x 4
3	4822 502 11715	Screw M 2.5 x 5
6	4822 502 12795	Screw M 2.5 x 6
7	4822 502 12799	Screw M 2.5 x 8
12	4822 502 11667	Screw M 3 x 6
13	4822 502 11679	Screw M 3 x 16
17	4822 502 30439	Screw 3 M x 8
18	4822 502 12863	Screw M 3 x 8
19	4822 502 30408	Screw 3 M x 10
20	4822 502 12794	Screw M 3 x 5
21	4822 502 30409	Screw 3 M x 12
22	4822 502 30412	Screw 3 M x 20
23	4822 502 30522	Screw Selftap 3.5 x 6.5
26	4822 502 30303	Screw 4 N x 6.5
27	4822 502 30085	Screw 4 N x 9.5
28	4822 502 30314	Screw 4 N x 22
29	4822 502 12864	Screw 4 N x 9.5
30	4822 502 11717	Screw for RS232-connector
31	5322 505 10711	Nut for RS232-connector
33	4822 505 10892	Nut M 3 Speed nut
36	4822 505 10635	Nut M 3
37	4822 505 10893	Nut M 4 Speed nut
42	4822 530 80146	Ring 3.2 x 6
43	4822 532 10332	Washer 3.2 x 7
44	4822 532 51843	Washer 3.2 x 9
47	4822 532 51844	Washer
51	4822 530 70121	Retaining ring 1.5
52	4822 530 70122	Retaining ring 1.9
OPTICAL DECK		
101	4822 691 30185	Slide drive assy
103	4822 361 20963	Motor assy
112	4822 361 20965	Motor
132	4822 358 20264	Tooth belt
152	4822 361 20964	ATC motor assy
154	4822 358 10107	Belt
157	4822 691 30186	ATC drive assy

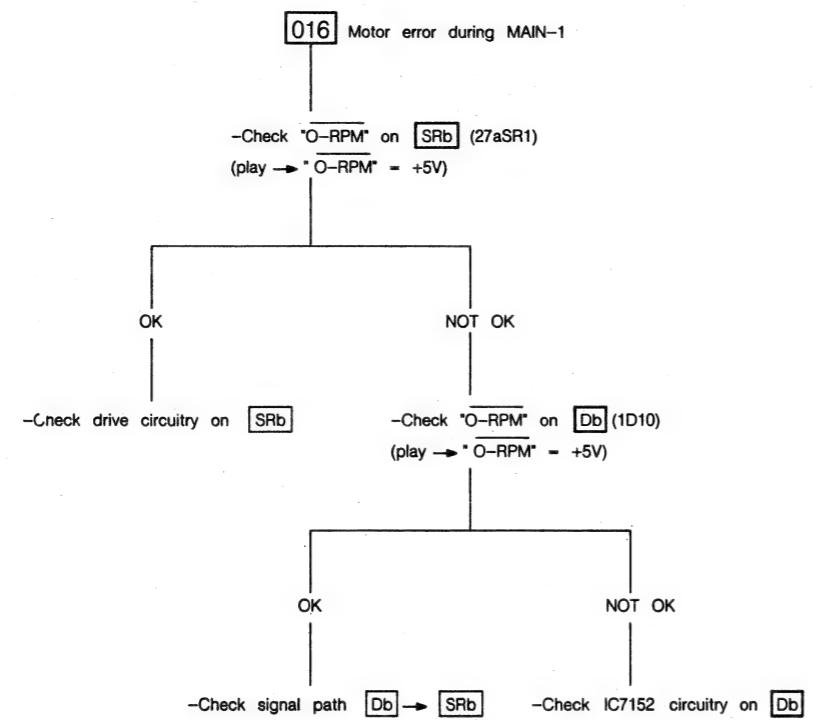
FRONTLOADER

Item	Service codenr	Description
201	4822 418 40547	Tray assy
202	4822 691 30184	Front tray assy
203	4822 532 61051	Disc carrier
204	4822 466 82136	Guide section
206	4822 691 20403	Front loading drive
207	4822 358 30741	Belt
208	4822 528 81143	Pulley
209	4822 361 20933	Motor assy
211	4822 532 61049	Mounting bush
212	4822 528 90636	Friction wheel
213	4822 522 32254	Gear wheel
214	4822 492 32671	Tension spring
216	4822 466 82139	Slide block
217	4822 535 92288	Pin
218	4822 528 90637	Roller
219	4822 535 92289	Pin
221	4822 402 61074	Bracket assy
222	4822 402 61075	Guide support
223	4822 402 61072	Guide bracket
224	4822 528 90634	Wheel
226	4822 466 82137	Block
227	4822 522 32253	Gear wheel
228	4822 522 32252	Gear wheel
229	4822 532 51845	Catch ring
231	4822 402 61073	Pressure bracket assy
232	4822 466 82139	Slide block
233	4822 535 92288	Pin
234	4822 528 90635	Nave
236	4822 466 82138	Guide support
237	4822 528 30324	Rise cam
238	4822 528 90634	Wheel
239	4822 466 82137	Block
241	4822 402 61072	Guide bracket
242	4822 214 51583	Printed board assy
243	4822 276 11897	Switch assy
244	4822 402 61074	Bracket assy
246	4822 528 30324	Rise cam



PRS.03771
T-04 849





PRS.03765
T-04 849

017 No focus 20 steps after focus error

-Check disc for damages

OK

NOT OK

-Check "LA" on **Z** (9Z5)
(play → "LA" = + 12V)

OK

-Check "LA-STA" on **Z** (10Z5)
(play → "LA-STA" = 0V)

OK

NOT OK

-Check "LA-STA" on **SRb** (32aSR1) Replace Deck
(play → "LA-STA" = 0V)

OK

NOT OK

-Check "FPI" on **Ab** (4A7)
(focus finding: "FPI" +12V → -12V)

-Check Focus loop switch
circuitry on **Ab**

-Check "FPI" on **Z** (8Z4)
(play → "FPI" = - 12V)

-Check signal path **Ab** → **Z**

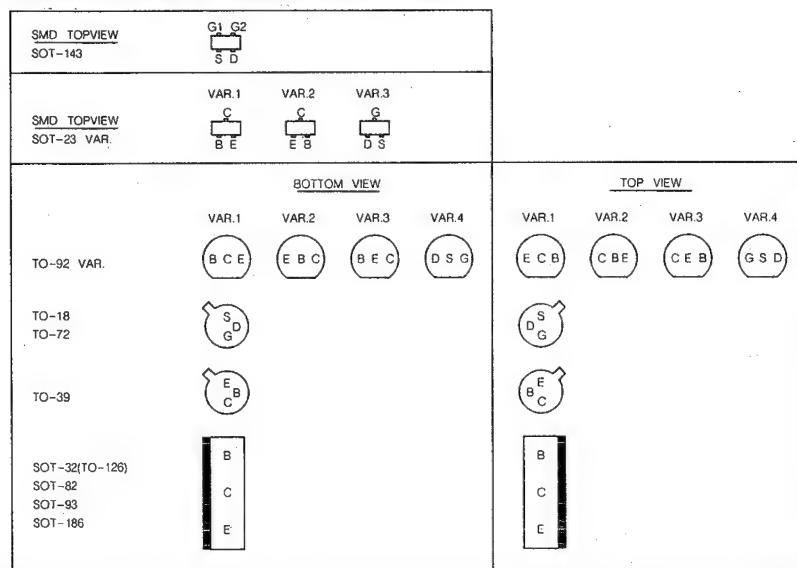
-Check driver stage circuitry on **Ab**
(IC7820 & T7808-7811)

OK
-Replace Deck

NOT OK
-Replace or repair **Ab**

PRS.03764
T-04 849

CONNECTIONS OF SEMICONDUCTORS



MDA.0063
T10 716

SOT-143	BF992	BC264	TO-92 VAR.4
SOT-186	BUT11F	BC327	TO-92 VAR.2
SOT-23 VAR.1	BC807	BC337	TO-92 VAR.2
	BC817	BC368	TO-92 VAR.1
	BC847	BC369	TO-92 VAR.1
	BC848	BC375	TO-92 VAR.2
	BC849	BC376	TO-92 VAR.2
	BC858	BC546	TO-92 VAR.2
	BC859	BC547	TO-92 VAR.2
	BFS19	BC548	TO-92 VAR.2
		BC549	TO-92 VAR.2
SOT-23 VAR.3	BFR30	BC556	TO-92 VAR.2
		BC557	TO-92 VAR.2
SOT-32 (TO-126)	BD135	BC558	TO-92 VAR.2
	BD434	BC639	TO-92 VAR.1
	BD435	BC640	TO-92 VAR.1
	BD436	BC807	SOT-23 VAR.1
	BD437	BC817	SOT-23 VAR.1
	BD438	BC847	SOT-23 VAR.1
	BUX86	BC848	SOT-23 VAR.1
		BC849	SOT-23 VAR.1
SOT-82	BUW85	BC858	SOT-23 VAR.1
SOT-93	BUW12	BC859	SOT-23 VAR.1
TO-18	BSV78	BD135	SOT-32 (TO-126)
	BSV80	BD434	SOT-32 (TO-126)
		BD435	SOT-32 (TO-126)
TO-39	BSW68	BD436	SOT-32 (TO-126)
TO-72	BSD213	BD437	SOT-32 (TO-126)
TO-92 VAR.1	BC368	BD438	SOT-32 (TO-126)
	BC369	BD439	SOT-32 (TO-126)
	BC639	BFR30	SOT-23 VAR.3
	BC640	BFR54	TO-92 VAR.2
TO-92 VAR.2	BC327	BFS19	SOT-23 VAR.1
	BC337	BF256	TO-92 VAR.4
	BC375	BF450	TO-92 VAR.3
	BC376	BF494	TO-92 VAR.3
	BC546	BF992	SOT-143
	BC547	BSD213	TO-72
	BC548	BSV80	TO-18
	BC549	BSW68	TO-39
	BC556	BUT11F	SOT-186
	BC557	BUW12	SOT-93
	BC558	BUW85	SOT-82
		BUX86	SOT-32 (TO-126)
		PH2369	TO-92 VAR.2
TO-92 VAR.3	BF450		
	BF494		
TO-92 VAR.4	BC264		
	BF256		

LIST OF USED SYMBOLS

	Safety resistor Veiligheidsweerstand Sicherheitswiderstand Résistance de sécurité		Sawtooth pulse converter Zaagtand-puls omzetter Sägezahn Impulsúmformer Convertisseur d'impulsions en dents de scie
	0.2 W \leq 220 k Ω - 5% (CR16) > 270 k Ω - 10%		Pulse-code modulation (6-unit binary code) Puls code modulatie (6 bits code) Impulscode-Modulation (6 Bits-code) Modulation code d'impulsions (code 6 bits)
	0.33 W < 1 M Ω - 5% (SFR25) > 1 M Ω - 10%		Puls-duration modulation Pulslenge modulatie Impulslänge-Modulation Modulation de durée d'impulsion
	0.5 W \leq 1 M Ω - 5% (CR37) > 1 M Ω - 10%		Sync separator Sync scheider Sync-Trenner Séparateur sync
	0.33 W - MR25 - 1%		FM detector FM detector FM-Detektor Détecteur FM
	0.5 W \leq 1 M Ω - 5% (CR52) > 1 M Ω - 10%		Phase discriminator Fasediscriminator Phasenvergleich Discriminateur de phase
	1 W \leq 1.6 M Ω - 5% (CR68) > 1.6 M Ω - 10%		Detector Detector Detektor Détecteur
	0.5 W High voltage resistor (VR37) Hoogspanningsweerstand Hochspannungswiderstand Résistance haute tension		Level detector Niveau detector Niveau-Detektor Détecteur de niveau
	Safety capacitor Veiligheidscondensator Sicherheitskondensator Condensateur de sécurité		Phase-changing network Faseverschuiver Phasenverschiebung Circuit de déphasage
	Ceramic plate capacitor Keramische plaatcondensator Keramischer Platten-Kondensator Condensateur céramique plaque		Rejection filter Bandsperfilter Bandsperrefilter Filtre de suppression
	Metalized polyester flat film capacitor Gemetalliseerde polyester condensator Metallisierter Polyester-Flachkondensator Condensateur plat à feuille de polyester métallisée		Bandpass filter Band-doorlatend filter Bandpassfilter Filtre passe-bande
	Miniature electrolytic capacitor Miniatuur electrolytische condensator Miniatur-Elektrolytkondensator Condensateur électrolytique miniature		Low-pass filter Laag-doorlatend filter Tiefpassfilter Filtre passe-bas
$a = 2.5 \text{ V}$			Mixer stage Mengtrap Mischstufe Etage mélangeur
$b = 4 \text{ V}$			
$c = 6.3 \text{ V}$			
$d = 10 \text{ V}$			
$e = 16 \text{ V}$			
$f = 25 \text{ V}$			
$g = 40 \text{ V}$			
$h = 63 \text{ V}$			
$j = 100 \text{ V}$			
$l = 125 \text{ V}$			
$m = 150 \text{ V}$			
$q = 200 \text{ V}$			
$r = 250 \text{ V}$			
$s = 350 \text{ V}$			
$u = 400 \text{ V}$			
$v = 500 \text{ V}$			
$w = 630 \text{ V}$			
$x = 1000 \text{ V}$			
$y = 1600 \text{ V}$			

	High-pass filter Hoog-doorlaend filter Hochpassfilter Filtre passe-haut	Common control block Gemeenschappelijk controleblok Gemeinschaftlicher Kontrollblock Bloc de contrôle commun
	HF generator HF generator HF-Generator Générateur HF	SRG Shift register Schuif register Schieberegister Registre à décalage
	Sawtooth generator Zaagtandgenerator Sägezahngenerator Générateur en dents de scie	Q Output Uitgang Ausgang Sortie
	Square wave generator Pulsgenerator Rechteckgenerator Générateur d'impulsions rectangulaires	Open collector output Open kollektor uitgang Offenen Kollektor ausgang Sortie collecteur ouvert
	Delay element Vertragingselement Verzögerungselement Elément à retard	G Command input Kommando ingang Kommando eingang Entrée ordres
	Limiter Begrenzer Begrenzer Limiteur	CE Chip enable input Chip enable ingang Chip enable eingang Entrée chip validation
	Positive-going step function Positieve flank Übergang von tief zu hoch Fonction de palier en sens positif	00 Bidirectional Tweezijdig gevoelig Doppelseitig empfindlich Bidirectionel
	Negative-going step function Negatieve flank Übergang von hoch zu tief Fonction de palier en sens négatif	 Inverter Inverter Inverter Invertisseur
	Emitter follower Emitter volger Emitter folger Emetteur suiveur	 Or gate Of-poort Oder Porte ou
	Automatically controlled amplifier Automatisch gestuurde versterker Automatisch gesteuerte Verstärker Amplificateur à commande automatique	 Nor gate "Nor" "Nor" Porte Non-ou
	Mixer stage Mengtrap Mischstufe Etage mélangeur	 And gate En-poort Und Gatter Porte Et
	Amplifier Versterker Verstärker Ampli	 Nand gate "Nand" "Nand" Porte "Non-Et"
	Differential amplifier Verschilversterker Differentialverstärker Ampli différentiel	 Buffer Buffer Puffer Tampon
	Amplifier with open output Versterker met open uitgang Verstärker mit offenem ausgang Ampli a sortie ouverte	 Inverting buffer Inverterende buffer Invertierender puffer Tampon invertisseur
	Electronic switch Electronische schakelaar Elektronische Schalter Commutateur électronique	 Buffer with open output Buffer met open uitgang Puffer mit offenem ausgang Tampon à sortie ouverte
	Electronic switch Electronische schakelaar Elektronischer Schalter Commutateur électronique	

Chapter 3

**Module- and connector lay-out
Signal listing
Wiring diagram
Blockdiagram Control routes
Blockdiagram AUDIO/VIDEO signal path
Blockdiagram Servo**

Chapter 4

Survey of modules and panels

- Circuit diagram**
- PCB lay-out**
- Remote control**

SURVEY OF MODULES AND PANELS

MOD	DESCRIPTION
A	VIDEO PROC PANEL
B	RAD + TBC PANEL
C	HF + AUDIO PANEL
D	MOTORSEQ + TBC MODULE
SR	CONTROL + DRIVE MODULE
F	SUPPLY MODULE
N	KEYBOARD
P	FRONT LOADER
Z	DECK ELECTRONICS

Chapter 5

**Exploded view drawings
List of mechanical parts
List of electrical parts**

DISC DRIVE

Item	Service codenr	Description
301	4822 454 30384	Ornamental plate
302	4822 444 40204	Front assy
303	4822 492 51891	Spring
304	4822 410 25447	Eject knob
306	4822 410 25448	Standby knob
307	4822 492 51889	Spring
308	4822 276 10974	Switch
312	4822 464 50639	Frame assy
318	4822 255 40825	Heat sink
319	4822 402 61083	Clamping spring
321	4822 255 40824	Heat sink
322	4822 466 61621	Isolating plate
323	5322 401 10783	Clamping spring
324	4822 267 10161	BNC connector
326	4822 267 60198	SCART connector
327	4822 267 30631	Cinch connector
329	4822 267 70202	Connector
331	4822 267 50443	Connector
332	4822 267 60208	RS232 assy
334	4822 276 11301	Switch
336	4822 410 23697	Knob
337	4822 267 40701	Connector
338	4822 410 22364	Knob
339	4822 267 50881	Connector
341	4822 276 12035	Mainsswitch

CABINET

367	4822 444 60462	Cover assy
368	4822 321 10497	Mains cord
368	4822 321 10472	Mains cord (only for VP406/05)
369	4822 321 22527	SCART cable
372	4822 459 10767	Textplate assy
373	4822 462 71261	Foot

IC SOCKETS

5322 255 44122	14p.
5322 255 44047	28p.
4822 255 40129	40p.

CONNECTORS

male top
4822 267 40352
4822 267 40353
4822 267 40354
4822 267 40355
4822 267 50285
4822 267 50406
4822 265 40229
4822 267 50332

male side
4822 265 30572
4822 267 50694
4822 267 50695
4822 267 50693

MODULE CONNECTORS

male (on module A,B,C)
4822 267 50591
4822 264 50149
female (on module D,E,F)
4822 265 40469
4822 265 40472

SERVICE TOOLS

4822 397 30156	Test disc 6"
4822 397 30118	Test disc 8"
4822 397 30119	Test disc 12"
4822 397 30173	Test software "VP400 TEST
4822 395 50145	Torx screwdriving set
4822 310 20411	Complete repair set
Repair set is containing :	
4822 532 60775	Disc clamping piece
4822 267 50706	Simulation F.L.8p.
4822 267 40712	Coupling piece 6p.
4822 267 50705	Coupling piece 12p.
*4822 321 22605	Extender cable 6p.
4822 321 22268	Extender cable 6p.
4822 321 22267	Extender cable 10p.
4822 321 22269	Extender cable 12p.
*4822 321 22606	Extender print 10p.
4822 263 70208	Extender print 64p.

* New for VP406

Rest is existing in repair set 4822 310 3 (VP41X)

LIST OF ELECTRICAL PARTS

INTEGRATED CIRCUITS

4822 209 71276 CXL1004P
 4822 209 71275 CXL5001
 4822 209 73859 EPROM 7105+PROGRAM
 4822 209 73858 EPROM 7104+PROGRAM
 4822 209 72422 HA12083NT
 4822 209 10247 HEF4011BP
 5322 209 10489 HEF40244BP
 5322 209 10576 HEF4053BP
 5322 209 10357 HEF4066BP
 4822 209 10269 HEF4081BP
 5322 209 14927 HEF4093BP
 4822 209 10273 HEF4104BP
 4822 209 10866 HEF4428BP
 5322 209 10422 HEF4538BP
 4822 209 70289 HZ9C1
 5322 209 85503 LM311N
 4822 209 71285 LM358N (MTLA)
 5322 209 70225 LM393D
 4822 209 80797 LM393N
 4822 209 71279 LM4921
 4822 209 72639 MA8031AH-12P/04
 4822 209 71278 MB88303
 5322 209 10421 MC14094BCP
 4822 209 71469 MC1458D
 4822 209 81349 MC1458P1 (MTLA)
 5322 209 84307 MC1488P
 5322 209 85619 MC1489AP
 4822 209 71382 MC34002BP
 4822 209 71361 MC34002D
 4822 209 81713 MC78M08CT
 4822 209 60001 MDC405/2
 4822 209 71825 PA0017
 5322 209 82899 PC74HC10P
 4822 209 60002 PC74HC4052P
 4822 209 11529 PC74HC4066P
 5322 209 82575 PC74HC74P
 5322 209 11316 PC74HCT03P
 4822 209 82341 PC74HCT04P
 5322 209 11379 PC74HCT123P
 5322 209 11378 PC74HCT14P
 5322 209 11268 PC74HCT164P
 5322 209 11266 PC74HCT32P
 5322 209 11118 PC74HCT373P
 5322 209 11119 PC74HCT374P
 4822 209 71583 PC74HCT4052P
 4822 209 71584 PC74HCT4053P
 4822 209 71585 PC74HCT4538P
 5322 209 11109 PC74HCT74P
 4822 209 71277 PD0011
 5322 209 81468 SAA1043P
 5322 209 85752 SN74LS155N (MTLA)
 4822 209 81062 TDA1432P
 4822 209 82146 TDA2501
 4822 209 72155 TDA2595/V7
 4822 209 80744 TDA2730
 4822 209 71971 TDA3505/V9
 4822 209 71319 TDA3793T/N1
 4822 209 70019 TDA4510/V4
 4822 209 71512 TDA4565/V4
 4822 209 11412 TL8704P
 4822 209 11569 TMS27C128-20JL
 4822 209 71579 TY40408
 4822 209 71316 UAA1031
 4822 209 72359 UPD4364C-20L
 4822 209 71754 UPD8041
 4822 209 72638 UPD8155HC-2
 5322 209 70336 UPD8255AC-5

TRANSISTORS

5322 130 44476 BC264A
 4822 130 41066 BC264B
 4822 130 60711 BC264C
 4822 130 41327 BC327-40
 5322 130 44647 BC368
 5322 130 44593 BC369
 4822 130 40937 BC548B
 4822 130 41041 BC637
 4822 130 41087 BC638
 4822 130 42133 BC817
 4822 130 42804 BC817-25
 4822 130 60511 BC847B
 5322 130 41982 BC848B
 5322 130 42136 BC848C
 4822 130 42711 BC849B
 4822 130 42614 BC849C
 5322 130 41983 BC858B
 4822 130 60514 BC859B
 4822 130 60516 BC859C
 4822 130 40823 BD135
 4822 130 40824 BD136
 4822 130 60089 BD436
 4822 130 40982 BD437
 4822 130 40995 BD438
 5322 130 44744 BF256B
 4822 130 44237 BF450
 4822 130 44195 BF494
 4822 130 41376 BF494B
 4822 130 42131 BF550
 4822 130 60515 BF992
 5322 130 44343 BFR30
 4822 130 41801 BFR54
 4822 130 42353 BFS19
 5322 130 44093 BSV78
 5322 130 34044 BSV80

DIODES

4822 130 30621 1N4148
 5322 130 31928 BAS16
 4822 130 31983 BAT85
 4822 130 32227 BB112
 5322 130 31684 BB809
 5322 130 81178 BYR29-800
 5322 130 34865 BZV46-1V5
 4822 130 31248 BZV46-2V0
 4822 130 34048 BZX75-C2V8
 5322 130 31937 BZX84-C4V7
 4822 130 80125 BZX84-C5V6
 4822 130 81216 BZX84B10 (THCF)
 4822 130 33707 BZX84B6V2 (THCF)
 4822 130 80114 HZ4A2
 4822 130 32843 HZ4B2
 4822 130 80109 HZ4C3
 4822 130 32986 HZ5B1
 4822 130 32697 HZ6A3
 4822 130 32698 HZ6C2
 4822 130 33294 HZ9A2
 4822 130 80644 OF965
 4822 130 41594 PH2369
 4822 130 81217 TLSV5100

RESISTORS

MRS25 Resistors

4822 116 80204	150R
4822 116 52924	680E
4822 116 52438	5K6
4822 116 52238	12KE
5322 116 53732	20KE
4822 116 53534	24KE
4822 116 52471	43KE
4822 116 52973	100KE
5322 116 53345	169KE

Chip Resistors

4822 111 90163	0E
4822 111 30483	1E
4822 111 30487	1E5
4822 111 30492	2E2
4822 111 30499	4E7
4822 111 30508	10E
4822 111 30513	15E
4822 111 90171	20E
4822 111 90178	20E
4822 111 90339	20E
4822 111 30517	22E
4822 111 30519	27E
4822 111 90357	33E
4822 111 90361	39E
4822 111 90217	47E
5322 111 90098	50E
5322 111 90306	50E
4822 111 30528	56E
5322 111 90113	60E
4822 111 90203	68E
5322 111 90109	70E
4822 111 90154	70E
4822 111 90162	80E
5322 111 90242	80E
5322 111 90138	90E
5322 111 90091	100E
4822 111 90156	300E
4822 111 90372	910E
5322 111 90092	1kE
5322 111 90096	1k2
4822 111 90151	1k5
5322 111 90101	1k8
4822 111 90165	2kE
4822 111 90248	2k2
4822 111 90569	2k7
4822 111 90157	3k3
4822 111 90571	3k9
5322 111 90111	4k7
4822 111 90572	5k6
4822 111 90544	6k8
5322 111 90118	8k2
4822 111 90249	10kE
5322 111 90097	12kE
4822 111 90509	13kE
4822 111 90196	15kE
4822 111 90238	18kE
4822 111 90197	20kE
4822 111 90568	20kE
4822 111 90251	22kE
4822 111 90542	27kE
5322 111 90271	30kE
4822 111 90513	30kE
5322 111 90267	33kE
4822 111 90514	36kE
5322 111 90108	39kE
4822 111 90543	47kE
5322 111 90099	50kE
5322 111 90274	51kE
4822 111 90573	56kE
4822 111 90202	68kE
4822 111 90161	70kE
4822 111 90302	70kE
4822 111 90574	75kE
4822 111 90368	80kE
4822 111 90565	80kE
4822 111 90575	82kE
4822 111 90182	90kE
4822 111 90214	100kE
5322 111 90797	100kE
4822 111 90409	1M2
4822 111 90412	1M5
4822 111 90185	2M2

VIDEO PROCESSOR PANEL A
LIST OF ELECTRICAL PARTS
Crystals

Item	Service codenr	Description
5309	4822 242 70304	8,867238 MHz
5701	4822 242 70323	4,433619 MHz

Delay lines

5310	4822 320 40051	DL711
------	----------------	-------

Coils

5001	4822 156 11004	26.5 μ H
5002	4822 158 10101	5.3 μ H
5301	4822 157 53134	150 μ H
5302	4822 157 52874	12.5 μ H
5303	4822 157 52873	5.5 μ H
5304	4822 157 52875	66 μ H
5305	4822 157 53134	150 μ H
5306	4822 156 10995	10 μ H
5307	4822 156 10995	10 μ H
5702	4822 156 10996	15 μ H
5703	4822 156 10996	15 μ H

PTC Resistors

3840	4822 116 40029	3E7 60V
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Potentiometers

3118	4822 100 10254	1kE
3213	4822 100 10598	47kE
3327	4822 100 10359	220E
3408	4822 100 10254	1kE
3536	4822 100 10254	1kE
3539	4822 100 10254	1kE
3545	4822 100 10254	1kE
3550	4822 100 10254	1kE

Fuse Resistors

3109	4822 111 30508	10E
3232	4822 111 30508	10E
3334	4822 111 30508	10E
3637	4822 111 30508	10E

NFR25 Resistors

3857	4822 111 30492	2E2
3860	4822 111 30492	2E2
3901	4822 111 30483	1E
3902	4822 111 30483	1E
3903	4822 111 30483	1E

Capacitors

Item	Service codenr	Description
2001	4822 121 43066	1nF 1% 400V
2002	4822 121 43066	1nF 1% 400V
2003	4822 121 43066	1nF 1% 400V
2004	4822 122 31746	1000pF 5% 50V
2006	5322 121 50999	470pF 1% 400V
2007	4822 122 31775	680pF 5% 50V
2008	4822 122 31773	560pF 5% 50V
2010	4822 122 33104	100nF 10% 63V
2011	4822 124 40963	33 μ F 20% 10V
2012	4822 122 33104	100nF 10% 63V
2013	4822 124 22027	47 μ F 20% 25V
2014	4822 122 33104	100nF 10% 63V
2101	5322 121 50999	470pF 1% 400V
2102	4822 122 33064	330nF 20% 25V
2103	4822 124 22029	2,2 μ F 20% 63V
2104	4822 124 22027	47 μ F 20% 25V
2105	5322 124 21749	10 μ F 20% 63V
2106	4822 122 32891	68nF 20% 50V
2107	4822 122 31797	22nF 10% 63V
2108	4822 122 31797	22nF 10% 63V
2110	4822 121 51413	10nF 2% 63V

2112	4822 122 31765	100pF 5% 50V
2201	4822 122 33104	100nF 10% 63V
2202	4822 122 31797	22nF 10% 63V
2203	4822 122 32442	10nF 50V
2204	4822 122 33104	100nF 10% 63V
2205	4822 121 51051	4.7nF 1% 160V
2208	4822 122 31797	22nF 10% 63V
2209	4822 122 32927	330nF 20% 25V
2210	4822 124 20231	4,7 μ F 20% 63V
2211	4822 121 41898	560nF 10% 250V
2212	4822 122 32442	10nF 50V
2215	5322 124 21711	100 μ F 20% 25V
2216	4822 122 31797	22nF 10% 63V
2217	4822 122 31971	10pF 10% 50V
2218	4822 121 51255	390pF 5% 400V
2220	4822 121 51288	100pF 630V
2301	4822 124 22027	47 μ F 20% 25V
2302	5322 124 21643	22 μ F 20% 40V
2303	4822 122 31766	120pF 5% 50V
2304	4822 122 31965	220pF 5% 63V
2305	4822 122 31746	1000pF 5% 50V
2306	4822 122 32506	5,6pF 5% 50V
2307	5322 124 21643	22 μ F 20% 40V
2308	4822 122 33064	330nF 20% 25V
2310	4822 124 20947	3,3 μ F 20% 16V
2312	4822 122 31783	2700pF 10% 50V
2313	4822 125 50088	27pF
2314	4822 122 31916	5,6nF 10% 50V
2317	4822 122 32183	56nF 10% 50V
2318	4822 122 31727	470pF 5% 63V
2319	5322 124 10512	68 μ F 20% 16V
2320	4822 122 31797	22nF 10% 63V
2321	4822 122 31797	22nF 10% 63V
2322	4822 122 32442	10nF 50V
2325	4822 122 32927	330nF 20% 25V
2326	4822 121 41719	1 μ F 10% 100V
2327	4822 121 41719	1 μ F 10% 100V
2328	4822 122 31961	68 pF 10% 50V
2329	4822 122 31961	68 pF 10% 50V
2330	5322 122 31844	330pF 10% 63V
2331	4822 122 31765	100pF 5% 50V
2332	4822 122 31765	100pF 5% 50V
2333	4822 122 33104	100nF 10% 63V
2401	4822 124 22029	2,2 μ F 20% 63V
2402	4822 124 22027	47 μ F 20% 25V
2403	5322 124 21749	10 μ F 20% 63V
2404	4822 122 32891	68nF 20% 50V
2405	4822 122 31797	22nF 10% 63V
2409	4822 122 31797	22nF 10% 63V
2410	5322 124 21749	10 μ F 20% 63V
2411	4822 122 33104	100nF 10% 63V
2502	4822 122 33325	470nF 20% 16V
2503	5322 124 21749	10 μ F 20% 63V
2504	4822 122 33325	470nF 20% 16V
2601	4822 122 33064	330nF 20% 25V
2602	4822 122 33104	100nF 10% 63V
2603	4822 122 33104	100nF 10% 63V
2604	5322 124 21643	22 μ F 20% 40V
2605	4822 122 31797	22nF 10% 63V
2606	4822 122 31797	22nF 10% 63V
2607	4822 122 31797	22nF 10% 63V
2608	5322 124 21711	100 μ F 20% 25V
2609	4822 122 31746	1000pF 5% 50V
2701	4822 122 33325	470nF 20% 16V
2702	4822 122 33325	470nF 20% 16V
2703	4822 124 22027	47 μ F 20% 25V
2704	5322 122 31848	33nF 10% 63V
2705	4822 122 32444	33pF 5% 50V
2706	4822 122 31797	22nF 10% 63V
2707	4822 122 31797	22nF 10% 63V
2708	4822 122 31797	22nF 10% 63V
2711	4822 122 31767	150pF 5% 50V
2712	4822 122 31769	18pF 5% 50V
2713	4822 125 50062	10pF
2714	4822 122 31767	150pF 5% 50V
2715	5322 122 31848	33nF 10% 63V
2716	4822 124 22027	47 μ F 20% 25V
2722	4822 122 31797	22nF 10% 63V
2723	5322 124 10512	68 μ F 20% 16V
2801	4822 121 41757	470nF 10% 63V
2802	4822 122 32442	10nF 50V
2803	4822 122 31783	2700pF 10% 50V

2804	5322	124	21643	22 μ F	20%	40V
2805	5322	124	21643	22 μ F	20%	40V
2807	5322	124	21976	10 μ F	20%	25V
2808	4822	122	31644	2,2nF	10%	63V
2811	4822	122	32442	10nF		50V
2812	4822	122	32927	220nF	20%	
2813	4822	124	22031	4,7 μ F	20%	63V
2814	4822	124	20688	33 μ F	50%	16V
2815	4822	124	22027	47 μ F	20%	25V
2816	4822	124	22027	47 μ F	20%	25V
2901	4822	124	22335	220 μ F	20%	25V
2902	4822	124	22335	220 μ F	20%	25V
2903	4822	124	22335	220 μ F	20%	25V
2904	5322	124	21643	22 μ F	20%	40V
2905	4822	122	33724	120nF	20%	50V
2906	4822	124	20688	33 μ F	50%	16V
2907	4822	122	33104	100nF	10%	63V
2910	4822	124	22335	220 μ F	20%	25V
2911	4822	124	22335	220 μ F	20%	25V
2912	5322	124	21711	100 μ F	20%	25V

RADIAL & TBC PANEL B

LIST OF ELECTRICAL PARTS

Coils

Item	Service codenr	Description
5410	4822 156 11002	7.7 μ H
5470	4822 156 10998	3.0 μ H
5471	4822 156 11001	6.0 μ H
5472	4822 156 11001	6.0 μ H
5473	4822 156 11001	6.0 μ H
5474	4822 156 11001	6.0 μ H
5475	4822 156 11001	6.0 μ H
5476	4822 156 10998	3.0 μ H

Potentiometers

3400	5322 101 14008	2K2
3419	4822 100 10254	1K
3484	4822 100 10254	1K
3490	5322 101 14069	22K

PTC Resistors

3033	4822 116 40026	5.6E
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Fuse Resistors

3401	4822 111 30513	15E
3402	4822 111 30517	22E
3404	4822 111 30517	22E

NFR25 Resistors

3403	4822 111 30492	2E2
3090	4822 111 30492	2E2
3093	4822 111 30492	2E2

Capacitors

2003	4822 122 31974	820pF 10% 50V
2010	4822 121 43101	6.8nF 1% 63V
2011	4822 121 41785	270nF 10% 100V
2012	4822 122 31644	2.2nF 10% 63V
2013	4822 122 32444	33pF 5% 50V
2014	4822 122 32927	220nF 20%
2015	5322 122 31848	33nF 10% 63V
2020	4822 124 22027	47 μ F 20% 25V
2021	4822 124 22027	47 μ F 20% 25V
2022	5322 122 31848	33nF 10% 63V
2023	5322 122 31848	33nF 10% 63V
2371	4822 121 42245	220nF 10% 63V
2372	4822 122 32541	27nF 10% 50V
2373	4822 122 32541	27nF 10% 50V
2401	5322 124 21711	100 μ F 20% 25V
2402	4822 122 33104	100nF 10% 63V
2403	5322 124 21711	100 μ F 20% 25V
2404	4822 122 33104	100nF 10% 63V

Item	Service codenr	Description
2405	4822 122 33104	100nF 10% 63V
2406	5322 124 21711	100 μ F 20% 25V
2407	4822 122 33104	100nF 10% 63V
2408	4822 124 22027	47 μ F 20% 25V
2410	5322 124 21643	22 μ F 20% 40V
2411	4822 122 31767	150pF 5% 50V
2412	4822 122 31767	150pF 5% 50V
2413	4822 122 32927	220nF 20%
2414	4822 124 22188	3.3 μ F 20% 63V
2415	4822 124 22188	3.3 μ F 20% 63V
2416	5322 124 21749	10 μ F 20% 63V
2417	4822 122 32442	10nF 50V
2418	5322 124 21749	10 μ F 20% 63V
2419	4822 122 32442	10nF 50V
2420	5322 124 21749	10 μ F 20% 63V
2421	4822 122 32139	12pF 5% 63V
2422	4822 122 31797	22nF 10% 63V
2423	4822 122 31797	22nF 10% 63V
2424	4822 122 31797	22nF 10% 63V
2425	4822 122 31797	22nF 10% 63V
2426	4822 122 31797	22nF 10% 63V
2430	4822 122 31797	22nF 10% 63V
2431	4822 122 33104	100nF 10% 63V
2432	4822 122 33104	100nF 10% 63V
2433	4822 124 22027	47 μ F 20% 25V
2436	4822 124 22028	1 μ F 20% 63V
2437	4822 122 31797	22nF 10% 63V
2438	4822 122 32142	270pF 5% 63V
2440	5322 124 21749	10 μ F 20% 63V
2441	4822 122 32442	10nF 50V
2442	4822 122 32442	10nF 50V
2449	4822 122 33104	100nF 10% 63V
2450	4822 122 33104	100nF 10% 63V
2451	4822 122 33104	100nF 10% 63V
2452	4822 122 33104	100nF 10% 63V
2460	5322 124 21643	22 μ F 20% 40V
2461	5322 124 21643	22 μ F 20% 40V
2462	4822 124 22031	4.7 μ F 20% 63V
2471	4822 122 31797	22nF 10% 63V
2472	4822 122 31797	22nF 10% 63V
2473	4822 122 31772	47pF 5% 50V
2474	4822 122 31972	39pF 5% 50V
2480	4822 122 31767	150pF 5% 50V
2490	5322 124 21749	10 μ F 20% 63V
2491	4822 122 33104	100nF 10% 63V
2492	4822 122 31746	1000pF 5% 50V
2493	4822 122 31797	22nF 10% 63V
2494	4822 122 31797	22nF 10% 63V

HF & AUDIO PANEL C

LIST OF ELECTRICAL PARTS

Delay line

Item	Service codenr	Description
5401	4822 320 40081	470 ns

Filters

5106	4822 242 71658	SLC3251
5107	4822 242 71659	SLC3251

Coils

5100	4822 157 53135	205.0 μ H
5101	4822 157 53136	136.0 μ H
5102	4822 157 53137	81.0 μ H
5103	4822 157 53516	8.2 mH
5104	4822 157 53516	8.2 mH
5105	4822 156 10524	26.0 μ H
5201	4822 156 10994	87.0 μ H
5202	4822 156 21147	7.2 μ H
5203	4822 156 11011	2.6 μ H
5204	4822 156 10994	87.0 μ H
5205	4822 156 10999	4.0 μ H
5206	4822 156 21026	34.0 μ H
5207	4822 157 52871	25.0 μ H
5208	4822 157 52871	25.0 μ H
5402	4822 156 21026	34.0 μ H
5403	4822 156 11003	12.0 μ H
5404	4822 156 11007	212.0 μ H
5405	4822 156 11007	212.0 μ H
5406	4822 157 53133	100.0 μ H
5407	4822 156 10997	1.7 μ H
5601	4822 158 10101	5.3 μ H

Potentiometers

3106	5322 101 14069	22KE
3114	5322 101 14069	22KE
3123	5322 101 14069	22KE
3128	5322 101 14069	22KE
3243	4822 100 10254	1KE
3450	5322 101 14008	2k2
3465	4822 100 10254	1KE

Fuse Resistors

3153	4822 111 30526	47E
3164	4822 111 30526	47E
3241	4822 111 30517	22E

NFR25 Resistors

3235	4822 111 30542	180E
3411	4822 111 30537	120E
3435	4822 111 30537	120E
3606	4822 111 30492	2E2

Capacitors

Item	Service codenr	Description
2101	4822 122 31797	22nF 10% 63V
2102	4822 122 31797	22nF 10% 63V
2103	4822 122 32442	10nF 50V
2104	4822 122 32442	10nF 50V
2105	4822 122 31797	22nF 10% 63V
2106	4822 122 31797	22nF 10% 63V
2107	5322 124 21711	100 μ F 20% 25V
2108	5322 124 21711	100 μ F 20% 25V
2110	4822 122 33104	100nF 10% 63V
2111	4822 124 22027	47 μ F 20% 25V
2112	4822 122 33104	100nF 10% 63V
2113	4822 122 33104	100nF 10% 63V
2114	4822 124 22027	47 μ F 20% 25V
2116	4822 122 31771	390pF 5% 50V
2117	4822 122 32442	10nF 50V
2118	4822 122 31727	470pF 5% 63V
2119	4822 124 22335	220 μ F 20% 25V
2120	4822 122 31965	220pF 5% 63V

2121	4822 122 31969	3.3nF 10% 50V
2123	4822 122 31767	150pF 5% 50V
2124	4822 122 31775	680pF 5% 50V
2125	5322 122 31843	270pF 5% 63V
2126	4822 122 31916	5.6nF 10% 50V
2127	5322 124 21749	10 μ F 20% 63V
2128	4822 122 31784	4.7nF 10% 50V
2129	5322 122 31843	270pF 5% 63V
2130	4822 122 31774	56pF 5% 50V
2131	4822 122 32442	10nF 50V
2132	4822 122 32142	270pF 5% 63V
2134	4822 124 22335	220 μ F 20% 25V
2135	4822 122 31965	220pF 5% 63V
2136	4822 124 22031	4.7 μ F 20% 63V
2137	5322 122 31843	270pF 5% 63V
2138	5322 124 21749	10 μ F 20% 63V
2139	4822 122 31784	4.7nF 10% 50V
2140	5322 122 31843	270pF 5% 63V
2141	4822 122 31916	5.6nF 10% 50V
2142	4822 122 31969	3.3nF 10% 50V
2143	4822 122 31965	220pF 5% 63V
2144	4822 122 31767	150pF 5% 50V
2145	4822 122 31775	680pF 5% 50V
2146	5322 122 32838	82nF 10% 50V
2147	5322 122 32838	82nF 10% 50V
2148	5322 124 21749	10 μ F 20% 63V
2149	5322 124 21749	10 μ F 20% 63V
2150	4822 122 31971	10pF 10% 50V
2151	4822 122 31969	3.3nF 10% 50V
2152	4822 122 31971	10pF 10% 50V
2153	4822 122 31969	3.3nF 10% 50V
2154	4822 124 22029	2.2 μ F 20% 63V
2155	4822 124 22029	2.2 μ F 20% 63V
2156	4822 124 22335	220 μ F 20% 25V
2157	4822 124 22027	47 μ F 20% 25V
2158	4822 124 22027	47 μ F 20% 25V
2159	4822 122 33104	100nF 10% 63V
2160	4822 122 33104	100nF 10% 63V
2161	4822 122 33104	100nF 10% 63V
2162	4822 122 33104	100nF 10% 63V
2201	4822 122 31797	22nF 10% 63V
2202	4822 124 22027	47 μ F 20% 25V
2203	4822 122 31797	22nF 10% 63V
2204	4822 122 31961	68pF 10% 50V
2205	4822 122 31727	470pF 5% 63V
2207	4822 122 32442	10nF 50V
2208	4822 122 31797	22nF 10% 63V
2209	4822 122 31774	56pF 5% 50V
2210	4822 122 32506	5.6pF 5% 50V
2211	4822 122 31797	22nF 10% 63V
2212	4822 122 32442	10nF 50V
2213	4822 122 31797	22nF 10% 63V
2215	4822 122 31765	100pF 5% 50V
2216	4822 122 31965	220pF 5% 63V
2217	4822 122 32142	270pF 5% 63V
2218	4822 122 31797	22nF 10% 63V
2219	4822 122 31965	20pF 5% 63V
2220	4822 122 31772	47pF 5% 50V
2221	4822 122 31727	270pF 5% 63V
2222	4822 122 31797	22nF 10% 63V
2223	4822 124 22027	47 μ F 20% 25V
2224	4822 122 32442	10nF 50V
2225	4822 122 31774	56pF 5% 50V
2226	4822 122 31774	56pF 5% 50V
2227	4822 124 22027	47 μ F 20% 25V
2228	4822 122 31797	22nF 10% 63V
2229	4822 122 31644	2.2nF 10% 63V
2230	4822 122 31797	22nF 10% 63V
2231	4822 122 31797	22nF 10% 63V
2232	4822 122 31769	18pF 5% 50V
2233	4C22 122 31769	18pF 5% 50V
2234	4822 122 31797	22nF 10% 63V
2235	4822 122 32444	33pF 5% 50V
2236	4822 122 32505	2.7pF 5% 50V
2237	4822 122 31774	56pF 5% 50V
2238	4822 122 32504	15pF 5% 50V
2239	4822 122 31774	56pF 5% 50V
2240	4822 122 32139	12pF 5% 63V
2242	4822 124 22187	15 μ F 20% 63V
2243	4822 122 32444	33pF 5% 50V
2244	4822 122 31797	22nF 10% 63V
2401	4822 122 32082	4.7pF 5% 50V

2402	4822	124	22027	47 μ F	20%	25V
2403	4822	122	31797	22nF	10%	63V
2404	5322	124	21749	10 μ F	20%	63V
2405	5322	124	21749	10 μ F	20%	63V
2406	4822	122	33104	100nF	10%	63V
2407	4822	122	31797	22nF	10%	63V
2408	4822	122	31797	22nF	10%	63V
2409	4822	122	31727	470pF	5%	63V
2410	4822	122	31765	100pF	5%	50V
2411	4822	122	31797	22nF	10%	63V
2413	4822	122	31746	1000pF	5%	50V
2414	4822	122	31797	22nF	10%	63V
2415	4822	124	22027	47 μ F	20%	25V
2416	4822	124	22029	2.2 μ F	20%	63V
2417	4822	122	31765	100pF	5%	50V
2418	4822	122	31765	100pF	5%	50V
2419	4822	122	31797	22nF	10%	63V
2420	4822	121	41719	1 μ F	10%	100V
2421	4822	122	32442	10nF		50V
2422	4822	122	32442	10nF		50V
2423	4822	122	31797	22nF	10%	63V
2424	4822	124	22031	4.7 μ F	20%	63V
2425	4822	124	22028	1 μ F	20%	63V
2426	4822	122	31797	22nF	10%	63V
2427	4822	122	33104	100nF	10%	63V
2428	4822	122	31765	100pF	5%	50V
2429	4822	122	31765	100pF	5%	50V
2430	4822	122	31797	22nF	10%	63V
2431	4822	124	22027	47 μ F	20%	25V
2432	4822	122	33668	270nF	20%	25V
2433	4822	122	31797	22nF	10%	63V
2434	4822	122	32482	22pF	5%	63V
2435	4822	122	31797	22nF	10%	63V
2436	4822	122	31797	22nF	10%	63V
2437	4822	122	31797	22nF	10%	63V
2439	4822	122	31797	22nF	10%	63V
2440	4822	122	31961	68pF	10%	50V
2601	4822	122	31775	680pF	5%	50V
2602	4822	121	51154	3.9nF	1%	160V
2607	4822	124	22027	47 μ F	20%	25V
2608	4822	124	22027	47 μ F	20%	25V

MOTORSEQUENCE & TBC PANEL D

LIST OF ELECTRICAL PARTS

Crystals

Item	Service codenr	Description
5201	4822 242 70361	4,5 MHz

Coils

5320	4822 156 11003	12.0 μ H
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Fuse Resistors

3076	4822 111 30528	56E
3077	4822 111 30528	56E
3086	4822 111 30528	56E
3087	4822 111 30528	56E
3096	4822 111 30528	56E
3097	4822 111 30528	56E
3108	4822 111 30499	4E7
3109	4822 111 30499	4E7
3110	4822 111 30499	4E7
3201	4822 111 30492	2E2
3202	4822 111 30513	15E
3204	4822 111 30513	15E
3205	4822 111 30492	2E2
3215	4822 111 30517	22E

Capacitors

2005	4822 122 33104	100nF	10%	63V
2006	4822 122 31746	1000pF	5%	50V
2007	4822 122 31746	1000pF	5%	50V
2008	4822 122 31746	1000pF	5%	50V
2009	4822 124 22027	47 μ F	20%	25V
2020	5322 122 31848	33nF	10%	63V
2030	4822 121 50591	1nF	1%	630V
2031	4822 122 33104	100nF	10%	63V
2032	4822 124 22027	47 μ F	20%	25V
2033	4822 122 32139	12pF	5%	63V
2053	4822 124 21315	6,8 μ F	20%	16V
2054	4822 124 22027	47 μ F	20%	25V
2070	4822 122 31969	3,3nF	10%	50V
2071	4822 122 31969	3,3nF	10%	50V
2080	4822 122 31969	3,3nF	10%	50V
2081	4822 122 31969	3,3nF	10%	50V
2090	4822 122 31969	3,3nF	10%	50V
2091	4822 122 31969	3,3nF	10%	50V
2092	5322 122 31848	33nF	10%	63V
2101	4822 122 33104	100nF	10%	63V
2103	4822 122 33104	100nF	10%	63V
2105	4822 122 33104	100nF	10%	63V
2110	4822 124 22027	47 μ F	20%	25V
2112	4822 124 41686	47 μ F	20%	63V
2113	4822 124 22027	47 μ F	20%	25V
2114	4822 124 22027	47 μ F	20%	25V
2116	4822 122 33104	100nF	10%	63V
2118	5322 122 31848	33nF	10%	63V
2119	5322 122 31848	33nF	10%	63V
2122	5322 122 31848	33nF	10%	63V
2123	5322 122 31848	33nF	10%	63V
2200	4822 124 22027	47 μ F	20%	25V
2201	4822 124 22027	47 μ F	20%	25V
2202	4822 124 22027	47 μ F	20%	25V
2204	4822 122 33147	22nF	20%	
2208	4822 124 22027	47 μ F	20%	25V
2210	4822 124 22027	47 μ F	20%	25V
2211	5322 122 31848	33nF	10%	63V
2212	4822 122 33668	270nF	20%	25V
2213	4822 122 31727	470pF	5%	63V
2214	4822 122 31765	100pF	5%	50V
2215	4822 125 50062	10pF		
2216	4822 122 32148	5,6pF	5%	100V
2219	4822 122 33142	6,8pF	2%	100V
2222	4822 122 33104	100nF	10%	63V
2223	4822 121 51111	2,4nF	2%	250V
2228	4822 122 31783	2700pF	10%	50V
2241	4822 122 31727	470pF	5%	63V
2242	4822 122 31765	100pF	5%	50V
2300	4822 122 33668	270nF	20%	25V
2304	5322 122 31848	33nF	10%	63V
2305	4822 122 31727	470pF	5%	63V
2306	4822 122 31765	100pF	5%	50V
2307	4822 122 33668	270nF	20%	25V
2308	5322 122 32517	15pF	2%	100V
2309	4822 122 31774	56pF	5%	50V
2310	4822 122 31774	56pF	5%	50V
2311	4822 122 31784	4,7nF	10%	50V
2312	4822 122 31797	22nF	10%	63V
2313	4822 122 31765	100pF	5%	50V
2314	4822 122 31767	150pF	5%	50V
2315	4822 122 31783	2700pF	10%	50V
2317	4822 122 31797	22nF	10%	63V
2320	4822 122 31783	2700pF	10%	50V
2330	4822 122 31797	22nF	10%	63V
2331	4822 122 31746	1000pF	5%	50V
2332	4822 122 32482	22pF	5%	63V
2333	4822 122 31775	680pF	5%	50V
2334	5322 122 31844	330pF	10%	63V
2340	4822 122 31972	39pF	5%	50V
2341	4822 122 31772	47pF	5%	50V
2342	4822 122 32542	47nF	10%	50V
2350	4822 122 31746	1000pF	5%	50V
2351	4822 122 32142	270pF	5%	63V
2352	4822 121 51051	4,7nF	1%	160V
2353	4822 124 22027	47 μ F	20%	25V
2354	4822 122 32891	68nF	20%	50V
2356	4822 122 31971	10pF	10%	50V
2357	4822 122 31765	100pF	5%	50V
2360	4822 124 22027	47 μ F	20%	25V
2380	4822 122 33147	22nF	20%	
2381	4822 122 33147	22nF	20%	
2382	4822 122 33147	22nF	20%	
2383	4822 122 33147	22nF	20%	
2384	4822 122 33147	22nF	20%	
2385	4822 122 33147	22nF	20%	
2386	4822 122 33147	22nF	20%	
2388	4822 122 33668	270nF	20%	25V
2392	4822 122 32142	270pF	5%	63V
2395	4822 122 33147	22nF	20%	
2397	4822 122 31797	22nF	10%	63V

CONTROL & DRIVE PANEL SR

LIST OF ELECTRICAL PARTS

Eeprom (programmed)

Item	Service codenr	Description	Item	Service codenr	Description
7104	4822 209 73858	EPROM 7104+PROGRAM	2023	4822 122 33147	22nF 20%
7105	4822 209 73859	EPROM 7105+PROGRAM	2024	4822 122 33147	22nF 20%
Crystals			2025	4822 122 33147	22nF 20%
5101	4822 242 71845	120,0 MHz	2026	4822 122 33147	22nF 20%
5102	4822 242 70917	11,059 MHz	2027	4822 122 33147	22nF 20%
5103	4822 242 70668	4,0 MHz	2028	4822 122 33147	22nF 20%
Coils			2029	4822 122 33147	22nF 20%
5001	4822 158 10101	5,3 μ H	2030	4822 122 33147	22nF 20%
5002	4822 158 10101	5,3 μ H	2031	4822 122 33147	22nF 20%
5003	4822 158 10101	5,3 μ H	2032	4822 122 33147	22nF 20%
5004	4822 157 53905	120.0 μ H	2033	4822 122 33147	22nF 20%
Resistor networks			2034	4822 122 33147	22nF 20%
3101	5322 111 90431	4610X-101-103	2035	4822 122 33147	22nF 20%
3102	5322 111 90431	4610X-101-103	2036	4822 122 33147	22nF 20%
3103	5322 111 90431	4610X-101-103	2037	4822 122 33147	22nF 20%
3104	5322 111 90431	4610X-101-103	2038	4822 122 32482	22pF 5% 63V
3105	5322 111 90797	4610X-101-104	2039	4822 122 31972	39pF 5% 50V
NFR25 Resistors			2040	4822 122 31644	2,2nF 10% 63V
3014	4822 111 30487	1E5	2041	4822 122 31644	2,2nF 10% 63V
Capacitors			2042	4822 122 31644	2,2nF 10% 63V
2001	4822 122 33147	22nF 20%	2044	4822 122 32444	33pF 5% 50V
2002	4822 122 33147	22nF 20%	2045	4822 122 32444	33pF 5% 50V
2003	4822 122 33147	22nF 20%	2046	4822 122 32444	33pF 5% 50V
2004	4822 122 33147	22nF 20%	2047	4822 122 32444	33pF 5% 50V
2005	4822 122 33147	22nF 20%	2048	4822 122 32482	22pF 5% 63V
2006	4822 122 33147	22nF 20%	2049	4822 122 32482	22pF 5% 63V
2007	4822 122 33147	22nF 20%	2050	4822 122 31727	470pF 5% 63V
2008	4822 122 33147	22nF 20%	2051	4822 122 31727	470pF 5% 63V
2009	4822 122 33147	22nF 20%	2054	4822 122 32504	15pF 5% 50V
2010	4822 122 33147	22nF 20%	2055	4822 124 22027	47 μ F 20% 25V
2011	4822 122 33147	22nF 20%	2056	4822 124 22027	47 μ F 20% 25V
2012	4822 122 33147	22nF 20%	2057	4822 124 22027	47 μ F 20% 25V
2013	4822 122 33147	22nF 20%	2058	4822 124 22027	47 μ F 20% 25V
2014	4822 122 33147	22nF 20%	2059	5322 124 21643	22 μ F 20% 40V
2015	4822 122 33147	22nF 20%	2060	4822 124 22031	4,7 μ F 20% 63V
2016	4822 122 33147	22nF 20%	2061	5322 124 21643	22 μ F 20% 40V
2017	4822 122 33147	22nF 20%	2062	4822 124 22027	47 μ F 20% 25V
2018	4822 122 33147	22nF 20%	2063	4822 124 22027	47 μ F 20% 25V
2019	4822 122 33147	22nF 20%	2064	4822 124 22029	2,2 μ F 20% 63V
2020	4822 122 33147	22nF 20%			
2021	4822 122 33147	22nF 20%			
2022	4822 122 33147	22nF 20%			

POWER SUPPLY PANEL F

LIST OF ELECTRICAL PARTS

Fuses

Item	Service codenr	Description
F 401	4822 253 10048	3.15 A
F 601	4822 253 10052	1 A
F1001	4822 253 10052	1 A
F1101	4822 253 10052	1 A
F1102	4822 253 10052	1 A

Optocoupler

H501	4822 130 10025	CNX82A
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Transformer

T901	4822 146 30748	Power Trafo
------	----------------	-------------

Coils

L 201	4822 152 20685	15 μ H
L 301	5322 157 52513	10 μ H
L 401	5322 157 52513	10 μ H
L1001	4822 152 20685	15 μ H

Potentiometers

R119	4822 101 10793	5kE
R508	4822 101 10792	1kE
R605	4822 101 10792	1kE
R805	4822 101 10792	1kE

Wirewound Resistors

R122	4822 2112 41098	470 E
R124	4822 2112 41098	470 E

NFR25 Resistors

R104	4822 111 30508	10 E
R106	4822 111 30531	68 E
R107	4822 111 30553	470 E
R108	4822 111 30544	220 E
R111	4822 111 30499	4E7
R112	4822 111 30499	4E7
R116	4822 111 30499	4E7
R117	4822 111 30499	4E7
R123	4822 111 30561	1kE
R126	4822 111 30499	4E7
R504	4822 111 30531	68 E
R702	4822 111 30531	68 E

VR37 Resistors

R1104	5322 116 60459	220kE
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PR37 Resistors

R 114	4822 116 51098	100 E
R 131	4822 116 51848	15kE
R 132	4822 116 51848	15kE
R 133	4822 116 51848	15kE
R 134	4822 116 51848	15kE
R 136	4822 116 51098	100 E
R1001	4822 116 51167	33 E

NTC Resistors

R1103	4822 116 30333	10 E
-------	----------------	------

Capacitors

C 101	5322 121 42386	100nF 10% 63V
C 102	4822 121 51431	2,2 μ F 20% 35V
C 103	4822 121 51432	68 μ F 20% 6,3V
C 104	4822 121 41857	10nF 10% 100V
C 106	4822 121 51184	680pF 10% 1600V
C 107	5322 121 41796	2,2nF 10% 1000V
C 201	4822 124 41329	2200 μ F 20% 35V
C 202	4822 124 41329	2200 μ F 20% 35V
C 203	5322 121 42386	100nF 10% 63V
C 301	4822 124 41329	2200 μ F 20% 35V
C 302	4822 124 41329	2200 μ F 20% 35V
C 303	5322 121 42386	100nF 10% 63V
C 304	4822 124 41329	2200 μ F 20% 35V
C 401	4822 124 41458	4700 μ F 20% 16V
C 402	4822 124 41458	4700 μ F 20% 16V
C 403	5322 121 42386	100nF 10% 63V
C 404	4822 124 41458	4700 μ F 20% 16V
C 501	4822 121 43078	22nF 10% 100V
C 502	4822 121 43079	4,7nF 10% 100V
C 601	4822 121 43079	4,7nF 10% 100V
C 602	5322 121 42386	100nF 10% 63V
C 604	4822 121 43078	22nF 10% 100V
C 607	4822 124 41393	220 μ F 20% 25V
C 701	5322 121 42386	100nF 10% 63V
C 801	4822 121 41857	10nF 10% 100V
C 802	4822 124 41393	220 μ F 20% 25V
C 803	5322 121 42386	100nF 10% 63V
C 804	4822 121 43079	4,7nF 10% 100V
C 806	5322 121 41796	2,2nF 10% 1000V
C 901	4822 122 31938	4,7nF 20% 400V
C1001	4822 124 41458	4700 μ F 20% 16V
C1002	4822 124 41393	220 μ F 20% 25V
C1003	5322 121 42386	100nF 10% 63V
C1101	5322 121 41731	600nF 20% 250V
C1104	4822 122 32576	2,2nF 20% 400V
C1105	4822 122 32576	2,2nF 20% 400V
C1106	4822 124 41455	220 μ F 20% 200V
C1107	4822 124 41455	220 μ F 20% 200V
C1108	5322 121 42461	100nF 20% 250V

KEYBOARD MODULE N

LIST OF ELECTRICAL PARTS

Switch

4822 276 10974 Switch

Diodes

4822 130 81217 LED Bi-colour

FRONT LOADER PANEL P

LIST OF ELECTRICAL PARTS

NFR Resistors

3010 4822 111 30483 1E

Capacitors

2001	4822 124 22027	47 μ F 20% 25V
2002	4822 124 22031	4,7 μ F 20% 63V

Repair method

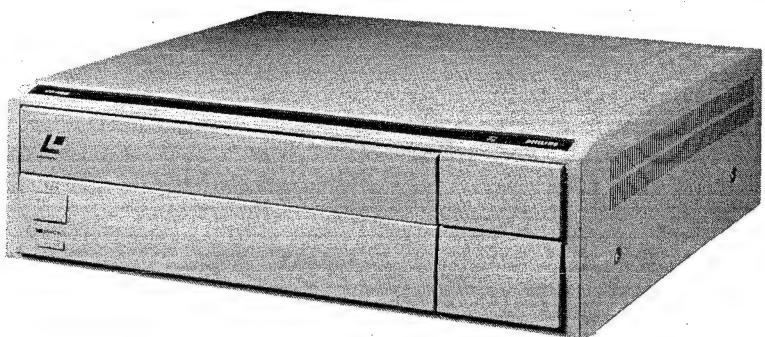
Chapter 6

Standard LaserVision disc drive VP406

Service
Service
Service



00/05/23/30



42 047 A12

Repair Method

Contents:

1. Introduction
2. Diagnostic Software
 - a. Set-up
 - b. Switching on the Diagnostic Software
 1. Check mode
 2. Self-test mode
 - c. Reproducing the error codes on the screen
 1. Check mode
 2. Self-test mode
 - d. Programme loop in the self-test mode
 - e. Meaning of the error codes
3. Faultfinding
 - a. Meaning of the symbols used
 - b. Test procedure



PHILIPS

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Repair Method

1. Introduction

The object of this repair method is to facilitate faultfinding in a defective set for the service technician. The method is set up in such a way that the fault diagnosis in a set under repair is made via a test procedure. In this test procedure several operations should be carried out sequentially and decisions should be made on various points. Via a yes/no decision, the technician is led to a defective module or part of it. A central role in the repair method is played by the Diagnostic Software, which has been implemented in the Drive Processor.

2. Diagnostic Software

In the control of the various functions in the set, an important role is played by the Drive Processor. For this reason the diagnostic software forms an integral part of the drive software of this module.

a. Set-up

The diagnostic software has been integrated in the drive software in such a way that many of the tasks of the drive are checked for proper performance. If a fault is detected in the execution of a task, an error code is shown on the screen as video overlay.

The error code meets the following priority rule:

1 – 30 fatal fault
31 – 59 major fault
60 – 80 behaviour fault
81 – 99 minor fault
100 – 254 for development
255 initial value (Display ---)

The lower the error code, the more serious the fault.

b. Switching on the Diagnostic Software

A fault can be detected in two different modes:

1. Check mode

The error code is shown on the screen during manual- or computercontrolled use.

You can enable this check mode by switching on the mains switch while keeping the STAND-BY key on the front panel depressed. Do not release the STAND-BY key until 3 horizontal stripes are visible in the right-hand bottom corner of the picture screen.

2. Self-test mode

Now the drive is controlled in a programme loop while the normal operating functions are inoperative.

You can enable the self-test mode by pressing the mains switch while keeping both the EJECT and the STAND-BY key depressed. Do not release the two keys until the word DIAGNOSTICS appears on the screen.

Now the screen not only shows the error code, but also the position of the loop counter and the text DIAGNOSTICS.

The occurrence of minor faults (error code > 60) does not influence the execution of the programme loops; on the other hand, faults having an error code < 60 will interrupt the programme loop and switch the drive into position STAND-BY while keeping the last LDU-slide position.

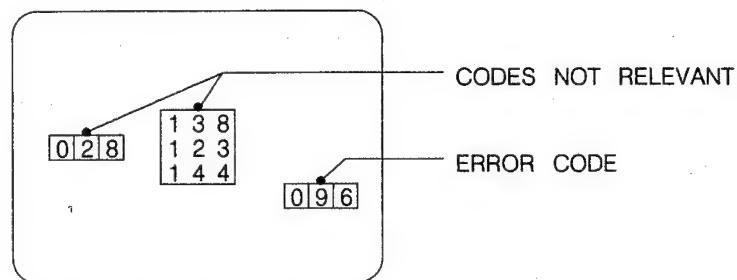
Both modes are reset again after the mains switch is switched off.

It is advisable to switch off the set only when it is in STAND-BY mode.

c. Reproducing the error codes on the screen

The error code is shown as video overlay on the screen as follows:

1. Check mode

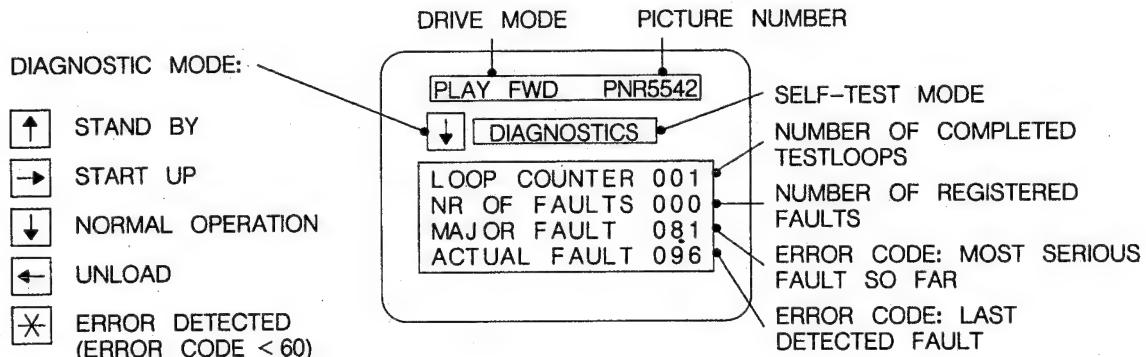


CHECK MODE

The error code is shown in the right-hand bottom corner of the screen.

This is the last detected fault.

2. Self-test mode



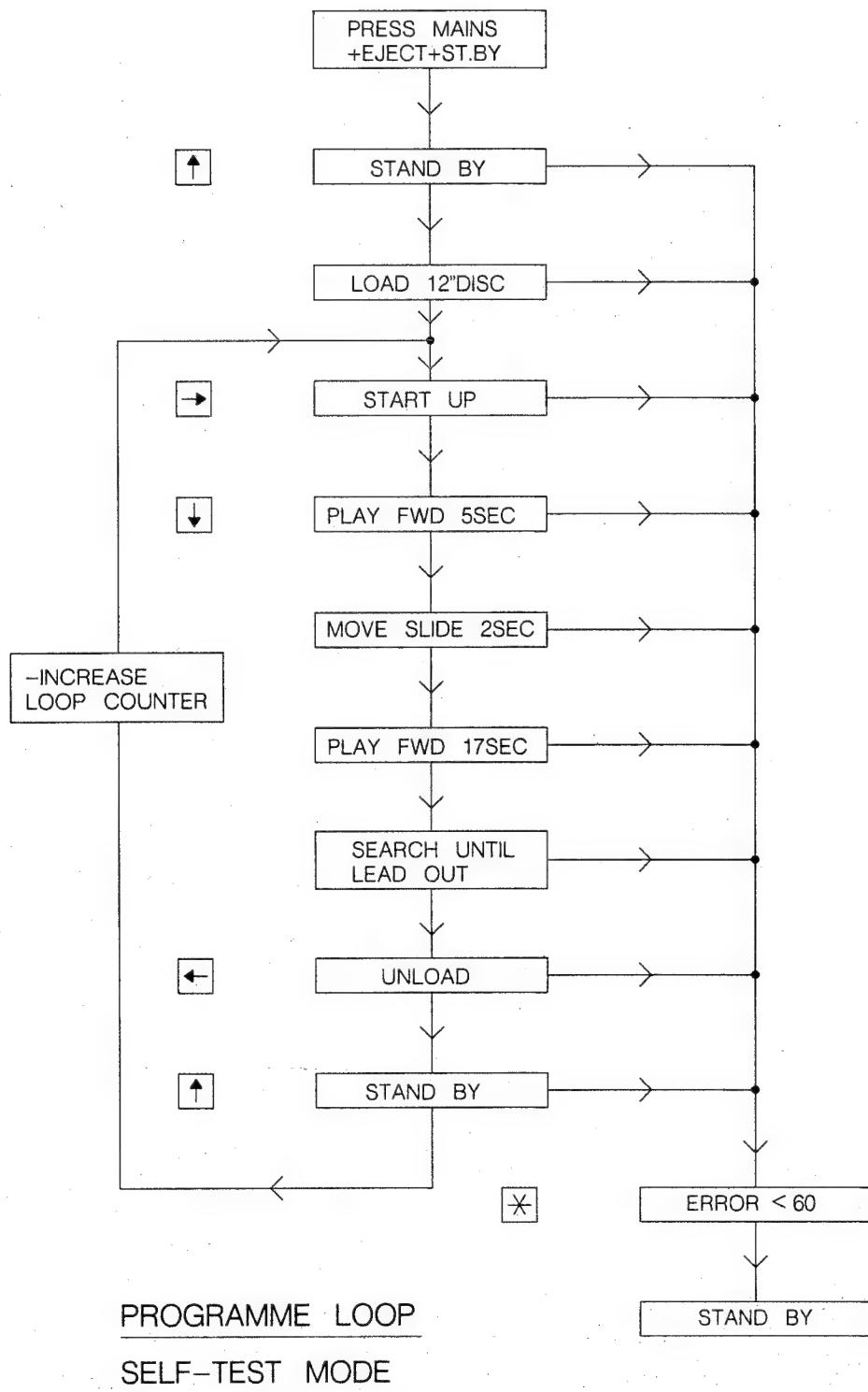
SELF-TEST MODE

MDA.00615
T27/716

By displaying the text DIAGNOSTICS, the screen indicates that the set is in self-test mode. It also shows the drive mode and the diagnostic mode. In the middle of the screen the position of the loop counter and the number of registered faults are given. The error codes are divided into major and actual faults. The code for a major fault shown on the screen will only be overwritten if the new code has priority (that is, a lower error code).

d. Programme loop in the self-test mode

The following flow-chart shows what operations are carried out by the diagnostic software on behalf of the programme loop.



MDA.01150
T33/752

e. *Meaning of the error codes*

The survey below gives the meaning of the error codes shown on the picture screen. A detailed description of these error codes and a possible fault cause is assimilated in the subsequent repair method.

For the player and thus for the control system, two essential modes can be distinguished.

- The player is playing (MAIN 1)
- The player is not playing (MAIN 0)

In the first mode, the player has been started and is executing all kinds of commands such as play forward, jump pause, etc. The second mode applies during LOAD, UNLOAD, EJECT and STANDBY (motor and laser off).

An additional situation in which the player may function is the diagnostic mode, also called MAIN 2.

In table 1 the error codes lower than 60 are described. If the corresponding faults occur, the player will adopt the standby mode. These error codes have been elaborated into faultfinding trees, see 3b, block 2.

Error code	Description of error
error code	description of error
1	tray is impeded in getting in or out
2	no disc reflection
3	SPI not found
4	time-out tilt
5	laser not on
6	not out focus
7	not in focus after 5x (no rotation of disc)
8	motor speed error
9	framelock
10	motor slows down
11	laser not off
12	not out of focus after unloading
13	not switched into 'standby off' (time-out 2 sec.)
14	active 0-RPM without a LV disc at start up
15	laser out during MAIN 1
16	motor error during MAIN 1
17	no focus 20 steps after focus error
20	drive board inside LV player during hardware test
25	no REFV pulse at system start-up
26	REFV period ≥ 64 msec
27	REFV pulse is not in conformity with NTSC/PAL standard
28	out of valid active video area, action: unload
29	no reference pulse
30	radial offset outside of window set to upper limit
43	radial offset outside of window set to lower limit
44	no 2ppr pulse
52	no lead-in code at start-up of player (diagnostics)
53	no active video area detected (diagnostics)
54	time-out (100 s) scan forward (diagnostics)
56	play forward error (diagnostics)
58	

Table 1

In table 2 the remaining error codes are described so that it may be an aid for complaints that do not have a clear fault cause.

Error code	Description of error
60	out of focus during 'main 1'
61	out of focus at start-up (disc rotates)
62	detection of radial mirror movements fails during instant jump
63	goto time-out
64	no valid command
65	lead-in/lead-out
66	no valid 24-bit code
67	instant jump error in one of the previous jump(s)
68	time-out during track crossing instant jump
70	error 62 during 'scan'; corr. of slide with 1 fs.
71	radial mirror sensitivity $\geq 900 \mu\text{V}$
72	radial mirror sensitivity $\geq 200 \mu\text{V}$
73	a/d converted mirror pos. min. (out of field of view)
74	a/d converted mirror pos. max. (out of field of view)
75	SPI detected during master mode & slid moves inward.
76	The slide is stopped by 'timer0'
79	SPI protection is activated apply for update of comm. pattern over zero steps
80	no 24 bits
81	no 8 or F keys
82	no valid 8 key codes
83	no valid chapter code
84	lead-in code
85	lead-out code
86	time code
87	BCD error in picture no. X2X3
88	BCD error in picture no. X4X5
89	out of lock during main1 (only detec. for CA discs)
95	no datic interrupt (no 24-bit code?)
96	time-out during start-up 'diagnostics'
99	master mode: actual slide speed \geq limited speed
110	timer 1 overflow / sw error
111	instant jump of ≥ 51 tracks (limited to 51)
112	instant jump of 0 tracks
113	selection of 'slave mode' at high speed master mode
117	hwtest activated after detection of low level pin p3.5
119	hardware test is active
120	command sequence in undefined mode (diagnostics)
121	synchronization error timing single track crossing
124	instant jump at high speed master mode (not executed)
126	instant jump during master mode (not executed)
127	error during 'step procedure'
133	re-initialisation of delay counter stand-by
137	overflow of 2 byte step converter radial movement
141	underflow of 2 byte step counter radial movement
142	instant jump & master mode active
148	re-init. delay counter stand-by
151	fault in (rough) backward timing, i.e. overflow of slice register
159	precontrol instant jump ≥ 1 step
170	precontrol error instant jump
171	

Table 2

3. Test software

For the finding of faults or fault causes in the communication between computer and disc drive via RS232, a test programme has been developed which is used as a fault-finding tool. This test programme is available on floppy disk and can be ordered under service code no. 4822 397 30173. Service always supplies the latest release.

Programme contents test software

1. Manual control

The LV disc drive can be controlled manually by sending F-codes. The player will give acknowledge, if present.

2. Automatic testing (For 12" standard CAV discs only)

an interactive test program will be started by selecting "2".

The player will be tested on:

- step forward/reverse
- play forward/reverse
- slow forward/reverse
- fast forward/reverse
- audio/video on/off
- instant jump
- internal/external audio/video (if applicable)
- chapter search (if present)

This program can be stopped by pressing <ctrl> + <break>.

At the end of the program a summary is given whether the test has passed or failed.

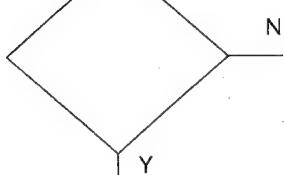
4. Faultfinding

a. Meaning of the symbols used

The symbols used in the test procedure and in the faultfinding tree have the following meaning:



– action/operation to be carried out



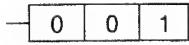
– decision



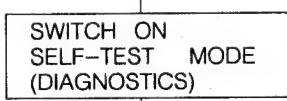
– Check module T or the circuits on this module



– Go on to block 1 in the faultfinding tree



– Error code on the picture screen (no error = ---)



– Switch on the drive by pressing STANDBY + EJECT and MAINS together.
Release buttons when display DIAGNOSTICS is visible

"FOC-EN" (32SR1)

– For a possible fast faultfinding procedure, the signal mentioned (e.g. "FOC-EN") can be measured at the plug indicated, e.g. plug no. 32SR1.
Note: The voltages and signals must be measured relative to ground unless stated otherwise.

Start test software

– Start the test programme according to the directions for use of the test software.

Connect a P3100
via RS232

– Connect a P3100 family or an IBM-compatible personal computer via the RS232C connector.

Introduction

The VP406 is a standard LaserVision disc drive from the VP400 range, with all the versatile LaserVision facilities, such as picture or chapter search, moving pictures, still frames, forward, reverse and variable speed. These facilities can be programmed through a separate computer for interactive applications.

Characteristic of this disc drive:

- Front loading
- Solid-state laser
- Computer control via RS232C interface.
- RGB output for full-bandwidth moving or still pictures.
- Average random access time ≤ 1 sec.
- Instant jump of up to 50 frames in either direction.
- Electronic timebase correction.
- Wired or SCART RC-5 remote control.
- Programmable with the remote control handset.
- Auto replay via replay switch.

Audio / Video signal path

The audio and video information on the video disc has been fixed in the form of pits. The information can be read by means of a laser beam having a wavelength of 780nm. The laser light modulated by the disc falls on the photodiode present and is thus converted into an electrical signal. This signal is a highfrequency signal which is amplified on module Z, see the block diagram of the audio/video signal path. The output signal of this module, HF-OUT 1, goes to panel C where it is in the first instance split into an h.f. audio and an h.f. video signal. The h.f. audio signal goes as HF-AUD to panel B on behalf of timebase correction. The h.f. video signal is also demodulated on panel C and gets amplification correction by means of the MTF signal. The demodulated composite video signal, CV-DEM, will be drop-out corrected.

Drop-out correction is realized by filling it in on a video line which contains a drop-out, together with the video contents of the preceding video line. To achieve this the video signal is delayed one line time ($64\mu s$) and, if a drop-out is detected, filled in in the passing video signal. This is possible because a switch, operated by the drop-out detector, can select the "direct" video or the delayed video. On this panel the MTF signal is created too. This is done by measuring the amplitude of the colour burst signal in the video signal and realizing a dc voltage dependent on this value (the MTF signal). The output signal of this panel is fed to panel B to obtain timebase correction just like the h.f. audio signal.

On panel B the h.f. signal (HF-AUD) and the composite video signal (CV-DOC) are both led through a CCD memory IC and as a result the signals get a delay which depends on the clock frequency offered. The clock frequency is determined by the VCO present which is controlled by the TANG-ER signal (tangential or timebase error signal). The correction which takes place by the TANG-ER signal is the coarse correction. Next the video signal is led through a variable LC delay line with a delay that depends on the BURST-ER signal. This BURST-ER signal is the result of a phase comparison of the disc video signal (CV-TBM) with a reference signal derived from the TBC reference circuitry on panel D. The timebase correction by means of the BURST-ER signal is a fine adjustment. The timebase corrected h.f. audio signal (HFATBC) and composite video signal (CV-TBC) are processed further on panels C and A resp.

On panel C the HFATBC is split into two paths on behalf of demodulation of the two audio channels. In this circuit drop-out detection takes place too where, in the case of a drop-out, the l.f. audio signal is kept at the last level just before the dropout (track and hold principle).

The audio signals can also be switched off by means of switching signals AUD1ON and AUD2ON. The two audio signals are available on 2 CINCH connectors at the rear of the disc drive and also on the Euroconnector.

The composite video signal CV-TBC goes from panel B to panel A where it is further processed into encoded CVBS and RGB.

First of all the video signal is split in a luminance and a chrominance signal. The chrominance signal is decoded into the colour difference signals R-Y and B-Y and next these signals get colour improvement in the **colour transient improver** (CTI). The luminance signal is also fed through the CTI in order to obtain the same delay as the colour difference signals. In the **U/V processor** the colour difference signals can be switched off during a mute by means of the CV/CS signal. On behalf of a possible index signal insert the colour difference signals will be switched off during the index background information and be put at a reference level during the index characters. Colour difference signals (R-Y)ENC and (B-Y)ENC are converted into an encoded chrominance signal in the **PAL encoder**. Colour difference signals (R-Y)RGB and (B-Y)RGB proceed to the **RGB matrix** circuit to be converted into the R, G and B signals together with luminance signal Y (RGB). These R,G and B signals are, at full bandwidth, available on the SCART connector at pins 15, 11 and 7.

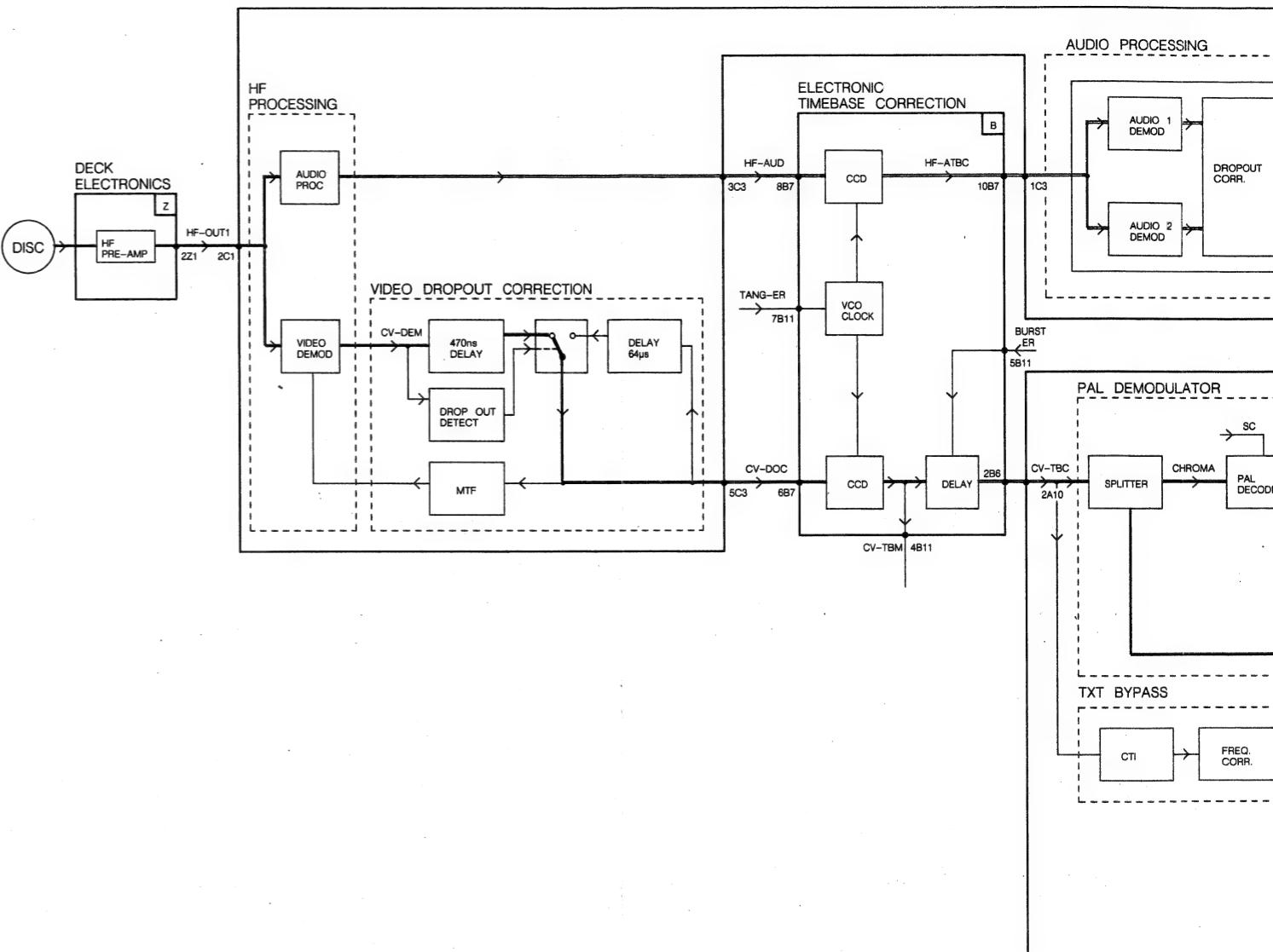
The luminance signal which is available as output signal of the CTI can also be switched off by means of the CV/CS signal, and after that the sync pulses are removed from the video signal by a clamping process. If the user wants to retrieve an index signal, insert of background (with VOBN) and characters (with VOW) will take place. Also, at all times, the luminance signal will be filled up with the possible TXT data from the video disc. This TXT signal (INSERT) comes from the **TXT bypass** circuit, which has the CV-TBC signal as input signal. This signal too will be fed through a CTI just to obtain the same delay as the other video signal path. After a frequency correction and the removal of the sync pulses this video signal is present as INSERT signal for TXT data. The complete luminance signal is as Y(ENC) combined with the encoded chrominance signal. This signal is completed with defined composite sync pulses and is then as standard CVBS suited as output signal. The signal is present on a BNC connector as well as on the SCART connector (pin 19).

The servo block diagram

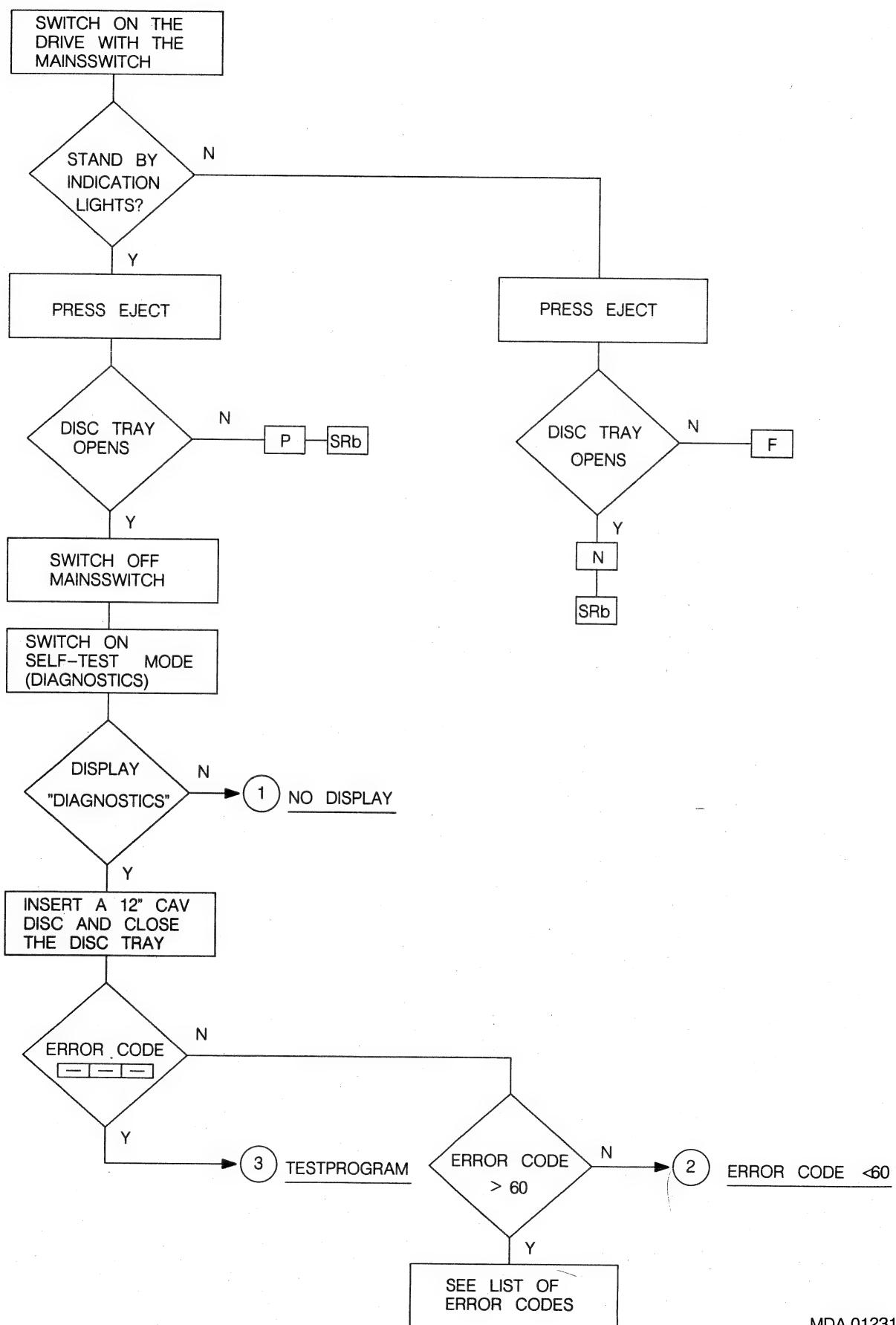
The servo block diagram is a survey of all circuits which are necessary for a correct functioning of the optical deck.

The circuits are:

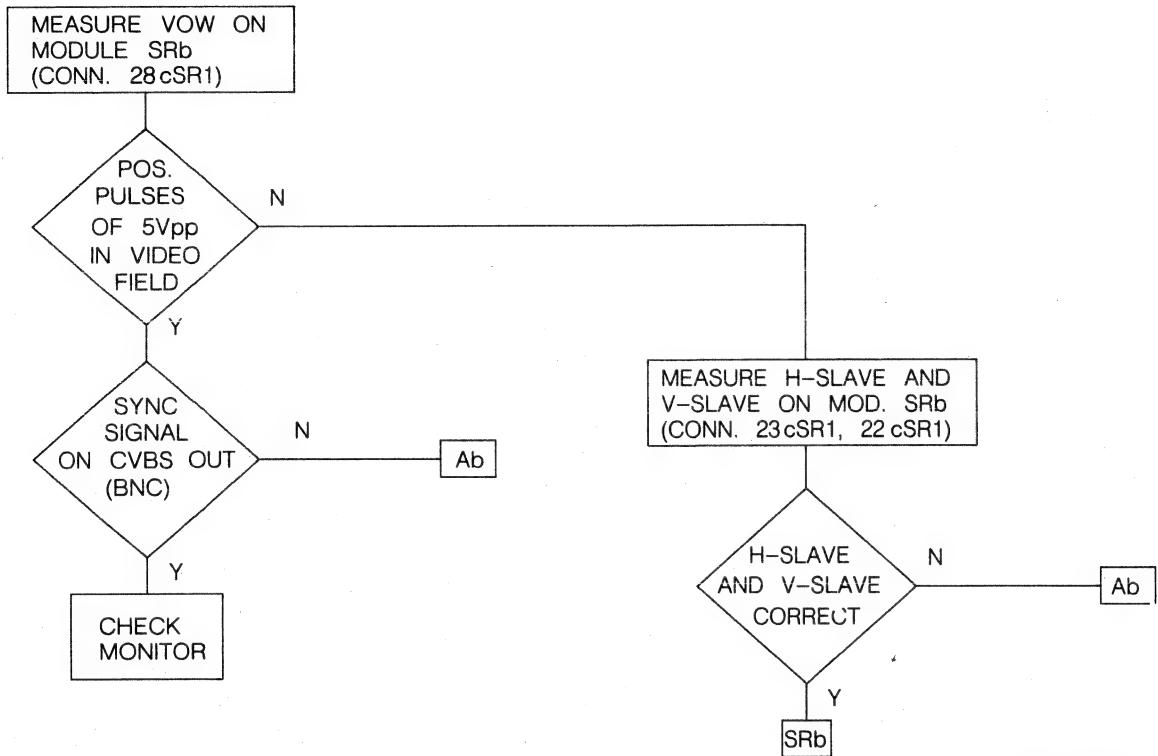
- The deck electronics **Z**
- Focus drive **A_b**
- Radial drive **B**
- Drive processor **SR**
- Slide motor drive **C_b**
- Motor + Sequence module **D_b**
- Sequence circuit **D_a**



b. TEST PROCEDURE

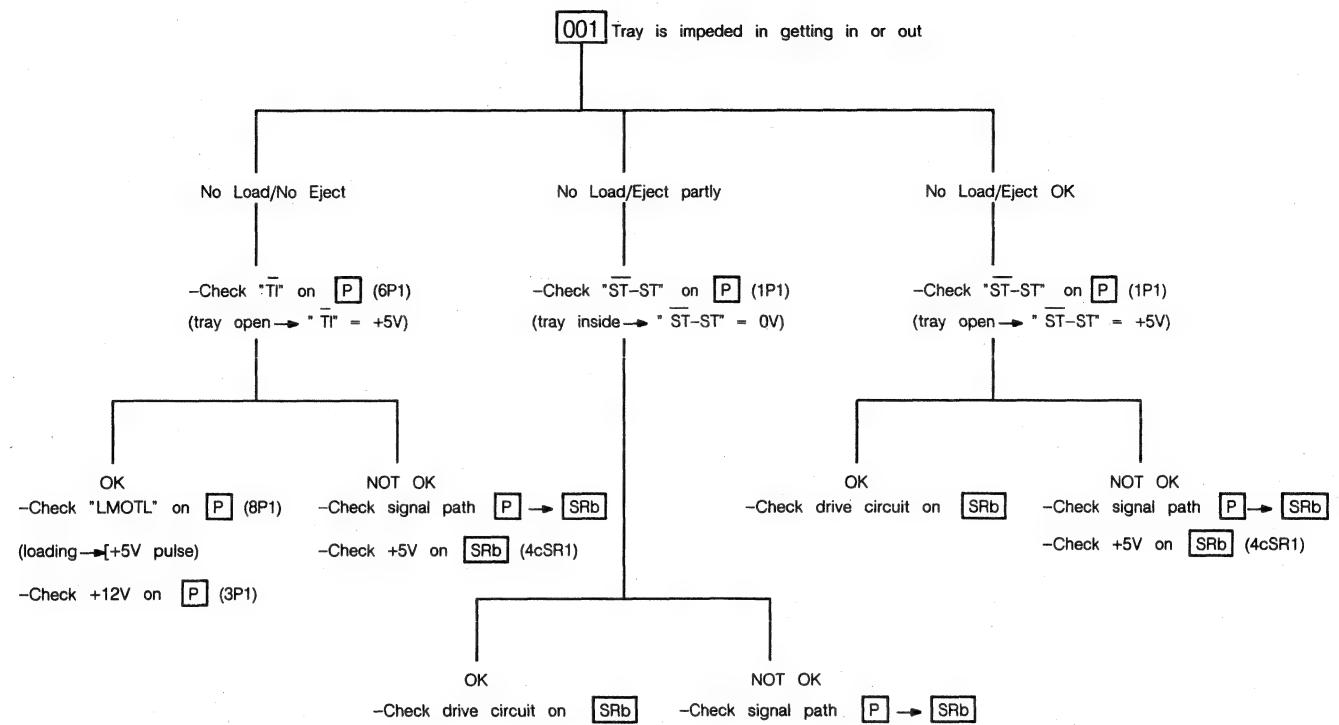


① NO DISPLAY

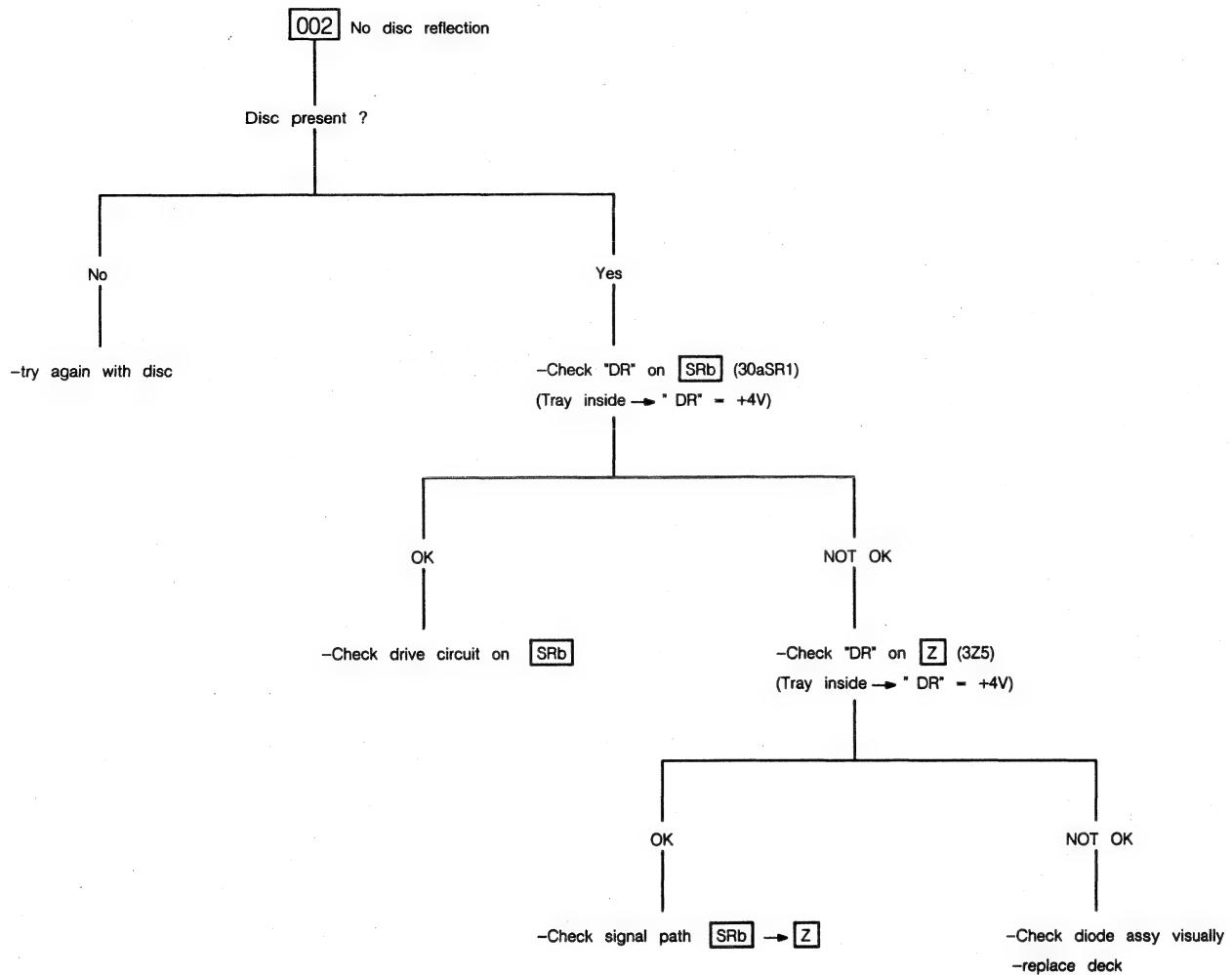


MDA.01229
T-04 849

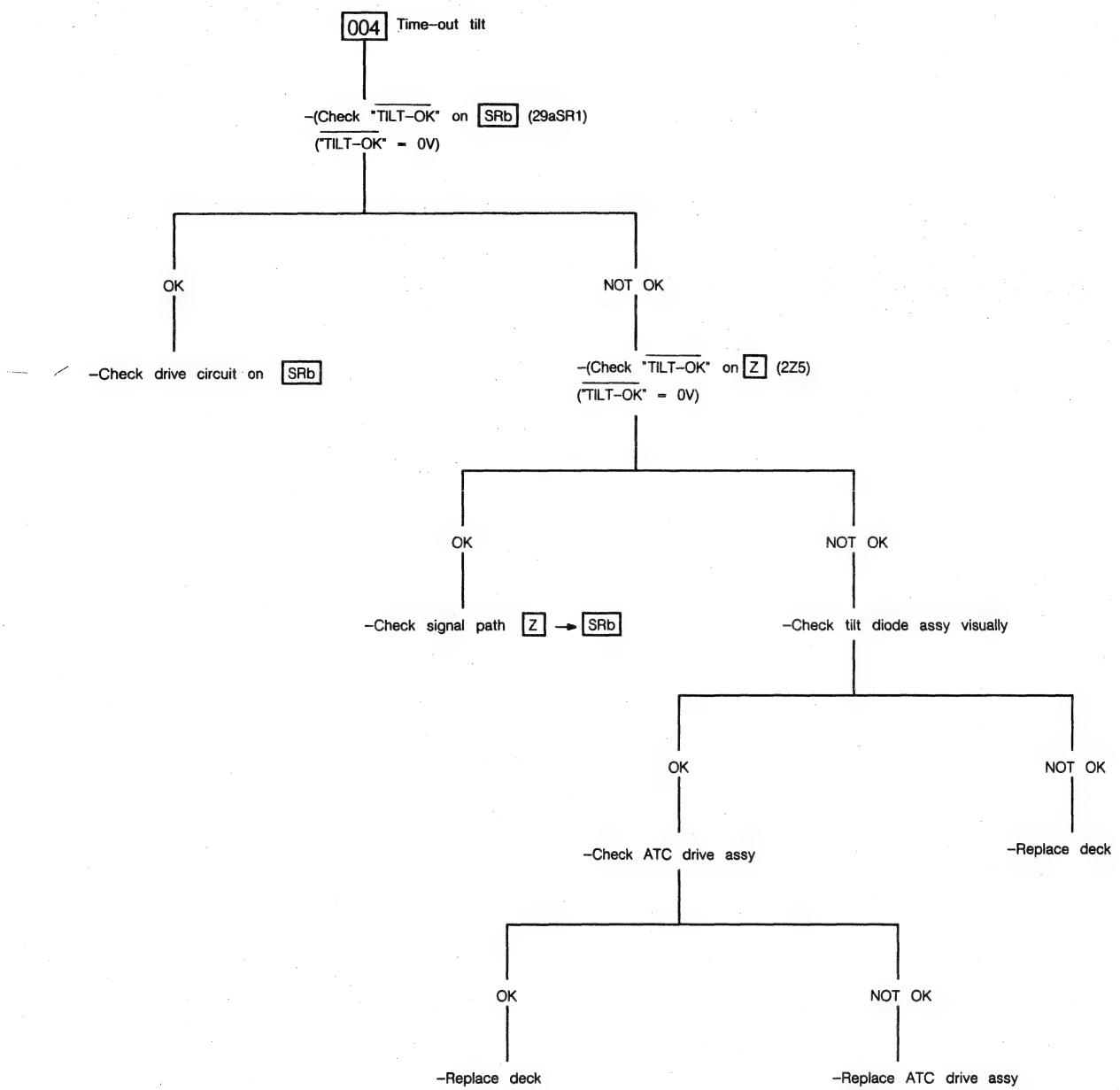
② ERROR CODE <60 (SELF TEST MODE)



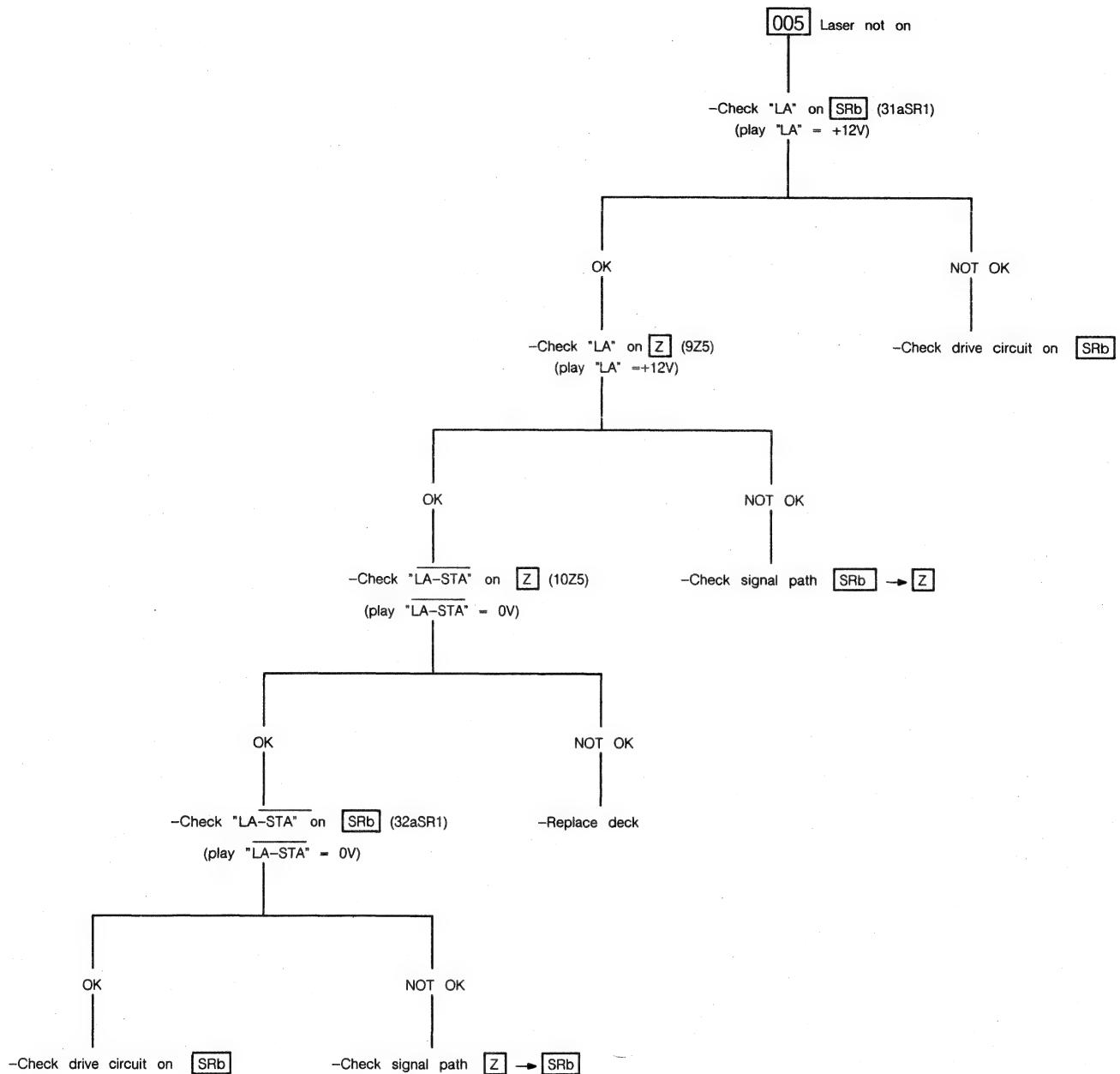
PRS.03778
T-04 848



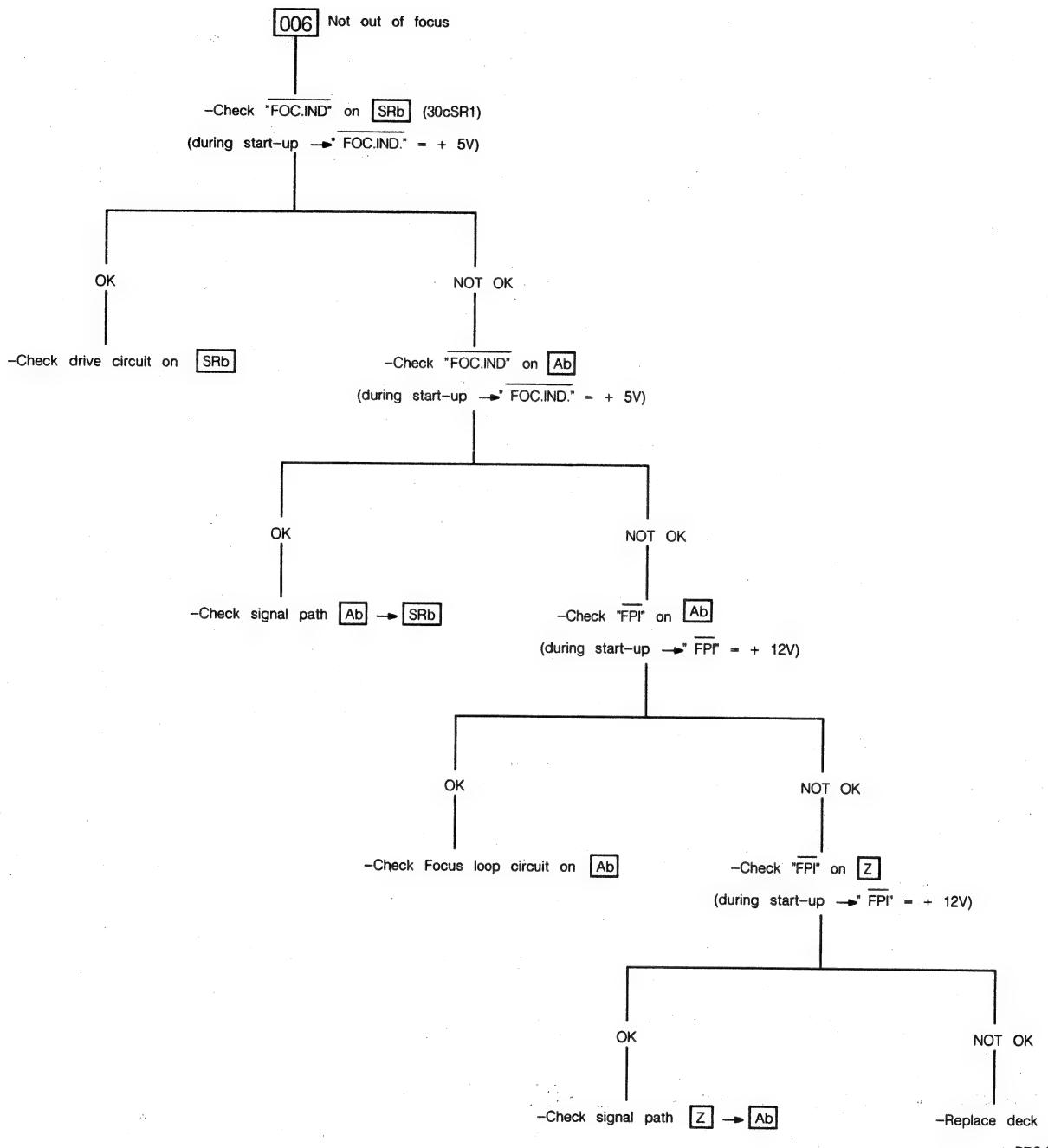
PRS.03777
T-04 848



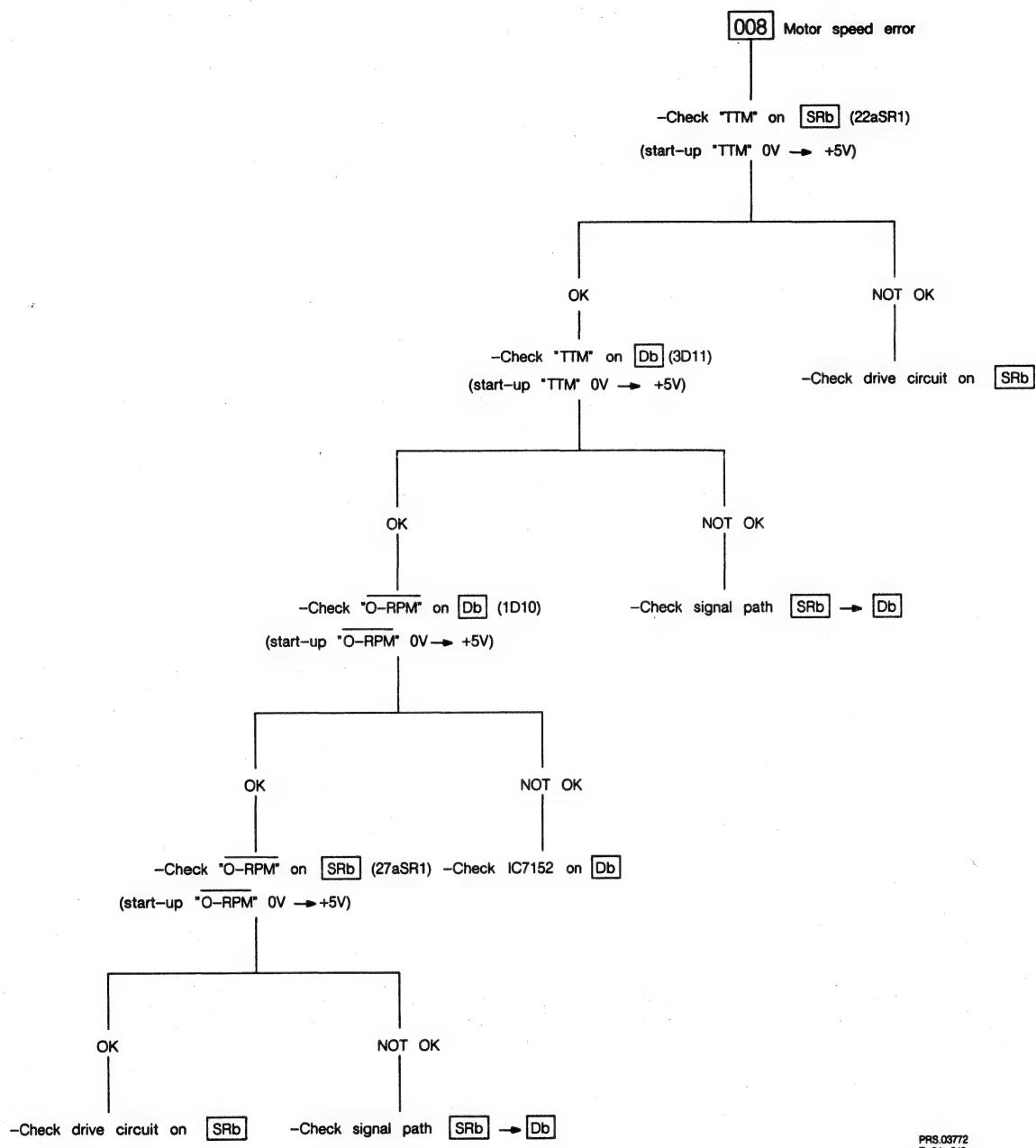
PRS.03776
T-04 848

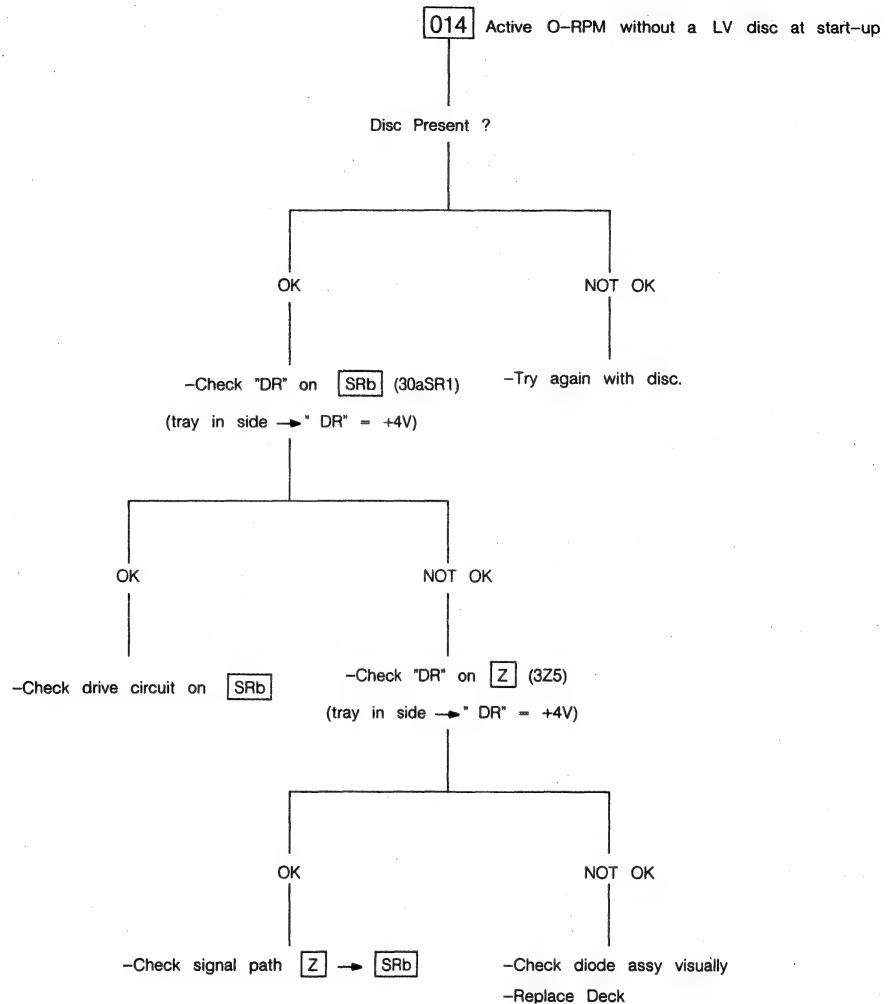


PRS.03775
T-04 848

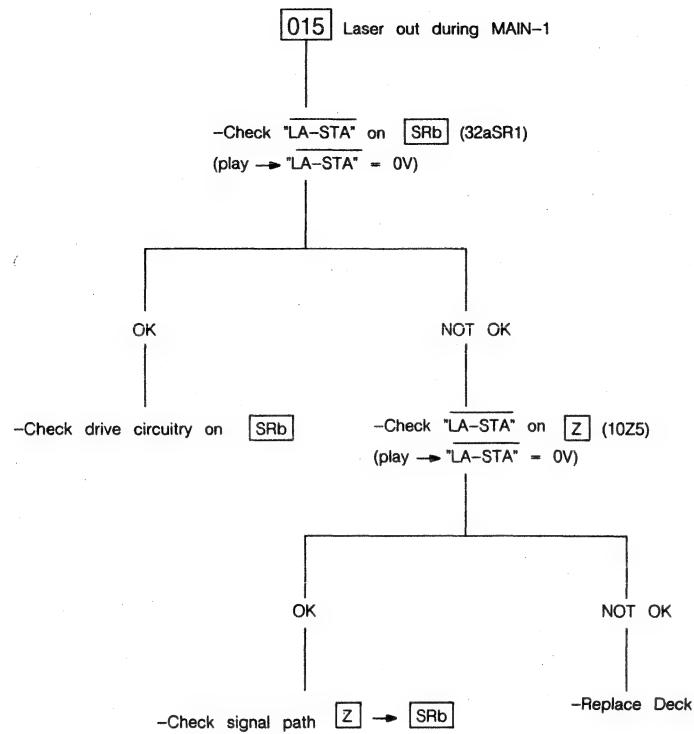


PRS.03774
T-04 849

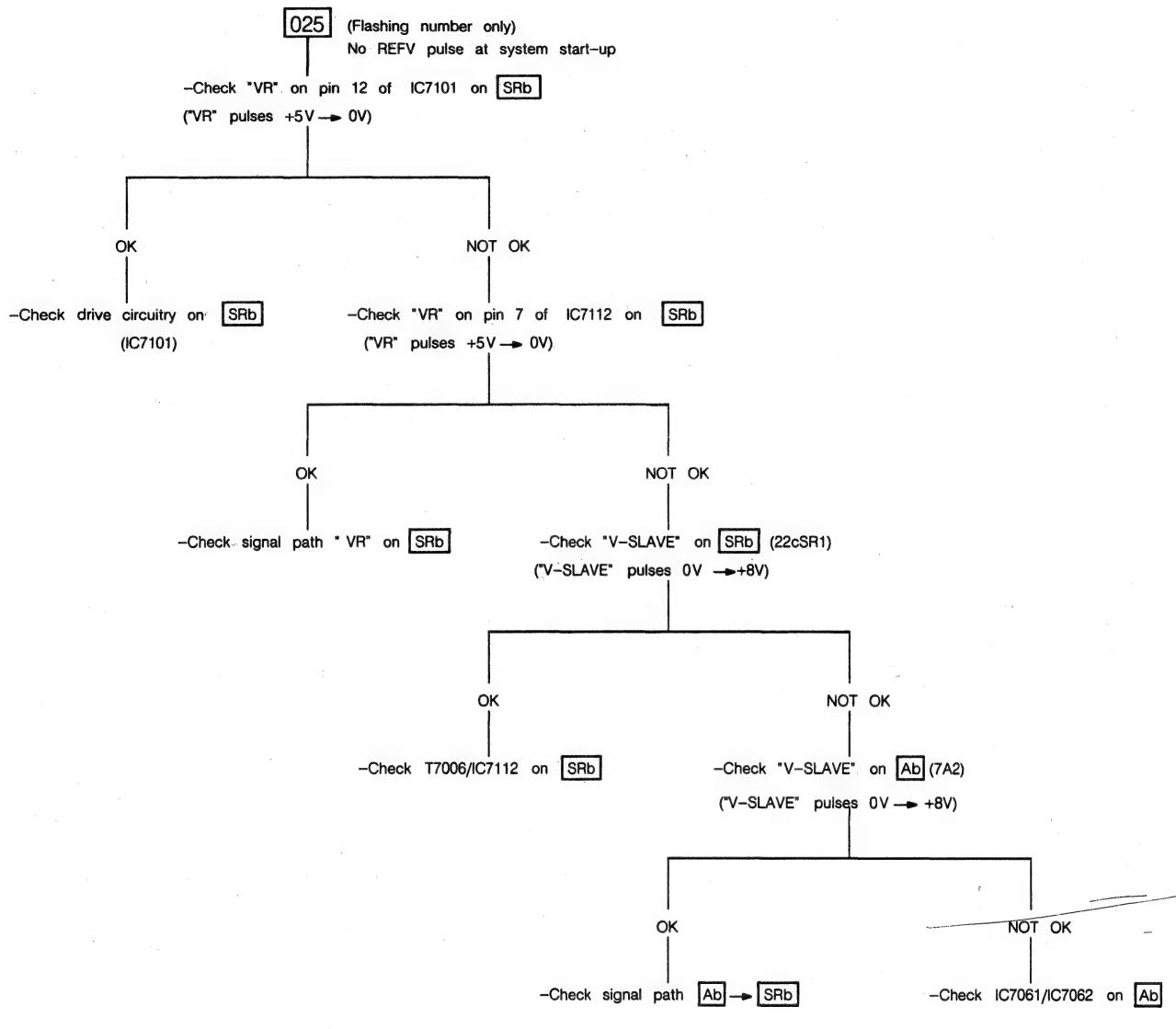




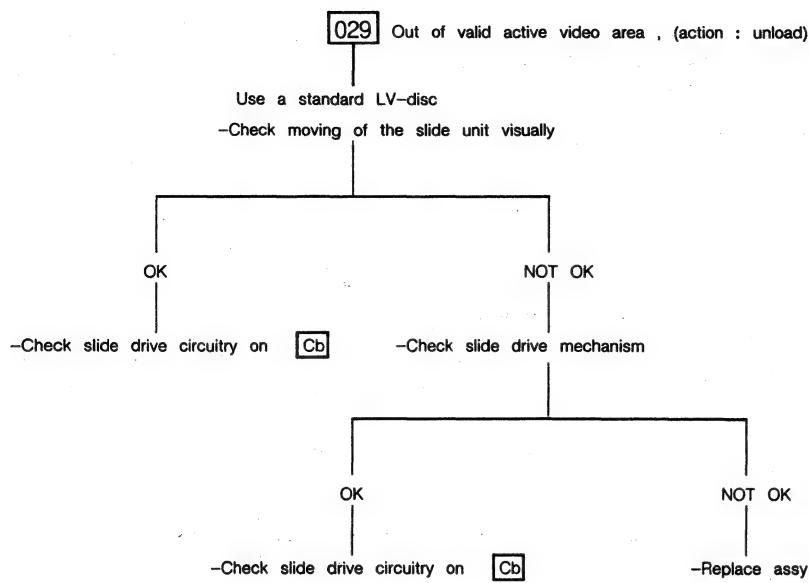
PRS.03768
T-04 849



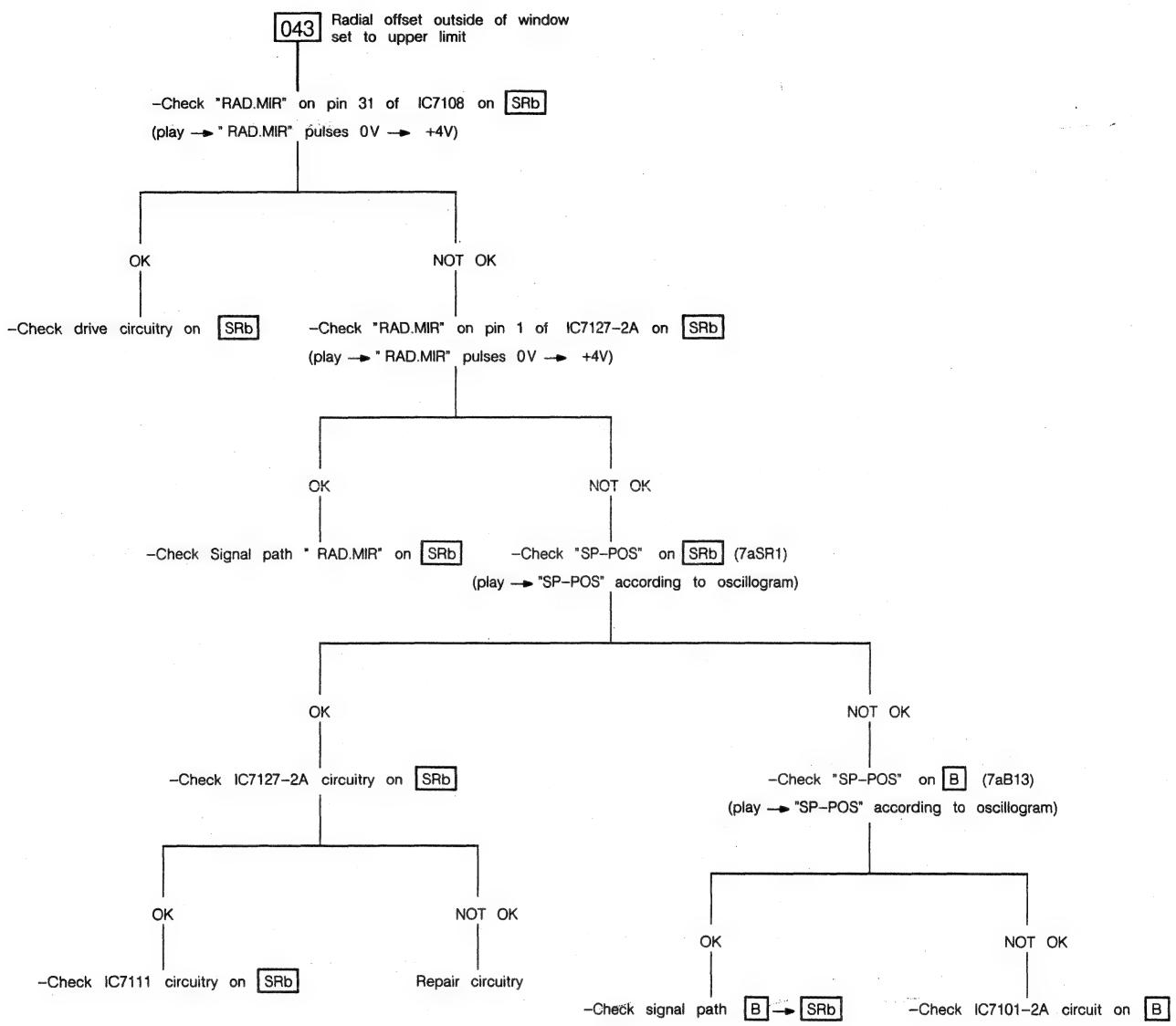
PRS.03766
T-04 849



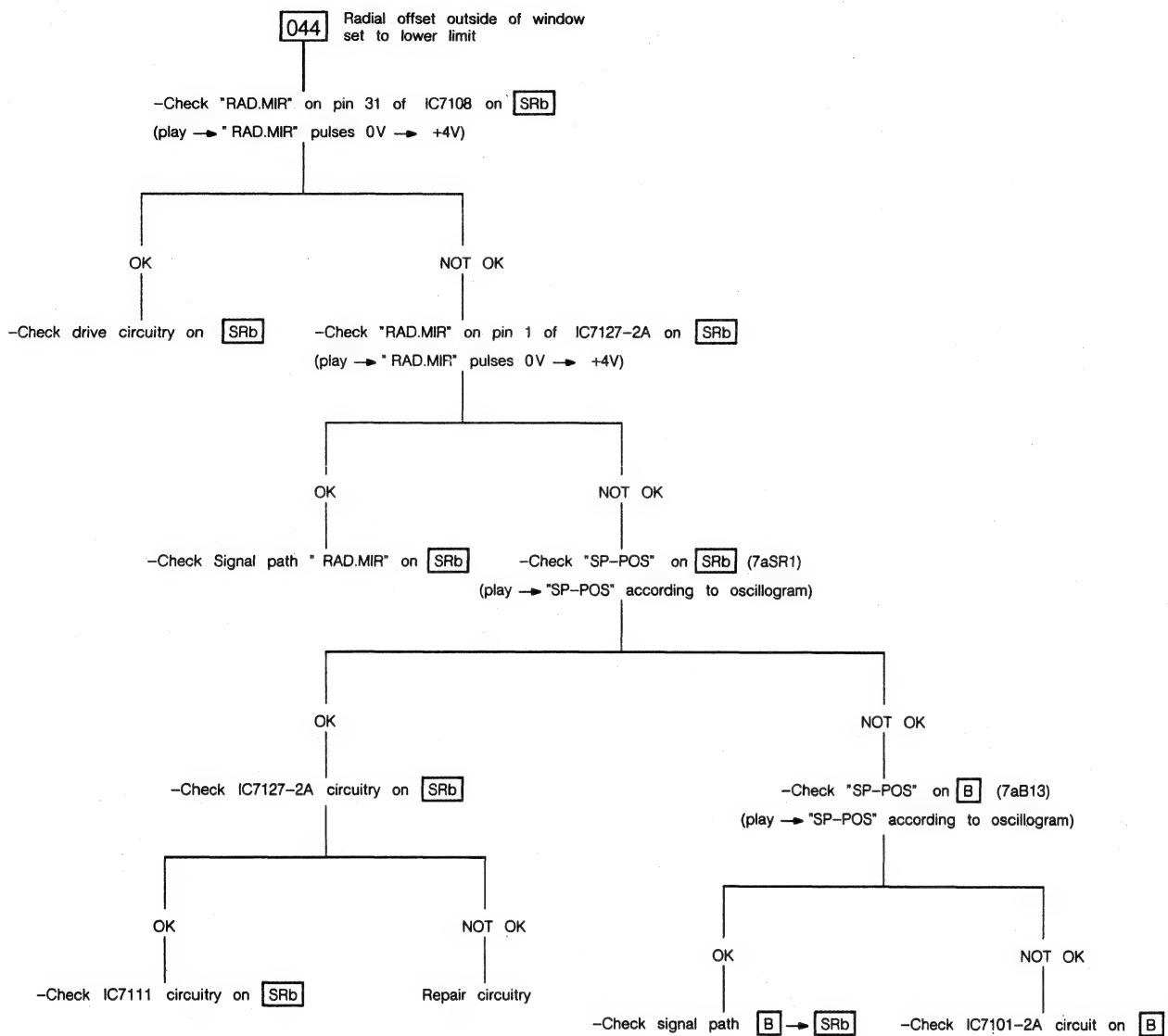
PRS.03763
T-04 849



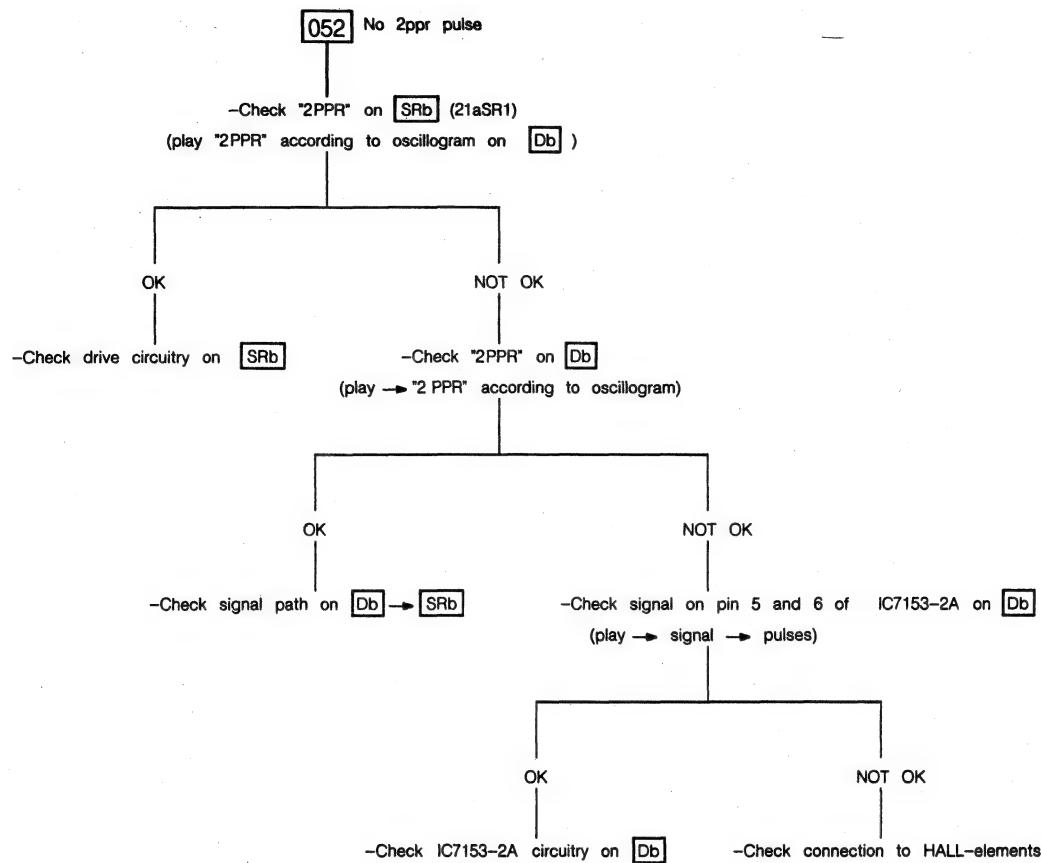
PRS.03762
T-04 804
VP405



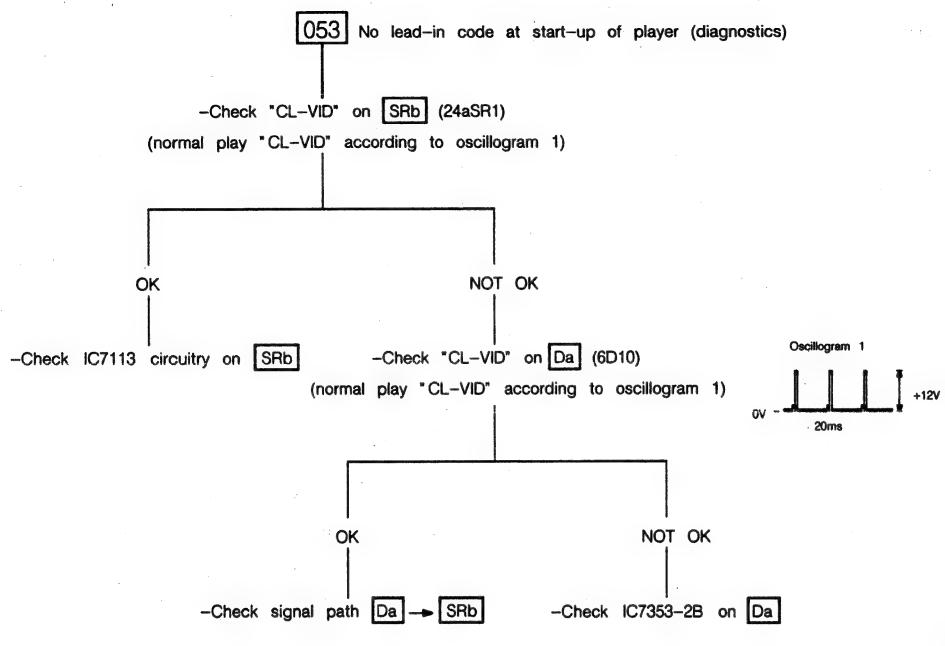
PRS.03761
T-04 849



PRS.03760
T-04 849



PRS.03759
T-04 849



058 Play forward error (diagnostics)

-Check moving of the slide circuit visually

OK

-Check "SL-PWR" on [Cb] (5C5)
(play "SL-PWR" pulses + 5 V → 0 V)

OK

-Check COMM-1,2,3,4 on [Cb]
(play: signals according to oscilloscope)

OK

-Check slide drive circuitry on [Cb]

NOT OK

-Check "SL-PWR" on [SRb] (14aSR1)

OK

OK

NOT OK

-Check slide drive mechanism

NOT OK

NOT OK

-Replace assy

-Check signal path [SRb] → [Cb]

NOT OK

-Check signal path [SRb] → [Cb]

NOT OK

-Check drive circuitry on [SRb]

-Check COMM-1,2,3,4 on [SRb] (10aSR1)
(11aSR1)
(12aSR1)
(13aSR1)

OK

-Check signal path [SRb] → [Cb]

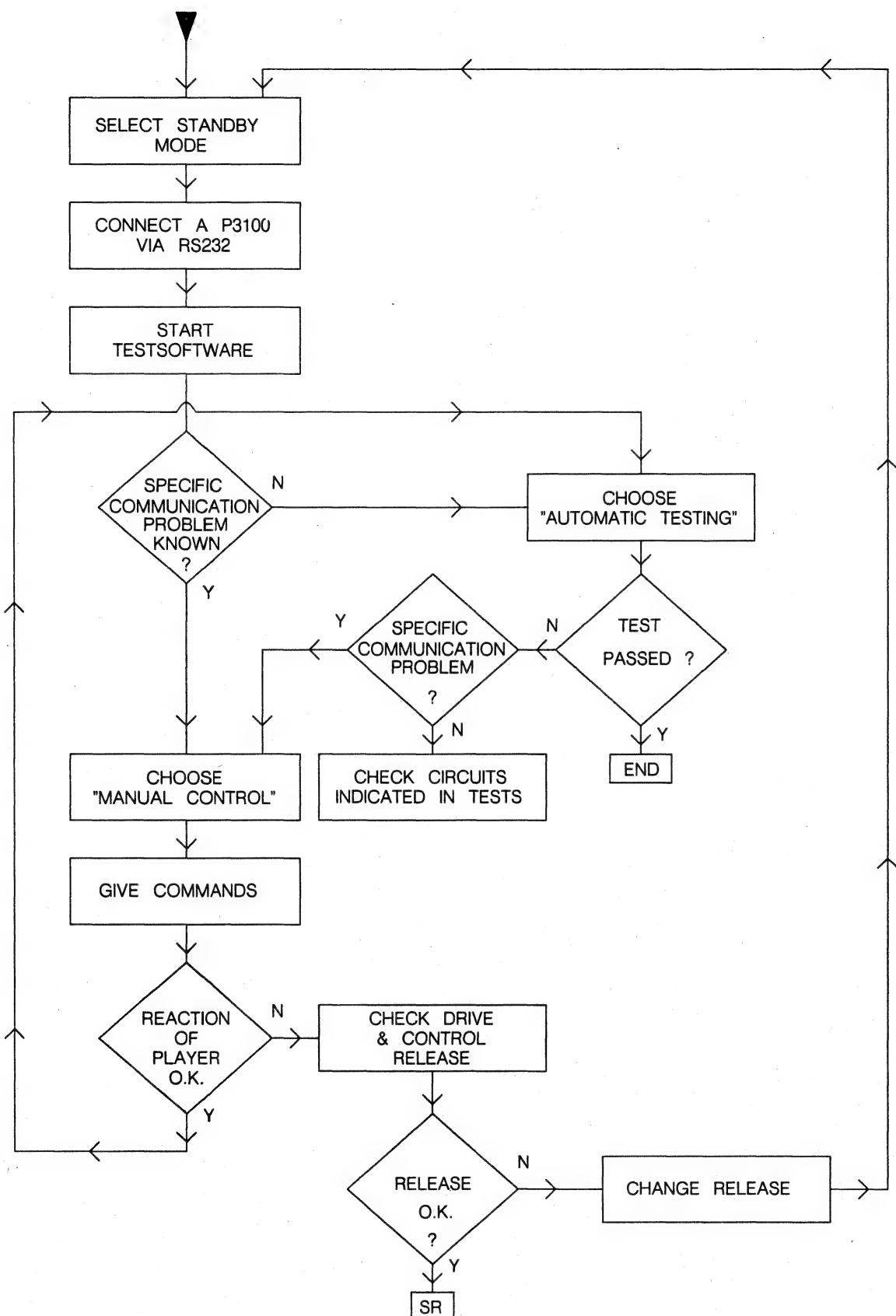
NOT OK

OK

-Check drive circuitry on [SRb]

PRS.03757
T-04 849

3 TESTPROGRAM



MDA.01230
T-04 848

Circuit description

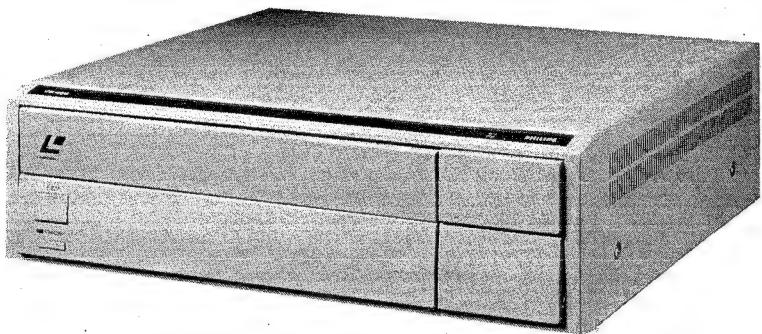
Chapter 7

Standard LaserVision disc drive VP406

Service
Service
Service



00/02/05



Circuit Description

CONTENTS

	Page		Page
Chapter 1 The LaserVision system	1	Chapter 3 Panel and module description	11
Introduction	1	A: Video processor panel	11
Encoding of the signals on the disc	1	PAL demodulator	11
Focusing	2	U/V processor	11
Radial tracking	3	PAL encoder	11
Time base correction	3	Y processor	12
The optical deck	5	RGB matrix	12
Chapter 2 VP400 series	7	Sandcastle generator	12
Introduction	7	Teletext bypass	13
Blockdiagram audio/video signal path	7	Slave source	13
Blockdiagram servo	7	Focus drive	14
Control routes + Start-up sequence	9	B: Radial + TBC panel	14
S-bus	10	ETBC signal processing	15
		Radial drive	16
		C: HF + Audio panel	16
		HF processor	16
		Audio processor	16
		Video dropout correction	17
		MTF	17
		Slide drive	18
		D: Motor sequence + TBC module	18
		ETBC reference & measuring	18
		Motor + sequence	19
		F: Supply module	20
		P: Frontloader module	21
		SR: Control + drive module (CODRIVE)	22
		Z: Deck electronics	25

Description des circuits Schaltungsbeschreibung Kredsløbsbeskrivelse Kretsbeskrivelse Kretsbeskrivning Toimintaselostus Descrizione del circuito Description del circuito



Subject to modification

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Service Consumer Electronics

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CHAPTER 1 THE LASERVISION SYSTEM

Introduction

In the LaserVision system the video and audio information are stored on a disc in encoded form.

The information on the disc is scanned optically on a LaserVision disc drive and then converted into a CVBS signal as well as RGB signals suitable for a standard colour television receiver with Euroconnector. The information is stored on the disc along a spiral track in the form of pits; the disc is scanned from the centre to the outside. The length of the pits and their spacing are determined by the stored information.

The pits are $0.4 \mu\text{m}$ wide and approximately $0.1 \mu\text{m}$ deep. The track-to-track spacing is 1.6 to $1.8 \mu\text{m}$ (refer to Fig. 1). The overall length of the track on a 30 cm disc is about 34 kilometres !

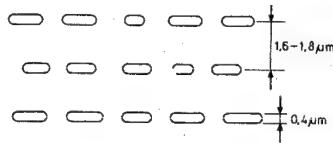


Fig. 1

The disc is made of a transparent plastic into which the pits are pressed. An extremely thin reflective layer of aluminium is added on top, followed by a protective coating that covers the whole. Two of these discs are glued together to form a double-sided disc. A cross section of the disc is shown in Fig. 2.

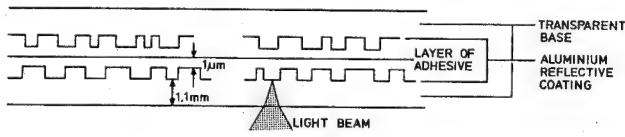


Fig. 2

A great advantage of the optical system is the contactless readout of the information on the disc, as a result of which wear of disc and read-out device is non-existent. A second advantage is the effective protection of the information on the disc against dust, fingerprints, etc. When taking a closer look at the beam path from the objective to the disc (refer to Fig. 3), we notice that at the place where the light cone enters the transparent base section the light cone's diameter is still fairly large.

Dust particles, etc. at this place exert very little influence; the light passes, as it were, around the dust particle. This highly effective protection of the information enables normal handling of the disc.

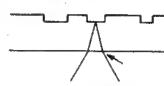


Fig. 3

Optical read-out of the information on the disc takes place as follows:

The light beam from a AlGaAs semiconductor laser is focused on the disc by a lens (objective). In the absence of a pit practically the full amount of light is reflected. The reflected light passes through the objective and is then separated from the light beam going to the disc. The reflected light now falls on a photodiode; the amount of current that starts flowing through the diode is proportional to the amount of light falling on it.

When the light beam hits a pit, practically no light will be reflected due to the properties of the laser light and the depth of the pit; consequently, the current passing through the photodiode will be reduced.

In this way it is possible to convert the information on the disc into an electrical signal that is suitable for further processing to a standard videosignal in the disc drive.

Encoding of the signals on the disc

The videosignal is frequency modulated on a carrier (refer to Fig. 4a). Top sync level is situated at a frequency of 6.76 MHz , black level at a frequency of 7.1 MHz and white level at a frequency of 7.9 MHz . This results in a total frequency swing of $7.9 - 6.76 = 1.14 \text{ MHz}$.

Including this side bands the video FM signal encompasses a frequency range up to approximately 2.5 MHz at the lower side.

The two audio signals are equally frequency modulated on carriers of 683 kHz and 1066 kHz respectively. The frequency swing of the two channels is $\pm 100 \text{ kHz}$ (refer to Fig. 4b).

Summing these three signals and next limiting them results in a pulse-width modulated signal (refer to Fig. 4c). The negative half periods of this signal determine the length of the pits, the positive half periods determine the spacing of the pits (refer to Fig. 4d).

Fig. 5 shows the entire frequency spectrum with associated recording levels of the video and audio RF signals.

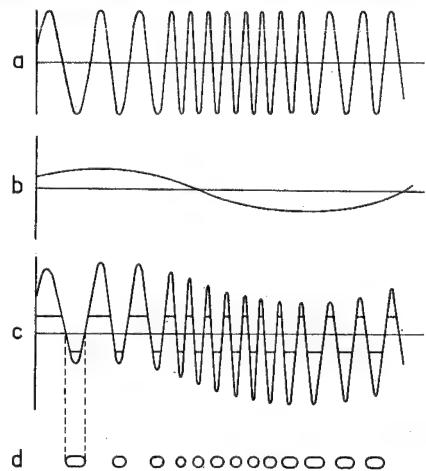


Fig. 4

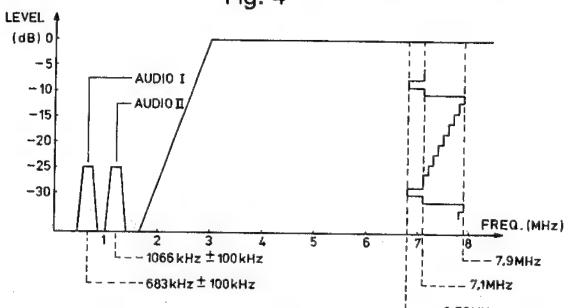


Fig. 5

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The encoded RF signals may be stored on the disc in two different ways:

1. The disc rotates at a constant speed ($1500 \text{ rpm} = 25 \text{ rps}$). At each revolution of the disc a complete TV picture is reproduced. This implies that the length of the track corresponding to one picture gradually increases from the centre of the disc to the outside. The frame sync pulses are situated on a diagonal. This type of disc is referred to as CAV disc (Constant Angular Velocity disc). Special playing modes like 'still picture', 'slow motion', 'fast forward' and 'reverse' are feasible with this type of disc only, since the frame sync pulses and, consequently, the frame blanking are situated on a diagonal. This allows jumping from one track to the next one or to the preceding one during the frame blanking period.

The maximum playing time of a CAV disc is 36 minutes/side.

2. The track length of each frame on the disc is constant. This implies that the rotational speed of the disc decreases when scanning the disc from the inside to the outside, and that from 1500 rpm at the inside to 565 rpm at the outside of the disc. This type of disc is referred to as CLV disc (Constant Linear Velocity disc). No special playing modes can be realised with this type of disc, because the frame sync pulses and frame blanking are no longer on a diagonal, thus putting jumping from one track to the other out of the question.

The maximum playing time of a CLV disc is 54 minutes per side. The disc drive is suited for both types of discs.

In addition to the video and audio information, the disc contains a number of special codes, inserted in the frame blanking periods.

Test signals have been inserted during the lines 19, 20, 332, 333. Digital codes for various purposes have been inserted during the lines 16, 17, 18, 329, 330, 331.

These signals have the following functions:

Lead-in tracks

A minimum of 900 tracks prior to the start of the actual programme contain a start code which sends the read-out objective to the beginning of the programme at nine times the normal speed.

Lead-out tracks

A minimum of 600 tracks immediately after the end of the programme contain an end code which sends the read-out objective back to the beginning at 75 times normal speed. Video and audio signals are muted during the return period.

Programme area

Here a distinction has to be made between CAV and CLV types of discs.

CAV discs

1. Picture code consisting of a picture number by means of which each individual picture of a programme can be identified.

The number may be displayed on the monitor screen, if desired.

The picture number code is always present in the first field of each complete television frame. The second field may contain a stop code to switch the disc drive to STILL PICTURE mode.

2. Chapter code consisting of a chapter number by means of which a search action can be automatically stopped as soon as the start of the relevant chapter is reached. The chapter number may also be displayed on the monitor screen, if desired.

The presence of stop code and chapter code is optional and depends on the programme content.

CLV discs

1. A normal play code is always present in CLV discs. This code disables the special modes of operation of the disc drive.

2. Instead of a picture number code a time code is present in LV discs. It contains a time coding with hour and minutes indication showing the time elapsed since the start of the programme. This time may be displayed on the monitor screen, if desired.

Focusing

The objective used to read the information on the disc has a very small depth of focus, that is, maximum 1.5 μm . In view of tolerances in disc and in disc drive construction this accuracy can only be realised by means of a servo-control system that continuously verifies and corrects the focusing of the objective. For this purpose the objective is

mounted in a magnet so as to allow vertical motion. Around the objective and firmly attached to it, a coil has been mounted. By feeding a current through the coil, the objective will move more or less upwards, depending on the current intensity. Fig. 6 shows a cross-sectional view of the objective plus coil and magnet.

The system is very much similar to a loudspeaker system.

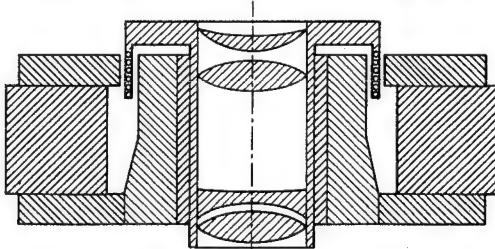


Fig. 6

27623A19

The objective is driven in the following way:

The light reflected by the disc is focused on the photodiodes by the objective. On its way to the diodes the reflected beam passes an astigmatic lens system, like a cylinder lens.

Unlike a spherical lens, an astigmatic lens does not have one single focal point, but two focal lines at some distance from each other and at right angles to each other. Between the focal lines a plane exists where a circular picture is formed. When the disc is out of focus with respect to the objective, that is too far from or too close to the objective, the astigmatism will modify the shape of the picture from the focused state (circular picture) to an elliptical picture. The direction of the ellipsis' axes is determined by the fact whether the disc is too far from or too close to the objective. The photodiode that converts the light variations into an RF signal is composed of four quadrants A, B, C and D (refer to Fig. 7). When the objective is in focus, all four quadrants receive equal amounts of light.

When the objective is out of focus, either A and B or C and D receive more light. The quadrants are interconnected crosswise. The sum of the signals over A, B, C and D receive more light. The quadrants are interconnected crosswise. The sum of the signals over A, B, C and D constitutes the RF signal. The difference signal $(A+B)-(C+D)$ is the drive signal for the objective.

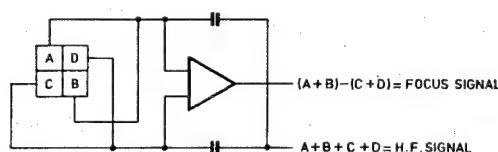
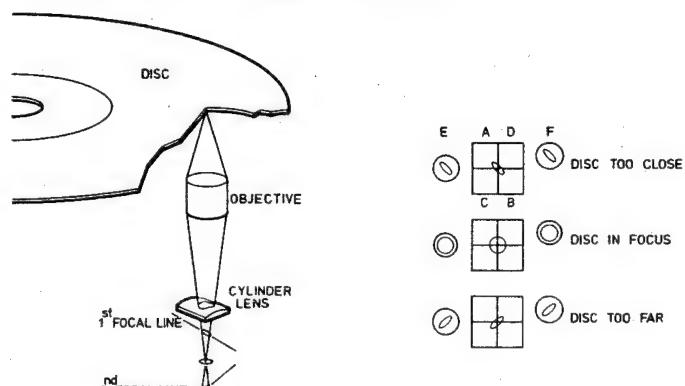


Fig. 7

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Radial tracking

The information on the disc is contained in a spiral track that is read from the inside to the outside. This implies that objective – in order to be capable of following the track – has also to move from the centre of the disc to the outside. For this purpose the objective and all associated components which constitute the optical system are mounted on a slide, driven by a motor and moving radially under the disc.

The light has to follow the track on the disc with an accuracy of approximately $0.1 \mu\text{m}$.

Tolerances in player and disc may cause a track wobble of $130 \mu\text{m}$. It will be clear that the slide is incapable of following this wobble at a rotational speed of 25 rps.

To obtain the required accuracy a movable mirror has been inserted in the light path under the objective; this mirror allows to move the light spot radially over the disc.

A magnet is attached to the mirror. Around the mirror a coil is mounted. When a current flows through the coil, the intensity and the direction of this current determine to what extent the mirror will pivot to the left or to the right (refer to Fig. 8).

Driving of the mirror is obtained as follows:

In the optical system, apart from the main beam for track scanning, two further auxiliary light beams are formed whose impact is slightly displaced with respect to the track's centre line, in opposite directions.

The light spots formed on the disc by the two auxiliary light beams fall partly on the track and partly outside the left or right edge of the track. The objective focuses these light spots on two separate photodiodes situated at either side of the signal diodes (E and F in Fig. 7). When the track is followed correctly, the signals coming from each diode will be equal. When tracking is less optimal, it depends on the direction of deviation which diode output will exceed that of the other diode (Refer to Fig. 9).

The difference between both signals is – after amplification – used to drive the mirror. When the average voltage across the mirror coil is positive or negative, the slide motor will be controlled until the average voltage is again 0 (zero).

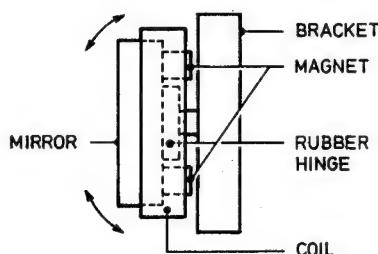


Fig. 8 27628A19A

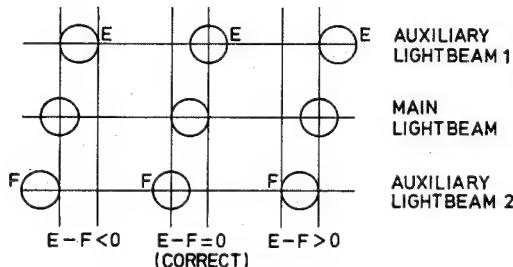


Fig. 9 27626A19A

TIME BASE CORRECTION

As known, a TV picture consists of lines that are written in an accurately laid down time ($64 \mu\text{sec}$ for the PAL system). Deviations from this time cause a distorted picture and phase errors in the colour signal which may lead to dropping out of the colour.

The video signal of the disc drive should also meet this requirement of constancy of the time base to be able to give an undistorted picture with colour.

The presence of several tolerances (disc, centring, motor) results in variations in the line time of the video signal.

Now the maximum permissible deviation from the time base to give a stable picture with every TV receiver is 5 nsec. To reach this value it will first of all be necessary to keep the speed of the turntable motor as constant as possible. To achieve this the phase of the line sync pulses is compared with the phase of pulses with the line frequency coming from a crystal oscillator. The resultant control voltage is used to drive the turntable motor. It is clear, however, that variations in speed with a frequency of 25 Hz and higher cannot be corrected by this control.

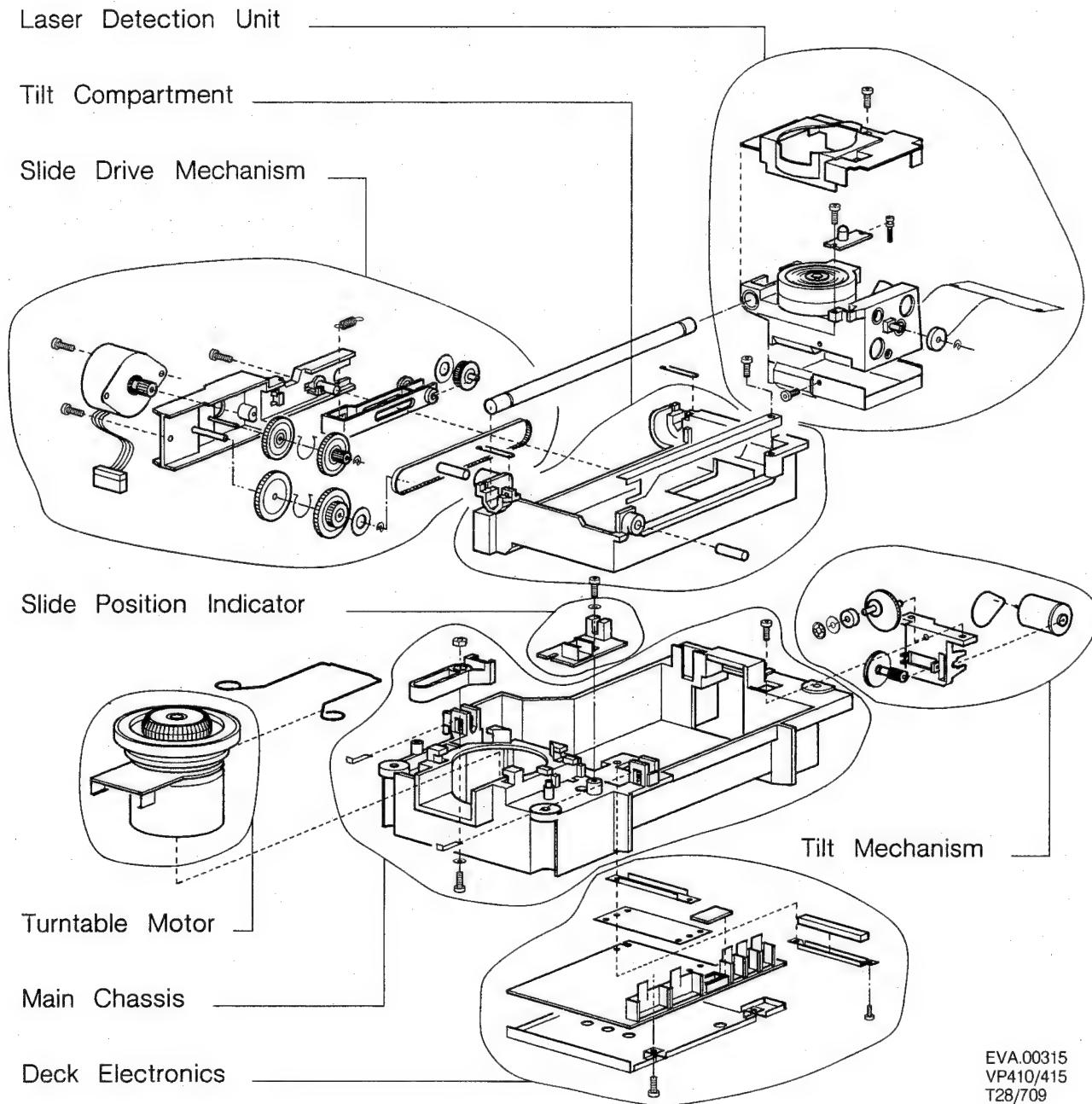
For the correction of these errors use is made of a CCD (charge coupled device) which functions as a variable delay line for the great time errors ($+/- 17 \mu\text{sec}$) and a variable LC delay line for fine control ($+/- 50 \text{nsec}$).

The CCD is driven by a signal which is obtained through comparison of the phase of crystal-controlled reference signal with the line frequency and line frequency pulses of the disc video signal.

Since the line sync pulses themselves are not suited for an accurate enough measurement of the time difference use is made of a signal having a frequency of 3.75 MHz ($240 \times$ the line frequency) which has been laid down on the disc at the level of the peak sync pulses.

If the same zero crossing of the 3.75 MHz signal is used for every line sync pulse, the actual line time can be measured sufficiently accurately. The time base correction makes it possible to connect the disc drive to any TV set.

Fig.OD1 OPTICAL DECK



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VP410/415
T28/709

THE OPTICAL DECK

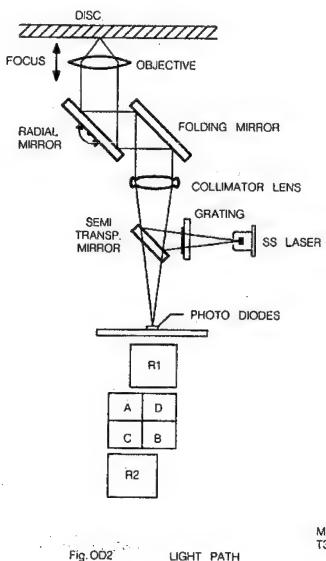
The optical deck reads the information from the video disc by means of a laser beam. The modulated laser light is transferred into an electrical signal which is further processed in the electronics of the player.

The deck consists of a main chassis, containing the following parts (see Fig. OD1):

- The Laser detection Unit (LDU) to read the information from the video disc.
- The slide drive mechanism to move the LDU under the disc.
- The turntable motor to spin the disc.
- The tilt compartment which causes an angular (and vertical) move of the LDU under the disc.
- The tilt mechanism to drive the tilt compartment.
- The slide position indicator to indicate the starting position of the slide.
- The deck electronics where the signals from the LDU and tilt control are processed.

The Laser Detection Unit (LDU)

The LDU reads the information from the video disc and delivers electrical signals to be processed further. The principle of the unit has been drawn in Fig. OD2.



A Solid State laser emits a diverging laser beam. The power of the beam is 3mW and the emitted light has a wavelength of 780 nm. The laser is of the Aluminium Gallium Arsenide (AlGaAs) type.

Just in front of the laser, a grating plate has been situated, causing the laser beam to be split into a main beam and two auxiliary beams, to be used for radial tracking.

After the grating, the beam reflects partly on the surface of a semi transparent mirror. The reflected beam, still diverging, passes through a collimator lens causing the beam to proceed exactly parallel. A folding mirror projects the beam onto a radial mirror which is activated by the radial correction signal.

Eventually the objective focusses the beam on the surface of the video disc. The objective is driven in vertical direction by the focus correction signal.

The laser light that is reflected by the video disc, containing the disc-information, returns by the same path as described before, so via the objective, radial and folding mirror, through the collimator lens to the semi transparent mirror.

On this mirror, the laser light is partly reflected back into the laser, but enough light is going through the mirror to be detected on the photodiodes. These diodes consist of a quadrant diode and 2 auxiliary diodes R1 and R2. The quadrant diode delivers the signals AB CD to compose the HF- and focus signal, diodes R1 and R2 deliver the radial tracking signals.

Fig. OD3 shows the detailed construction of the LDU.

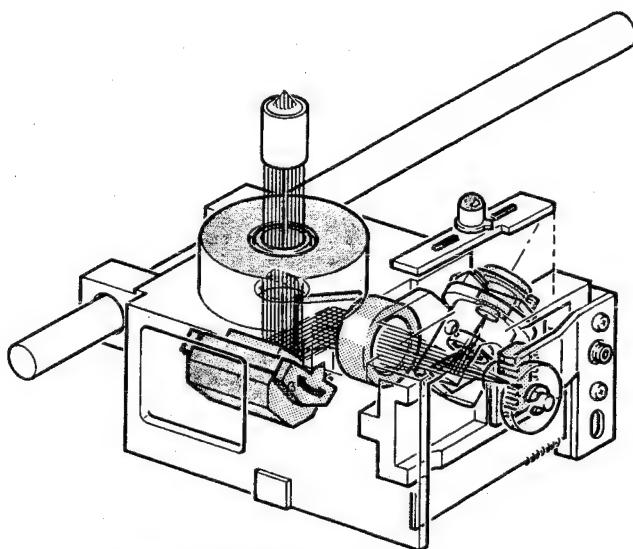


FIG. OD3 LASER DETECTION UNIT

42 043 A12

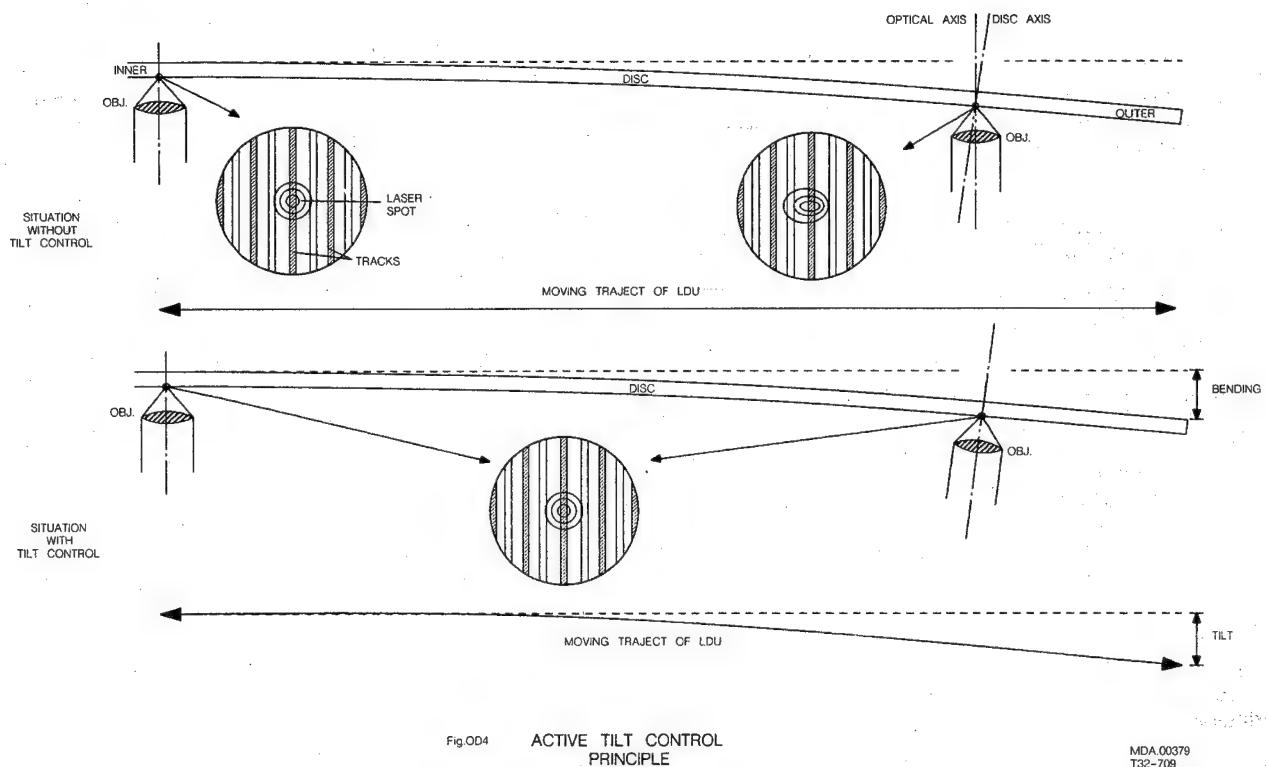


Fig.OD4 ACTIVE TILT CONTROL PRINCIPLE

MDA 00379
T32-709**Active Tilt Control (ATC)**

- Principle (see Fig. OD4)

When a video disc is put on the turntable it will bend, caused by its own weight (umbrella shaped).

The LDU which is moving in a horizontal plane under the disc will have a different distance related to the surface of the disc when reading in the beginning of the disc or at the outer side of the disc. At the outer side, the optical axis of the LDU is not perpendicular to the disc surface anymore. In this area, the focussed laser spot is distorted, causing optical cross-talk between the tracks. Active Tilt Control means that the LDU is moved in angular direction to achieve that the LDU is always perpendicular to the disc surface, so that the cross-talk is minimal. Therefore the distance between LDU and disc has to be measured to detect a possible deviation.

- Measuring the distance

To measure the distance between the LDU and the disc surface, a LED is mounted on the LDU which emits infrared light.

The light that is reflected on the disc surface, hits receiving diodes D1 and D2 (see Fig. OD5). When the reflected light on D1 equals D2, the position of the LED (and of the LDU) related to the disc, is correct. If D1 differs from D2, a positive or negative error signal will be generated, which drives a DC motor. This so-called tilt motor corrects the position of the LDU, until D1 equals D2.

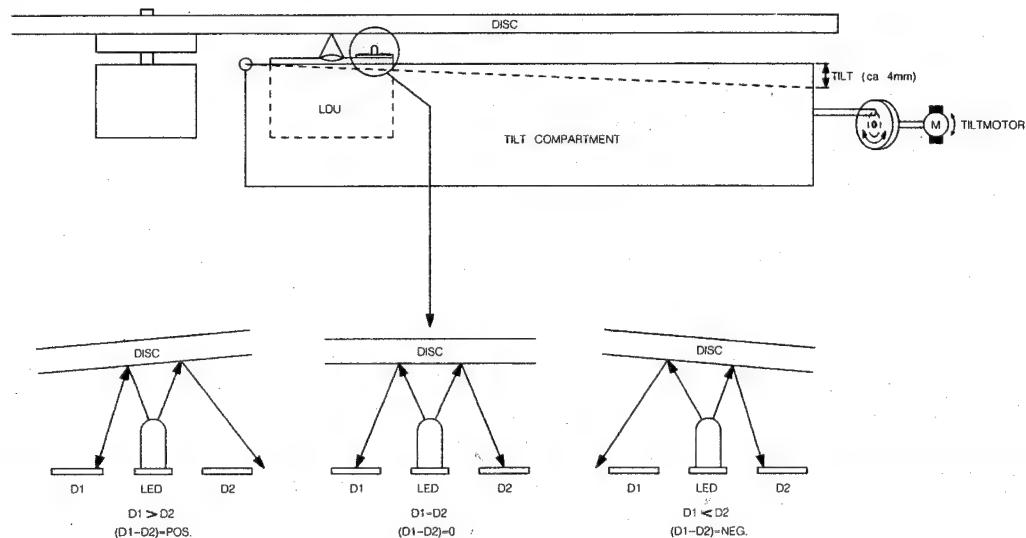


Fig.OD5 ACTIVE TILT CONTROL

PRS.01730
T-08 709

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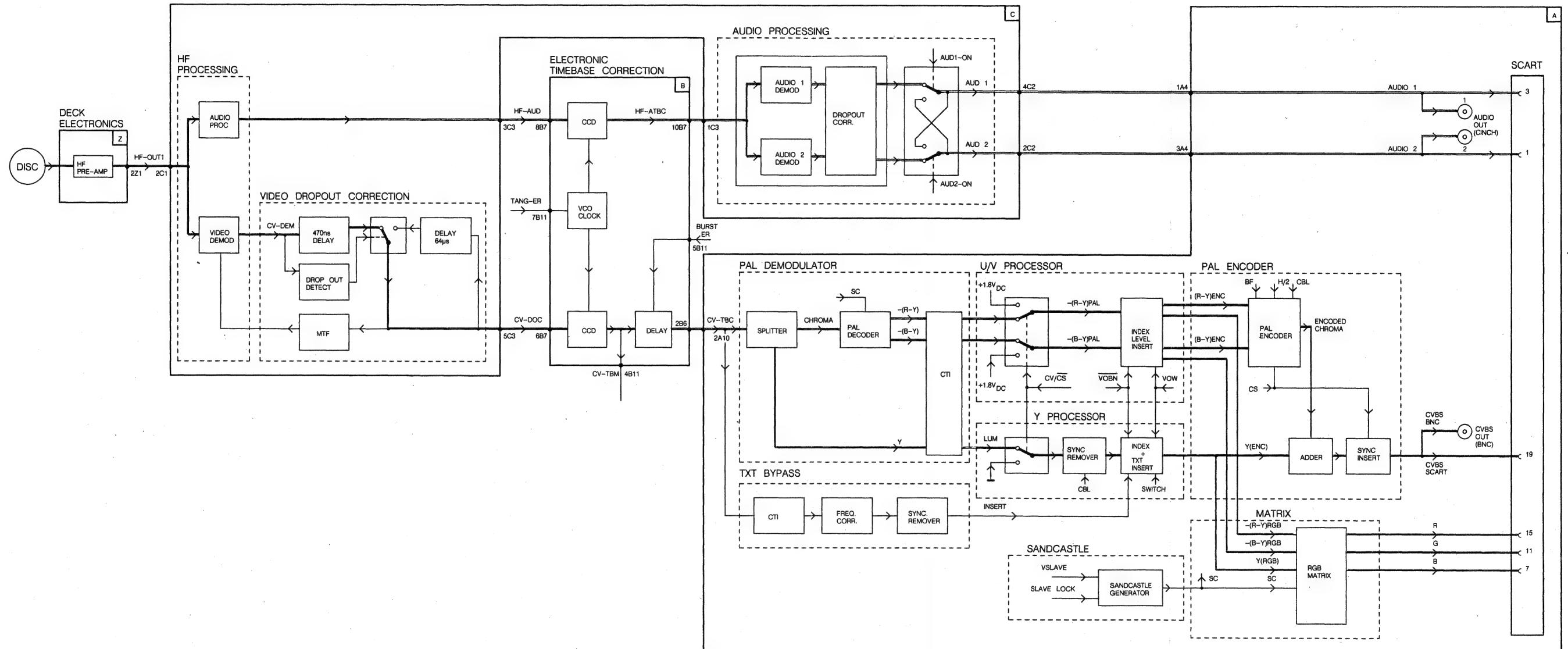
a luminance and a
signal is decoded
and B-Y and next
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same delay as the
processor the colour
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and (B-Y)ENC are
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present on a BNC
onnecter (pin 19).

of all circuits which
of the optical deck.

BLOCKDIAGRAM AUDIO/VIDEO SIGNALPATH VP406



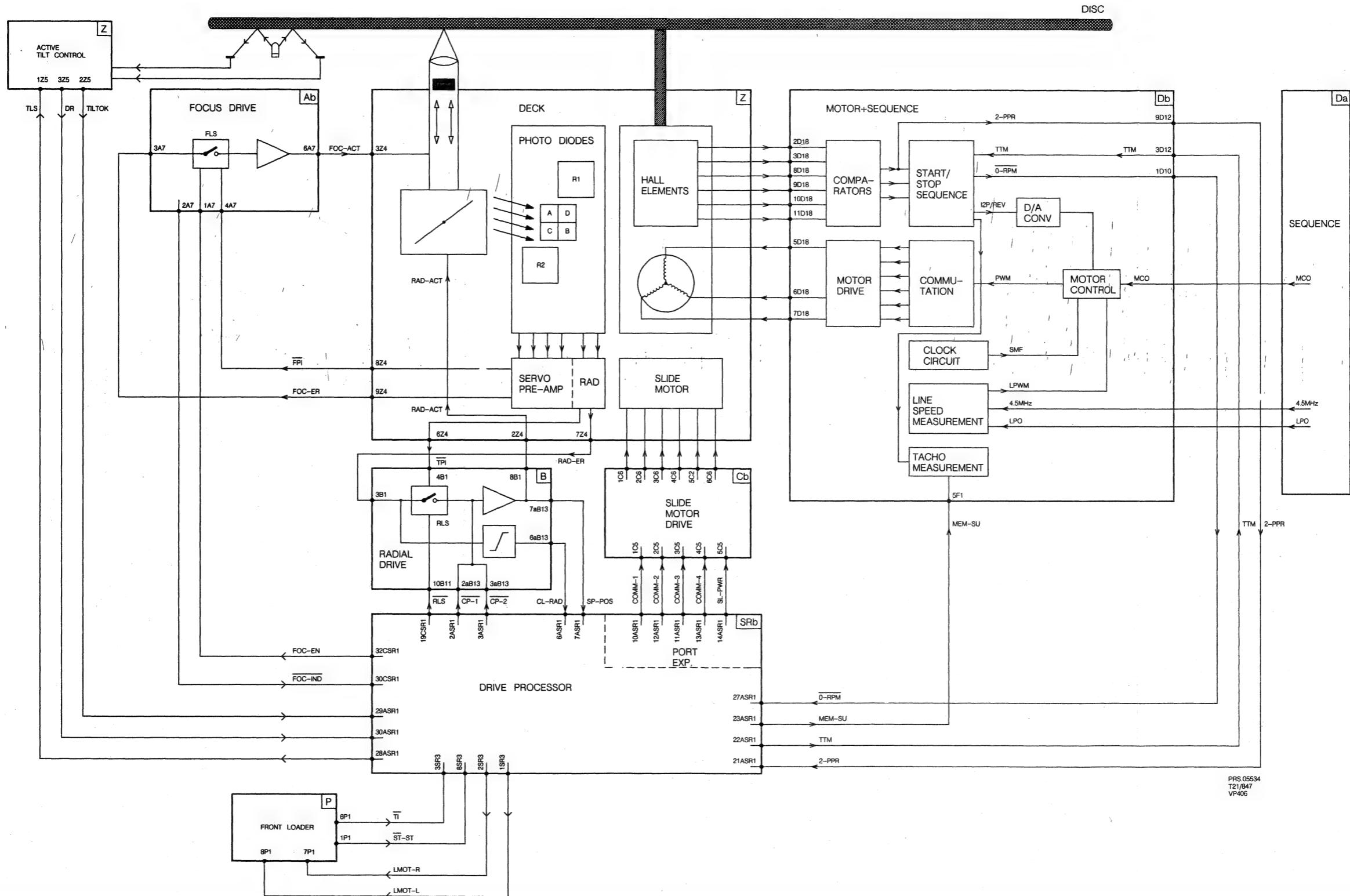
PRS.05535
T02/847
VP406

Short description

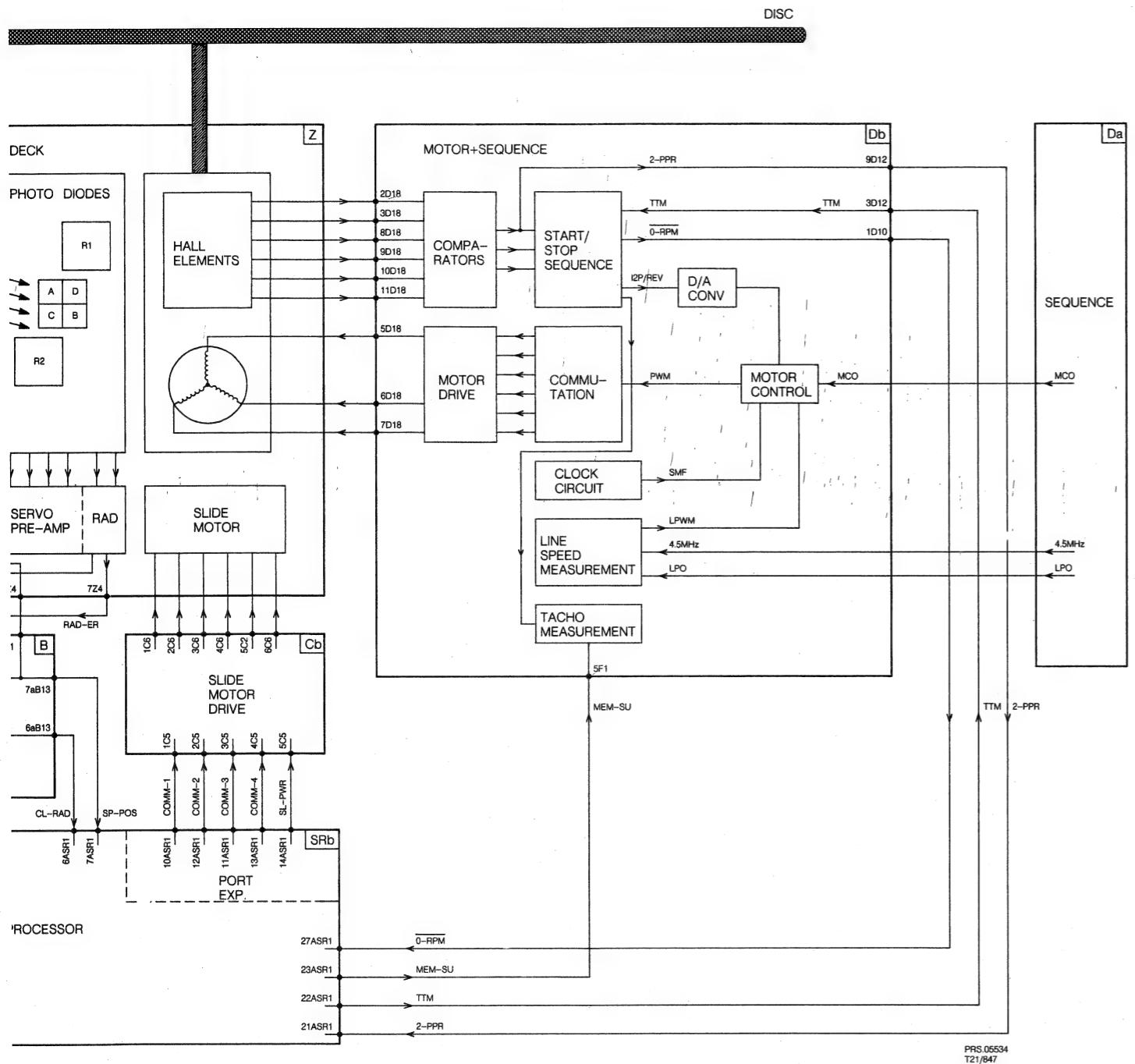
From the laser source on photodiodes A-D a laser light is converted to the servo preamplifier and the focus error signal connectors 8Z4-4A7 all circuit focus drive signal back to the objective v operate when focus error coming via 32CSR1-1. When the objective is f signal FOCIND "L" is fed processor SR.

From the radial part of signal RAD-ER is applied 7Z4-3B1 and tracking 6Z4-4B1. The output of fed via 8B1-2Z4 to the The radial circuit only signal RLS coming from case of jumps over one signal is coming from 2ASR1-2aB13 or 3aE1 clipped radial signal CI processor.

The drive processor controls motor by means of the 22ASR1-3D11 fed to the and when the motor is revolution) signal is fed. The drive processor also feeds 4 commutating signals 1C5-4C5 and a slide position signal 14ASR1-5C5 to the slide drive circuit the commutating drive signals for the slide supplied to the deck.

BLOCKDIAGRAM SERVO VP406

BLOCKDIAGRAM SERVO VP406



Short description

From the laser source a beam of laser light is projected on photodiodes A-D and R1-R2 on the optical unit. The laser light is converted into electrical signals and applied to the servo preamplifier and the radial amplifier. From the servo preamplifier a signal FPI (objective focussed) and the focus error signal are fed to the focus drive via connectors 8Z4-4A7 and 9Z4-3A7. In the focus drive circuit focus drive signal FOC-ACT is generated and fed back to the objective via 6A7-3Z4. This module can only operate when focus enable signal FOC-EN which is coming via 32CSR1-1A7 from the drive processor is "H". When the objective is focussed, the focus indication signal FOCIND "L" is fed via 2A7-30CSR1 to the drive processor SR.

From the radial part of the servo preamplifier radial error signal RAD-ER is applied to the radial drive circuit via 7Z4-3B1 and tracking position indication signal TPI via 6Z4-4B1. The output of radial drive RAD-ACT, which is fed via 8B1-2Z4 to the deck, controls the radial mirror. The radial circuit only operates when radial loopswitch signal RLS coming from the drive processor is "L". In case of jumps over one or more tracks, a CP1 or CP2 "L" signal is coming from the drive processor via 2ASR1-2aB13 or 3aE13-3AB19 and at the same time clipped radial signal CL-RAD is fed back to the drive processor.

The drive processor controls the start of the turntable motor by means of the TTM signal which is via 22ASR1-3D11 fed to the motor and sequence module F and when the motor is running a 2PPR (2 pulses per revolution) signal is fed back via 9D12-21ASR1. The drive processor also controls the position of the slide. This is executed by the output expander which feeds 4 commutating signals via 10ASR1-13ASR1 to 1C5-4C5 and a slide power signal SLPWR via 14ASR1-5C5 to the slide motor drive. In the slide motor drive circuit the commutating signals are converted into drive signals for the slide motor and via plugs 1C6-6C6 supplied to the deck.

Motor+sequence circuit Db takes care of the drive of the turntable motor. For control of this motor various signals are used, depending on the conditions. For running, condition the TTM signal is "H" and is fed to the block start/stop sequence. The start/stop sequence block also gets information from the Hall elements in the motor via plugs 2-11D18 and the comparator block. During acceleration only the TTM signal is operating and via the motor control block converted in a pulse width modulated signal PWM with a minimum duty-cycle. The PWM-signal controls the commutation block which is supplying 6 drive voltages to the three output stages in the motor drive block. The output stages are connected via plug 5D18-7D18 to the motor. When the motor reaches the speed of 1500 RPM, the acceleration is stopped by the D/A converter and the motor control is taken over by LPWM, a frequency control signal coming from the block line speed measurement. In this block the line frequency of the video signal on the disc is measured by means of LPO pulses supplied by the sequence circuit. After a short time, when the speed is within 5% of the correct speed, the motor control will be switched over to phase control. This is performed by the sequence circuit which then delivers the 15625 Hz dutycycle controlled MCO- signal to the motor control block.

In case there is a loss of focus during search, the drive processor delivers a MEM-SU signal via 23ASR1-8D12, which activates a memory in the tachocircuit and the information of the last motor speed will be stored. As soon as focus is correct again, the motor will speed up to the original velocity.

9 9 Fig. CR1 BLOCKDIAGRAM CONTROL ROUTES VP406

Control Routes

The control and drive section of the VP406 disc drive is determined by module SR. This module determines the actions of the disc drive which is composed of a number of functional circuits. See the block diagram of the control routes in Fig. CR1. The control processor and the drive processor communicate on this module.

- The **control processor** has interactions with the outer world via the RS232 connector (RS232-1 bus). The control processor controls the remote control communication (RC5); namely the wired RC5 commands, and the SCART-RC5 commands. Via line LED the led on the keyboard module N is driven.

- The **drive processor** has various main tasks:
 - a) To accept and interpret commands from the control processor parts.
 - b) Radial tracking and access
 - c) Manchester code reading
 - d) Display on screen drive
 - e) Start-up sequence of the disc drive
 - f) Local control: 'stand-by' and 'eject'.
 - g) Audio and video switching
 - h) Service diagnostics

sub a) Command inputs from and responses to the control part are dealt with on this module.

sub b) During start-up the voltage on the radial mirror is studied. By means of the actual mirror position the slide is displaced, if necessary, under certain conditions. The required signals of the radial drive circuit are SP-POS and CL-RAD.

sub c) The manchester code is present in the video read from the disc and gives information on picture numbers, chapter code, stop code and CLV code. This information is necessary for the drive processor i.a. to give the index contents, search actions and instant jump. The required signals of the ETBC circuit (Da) are VMANCH, HMANCH and CL-VID.

sub d) To give index information on a connected picture screen a character generator is present in the drive processor circuitry. Synchronized to the video signal present an index background signal (VOBN) and an index information signal (VOW) are inserted in the video signal on panel Aa.

sub e) **Start-up sequence.** The drive processor takes care of and checks the start-up procedure. After the disc has been inserted on the tray and the tray has been pushed in, the start-up procedure is actuated, provided the disc drive is in stand-by. The start-up sequence has been elaborated in timing diagrams, to be seen in Fig. CR2. The numbered steps in this sequence can be found back in the block diagram of the control routes in Fig. CR1. In this way one can see in which sequence the various circuits are energized by the drive processor. In the story below the required signals have been named followed by the number corresponding with the timing diagrams.

After the start, the pushing in of the tray with 'start-stop' ($\bar{S}T$ - S T: 1) as command, we see the following:

- * The pulling in of the front loader (LMOT-L: 2a) with as control the "tray inside" (\bar{T} I: 2b) signal.
- * Bringing the slide to the initial position (SL-PWR: 3a and COMM-1,2,3,4: 3b) with as control the 'slide position indication' (SPI: 3c) signal.
- * Detection of the presence of a disc by means of a photosensor and control signal 'disc reflection' (DR: 4).
- * Activation of the tilt control (TLS: 5a) with as control the 'tilt ok' (TILTOK: 5b) signal.
- * Switching on of the laser (LA: 6a) with as control the 'laser status' (LA-STA: 6b) signal.

* Activation of the focus control by means of the 'focus enable' (FOC-EN: 7a) signal. If focus is found, the deck electronics, module Z, give the 'focus position indication' (FPI: 7b) signal to the focus drive. This FPI signal gives together with the zero crossing of the 'focus error' (FOC-ER: 7c) signal, the control command for the drive processor, namely the 'focus indication' (FOC-IND: 7d) signal.

* The turntable motor is brought to the correct speed after the 'turntable motor' (TTM: 8a) command. The control is the '0 rpm' (0-RPM: 8b) signal.

* The loop for the radial tracking is closed with the "radial loop switch" (RLS: 9) signal.

* The motor is locked to the read-out video of the disc with as indication to the timebase correction circuit D, the 'motor lock' (M-LOCK: 10) signal.

* The synchronization of the video signal of the disc is then locked to the reference on panel A with as control to the drive processor the 'frame lock' (FRLOCK: 11) signal.

* The control of the timebase correction becomes active, resulting in a correcting signal, namely the 'tangential error' (TANGER: 12) signal. This signal goes from panel D to the ETBC circuit on panel B.

* The lead-in code is read by the drive processor by means of the HMANCH, VMANCH and CL-VID signals. The drive processor will give course pulses for the radial mirror up to picture 1 to the radial drive, which results in the 'radial error' signal as indicated (RAD-ER: 13).

* During start-up a sync signal is present on each video and sync output, derived from the slave source circuit on panel A. With the 'composite video / composite sync' (CV/CS: 14) command the video read from the disc is put on the outputs. On a connected monitor a picture with colour will appear (one short catch-in behaviour).

* The audio lines switch over, because of the 'audio 1 on' and 'audio 2 on' (AUD1ON, AUD2ON: 15) signals.

sub f) On the front of the disc drive you will find two keys, 'eject' and 'stand-by', which pass the related commands directly to the drive processor via display + keyboard module N.

sub g) The drive processor also takes care of the switching of the audio and video signals e.g. the muting of the signals during search actions.

sub h) The diagnostic software has been integrated in the drive software in such a way that many of the tasks of the drive are checked for proper performance. If a fault is detected in the execution of a task, an error code is shown on the screen as video overlay (like the index information). The software program is very useful on behalf of service diagnosing. The working and the use of this diagnosis software will be dealt with extensively in the REPAIR METHOD description.

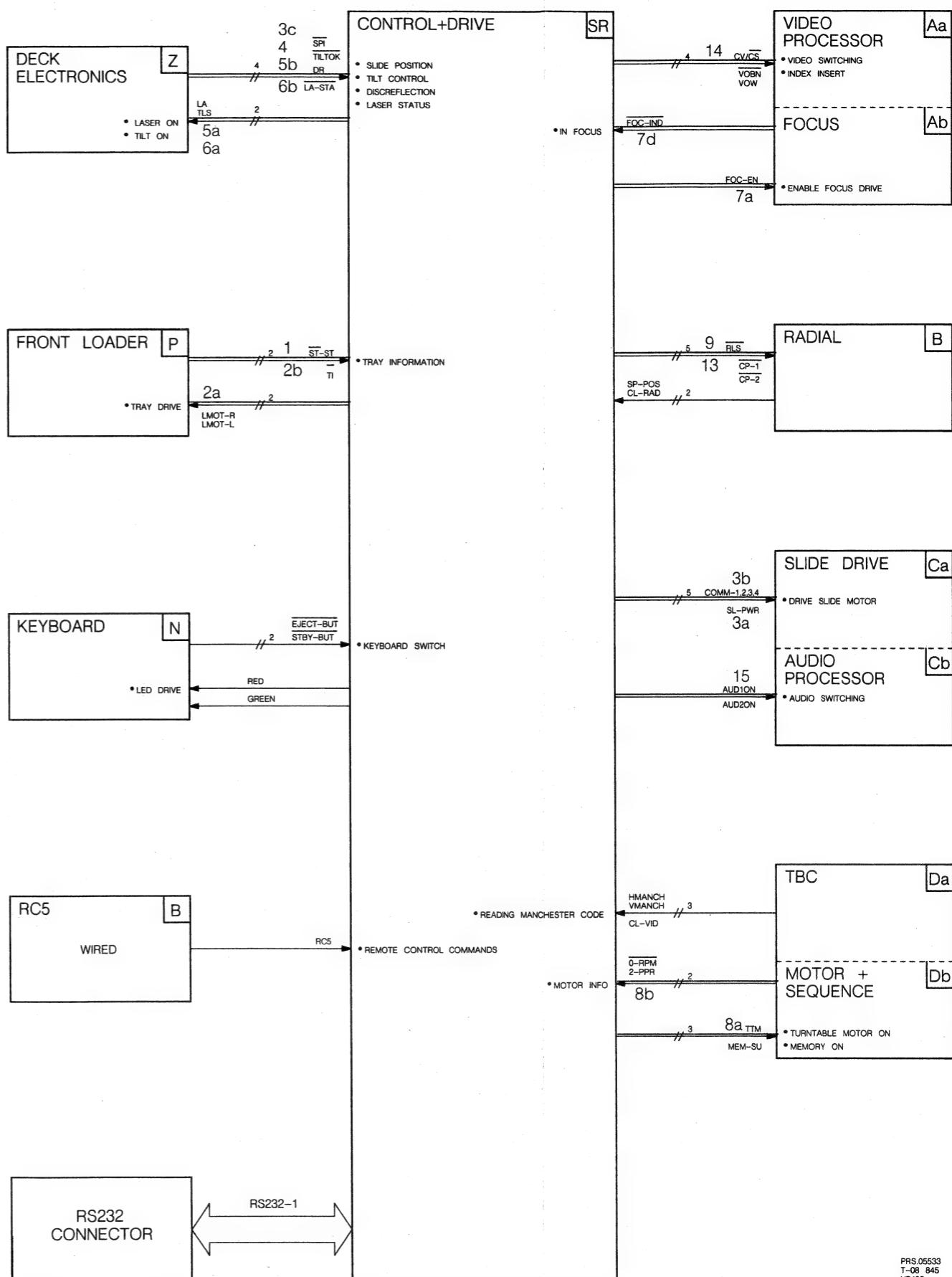
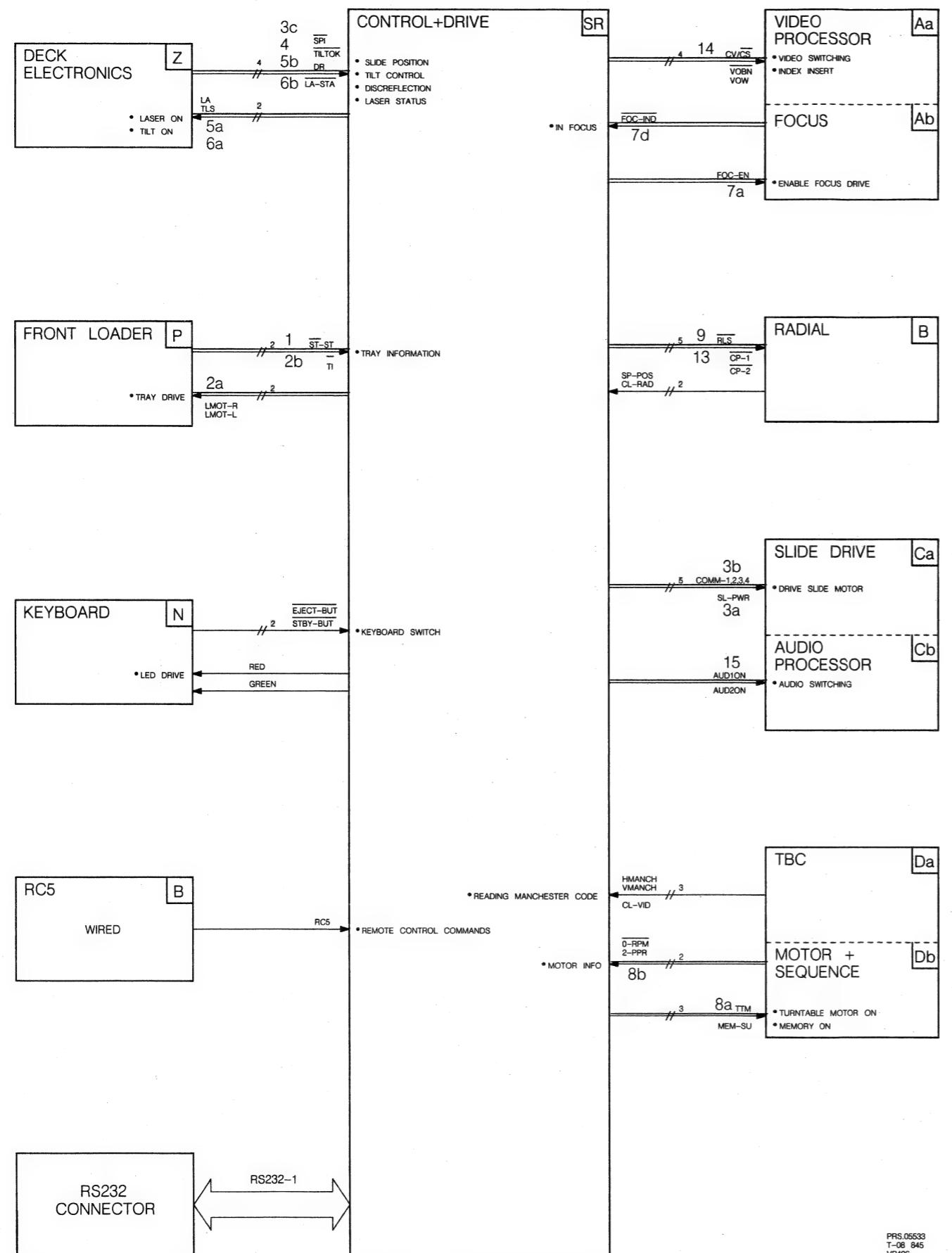


Fig. CR2 §

1. START
 - a. ST-S
2. FRONTLOAD
 - a. LMOT
 - b.
3. SLIDE DRIVE
 - a. SL-PW
 - b. COMM-1,2,3,
 - c. S
4. DISC
5. TILT CONTROL
 - a. TI
 - b. TILT
6. LASER
 - a.
 - b. LA-ST
7. FOCUS
 - a. FOC-E
 - b. F
 - c. FOC-E
 - d. FOC-IP
8. TURNTABLE
 - a. TT
 - b. O-RP

Fig. CR1 BLOCKDIAGRAM CONTROL ROUTES VP406



means of the 'focus us is found, the deck us position indication' This FPI signal gives the 'focus error' command for the drive ation' (FOC-IND: 7d)

the correct speed
a) command. The
signal.
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out video of the disc
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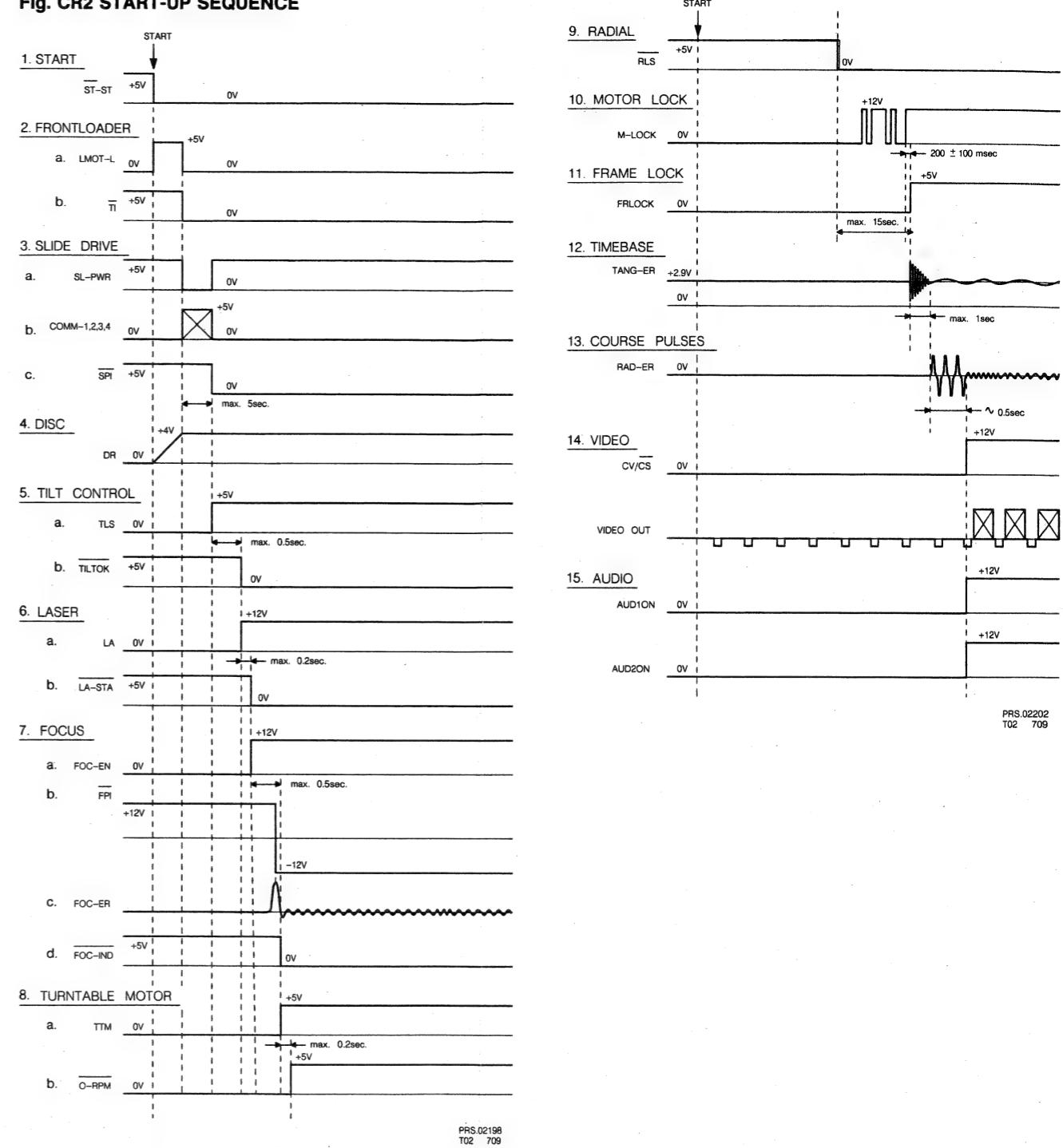
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D2ON: 15) signals.

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been integrated in
at many of the tasks
performance. If a
f a task, an error code
verlay (like the index
is very useful on
working and the use of
it with extensively in

Fig. CR2 START-UP SEQUENCE



S-BUS

The communication
the drive processor

The S-BUS is a system intended for use between controller. The bus is byte serial.
Bus activity is not continuous 'window' occurring in 8ms duration in each may not extend beyond termination of a window.

Commands are allo...

Priority 1: Manchester
du...
ac...

Priority 2: Asynchronous
co...
co...

Priority 3: Th...
ex...

Constraints on operation

For the S-BUS to operate correctly it must be locked to either the start in both line and field fields be readable.

Command and response

The data is organised in three byte strings.

A command frame consists of 1 packet

Responses may have different lengths. The length of a response depends on the number of packets required for the initialising sequence.

By way of example:

Packet 1: Manchester
Packet 2: Byte 1

Packet 3: Manchester
Packet 4: Byte 2

Byte 3
Byte 4
Byte 5

If the fifth packet is Manchester code from the controller. In the case of the packet containing all zero's codes are not read.

S-BUS

The communication between the control processor and the drive processor is via the S-BUS.

The S-BUS is a synchronous communication link intended for use between a LaserVision drive and a host controller. The bus is bi-directional with handshake and is byte serial. Bus activity is not continuous but is confined to a 'window' occurring in each video field. The window is of 8ms duration in each 20ms field period. Communications may not extend beyond the limits of the window. Execution of commands will commence following the termination of a window.

Commands are allocated a priority order:

Priority 1: More than one command may be sent during a window but only the last one accepted will be executed.

Priority 2: As for priority 1 but if a priority 1 command is included the priority 2 command will be ignored.

Priority 3: These commands will always be executed.

Constraints on operation

For the S-BUS to operate, the video from the disc must be locked to either the internal or an external reference in both line and field. Also the Manchester codes must be readable.

Command and response structure

The data is organised as packets each consisting of a three byte string.

A command from controller to drive processor module consists of 1 packet.

Responses may have a length of 0 to 5 packets, the length of a response being defined by a command from the controller in the form of - 05 00 0x where x is the number of packets required in the response. The initialising sequence calls for 4 packets.

By way of example the contents of these packets are :

Packet 1:	Manchester code from line 18.
Packet 2:	Byte 1 Disc loaded – CAV/CLV. Byte 2 Player mode. Byte 3 Error status.
Packet 3:	Manchester code from line 16.
Packet 4:	Byte 1 Laservision deck status. Byte 2 Audio/video status. Byte 3 Miscellaneous status.

If the fifth packet is requested this will contain the Manchester code from line 17.

In the case of the packets containing Manchester code information all zero's will be returned if the Manchester codes are not readable.

S-bus signals

Databus:

SD0-7 SD7 is MSB.

Signals to LaserVision drive:

<u>WREN</u>	Write enable (Write data to drive).
<u>RDEN</u>	Read enable (Read data from drive).

Signals from LaserVision drive:

<u>DAK</u>	Data acknowledge (Data has been read by drive).
<u>DAV</u>	Data available.
<u>WINDOW</u>	Drive can communicate.

CHAPTER 3 PANEL AND MODULE DESCRIPTION

A: VIDEO PROCESSOR PANEL

The video processor panel consists of the following circuit functions:

- PAL demodulator
- U/V processor
- PAL encoder
- Y processor
- RGB matrix
- Sandcastle generator
- Teletext bypass
- Slave source
- Focus drive

These functions will be discussed in the indicated sequence and can be found in the audio/video signal path block diagram. This does not apply to the focus drive. This function has been indicated in the servo block diagram.

PAL DEMODULATOR

Circuit description

First the incoming CVBS signal (CVTBC) will be split into a luminance and a chrominance signal. By filtering the CVBS signal on the emitter of transistor 7301, the luminance signal Y is present on the emitter of transistor 7302. Via bandpass filtering with L 5302 + C 2303 the chrominance signal is present on pin 9 of IC 7351.

Chroma decoding

The chroma signal will be decoded by IC 7351, PAL decoder, in an R-Y and a B-Y signal. The IC needs a crystal oscillator with a frequency of 8.86MHz (Cristal 5309) for chroma subcarrier generation.

Colour transient improver

The colour difference signals R-Y and B-Y are present at pin 1 and pin 2 of IC 7352 resp. This IC functions as colour transient improver. This means that the slope of the colour signal will be improved, from 800 ns to about 200 ns, thus giving a better visual impression.

The improved (R-Y) and (B-Y) signals are the output signals on pins 8 and 7 of IC 7352.

Because of the processing time required to improve the colour transient, some time delay will occur in these output signals (about 800 ns). The Y signal must have the same delay, which will also be realised in IC 7352. The output signals of IC 7352, the luminance signal Y and the colour difference signals (R-Y) and (B-Y), will go to the Y processor respectively the U/V processor.

U/V PROCESSOR

The two colour difference signals R-Y and B-Y, coming from the PAL demodulator, receive index information in the U/V processor. This implies that the colour difference signals receive a certain attenuation during the index information when we are dealing with the index background and are switched off with the index characters. Furthermore, the signals are switched so that a fixed DC level is transmitted during a mute action or a scan CLV action. The DC level corresponds with a black video picture.

These 3 different switching possibilities (video, mute and scan CLV) are realized by means of switching IC 7551 and switching signals CV/CS and NSVID. In the table below the various possibilities are shown.

	IC 7551	VIDEO	MUTE	SCAN-CLV
NSVID	L	L	H	
CV/CS	H	L	H	

In the 'video' selection mode, in case of colour difference signal -(R-Y)PAL, this signal is processed into -(R-Y)RGB on behalf of the RGB matrix and into (R-Y)ENC for encoding in the PAL encoder. In principle the same processing applies to the (B-Y) signal.

To (R-Y) applies: the signal enters at pin 14 of IC 7551 and is available as output signal at pin 13 of IC 7551, if selected. The normal signal path is via emitter follower 7506 to pin 5 of IC 7553 and, if selected, as output signal present at pin 3 of IC 7553. This signal goes to buffer circuit T 7512/7517 and as -(R-Y)RGB to the RGB matrix circuit. The amplitude of this signal is adjustable with R 3550. Via buffer circuit T 7511/7513 the transmitted R-Y signal also goes as (R-Y)ENC to the PAL encoder circuit. This signal too has an adjustable amplitude (R 3545).

During the blanking periods the R-Y signal will have to be laid at black level. This is realized by actuating switch IC 7452 with CBL, thus interconnecting the R-Y signal of pin 13 of IC 7452 with the reference voltage of pin 15 of the same IC.

The reference voltage has been derived from the DC voltage at the base of T 7505 and is via the emitter of T 7505 present at the base of T 7504 and T 7507. This reference voltage will thus be transmitted as output signal via pins 11 and 12 of IC 7551 in the selections of mute and scan CLV.

During the index background frames the R-Y signal will be transmitted from the voltage division caused by R 3529 and R 3532. This attenuated signal is namely present at pin 1 of IC 7553 and with the selection for index background also at output pin 3 of IC 7553. In case of the insert of the index characters (white level) the reference voltage at the base of T 7507 will be brought one diode porch lower. This signal, on the emitter of T 7507, is then as input signal of IC 7553 selected as output signal at pin 3.

PAL ENCODER

This part of panel A re-encodes (R-Y)ENC and (B-Y)ENC as a PAL chroma signal, mixes luminance and chroma. New syncs are inserted and the resulting signal output goes as CVBS to SCART and encoded CVBS to the BNC outlet socket. See the block diagram Audio / Video signal path.

Circuit description

Luminance processing

The luminance signal Y(ENC) arrives from the Y-processor. The Y signal will go via emitter follower T 7710 to C 2721. The luminance signal without syncs is available on the base of T 7717. In the meanwhile the luminance signal will be mixed with the encoded chroma signal via L 5703 and C2721. Unwanted chroma in the luminance signal will be filtered out via C 2721 and L 5703. New syncs are now added to the signal at the base of T 7715 from the CS signal (generated in the Slave source circuit), via T 7711/7712. The amplitude of the offered sync signal can be adjusted with potmeter R 3740, via T 7713.

The complete video signal (CVBS) will go via IC 7453-2A and the 2 emitter followers T 7715 and T 7716 to the outlet sockets SCART (pin 19) and BNC (CVBS out) resp.

Chroma encoding

Encoding of the chroma signal is taken care of by IC 7753. The (B-Y)ENC signal and the (R-Y)ENC signal are coming from the U/V processing circuit. The (B-Y)ENC signal is available on pin 12 of IC 7753, via T 7704.

The (R-Y)ENC signal will have the same process via T 7705 and is present on pin 5 of IC 7753. A crystal oscillator (5701) is connected to IC 7753 to generate the chroma subcarrier frequency of 4.43MHz.

In IC 7753 itself generation of 2 carrier signals with a relative phase difference of 90° (pin 2 and 14) takes place.

A signal with half the line frequency (H/2, from the Slave Source circuitry) is provided to pin 8 of the IC (square-wave form). This signal will take care of a 0° or 180° phase shift of the subcarrier signal to have the (R-Y) signal phase shifted 180° every second line.

The CBL (Composite BLANKing) signal is applied to switch ICs 7751. These switches can be closed by the CBL signal, which causes the (R-Y) and (B-Y) signals to be clamped to the voltage level of pin 10 of IC 7753 offered to pins 2 and 3 of IC 7751, via T 7703.

This is done to prevent chroma signals during the blanking period. In that period the dc-levels on pin 12 and 5 of the IC have the same level as the reference voltage of pin 10.

Because the colour burst also has to be generated, the BF (burst flag) signal will take care of pulse creation at the right moment. The amplitude of the pulse to be added is adjustable by potmeter R 3709 for the (R-Y) signal and by R 3705 for the (B-Y) signal. The dc levels will be added to the chroma difference signals via switch IC 7751. The dc level is derived from the reference voltage of pin 10 (via T 7702 and T 7701).

The signals of the (R-Y) modulator and (B-Y) modulator will be added, clamped to the reference voltage of pin 10 by the CS signal on pin 7, and made available as encoded chroma signal on pin 9 of the IC. The encoded chroma signal arrives via emitter follower T7707 on pin 15/11 of switch IC 7453. The other input is connected to ground. Whether there is an output signal available on pin 13 or not depends on the selection signals VOBN and SWITCH. If teletext data from the disc is inserted in the luminance signal via the teletext bypass circuitry, no insertion of chroma signals should be done. See the table for the selection overview. This encoded chroma signal will be inserted in the original luminance signal.

Y PROCESSOR

In the Y-processor circuit luminance signal Y, coming from the PAL demodulator, will be clamped at the correct black level, be muted or not and be provided or not with index information and teletext data. Moreover, the sync pulse is removed for correct transmission of the luminance signal. During further processing a defined sync pulse will be added to the luminance signal.

The LUM signal arrives via T 7401, potentiometer 3408 for amplitude adjustment and T 7402 at the base of T 7403. Via emitter follower T 7403 it arrives as input signal at pin 1 of switching IC 7451. This signal has received a black level at O V via FET 7404 and switching signal BPCLP. Switching IC 7451 is controlled by the CV/CS signal and, when the CV/CS signal is 'high', it will transmit the luminance signal to output pin 15. When the CV/CS signal is 'low', the output signal (pin 15) will lie at black level. For, this is the level of the other input of IC 7451 (pin 2). The muted or non-muted luminance signal arrives at the basis of T 7406, which is incorporated in the amplifier circuit with transistor 7407. The voltage level of the base of T 7407 lies practically at zero volt. As a result the level of this luminance signal below this 'clamping' level will not be transmitted to the base of transistor 7408.

Via this transistor and T 7409 the luminance signal is present at the base of T 7411. Sync pulse residues have been removed via switching IC 7452-2A. The luminance signal, without sync pulses, arrives via emitter follower T 7411 directly at input pin 4 of switching IC 7453. In attenuated form the signal is also present at input pin 2 of switching IC 7453. A third input signal at pin 5 is formed by the teletext data, coming from the teletext bypass circuit. This signal, INSERT, contains possible teletext data that might be present in the video signal of the disc. The switching possibilities of IC 7453 have been indicated in the table.

	VIDEO	INDEX FRAME	TXT
VOBN	H	L	H
SWITCH	H	H	L

The possibilities indicated are thus determined by the selection signal VOBN, for index background signal, and signal SWITCH, for TXT insert. In case of transmission of the luminance signal pin 4 will be interconnected with the output, pin 3.

Via emitter follower T 7413 and difference amplifier circuit T 7414/7415 the luminance signal arrives at the base of transistor 7417. The luminance signal of the emitter of T 7417, Y(ENC), is processed further in the PAL encoder. Via potentiometer 3465, for amplitude adjustment, and emitter follower T 7418 luminance signal is available as Y(RGB). This signal is used in the RGB matrix circuit. During the index background the luminance signal is transmitted in attenuated form. This amplitude attenuation is realized with resistors R 3449 and R 3450, because pin 2 of IC 7453 is interconnected with pin 3. The index characters, which are lying at white level, are via transistor 7415 added to the luminance signal. This is realized by means of the VOW signal.

In case of addition of TXT data to the luminance signal, pin 5 will be interconnected with output pin 3.

RGB MATRIX

In IC 7651 decoding takes place of colour difference signals -(R-Y)RGB, -(B-Y)RGB and luminance signal Y(RGB). These signals appear as input signal at pin 17, pin 18 and pin 15 resp. of IC 7651. Output signals R, G and B are present at pins 1, 3 and 5 resp. As buffered signals they are present at SCART pins 15, 11 and 7. The saturation, contrast and luminance levels of the output signals are fixed at the specified values for SCART. The DC level of the output signals is adjustable by means of potentiometer R3614, the black level of the video signal being the point of reference (0V). The condition here is that the outputs are shut off with 75 Ω. The SC sandcastle signal required for decoding arrives at pin 10 of IC 7651.

SANDCASTLE GENERATOR

The sandcastle circuit sees to generation of sandcastle signal SC on behalf of the decoding of the colour difference signals into R,G and B. SC is also necessary as input for the PAL demodulator circuit.

The signal for creating the clamp pulses is the burst key pulse which is separated from the sandcastle signal of pin 6 of IC7253, via T 7201. The clamp pulses (BPCLP) are needed for clamping of the black level of the video signal.

The sandcastle signal contains line frequency parts and frame frequency parts. The line frequency part is created in IC7253, the output signal of pin 6. The frame frequency part (V-SLAVE signal) is added to it via T7203.

The sandcastle signal can be adjusted to the correct horizontal frequency (15625Hz) with potentiometer R3213. In IC 7253 a square waveform signal (15625Hz) is generated, dutycycle 50%, and is available on pin 4. With the aid of circuit IC 7252-3A, -3B and -3C a duty cycle control of the block signal is made possible. The output signal of this circuit is fed back to IC 7253 (pin2) and takes care of the horizontal blanking duration in the sandcastle signal. The width of the horizontal blanking is of a fixed value.

TELETEXT BYPASS

The teletext bypass circuit is necessary in order not to loose the possible data in some video lines during frame blanking of the video of the disc, in the video processing section. The normal video signal is processed into RGB. During this process TXT data is lost. To prevent this from happening, the data of the complete video signal (CVTBC) is used for insertion in the luminance signal Y(ENC).

Circuit description

The CVTBC signal is the input signal for the colour transient improver IC 7150.

The IC is only used to give the video signal the same delay as the video to be processed, so that the timing of the insert is correct.

Via a frequency correction network consisting of T 7101, R 3118, 3146 and C 2112 the signal arrives via inverter T 7102 and emitter follower T 7103 at the emitter of T 7103. Here the black level of the video signal is clamped at 0V via FET 7107. This FET is driven by the BPCLP signal. The circuit with transistors T 7104 and T 7105 acts as sync remover as a result of which the signal at the emitter of T 7106 no longer has negative voltage components.

This is necessary for switching IC 7453 which cannot have negative voltage. Via this switching IC the insert will take place. In the encoded video signal a correct sync pulse will be added.

The moment of insertion is determined by the SWITCH signal. This signal is the output signal of NAND IC 7152. The input signals are: the CV/CS signal at pin 13, the output signal of the one shot IC 7151-2A (triggered by H-MANCH), and the output signal of one-shot IC 7151-2B (triggered by V-SLAVE).

As a result of this combination the SWITCH pulse will only during some data lines of the INSERT video signal, switch over switching IC 7453 to INSERT.

SLAVE SOURCE

The function of the slave source circuit is the generation of sync and timing signals for the video signal processing in the player. These reference signals have to be very accurate and are generated by sync generator IC 7061 with a feedback oscillator (5MHz).

During the start-up cycle of the player the sync generator will create the timing signals related to the free-running oscillator. The oscillator is readjusted dependent on the input signal of the sync generator, hence the name slave source. On behalf of the synchronism with the video signal of the disc a frame reset takes place, if necessary.

Thus, at the end of the start-up cycle, a unique lock-in performance can be observed in the video picture. The slave source circuit can be split in two parts:

- sync generator circuit
- frame reset circuit

Sync generator circuit

Sync generator IC 7061 has as output signals:

- BF Burst flag, in behalf of positioning of a mark at the correct place in the video signal for the encoding process (chroma burst).

- H/2 Square-wave voltage with half the line frequency to shift the phase of the R-Y phase every other line 180° during encoding
- V-SLAVE A sync signal having the frame frequency (vertical sync).
- H-SLAVE A sync signal having the line frequency (horizontal sync).
- CBL Composite blanking signal used to clamp the video signals at black level at the required places.
- CS Composite sync, in behalf of the insertion of a defined, clean sync pulse in the outgoing video signal.

These signals are buffered by IC 7062, where the voltage levels of BF and CBL are reduced from 0V/+8V to 0V/+5V by means of diode circuits D 6005 / R 3027 and D 6006 / R 3028.

Sync IC 7061 will generate the above-mentioned output signals as soon as supply voltage is present, thus also without input signal at pin 15. As soon as sync pulses enter at pin 15, the sync IC will adapt the frequency of the external 5MHz oscillator to the input signal by means of the DC output signal at pin 12. The input signal may come from two sources:

- Either the RAMP-EN signal from the reference source at PCB B acts as input;
- Or the HMANCH signal derived from the disc video acts as input.

This is determined by the NS-VID (non-standard video indication) signal, coming from Drive module SR, via PCB B. For, on module SR measurement takes place to see if the video signal from the disc is according to standard or not. Normally, this is the case, as with the use of CAV discs, under all conditions and then the NS-VID signal has a low level. If a CLV disc is used in the visible scan mode, the player will be unable to generate a standard video. In that case NS-VID is actively high.

If NS-VID is low, NAND gate 7058-4B is blocked for the other input, viz HMANCH. The output of NAND gate 7058-4C is high then and as a result NAND gate 7058-4A can pass on the inverted input signal at pin 1 of IC 7058-4A. This signal comes from one-shot IC 7060 which is triggered by reference signal RAMP-EN.

If NS-VID is high, NAND gate 7058-4A is blocked for the incoming RAMP-EN signal via NAND gate 7058-4C which is switched as inverter. NAND gate 7058-4B, however, is free now to pass on the inverted HMANCH signal as input for sync IC 7061. HMANCH has been derived from the disc video signal, so if the video signal is non-standard, the sync IC can also give "non-standard" timing signals.

Frame reset circuit

If necessary, the frame reset circuit generates a frame reset pulse to lock sync generator IC 7061 to the video signal of the disc. Input signals VMANCH (vertical sync) and HMANCH (horizontal sync) have been derived from the video signal of the disc, CV-TBM (timebase corrected). The input signal of the sync generator, RAMP-EN, has been derived from the reference on module D and sees to the drive of the turntable motor by means of the MCO signal after comparison with the CV-DOC video signal coming from the disc. This CV-DOC signal has not yet been corrected for timebase and might drift relative to CV-TBM. To prevent this from happening the frame reset is required.

The VMANCH signal is first inverted by IC 7051-3A, thus a negative-going frame frequency pulse is available as input signal for the 2 D flipflops 7054-2A and -2B. The clock pulses come from 2 one-shot ICs 7052-2A and -2B and have different pulse times.

Both one-shots are triggered by the line frequency HMANCH signal. IC 7052-2A gives a negative-going pulse of 1 µs and IC 7052-2B a negative-going pulse having a pulse time of 27 µs. The intention of the two crosswise coupled D flipflops is to generate a pulse of once every 2 frames.

The flipflops are switched in an asynchronous reset mode. One output signal comes from pin 9 of IC 7054-2B and goes to the input of shift register IC 7055.

Because this IC receives clock pulses with the line frequency (HMANCH), in this case the input signal will get a delay of 5x 64µs or 320µs. The output signal at pin 10 of IC 7055 triggers one-shot IC 7056-2A thus creating a positive-going pulse having a pulse time of 82µs and serving as D input signal of IC 7057-2A. This flipflop has been switched in an asynchronous set mode, implying that output Q1 remains "low" as long as the set input (determined by CS-SWITCH) is "low".

Normally the CS SWITCH is "high" but during "pause CLV" and "CLV scan" the CS-SWITCH signal will be "low" thus blocking the frame reset circuit.

The clock pulse input is determined by sync generator IC 7061 and is a frame frequency pulse. In this circuit these frame pulses give a "window" signal as output signal of flipflop IC 7057-2A which is compared in NAND gate 7058-4D with the frame pulse of pin 5 of IC 7054-2A. Via inverter 7051-3B a reset pulse will be formed when the frame pulse falls outside the window (no synchronism in frame frequency). This frame reset pulse triggers IC 7061 via pin 18.

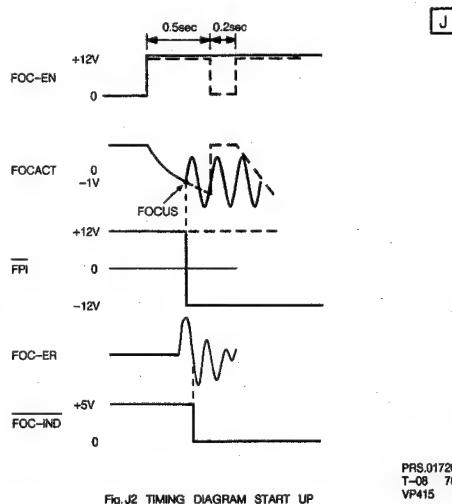
FOCUS DRIVE

The function of the focus drive circuit is to move the objective in starting condition up to such a position that the laser beam is focussed on the disc and to keep the spot focussed under all play conditions.

Circuit description

The objective is driven by amplifier transistors 7808-7811, which supply a positive or negative voltage FOCACT. Negative means that the objective is driven upwards to the disc and positive means that the objective is pulled downwards. The range of the objective movement is approximately 5mm.

When the player is started up (motor not yet turning), the focus enable signal FOC-EN is low and the focus position indication signal FPI from the deck electronics is high, resulting in 0 V on the objective (see timing diagram Fig. J2). As soon as the driving module detects a disc reflection (DR), a correct slide position SPI and a laser-on signal LA-STA, the FOC-EN will go high.



When FPI is still high, the drive voltage for the objective becomes negative causing the objective to go upwards. This movement is slowed down because of the feedback through filters 2806, 2807, 3815, 3816, 3817 and 3818. Switch 7805 is still open, which means that there is maximum gain (low negative feedback).

When the objective focusses the laser beam onto the disc, the FPI signal will go low, causing the focus loop switch (transistor 7806) to close and after that the focus indication signal FOC-IND to go low. FOC-EN remains high.

At the same time switch 7805 will be closed, which causes more negative feedback and as a consequence less gain. The FOC-IND low signal is applied to the drive module as a command that the turntable can be started. The objective is then driven by the focus error signal FOC-ER and is kept in focus by a negative voltage of average -1V on amplifier output 7808-7811.

When no focus is found, the FPI will stay high and the drive module switches the FOC-EN to low after 0.5 sec. The drive voltage becomes 0V and the objective will move downwards. After 0.2 sec the FOC-EN will become high again and will move the objective upwards. This sequence is repeated 5 times. If no focus is found, the player is switched to stand by.

If there is a minor disturbance in the reflection, FPI and consequently also FOC-IND will become high for a short moment.

The positive pulse on FPI causes a negative drive voltage on the objective and without protection the objective should move upwards. The function of one shot transistors 7814/7815 is to prevent this. The positive FPI pulse triggers the one shot and keeps via collector of 7814 the FOC-EN signal low and via 7817/6810 the drive voltage at 0V during 40 ms. During this time the objective will not move.

The FOC-ER signal is fed through a low pass filter with transistor 7801 to an AC/DC converter with transistor 7804 and diode 6801. The DC voltage drives the gain switch in the feedback circuit of the output stage. As soon as the FOC-ER signal increases up to a certain AC level, the AC/DC converter switches the gain switch to high gain of the objective drive. The increasing error current through the objective then causes an audible noise in the LDU. When a low FOC-ER signal occurs, the circuit switches to low gain, resulting in a smooth objective drive.

B: RADIAL + TBC PANEL

The radial and "time base correction" panel consists of the following circuit functions:

- ETBC signal processing
- Radial drive

These two parts are described here and indicated in the "audio/video signal path" block diagram concerning the ETBC function and in the servo blockdiagram concerning the radial drive.

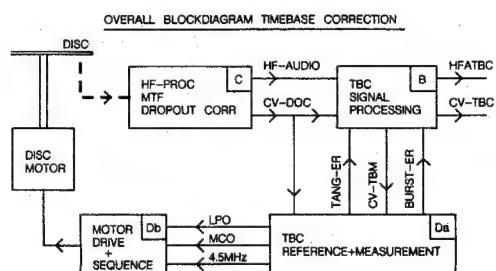


Fig.B1

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ETBC SIGNAL PROCESSING

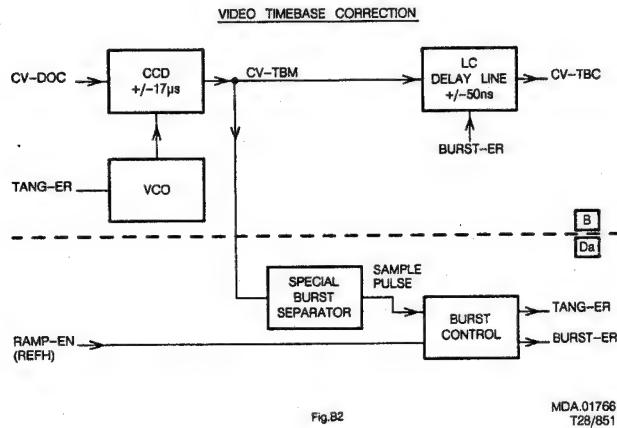
This circuit is part of the electronic timebase correction system (see block diagram overall timebase correction, fig.B1).

It is comprised of two CCD (charge coupled devices) delay lines to effect coarse correction ($+/- 17 \mu s$) and a variable LC delay lines to effect fine correction ($+/- 50 ns$) for the video signal processing.

Video and audio signals are treated separately, in parallel. IC 7401 is the CCD for the video channel and IC 7404 the CCD for the audio channel.

On this module the timebase of the drop-out corrected composite video (CV-DOC) is corrected. This is necessary because of the presence of several tolerances (disc, centring, motor) which cause variations on the line phase of the video signal read. The variations can be about $+/- 17 \mu s$ compared with the reference. This is unacceptable for video processing, so correction is needed. In the previous players the correction was realised in a mechanical way, the tangential mirror. In the new-generation disc drives the tangential mirror is not applied anymore. The timebase is corrected electronically. The ETBC circuit will have the timebase corrected comp. video signal (CV-TBC) as output signal for further video processing on panel A. Also it is necessary to have timebase correction of the audio signal (HF AUD), which is realised too on this panel. As a result the output signal is the timebase corrected hf audio signal (HFATBC).

Control of the time delay is by means of TANG-ER and BURST-ER both from the ETBC measuring circuitry on module D, see the blockdiagram in fig. B2.



Circuit description

Video timebase correction

The CV-DOC signal from panel C arrives at this panel on plug 6b7 and goes, via emitter follower T 7410 and a lowpass filter ($\leq 6.6\text{MHz}$), to the input of the CCD memory IC 7401. Lowpass filtering is necessary to prevent aliasing effects in the CCD. The video signal will get a time delay in the CCD depending on the frequency of the clock signal offered. The clock oscillator is connected to pin 14 of IC 7401 and functions as a voltage controlled oscillator (VCO), IC 7402.

The voltage offered is the measured error signal (TANG-ER) created on module D. The TANG-ER signal is present on plug 7B11 of this panel. As the clock rate is determined by TANG-ER, so the time the signal is delayed in the CCD's is also determined by TANG-ER.

This shows that as TANG-ER is a measure of the time error, a loop is set up which will compensate for timebase errors within the measuring accuracy of TANG-ER.

The frequency of the clock oscillator output signal is inversely proportional to TANG-ER and has a centre frequency of about 19MHz.

Referring to the anti aliasing phenomenon mentioned above it will be seen that low pass filtering of the input signal is required to eliminate any frequencies greater than half the clock rate.

In the CCD IC 7401 a flipflop is situated which acts as a :2 divider. The 2 output signals of this flipflop go to the 2 x 680 stages shift register, so the complete delay is 1360 stages for the video signal. Reading by the CCD memory happens every positive going edge of the flipflop output signals Q and Q.

The timebase corrected output signal of IC 7401 goes, via T 7460, to T 7461 to have a 3x amplification. The signal continues from the collector of T 7461, via emitter follower T 7462, to plug 4B11 as CV-TBM signal. For the system this signal is the measuring signal to create the error signals in the ETBC measuring circuitry on module D. On that module a comparison takes place of the measure signal and the reference signals, see also fig. B2. So this is the feedback loop of the timebase correction mechanism.

At the same time the signal of the emitter of T 7460 goes, via T 7470, to a steep lowpass filter ($\leq 7\text{MHz}$). This filter is realised by coils L5470.....L5476 and the varicap diodes D6471.....D6476. The filter circuit provides the video signal with a delay time of 200ns and depending on the voltage on the varicap diodes another $+/- 50\text{ns}$. This depends on the BURST-ER signal. Lowpass filtering is also necessary to prevent switching noise of the CCD.

In the video path there is some high frequency loss in the CCD. This is compensated for with a high pass network in the emitter of T 7480 giving a rising response of about 6dB between 2 and 4MHz. From this network the video signal will be available on plug 2B6 as CV-TBC signal, via amplifier T 7480/7481 and emitter follower T 7482.

The BURST-ER signal is present on plug 5B11 and goes, via potentiometer R 3490, to the + input of opamp IC 7405-2A. From the output of this opamp the signal goes, via voltage follower IC7405-2B, to the varicap diodes of the variable LC delay line.

Dependent on the voltage offered the delay time will change, and this with a maximum of the above-mentioned $+/- 50\text{ns}$. The functioning of this circuit can be seen as a fine correction of the timebase errors.

Audio timebase correction

The HF-AUD (high frequency audio) signal from panel C arrives this panel on plug 8B7. The audio signal goes, just like the video signal, via a lowpass filter to a CCD memory IC (IC 7404). The audio signal needs timebase correction too.

The clock drive for the shift register is driven by the clock signal coming from flipflop IC 7403-2A. The input signal of the flipflop is realised by the same VCO as used for the video path.

The flipflop IC 7403-2A is used as :2 divider. The clock frequency can be half the value because of the lower number of stages used (680 instead of 1360). The time delay will be the same as for video, but the passband of the audio signal is lower.

Via amplifier stage T 7450 and emitter follower T 7451 the timebase corrected hf audio signal is available on plug 10B7 as HFATBC signal.

RADIAL DRIVE

The function of the radial drive circuit is, to supply the required current to drive the radial mirror in such a way that the laser beam is kept on the required track, depending on the various play modes.

Circuit description

In the normal play mode the radial error signal RAD-ER, originating from the deck electronics and proportional to the deviation of the laser beam relative to the track, is applied to the radial loop switch RLS transistor 7002 via a phase compensation network and a limiter IC 7100-2B. The radial loop switch, which is driven by a signal from the microprocessor 7201 on the CODRIVE module, is only closed when a track is followed. The radial error signal is then amplified in IC 7100-2A and via the output stage transistors 7010-7013 fed to the radial mirror. As the range of the deviation of the mirror is limited, the drive signal of the mirror is also applied via a level shifter IC 7101 to the drive processor. In this way too high a deviation will be compensated for by a displacement of the slide. The level shifter converts the signal, which may vary both to a positive and to a negative value, into a positive signal with the same variations.

In special play modes, the laserbeam jumps across one or more tracks. This is realised by giving the laser beam, with the aid of the radial mirror, a fast forward or reverse deviation. For this fast deviation use is made of the course pulse CP-1 for a forward jump and CP-2 for a reverse jump. The course pulses are also fed to the radial amplifier in IC 7100-2A. During a jump, the radial loop switch is opened by the RLS signal. The number of tracks that will be crossed in this way depends on the duration of CP-1 and CP-2 respectively. Both CP-1 and CP-2 are delivered by the CODRIVE module.

As an indication of how many tracks are crossed, the RAD-ER signal is fed to a clipper circuit in IC 7102 and converted into a square wave clipped radial signal CL-RAD. The number of pulses of the CL-RAD signal, which indicates how many tracks are crossed, is fed as "count pulses" to the microprocessor on the CODRIVE module. In case of a jump across more than 15 tracks the radial mirror will get a high speed and about every 25 microseconds a track will be crossed. The CL-RAD signal has a frequency of about 40 kHz.

The TPI signal "L" on track causes switch 7003 to be closed when the beam is on track. The input voltage of the radial amplifier is present across capacitor 2014. When the beam loses track, the switch will be opened and the voltage remains on capacitor 2014. As soon as the beam is on track again, the initial input voltage for the radial amplifier is equal to the last voltage before the beam lost the track.

C: HF + AUDIO PANEL

The hf + audio panel consists of the following functions:

- HF processor
- Audio processor
- Video dropout correction
- Slide drive

These functions will be described in this part. In the "audio/video signal path" block diagram the functions can be found in relation to each other. The slide drive is not in the signal processing part, but is a separate function.

HF PROCESSOR (diagram Ca)

The h.f. signal of the disc will be splitted up into a video and an audio signal in this circuit. The h.f. signal goes to the h.f. video processor section.

After a highpass filter an adaptation of the frequency response will take place there by means of the MTF voltage. This is necessary dependent on the read-out diameter of the disc. The corrected h.f. video signal will be demodulated in IC 7220-3A. After filtering and amplification, output signal CV-DEM will be available for further processing in the drop-out correction circuit.

The h.f. signal also goes to the h.f. audio processor where the audio is filtered out by means of a lowpass filter. Output signal HF-AUD will be timebase corrected on panel B.

Circuit description

The h.f. signal is first filtered by LC circuit 5203, 2214 and 2215. The h.f. signal will be used for the video part from the collector of transistor 7205. Therefore filtering is necessary by highpass filter (≥ 2 MHz) 2204, 2205, 2206 and 5201. Via amplifier stage 7202, 7203 and 7204 the h.f. video signal is available on the collector of transistor 7204. In the collector circuit of 7202 an LC circuit is situated, tuned to a frequency of 8 MHz.

The LC circuit will be damped more or less depending on the value of the MTF signal. So the MTF signal will via transistor 7201 take care of adaptation of the frequency responses.

Demodulation of the h.f. video signal takes place in IC 7220-3A with an adjustable output amplitude with the aid of potentiometer 3243. At point 16 of IC 7220-3A the demodulated video is available which will give a composite video signal (CV-DEM) after lowpass filtering (≤ 5 MHz) and amplification by IC 7220-3B.

The h.f. audio signal will be obtained from the emitter of transistor 7205. This is realised with the amplifier stage in feedback mode, 7206, 7207 and 7208 and the lowpass filter (≤ 2 MHz) in the collector circuit of transistor 7206. This filter consists of 5204 and 2219, 2220 and 2221. The h.f. audio signal is available at point 3C3 of the panel.

AUDIO PROCESSOR (diagram Cb)

On this panel the hf audio signal (time base corrected) will be split up and demodulated into the 2 possible If audio signals. Drop out correction takes place for both channels. On/off switching of one or both of the audio signals is possible in this circuit.

The hf audio signal, time base corrected, (HFATBC) comes from the ETBC circuit on panel B. This signal is fed through 2 identical circuits for both audio channels. Only some values of the applied components differ because of the different subcarrier frequencies (audio-1:683kHz, audio-2:1066kHz). Only the circuit for audio 1 will be discussed.

Circuit description

The timebase corrected HFATBC signal goes from connector 1C3 via bandpass filter 5106 (684kHz) to pin 1 of demodulation IC 7115-3A. First of all the signal passes through the limiter and goes as square-wave to the demodulation block via 2 paths. Namely internally as direct signal to the demodulation block and also via pin 7 to an externally applied lowpass filter on behalf of 90° phase shift. The latter signal enters the IC again via pin 8. The demodulated signal is present at pin 6. This signal still contains residues of the double carrier frequency which is filtered out with the lowpass filter (28kHz) around L5103. The audio signal is adjustable in amplitude by means of potentiometer R3114 and enters the IC again at pin 10 (IC 7115-3B). There it first receives an amplification of approx 8 dB and then it passes via an internal drop-out switch through an internal buffer. This has been done in order not to load external drop-out hold capacitor C2128.

Via the internal mute switch the signal arrives at the next amplifier (12dB) and is then available at pin 15 as output signal. After the de-emphasis ($75\mu s/2\text{kHz}$) by R3138/C2146 the signal arrives at pin 14/11 of multiplexer IC 7116. This IC acts as external mute and double-throw switch. In this IC the audio-1 signal can be switched on to the output (pin 13) or, via the double-throw switch, to the output of audio-2 (pin 1 to pin 3). This switching depends on switching signals AUD1ON and AUD2ON. The table below gives the possibilities.

	stereo	audio-1	audio-2	mute
AUD1ON	H	H	L	L
AUD2ON	H	L	H	L

The audio-1 signal, or possibly audio-2, will then be available at output pin 13 of multiplexer IC 7116, receives via IC 7117-2A an amplification of about 5 times and is then present at the cinch connector at the rear of the set as low-frequency audio signal. The internal mute switch is driven by AUD1ON via transistor 7104, but does not act as double-throw switch.

Drop-out correction

In the IC drop-out detection takes place separately for the two audio signals and this in two ways:

- **DO1.** First of all drop-out detection takes place in IC 7115-3A on the high-frequency signal by establishing by means of a window whether the highfrequency carrier is present or not (DO1). If the carrier falls within the window, a drop-out pulse will be present at pin 12 which will be lengthened slightly by C2120 and is then used to drive the internal drop-out switch.

- **DO2.** The demodulated audio signal at pin 6 of IC 7115-3A is also studied. Via the sensitivity adjustment with R 3106 the signal is, via T7100, fed through a filter which filters out both the double carrier ($2x684\text{kHz}$) (with notch filter L5102/C2122) and the lowfrequency audio signal itself ($<20\text{kHz}$). For, if there is a drop-out, this will cause interference outside the audio band. The filtered signal goes via pin 11 to the internal DO2 block. There it is judged if the signal falls within a window and if so, the drop-out switch will be driven. The window is lying at 2.9 and 2.95V. The reference for this window arrives at pin 17 of IC 7115-3B, derived from the internal voltage stabilizer of 2.95V (pin 27 of IC 7115-3C).

Drop-out correction takes places according to the track and hold principle with RC network R3120/C2128 at pin 13 for the audio-1 signal and with R3135/C2139 at pin 18 for the audio-2 signal.

VIDEO DROPOUT CORRECTION (diagram Ca)

This circuit takes care of drop-out compensation of the demodulated video signal and of generation of the MTF signal. The drop-out detector circuit measures a negative going drop-out and in case of a drop-out it will give a pulse to switch over the DO switch to have the delayed video as output signal. This will be the case as long as there is drop-out. The drop-out pulses can be blocked by the DO-INH signal. This is necessary to prevent drop-out correction during the data part of the video signal. Drop-out correction is only done with the luminance signal. The luminance signal is fed to the CCD memory part, which takes care of the $64\mu\text{s}$ delay (one linetime).

The DC RESTORER will take care of clamping of the dc level of the delayed video to the dc level of the direct video with the aid of the burst key pulses. The MTF signal is also created in this circuit.

This MTF signal is a dc voltage which will vary in value depending on the read-out diameter of the disc. This voltage is used to adapt the frequency response of the hf signal in the hf processing circuitry.

Circuit description

Direct video

The demodulated video signal (CV-DEM) is obtained from the demodulator part and arrives on the base of transistor 7401. Via the emitter of 7401 the signal goes via a delay line of 470ns (5401) to the amplifier stage 7402, 7403. The signal goes via emitter follower 7404 to the drop-out switch IC 7220-3C. If there is no drop-out, the video signal will, via emitter follower 7405, be available at plug 5C3.

Drop-out detection

Drop-out detection will be realised in the drop-out detector formed by IC 7450. The demodulated video goes via emitter follower 7406 to the pos.input of the opamp IC 7450, which is applied as comparator. Under normal conditions the output of the opamp is high (+12V). As soon as the pos. input will come under the switch level as a result of a drop-out, the output will become low (0V). If the video signal has no drop-out, the video level will be normal, the pos. input of the opamp will be high again. In that way a pulse is created which goes, via transistor 7407 in order to obtain the right amplitude (6V) and polarity, to pin 10 of switch IC 7220-3C.

Delayed video

Realisation of the delayed video is done in the following way. The drop-out corrected video signal (CV-DOC) is also fed to the base of transistor 7414. In the emitter circuit a lowpass filter ($\leq 2\text{MHz}$) is provided to separate the luminance signal. The luminance signal is fed to the CCD memory IC 7451, which takes care of the $64\mu\text{s}$ delay. The output signal will be made proper again with a lowpass filter ($\leq 2\text{MHz}$) in the collector circuit of transistor 7417 and will, via transistors 7418 and 7419, be available on the emitter of transistor 7421 as video in case of a drop-out. The CCD memory needs a clock signal, which is realised with the 13.4MHz clock generator circuit (7422, 7423). The frequency can be adjusted with coil 5407 to have a delay of exactly $64\mu\text{s}$. The DC RESTORER mainly consists of switch FET 7420 which brings the dc decoupled delayed video from the base of transistor 7421 via filter 5406 at the dc level of the direct video. This is done during the DEM-BK pulses (burst key) that are connected with the gate of FET 7420.

MTF circuit

The drop-out corrected video signal (CV-DOC) goes, via resistor 3443 and capacitor 2410, to the base of transistor 7409. In the collector circuit of this transistor a circuit (5403/2412) which is tuned to 4.43MHz is situated. The 4.43MHz signal will, via emitter follower 7410, go to the source of FET 7411. The gate is driven by the burstkey pulses (DEM-BK) from panel B. Transistor 7411 is only conducting during the burstkey pulses, so on the drain of this FET only the colour burst is available. The burst signal will via capacitor 2414 go to the base of transistor 7412.

The burst voltage is clamped to 0.7V by the base-emitter junction of transistor 7412, so in case of a small burst the average base emitter voltage is higher than with a large burst amplitude. Consequently a large burst causes less collector current. So the collector voltage will increase and the dc-voltage across capacitor 2416 is a measure for the amplitude of the burst signal. This voltage can vary between 2V and about 10V and goes to the hf video processor circuitry. This circuit is incorporated in a closed loop thus causing continuous adaptation.

SLIDE DRIVE (Diagram Cb)

The slide drive circuit controls the slide drive motor. The function of the slide drive motor is to move the LDU under the disc in such a way that the tracks can be read out in an optimal way.

Circuit description

The slide is driven by a stepping motor. Each step moves the slide by about 50 track spaces. The motor is driven by means of pulses on COMM 1-4 and SL-PWR which switches the motor coils between holding and moving power levels via an astable multivibrator with transistors 7602, 7603.

The drive signals are provided by the drive processor, module SR, via panel B.

D: MOTOR SEQUENCE + TBC MODULE

This module consists of the following functions:

- ETBC reference
- ETBC measuring
- Motor + sequence

The motor + sequence function can be found in the servo block diagram. For the timebase correction functions mentioned see block diagram "overall timebase correction".

ETBC REFERENCE & MEASURING (diagram Da)

This circuit is part of the electronic timebase correction system (see block diagram "overall timebase correction", fig.B1). Its primary function is to measure the timebase error and provide coarse (TANG-ER) and fine (BURST-ER) correction control signals to panel B. The TANG-ER signal is used in a feedback loop for coarse correction (+/-17μs) and the BURST-ER signal in a feedforward loop to give the fine correction (+/-50ns), so together the required accuracy.

The CV-TBM signal is coming from the ETBC signal processing circuit on panel B and is the composite video signal for measuring the timebase error.

The turntable motor is driven by a duty-cycle controlled signal (MCO), the output signal of the reference circuitry formed by IC 7251-2B driven by accurate cristal oscillator 5201 at a frequency of 4.5 MHz. This frequency divided by 288 is exactly the line frequency of 15,625 Hz (the reference). In IC 7251-2B the video signal from the disc, CV-DOC, will be compared with the reference and dependent on the difference measured, the MCO signal varies. So for slow variations in the video signal frequencies, the motor speed will be adapted. During reading of the information, the timebase of the video signals will vary rapidly, which is impossible to correct with the motor speed. So extra timebase correction is needed and is realized electronically.

Error measurement is obtained from the special burst, a 3.75 MHz signal during sync pulses. This inserted signal can only be found in the video signal from the disc, also see the block diagram in fig. B2.

Circuit description

Special burst separator + gate

The special burst is extracted from CV-TBM by T 7321, L 5320, C 2314 and is available at pin 1 of switch IC 7354-4A via emitter follower T 7322. The special burst signal is gated by the syncs from pin 6, IC 7353-2B at pin 13 of switch IC 7354-4A.

T 7326, T 7327 act as a 'special burst presence' detector, the collector of T 7327 going high if a special burst is present. The special burst is applied via T 7323, T 7324 to input 4, IC 7355-2A.

Sample detector

The sample detector sees to delivery of a sample pulse signal which is an accurate measure for the frequency of the disc video. This is realized by looking at exactly the same zero crossing of the special burst signal each line time.

The special burst signal is fed to one shot IC 7355-2A, pin 4. Pin 6 of this IC will change over to a high level as soon as pins 4 and 5 are high and pin 3, the reset input, is high too. The latter will be realized via one shot IC 7355-2B and T 7335. The input signal of this IC is the composite sync signal derived from the disc video (CS-TBC). This composite sync signal thus triggers one shot IC 7355-2B, which in its turn delivers a defined pulse at pin 10. Via T 7335 this pulse sets one shot IC 7355-2A free. Dependent on the pulse time at pin 3, which is determined by C 2333 and R 3347, one shot IC 7355-2A will be reset (low level at pin 3). One shot IC 7355-2A will be active after release at pin 3 and will give a pulse at pins 6 and 7 on the next zero crossing of the special burst signal. T 7328 ensures the selection of the correct zero crossing with respect to the line sync.

Tangential phase detector

The line frequency signal of pin 5 of IC 7251-2B (REFH) goes to the base of T 7330. This signal will let T 7330 conduct at high levels thus discharging C 2352. Via C 2350 the output signal of IC 7355-2A, pin 7, will appear on the collector of T 7339 as sample pulse signal.

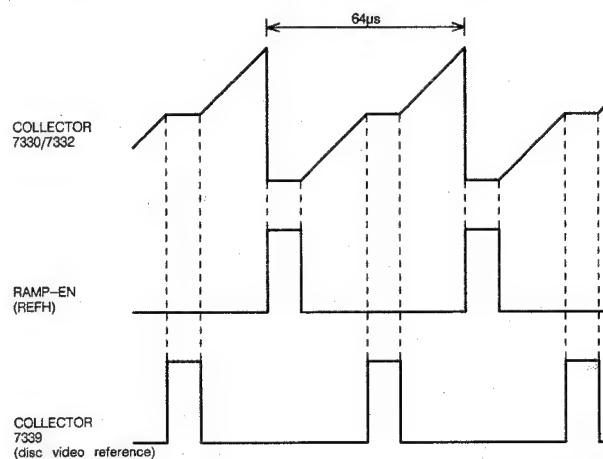


Fig. D4

MDA.01785
T28/851

The sample pulse signal indicates exactly where a fixed zero crossing of the special burst signal is situated. The frequency of the sample pulse signal can be seen as an accurate measure for the line frequency of the disc video signal. Via R 3353 this pulse is present at the base of T 7332 and will let this transistor conduct in case of low levels. As a result C 2352 will be charged via R 3354. This causes a certain sawtooth signal on C 2352. The total picture of charging and discharging can be seen in Fig.D4.

This sawtooth signal goes to input pin 4 of switch IC 7354-4B via voltage follower IC 7356-2A. This IC samples out the platform level in the sawtooth voltage. This voltage level will then be present at C 2354. When the zero crossing of the special burst takes place, switches 7354-4B and -4C are turned on, loading a new voltage into C 2354. The value across C 2354 is in proportion to the timebase error as measured from the special burst. Should the phase relation between the line sync signal and the sample pulse be disturbed, the result will be a level change of the platform in the sawtooth signal. Thus a dc-change at C 2354 and thus a change in the BURST-ER signal via opamp IC 7356-2B and a change in the TANG-ER signal via IC 7357-2A.

It is important that timebase correction is disabled during the start-up sequence until motor lock (frame lock, FRLOCK) has been reached. The BURST-ER and TANG-ER signals are clamped to a mean value until this moment. This mean value is realized with the aid of R 3386/3387 and switch IC 7354-4D. For the TANG-ER signal it also depends on the position of potentiometers R 3392 and R 3385/3389. The switch signal at pin 6 (pointed with A) is coming from output pin 10 of IC 7351-4C. This IC gets input signal M-LOCK from pin 19 of reference synchronization IC 7251-2B. The M-LOCK signal is of a high level if the motor speed is in lock with the reference signal.

IC 7353 also provides the CL-VID, HMANCH and VMANCH signals. These signals are necessary for decoding the manchester codes in the video signal from the disc.

The circuitry with the ICs 7351/7352 is used to prevent timebase correction if the special burst signal fails for a number of lines and also if the motor goes out of lock. The output signal of the special burst presence detector, the collector signal of T 7327, goes ultimately to IC 7352-4D via IC 7352-4A to block the sample pulse (collector T 7339). The FRLOCK signal is fed to pin 2 of IC 7351-4A (marked with B), and will block the sample pulse if FRLOCK is not active (low).

MOTOR + SEQUENCE (Diagram Db)

The circuits on this panel take care of the drive of the turntable motor. See the servo block diagram. The turntable motor is of the brushless type provided with Hall elements. The main groups on the board are:

- The MDS-IC 7152. This IC takes care of the communication between the motor and the other circuits and delivers the required drive voltages to the output amplifiers of the motor.
- The Hall elements which are continuously passing the position of the motor via comparators to the MDS-IC.
- Pulse-width modulator IC 7151-2A which is converting the drive voltages into a duty cycle controlled input pulse for the MDS-IC
- The output stages which are supplying the required drive currents to the motor coils. These currents are derived from the commutating voltages supplied by the MDS-IC.

Circuit description

For a proper functioning of the turntable motor, several input signals are required:

- TTM, the 'turntable motor on' signal which is "H" in the start and play modes and delivered by the drive processor
- MCO, a duty cycle controlled pulse which is originating from the reference circuitry on module D and only active in the locked mode.
- MEM-SU, Memory start up, a logic "H" signal in case of focus loss on the CLV disc in the search mode. The last tacho information is then stored in a memory. As soon as the laser beam is focussed again the motor will accelerate until the last speed before focus loss is reached .

Start mode

In the start mode the TTM signal is "H" and is fed to pin 27 of the MDS-IC. This causes speeding up of the motor. Pulse-width modulator 7151-2A compares the control voltage with a sawtooth signal derived from the clock circuit in IC 7152. The frequency is about 17.6 kHz. The sawtooth voltage is obtained by the generator consisting of transistor 7023, capacitor 2030 and resistor 3031. It will be clear, that the the duty-cycle decreases when the d.c. control voltage increases. When the required speed of 1500 RPM has been reached, speed control will be taken over by the duty-cycle controlled MCO-signal via IC 7154-2A.

Active braking

When TTM goes "L", the MDS-IC is brought in the active braking mode. When the turntable motor comes to a complete stop, all driver inputs are disabled.

F : SUPPLY MODULE

The supply module which is suitable both for 220 V and for 110V has the function to feed stabilised dc voltages to the various circuits in the disc drive. These voltages are obtained in a self oscillating power supply (SOPS). The supply circuit is protected against overload by a power limiter and against overvoltage by a thyristor circuit. Mains separation is realised by an isolating transformer T901, while the voltage error control is obtained by a feedback from the secondary to the primary side of the transformer via optocoupler H 501.

Circuit description

The mains voltage is filtered against mains interferences by C1101–L1101–C1108 and rectified by bridge rectifier V1101. The switching-on current is limited by NTC-resistor R1103.

Connector X1101 serves to select 110V or 220V. In 110V mode the rectified mains voltage is present across R1101–C1107 and in 220V mode across (R1101–C1107) + (R1102–C1106) + R123.

The non-stabilised output voltage from the bridge rectifier is used as supply voltage for the SOPS.

The initial base voltage for switching transistor V101 is obtained by voltage divider R1101–R1102–R123. The switching transistor is conducting and causes an increasing current through V101 and S3 of T901. The increasing current induces a voltage across winding 4–9 (S1) of T901 which drives V101 via V114 – V116 – V117 – R114 – R104 into full saturation.

The current through V101 flows also through parallel resistors R111 – R112 – R116 – R117 – R126, causing an increasing voltage which is fed to the base of transistor V107 via C104–R107 and C103. Transistor V107 is part of a thyristor circuit. When this thyristor circuit is ignited, V101 will be cut off. As the voltage across winding S2 is rectified by V104, capacitor C103 will be charged negative causing the thyristor circuit to be blocked again. A new cycle can start. The repetition frequency is about 100 kHz.

Output voltages

The various positive and negative output voltages +13, +5SB, -5SB and -13 are obtained by single-phase rectification of the output pulses on secondary windings S4–S7 of T901. These output voltages are smoothed by C–L–C pi-filters.

Error correction

Error correction is performed by measuring the +5SB voltage via R501 – R503 – R507 – R508. The voltage across R503 is applied to a programmable zener diode N501. The current through this diode flows also through optocoupler H501 and depends on the gate voltage of N501. This current is converted into a current in the transistor part of H501. A part of the emitter voltage of H501 is fed to the base of V107 via C103. An increasing voltage at this point causes the thyristor circuit to ignite earlier, so that the duty-cycle of V101 is decreased. The correct output voltage +5SB can be adjusted by potentiometer R508.

Power limitation is obtained by measuring resistors R111 – R112 – R116 – R117 – R126, while too high a voltage across these resistors also causes V101 to block via thyristor circuit V107–V108.

Overvoltage protection

For overvoltage protection the +5SB voltage is applied to the gate of thyristor V703 via V702 and zener diode V701. As soon as the +5SB voltage exceeds 5.8V, thyristor V703 will be ignited and causes an overload on +5SB. In consequence, the overload protection circuit becomes active and the power will be switched off.

Stabilised output voltages

The +12SB output voltage is derived from +13 and stabilised via a MOS-fet series regulator V807–V808. The gate reference voltage for V807/V808 is obtained from peak rectifier V806–C806 and reduced by R801 and a programmable zener diode N801. The reference voltage is adjustable by R805.

-12SB is derived from -13 and stabilised by series regulator V601. The gate voltage of V601 is obtained via programmable zener diode N601, transistor V602 and transistor V603. The correct value is adjusted by potentiometer R605. If +12SB fails, then automatically V601 is blocked and -12SB is switched off too.

MODULE P - FRONTLOADER

The purpose of this module is to provide the required drive current to the motor of the front loading mechanism, which takes care, that the disc is positioned at the correct place in the player. Control signals are fed in from the drive processor module SR and status signals are fed back to the drive processor. See Fig. P1.

FRONT LOADER CIRCUIT

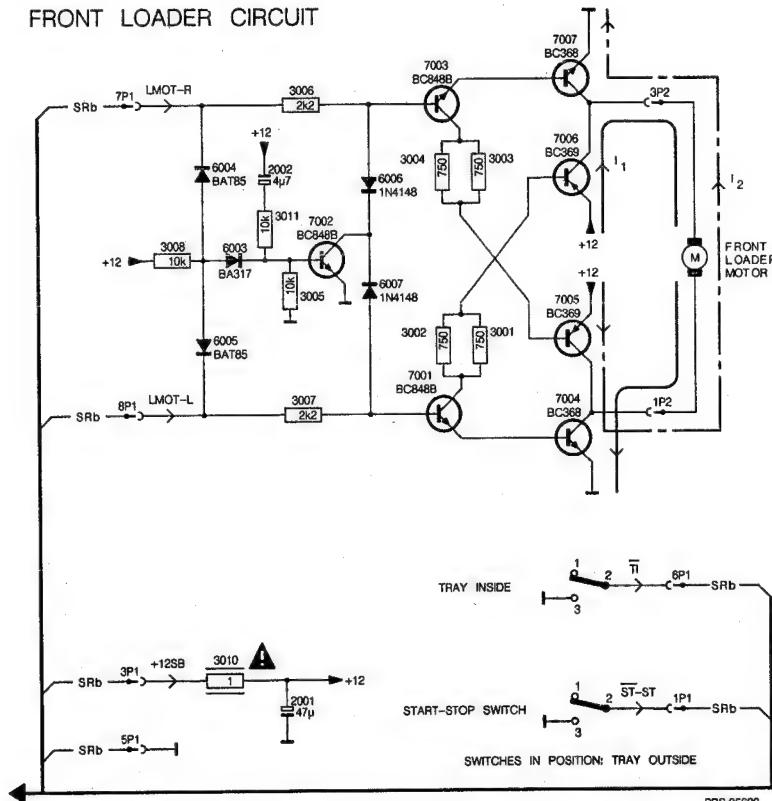


Fig.P1

PRS.05622
T2B/851
VP406

Circuit description

The front loader motor is a d.c. motor, which can be driven in two ways, for loading and unloading respectively. Therefore the motor is connected to a bridge circuit. See Fig. P2.

Loading: When the tray is partly pushed in, the start stop switch is connected to ground and ST-ST signal "L" is fed to drive processor SR. At this moment the LMOT-L signal from drive processor SR becomes "H" and transistors 7001, 7006 and 7004 will conduct. This causes current I1 to drive the motor and the tray will move further inside. When the tray is fully inside, the "tray inside" switch is closed and TI becomes "L". LMOT-L becomes "L" again and all transistors are cut off. The motor will stop.

Unloading: When "EJECT" is pressed, the drive processor delivers an LMOT-R signal "H". Now transistors 7003, 7005 and 7007 will conduct and the motor is driven by current I2. As I2 is in direction opposite to I1, the tray will now move outwards. This continues until the ST-ST switch is open again and ST-ST signal "H" is fed to the drive processor. LMOT-R becomes low and all transistors are blocked again.

Protection device: When the tray is blocked during loading as well as during unloading, the LMOT-L and LMOT-R signals become "L" and the motor is not energized anymore.

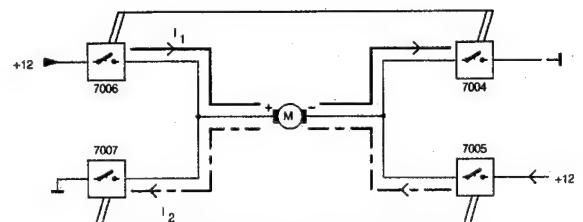


Fig.P2

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T02/708
VP415

SR: CONTROL + DRIVE (CODRIVE) MODULE

On a number of points the drive software has been adapted for the specific VP406 environment. These adaptations refer to e.g. the changing frame pulse which is presented to the drive. The main part and functioning of the codrive circuitry is similar to the control and drive circuits of the VP410, in which 2 separate modules were used instead of 1 like in the VP406. Although the circuitry has been realized on 1 module, the circuit diagram is split up into 2 diagrams, the control part on diagram SRa and the drive part on diagram SRb. See the block diagram in Fig. SR1 to understand the functioning of the CODRIVE circuitry.

The main tasks of the **control processor part (SRa)** are:

- To communicate with the drive part via the S-bus
- To provide an RS232 interface between the player and an external computer
- To interpret the RC5 commands via the UPI
- To drive the indication leds

All control functions of module SR run under control of micro processor IC 7102. A 64k EPROM is used for the control software (IC 7105) and a 8k RAM memory IC 7106 for e.g. the programmed sequence in the index frame. Because of the required 16 address lines and the 8 bit data bus, address latch IC 7120 is used for the lower address lines. The address latch is controlled by the ALE signal (address latch enable). Dependent on the various chip select signals the ICs will be activated or not, so no problems with corresponding address lines.

sub a) S-bus communication

The S-bus communication is byte serial with a bi-directional data flow under control of the handshake principle. For a detailed description please refer to the S-bus section in chapter 2. The S-bus interface can be found on diagram SRb. For more information also see the description in the drive part.

sub b) RS232 communication

The RS232 is the serial computer interface, in accordance with the international communication standards. Communication is fully duplex, with a selectable baudrate of 9600 or 1200. Selection can be done with the push button at the rear of the drive (released 9600 bauds, depressed 1200). The input and output buffers of the RS232 interface are formed by IC 7114 and 7115 respectively. For more information see the operating instructions.

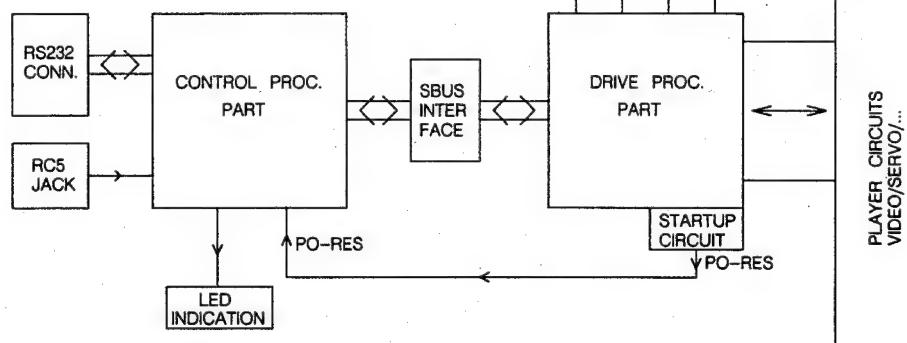


FIG. SR1 BLOCKDIAGRAM CODRIVE MODULE

sub c) RC5 communication

RC5 commands can control the disc drive via the wired input at the rear of the drive. Infrared communication is optional but activates the same input of the UPI, pin 1 of IC 7103.

sub d) LED drive

Output pins 2 and 3 of microprocessor IC 7102 drive the LED at the front of the player, which is a 2-in-1 LED lighting up in green or red dependent on the 2 drive signals 'GREEN' and 'RED'. There are 4 status possibilities:

- 'Stand-by' indication: continuously red.
- 'Start-up' indication: blinking red.
- 'On' indication: continuously green.
- 'Eject' indication: blinking green.

Watchdog

The watchdog circuitry is formed by the retriggerable monostable IC 7117 and provides a power on reset and also gives a reset if hang up of the program occurs or if the local stand-by key is pressed. In the latter case a software reset is performed. Under normal conditions the IC 7117 is continuously retriggered giving a non-active reset signal. With power on or if the program crashes, the circuit is no longer triggered and generates a reset active signal.

The main tasks of the **drive processor part (SRb)** are:

- To accept and interpret commands from the control part
- Radial tracking and access
- Manchester code reading
- Display on screen drive
- Start-up sequence of the disc drive
- Local control: 'standby' and 'eject'
- Audio and video switching
- Service diagnostics

All drive functions of module SR run under control of micro processor IC 7101. A 16k EPROM is available on this module (IC 7104).

Disc drive communication takes place via 2 I/O port expanders, ICs 7107 and 7108. Various drive and switching signals are given by the drive processor via 2x8-bit shift registers ICs 7109 and 7110. The drive processor reads the manchester codes of the video signal (clipped video) and also sees to insertion of the index signal.

sub a) Control communication

The design of the VP406 is such that the control and the drive are running on 2 separate processing circuits. The S-bus protocol as realized in the VP41X is valid. The S-bus interface comprises ICs 7108, 7121, 7122, 7123, 7124. IC 7108 is a port expander by which processor IC 7201 accesses S-bus handshake signals DAV and DAK. IC 7122 is the data input buffer latch and IC 7121 the data output buffer latch. DAV and DAK are serviced via D-type flip flops 7123-2A and -2B. For detailed information on the operation of the S-bus please refer to the S-bus section.

sub b) Control of the slide motor

Control of the slide motor takes place via software. The slide motor is a stepping motor driven by the 4 phase signals COMM-1 to COMM-4 and SL-PWR which are output by port expander IC 7107. During normal play functions the slide motor is driven when the deflection of the radial mirror is approximating its limit. This is determined by measuring the mirror offset via comparison of SP-POS (radial error from the mirror drive) with the output of digital to analog converter IC 7111 in IC 7127-2A. The result of this comparison (RAD-MIR) is applied to input pin 31 of port expander IC 7108.

sub c) Reading Manchester codes

IC 7113 is a dedicated device which reads Manchester codes from the clipped video signal CL-VID. The code data is stored on-board to be read by the processor via the data bus. Signals required are:

- Handshake from processor IC 7101:
ATN, TX/RX, STB an IRQ
- Horizontal sync:
HMANCH
- Vertical sync:
VMANCH
- Clipped video:
CL-VID

sub d) Display on screen

Status information from the manchester codes for display on screen is read from IC 7113 by processor IC 7101 and loaded into display driver IC 7112. This IC contains the character generator for on screen display.

Inputs to IC 7112:

	Pins
Databus	14-21
Reset	1
H SYNC	8
V SYNC	7
LDI (load index)	12

Outputs from IC 7112:

VOBN (background for insertion)	pin 6
VOW (character for insertion)	pin 5

For normal index situations background signal VOBN and white character signal VOW are separate output signals. In the case of external character insertion, background is needed during the characters. This is realised with the aid of ICs 7124-4D and 7126-6E.

sub e) Start-up and control

The start-up procedure has been dealt with in chapter 2 sub 'control routes + start-up sequence' by means of a block diagram with command signals (Fig.CR1) and timing diagrams (Fig.CR2). Here the interaction with the various circuits is discussed.

The start-up sequence operates under control of processor IC 7101 via output buffers ICs 7109, 7110 and I/O port expanders 7107 and 7108. Buffer 7109 operates with +12V supply so the input signals are first converted by level converter IC 7118. Buffer 7110 works directly with +5V supply. The start-up consists of the sequence: Close tray, move slide to start position, detect disc, activate tilt control, switch laser on, find focus, spin disc, close radial tracking loop and find picture number 1. During start-up it is determined which type of player we are dealing with (PAL or NTSC). This is done by determining the distance between successive VR pulses over a number of periods. These VR pulses are the derivatives of the V-SLAVE pulses of the slave source circuitry. The measured period time is studied within certain limits (windows) and next the system is evaluated. If the VR signal is missing, the player will not start up.

sub f) Local control

Once activated, the 'stand-by' and 'eject' keys on the front of the player give a low level signal directly to I/O port expander IC 7108. The drive processor will respond to this signal.

sub g) A/V switching

The drive processor sees to switching on and off of the audio and video signals, not only during start-up but also during normal play procedures. It is e.g. necessary to mute audio and video during search actions, realized with the AUD1ON, AUD2ON and CV/CS signals respectively.

sub h) Service diagnostics

The diagnostic software has been integrated in the drive software in such a way that many of the tasks of the drive are checked for proper performance. If a fault is detected in the execution of a task, an error code is shown on the screen as video overlay (like the index information). The software program is very useful for service diagnosis. The working and the use of this diagnosis software is dealt with extensively in the REPAIR METHOD description.

Watchdog and power-on reset

IC 7116 is a watchdog circuit which provides a reset for the processor on power up and also monitors the operation of the processor giving a reset if the program crashes.

The power-on reset (signal **PO-RES**) for the motor control circuit does not come from the watchdog circuit but via a circuit which monitors the power supply voltage (+5V). This has been realized by means of C2059, R3004, R3005 and T7001. In this way backward running of the motor is not possible if an EPROM signal is missing. The enable signals of shift registers IC 7109 and 7110 have also been derived from this circuit. As soon as the player is started up the shift registers will be held at the tri-state level in order not to get an undefined start-up.

Finger protection

To prevent the user's fingers from getting jammed in the front loader tray, a finger protection circuit has been added, which generates an 'eject' command as soon as the front loader tray meets an obstacle. In that case the current through R3014 will increase so that T 7009 and T 7004 will conduct and the EJECT line will go low.

Foreground processes

Every frame (20 ms) the drive software goes through a number of procedures. These procedures are called foreground processes and are accomplished in a fixed sequence.

3 Different main levels can be distinguished in which foreground processes are running:

- main0 : during standby and when the disc has not yet reached the desired speed during the start-up sequence,
- main1 : when the disc has been loaded,
- main2 : during the diagnostic program.

Some foreground processes are called at a fixed point of time in every frame, for instance the loop-switch switching procedures.

The last foreground process of a frame in main0 and main1 is the reference test procedure. Every frame this procedure will synchronize the drive software to the next frame.

During main0 and main1 the watchdog is triggered at fixed points of time. The time difference between these two results in the window signal for the external world. The watchdog is triggered during a foreground process. If a number of subsequent frame pulses are missed by the reference, the test procedure will result in a reset pulse from the watchdog circuit and the entire drive board will be reset.

Background processes

Background processes are organized from timer 0 and timer 1. These background processes see to the real-time operations such as instant jump and tracking. Timer 0 also sees to the division of the frame pulse in slices.

Frame pulse

In the VP41X the presented frame pulse is not subjected to interference thanks to the genlock circuit. At all times it is certain that the frame pulse will be generated every 20 ms.

The VP406 has no genlock circuit.

Upon switching-on of the power supply a frame pulse is presented by a slave source circuitry. The slave source too generates a neat frame pulse every 20 ms. In the beginning this frame pulse is running "free". At certain moments this free-running slave source has to be synchronized to the frame pulses coming from the disc. This synchronization has to be started from the drive with a switching signal: the switching from 0 to 1 of the CS-SWITCH composite sync switch. The switching from 1 to 0 of this signal has no consequences.

Practice has shown that the synchronization of the slave source to the disc can take place within 4 frame pulses after the switching from 0 to 1 of CS-SWITCH.

During 4 frames it will be possible that one of these frames lasts less than 20 ms. Naturally, this has consequences for the synchronization of the drive software to the frame pulse which has to be realized every frame.

The moments at which the slave source has to be synchronized to the disc are:

- end of start-up sequence (criterion loaded)
- at the end of the CLV scan and CLV goto, when the drive assumes the play mode, with muted picture, searching for the correct time code.

The switching to 0 of the CS-SWITCH has to be done at the following moments:

- upon initialization of the drive,
- upon an unload,
- or when a CLV goto or a CLV scan action is started.

Synchronization drive software

After initialization of the drive and just before the main0 path is gone through for the first time, the drive software should for the first time be synchronized to the frame pulse by the reference test procedure.

Synchronization of the drive software to the frame pulse shows a specific VP406 performance during the transition from main0 to main1 (the loading) and at the end of a CLV goto (or scan). Within 4 frames the slave source can be synchronized to the frame pulse coming from the disc.

MODULE Z - DECK ELECTRONICS

The Deck Electronics consist of the circuitry to process the signal from the LDU and the Active Tilt Control. The circuits are built on a PCB, situated under the optical deck chassis. The LDU is connected to this PCB by means of a flex-foil connection. For the block diagram of the LDU signal processing see Fig.Z1.

Circuit description

The laser supply

The Solid State laser is supplied by the +5V through a controllable DC amplifier. The laser emits part of the light to the optics and part to an internal monitor-diode. This diode measures the amount of light and feeds the monitor information back to amplifier T 7005 via T 7002, 7003. In this way, a constant current through the laser is realised. The monitor signal also drives switch T 7004, causing the LA-STA signal to go low when the laser has been switched on. This signal is fed to the drive processor module (R).

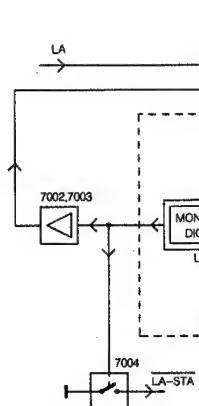
The signal LA switches, via T 7001, the controllable amplifier T 7005, thus the laser, on and off (LA low = off).

The LDU signal processing

The LDU signal processing converts the signals from the photodiodes into drive signals to be processed further in the electronics of the player.

- HF signal

The signals from photodiodes A, B, C and D contain the information of the pit pattern on the video disc, read out by the laser beam. The sum signal A + B + C + D is fed to the HF preamplifier via a highpass filter (>50kHz). This amplifier delivers the HF-OUT1 and HF-OUT2 signals, both FM modulated by the disc info.



- Radial signals

The radial fault signal on photodiodes R1 and R2 occurs when the laser spots are not exactly positioned on the tracks of the disc. In the servo preamplifier, the difference signal (R1-R2) represents the radial error signal RAD-ER. When the laser spot is exactly positioned on the track, a track position indication TPI is obtained from the servo preamp. The TPI signal is low when on track and high when the spot is off the track.

As soon as the TPI signal becomes high, the radial mirror in the LDU will be driven by the RAD-ER signal.

The ATC circuit

The block diagram of the ATC circuit is shown in Fig.Z2. The signals of D1 and D2 are measured in IC 7204. Addition of the two signals gives a sign that a disc is present above the LDU. In this case DR (disc reflection) is high. Subtraction of the signals represents the error-signal (D1-D2), that is fed to the tilt loop switch T 7015. Signal TLS, coming from the Drive Module, is high when the ATC circuit has to become active (DR = high).

The tilt error signal is fed to amplifier IC 7206 which drives the tilt motor. As soon as the tilt motor voltage is within a range of + and - 0.5V, the TILTOK signal will be low, as a sign that the ATC is in a correct position.

DECK ELECTRONICS
(LDU SIGN. PROC.)

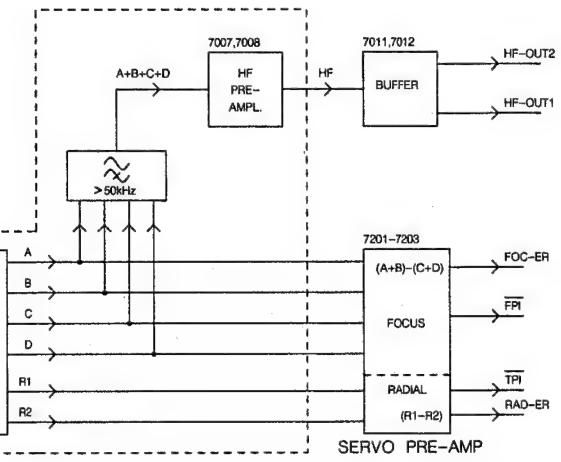


Fig.Z1

PRS.01683
T-08 709
VP415

- Focus signals

The signals A, B, C and D are processed in the servo preamplifier to gain the focus error signal FOC-ER and the focus position indication FPI. Both signals drive the focus circuit which focusses the objective onto the video disc.

The FOC-ER representing the deviation between objective and disc is composed by the difference signal (A+B) - (C+D).

The FPI signal is high when the objective is not focussed. As soon as focus is obtained, the FPI will go low and the objective is kept in focus by the FOC-ER signal.

DECK ELEKTRONICS
(ACTIVE TILT CONTROL)

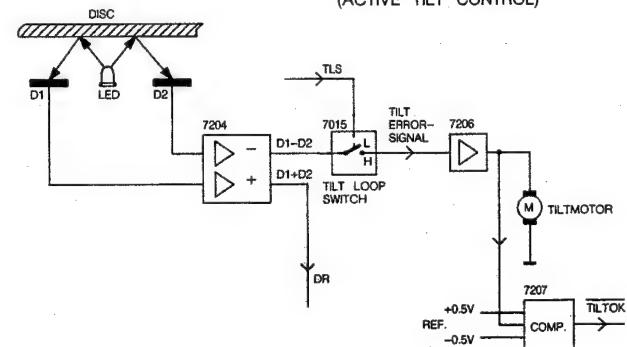


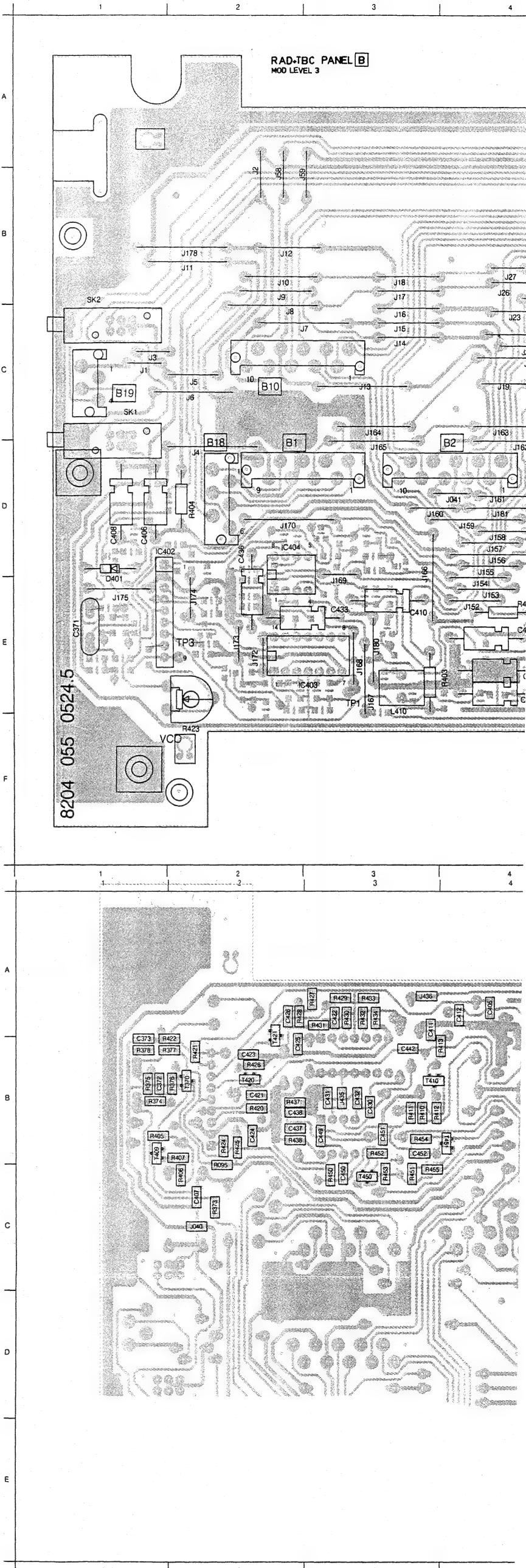
Fig.Z2

PRS.01728
T32-709
VP415

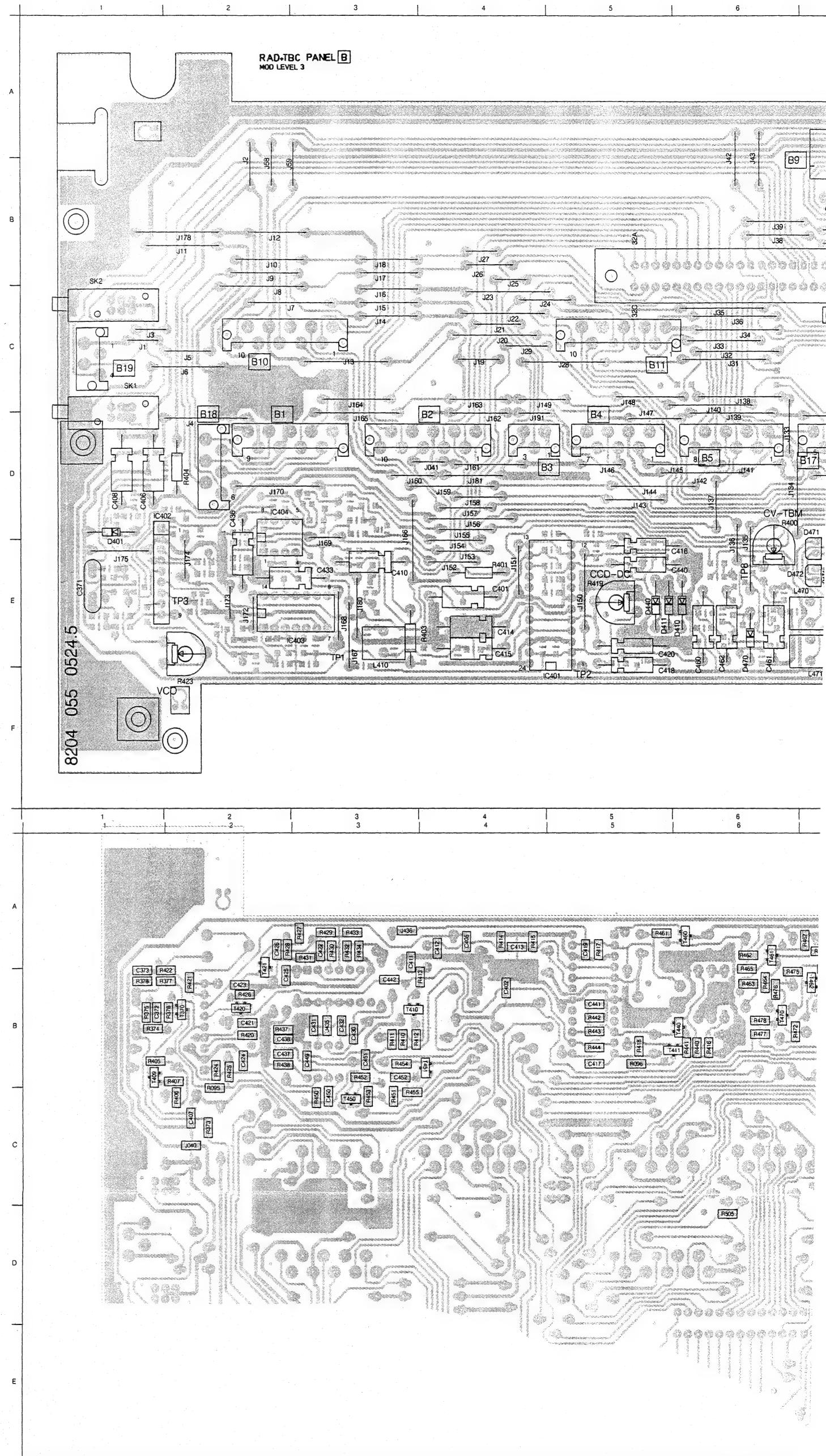
LIST OF LOOP-THROUGH SIGNALS ON PANEL B

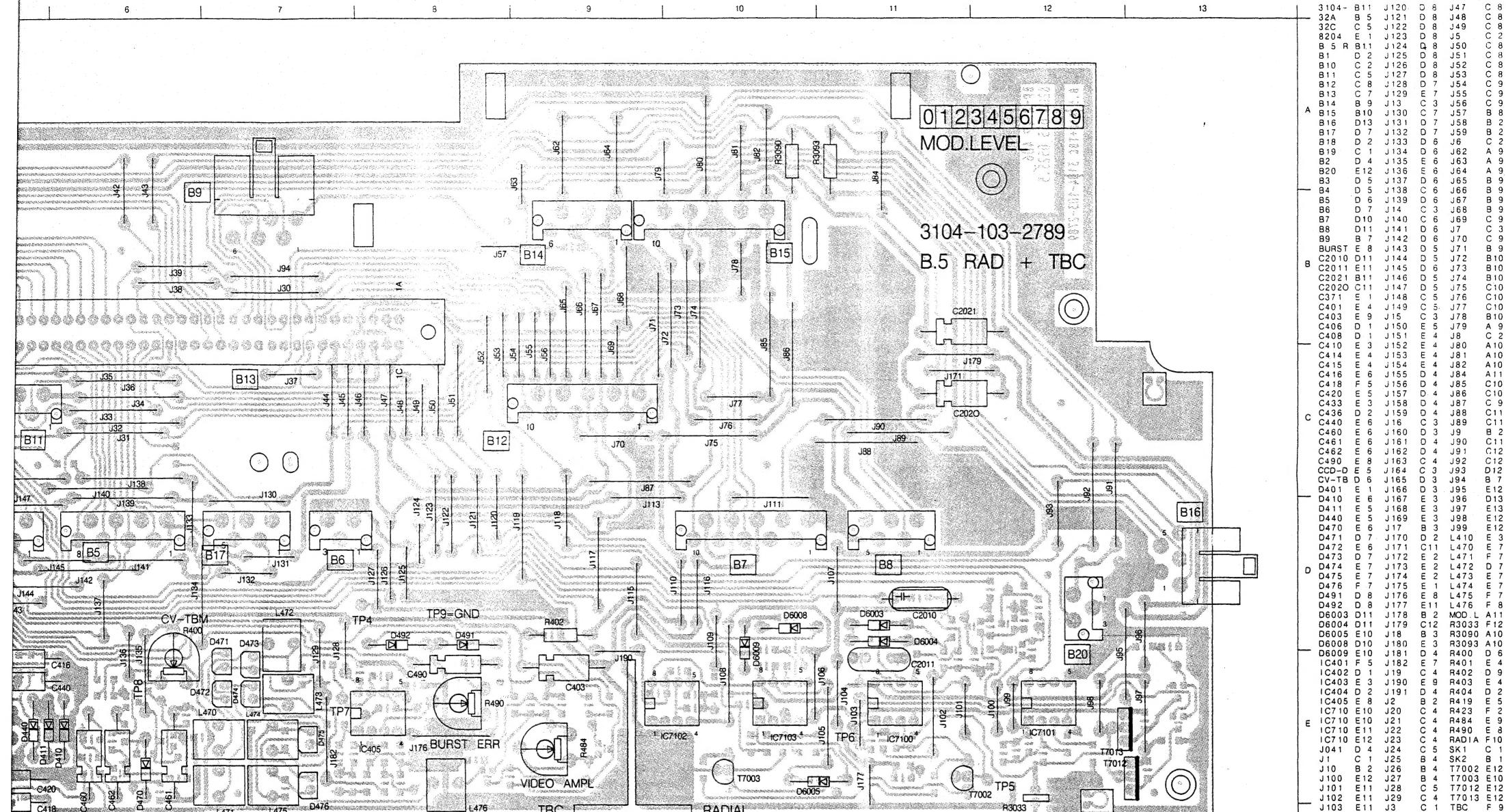
CONNECTORS:

FROM	TO	SIGNAL NAME	FROM	TO	SIGNAL NAME
1B1	4B18	FOC-ER	1B12	9B15	-12
2B1	3B18	FPI	2B12	8B15	-13
5B1	6B1	GND	3B12	4B15/5B15/6B15	GND
6B1	5B1/2B18	GND	4B12	3B14/4B14	+5
7B1	1B18	FOCACT+	5B12	1B14/2B14	+5SB
1B2	32aB13	LA-STA	6B12	3B15	+12
2B2	31aB13	LA	7B12	2B15	+13
3B2	10B15	-5SB	8B12	23aB13	MEM-SU
4B2	9B15	-12	9B12	21aB15	2-PPR
5B2	4B15/5B15/6B15	0	10B12	20aB15	PO-RES
6B2	3B14/4B14	+5			
7B2	3B15	+12	8aB13	2B8	AUD1ON
8B2	30aB13	DR	9aB13	1B8	AUD2ON
9B2	29aB13	TILTOK	10aB13	6B9	COMM-1
10B2	28aB13	TLS	11aB13	5B9	COMM-2
1B3	3B14/4B14	+5	12aB13	4B9	COMM-3
2B3	31cB13	SPI	13aB13	3B9	COMM-4
1B4	9B15	-12	14aB13	2B9	SL-PWR
2B4	10B15	-5SB	15aB13	4B16	EJECT-BUT
3B4	4B15/5B15/6B15	0	17aB13	3B19	RC5
4B4	3B14/4B14	+5	20aB13	10B12	PO-RES
5B4	1B14/2B14	+5SB	21aB13	9B12	2-PPR
6B4	3B15	+12	22aB13	3B11	TTM
7B4	1B15	+12SB	23aB13	8B12	MEM-SU
2B5	22cB13	V-SLAVE	24aB13	6B10	CL-VID
3B5	23cB13	H-SLAVE	25aB13	5B10	FRLOCK
4B5	24cB13/3B10	VMANCH	26aB13	2B10	CLV-TC
5B5	25cB13/4B10	HMANCH	27aB13	1B10	0-RPM
6B5	26cB13	CV/CS	28aB13	10B2	TLS
7B5	27cB13	VOBN	29aB13	9B2	TILTOK
8B5	28cB13	VOW	30aB13	8B2	DR
1B6	6B11	GND	31aB13	2B2	LA
3B6	8B11	CS-TBC	32aB13	1B2	LA-STA
4B6	9B11	RAMP-EN	1cB13	7B15	-12SB
5B6	4B7/9B10	DO-INH	2cB13	4B15/5B15/6B15	GND
6B6	20cB13	CS-SWITCH	3cB13	1B15	+12SB
7B6	21cB13	NS-VID	4cB13	1B14/2B14	+5SB
3B7	10B10	DEM-BK	5cB13	1B15	+12SB
4B7	5B6/9B10	DO-INH	6cB13	1B15	+12SB
5B7	1B11	CV-DOC-GND	7cB13	NC	RESO1
6B7	2B11	CV-DOC	8cB13	NC	RESO2
9B7	7B7	HF-ATBC-GND	9cB13	NC	RES11
1B8	9aB13	AUD2ON	10cB13	NC	RES12
2B8	8aB1	AUD1ON	11cB13	NC	RES13
3B8	9B15	-12	12cB13	NC	RES14
4B8	4B15/5B15/6B15	0	13cB13	NC	HW-TEST
5B8	3B15	+12	14cB13	5B14	STBY
2B9	14aB13	SL-PWR	15cB13	3B16	STBY-BUT
3B9	13aB13	COMM-4	19cB13	10B11	RLS
4B9	12aB13	COMM-3	20cB13	6B6	CS-SWITCH
5B9	11aB13	COMM-2	21cB13	7B6	NS-VID
6B9	10aB13	COMM-1	22cB13	2B5	V-SLAVE
1B10	27aB13	0-RPM	23cB13	3B5	H-SLAVE
2B10	26aB13	CLV-TC	24cB13	3B10/4B5	VMANCH
3B10	24aB13/4B5	VMANCH	25cB13	4B10/5B5	HMANCH
4B10	25aB13/5B5	HMANCH	26cB13	6B5	CV/CS
5B10	25aB13	FRLOCK	27cB13	7B5	VOBN
6B10	24aB13	CL-VID	28cB13	8B5	VOW
7B10	3B15	+12SB	29cB13	NC	OBS
8B10	9B15	-12SB	30cB13	5B18	FOC-IND
9B10	4B7/5B6	DO-INH	31cB13	2B3	SPI
10B10	3B7	DEM-BK	32cB13	6B18	FOC-EN
1B11	5B7	CV-DOC-GND	5B14	14cB13	STBY
2B11	6B7	CV-DOC	2B15	7B12	+13
3B11	22aB13	TTM	8B15	2B12	-13
6B11	1B6	GND	10B15	3B2	-5SB
8B11	3B6	CS-TBC	1B16	3B14/4B14	LED
9B11	4B6	RAMP-EN	3B16	15cB13	STBY-BUT
10B11	19cB13	TLS	4B16	15cB13	EJECT-BUT
			3B19	17aB13	RC5

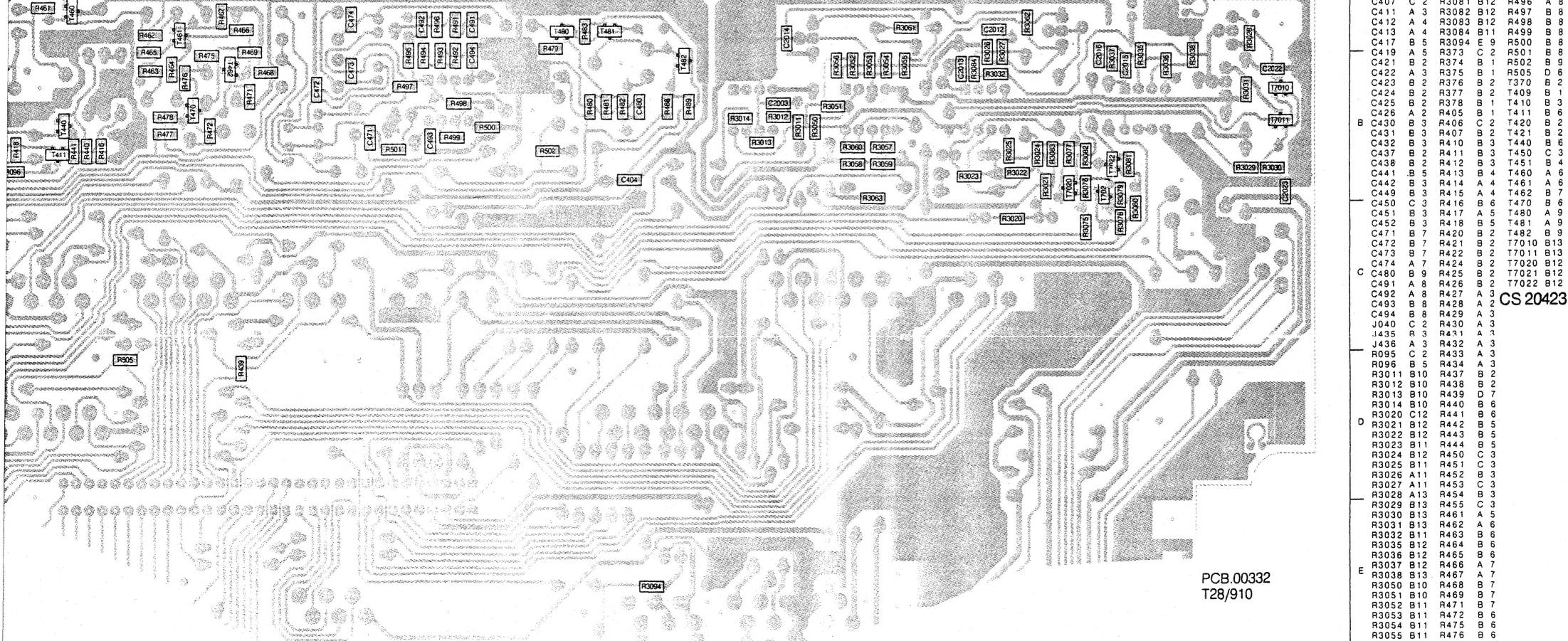


FROM	TO	SIGNAL NAME
1B12	9B15	-12
2B12	8B15	-13
3B12	4B15/5B15/6B15	GND
4B12	3B14/4B14	+5
5B12	1B14/2B14	+5SB
6B12	3B15	+12
7B12	2B15	+13
8B12	23aB13	MEM-SU
9B12	21aB15	2-PPR
10B12	20aB15	PO-RES
8aB13	2B8	AUD1ON
9aB13	1B8	AUD2ON
10aB13	6B9	COMM-1
11aB13	5B9	COMM-2
12aB13	4B9	COMM-3
13aB13	3B9	COMM-4
14aB13	2B9	SL-PWR
15aB13	4B16	EJECT-BUT
17aB13	3B19	RC5
20aB13	10B12	PO-RES
21aB13	9B12	2-PPR
22aB13	3B11	TTM
23aB13	8B12	MEM-SU
24aB13	6B10	CL-VID
25aB13	5B10	FRLOCK
26aB13	2B10	CLV-TC
27aB13	1B10	0-RPM
28aB13	10B2	TLS
29aB13	9B2	TIILTOK
30aB13	8B2	DR
31aB13	2B2	LA
32aB13	1B2	LA-STA
1cB13	7B15	-12SB
2cB13	4B15/5B15/6B15	GND
3cB13	1B15	+12SB
4cB13	1B14/2B14	+5SB
6cB13	1B15	+12SB
7cB13	NC	RESO1
8cB13	NC	RESO2
9cB13	NC	RESI1
10cB13	NC	RESI2
11cB13	NC	RESI3
12cB13	NC	RESI4
13cB13	NC	HW-TEST
14cB13	5B14	STBY
15cB13	3B16	STBY-BUT
19cB13	10B11	RLS
20cB13	6B6	CS-SWITCH
21cB13	7B6	NS-VID
22cB13	2B5	V-SLAVE
23cB13	3B5	H-SLAVE
24cB13	3B10/4B5	VMANCH
25cB13	4B10/5B5	HMANCH
26cB13	6B5	CV/CS
27cB13	7B5	VOBN
28cB13	8B5	VOW
29cB13	NC	OBS
30cB13	5B18	FOC-IND
31cB13	2B3	SPI
32cB13	6B18	FOC-EN
5B14	14cB13	STBY
2B15	7B12	+13
8B15	2B12	-13
10B15	3B2	-5SB
1B16	3B14/4B14	LED
3B16	15cB13	STBY-BUT
4B16	15cB13	EJECT-BUT
1B18	7B1	FOCACT+
2B18	6B1	FOCACT-
3B18	2B1	FPI
4B18	1B1	FOC-ER
5B18	30cB13	FOC-IND
6B18	32cB13	FOC-EN
3B19	17aB13	RC5



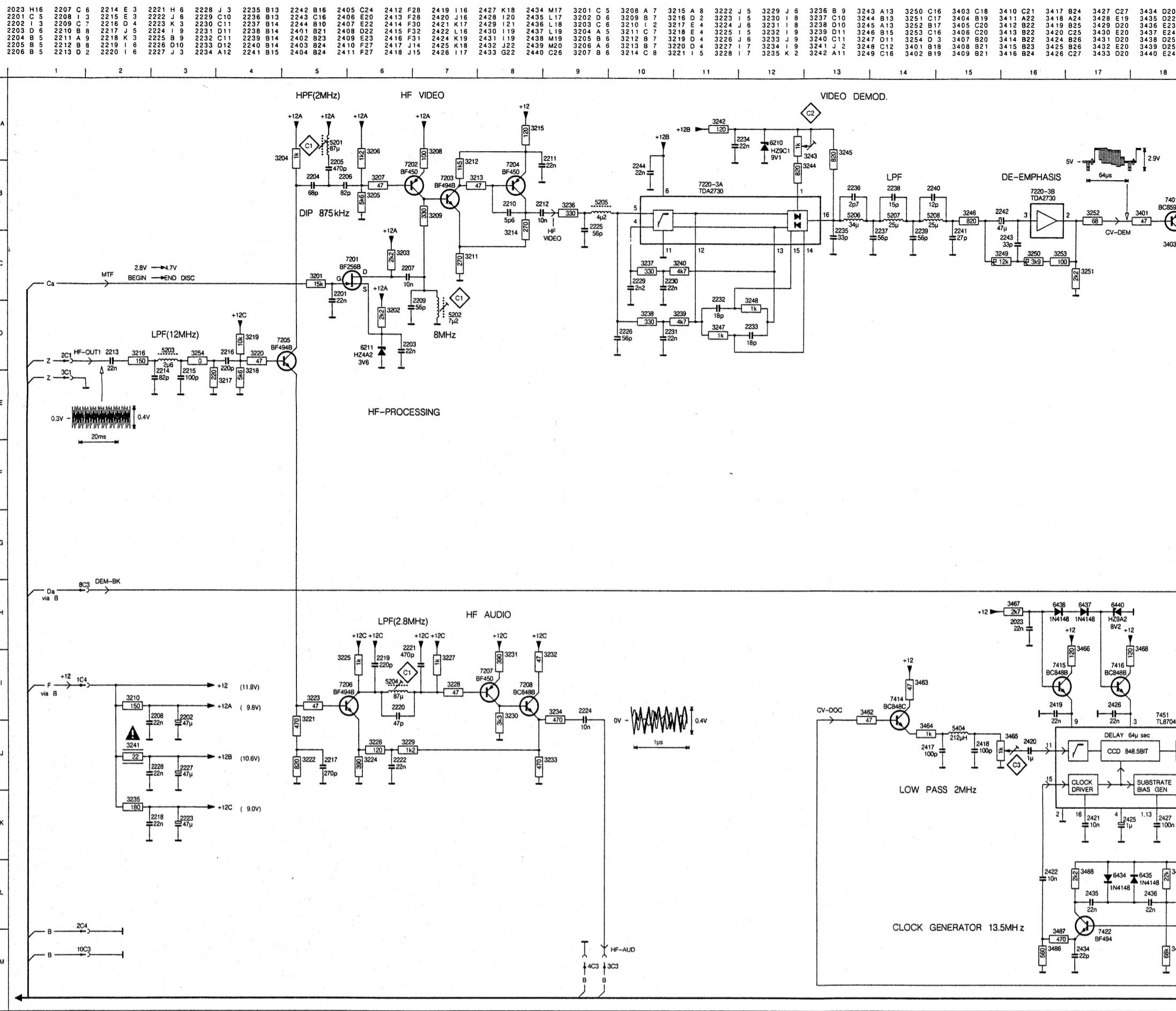


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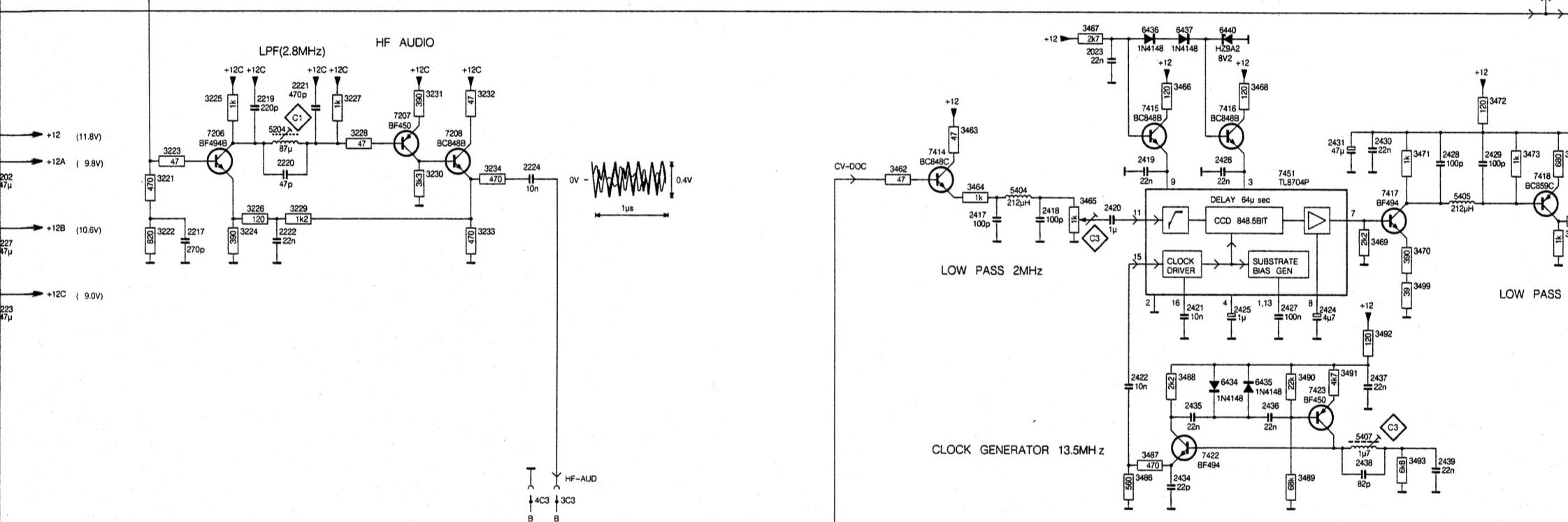
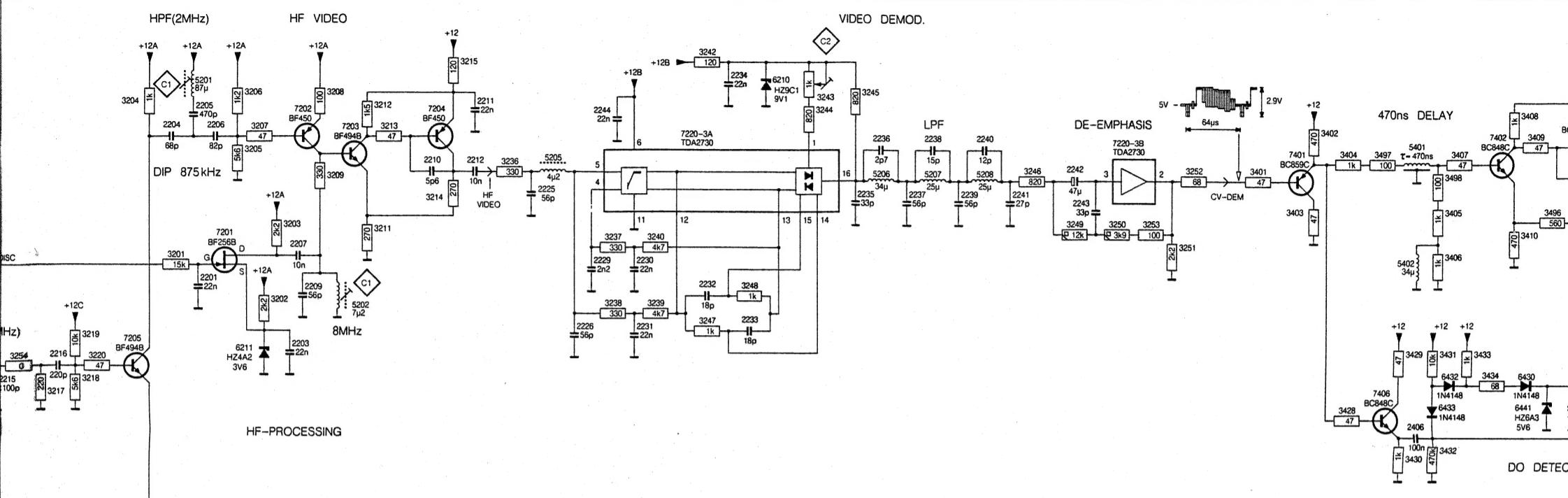
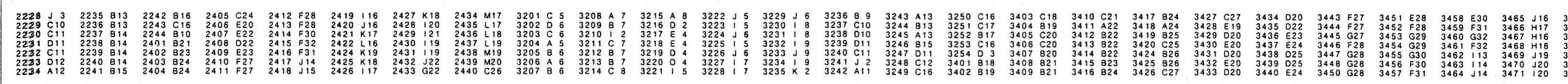


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CS 20 424



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