C5 Process

ON Semiconductor (formerly AMIS) 0.50 Micron

Related Resources

MOSIS-Supported ON Semiconductor Processes

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Process Family Description

This non-silicided CMOS process has 3 metal layers and 2 poly layers, and a high resistance layer. Stacked contacts are supported. The process is for 5 volt applications. MOSIS orders EPI wafers for this process. Non-EPI (bulk) is an additional cost option and not available for MEP submissions. For further information, see the **ON Semiconductor Foundry Mixed-Signal Offerings** web page.

C5N Process

PiP (poly2 over poly) capacitors (950 aF/μm^2) and the HRP (High Resistance) option are available on multiproject runs.

C5F Process

The C5F process offers the above layers of C5N plus Thick_Gate, N_Minus_Implant (Npblk), and P_Minus_Implant (Ppblk).

Design Rules

This process supports the following design rules.

Design Rules	Lambda[1]	Feature Size[1]	Availablility
ON Semi C5F/N Rules	n/a	0.60	**MOSIS, ON Semiconductor**
SCMOS_SUBM	0.30	0.60	MOSIS in **PDF**
SCMOS	0.35	0.60 (after sizing)	MOSIS in **PDF**

[1]Values in micrometers (μm)

Review the **CMP and antenna guidelines** which apply to both sets of design rules.
MOSIS Technology Codes See **Technology Codes for ON Semiconductor C5F/N Process**.

Important note about pads. The bonding pads on designs submitted to these runs should have metal2 (and via2) under the metal3. If these guidelines are not followed, metal lifting problems can occur.

ON Semiconductor Design Rules, Process Specifications, and SPICE Parameters
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Reticle/Wafer Size, Steps, Turnaround Time, Wafer and Die Thickness.

ON Semiconductor C5 Process

Wafer Size (inches)	Reticle Size (mili- meters, approx.)	Reticle Copies Stepped on Wafer (approx.)	Turn- around Time (weeks, approx.)[(1)]	Die Thickness (+/- .5 mil)		Wafer Thickness	
				Mils	Micro- meters	Mils	Micro- meters
8	21 x 21	55	26 weeks	10	250	30	760

[1]ON Semi is experiencing a line load issue for the foreseeable future that pushes out delivery up to 26 weeks.