



## SCN3ME and SCN3ME\_SUBM

### MOSIS SCMOS Technology Codes and Layer Maps

This is the layer map for the technology codes SCN3ME and SCN3ME\_SUBM using the MOSIS Scalable CMOS layout rules (**SCMOS**) and only for SCN3ME and SCN3ME\_SUBM. For designs that are laid out using other design rules (or **technology codes**), use the standard layer mapping conventions of that design rule set. For submissions in GDS format, the datatype is "0" (zero) unless specified in the map below.

SCN3ME: Scalable CMOS N-well, 3 metal, non-silicided, high resistance layer available. Adds a second polysilicon layer (poly2) as the upper electrode of a poly capacitor.

SCN3ME\_SUBM: Uses revised layout rules for better fit to sub-micron processes (see [MOSIS Scalable CMOS \(SCMOS\) Design Rules](#), Section 2.4).

Fabricated on **AMI 0.50 micron process** runs.

Layer	GDS	CIF	CIF Synonym	Rule Section	Notes
N_WELL	42	CWN		1	
ACTIVE	43	CAA		2	
POLY	46	CPG		3	
N_PLUS_SELECT	45	CSN		4	
P_PLUS_SELECT	44	CSP		4	
POLY2	56	CP2	CEL	11, 12, 13	Optional
HI_RES_IMPLANT	34	CHR		27	Optional
CONTACT	25	CCC	CCG	5, 6, 13	
POLY_CONTACT	47	CCP		5	Can be replaced by CONTACT
ACTIVE_CONTACT	48	CCA		6	Can be replaced by CONTACT
POLY2_CONTACT	55	CCE		13	Can be replaced by CONTACT.
METAL1	49	CM1	CMF	7	
VIA	50	CV1	CVA	8	
METAL2	51	CM2	CMS	9	
VIA2	61	CV2	CVS	14	
METAL3	62	CM3	CMT	15	
GLASS	52	COG		10	
PADS	26	XP			Non-fab layer used to highlight pads
Comments	--	CX			Comments



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