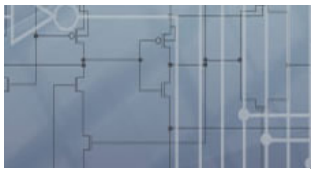
C5

ON Semiconductor Layer Map



Related Resources

Fabrication Schedule

Customer Support

MOSIS Products

This is the layer map for the ON Semi C5F/N 0.50 micron 3 metal, 2 poly (non-silicided) layout rules (AMI_C5F/N), and only for those ON Semi vendor design rules. For designs that are laid out using other design rules (or technology-codes), use the standard layer mapping conventions of that design rule set. For submissions in GDS format, the datatype is "0" (zero) unless specified in the map below.

Layer	GDS	CIF	Notes
N_WELL	1	A01	
ACTIVE	2	A02	
N_CHANNEL_FLD	3	A03	Derived from N_WELL when N_CHANNEL_FLD is completely absent from layout. See Note #1
POLY	4	A04	
N_PLUS_BLOCK	5	A05	A copy of the drawn P_PLUS_SELECT is used when N_PLUS_BLOCK is completely absent from layout. See Note #1 ON Semi calls this layer N_PLUS_SELECT and further requires that it be a copy of P_PLUS_SELECT. It is functionally an N_PLUS_BLOCK layer; the drawn regions will not receive the n+ implant.
P_PLUS_SELECT	6	A06	
CONTACT	8	A08	
METAL1	9	A09	
VIA1	10	A10	
METAL2	11	A11	
VIA2	12	A12	
METAL3	13	A13	
CAP_POLY (POLY2)	26	A26	Optional
HRP (HIGH RESISTANCE)	27	A27	
THICK_GATE	28	A28	C5F layer
N_MINUS_IMPLANT (Npblk)	36	A36	C5F layer
P_MINUS_IMPLANT (Ppblk)	37	A37	C5F layer
GLASS	14	A14	

Note #1:

If this layer is present anywhere in the submitted design or anywhere in the design after instantiation, then MOSIS will not derive it. If this layer is not in the submitted design or anywhere in the design after instantiation, then MOSIS will derive that layer from the listed layers. MOSIS does not create a layer partially from a layer drawn by the customer and partially derived from other layers.