Lab_HW_#5

M1522.000700 Logic Design (2019 Fall)

2013-12815 이 동 주

1. Klingon number system

(1) 코드의 구현은 다음과 같다. 좌측은 rtl, 우측은 gate level 로 구현하였다.

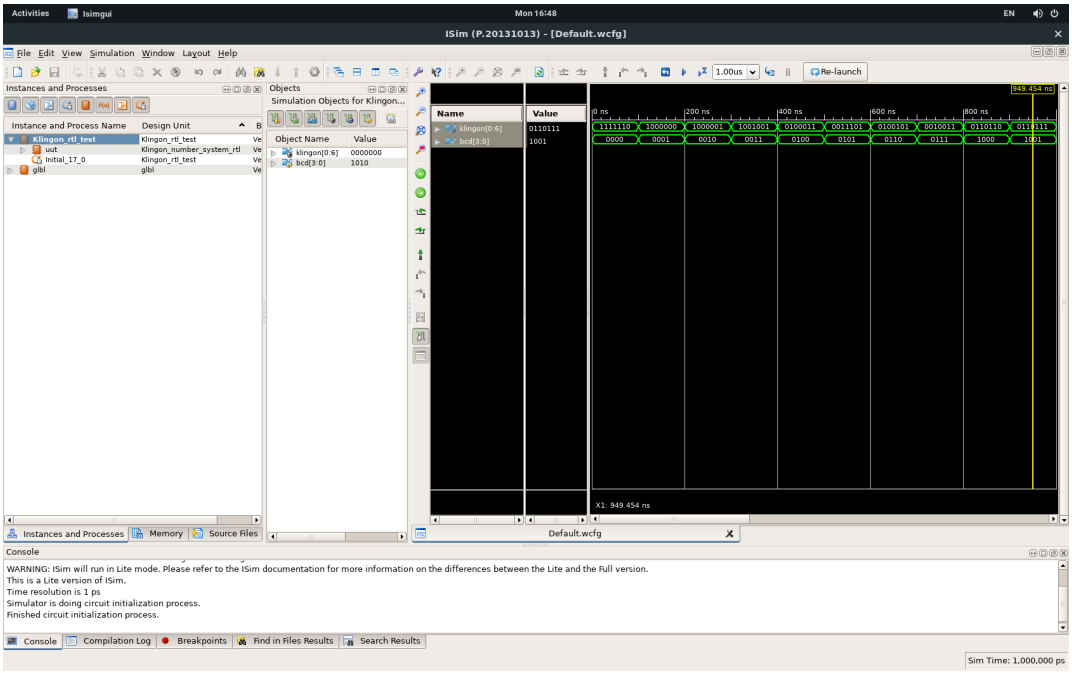
Klingon_number_system_rtl.v

```
`timescale 1ns / 1ps

module Klingon_number_system_rtl(
    input [3:0] bcd,
    output [6:6] klingon
    );


        assign klingon =       (bcd == 4'b0000)?       7'b1111110 :

(bcd == 4'b0001)?       7'b1000000 :

(bcd == 4'b0010)?       7'b1000001 :

(bcd == 4'b0011)?       7'b1001001 :

(bcd == 4'b0100)?       7'b0100011 :

(bcd == 4'b0101)?       7'b0011101 :

(bcd == 4'b0110)?       7'b0100101 :

(bcd == 4'b0111)?       7'b0010011 :

(bcd == 4'b1000)?       7'b0110110 :

(bcd == 4'b1001)?       7'b0110111 :

7'b0000000;


endmodule
```

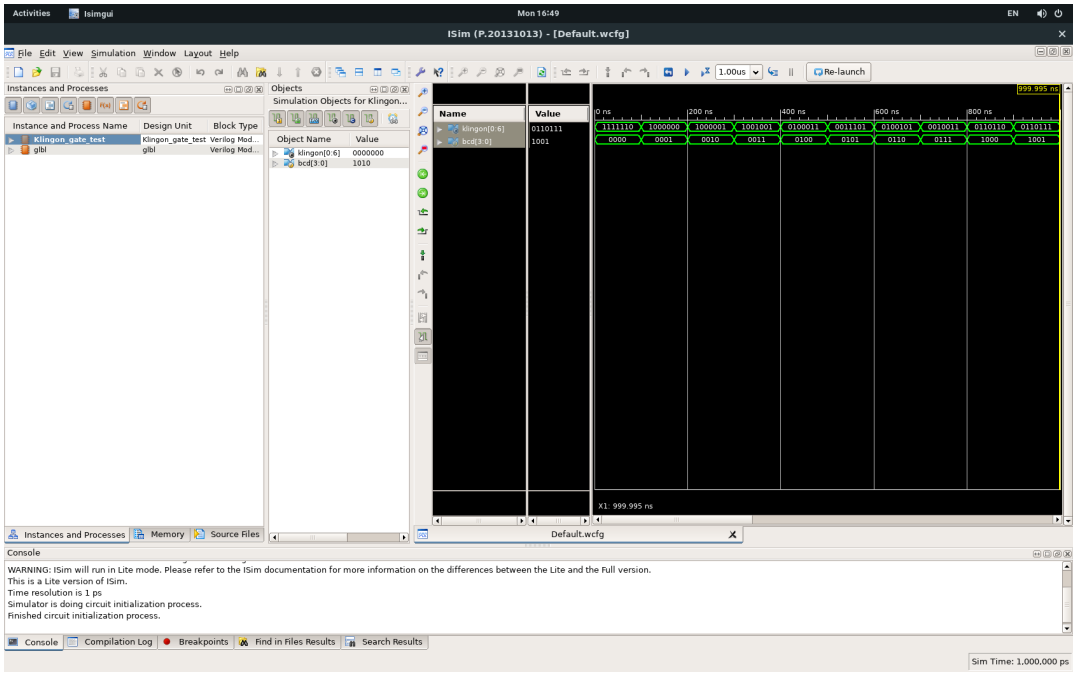
Klingon_number_system_gate.v

```
module Klingon_number_system_gate(
        input [3:0] bcd,
  output [6:6] klingon
  );

        wire [3:0] n_bcd;
        wire nanb;
        wire anb;
        wire a;
        wire nanbncnd;
        wire ad;
        wire bnd;
        wire bd;
        wire nbncnd;
        wire bncd;
        wire nbcd;
        wire bcnd;
        wire wbcd;
        wire b;
        wire ncnd;
        wire c;

        not U1(n_bcd[3], bcd[3]); // n_a
        not U2(n_bcd[2], bcd[2]);
        not U3(n_bcd[1], bcd[1]);
        not U4(n_bcd[0], bcd[0]); // _d

        and U5(nanb, n_bcd[3], n_bcd[2]);
        and U6(bnd, bcd[2], n_bcd[0]);
        and U7(ncnd, n_bcd[1], n_bcd[0]);
        and U8(anb, bcd[3], n_bcd[2]);//
        and U9(a, bcd[3]);//
        and U10(bd, bcd[2], bcd[0]); //
        and U11(nbncnd, n_bcd[2], n_bcd[1], n_bcd[0]);//
        and U12(nanbncnd, n_bcd[3], n_bcd[2], n_bcd[1], n_bcd[0]);//
        and U13(bncd, bcd[2], n_bcd[1], bcd[0]);
        and U14(nbcd, n_bcd[2], bcd[1], bcd[0]);
        and U15(bcnd, bcd[2], bcd[1], n_bcd[0]);
        and U16(wbcd, bcd[2], bcd[1], bcd[0]);
        and U17(b, bcd[2]);
        and U18(c, bcd[1]);
        and U19(ad, bcd[3], bcd[0]);

        or U20(klingon[0], nanb);
        or U21(klingon[1], bnd, ncnd, anb);
        or U22(klingon[2], a, bd, nbncnd);
        or U23(klingon[3], nanbncnd, bncd, nbcd);
        or U24(klingon[4], nanbncnd, a, bncd, bcnd);
        or U25(klingon[5], a, ncnd, wbcd);
        or U26(klingon[6], b, c, ad);
endmodule
```

(2) rtl 구현의 테스트 결과이다.

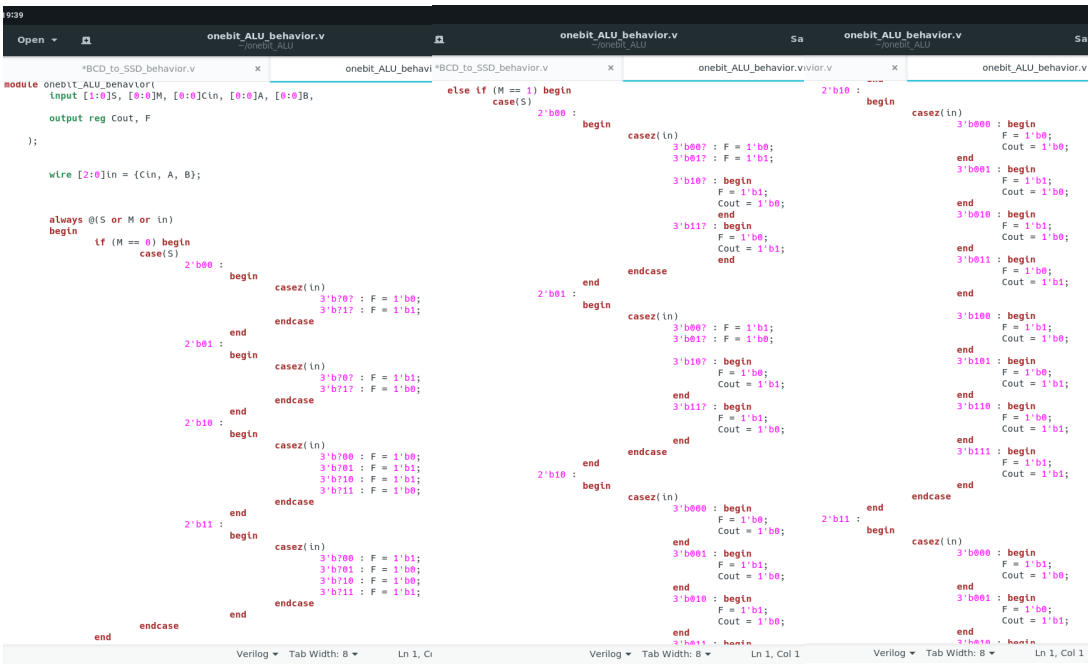


(3) gate level 구현의 테스트 결과이다.

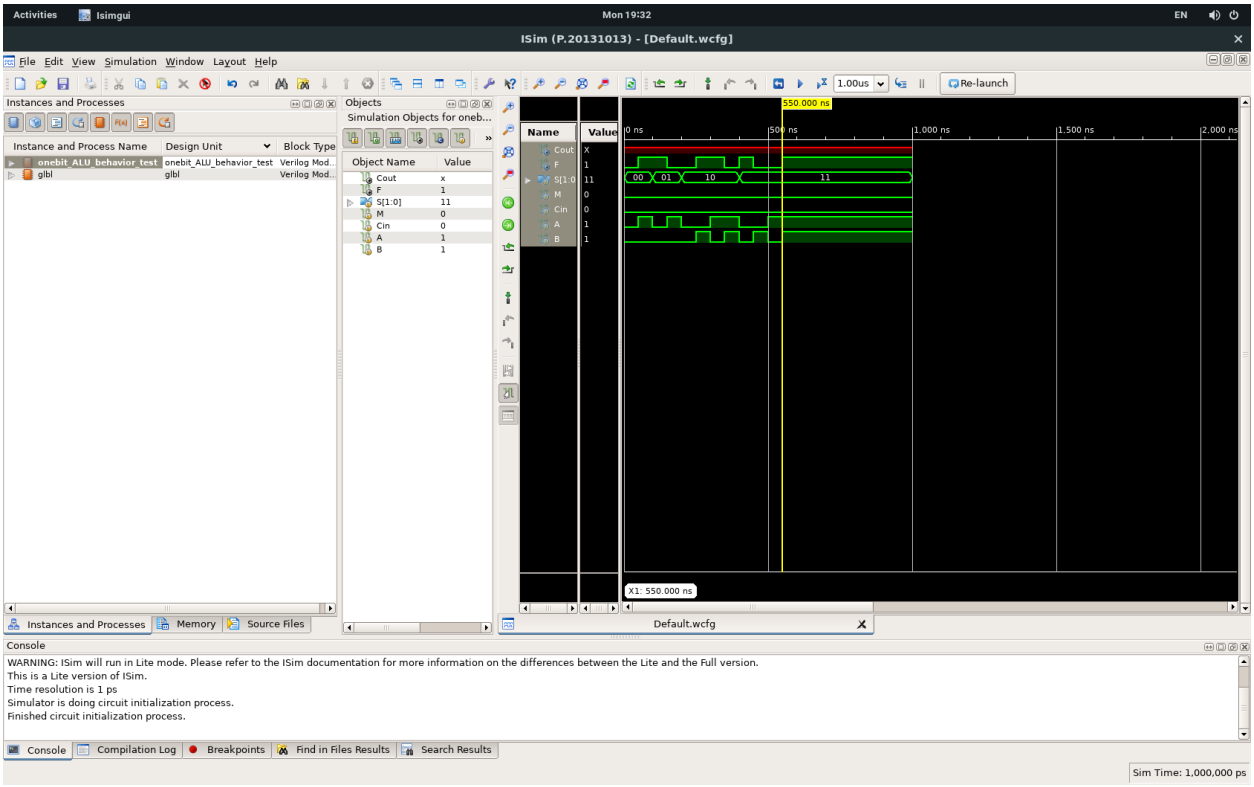


2. 1-bit ALU

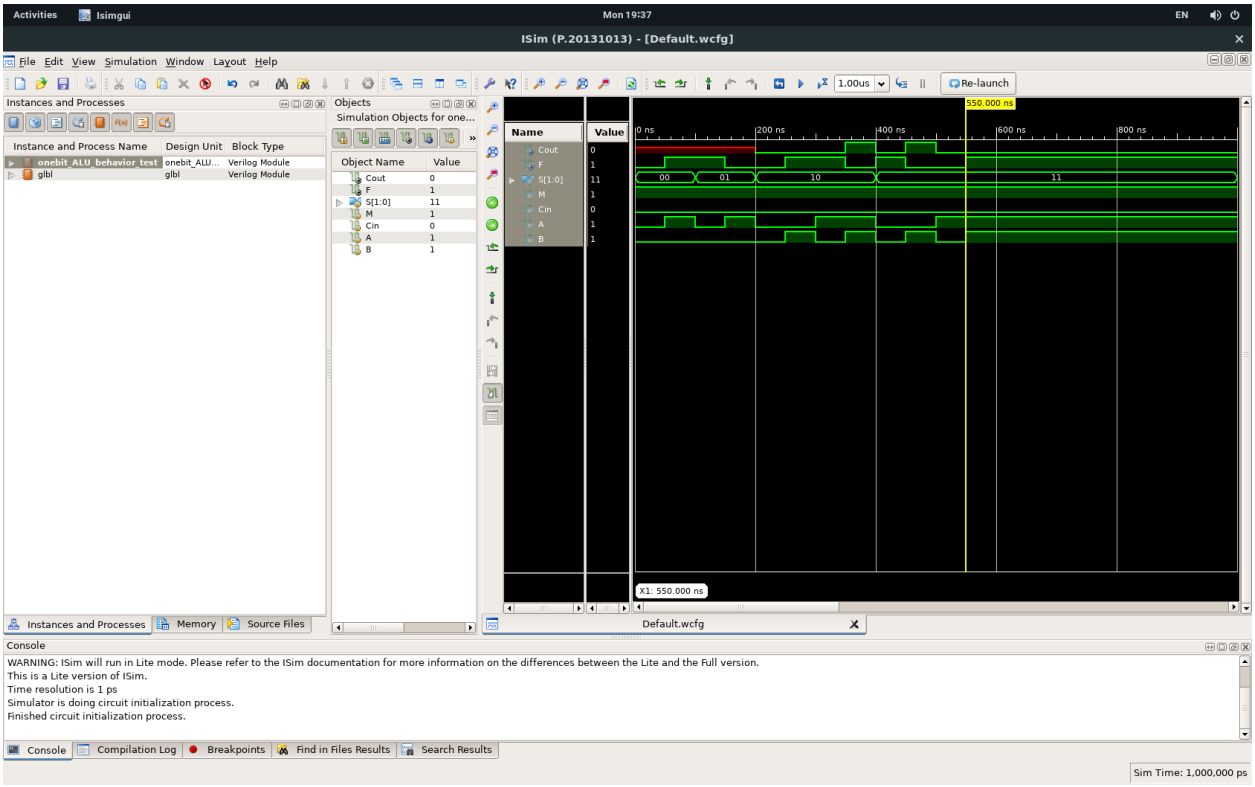
(1) behavior 구현을 통해 코드를 작성했으며, 다음과 같다.



(2) m = 0 에서 테스트 결과는 다음과 같다.



(3) m = 1, cin = 0 에서 테스트 결과는 다음과 같다.



(2) m = 0, cin = 1 에서 테스트 결과는 다음과 같다.