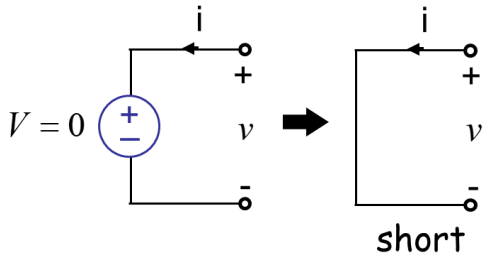
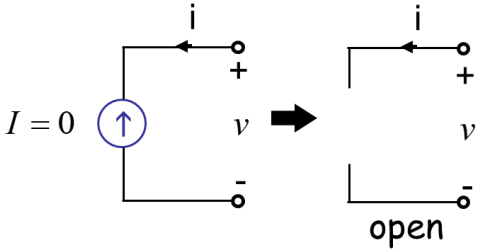
Electrical and Electronics Circuits (4190.206A 002)

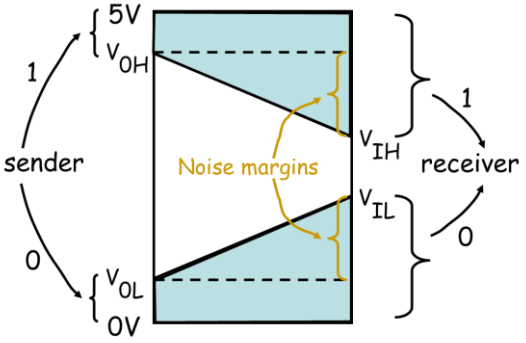
- HW #1 is due on Oct. 7, 2019 3:15pm
- Make-up class
  - 9/30 (Mon) 7pm-8:15pm (the class attendance won't be checked, and video recording of the class will become available at ETL)
  - There will be still a regular class between 2:00pm~3:15pm on 9/30 (Mon)
- 1st mid-term exam: 10/21(Mon) or 10/23(Wed)
- 2nd mid-term exam: 11/13(Wed) or 11/18(Mon)
- Final exam: 12/11 (Wed) 2:00pm~3:15pm
- There will be a class on 10/9 (Wed) Hangul Day, but the class attendance won't be checked, and video recording of the class will become available at ETL.
- Grades: 3 exams 30, 30, 30% homework + attendance: 10% (If you cannot attend the class for official reason, please let me or TA know in advance.)
- Self-attendance check

Review

- Circuit analysis method
  - Method 1: Basic KVL, KCL method
  - Method 2: combination of series and parallel resistors
  - Method 3: Node analysis method
  - Method 4: Superposition method and linearity
  - Method 5: Thevenin equivalent circuits
    - Thevenin equivalent source: voltage when the output terminals are open
    - Thevenin equivalent resistor: set all the source to zero and calculate the resistance
  - Method 6: Norton equivalent circuits
    - Norton equivalent source: current when the output terminals are shorted
    - Norton equivalent resistor = Thevenin equivalent resistor
- Digital abstraction
  - Why go from analog to digital?
  - Definition of forbidden region, $V_{OH}, V_{OL}, V_{IH}, V_{IL}$

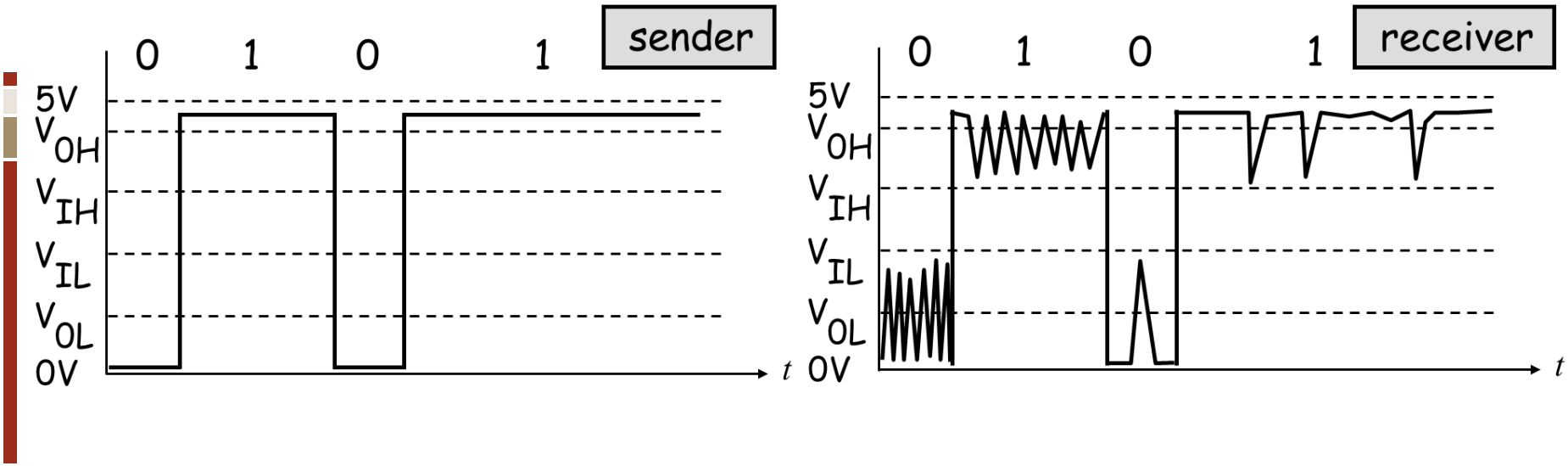






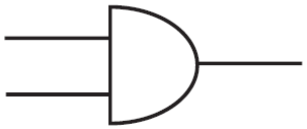
Static Discipline

- The static discipline requires devices to interpret correctly voltages that fall within the input thresholds. As long as valid inputs are provided to the devices, the discipline also requires the devices to produce valid output voltages that satisfy the output threshold.

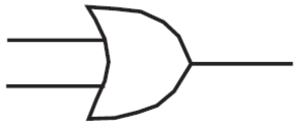


Binary Logic

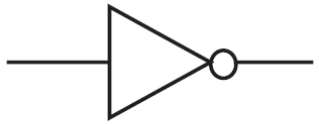
- Binary number representation
- Basic gates
  - AND: ·
  - OR: +
  - NOT: ~ or bar over signal



AND

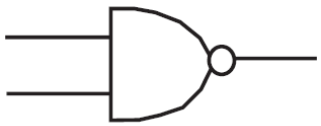


OR

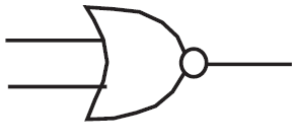


NOT

- How to build any arbitrary logic by combining only those 3 gates? ➔ sum-of-product
- De Morgan's law
  - $\sim(A \cdot B)=(\sim A) + (\sim B)$
  - $\sim(A + B)=(\sim A) \cdot (\sim B)$
- Can we even reduce the number of basic gates? ➔ Universal gates



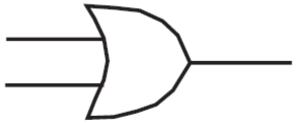
NAND



NOR

Boolean Logic

- Logic gates



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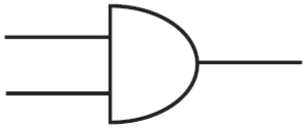
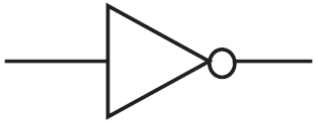
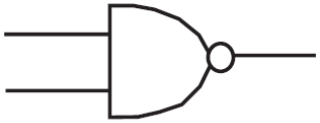


AND



NOT



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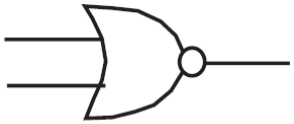
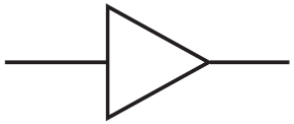


NOR

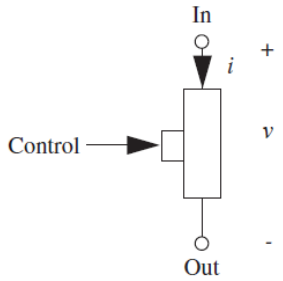


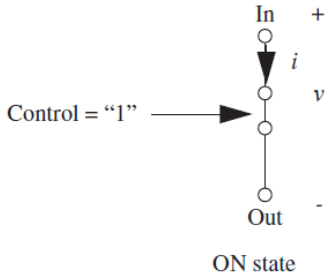
BUFFER

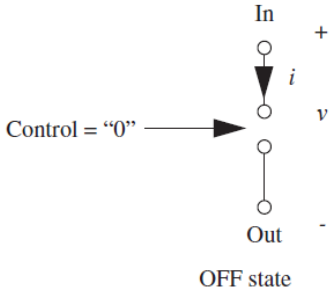
How to Implement Digital Gates?

- Switch

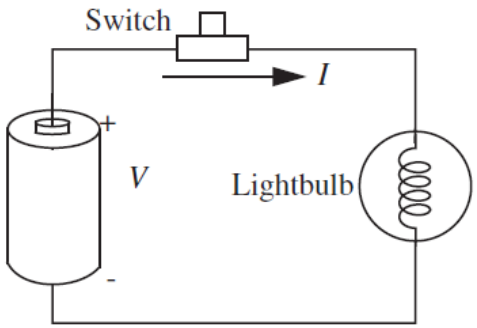
- Assume we have an ideal digital switch







- Can the following circuit implement NOT-like gate?



- Problem: output is not voltage

➔ Connect output directly to the switch

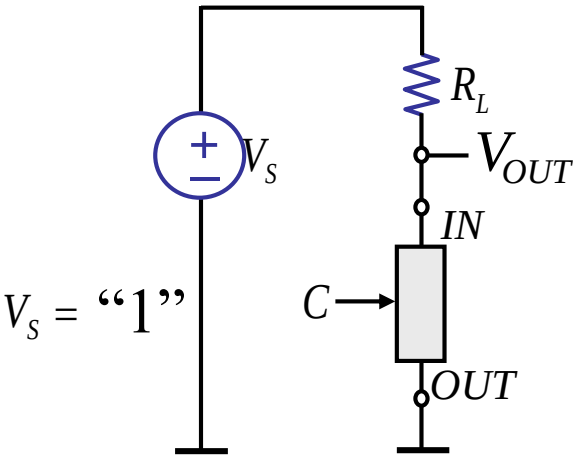
- Problem: "0" is not defined

➔ Connect to ground

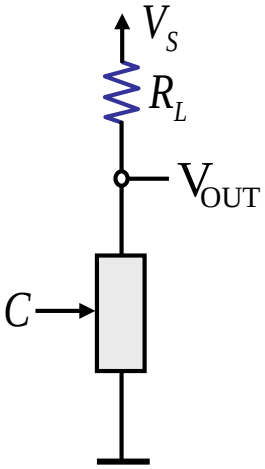
- Problem: circuit is shorted

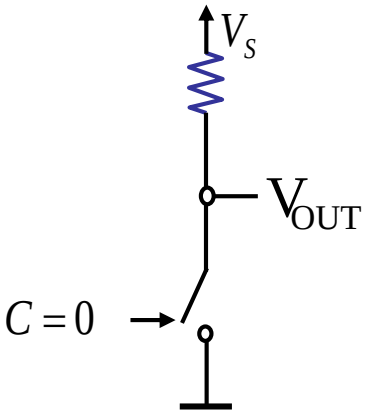
How to Implement correct NOT gate?

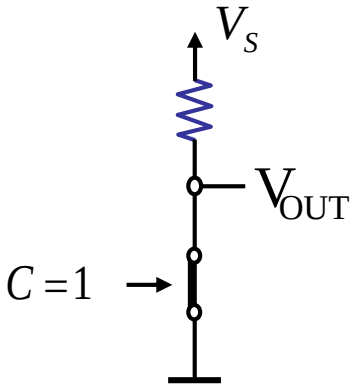
- Utilize the voltage drop!



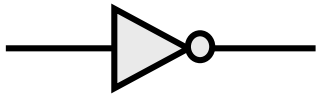
Common symbol for power supply





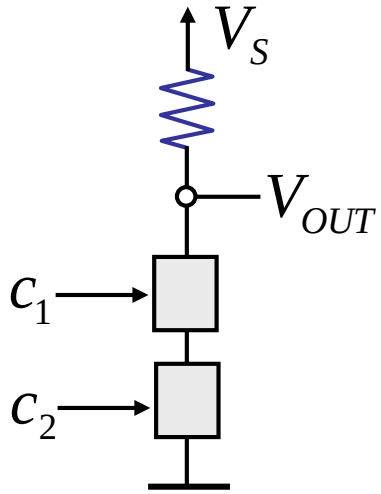


Truth table for

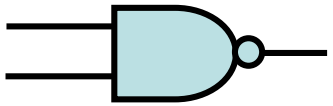


C	V_{OUT}
0	1
1	0

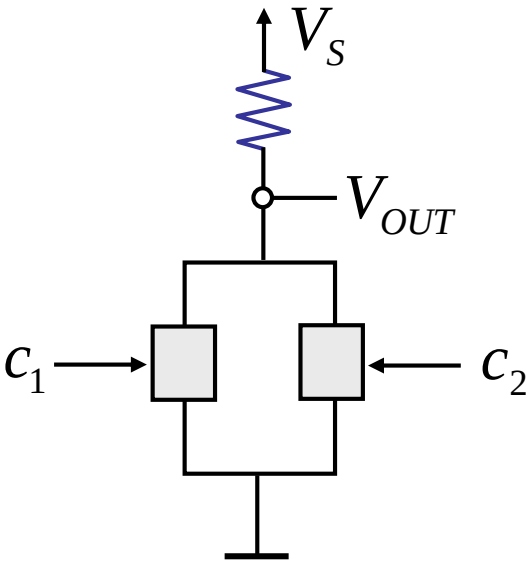
What about AND/OR gate?



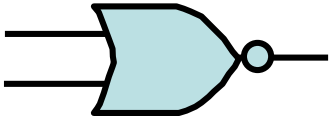
Truth table for



c_1	c_2	V_O
0	0	1
0	1	1
1	0	1
1	1	0

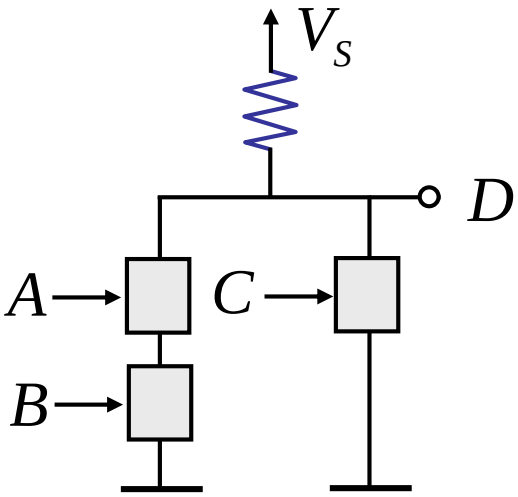


Truth table for



c_1	c_2	V_O
0	0	1
0	1	0
1	0	0
1	1	0

What is the following digital circuit?



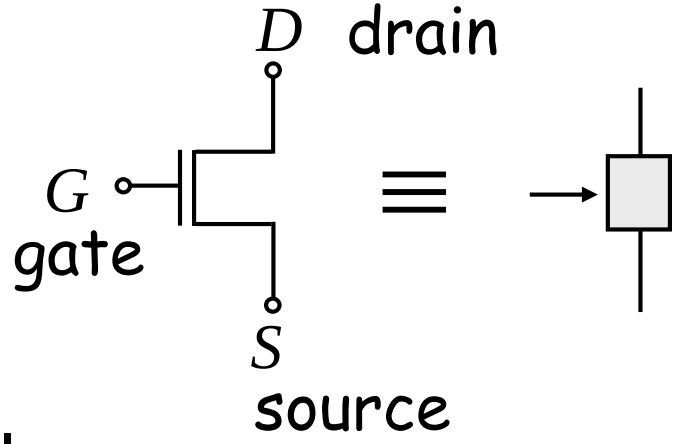
$$D = \overline{(A \cdot B) + C}$$

How to make digital switch?

- MOSFET device

➔ Metal-Oxide Semiconductor Field-Effect Transistor

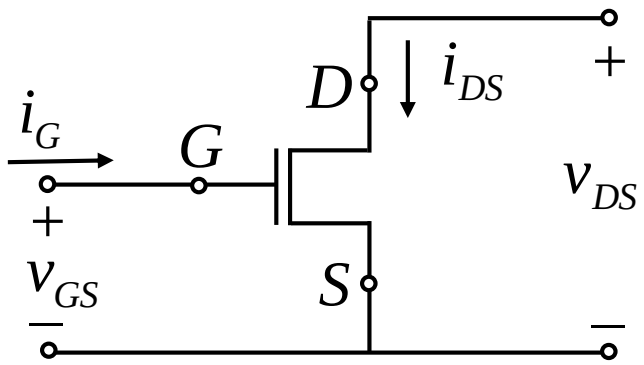
- 3-terminal lumped element behaves like a switch



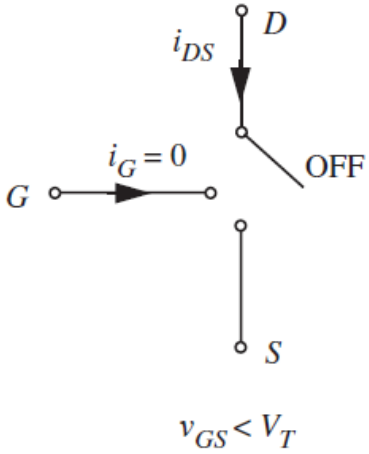
- G: control terminal
- D, S: behave in a symmetric manner when considered as a switch

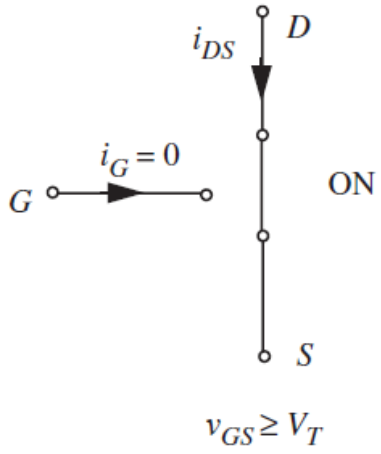
Ideal Behavior of MOSFET Device

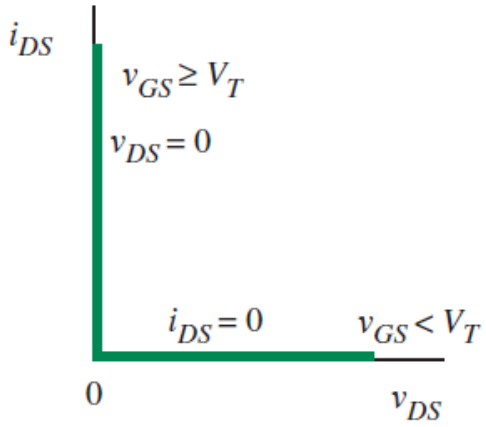
- "Switch" model (S model) of the MOSFET



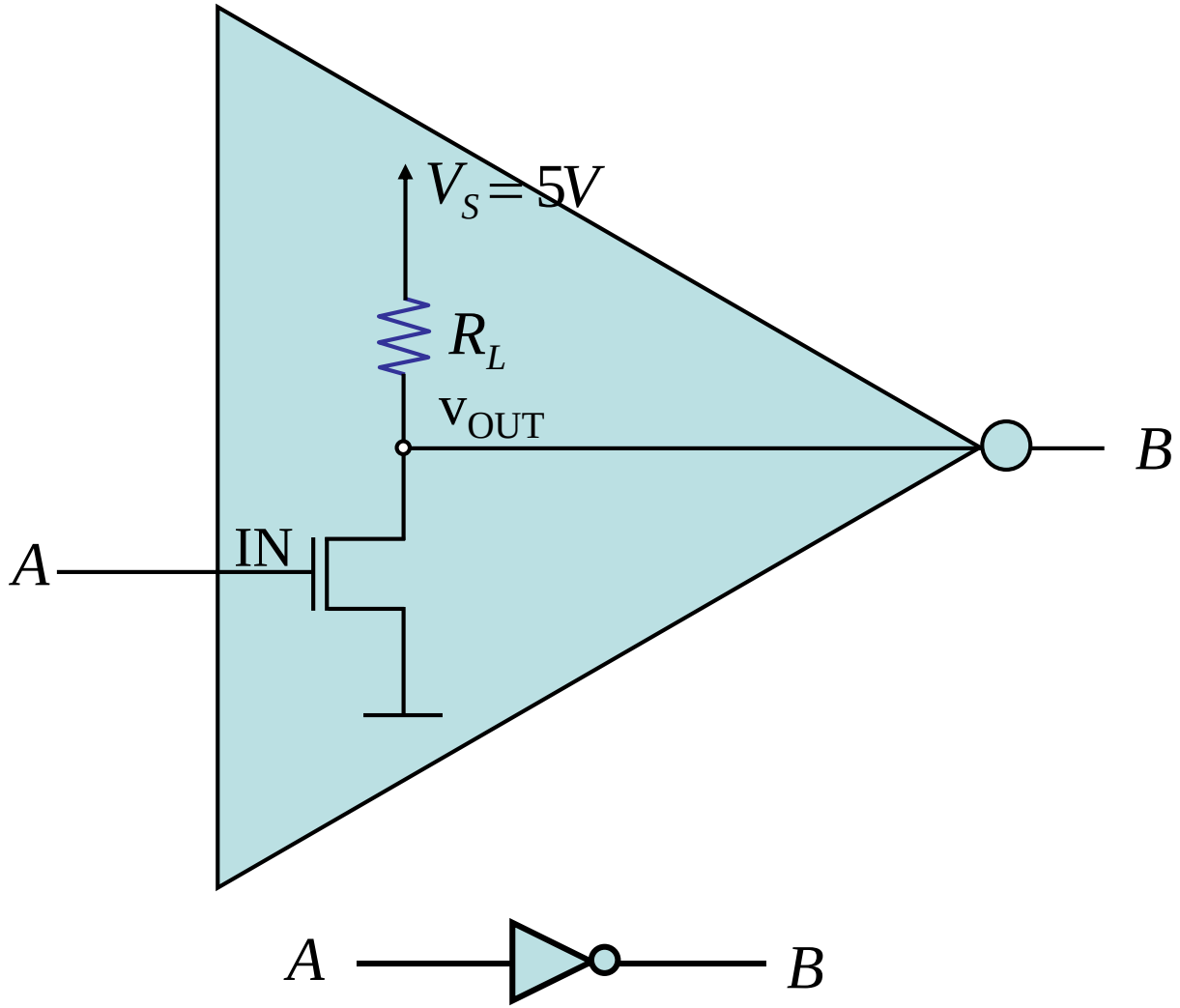
- Typical V_T: $0.7V \sim 1V$





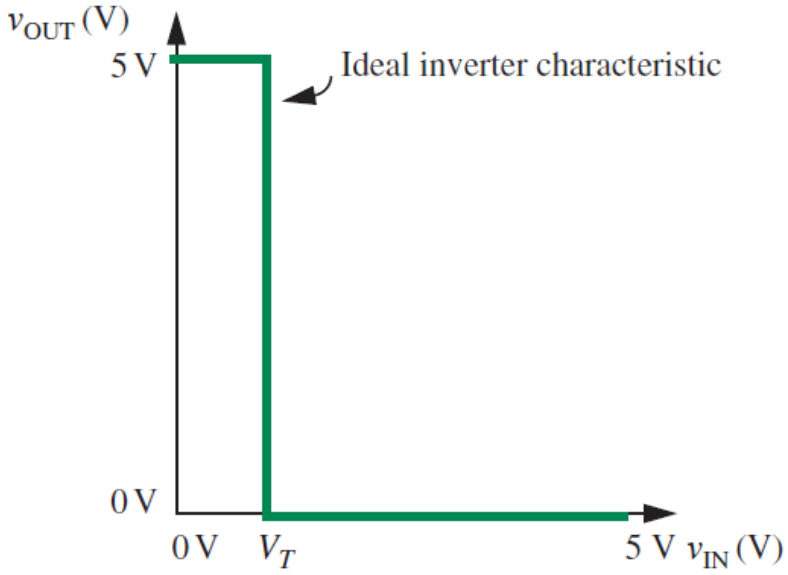


Inverter Circuit using MOSFET Switch

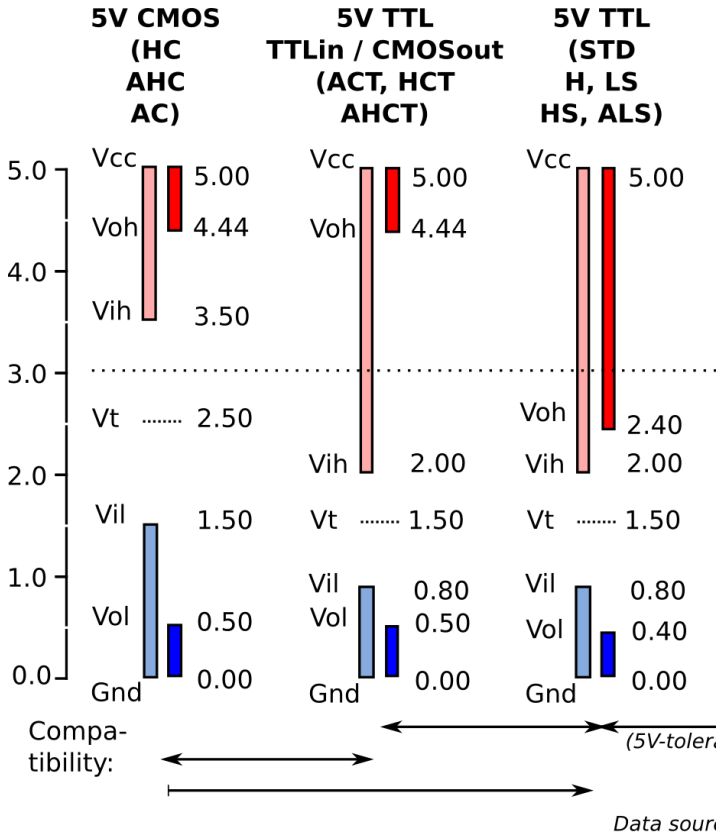


Example of datasheet: http://www.ti.com/lit/ds/symlink/cd4069ub.pdf

Can an Inverter Satisfy 5V TTL Standard?



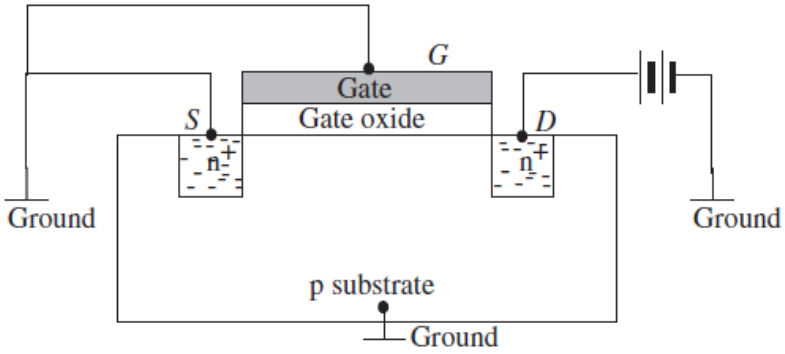
- What if $V_T \sim 0.7V$?
- What if $V_T \sim 1.0V$?

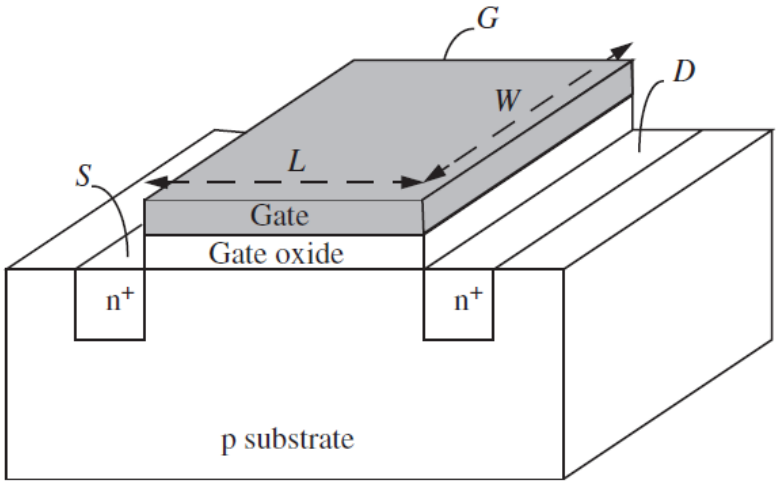


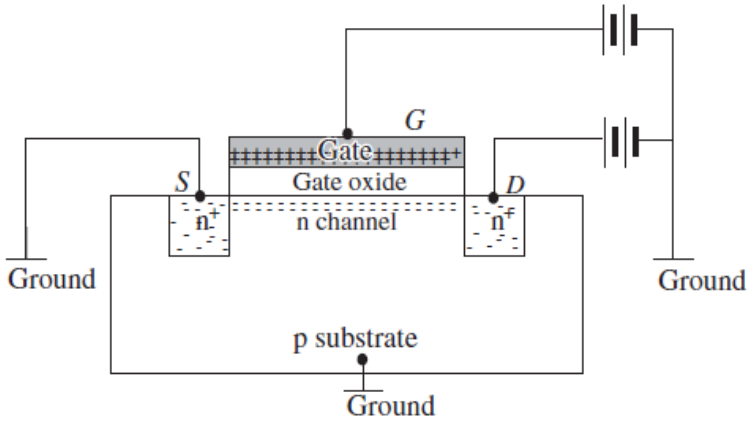
MOSFET Device Structure

- Metal-Oxide Semiconductor Field-Effect Transistor
- PN junction
- Resistance between S and D:

$$R_{ON} = R_n \frac{L}{W}$$

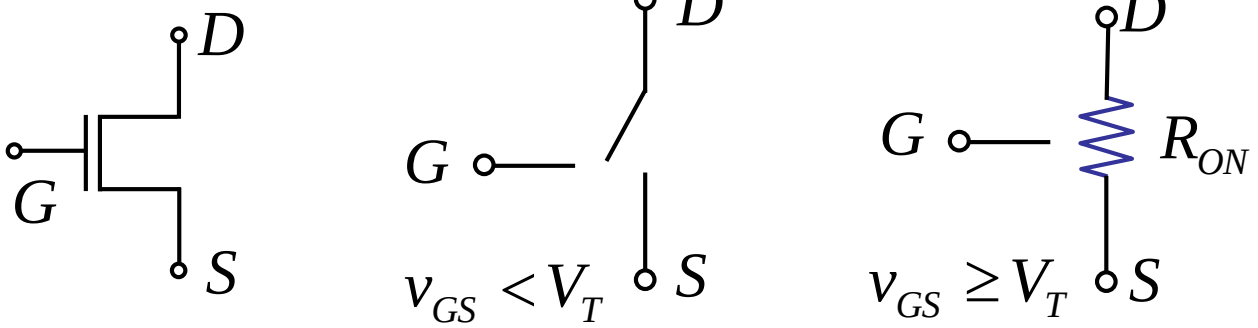




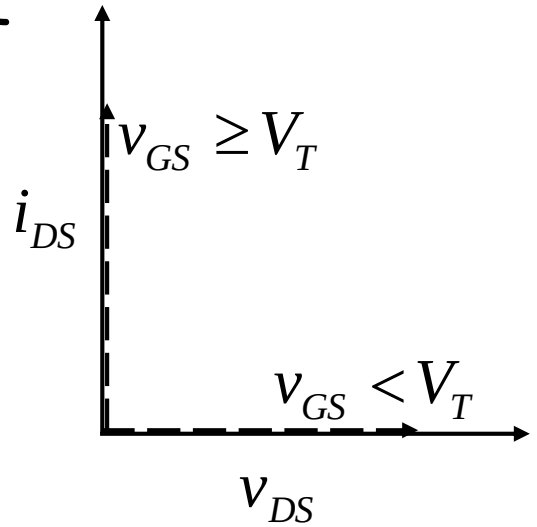


Switch Resistor (SR) Model of MOSFET

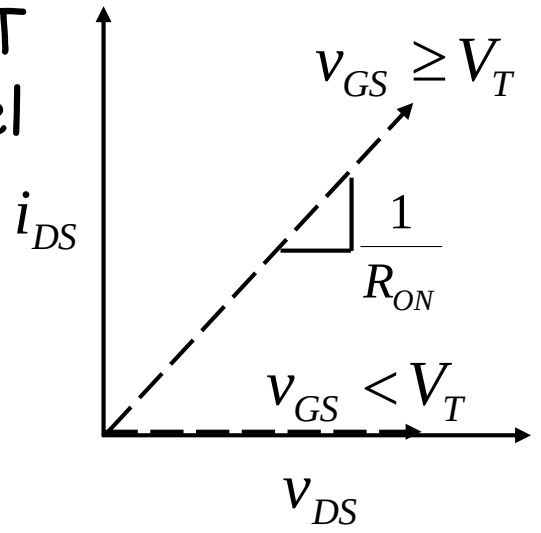
- When MOSFET switch is turned on, there is resistance
- For example, $R_{ON} = 1k\Omega$



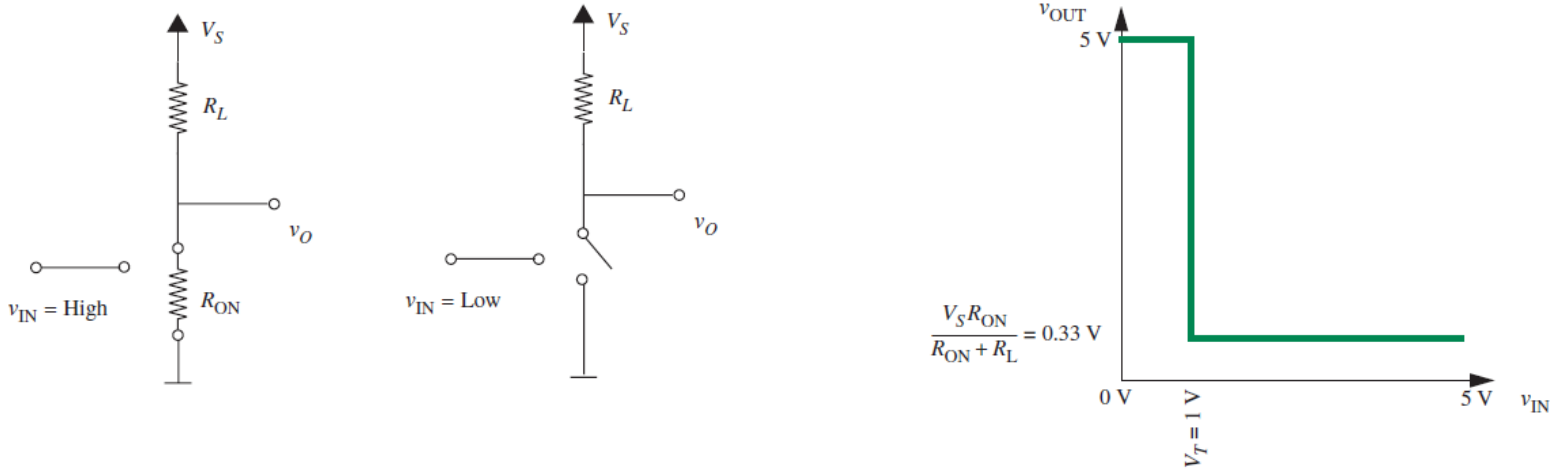
MOSFET
S model



MOSFET
SR model



What Determines Resistor Value in Inverter?



- When v_{IN}=High, $v_{OUT} = V_S \frac{R_{ON}}{R_{ON}+R_L}$
- If $V_S = 5V, V_T = 1V, R_{ON} = 1k\Omega, R_L = 14k\Omega$, $v_{OUT} = 0.33V$

Pull-up and Pull-down Resistors